

DN8643S

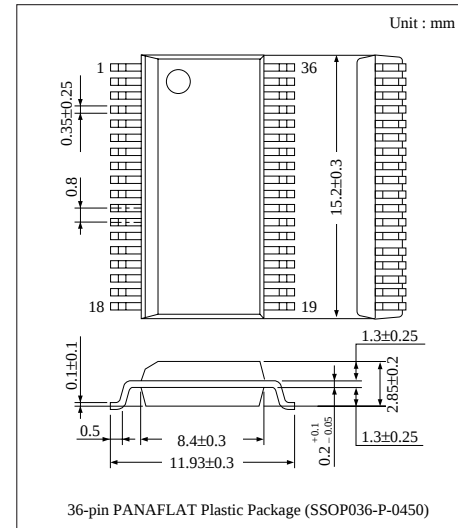
24-bit Shift Register Latch Driver IC

Overview

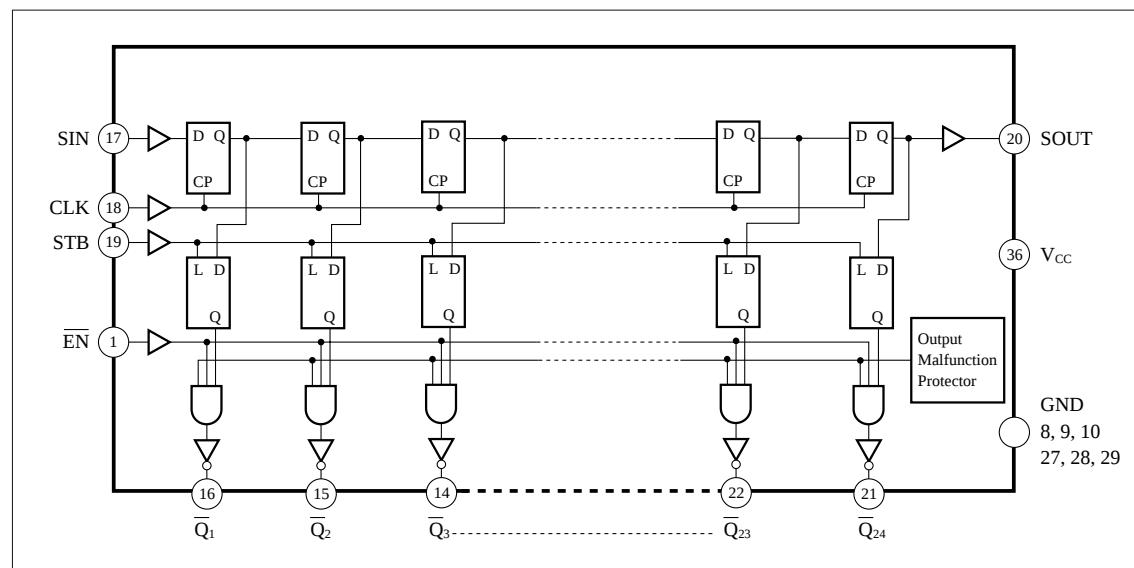
The DN8643S is an IC which incorporates a 24-bit shift register and a latch driver to meet high-speed operation, low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the serial-in and serial-out/parallel-out functions are incorporated, the 24-step shift register block and latch block are composed of CMOS, and the 24-step parallel driver block is bipolar.

Features

- Serial-in and serial-out/parallel-out
- Cascade connection allowed
- Built-in output malfunctioning preventive circuit
- Low current at standby $I_{CC} \leq 100\mu A$
- High-breakdown, large current drive type output steps
Breakdown : 30V
Output current : 120mA
- Surface mountable USONF-36D package (pin pitch : 0.8mm)



Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)			
Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	0 to 7	V
Output voltage	V _O	0 to 30	V
Output current	I _O	120	mA
Power dissipation	P _D	1.3 *	W
Operating ambient temperature	T _{opr}	−20 to + 75	°C
Storage temperature	T _{stg}	−55 to + 125	°C

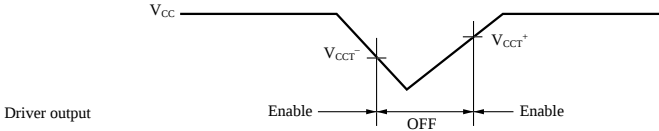
* When mounting onto the PCB, power dissipation is reduced at a rate of 10.4mW/°C from Ta=25°C

■ Recommended Operating Range (Ta=25°C)							
Parameter		Symbol	Condition	mim	typ	max	Unit
Supply voltage		V _{CC}		4	5	6	V
Output voltage		V _O		—	—	30	V
Output current *		I _O		—	—	100	mA
Clock frequency		f _{CLK}	Input Duty 40 to 60%	—	—	10	MHz
Input pulse width	CLK	t _w		40	—	—	ns
	STB			40	—	—	ns
Setup time	SIN	t _{su}		30	—	—	ns
	STB			40	—	—	ns
Hold time	SIN	t _h		20	—	—	ns
	STB			0	—	—	ns
Clock pulse rise time		t _r		—	—	500	ns
Clock pulse fall time		t _f		—	—	500	ns

* An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.

■ Electrical Characteristics (Ta=25°C)						
Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V _{IH}	V _{CC} =4 to 6V	0.7V _{CC}	—	V _{CC}	V
	V _{IL}		0	—	0.3V _{CC}	V
Input current	I _{IH}	V _{IH} =5V	—	—	25	μA
	I _{IL}	V _{IL} =0V	—	—	−25	μA
Output voltage	V _{OH}	I _O = −1μA	4.9	—	—	V
	V _{OL}	I _O =1μA	—	—	0.1	V
Output current	I _{OH}	V _{OH} =4.5V	−4	—	—	mA
	I _{OL}	V _{OL} =0.4V	4	—	—	mA
Output saturation voltage	V _{CE (sat) 1}	I _{OL} =100mA	—	—	0.4	V
	V _{CE (sat) 2}	I _{OL} =80mA	—	—	0.35	V
Output leakage current	I _{OLK1}	V _O =30V (output OFF)	—	—	50	μA
	I _{OLK2}	V _O =15V (output Off)	—	—	25	μA
Supply current	I _{CC1}	Total driver output OFF	—	—	100	μA
	I _{CC2}	Driver output 1 circuit ON	—	—	5	mA
Output malfunctioning preventive circuit operating voltage *	V _{CCT} ⁺		2.9	—	3.9	V
	V _{CCT} [−]		2.6	—	3.6	V

* Output malfunctioning preventive circuit operating voltage timing chart

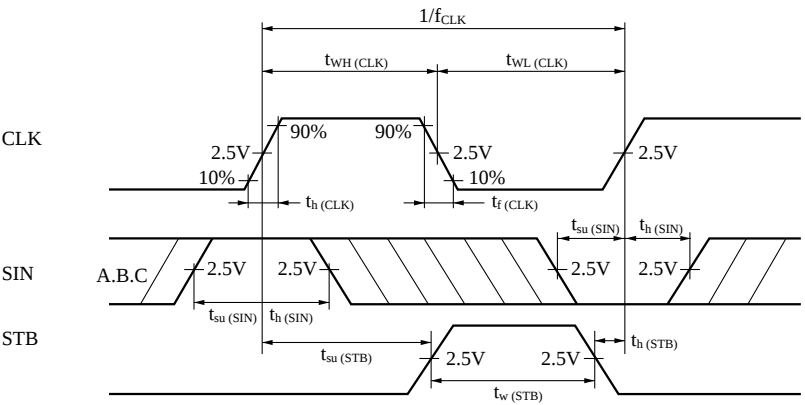


■ Switching Characteristics (Ta=25°C)

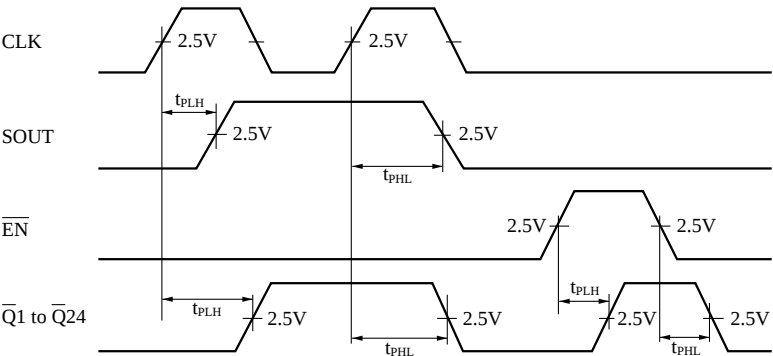
Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	f _{max}	CLK			10	—	—	MHz
Propagation delay time	t _{PLH}	CLK	SOUT	V _{CC} =5V C _L =15pF	—	—	100	ns
	t _{PHL}				—	—	100	ns
	t _{PLH}	CLK	Q _n	V _{CC} =5V R _L =100Ω C _L =15pF	—	—	2	μs
	t _{PHL}				—	—	0.5	μs
	t _{PLH}	EN	Q _n		—	—	2	μs
	t _{PHL}				—	—	0.5	μs

■ Timing Chart

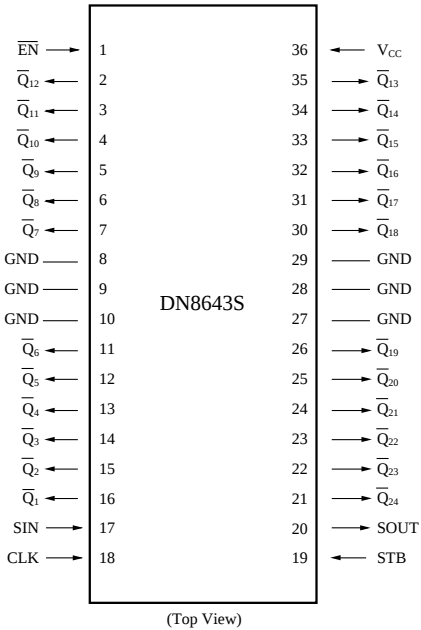
1. Input Timing



2. Propagation Delay Time



■ Pin Assignments



■ Functions Table

Input				Driver output		SOUT
CLK	$\overline{\text{EN}}$	STB	SIN	$\overline{\text{Q}}_1$	$\overline{\text{Q}}_n$	
↑	H	×	×	H	H	Q'_{23}
↓	H	×	×	H	H	nc
↑	L	L	×	nc	nc	Q'_{23}
↑	L	H	L	H	$\overline{\text{Q}}_{n-1}$	Q'_{23}
↑	L	H	H	L	$\overline{\text{Q}}_{n-1}$	Q'_{23}
↓	L	H	×	nc	nc	nc

Note) H=High level, L=Low level, × = Either “H” or “L” will do, ↑ = Transition from “H” or “L” , ↓ = Transition from “H” to “L” , nc=No change, Q'_{23} =Status of the 23rd shift register