2 MEG x 8, 1 MEG x 18, 512K x 36
1.8V VDD, HSTL, DDRIIb2 SRAM

18Mb DDRII CIO SRAM 2-Word Burst

MT57W2MH8B
MT57W1MH18B
MT57W512H36B

FEATURES

- 18Mb Density (2 Meg x 8, 1 Meg x 18, 512K x 36)
- DLL circuitry for wide-output, data valid window and future frequency scaling
- Pipelined, double-data rate operation
- Common data input/output bus
- Fast clock to valid data times
- Full data coherency, providing most current data
- Two-tick burst for low DDR transaction size
- Permits up to one new data request per clock cycle
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time and clock skew matching—clock and data delivered together to receiving device
- Simple control logic for easy depth expansion
- Internally self-timed, registered writes
- +1.8V core and HSTL I/O
- Clock-stop capability with µs restart
- 13 x 15mm, 1mm pitch, 11 x 15 grid FBGA package
- User programmable impedance output
- JTAG boundary scan

OPTIONS / MARKING

- Clock Cycle Timing

3ns (333 MHz)	-3
3.3ns (300 MHz)	-3.3
4ns (250 MHz)	-4
5ns (200MHz)	-5
6ns (167 MHz)	-6
7.5ns (133 MHz)	-7.5

- Configurations

2 Meg x 8	MT57W2MH8B
1 Meg x 18	MT57W1MH18B
512K x 36	MT57W512H36B

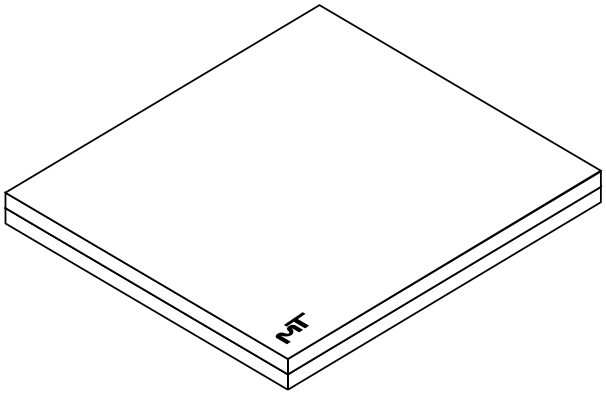
- Package

165-ball, 13mm x 15mm FBGA	F

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT57W2MH8BF-xx	2 Meg x 8, DDRIIb2 FBGA
MT57W1MH18BF-xx	1 Meg x 18, DDRIIb2 FBGA
MT57W512H36BF-xx	512K x 36, DDRIIb2 FBGA

165-BALL FBGA



GENERAL DESCRIPTION

The Micron® DDRII (Double Data Rate) synchronous, pipelined, burst SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process. The DDR SRAM integrates an SRAM core with advanced synchronous peripheral circuitry and a burst counter. All synchronous inputs pass through registers controlled by an input clock pair (K and K#) and are latched on the rising edge of K and K#. The synchronous inputs include all addresses, all data inputs, active LOW load (LD#), read/write (R/W#), and active LOW byte writes or nybble writes (BWx# or NWx#). Write data is registered on the rising edges of both K and K#. Read data is driven on the rising edge of C and C# if provided, or on the rising edge of K and K#, if C and C# are not provided.

Asynchronous inputs include impedance match (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the output data clocks C and C#, eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

Additional write registers are incorporated to enhance pipelined WRITE cycles and reduce READ-to-WRITE turnaround time. WRITE cycles are self-timed.

GENERAL DESCRIPTION (continued)

Four pins are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK), and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use 1.8V I/O levels to shift data during this testing mode of operation.

The device can be used in HSTL systems by supplying an appropriate reference voltage (VREF). The device is ideally suited for applications requiring very rapid data transfer by operation in data-doubled mode. The device is also ideal in applications requiring the cost benefits of pipelined CMOS SRAMs and the reduced READ-to-WRITE turnaround times of late write SRAMs.

The SRAM operates from a +1.8V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for cache, network, telecom, DSP, and other applications that benefit from a very wide, high-speed data bus.

Please refer to Micron's Web site (www.micron.com/sram) for the latest data sheet.

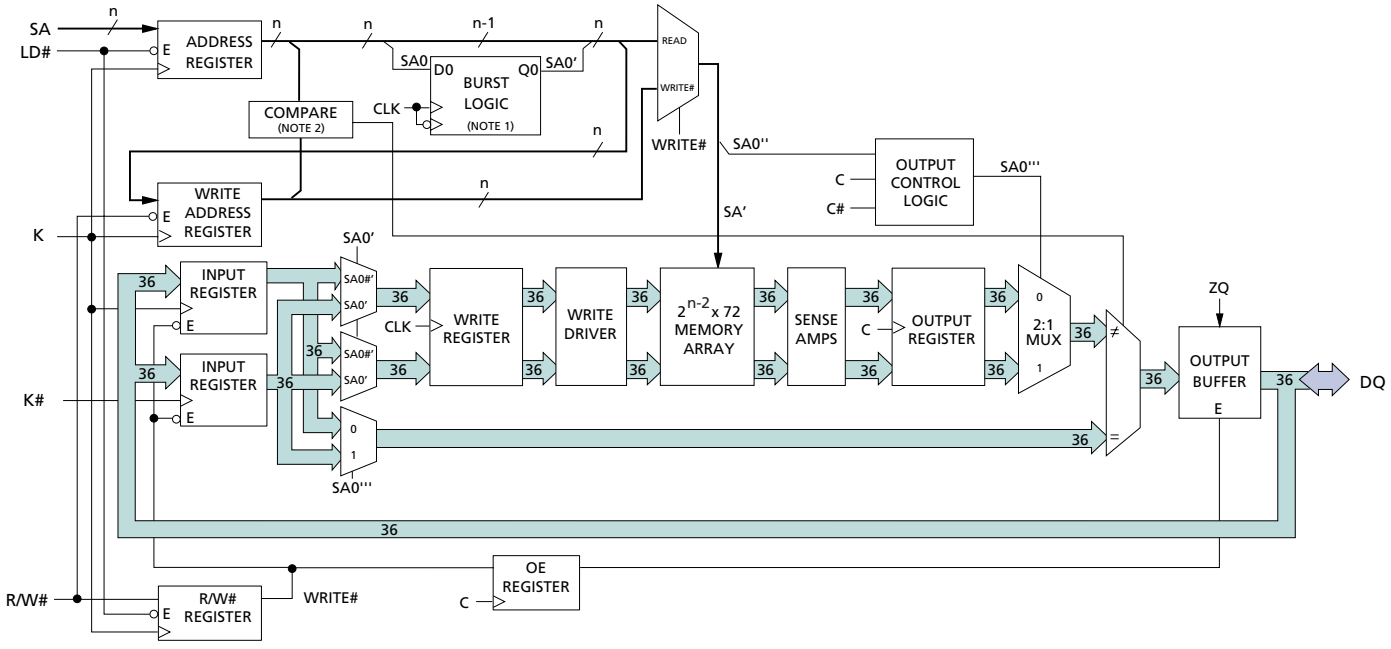
DDR OPERATION

The DDR SRAM enables high performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. At slower frequencies, the DDR SRAM requires a single NO OPERATION (NOP) cycle when transitioning from a READ to a WRITE cycle. At higher frequencies, a second NOP cycle may be required to prevent bus contention. NOP cycles are not required when switching from a WRITE to a READ.

If a read occurs after a WRITE cycle, address and data for the write are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next WRITE cycle occurs. On the first WRITE cycle after the READ(s), the stored data from the earlier WRITE will be written into the SRAM array. This is called a posted write.

A read can be made immediately to an address even if that address was written in the previous cycle. During this READ cycle, the SRAM array is bypassed, and data is

FUNCTIONAL BLOCK DIAGRAM
512K x 36



NOTE:
1. SA0 is toggled at each K and K# rising edge.
2. The compare width is a n-1 bits. The compare is performed only if a WRITE is pending and a READ cycle is requested. If the address matches, data is routed directly to the device outputs, bypassing the memory array.
3. The functional block diagram illustrates simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information. The x8 and x18 operation is the same, with appropriate adjustments of depth and width.
4. n = 19

DDR OPERATION (continued)

read instead from the data register storing the recently written data. This is transparent to the user. This feature facilitates system data coherency.

The DDR SRAM differs in some ways from its predecessor, the Claymore DDR SRAM. Single data rate operation is not supported, hence no SD/DD# pin is provided. Only bursts of two are supported. The need for echo clocks is reduced or eliminated by the two single-ended input clocks (C, C#), although tightly controlled echo clocks (CQ, CQ#) are provided. The SRAM synchronizes its output data to these data clock rising edges, if provided. No differential clocks are used in this device. This clocking scheme provides greater system tuning capability than Claymore SRAMs and reduces the number of input clocks required by the bus master.

PARTIAL WRITE OPERATIONS

BYTE WRITE operations are supported except for x8 devices, in which nybble write is supported. The active LOW write controls, BWx# (NWx#), are registered coincident with their corresponding data. This feature can eliminate the need for some READ-MODIFY-WRITE cycles, collapsing it to a single BYTE/NYBBLE WRITE operation in some instances.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER

The DDR SRAM is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSS. The value of the resistor must be five times the desired impedance. For example, a 350Ω resistor is required for an output impedance of 70Ω. To ensure that output impedance is one fifth the value of RQ (within 10 percent), the range of RQ is 175Ω to 350Ω. Alternately, the ZQ pin can be connected directly to VDD, which will place the device in a minimum impedance mode.

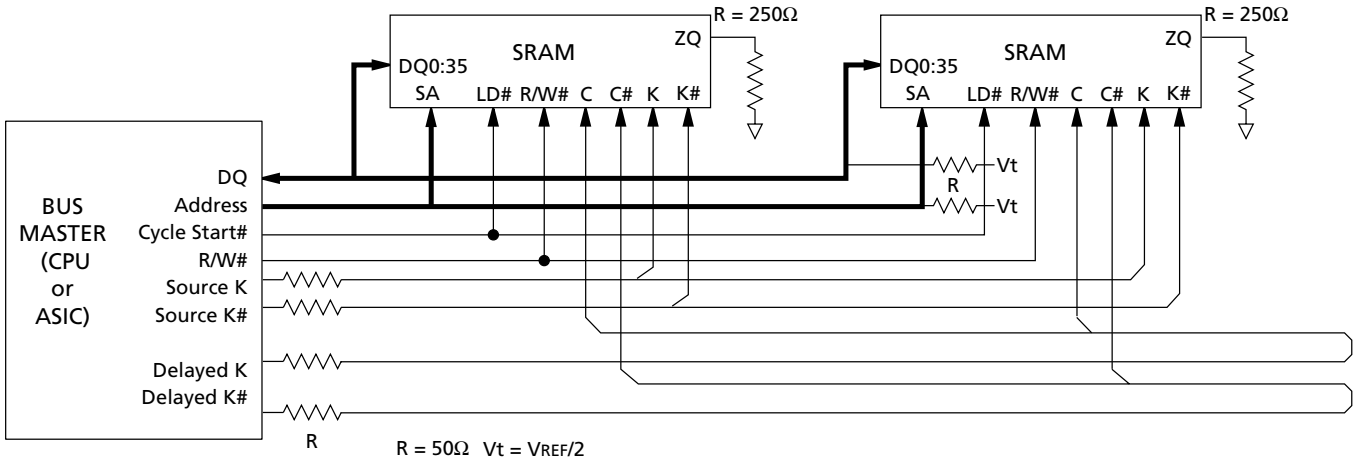
Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. An update of the impedance is transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 50Ω. To guarantee optimum output driver impedance after power-up, the SRAM needs 1,024 cycles to update the impedance. The user can operate the part with fewer than 1,024 clock cycles, but optimal output impedance is not guaranteed.

CLOCK CONSIDERATIONS

This device utilizes internal delay-locked loops for maximum output data valid window. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1,024 clock cycles. Circuitry automatically resets the DLL when the absence of input clock is detected. See Micron Technical Note TN-54-02 for more information on clock DLL start-up procedures.

APPLICATION EXAMPLE



NOTE: In this approach, the second clock pair drives the C and C# clocks, but is delayed such that return data meets data setup and hold times at the bus master.

SINGLE CLOCK MODE

The SRAM can be used with the single K, K# clock pair by tying C and C# HIGH. In this mode the SRAM will use K and K# in place of C and C#. This mode provides the most rapid data output but does not compensate for system clock skew and flight times.

DEPTH EXPANSION

Depth expansion requires replicating the LD# control signal for each bank. All other control signals can be common between banks as appropriate.

2 MEG x 8 PIN ASSIGNMENT (TOP VIEW)
165-BALL FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS/SA*	SA	R/W#	NW1#	K#	NC	LD#	SA	VSS/SA*	CQ
B	NC	NC	NC	SA	NC	K	NW0#	SA	NC	NC	DQ3
C	NC	NC	NC	VSS	SA	SA	SA	VSS	NC	NC	NC
D	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
E	NC	NC	DQ4	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
F	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
G	NC	NC	DQ5	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
H	DLL#	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ1	NC
K	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
L	NC	DQ6	NC	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ0
M	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
N	NC	NC	NC	VSS	SA	SA	SA	VSS	NC	NC	NC
P	NC	NC	DQ7	SA	SA	C	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

*Expansion addresses: 10A for 36Mb, 2A for 72Mb

NOTE: NW0# controls writes to DQ0:DQ3. NW1# controls writes to DQ4:DQ7
Note that 6C is not SA0. The x8 does not permit random start address on the least significant address bit.; SA0 = 0 at the start of each access.

1 MEG x 18 PIN ASSIGNMENT (TOP VIEW)
165-BALL FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS/SA*	SA	R/W#	BW1#	K#	NC	LD#	SA	VSS/SA*	CQ
B	NC	DQ9	NC	SA	NC	K	BW0#	SA	NC	NC	DQ8
C	NC	NC	NC	VSS	SA	SA0	SA	VSS	NC	DQ7	NC
D	NC	NC	DQ10	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
E	NC	NC	DQ11	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ6
F	NC	DQ12	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ5
G	NC	NC	DQ13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
H	DLL#	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ4	NC
K	NC	NC	DQ14	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ3
L	NC	DQ15	NC	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
M	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	DQ1	NC
N	NC	NC	DQ16	VSS	SA	SA	SA	VSS	NC	NC	NC
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

*Expansion addresses: (3A was for 18Mb), 10A for 36Mb, 2A for 72Mb
NOTE: BW0# controls writes to DQ0:DQ8. BW1# controls writes to DQ9:DQ17

512K x 36 PIN ASSIGNMENT (TOP VIEW)
165-BALL FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS/SA*	NC/SA*	R/W#	BW2#	K#	BW1#	LD#	SA	VSS/SA*	CQ
B	NC	DQ27	DQ18	SA	BW3#	K	BW0#	SA	NC	NC	DQ8
C	NC	NC	DQ28	VSS	SA	SA0	SA	VSS	NC	DQ17	DQ7
D	NC	DQ29	DQ19	VSS	VSS	VSS	VSS	VSS	NC	NC	DQ16
E	NC	NC	DQ20	VDDQ	VSS	VSS	VSS	VDDQ	NC	DQ15	DQ6
F	NC	DQ30	DQ21	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ5
G	NC	DQ31	DQ22	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ14
H	DLL#	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	DQ32	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ13	DQ4
K	NC	NC	DQ23	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ12	DQ3
L	NC	DQ33	DQ24	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
M	NC	NC	DQ34	VSS	VSS	VSS	VSS	VSS	NC	DQ11	DQ1
N	NC	DQ35	DQ25	VSS	SA	SA	SA	VSS	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

*Expansion addresses: (9A was for 18Mb), 3A for 36Mb, 10A for 72Mb, 2A for 144Mb

NOTE: BW0# controls writes to DQ0:DQ8. BW1# controls writes to DQ9:DQ17. BW2# controls writes to DQ18:DQ26. BW3# controls writes to DQ27:DQ35.

FBGA BALL DESCRIPTIONS

FBGA BALLS	SYMBOL	TYPE	DESCRIPTION
6C 7C, 8B, 5C, 4B, 9R, 8P, 8R, 7R, 7N, 7P, 7P, 6N, 5R, 5N, 5P, 4P, 4R, 3R, 9A, 3A, 10A, 2A	SA0 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. Balls 9A, 3A, 10A, and 2A are reserved for the next higher-order address inputs on future devices. All transactions operate on a burst-of-two words (one clock period of bus activity). SA0 is used as the lowest order address bit permitting a random starting address within the burst operation. These inputs are ignored when device is deselected.
8A	LD#	Input	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst-of-two data (one clock period of bus activity).
4A	R/W#	Input	Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R/W# is HIGH, WRITE when R/W# is LOW) for the loaded address. R/W# must meet the setup and hold times around the rising edge of K.
7B 7A 5A 5B	BW_# NW_# BW2# BW3#	Input	Synchronous Byte Writes (Nybble Writes on x8): When LOW, these inputs cause their respective byte or nybble to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. See Pin Assignment figures for the signal-to-data relationships.
6B 6A	K K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
6P 6R	C C#	Input	Output Clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C is used as the output timing reference for first output data. The rising edge of C# is used as the output reference for second output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, C and C# must remain HIGH and not be toggled during device operation.
11H	ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to 0.2 x RQ, where RQ is a resistor from this bump to ground. Alternately, this pin can be connected directly to VDD, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
1H	DLL#	Input	DLL DIsable: When LOW, this input causes the DLL to be bypassed for stable, low-frequency operation.
10R 11R	TMS TDI	Input	IEEE 1149.1 Test Inputs: 1.8V I/O levels. These pins may be left not connected if the JTAG function is not used in the circuit.

(continued on next page)

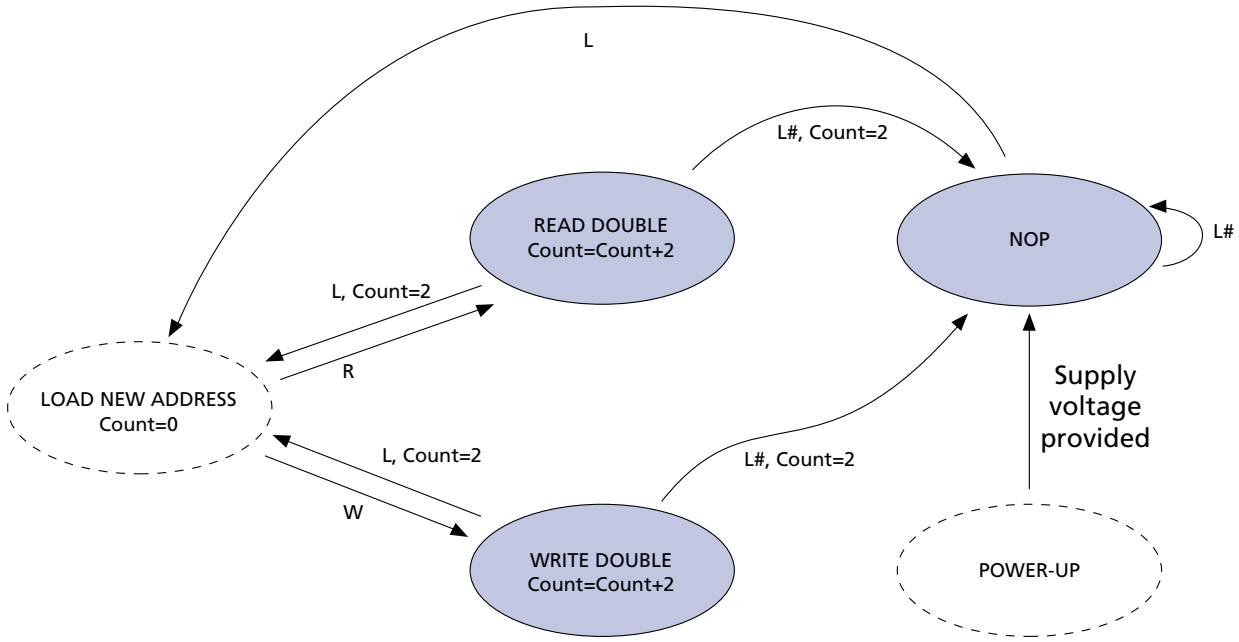
FBGA BALL DESCRIPTIONS (continued)

FBGA BALLS	SYMBOL	TYPE	DESCRIPTION
2R	TCK	Input	IEEE 1149.1 Clock Input: 1.8V I/O levels. This pin must be tied to VSS if the JTAG function is not used in the circuit.
2H, 10H	VREF	Input	HSTL Input Reference Voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers.
11P, 11M, 11L, 11K, 11J, 11F, 11E, 11C, 11B, 10P, 11N, 10M, 10K, 10J, 11G, 10E, 11D, 10C, 3B, 3D, 3E, 3F, 3G, 3K, 3L, 3N, 3P, 2B, 3C, 2D, 2F, 2G, 3J, 2L, 3M, 2N	DQ_	Input/ Output	Synchronous Data IOs: Input data must meet setup and hold times around the rising edges of K and K#. Output data is synchronized to the respective C and C# data clocks or to K and K# if C and C# are tied to HIGH. The x8 device uses DQ0–DQ7. Remaining signals are NC. The x18 device uses DQ0–DQ17. Remaining signals are NC. The x36 device uses DQ0–DQ35. Remaining signals are NC. NC signals are read in the JTAG scan chain as the logic level applied to the ball site.
1A, 11A	CQ#, CQ	Output	Synchronous Echo Clock Outputs: The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tri-states.
1R	TDO	Output	IEEE 1149.1 Test Output: 1.8V I/O level.
5F, 7F, 5G, 7G, 5H, 7H, 5J, 7J, 5K, 7K	VDD	Supply	Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
4E, 8E, 4F, 8F, 4G, 8G, 3H, 4H, 8H, 9H, 4J, 8J, 4K, 8K, 4L, 8L	VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally, 1.5V. 1.8V is also permissible. See DC Electrical Characteristics and Operating Conditions for range.
2A, 10A, 4C, 8C, 4D-8D, 5E-7E, 6F, 6G, 6H, 6J, 6K, 5L-7L, 4M-8M, 4N, 8N	VSS	Supply	Power Supply: GND.
1B, 9-10B, 1-2C, 9C, 1D, 9-10D, 1-2E, 9E, 1F, 9-10F, 1G, 9-10G, 1-2J, 9J, 1-2K, 9K, 1L, 9-10L, 1-2M, 9M, 1N, 9-10N, 1-2P, 9P	NC	—	No Connect: These signals are internally connected and appear in the JTAG scan chain as the logic level applied to the ball sites. These signals may be connected to ground to improve package heat dissipation.

BURST ADDRESS TABLE

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)
X...X0	X...X1
X...X1	X...X0

BUS CYCLE STATE DIAGRAM



NOTE: 1. SA0 is internally advanced in accordance with the burst order table. Bus cycle is terminated after burst count = 2.
2. State transitions: L = (LD# = LOW); L# = (LD# = HIGH); R = (R/W# = HIGH); W = (R/W# = LOW).
3. State machine, control timing sequence is controlled by K.

TRUTH TABLE

(Notes 1–6)

OPERATION	LD#	R/W#	K	DQ	DQ
WRITE Cycle: Load address, input write data on two consecutive K and K# rising edges	L	L	L→H	DIN(A1) at K(t+1)↑	DIN(A2) at K#(t+1)↑
READ Cycle: Load address, read data on two consecutive C and C# rising edges	L	H	L→H	QOUT(A1) at C#(t+1)↑	QOUT(A2) at C(t+2)↑
NOP: No operation	H	X	L→H	High-Z	High-Z
STANDBY: Clock stopped	X	X	Stopped	Previous State	Previous State

BYTE WRITE OPERATION

(Notes 7, 8)

OPERATION	K	K#	BW0#	BW1#
WRITE D0–17 at K rising edge	L→H		0	0
WRITE D0–17 at K# rising edge		L→H	0	0
WRITE D0–8 at K rising edge	L→H		0	1
WRITE D0–8 at K# rising edge		L→H	0	1
WRITE D9–17 at K rising edge	L→H		1	0
WRITE D9–17 at K# rising edge		L→H	1	0
WRITE nothing at K rising edge	L→H		1	1
WRITE nothing at K# rising edge		L→H	1	1

NOTE:
1. X means "Don't Care." H means logic HIGH. L means logic LOW. ↑ means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges, except if C and C# are HIGH, then data outputs are delivered at K and K# rising edges.
3. R/W# and LD# must meet setup/hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification. A1 refers to the address input during a WRITE or READ cycle. A2 refers to the next internal burst address in accordance with the burst sequence.
6. It is recommended that K = K# = C = C# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.
8. This table illustrates operation for x18 devices. The x36 device operation is similar, except for the addition of BW2# (controls D18–D26) and BW3# (controls D27–D35). The x8 device operation is similar, except that NW0# controls D0–D3, NW1# controls D4–D7.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD Supply
Relative to VSS ..... -0.5V to +2.9V
Voltage on VDDQ Supply
Relative to VSS ..... -0.5V to VDD
VIN ..... -0.5V to VDD + 0.5V
Storage Temperature ..... -55°C to +125°C
Junction Temperature** ..... +125°C
Short Circuit Output Current ..... ±70mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C; +1.7V ≤ VDD ≤ +1.9V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	VREF + 0.1	VDDQ + 0.3	V	3, 4
Input Low (Logic 0) Voltage		VIL	-0.3	VREF - 0.1	V	3, 4
Clock Input Signal Voltage		VIN	-0.3	VDDQ + 0.3	V	3, 4
Input Leakage Current	0V ≤ VIN ≤ VDDQ	ILI	-5	5	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (Q)	ILO	-5	5	µA	
Output High Voltage	|IOH| ≤ 0.1mA	VOH (LOW)	VDDQ - 0.2	VDDQ	V	3, 5, 7
	Note 1	VOH	VDDQ/2 - 0.08	VDDQ/2 + 0.08	V	3, 5, 7
Output Low Voltage	IOL ≤ 0.1mA	VOL (LOW)	VSS	0.2	V	3, 5, 7
	Note 2	VOL	VDDQ/2 - 0.08	VDDQ/2 + 0.08	V	3, 5, 7
Supply Voltage		VDD	1.7	1.9	V	3
Isolated Output Buffer Supply		VDDQ	1.4	VDD	V	3, 6
Reference Voltage		VREF	0.68	0.95	V	3

NOTE:
1. Outputs are impedance-controlled. | IOH | = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
2. Outputs are impedance-controlled. IOL = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
3. All voltages referenced to VSS (GND).
4. Overshoot: VIH (AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
   Undershoot: VIL (AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ VDDQ + 0.3V and VDD ≤ 2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. Control input signals may not have pulse widths less than ^{t}KHKL (MIN) or operate at cycle rates less than ^{t}KHKH (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. Output buffer supply can be set to 1.5V or 1.8V nominal ±0.1V with appropriate derating of AC timing parameters. Consult factory for further information.
7. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

IDD OPERATING CONDITIONS AND MAXIMUM LIMITS

(+20°C ≤ T_J ≤ +110°C; VDD = MAX unless otherwise noted)

				MAX							
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-3**	**-3.3**	**-4**	**-5**	**-6**	**-7.5**	**UNITS**	**NOTES**
Operating Supply Current: DDR	All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKHKH (MIN); Outputs open	IDD (x8,18) IDD (x36)	TBD TBD	525 710	475 640	400 545	330 445	280 380	235 310	mA	1, 2, 3
Standby Supply Current: NOP	tKHKH = tKHKH (MIN); Device in NOP state; All addresses/data static	ISB1 (x8,18) ISB1 (x8,18)	TBD TBD	255 265	235 240	200 210	170 180	150 160	125 135	mA	2, 4
Output Supply Current: DDR (Information only)	CL = 15pF	IDDQ (x8) IDDQ (x18) IDDQ (x36)		42 95 189	38 85 170	32 71 142	25 57 113	21 47 95	17 38 76	mA	5

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	CI	4	5	pF	6
Input, Output Capacitance (D, Q)		CO	6	7	pF	6
Clock Capacitance		CCK	5	6	pF	6

THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer, printed circuit board	θ_{JA}	25	°C/W	6, 7
Junction to Case (Top)		θ_{JC}	10	°C/W	6
Junction to Pins (Bottom)		θ_{JB}	12	°C/W	6, 8

NOTE:
1. IDD is specified with no output current. IDD is linear with frequency. Typical value is measured at 6ns cycle time.
2. Typical values are measured at VDD = 1.8V, VDDQ = 1.5V and temperature = 25°C.
3. Operating supply currents are measured at 100% bus utilizaton.
4. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
5. Average I/O current and power is provided for information purposes only and is not tested. Calculation assumes that all outputs are loaded with CL (in farads), f = input clock frequency, half of outputs toggle at each transition (for example, n=9 for x18 device), VDDQ=1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is: $P = 0.5 \times nf [C_L + 2C_O] V_{DD}Q^2$. Average $I_{DD}Q = nf [C_L + C_O] V_{DD}Q$.
6. This parameter is sampled.
7. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
8. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.

AC ELECTRICAL CHARACTERISTICS

(Notes 1–5, 7, 8); (+20°C ≤ T_J ≤ +110°C; +1.7V ≤ VDD ≤ +1.9V)

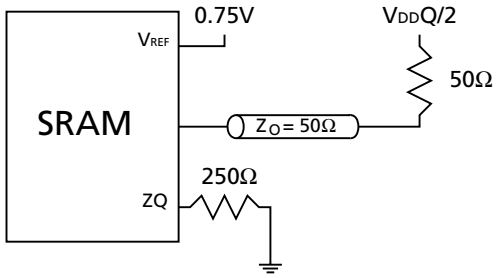
DESCRIPTION	SYMBOL	-3		-3.3		-4		-5		-6		-7.5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock															
Average clock cycle time (K, K#, C, C#)	tKHKH	3.00	3.60	3.30	4.00	4.00	5.00	5.00	6.00	6.00	7.50	7.50	8.00	ns	10
Clock Phase Jitter (K, K#, C, C#)	tKC var		0.20		0.20		0.20		0.20		0.20		0.20	ns	6
Clock HIGH time (K, K#, C, C#)	tKHKL	1.20		1.32		1.60		2.00		2.40		3.00		ns	
Clock LOW time (K, K#, C, C#)	tKLKH	1.20		1.32		1.60		2.00		2.40		3.00		ns	
Clock to clock# (K↑→K#↑, C↑→C#↑) at tKHKH minimum	tKHK#H	1.35		1.49		1.80		2.20		2.70		3.38		ns	
Clock to clock# (K#↑→K↑, C#↑→C↑) at tKHKH minimum	tK#HKH	1.35		1.49		1.80		2.20		2.70		3.38		ns	
Clock to data clock (K↑→C↑, K#↑→C#↑)	tKHCH	0.00	1.30	0.00	1.45	0.00	1.80	0.00	2.30	0.00	2.80	0.00	3.55	ns	
DLL lock time (K, C)	tKC lock	1024		1024		1024		1024		1024		1024		cycles	7
K static to DLL reset	tKC reset	30		30		30		30		30		30		ns	
Output Times															
C, C# HIGH to output valid	tCHQV		0.27		0.29		0.35		0.38		0.40		0.40	ns	
C, C# HIGH to output hold	tCHQX	-0.27		-0.29		-0.35		-0.38		-0.40		-0.40		ns	
C, C# HIGH to echo clock valid	tCHCQV		0.25		0.27		0.33		0.36		0.38		0.38	ns	
C, C# HIGH to echo clock hold	tCHCQX	-0.25		-0.27		-0.33		-0.36		-0.38		-0.38		ns	
CQ, CQ# HIGH to output valid	tCQHQV		0.27		0.29		0.35		0.38		0.40		0.40	ns	9
CQ, CQ# HIGH to output hold	tCQHQX	-0.27		-0.29		-0.35		-0.38		-0.40		-0.40		ns	9
C HIGH to output High-Z	tCHQZ		0.27		0.29		0.35		0.38		0.40		0.40	ns	
C HIGH to output Low-Z	tCHQX1	-0.27		-0.29		-0.35		-0.38		-0.40		-0.40		ns	
Setup Times															
Address valid to K rising edge	tAVKH	0.40		0.40		0.50		0.60		0.70		0.80		ns	2
Control inputs valid to K rising edge	tIVKH	0.40		0.40		0.50		0.60		0.70		0.80		ns	2
Data-in valid to K, K# rising edge	tDVKH	0.30		0.33		0.40		0.50		0.60		0.75		ns	2
Hold Times															
K rising edge to address hold	tKHAX	0.40		0.40		0.50		0.60		0.70		0.80		ns	2
K rising edge to control inputs hold	tKHIX	0.40		0.40		0.50		0.60		0.70		0.80		ns	2
K, K# rising edge to data-in hold	tKHDX	0.30		0.33		0.40		0.50		0.60		0.75		ns	2

NOTE:
1. This parameter is sampled.
2. This is a synchronous device. All addresses, data, and control lines must meet the specified setup and hold times for all latching clock edges.
3. Test conditions as specified with the output loading as shown in Figure 1 unless otherwise noted.
4. Control input signals may not be operated with pulse widths less than tKHKL (MIN).
5. If C, C# are tied HIGH, K, K# become the references for C, C# timing parameters.
6. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
7. VDD slew rate must be less than 0.1VDC per 50ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
8. VDDQ is +1.5VDC.
9. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.
10. The device will operate at clock frequencies slower than tKHKH MAX. See Micron Technical Note TN-54-02 for more information.

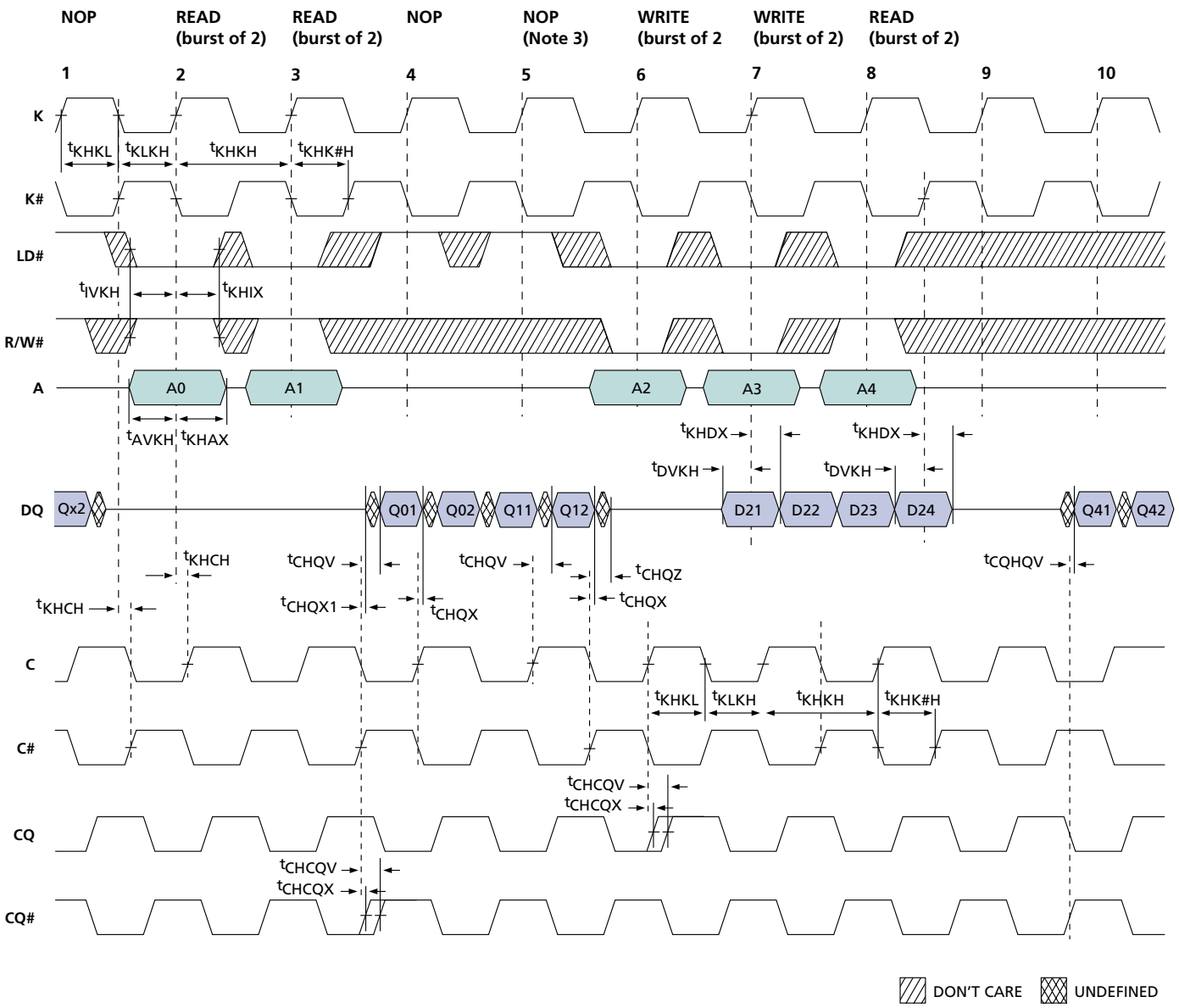
AC TEST CONDITIONS

Input pulse levels	0.25V to 1.25V
Input rise and fall times	0.3ns
Input timing reference levels	0.75V
Output reference levels	VDDQ/2
ZQ for 50Ω impedance	250Ω
Output load	See Figure 1

Figure 1
Output Load Equivalent



READ/WRITE TIMING



NOTE: 1. Q01 refers to output from address A0. Q02 refers to output from the next internal burst address following A0, etc.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The DDR SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1, fully-compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

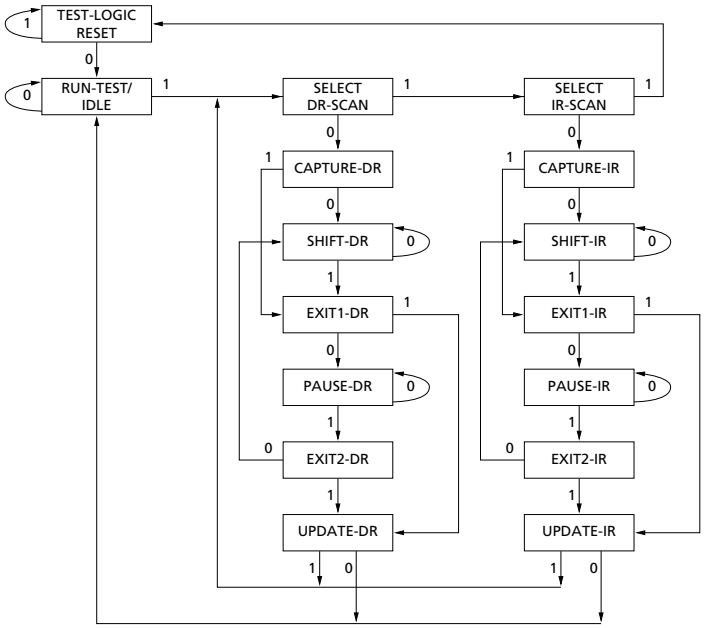
TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to input information serially into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 2. TDI is pulled up internally and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 3.)

Figure 2
TAP Controller State Diagram



NOTE: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TEST DATA-OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 2.) The output changes on the falling edge of TCK. TDO is connected to the least-significant bit (LSB) of any register. (See Figure 3.)

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is loaded serially into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Three-bit instructions can be loaded serially into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in Figure 3. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

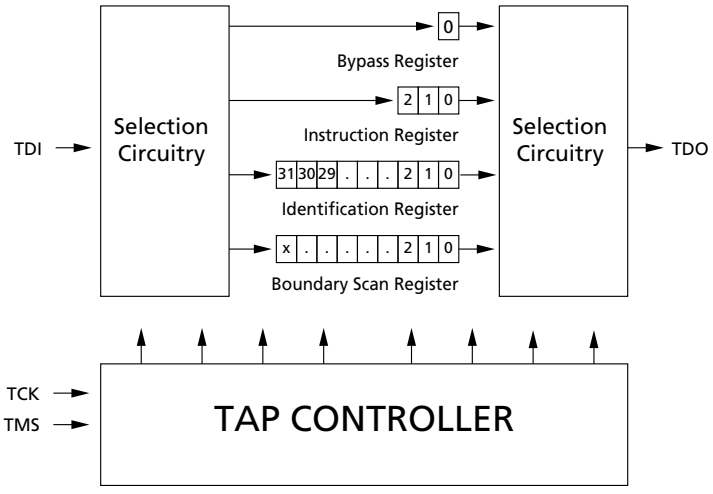
BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins. The SRAM has a 69-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the pins on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Figure 3
TAP Controller Block Diagram



x = 69 for the x8, x18, and x36 configurations.

IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

OVERVIEW

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, hence this device is not IEEE 1149.1 compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the SRAM outputs in a High-Z state, CQ, CQ#.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state, including CQ, CQ#.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins is captured in the boundary scan register.

The user must be aware that the TAP-controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

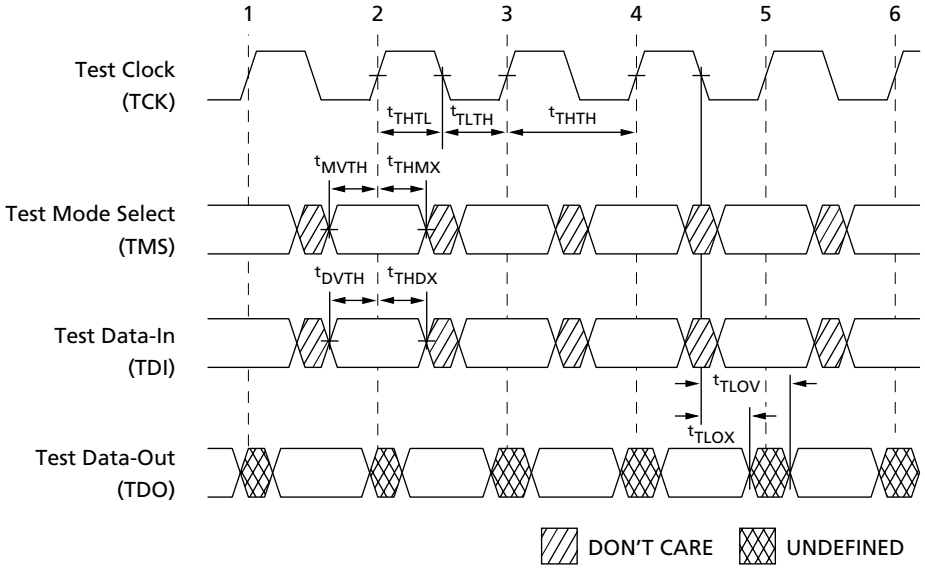
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instruction are not implemented but are reserved for future use. Do not use these instructions.

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) (+20°C ≤ T_J ≤ +100°C, +2.4V ≤ V_{DD} ≤ +2.6V)

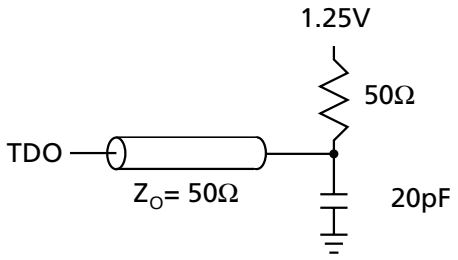
DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 4.

TAP AC TEST CONDITIONS

Input pulse levels	VSS to 1.8V
Input rise and fall times	1ns
Input timing reference levels	0.9V
Output reference levels	0.9V
Test load termination supply voltage	0.9V

Figure 4
TAP AC Output Load Equivalent



TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+20°C ≤ T_J ≤ +110°C, +1.7V ≤ VDD ≤ +1.9V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.3	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.5	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ	ILO	-5.0	5.0	µA	
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	1
Output Low Voltage	IOLT = 2mA	VOL2		0.4	V	1
Output High Voltage	|IOHC| = 100µA	VOH1	1.6		V	1
Output High Voltage	|IOHT| = 2mA	VOH2	1.4		V	1

NOTE: 1. All voltages referenced to VSS (GND).
2. Overshoot: VIH (AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
Undershoot: VIL (AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
Power-up: VIH ≤ +1.9V and VDD ≤ 1.7V for t ≤ 200ms
During normal operation, VDDQ must not exceed VDD. Control input signals (such as R#, W#, etc.) may not have pulse widths less than ^{t}KHKL (MIN) or operate at frequencies exceeding ^{f}KF (MAX).

IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	ALL DEVICES	DESCRIPTION
REVISION NUMBER (31:29)	000	Version number.
DEVICE ID (28:12)	00def0wx0t0q0b0s0	def = 001 for 18Mb density wx = 11 for x36, 10 for x18, 01 for x8 t = 1 for DLL version, 0 for non-DLL version q = 1 for QDR, 0 for DDR b = 1 for 4-word burst, 0 for 2-word burst s = 1 for separate I/O, 0 for common I/O
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE (x18)
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

INSTRUCTION CODES

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect SRAM operations. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

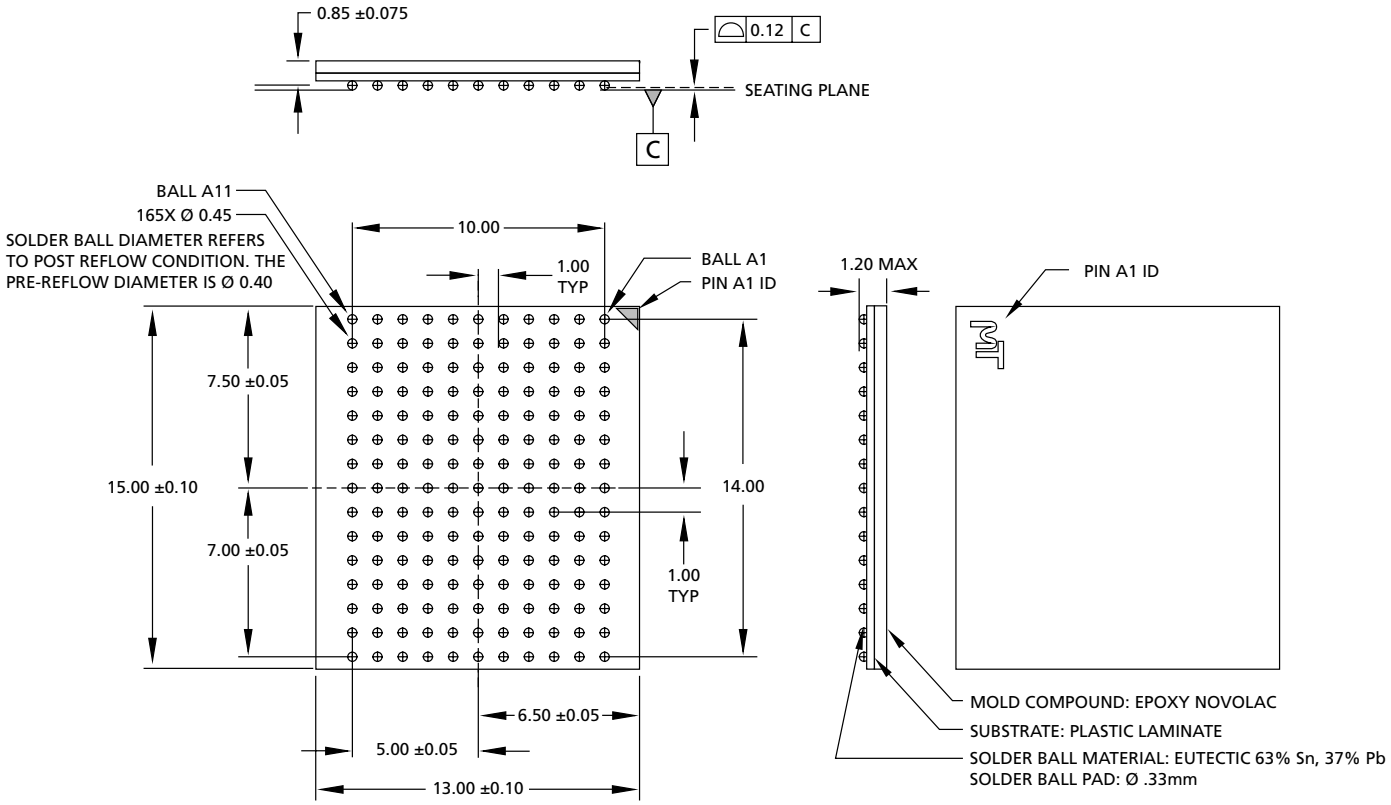
BOUNDARY SCAN (EXIT) ORDER

BIT#	FBGA BALL
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

BIT#	FBGA BALL
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

BIT#	FBGA BALL
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R

165-BALL FBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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REVISION HISTORY

Rev. 2, Pub. 11/01, ADVANCE 11/01

- Changed AC timing