# MC74LVX257

# Quad 2-Channel Multiplexer with 3-State Outputs

The MC74LVX257 is an advanced high speed CMOS quad 2−channel multiplexer fabricated with silicon gate CMOS technology.

It consists of four 2−input digital multiplexers with common select (S) and enable ($\overline{OE}$) inputs. When ($\overline{OE}$) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed: $t_{PD}$ = 4.5 ns (Typ) at $V_{CC}$ = 3.3 V
- Low Power Dissipation: $I_{CC}$ = 4 μA (Max) at $T_A$ = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: FETs = 100; Equivalent Gates = 25
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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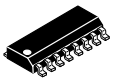
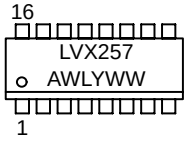
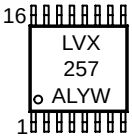
**MARKING DIAGRAMS**



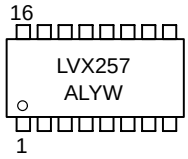
**SOIC−16**
**D SUFFIX**
**CASE 751B**




**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




**SOEIAJ−16**
**M SUFFIX**
**CASE 966**




| | | |
|---|---|---|
| A | = | Assembly Location |
| WL or L | = | Wafer Lot |
| Y | = | Year |
| WW or W | = | Work Week |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

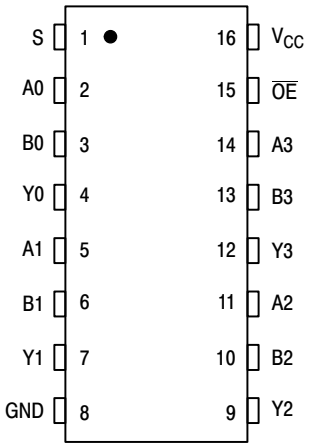



**Figure 1. Pin Assignment**

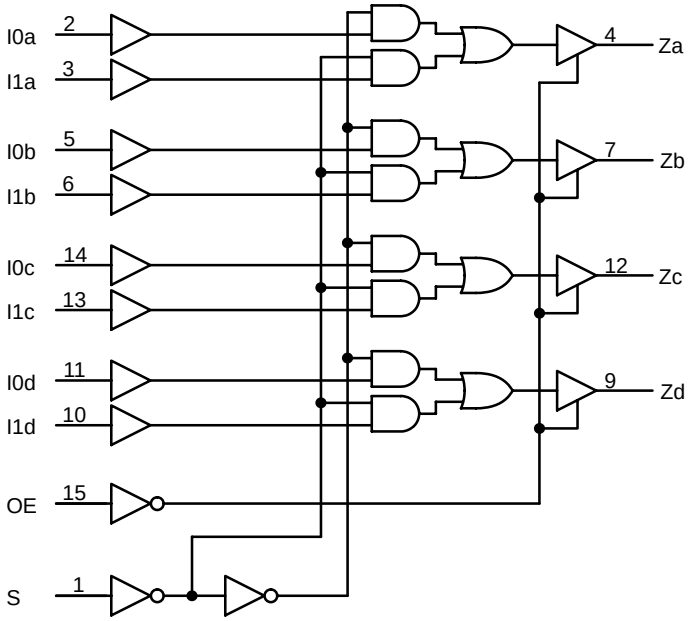



**Figure 2. Expanded Logic Diagram**

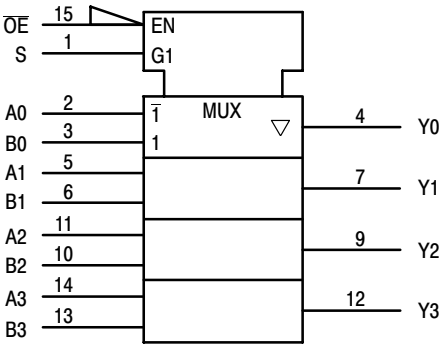



**Figure 3. IEC Logic Symbol**

**FUNCTION TABLE**

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | S | Y0 − Y3 |
| H | X | Z |
| L | L | A0−A3 |
| L | H | B0−B3 |

A0 − A3, B0 − B3 = the levels of the respective Data−Word Inputs.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74LVX257D | SOIC−16 | 48 Units / Rail |
| MC74LVX257DG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74LVX257DR2 | SOIC−16 | 2500 Tape & Reel |
| MC74LVX257DR2G | SOIC−16 (Pb−Free) | 2500 Tape & Reel |
| MC74LVX257DT | TSSOP−16* | 96 Units / Rail |
| MC74LVX257DTR2 | TSSOP−16* | 2500 Tape & Reel |
| MC74LVX257M | SOEIAJ−16 | 50 Units / Rail |
| MC74LVX257MEL | SOEIAJ−16 | 2000 Tape & Reel |
| MC74LVX257MELG | SOEIAJ−16 (Pb−Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | Digital Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | Input Diode Current | | −20 | mA |
| $I_{OK}$ | Output Diode Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±75 | mA |
| $P_D$ | Power Dissipation in Still Air | SOIC Package<br>TSSOP | 200<br>180 | mW |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | >2000<br>>200<br>>2000 | V |
| $I_{LATCHUP}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 4) | ±300 | mA |
| $\theta_{JA}$ | Thermal Resistance, Junction−to−Ambient | SOIC Package<br>TSSOP | 143<br>164 | °C/W |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 2.0 | 3.6 | V |
| $V_{IN}$ | DC Input Voltage | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range, all Package Types | −40 | 85 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Time $V_{CC}$ = 3.3 V ± 0.3 V | 0 | 100 | ns/V |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

**DC CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | −40°C ≤ $T_A$ ≤ 85°C Min | −40°C ≤ $T_A$ ≤ 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High−Level Input Voltage | | 2.0<br>3.0<br>3.6 | 0.75 $V_{CC}$<br>0.7 $V_{CC}$<br>0.7 $V_{CC}$ | | | 0.75 $V_{CC}$<br>0.7 $V_{CC}$<br>0.7 $V_{CC}$ | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 2.0<br>3.0<br>3.6 | | | 0.25 $V_{CC}$<br>0.3 $V_{CC}$<br>0.3 $V_{CC}$ | | 0.25 $V_{CC}$<br>0.3 $V_{CC}$<br>0.3 $V_{CC}$ | V |
| $V_{OH}$ | High−Level Output Voltage | $I_{OH}$ = −50 μA<br>$I_{OH}$ = −50 μA<br>$I_{OH}$ = −4 mA | 2.0<br>3.0<br>3.0 | 1.9<br>2.9<br>2.58 | 2.0<br>3.0 | | 1.9<br>2.9<br>2.48 | | V |
| $V_{OL}$ | Low−Level Output Voltage | $I_{OL}$ = 50 μA<br>$I_{OL}$ = 50 μA<br>$I_{OL}$ = 4 mA | 2.0<br>3.0<br>3.0 | | 0.0<br>0.0 | 0.1<br>0.1<br>0.36 | | 0.1<br>0.1<br>0.44 | V |
| $I_{OZ}$ | Maximum 3−State Leakage Current | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | 3.6 | | | ±0.1 | | ±1.0 | μA |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 0 to 3.6 | | | ±0.1 | | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per package) | $V_{IN}$ = $V_{CC}$ or GND | 3.6 | 1.0 | 1.0 | 2.0 | | 40 | μA |

**AC ELECTRICAL CHARACTERISTICS** Input $t_r$ = $t_f$ = 3.0 ns

| Symbol | Parameter | Test Conditions | | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | −40°C ≤ $T_A$ ≤ 85°C Min | −40°C ≤ $T_A$ ≤ 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, A or B to Y | $V_{CC}$ = 2.7 V | $C_L$ = 15pF<br>$C_L$ = 50pF | | 6.5<br>9.5 | 10.0<br>14.0 | 1.0<br>1.0 | 15.0<br>18.5 | ns |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | $C_L$ = 15pF<br>$C_L$ = 50pF | | 4.5<br>7.5 | 8.0<br>12.0 | 1.0<br>1.0 | 10.0<br>13.5 | |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, S to Y | $V_{CC}$ = 2.7 V | $C_L$ = 15pF<br>$C_L$ = 50pF | | 8.0<br>10.5 | 12.0<br>15.5 | 1.0<br>1.0 | 17.0<br>20.0 | ns |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | $C_L$ = 15pF<br>$C_L$ = 50pF | | 6.0<br>8.5 | 10.0<br>13.5 | 1.0<br>1.0 | 12.0<br>15.5 | |
| $t_{PZL}$,<br>$t_{PZH}$ | Maximum Output Enable, Time, $\overline{OE}$ to Y | $V_{CC}$ = 2.7 V<br>$R_L$ = 1 kΩ | $C_L$ = 15pF<br>$C_L$ = 50pF | | 7.5<br>10.5 | 11.5<br>15.0 | 1.0<br>1.0 | 16.5<br>18.0 | ns |
| | | $V_{CC}$ = 3.3 V ± 0.3 V<br>$R_L$ = 1 kΩ | $C_L$ = 15pF<br>$C_L$ = 50pF | | 5.5<br>8.5 | 9.5<br>13.0 | 1.0<br>1.0 | 11.5<br>15.0 | |
| $t_{PLZ}$,<br>$t_{PHZ}$ | Maximum Output Disable, Time, $\overline{OE}$ to Y | $V_{CC}$ = 2.7<br>$R_L$ = 1 kΩ | $C_L$ = 50pF | | 13.0 | 17.0 | 1.0 | 18.0 | ns |
| | | $V_{CC}$ = 3.3 V ± 0.3 V<br>$R_L$ = 1 kΩ | $C_L$ = 50pF | | 12 | 17.0 | 1.0 | 18.0 | |
| $C_{IN}$ | Maximum Input Capacitance | | | | 4 | 10 | | 10 | pF |
| | | | | Typical @ 25°C, $V_{CC}$ = 3.3 V | | | | | |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | | | | 20 | | | | pF |

5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

**NOISE CHARACTERISTICS** Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V

| Symbol | Characteristic | $T_A = 25°C$ | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.3 | 0.5 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −0.3 | −0.5 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

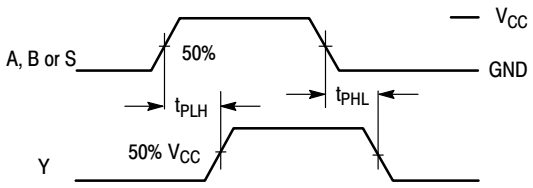



**Figure 4. Switching Waveform**

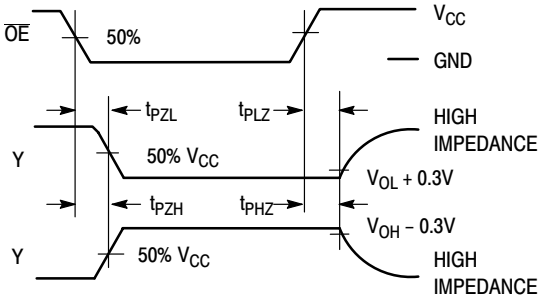
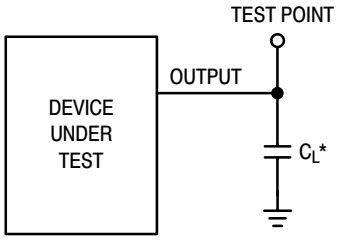
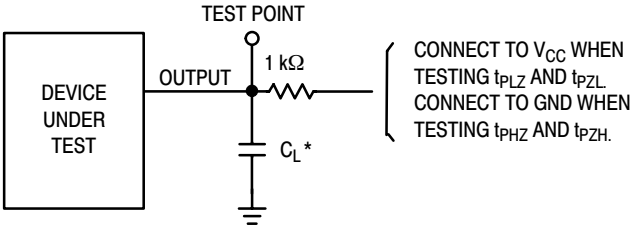



**Figure 5. Switching Waveform**




*Includes all probe and jig capacitance

**Figure 6. Test Circuit**




*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

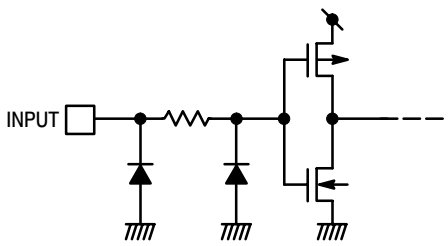
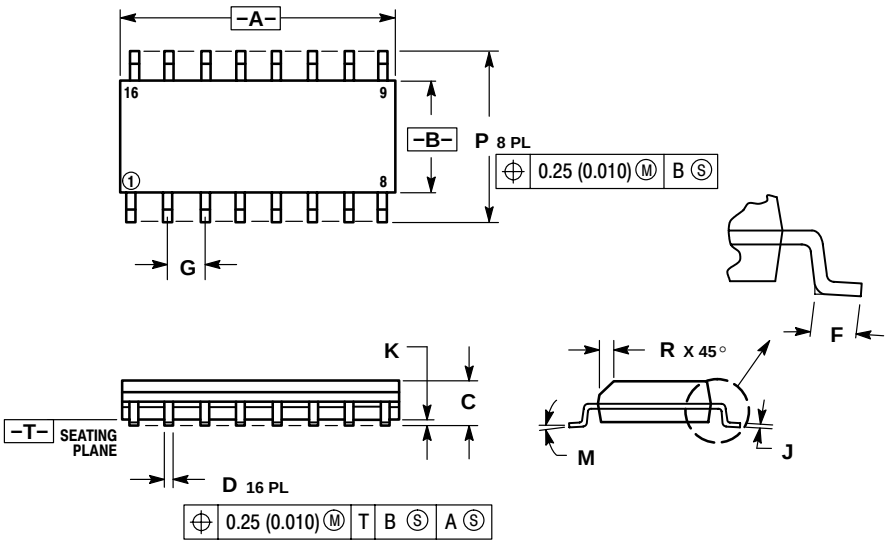



**Figure 8. Input Equivalent Circuit**

## PACKAGE DIMENSIONS

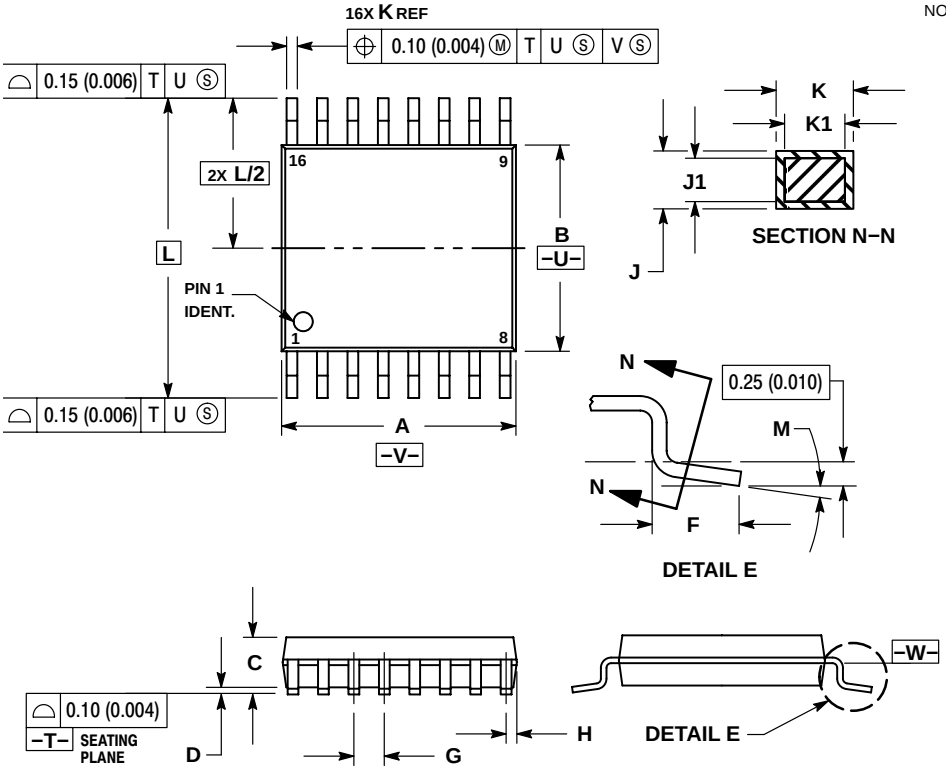
**SOIC−16**
**D SUFFIX**
CASE 751B−05
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

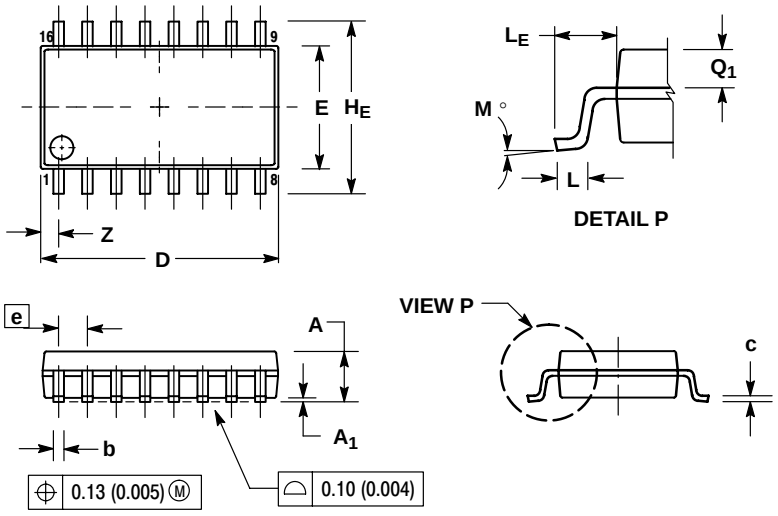
**TSSOP−16**
**DT SUFFIX**
CASE 948F−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**SOEIAJ−16**
**M SUFFIX**
CASE 966−01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

## PUBLICATION ORDERING INFORMATION

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**MC74LVX257/D**