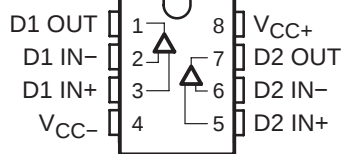


# THS6052, THS6053 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

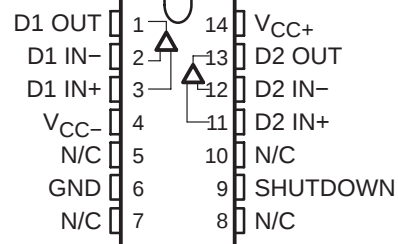
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- **Remote Terminal ADSL Line Driver**
  - Ideal for Both Full Rate ADSL and G.Lite
  - Compatible With 1:1 Transformer Ratio
- **Low  $2.7 \text{ pA}/\sqrt{\text{Hz}}$  Noninverting Current Noise**
  - Reduces Noise Feedback Through Hybrid Into Downstream Channel
- **Wide Supply Voltage Range  $\pm 5 \text{ V}$  to  $\pm 15 \text{ V}$** 
  - Ideal for  $\pm 12$ -V Operation
- **Wide Output Swing**
  - 42 Vpp Differential Output Voltage,  $R_L = 200 \Omega$ ,  $\pm 12$ -V Supply
- **High Output Current**
  - 175 mA (typ)
- **High Speed**
  - 110 MHz ( $-3 \text{ dB}$ ,  $G=8$ ,  $\pm 12 \text{ V}$ )
  - $1500 \text{ V}/\mu\text{s}$  Slew Rate ( $G = 8$ ,  $\pm 12 \text{ V}$ )
- **Low Distortion, Single-Ended,  $G = 8$** 
  - $-83 \text{ dBc}$  (250 kHz, 2 Vpp, 100- $\Omega$  load)
- **Low Power Shutdown (THS6053)**
  - 300- $\mu\text{A}$  Total Standby Current
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6052  
SOIC (D) AND  
SOIC PowerPAD™ (DDA) PACKAGE  
(TOP VIEW)

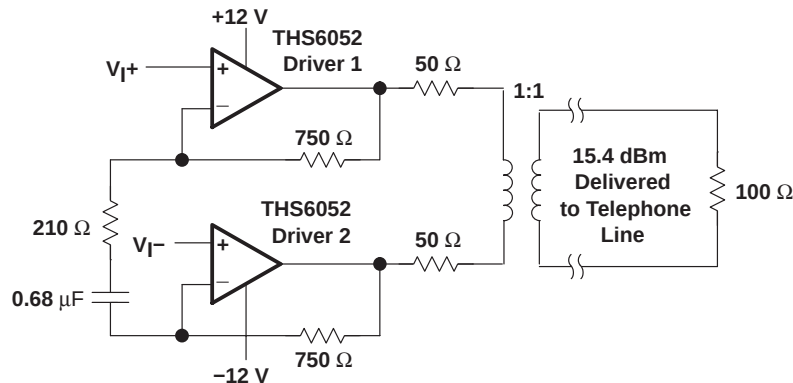


THS6053  
SOIC (D) AND  
TSSOP PowerPAD™ (PWP) PACKAGE  
(TOP VIEW)



## description

The THS6052/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from  $\pm 12$ -V supply voltages while drawing only 5.2 mA of supply current per channel. It offers low  $-83 \text{ dBc}$  total harmonic distortion driving a 100- $\Omega$  load (2 Vpp). The THS6052/3 offers a high 42-Vpp differential output swing across a 200- $\Omega$  load from a  $\pm 12$ -V supply. The THS6053 features a low-power shutdown mode, consuming only 300  $\mu\text{A}$  quiescent current per channel. The THS6052/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ packages.



## RELATED PRODUCTS

| DEVICE    | DESCRIPTION                             |
|-----------|-----------------------------------------|
| THS6042/3 | 350-mA, $\pm 12$ V ADSL CPE line driver |
| THS6092/3 | 275-mA, +12 V ADSL CPE line driver      |
| OPA2677   | 380-mA, +12 V ADSL CPE line driver      |
| THS6062   | Low noise ADSL receiver                 |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# THS6052, THS6053

## 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

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### AVAILABLE OPTION

| T <sub>A</sub> | PACKAGED DEVICE |                       |             |                | EVALUATION MODULES       |
|----------------|-----------------|-----------------------|-------------|----------------|--------------------------|
|                | SOIC-8 (D)      | SOIC-8 PowerPAD (DDA) | SOIC-14 (D) | TSSOP-14 (PWP) |                          |
| 0°C to 70°C    | THS6052CD       | THS6052CDDA           | THS6053CD   | THS6053CPWP    | THS6052EVM<br>THS6053EVM |
| –40°C to 85°C  | THS6052ID       | THS6052IDDA           | THS6053ID   | THS6053IPWP    | —                        |

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

|                                                                 |                               |
|-----------------------------------------------------------------|-------------------------------|
| Supply voltage, V <sub>CC+</sub> to V <sub>CC–</sub>            | 33 V                          |
| Input voltage                                                   | $\pm V_{CC}$                  |
| Output current (see Note 1)                                     | 275 mA                        |
| Differential input voltage                                      | $\pm 4$ V                     |
| Maximum junction temperature                                    | 150°C                         |
| Total power dissipation at (or below) 25°C free-air temperature | See Dissipation Ratings Table |
| Operating free-air temperature, T <sub>A</sub> : Commercial     | 0°C to 70°C                   |
| Industrial                                                      | –40°C to 85°C                 |
| Storage temperature, T <sub>stg</sub> : Commercial              | –65°C to 125°C                |
| Industrial                                                      | –65°C to 125°C                |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds    | 300°C                         |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6052 and THS6053 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

### DISSIPATION RATING TABLE

| PACKAGE | $\theta_{JA}$         | $\theta_{JC}$         | T <sub>A</sub> = 25°C<br>T <sub>J</sub> = 150°C<br>POWER RATING |
|---------|-----------------------|-----------------------|-----------------------------------------------------------------|
| D-8     | 95°C/W <sup>‡</sup>   | 38.3°C/W <sup>‡</sup> | 1.32 W                                                          |
| DDA     | 45.8°C/W <sup>‡</sup> | 9.2°C/W <sup>‡</sup>  | 2.73 W                                                          |
| D-14    | 66.6°C/W <sup>‡</sup> | 26.9°C/W <sup>‡</sup> | 1.88 W                                                          |
| PWP     | 37.5°C/W              | 1.4°C/W               | 3.3 W                                                           |

<sup>‡</sup> This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the  $\theta_{JA}$  is 168°C/W for the D–8 package and 122.3°C/W for the D–14 package.

### recommended operating conditions

|                                                      |               | MIN     | NOM | MAX      | UNIT |
|------------------------------------------------------|---------------|---------|-----|----------|------|
| Supply voltage, V <sub>CC+</sub> to V <sub>CC–</sub> | Dual supply   | $\pm 5$ |     | $\pm 15$ | V    |
|                                                      | Single supply | 10      |     | 30       |      |
| Operating free-air temperature, T <sub>A</sub>       | C-suffix      | 0       |     | 70       | °C   |
|                                                      | I-suffix      | –40     |     | 85       |      |



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electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  
 $V_{CC} = \pm 12$  V,  $R_{\text{FEEDBACK}} = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted)

**dynamic performance**

| PARAMETER |                                   | TEST CONDITIONS           |                                  | MIN                            | TYP  | MAX | UNIT             |
|-----------|-----------------------------------|---------------------------|----------------------------------|--------------------------------|------|-----|------------------|
| BW        | Small-signal bandwidth ( $-3$ dB) | $R_L = 50\ \Omega$        | G = 1, $R_F = 1\ \text{k}\Omega$ | $V_{CC} = \pm 5$ V             | 110  |     | MHz              |
|           |                                   |                           |                                  | $V_{CC} = \pm 12$ V            | 120  |     |                  |
|           |                                   |                           | G = 2, $R_F = 680\ \Omega$       |                                | 100  |     |                  |
|           |                                   |                           | G = 8, $R_F = 330\ \Omega$       | $V_{CC} = \pm 5$ V, $\pm 12$ V | 90   |     |                  |
|           |                                   | $R_L = 100\ \Omega$       | G = 1, $R_F = 1\ \text{k}\Omega$ | $V_{CC} = \pm 5$ V             | 150  |     |                  |
|           |                                   |                           |                                  | $V_{CC} = \pm 12$ V            | 170  |     |                  |
|           |                                   |                           | G = 2, $R_F = 680\ \Omega$       |                                | 135  |     |                  |
|           |                                   |                           | G = 8, $R_F = 330\ \Omega$       | $V_{CC} = \pm 5$ V, $\pm 12$ V | 110  |     |                  |
| SR        | Slew rate (see Note 2), G=8       | $V_O = 4\ \text{V}_{PP}$  | $V_{CC} = \pm 5$ V               | $V_{CC} = \pm 5$ V             | 650  |     | V/ $\mu\text{s}$ |
|           |                                   |                           | $V_{CC} = \pm 12$ V              | $V_{CC} = \pm 12$ V            | 850  |     |                  |
|           |                                   |                           | $V_{CC} = \pm 15$ V              | $V_{CC} = \pm 15$ V            | 950  |     |                  |
|           |                                   | $V_O = 16\ \text{V}_{PP}$ | $V_{CC} = \pm 12$ V              | $V_{CC} = \pm 12$ V            | 1500 |     |                  |
|           |                                   |                           | $V_{CC} = \pm 15$ V              | $V_{CC} = \pm 15$ V            | 1700 |     |                  |
|           |                                   |                           |                                  |                                |      |     |                  |

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

**noise/distortion performance**

| PARAMETER |                                                        | TEST CONDITIONS                                                       |                                                                                  | MIN | TYP  | MAX | UNIT                   |
|-----------|--------------------------------------------------------|-----------------------------------------------------------------------|----------------------------------------------------------------------------------|-----|------|-----|------------------------|
| THD       | Total harmonic distortion (single-ended configuration) | Gain = 8, $R_L = 100\ \Omega$ ,<br>$V_{CC} = \pm 12$ V, $f = 250$ kHz | $V_O(pp) = 2$ V                                                                  |     | -83  |     | dBc                    |
|           |                                                        |                                                                       | $V_O(pp) = 16$ V                                                                 |     | -78  |     |                        |
|           |                                                        | Gain = 8, $R_L = 50\ \Omega$ ,<br>$V_{CC} = \pm 5$ V, $f = 250$ kHz   | $V_O(pp) = 2$ V                                                                  |     | -74  |     |                        |
|           |                                                        |                                                                       | $V_O(pp) = 6$ V                                                                  |     | -72  |     |                        |
| $V_n$     | Input voltage noise                                    | $V_{CC} = \pm 5$ V, $f = 10$ kHz, $\pm 12$ V                          |                                                                                  |     | 2.1  |     | nV/ $\sqrt{\text{Hz}}$ |
| $I_n$     | Input current noise                                    | +Input                                                                | $f = 10$ kHz, $V_{CC} = \pm 5$ V,<br>$V_{CC} = \pm 12$ V,<br>$V_{CC} = \pm 15$ V |     | 2.7  |     | pA/ $\sqrt{\text{Hz}}$ |
|           |                                                        | -Input                                                                |                                                                                  |     | 10.7 |     |                        |
| $X_T$     | Crosstalk                                              | $f = 250$ kHz, $V_{CC} = \pm 12$ V,<br>G = 2, $R_L = 100\ \Omega$     | $V_O = 2\ \text{V}_{p-p}$                                                        |     | -79  |     | dBc                    |
|           |                                                        | $f = 250$ kHz, $V_{CC} = \pm 5$ V,<br>G = 2, $R_L = 50\ \Omega$       | $V_O = 2\ \text{V}_{p-p}$                                                        |     | -71  |     |                        |

# THS6052, THS6053

## 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 12$  V,  $R_{\text{FEEDBACK}} = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted) (continued)

### dc performance

| PARAMETER |                                 | TEST CONDITIONS                            |                           | MIN | TYP | MAX | UNIT                         |
|-----------|---------------------------------|--------------------------------------------|---------------------------|-----|-----|-----|------------------------------|
| $V_{OS}$  | Input offset voltage            | $V_{CC} = \pm 12$ V,<br>$V_{CC} = \pm 6$ V | $T_A = 25^\circ\text{C}$  |     | 5   | 10  | mV                           |
|           |                                 |                                            | $T_A = \text{full range}$ |     |     | 15  |                              |
|           | Differential offset voltage     |                                            | $T_A = 25^\circ\text{C}$  |     | 3   | 6   |                              |
|           | Offset drift                    |                                            | $T_A = \text{full range}$ |     |     | 8   | $\mu\text{V}/^\circ\text{C}$ |
| $I_{IB}$  | – Input bias current            | $V_{CC} = \pm 12$ V,<br>$V_{CC} = \pm 6$ V | $T_A = 25^\circ\text{C}$  |     | 5   | 10  | $\mu\text{A}$                |
|           |                                 |                                            | $T_A = \text{full range}$ |     |     | 12  |                              |
|           | + Input bias current            |                                            | $T_A = 25^\circ\text{C}$  |     | 2   | 5   |                              |
|           |                                 |                                            | $T_A = \text{full range}$ |     |     | 6   |                              |
|           | Differential input bias current |                                            | $T_A = 25^\circ\text{C}$  |     | 5   | 10  | $\mu\text{A}$                |
|           |                                 |                                            | $T_A = \text{full range}$ |     |     | 12  |                              |
| $Z_{OL}$  | Open loop transimpedance        | $V_{CC} = \pm 12$ V,<br>$V_{CC} = \pm 6$ V | $R_L = 1\ \text{k}\Omega$ |     | 1   |     | $\text{M}\Omega$             |

### input characteristics

| PARAMETER |                                 | TEST CONDITIONS                            |                           | MIN       | TYP        | MAX | UNIT             |
|-----------|---------------------------------|--------------------------------------------|---------------------------|-----------|------------|-----|------------------|
| $V_{ICR}$ | Input common-mode voltage range | $V_{CC} = \pm 12$ V                        |                           | $\pm 9.7$ | $\pm 10.1$ |     | V                |
|           |                                 | $V_{CC} = \pm 6$ V                         |                           | $\pm 3.8$ | $\pm 4.2$  |     |                  |
| CMRR      | Common-mode rejection ratio     | $V_{CC} = \pm 12$ V,<br>$V_{CC} = \pm 6$ V | $T_A = 25^\circ\text{C}$  | 59        | 66         |     | dB               |
|           |                                 |                                            | $T_A = \text{full range}$ | 57        |            |     |                  |
| $R_I$     | Input resistance                | + Input                                    |                           |           | 1.5        |     | $\text{M}\Omega$ |
|           |                                 | – Input                                    |                           |           | 15         |     | $\Omega$         |
| $C_I$     | Input capacitance               |                                            |                           |           | 2          |     | pF               |

### output characteristics

| PARAMETER |                       | TEST CONDITIONS                         |                                          | MIN                 | TYP        | MAX        | UNIT     |
|-----------|-----------------------|-----------------------------------------|------------------------------------------|---------------------|------------|------------|----------|
| $V_O$     | Output voltage swing  | Single ended                            | $R_L = 50\ \Omega$ , $V_{CC} = \pm 6$ V  | $\pm 4.2$           | $\pm 4.6$  |            | V        |
|           |                       |                                         | $R_L = 100\ \Omega$                      | $V_{CC} = \pm 12$ V | $\pm 10.1$ | $\pm 10.5$ |          |
|           |                       |                                         |                                          | $V_{CC} = \pm 6$ V  | $\pm 4.4$  | $\pm 4.8$  |          |
| $I_O$     | Output current        |                                         | $R_L = 25\ \Omega$ , $V_{CC} = \pm 12$ V | 150                 | 175        |            | mA       |
|           |                       |                                         | $R_L = 10\ \Omega$ , $V_{CC} = \pm 6$ V  | 150                 | 175        |            |          |
| $I_{SC}$  | Short-circuit current | $R_L = 0\ \Omega$ , $V_{CC} = \pm 12$ V |                                          |                     | 250        |            | mA       |
|           | Output resistance     | Open loop                               |                                          |                     | 14         |            | $\Omega$ |



**THS6052, THS6053**  
**175 mA,  $\pm 12$  V ADSL CPE LINE DRIVERS**

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electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 12$  V,  $R_{FEEDBACK} = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted) (continued)

**power supply**

| PARAMETER |                                 | TEST CONDITIONS     |                           | MIN       | TYP | MAX        | UNIT |
|-----------|---------------------------------|---------------------|---------------------------|-----------|-----|------------|------|
| $V_{CC}$  | Operating range                 | Dual supply         |                           | $\pm 4.5$ |     | $\pm 16.5$ | V    |
|           |                                 | Single supply       |                           | 9         |     | 33         |      |
| $I_{CC}$  | Quiescent current (each driver) | $V_{CC} = \pm 12$ V | $T_A = 25^\circ\text{C}$  |           | 5.2 | 7          | mA   |
|           |                                 |                     | $T_A = \text{full range}$ |           |     | 8          |      |
|           |                                 | $V_{CC} = \pm 6$ V  | $T_A = 25^\circ\text{C}$  |           | 4.5 | 6.5        |      |
|           |                                 |                     | $T_A = \text{full range}$ |           |     | 7.5        |      |
| PSRR      | Power supply rejection ratio    | $V_{CC} = \pm 12$ V | $T_A = 25^\circ\text{C}$  | -64       | -62 |            | dB   |
|           |                                 |                     | $T_A = \text{full range}$ | -61       | -   |            |      |
|           |                                 | $V_{CC} = \pm 6$ V  | $T_A = 25^\circ\text{C}$  | -60       | -70 |            |      |
|           |                                 |                     | $T_A = \text{full range}$ | -58       |     |            |      |

**shutdown characteristics (THS6053 only)**

| PARAMETER             |                                                | TEST CONDITIONS                                                     | MIN | TYP | MAX | UNIT          |
|-----------------------|------------------------------------------------|---------------------------------------------------------------------|-----|-----|-----|---------------|
| $V_{IL}(\text{SHDN})$ | Shutdown pin voltage for power up              | $V_{CC} = \pm 6$ V, $\pm 12$ V $GND = 0$ V, (GND Pin as Reference)  |     |     | 0.8 | V             |
| $V_{IH}(\text{SHDN})$ | Shutdown pin voltage for power down            | $V_{CC} = \pm 6$ V, $\pm 12$ V, $GND = 0$ V, (GND Pin as Reference) | 2   |     |     | V             |
| $I_{CC}(\text{SHDN})$ | Total quiescent current when in shutdown state | $V_{GND} = 0$ V, $V_{CC} = \pm 6$ V, $\pm 12$ V                     |     | 0.3 | 0.7 | mA            |
| $t_{DIS}$             | Disable time (see Note 3)                      | $V_{CC} = \pm 12$ V                                                 |     | 0.1 |     | $\mu\text{s}$ |
| $t_{EN}$              | Enable time (see Note 3)                       | $V_{CC} = \pm 12$ V                                                 |     | 0.4 |     | $\mu\text{s}$ |
| $I_{IL}(\text{SHDN})$ | Shutdown pin input bias current for power up   | $V_{CC} = \pm 6$ V, $\pm 12$ V                                      |     | 40  | 100 | $\mu\text{A}$ |
| $I_{IH}(\text{SHDN})$ | Shutdown pin input bias current for power down | $V_{CC} = \pm 6$ V, $\pm 12$ V, $V(\text{SHND}) = 3.3$ V            |     | 50  | 100 | $\mu\text{A}$ |

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.



# THS6052, THS6053 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

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## APPLICATION INFORMATION

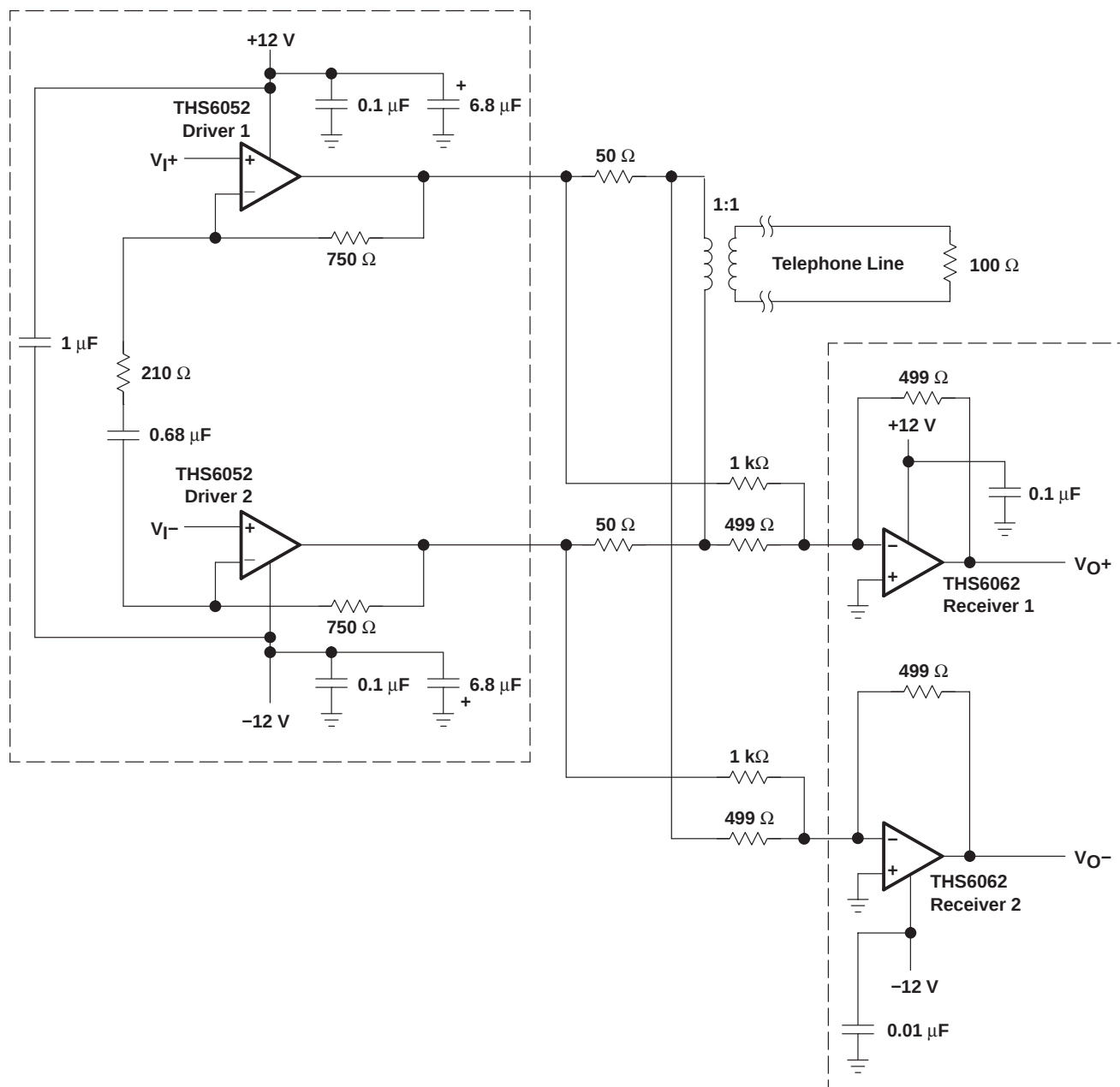


Figure 1. THS6052 ADSL Application With 1:1 Transformer Ratio

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins        | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">THS6052CDDA</a>  | Active        | Production           | SO PowerPAD (DDA)   8 | 75   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | 0 to 70      | 6052C               |
| THS6052CDDA.A                | Active        | Production           | SO PowerPAD (DDA)   8 | 75   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | 0 to 70      | 6052C               |
| <a href="#">THS6052ID</a>    | Active        | Production           | SOIC (D)   8          | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6052I               |
| THS6052ID.A                  | Active        | Production           | SOIC (D)   8          | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 6052I               |
| <a href="#">THS6052IDDA</a>  | Active        | Production           | SO PowerPAD (DDA)   8 | 75   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | 6052I               |
| THS6052IDDA.A                | Active        | Production           | SO PowerPAD (DDA)   8 | 75   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | 6052I               |
| <a href="#">THS6053CPWPR</a> | Active        | Production           | HTSSOP (PWP)   14     | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | HS6053C             |
| THS6053CPWPR.A               | Active        | Production           | HTSSOP (PWP)   14     | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | HS6053C             |
| <a href="#">THS6053IPWP</a>  | Active        | Production           | HTSSOP (PWP)   14     | 90   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | HS6053I             |
| THS6053IPWP.A                | Active        | Production           | HTSSOP (PWP)   14     | 90   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | HS6053I             |
| <a href="#">THS6053IPWPR</a> | Active        | Production           | HTSSOP (PWP)   14     | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | HS6053I             |
| THS6053IPWPR.A               | Active        | Production           | HTSSOP (PWP)   14     | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | HS6053I             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

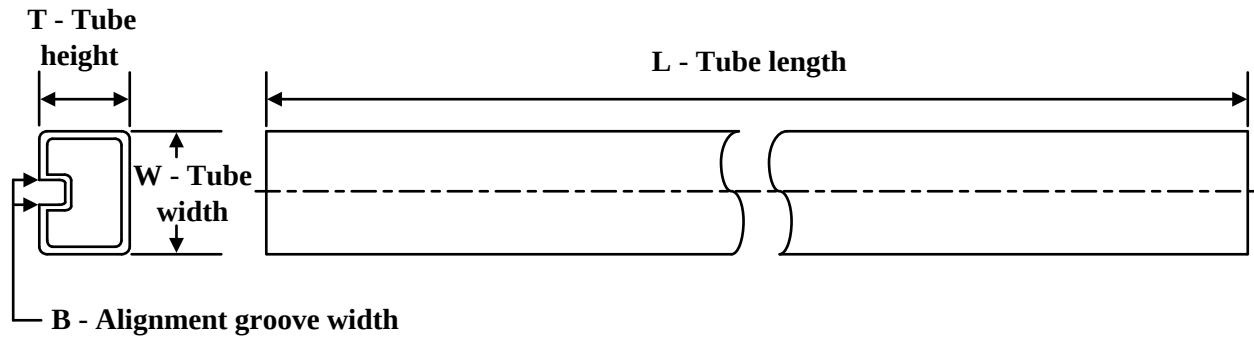
| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| THS6053CPWPR | HTSSOP       | PWP             | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| THS6053IPWPR | HTSSOP       | PWP             | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



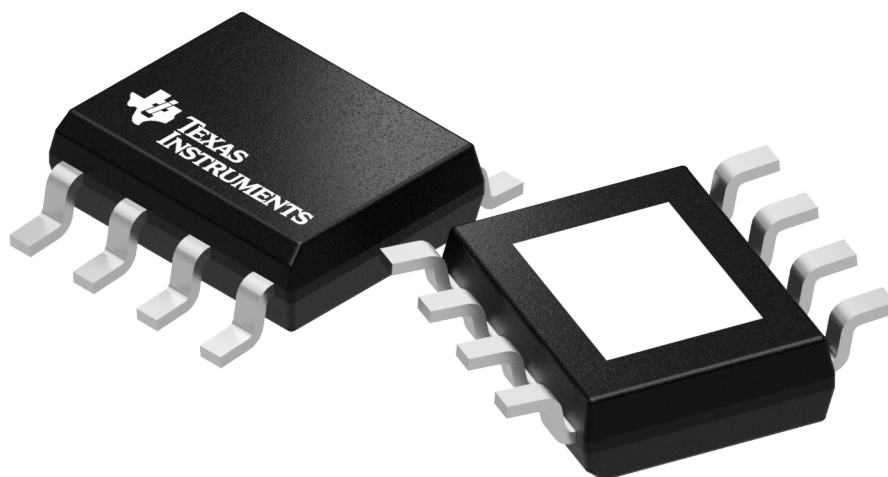
\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| THS6053CPWPR | HTSSOP       | PWP             | 14   | 2000 | 350.0       | 350.0      | 43.0        |
| THS6053IPWPR | HTSSOP       | PWP             | 14   | 2000 | 350.0       | 350.0      | 43.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| THS6052CDDA   | DDA          | HSOIC        | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| THS6052CDDA.A | DDA          | HSOIC        | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| THS6052ID     | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| THS6052ID.A   | D            | SOIC         | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| THS6052IDDA   | DDA          | HSOIC        | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| THS6052IDDA.A | DDA          | HSOIC        | 8    | 75  | 505.46 | 6.76   | 3810   | 4      |
| THS6053IPWP   | PWP          | HTSSOP       | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| THS6053IPWP.A | PWP          | HTSSOP       | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

## GENERIC PACKAGE VIEW

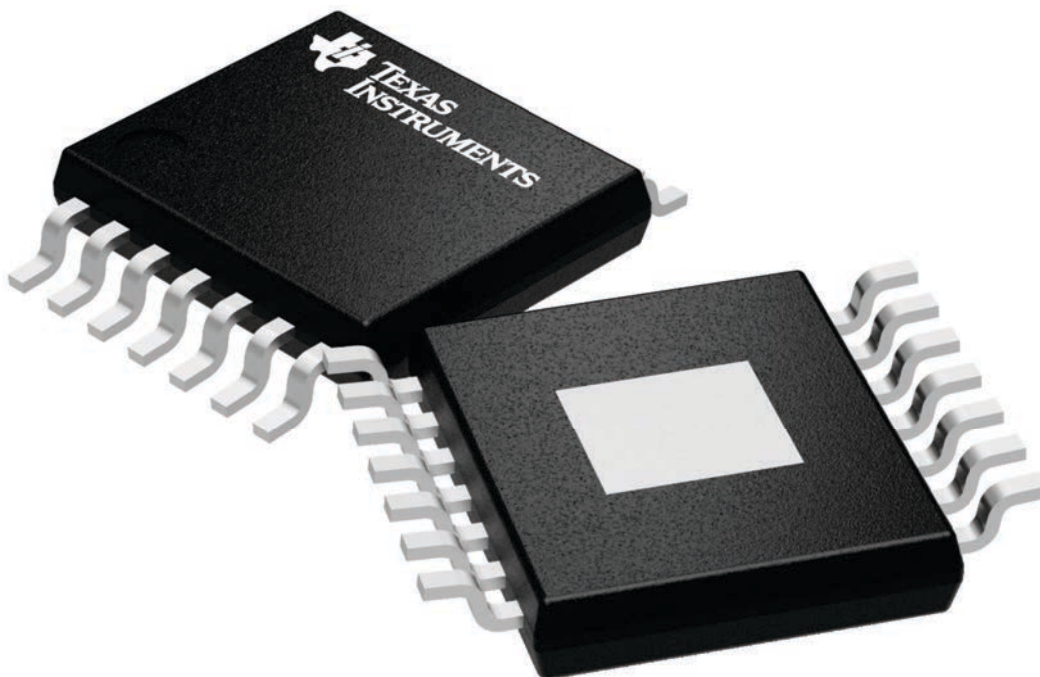
**PWP 14**

**PowerPAD TSSOP - 1.2 mm max height**

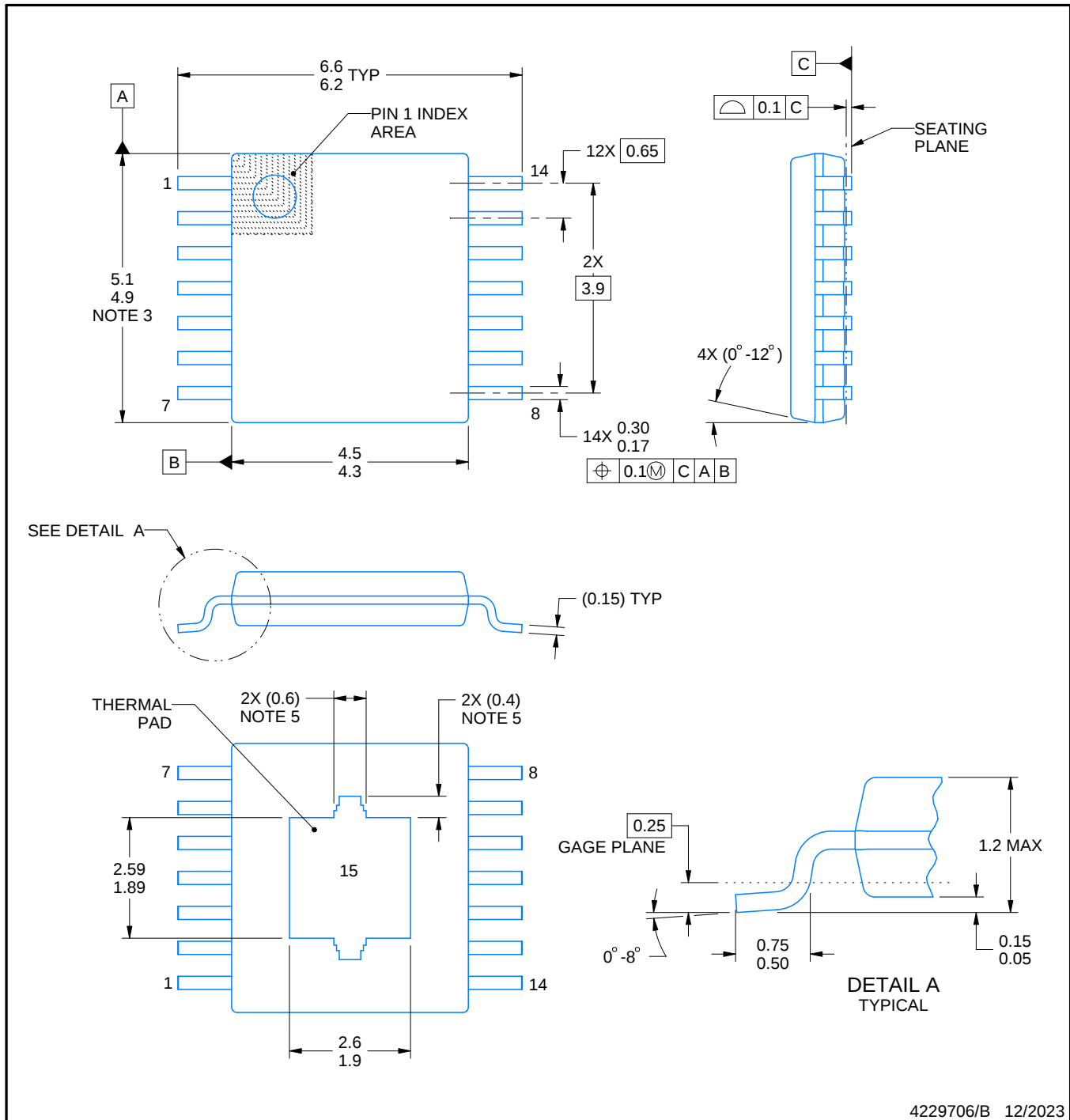
4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224995/A



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## NOTES:

PowerPAD is a trademark of Texas Instruments.

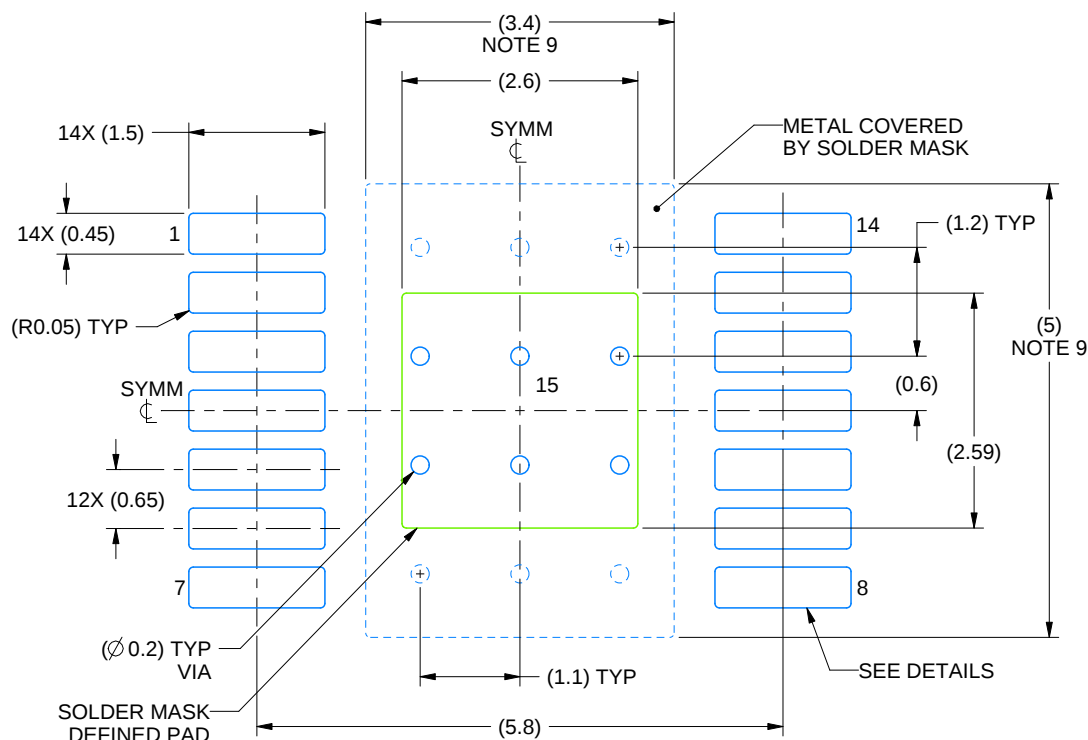
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

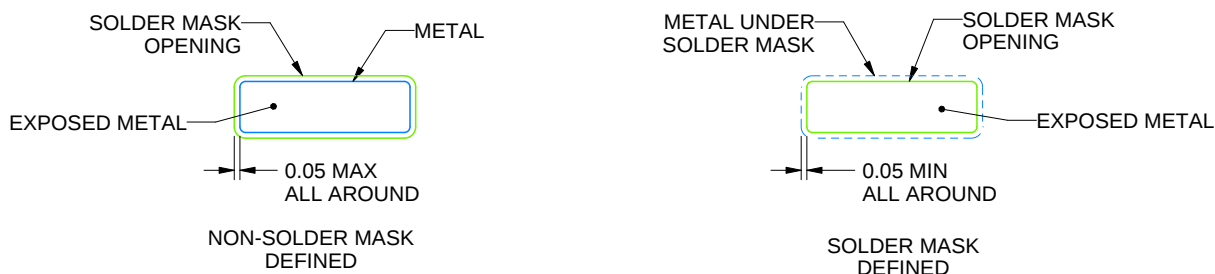
PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

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NOTES: (continued)

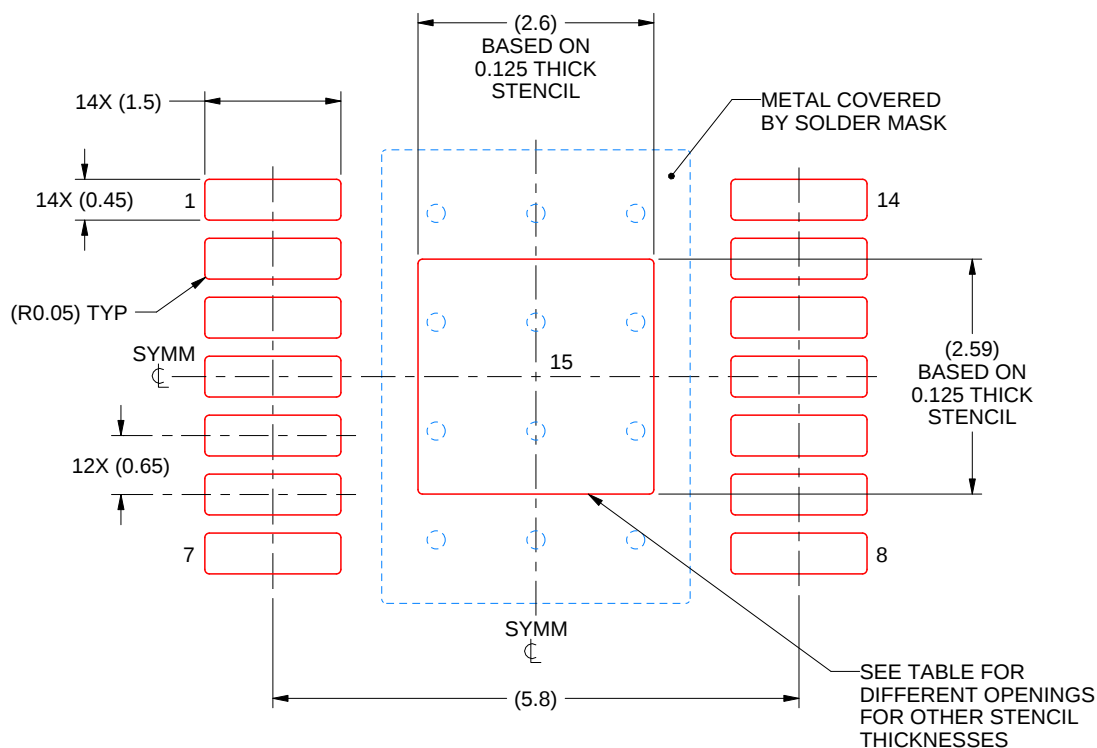
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 12X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 2.91 X 2.90            |
| 0.125             | 2.60 X 2.59 (SHOWN)    |
| 0.15              | 2.37 X 2.36            |
| 0.175             | 2.20 X 2.19            |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

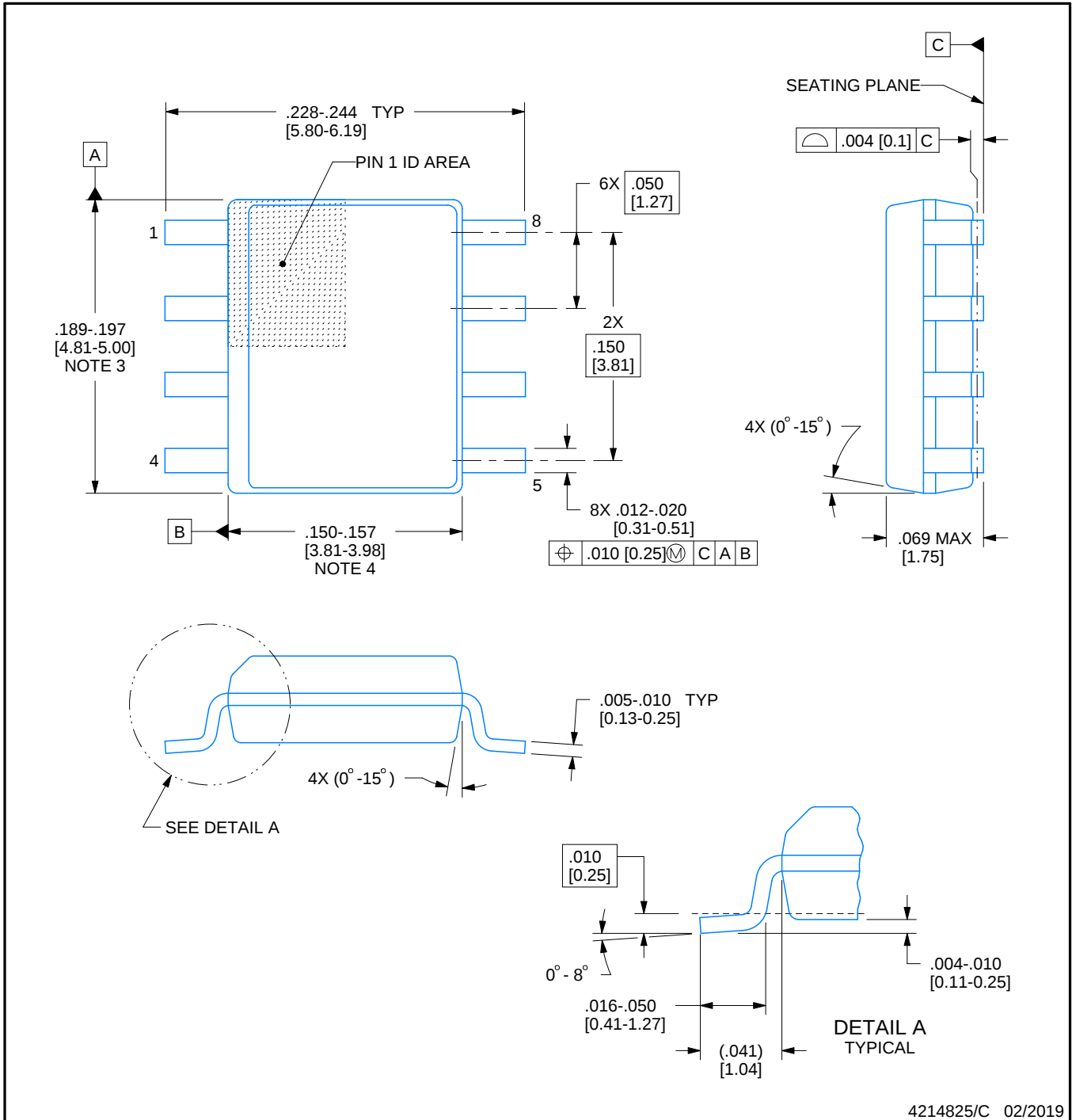


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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