

FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero added ground bounce
- Ultra low power with $0.2\mu\text{A}$ typical I_{cc}
- Undershoot clamp diodes on all switch and control inputs
- Two enables control five bits each
- Available in QSOP and TSSOP packages

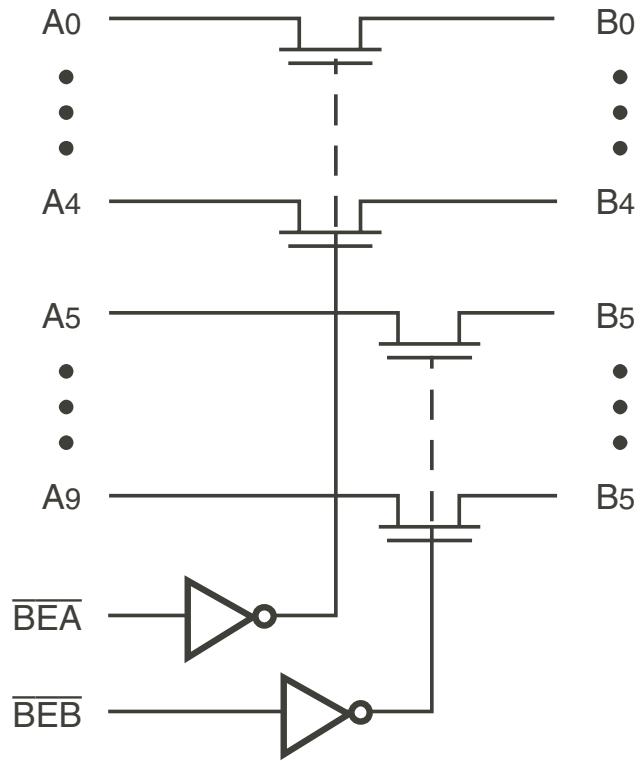
DESCRIPTION:

The QS3L384 provides a set of ten high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS3L384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{\text{BE}}$) signals turn the switches on. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses.

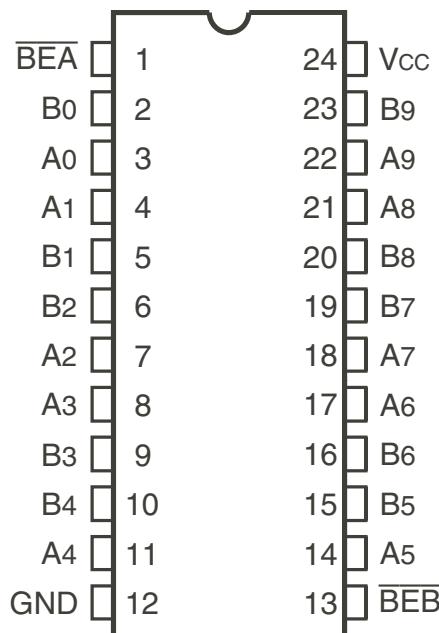
The QS3L384 is characterized for operation at -40°C to $+85^{\circ}\text{C}$.

APPLICATIONS:

- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Power Conservation
- Capacitance reduction and isolation
- Bus Isolation
- Clock Gating

FUNCTIONAL BLOCK DIAGRAM


PIN CONFIGURATION

QSOP/TSSOP
TOP VIEWABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|--|-------------|------------------|
| VTERM ⁽²⁾ | Supply Voltage to Ground | -0.5 to +7 | V |
| VTERM ⁽³⁾ | DC Switch Voltage Vs | -0.5 to +7 | V |
| VTERM ⁽³⁾ | DC Input Voltage VIN | -0.5 to +7 | V |
| VAC | AC Input Voltage (pulse width \leq 20ns) | -3 | V |
| IOUT | DC Output Current | 120 | mA |
| PMAX | Maximum Power Dissipation ($T_A = 85^\circ\text{C}$) | 0.5 | W |
| TSTG | Storage Temperature | -65 to +150 | $^\circ\text{C}$ |

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc .

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$)

| Pins | Typ. | Max. ⁽¹⁾ | Unit |
|-----------------------------------|------|---------------------|------|
| Control Inputs | 3 | 5 | pF |
| Quickswitch Channels (Switch OFF) | 5 | 7 | pF |

NOTE:

1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

| Pin Names | I/O | Description |
|-----------|-----|-------------------|
| A0 - A9 | I/O | Bus A |
| B0 - B9 | I/O | Bus B |
| BEA, BEB | I | Bus Switch Enable |

FUNCTION TABLE⁽¹⁾

| BEA | BEB | B0 - A4 | B5 - B9 | Function |
|-----|-----|---------|---------|------------|
| H | H | Hi-Z | Hi-Z | Disconnect |
| L | H | A0 - A4 | Hi-Z | Connect |
| H | L | Hi-Z | A5 - A9 | Connect |
| L | L | A0 - A4 | A5 - A9 | Connect |

NOTE:

1. H = HIGH Voltage Level
- L = LOW Voltage Level
- Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

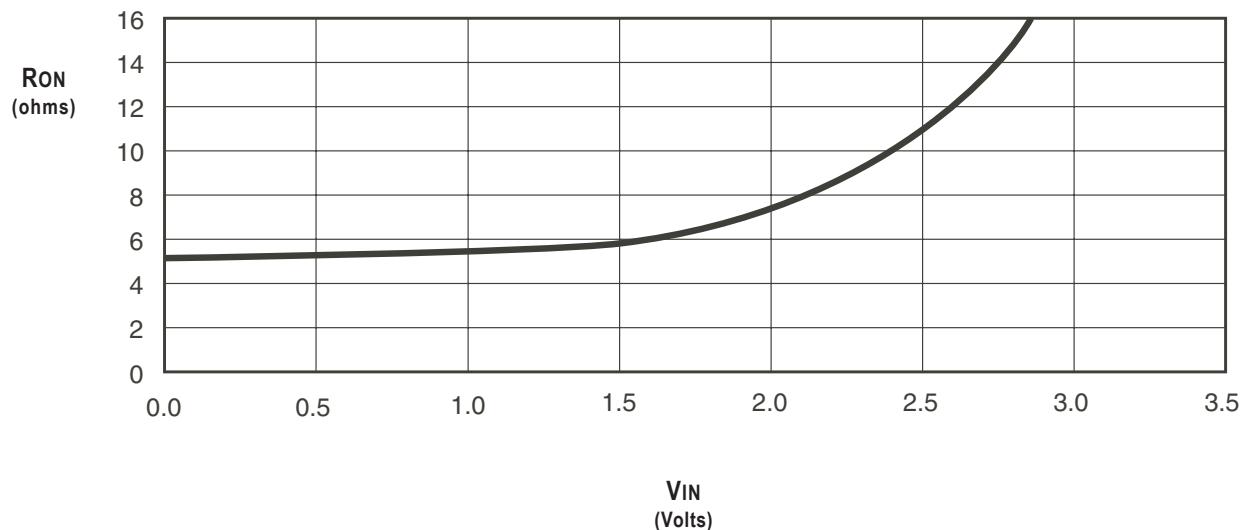
Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

| Symbol | Parameter | Test Conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|----------|--|--|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Voltage | Guaranteed Logic HIGH for Control Pins | 2 | — | — | V |
| V_{IL} | Input LOW Voltage | Guaranteed Logic LOW for Control Pins | — | — | 0.8 | V |
| I_{IN} | Input Leakage Current (Control Inputs) | $0\text{V} \leq V_{IN} \leq V_{CC}$ | — | — | ± 1 | μA |
| I_{OZ} | Off-State Current (Hi-Z) | $0\text{V} \leq V_{OUT} \leq V_{CC}$ | — | ± 0.01 | ± 1 | μA |
| R_{ON} | Switch ON Resistance | $V_{CC} = \text{Min.}$, $V_{IN} = 0\text{V}$, $I_{ON} = 30\text{mA}$ | — | 5 | 7 | Ω |
| | | $V_{CC} = \text{Min.}$, $V_{IN} = 2.4\text{V}$, $I_{ON} = 15\text{mA}$ | — | 10 | 15 | |
| V_P | Pass Voltage ⁽²⁾ | $V_{IN} = V_{CC} = 5\text{V}$, $I_{OUT} = -5\mu\text{A}$ | 3.7 | 4 | 4.2 | V |

NOTES:

1. Typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Pass voltage is guaranteed but not production tested.

TYPICAL ON RESISTANCE vs V_{IN} AT $V_{CC} = 5\text{V}$



POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Typ. | Max. | Unit |
|------------------|---|--|------|------|--------|
| I _{CCQ} | Quiescent Power Supply Current | V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0 | 0.2 | 3 | µA |
| ΔI _{CC} | Power Supply Current per Input HIGH ⁽²⁾ | V _{CC} = Max., V _{IN} = 3.4V, f = 0 | — | 1.5 | mA |
| I _{CCD} | Dynamic Power Supply Current per MHz ⁽³⁾ | V _{CC} = Max., A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle | — | 0.25 | mA/MHz |

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TTL-driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 5V ± 5%

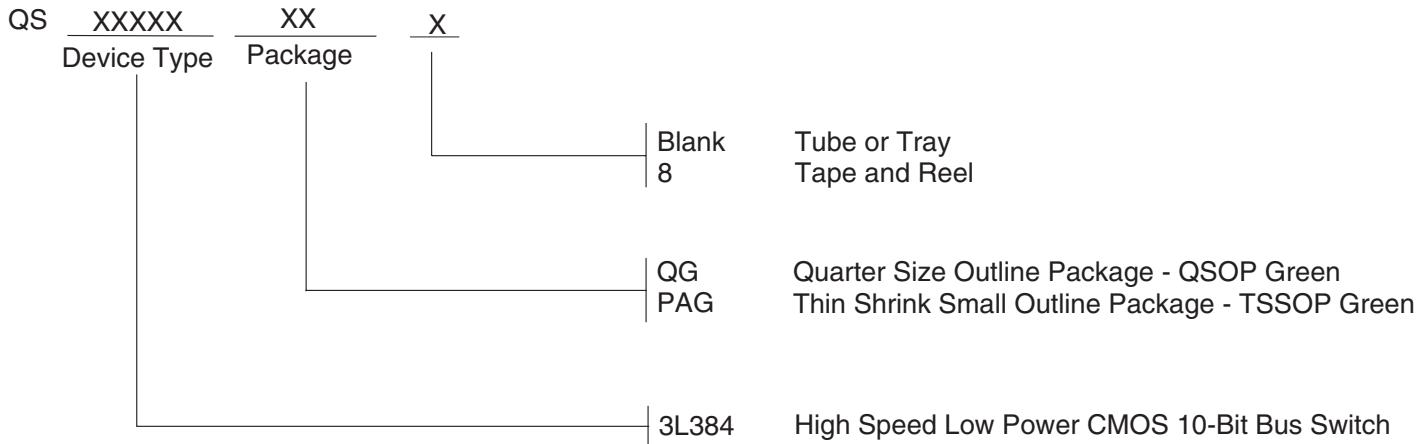
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

| Symbol | Parameter | Min. ⁽¹⁾ | Typ. | Max. | Unit |
|--------------------------------------|--|---------------------|------|---------------------|------|
| t _{PLH} t _{PHL} | Data Propagation Delay ⁽²⁾ Ax to Bx, Bx to Ax | — | — | 0.25 ⁽³⁾ | ns |
| t _{PZL} t _{PZH} | Switch Turn-On Delay B̄EA, B̄EB to Ax, Bx | 1.5 | — | 6.5 | ns |
| t _{PLZ} t _{PHZ} | Switch Turn-Off Delay ⁽²⁾ B̄EA, B̄EB to Ax, Bx | 1.5 | — | 5.5 | ns |

NOTES:

1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns at C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

ORDERING INFORMATION



Datasheet Document History

01/28/13

Pg. 1, 5

Updated the Ordering Information by removing non green package version, the "IDT" notation and Adding Tape and Reel information.



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com