

IS62/65WV2568DALL IS62/65WV2568DBLL



256K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

JULY 2017

FEATURES

- High-speed access time: 35ns, 45ns, 55ns
- CMOS low power operation
 - 36 mW (typical) operating
 - 9 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
 - 1.8V $\pm$ 10% V_{CC} (IS62/65WV2568DALL)
 - 2.5V–3.6V V_{CC} (IS62/65WV2568DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Lead-free available

DESCRIPTION

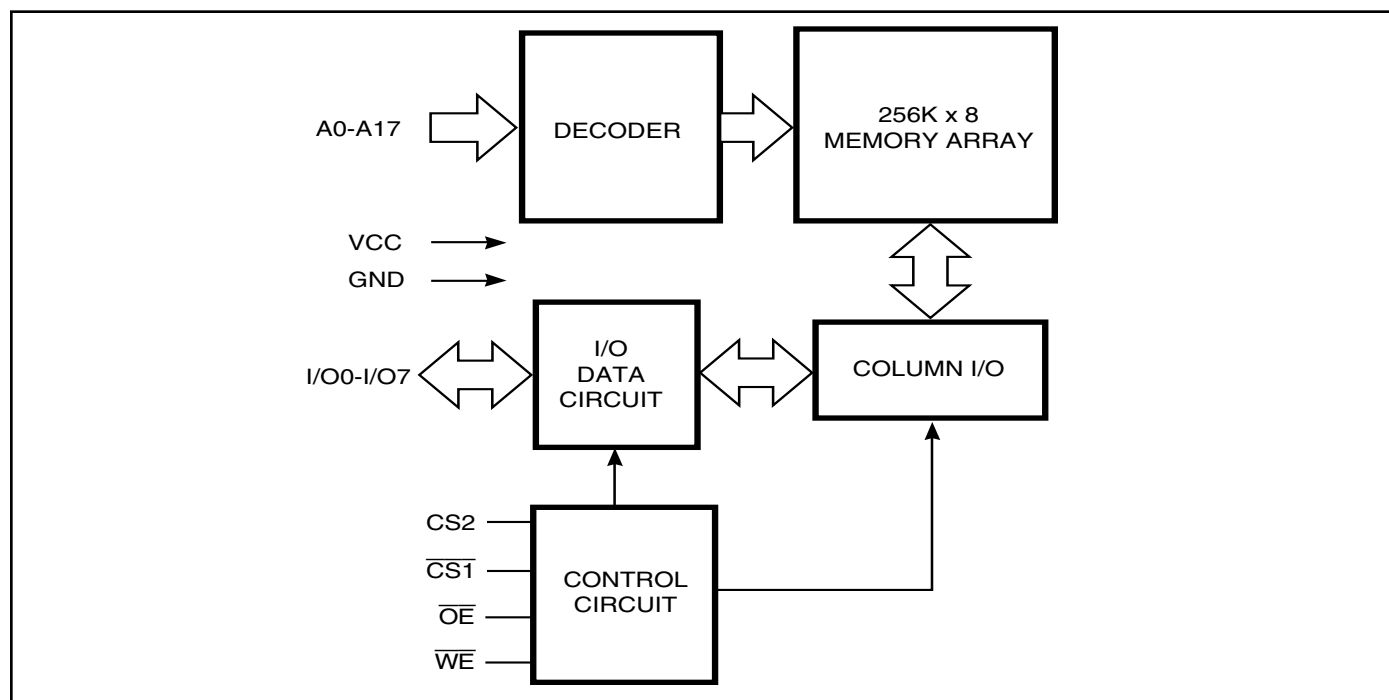
The *ISSI* IS62/65WV2568DALL and IS62/65WV2568DBLL are high-speed, 2M bit static RAMs organized as 256K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{\text{CS1}}$ is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{\text{WE}}$) controls both writing and reading of the memory.

The IS62/65WV2568DALL and IS62/65WV2568DBLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), sTSOP (TYPE I), and 36-pin mini BGA.

FUNCTIONAL BLOCK DIAGRAM



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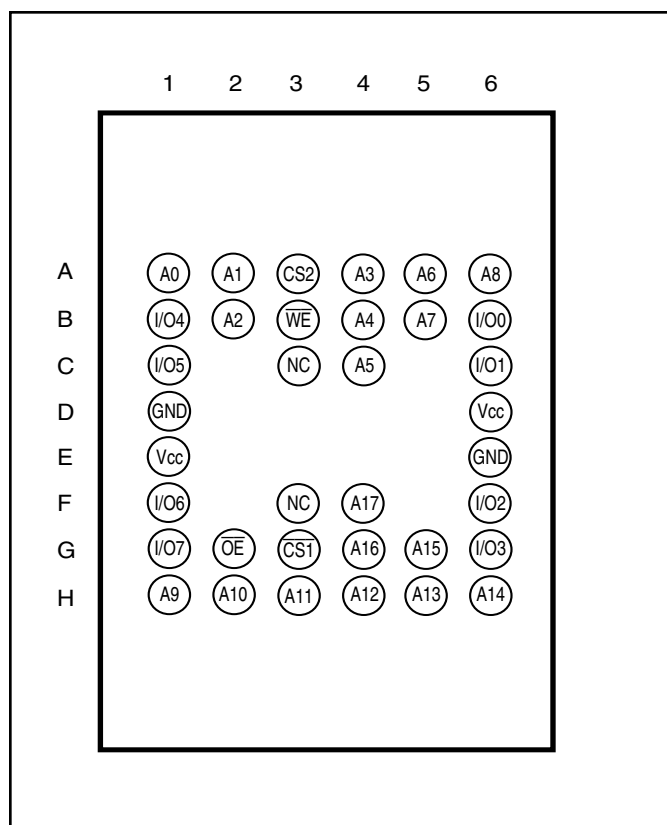
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN DESCRIPTIONS

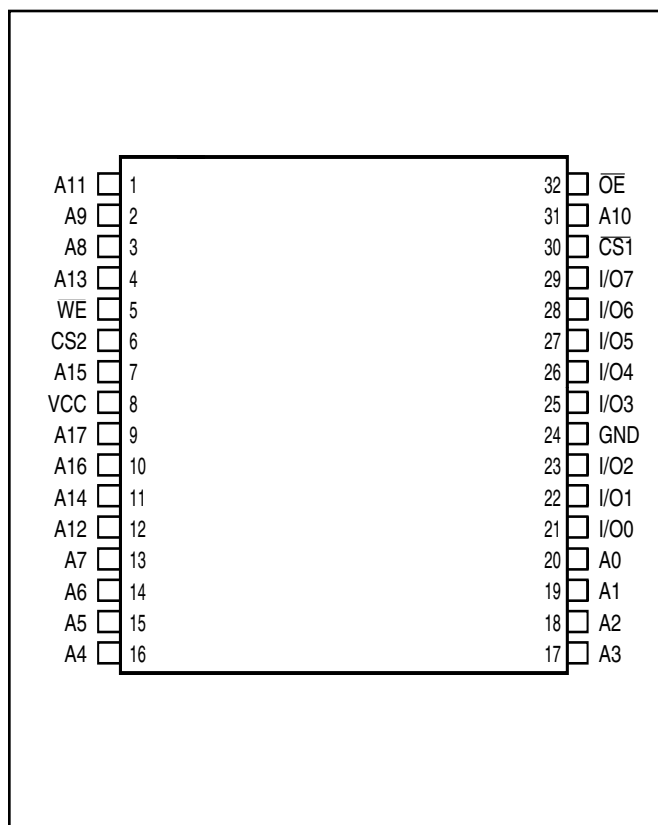
A0-A17	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

PIN CONFIGURATION

36-pin mini BGA (B) (6mm x 8mm)



32-pin TSOP (TYPE I), sTSOP (TYPE I)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.2 to V _{CC} +0.3	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{CC})

Range	Ambient Temperature	IS62/65WV2568DALL	IS62/65WV2568DBLL
Commercial	0°C to +70°C	1.8V ± 10%	2.5V - 3.6V
Industrial	-40°C to +85°C	1.8V ± 10%	2.5V - 3.6V
Automotive (A3)	-40°C to +125°C	1.8V ± 10%	2.5V - 3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V _{CC}	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	1.8V ± 10%	1.4	—	V
		I _{OH} = -1 mA	2.5-3.6V	2.2	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	1.8V ± 10%	—	0.2	V
		I _{OL} = 1.0 mA	2.5-3.6V	—	0.4	V
V _{IH}	Input HIGH Voltage		1.8V ± 10%	1.4	V _{CC} + 0.2	V
			2.5-3.6V	2.2	V _{CC} + 0.3	V
V _{IL} ⁽¹⁾	Input LOW Voltage		1.8V ± 10%	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}		-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled		-1	1	μA

Notes:

For IS62/65WV2568DALL:

V_{IL} (min.) = -1.0V AC (pulse width < 10ns). Not 100% tested.

V_{IH} (max.) = V_{CC} + 1.0V AC; (pulse width < 10ns). Not 100% tested.

For IS62/65WV2568DBLL:

V_{IL} (min.) = -2.0V AC (pulse width < 10ns). Not 100% tested.

V_{IH} (max.) = V_{CC} + 2.0V AC; (pulse width < 10ns). Not 100% tested.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	10	pF

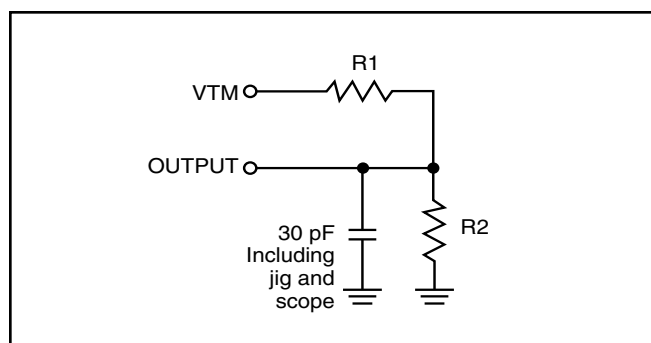
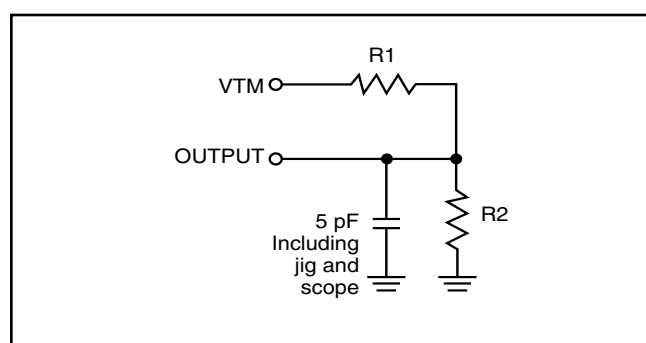
Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	62WV2568DALL (Unit)	62WV2568DBLL (Unit)
Input Pulse Level	0.4V to V _{CC} -0.2V	0.4V to V _{CC} -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V _{REF}	V _{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.8V ± 10%	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V _{REF}	0.9V	1.5V
V _{TM}	1.8V	2.8V

AC TEST LOADS**Figure 1****Figure 2**

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 35ns	Max. 45ns	Max. 55ns	Unit
I _{CC}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX}	Com.	15	12	10	mA
			Ind.	20	15	12	
			Auto.	25	20	15	
			typ. ⁽²⁾	10	8	6	
I _{SB1}	TTL Standby Current (TTL Inputs)	CS2 = VIL f = 0Hz	Com.	0.1	0.1	0.1	mA
			Ind.	0.2	0.2	0.2	
			AUTO.	0.3	0.3	0.3	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	(1) 0V ≤ CS2 ≤ 0.2V	Com.	7	7	7	μA
		OR	Ind.	10	10	10	
		(2) $\overline{\text{CS1}} \geq \text{VDD} - 0.2\text{V}$,	Auto.	—	30	30	
		CS2 ≥ VDD - 0.2V f = 0Hz	typ. ⁽²⁾		3		

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{CC} = 3.0V, T_a = 25°C and not 100% tested.

IS62/65WV2568DALL, IS62/65WV2568DBLL

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

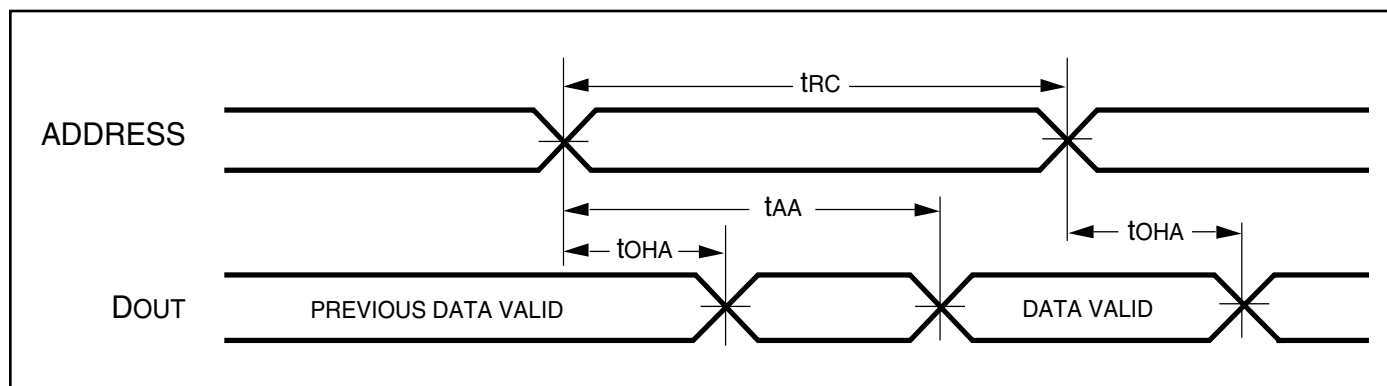
Symbol	Parameter	35ns		45ns		55ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t _{AA}	Address Access Time	—	35	—	45	—	55	ns
t _{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t _{ACS1} /t _{ACS2}	$\overline{CS1}/CS2$ Access Time	—	35	—	45	—	55	ns
t _{DOE}	$\overline{OE}$ Access Time	—	15	—	20	—	25	ns
t _{HZOE} ⁽²⁾	$\overline{OE}$ to High-Z Output	—	10	—	15	—	20	ns
t _{LZOE} ⁽²⁾	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t _{HZCS1} /t _{HZCS2} ⁽²⁾	$\overline{CS1}/CS2$ to High-Z Output	0	10	0	15	0	20	ns
t _{LZCS1} /t _{LZCS2} ⁽²⁾	$\overline{CS1}/CS2$ to Low-Z Output	10	—	10	—	10	—	ns

Notes:

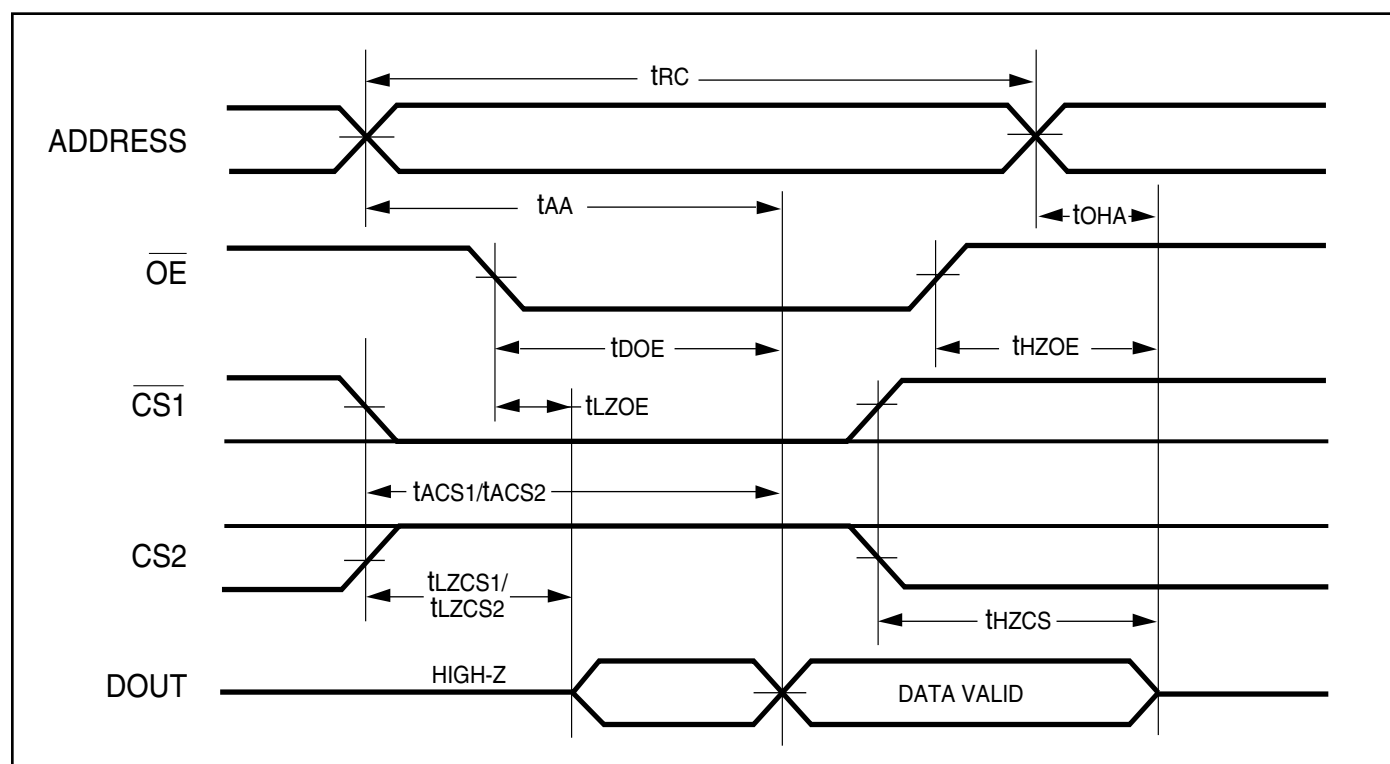
1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$)



AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, CS2, $\overline{OE}$ Controlled)

Notes:

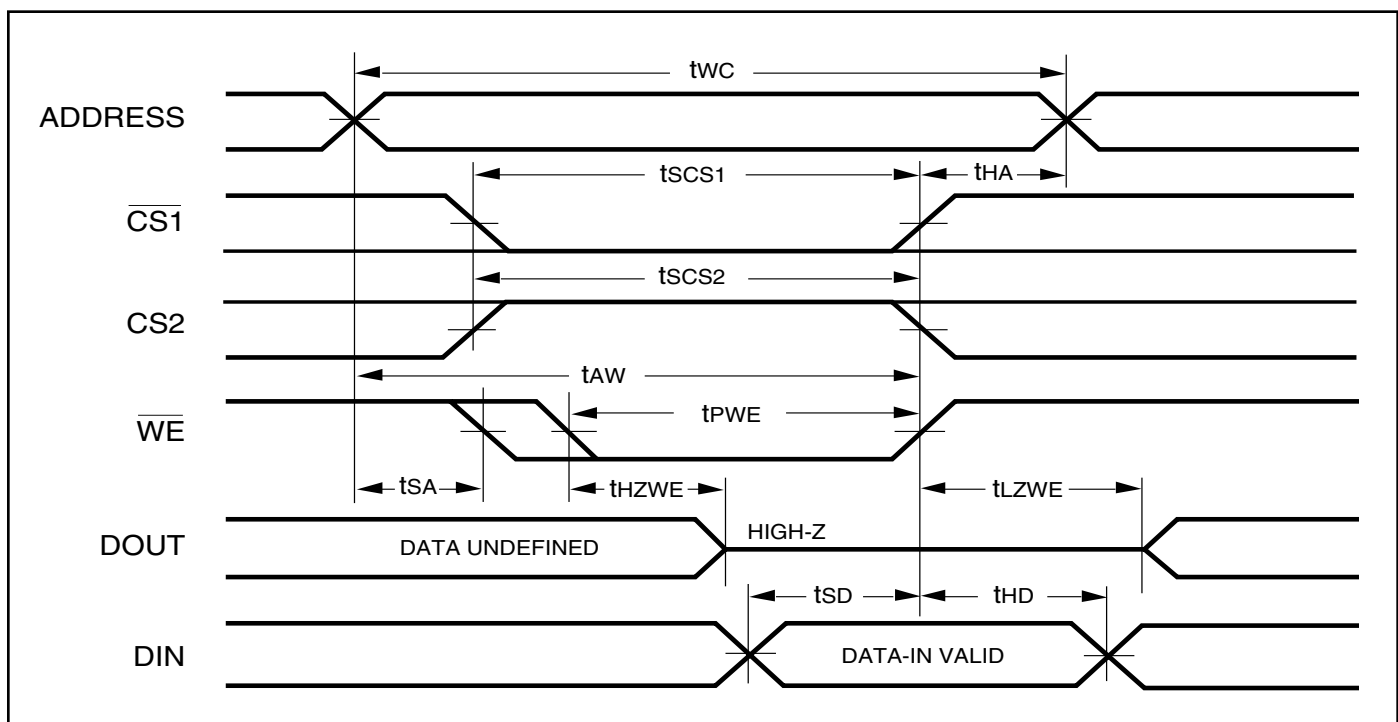
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1} = V_{IL}$. $CS2 = \overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and CS2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

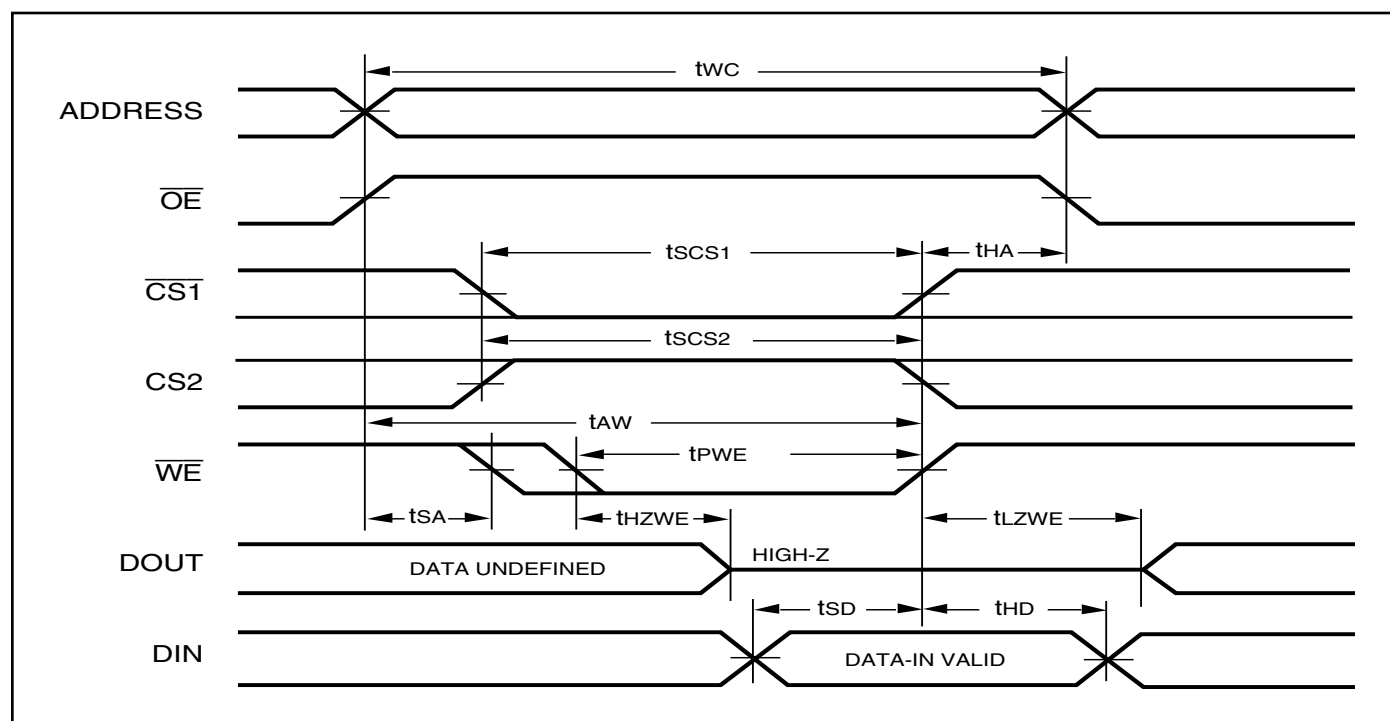
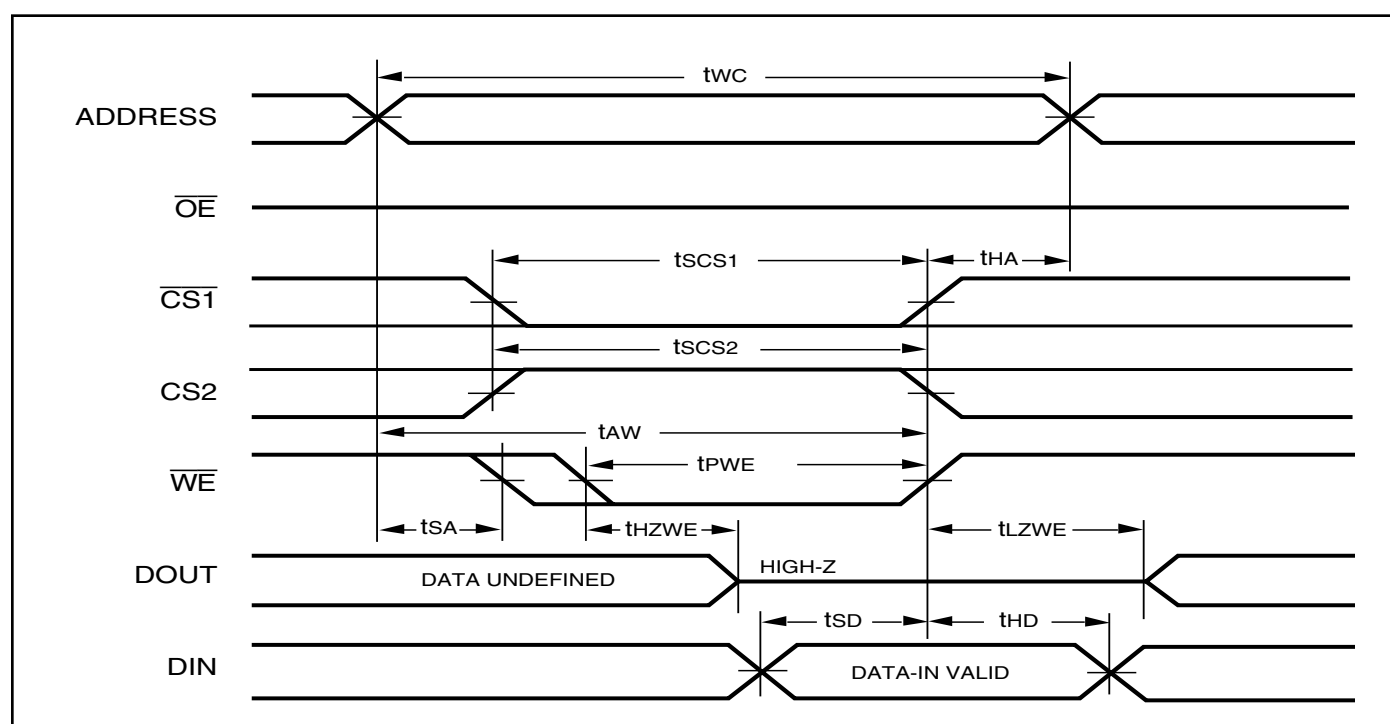
Symbol	Parameter	35ns		45ns		55ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t _{SCS1/tSCS2}	$\overline{CS1}/CS2$ to Write End	25	—	35	—	45	—	ns
t _{AW}	Address Setup Time to Write End	25	—	35	—	45	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWE}	$\overline{WE}$ Pulse Width	30	—	35	—	40	—	ns
t _{SD}	Data Setup to Write End	15	—	20	—	25	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, $CS2$ HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{CS1}/CS2$ Controlled, $\overline{OE}$ = HIGH or LOW)


AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

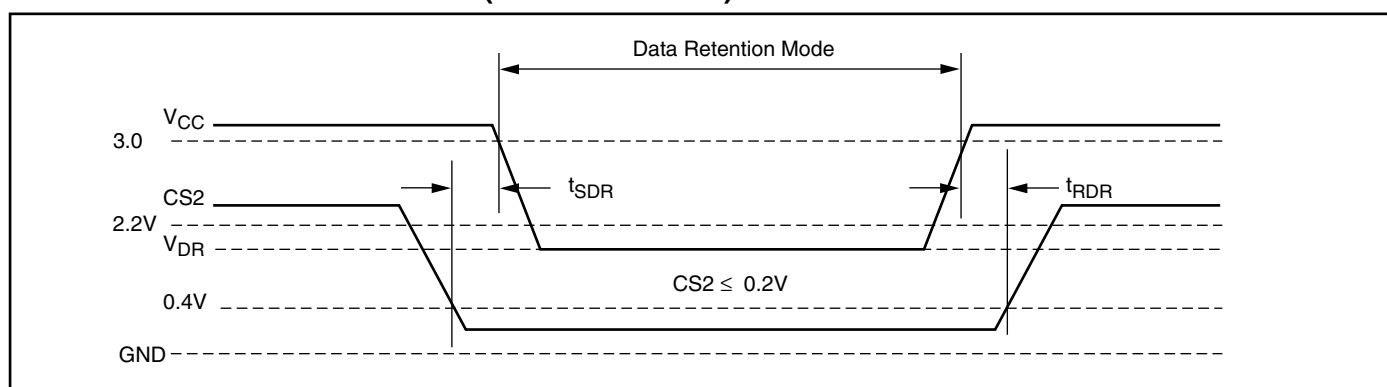
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	See Data Retention Waveform	1.5	3.6	V
I_{DR}	Data Retention Current	(1) $0V \leq CS2 \leq 0.2V$, or (2) $CS1 \geq V_{DD} - 0.2V$, $CS2 \geq V_{DD} - 0.2V$	Com. — Ind. — Auto. — typ. ⁽¹⁾ —	7 10 20 2	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

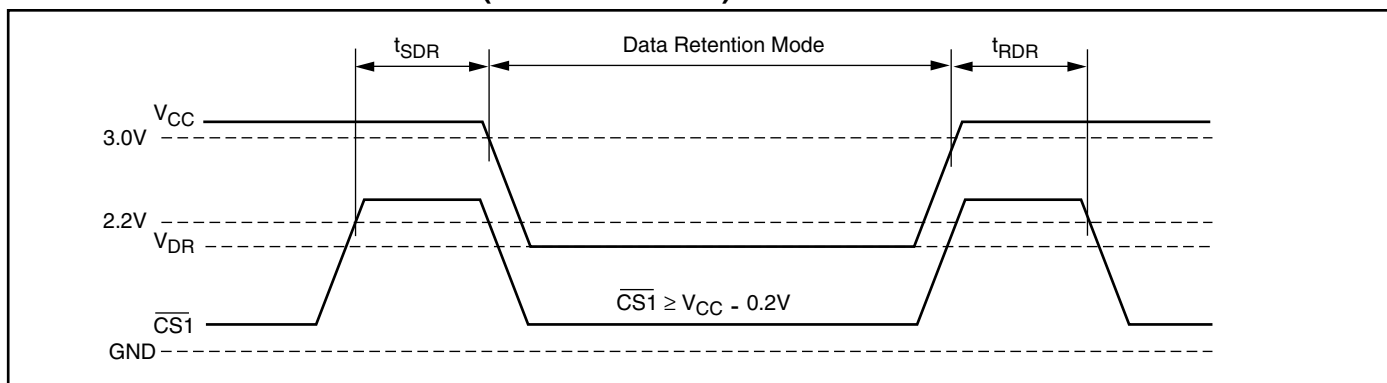
Note:

1. Typical values are measured at $V_{CC} = V_{DR}(\min)$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM (CS2 Controlled)



DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



Note: CS2 must satisfy either $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$

ORDERING INFORMATION
IS62WV2568DALL (1.8 ± 10%)
Industrial Range: –40°C to +85°C

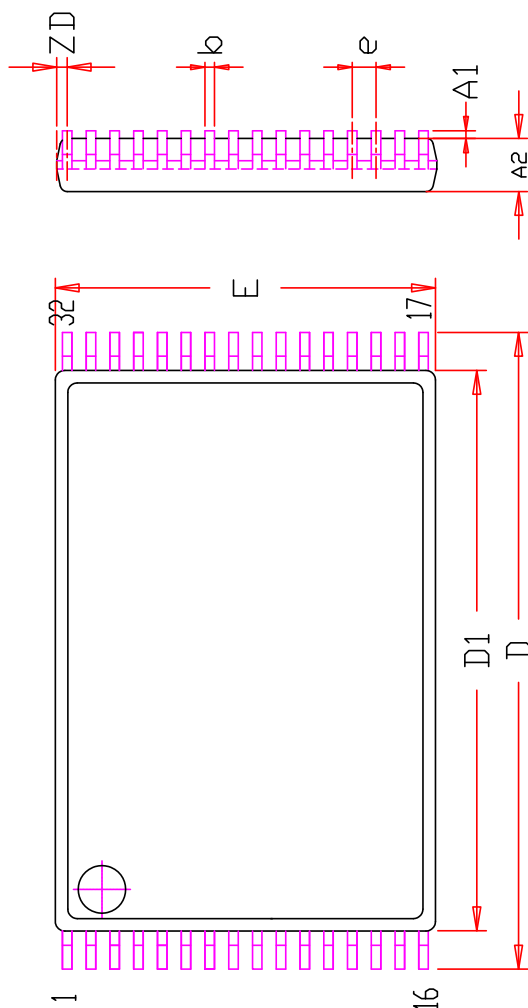
Speed (ns)	Order Part No.	Package
55	IS62WV2568DALL-55TI	TSOP, TYPE I
55	IS62WV2568DALL-55TLI	TSOP, TYPE I, Lead-free
55	IS62WV2568DALL-55BI	mini BGA (6mm x 8mm)
55	IS62WV2568DALL-55BLI	mini BGA (6mm x 8mm), Lead-free
55	IS62WV2568DALL-55HI	sTSOP, TYPE I
55	IS62WV2568DALL-55HLI	sTSOP, TYPE I, Lead-free

IS62WV2568DBLL (2.5V - 3.6V)
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
35	IS62WV2568DBLL-35HLI	sTSOP, TYPE I
35	IS62WV2568DBLL-35TLI	TSOP, TYPE I, Lead-free
45	IS62WV2568DBLL-45TI	TSOP, TYPE I
45	IS62WV2568DBLL-45TLI	TSOP, TYPE I, Lead-free
45	IS62WV2568DBLL-45BI	mini BGA (6mm x 8mm)
45	IS62WV2568DBLL-45BLI	mini BGA (6mm x 8mm), Lead-free
45	IS62WV2568DBLL-45HI	sTSOP, TYPE I
45	IS62WV2568DBLL-45HLI	sTSOP, TYPE I, Lead-free

IS65WV2568DBLL (2.5V - 3.6V)
Automotive Range (A3): –40°C to +125°C

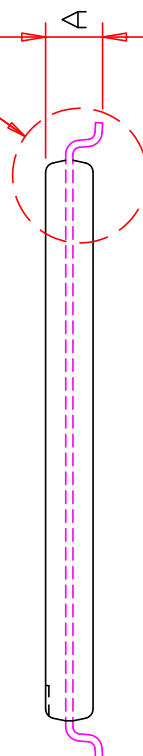
Speed (ns)	Order Part No.	Package
45	IS65WV2568DBLL-45TLA3	TSOP, TYPE I, Lead-free
45	IS65WV2568DBLL-45HLA3	sTSOP, TYPE I, Lead-free



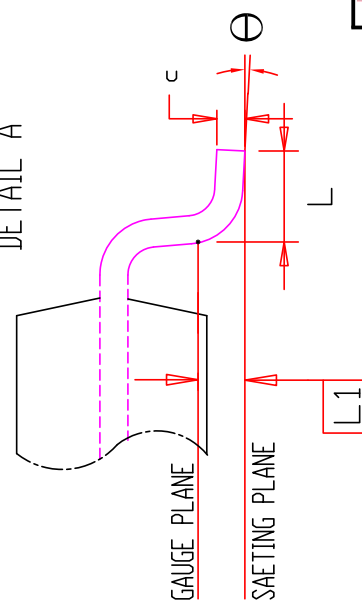
NOTE :

1. Controlling Dimension : mm
2. Dimension D1 and E do not include mold protrusion.
3. Dimension b does not include dambar protrusion/intrusion.
4. Reference Document : JEDEC MO-183
5. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

DETAIL A



DETAIL A



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°
c	0.10		0.21	0.004		0.008

CASE 2



TITLE

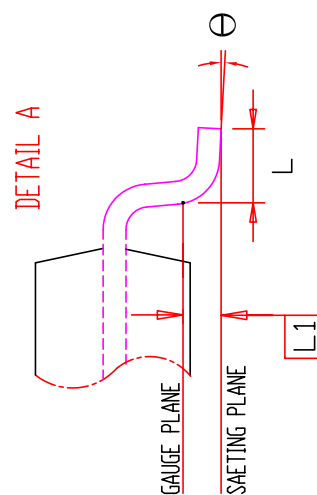
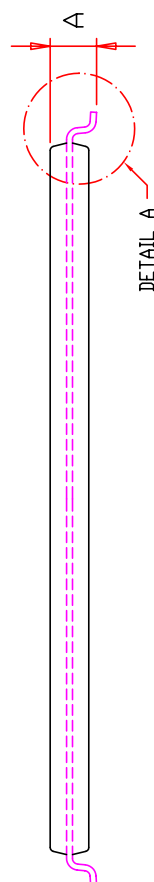
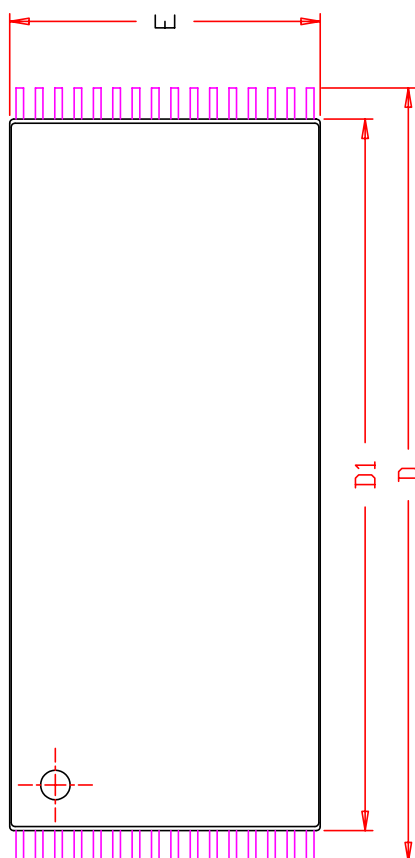
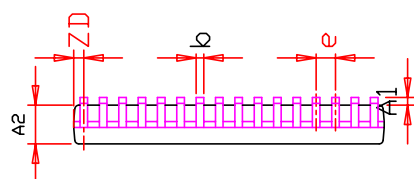
32L 8x13.4mm TSOP-1
Package Outline

REV.

F

DATE

06/21/2017



NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00		1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e		0.50 BSC.	
L	0.40		0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
Θ	0	5°	8°



32L 8x20mm TSOP-1
Package Outline

REV.

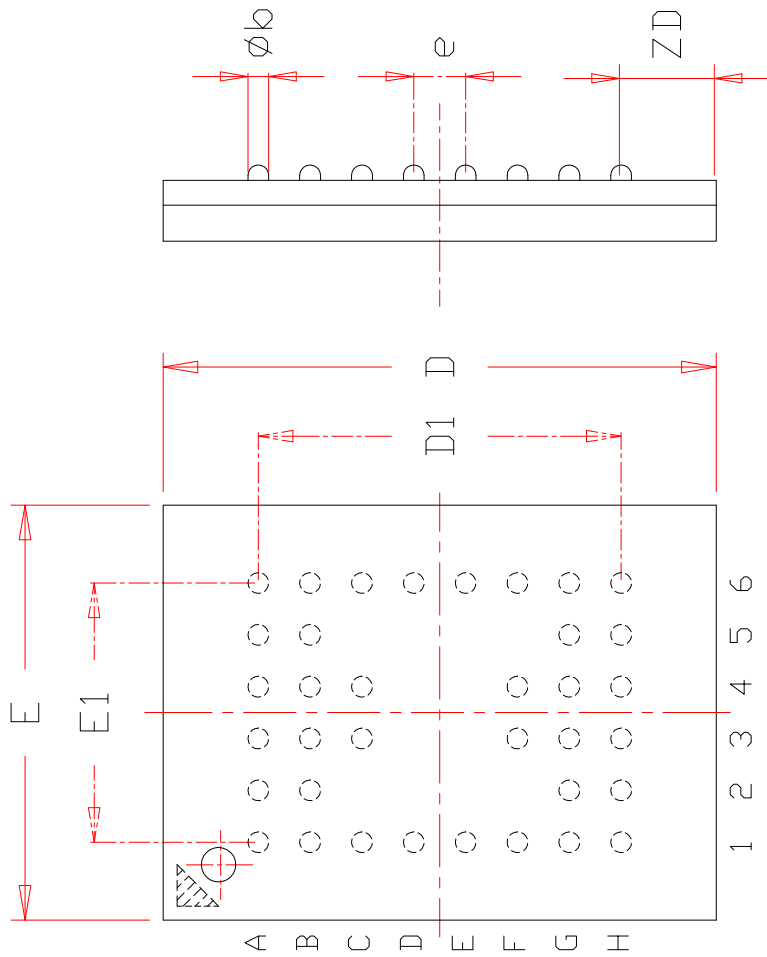
E

DATE

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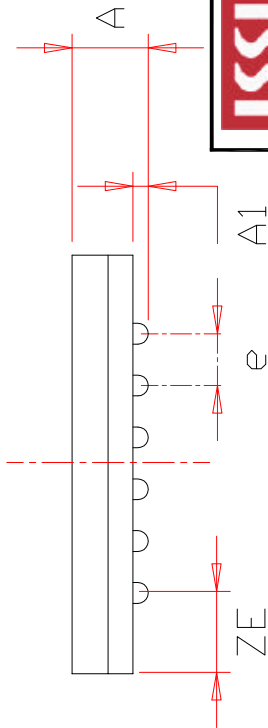
TOP VIEW



NOTE :

- 1. CONTROLLING DIMENSION : MM .
- 2. Reference document : JEDEC MO-207

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC.			0.207 BSC.		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC.			0.148 BSC.		
e	0.75 BSC.			0.030 BSC.		
ZD	1.375 REF.			0.054 REF.		
ZE	1.125 REF.			0.044 REF.		



ISSI	TITLE	36/48L 6x8mm TF-BGA Package Outline	REV.	E	DATE	08/12/2008