



Very Fast, Complete 10- or 12-Bit A/D Converters

AD578/AD579

FEATURES

Performance

Complete 12-Bit A/D Converter with Reference and Clock

Fast Conversion: 3 μ s (max)

**Buried Zener Reference for Long Term Stability and Low Gain T.C.: ± 30 ppm/ $^{\circ}$ C max (AD578)
 ± 40 ppm/ $^{\circ}$ C max (AD579)**

Max Nonlinearity: $< \pm 0.012\%$

No Missing Codes Over Temperature

Low Power: 555 mW (AD578); 775 mW (AD579)

Available to MIL-STD-883

Versatility

Positive-True Parallel or Serial Logic Outputs

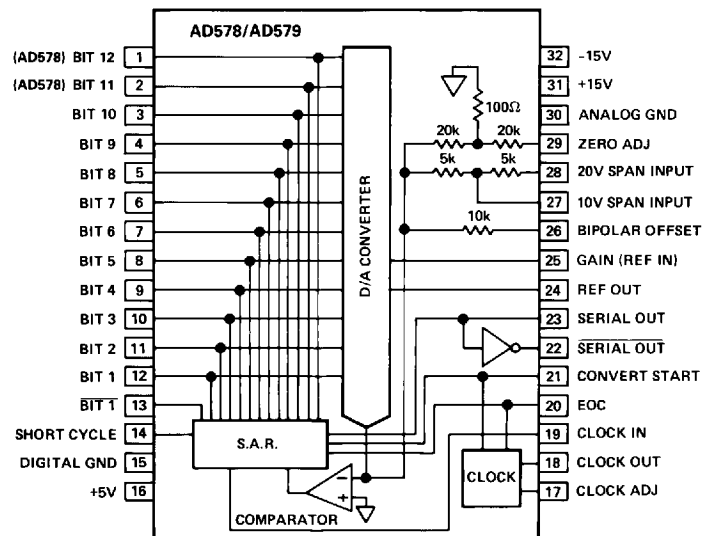
Short Cycle Capability

Precision ± 10 V Reference for External Applications

Adjustable Internal Clock

"Z" Models for ± 12 V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 and AD579 are high speed 12-bit and 10-bit successive approximation analog-to-digital converters that include internal clock, reference, and comparator. Their hybrid design utilizes MSI digital and linear ICs in conjunction with a 12-bit or 10-bit monolithic, monotonic DAC to provide superior performance and versatility with IC size, price, and reliability.

Important performance characteristics of the AD578 include $\pm 1/2$ LSB₁₂ linearity error maximum at $+25^{\circ}$ C, maximum gain tempco of ± 30 ppm/ $^{\circ}$ C, and maximum conversion time of 3 μ s at a typical power dissipation of 555 mW. The 10-bit AD579 provides $\pm 1/2$ LSB₁₀ maximum linearity error at 1.8 μ s maximum, and 775 mW typical P_D.

Both the AD578 and AD579 include scaling resistors that provide analog input signal ranges of ± 5 V, ± 10 V, and 0 to $+10$ V. Both are contained in 32-pin ceramic side-brazed DIP packages, and are available with MIL-STD-883 Class B processing.

PRODUCT HIGHLIGHTS

1. Both are complete analog-to-digital converters. No external components are required to perform a conversion.
2. The fast conversion rates—3 μ s for the AD578, and 1.8 μ s for the AD579—make them ideal candidates for high speed data acquisition systems requiring high throughput.
3. The internal buried Zener reference is laser trimmed to high initial accuracy and low T.C. and is available externally.
4. Precision thin film scaling resistors on the DAC provide for excellent thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolution.

REV. A

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AD578/AD579—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Model	AD578J	AD578K	AD578L	AD578SD ¹	AD578TD ¹
RESOLUTION	12 Bits	*	*	*	*
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±5.0 V, ±10 V	*	*	*	*
Unipolar	0 to +10 V, 0 to +20 V	*	*	*	*
Input Impedance					
0 to +10 V, ±5 V	5 kΩ	*	*	*	*
±10 V, 0 to +20 V	10 kΩ	*	*	*	*
DIGITAL INPUTS					
Convert Command ²	1 LSTTL Load	*	*	*	*
Clock Input	1 LSTTL Load	*	*	*	*
TRANSFER CHARACTERISTICS					
Gain Error ^{3, 4}	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Unipolar Offset ⁴	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Bipolar Error ^{4, 5}	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Linearity Error, +25°C	±1/2 LSB max	*	*	*	*
T _{min} to T _{max}	±3/4 LSB	*	*	±3/4 LSB max	±3/4 LSB max
DIFFERENTIAL LINEARITY ERROR					
(Minimum resolution for which no missing codes are guaranteed)					
+25°C	12 Bits	*	*	*	*
T _{min} to T _{max}	12 Bits	*	*	*	*
POWER SUPPLY SENSITIVITY					
+15 V ±10%	0.005%/ΔV _S max	*	*	*	*
-15 V ±10%	0.005%/ΔV _S max	*	*	*	*
+5 V ±10%	0.005%/ΔV _S max	*	*	*	*
TEMPERATURE COEFFICIENTS					
Gain	±15 ppm/°C typ	*	*	*	*
	±30 ppm/°C max	*	*	±50 ppm/°C max	±30 ppm/°C max
Unipolar Offset	±3 ppm/°C typ	*	*	*	*
	±10 ppm/°C max	*	*	±15 ppm/°C max	±10 ppm/°C max
Bipolar Offset	±8 ppm/°C typ	*	*	*	*
	±20 ppm/°C max	*	*	±25 ppm/°C max	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ	*	*	*	*
CONVERSION TIME ^{6, 7, 8} (max)	6.0 μs	4.5 μs	3 μs	6.0 μs	4.5 μs
PARALLEL OUTPUTS					
Unipolar Code	Binary	*	*	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*	*	*
Output Drive	2 LSTTL Loads	*	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)					
Unipolar Code	Binary/Complementary Binary	*	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*	*
Output Drive	2 LSTTL Loads	*	*	*	*
END OF CONVERSION (EOC)					
Output Drive	Logic "1" During Conversion	*	*	*	*
	8 LSTTL Loads	*	*	*	*
INTERNAL CLOCK ⁸					
Output Drive	2 LSTTL Loads	*	*	*	*
INTERNAL REFERENCE					
Voltage	10.000 ±100 mV	*	*	*	*
Drift	±12 ppm/°C, ±20 ppm/°C max	*	*	*	*
External Current	±1 mA max	*	*	*	*
POWER SUPPLY REQUIREMENTS ⁹					
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*
Supply Current +15 V	5 mA typ, 8 mA max	*	*	*	*
-15 V	22 mA typ, 35 mA max	*	*	*	*
+5 V	30 mA typ, 40 mA max	*	*	*	*
Power Dissipation	555 mW typ	*	*	*	*
TEMPERATURE RANGE					
Operating	0 to +70°C	*	*	-55°C to +125°C	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*	*

NOTES

¹Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.

²Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

³With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.

⁴Adjustable to zero.

⁵With 50 Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

⁶Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

⁷Each grade is specified at the conversion speed shown.

⁸Externally adjustable by a resistor or capacitor (see Figure 6).

⁹For "Z" models order AD578ZJ, ZK, ZL (±11.6 V to ±16.5 V).

*Specifications same as AD578J.

Specifications subject to change without notice.

Model	AD579JN	AD579KN	AD579TD ¹
RESOLUTION	10 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	$\pm 5.0 \text{ V}$, $\pm 10 \text{ V}$	*	*
Unipolar	0 to $+10 \text{ V}$, 0 to $+20 \text{ V}$	*	*
Input Impedance			
0 to $+10 \text{ V}$, $\pm 5 \text{ V}$	5 k Ω ($\pm 20\%$)	*	*
$\pm 10 \text{ V}$, 0 to $+20 \text{ V}$	10 k Ω ($\pm 20\%$)	*	*
DIGITAL INPUTS			
Convert Command ²	1 LSTTL Load	*	*
Clock Input	1 LSTTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error ^{3, 4}	$\pm 0.1\%$ FSR ($\pm 0.25\%$ FSR max)	*	*
Unipolar Offset ³	$\pm 0.1\%$ FSR ($\pm 0.25\%$ FSR max)	*	*
Bipolar Error ^{3, 4}	$\pm 0.1\%$ FSR ($\pm 0.25\%$ FSR max)	*	*
Linearity Error, $+25^\circ\text{C}$	$\pm 1/2$ LSB max	*	*
$T_{\min}$ to $T_{\max}$	$\pm 3/4$ LSB	*	*
DIFFERENTIAL LINEARITY ERROR			
(Minimum resolution for which no missing codes are guaranteed)			
$+25^\circ\text{C}$	10 Bits	*	*
$T_{\min}$ to $T_{\max}$	10 Bits	*	*
POWER SUPPLY SENSITIVITY			
$+15 \text{ V} \pm 10\%$	0.005%/ ΔV_S max	*	*
$-15 \text{ V} \pm 10\%$	0.005%/ ΔV_S max	*	*
$+5 \text{ V} \pm 10\%$	0.001%/ ΔV_S max	*	*
"Z" Versions			
$+12 \text{ V} \pm 5\%$	0.007%/ ΔV_S max	*	*
$-12 \text{ V} \pm 5\%$	0.007%/ ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	± 25 ppm/ $^\circ\text{C}$ typ	*	*
	± 40 ppm/ $^\circ\text{C}$ max	*	*
Unipolar Offset	± 5 ppm/ $^\circ\text{C}$ typ	*	*
	± 15 ppm/ $^\circ\text{C}$ max	*	*
Bipolar Offset	± 8 ppm/ $^\circ\text{C}$ typ	*	*
	± 20 ppm/ $^\circ\text{C}$ max	*	*
Differential Linearity	± 2 ppm/ $^\circ\text{C}$ typ	*	*
CONVERSION TIME ^{5, 6} (max)	2.2 μs	1.8 μs	**
Conversion Time $T_{\min}$ to $T_{\max}$	2.4 μs	2.0 μs	**
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*
Output Drive	2 LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2 LSTTL Loads	*	*
END OF CONVERSION (EOC)			
Output Drive	Logic "1" During Conversion	*	*
	8 LSTTL Loads	*	*
INTERNAL CLOCK ⁷			
Output Drive	2 LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 $\pm 10 \text{ mV}$ typ	*	*
Temperature Coefficient	15 ppm/ $^\circ\text{C}$	*	*
External Current	$\pm 1 \text{ mA}$ max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ± 13.5 to ± 16.5	*	*
Z Models ⁸	4.75 to 5.25 and ± 11.4 to ± 16.5	*	*
Supply Current $+15 \text{ V}$	5 mA typ, 8 mA max	*	*
-15 V	22 mA typ, 35 mA max	*	*
$+5 \text{ V}$	100 mA typ, 150 mA max	*	*
Power Dissipation	775 mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to $+70^\circ\text{C}$	*	-55°C to $+125^\circ\text{C}$
Storage	-65°C to $+150^\circ\text{C}$	*	*

NOTES

¹Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.²Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.³With 50 Ω , 1% fixed resistor in place of gain adjust potentiometer.⁴Adjustable to zero.⁵With 50 Ω , 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).⁶Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.⁷Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.⁸Externally adjustable by a resistor or capacitor.⁹For "Z" models order AD579ZJN, AD579ZKN or AD579ZTD.

*Specifications same as AD579JN.

**Specifications same as AD579KN.

Specifications subject to change without notice.

ORDERING GUIDE¹

Model	Resolution	Conversion Speed	Temperature Range	Package Option ²
AD578JN (JD)	12 Bits	6.0 μ s	0°C to +70°C	DH-32B
AD578KN (KD)	12 Bits	4.5 μ s	0°C to +70°C	DH-32B
AD578LN (LD)	12 Bits	3.0 μ s	0°C to +70°C	DH-32B
AD578SD	12 Bits	6.0 μ s	-55°C to +125°C	DH-32B
AD578TD	12 Bits	4.5 μ s	-55°C to +125°C	DH-32B
AD578SD/883B	12 Bits	6.0 μ s	-55°C to +125°C	DH-32B
AD578TD/883B	12 Bits	4.5 μ s	-55°C to +125°C	DH-32B
AD579JN	10 Bits	2.2 μ s	0°C to +70°C	DH-32B
AD579KN	10 Bits	1.8 μ s	0°C to +70°C	DH-32B
AD579TD	10 Bits	1.8 μ s	-55°C to +125°C	DH-32B
AD579TD/883B	10 Bits	1.8 μ s	-55°C to +125°C	DH-32B

NOTES

¹For ± 12 V operation "Z" Version, order AD578ZTD

THEORY OF OPERATION

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

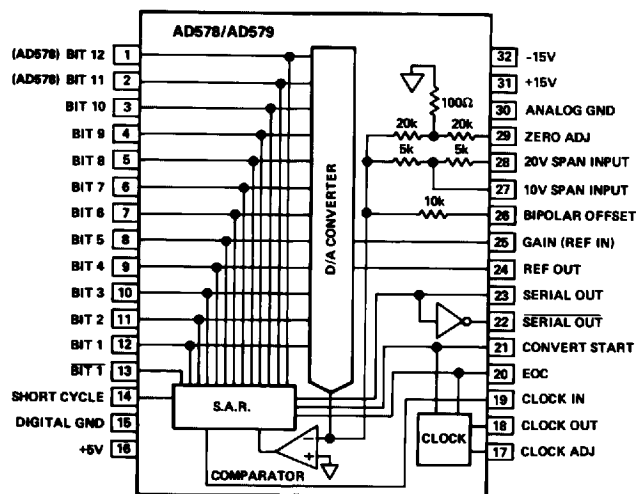
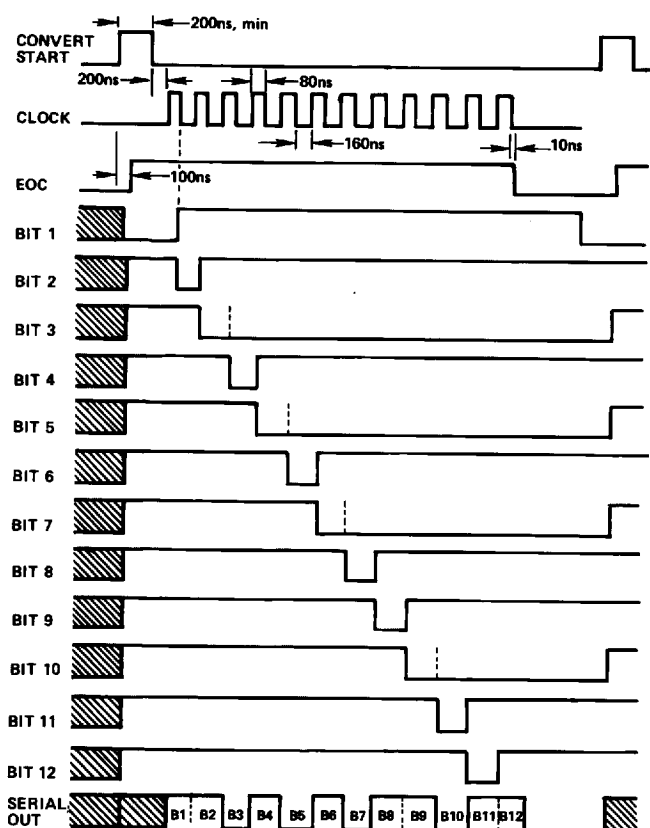


Figure 1. AD578/AD579 Functional Block Diagram and Pinout

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The data bits are valid on the falling edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within $\pm 1/2$ LSB.



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH
MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
¹THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2a. AD578 3 μ s Timing Diagram

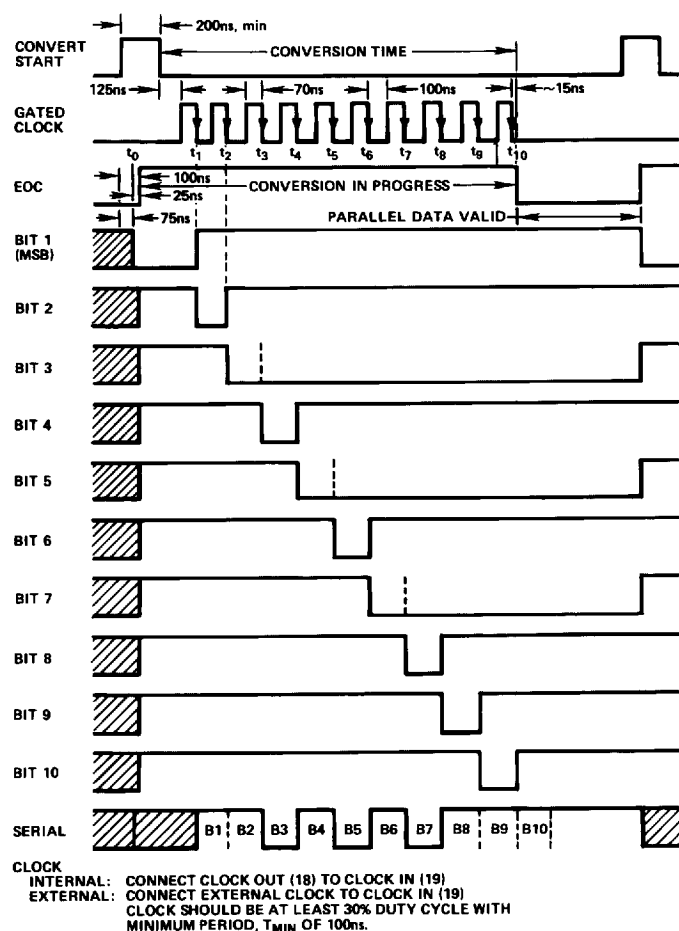


Figure 2b. AD579 Timing Diagram

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts $\pm 1.0\%$, it is buffered and can supply up to 1.0 mA to an external load in addition to the current required to drive the reference input resistor (0.5 mA) and bipolar offset resistor (1 mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5 k Ω input scaling resistors to allow either a 10 volt or 20

volt span. The 10 k Ω bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578/AD579 is intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB.

If Pin 26 is connected to Pin 30, the unit will behave in this manner, within specifications. Refer to Table I, Table II, and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ± 25 mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale. Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

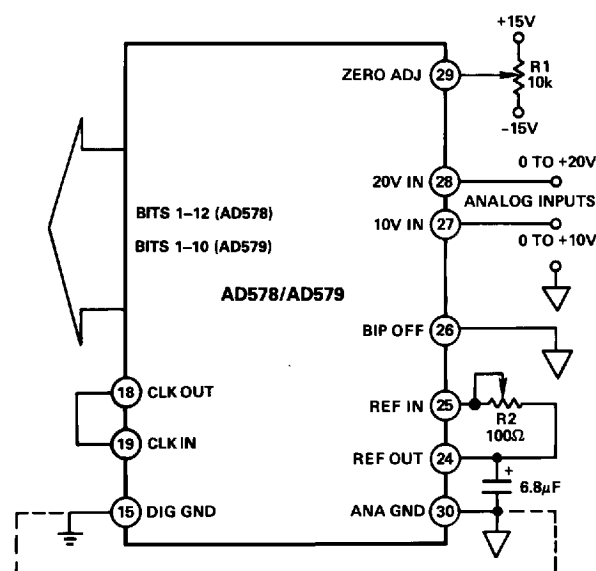


Figure 3. Unipolar Input Connections

Table I. AD578 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input-Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10 V Range	0 to +20 V Range	-5 V to +5 V Range	-10 V to +10 V Range	B1 (MSB)	B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1	1
+9.9952	+19.9902	+4.9952	+9.9902	1	1
•	•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1	0
+5.0000	+10.0000	+0.0000	+0.0000	1	0
•	•	•	•	•	•
+0.0024	+0.0051	-4.9976	-9.9951	0	0
+0.0000	+0.0000	-5.0000	-10.0000	0	0

Table II. AD579 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input-Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10 V Range	0 to +20 V Range	-5 V to +5 V Range	-10 V to +10 V Range	B1 (MSB)	B12 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 1 1 0	
•	•	•	•	•	
•	•	•	•	•	
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0	
•	•	•	•	•	
•	•	•	•	•	
+0.0097	+0.0195	-4.9902	-9.9804	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0 0 0 0 0 0 0 0 0	

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100 Ω trimmer shown can be replaced by a 50 $\Omega \pm 1\%$ fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale is applied and R2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

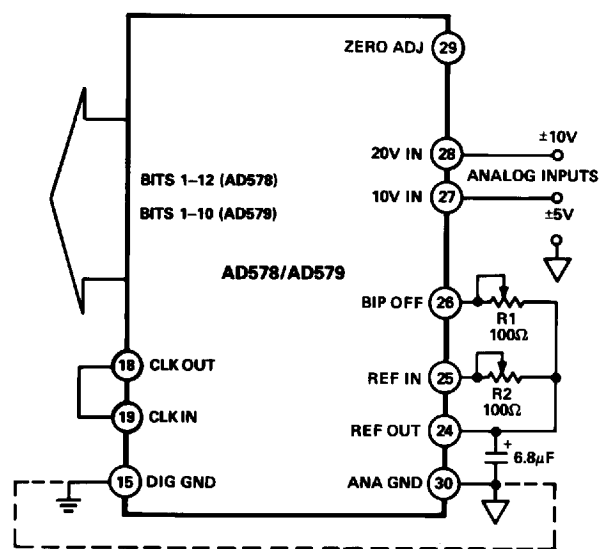


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578 or AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

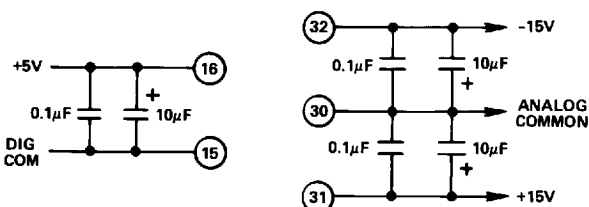


Figure 5. Basic Bypassing Practice

Each of the AD578 or AD579 supply terminals should be capacitively decoupled as close to the ADC as possible. A large value capacitor such as 10 μF in parallel with a 0.1 μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8 μF capacitor to Pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of $5.6 \mu\text{s}$ (AD578) or $4.8 \mu\text{s}$ (AD579). It can be adjusted for either faster or slower conversion rates. For faster conversions connect the appropriate 1% resistor between Pins 17 and 18, and short Pin 18 to Pin 19. See Figure 6 or 7.

For slower conversions (AD578 only) connect a capacitor between Pins 15 and 17.

NOTE: No-Missing-Code operation is not guaranteed when operating in this mode if a particular grade's conversion speed specification is exceeded.

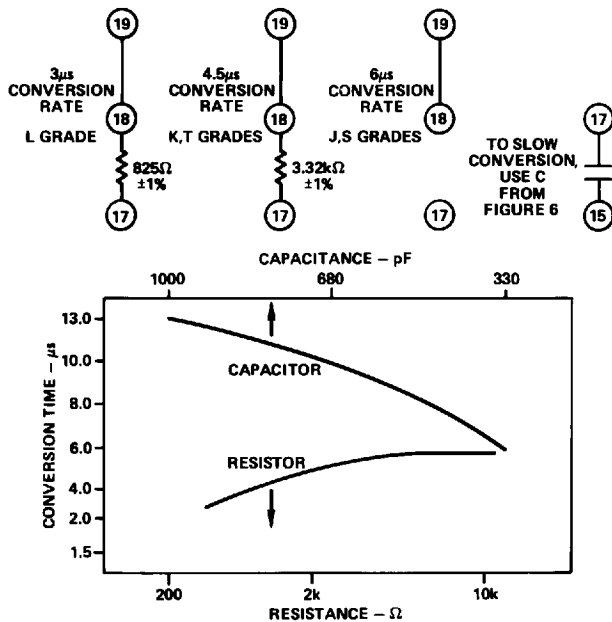


Figure 6. AD578 Conversion Times vs. R or C Values

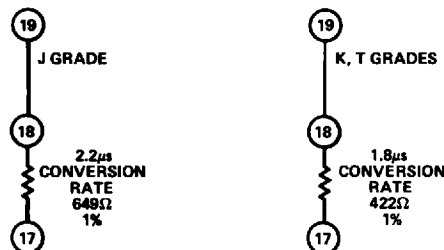


Figure 7. AD579 Clock Rate Control Connection

Short Cycle Input—A short cycle input, Pin 14, permits the timing cycle to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring the full 10-bit (AD579) or 12-bit (AD578) resolution. Short cycle pin connections and associated conversion times are summarized in Tables III and IV.

Table III. AD578 Short Cycle Connections

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table IV. AD579 Short Cycle Connections

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

External Clock—An external clock may be connected directly to the clock input, Pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier—In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD711 should be used.

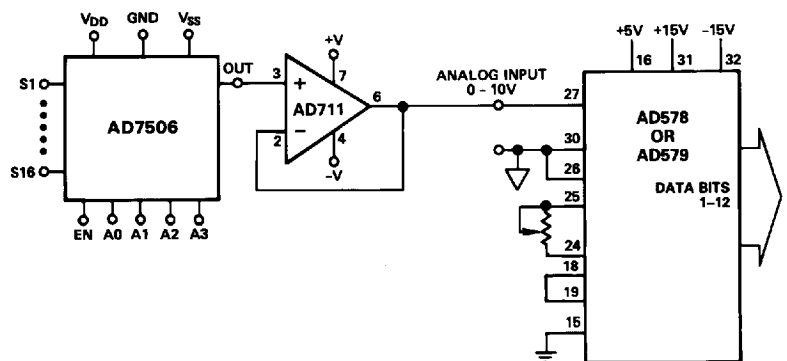


Figure 8. Input Buffer

AD578/AD579

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

