



74HC4017-Q100; 74HCT4017-Q100

Johnson decade counter with 10 decoded outputs

Rev. 3 — 27 March 2024

Product data sheet

1. General description

The 74HC4017-Q100; 74HCT4017-Q100 is a 5-stage Johnson decade counter with 10 decoded outputs (Q0 to Q9), an output from the most significant flip-flop ($\overline{Q}5-9$), two clock inputs (CP0 and $\overline{CP}1$) and an overriding asynchronous master reset input (MR). The counter is advanced by either a LOW-to-HIGH transition at CP0 while $\overline{CP}1$ is LOW or a HIGH-to-LOW transition at $\overline{CP}1$ while CP0 is HIGH. When cascading counters, the $\overline{Q}5-9$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0 = $\overline{Q}5-9$ = HIGH; Q1 to Q9 = LOW) independent of the clock inputs (CP0 and $\overline{CP}1$). Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC4017-Q100: CMOS level
 - For 74HCT4017-Q100: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4017D-Q100 74HCT4017D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4017PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4017BQ-Q100 74HCT4017BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

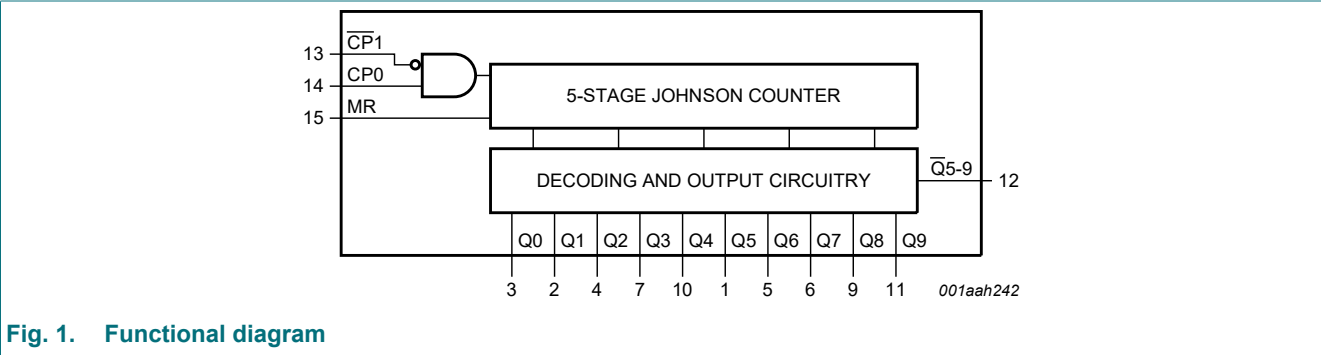


Fig. 1. Functional diagram

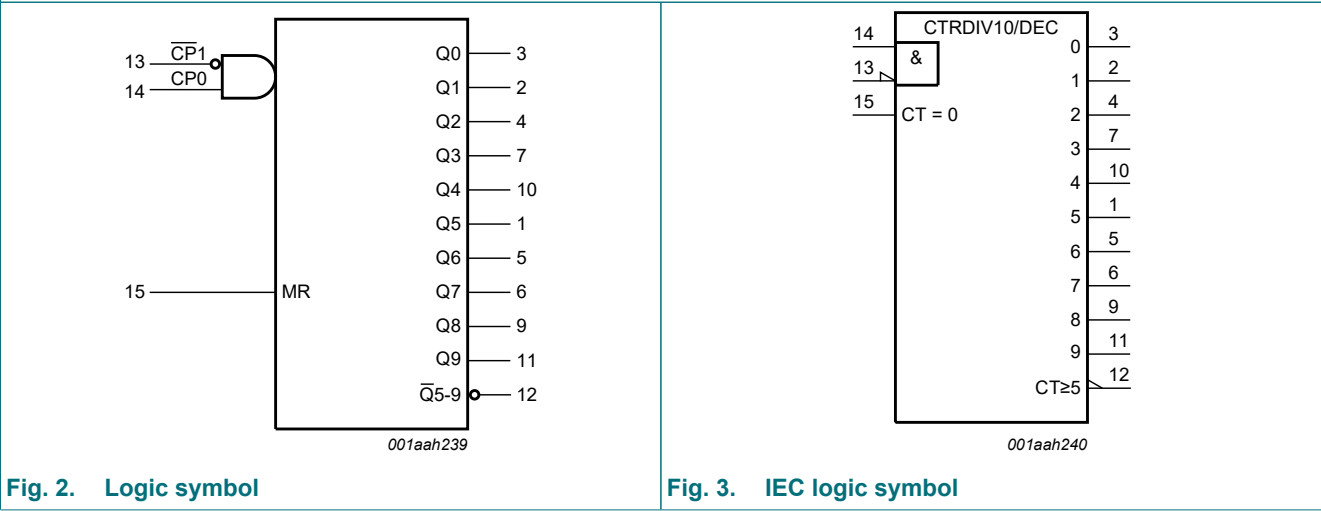


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

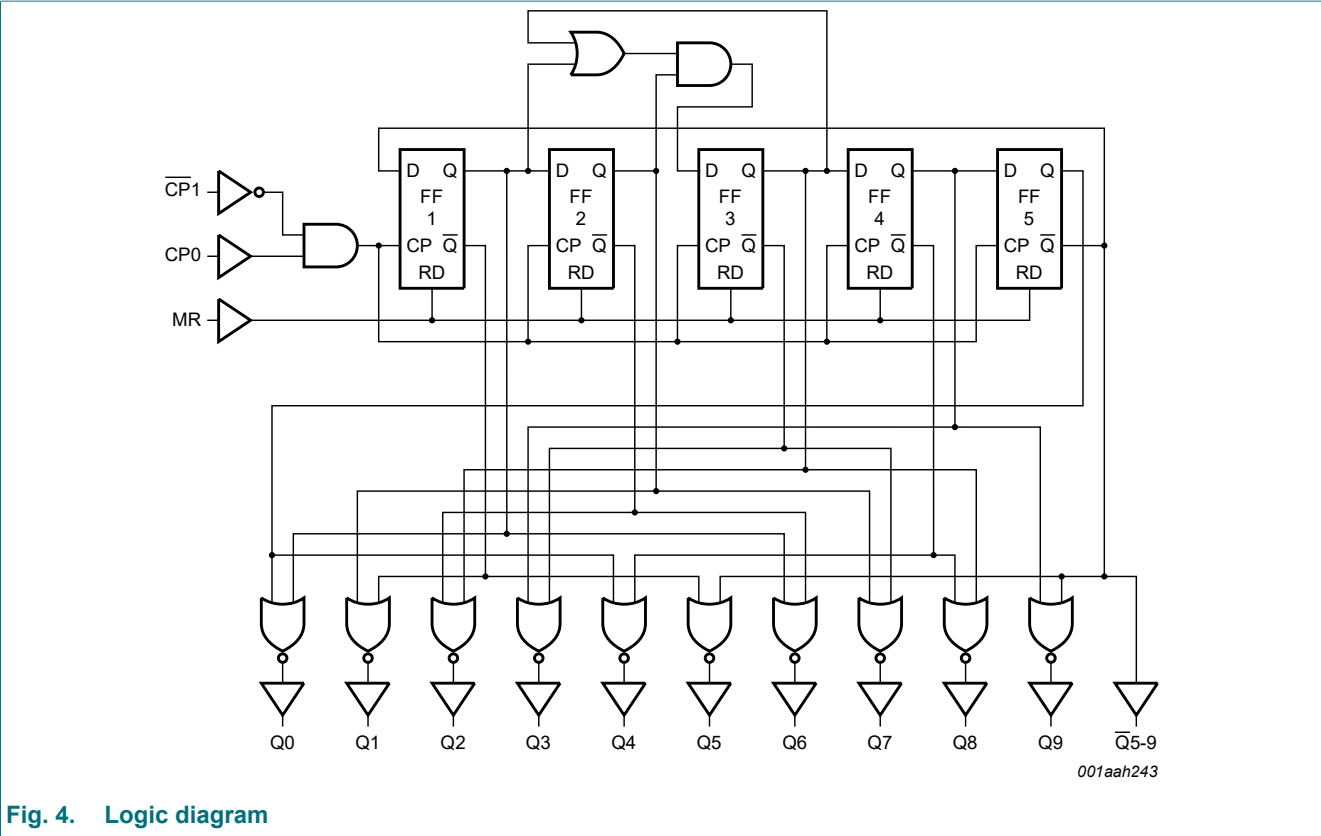


Fig. 4. Logic diagram

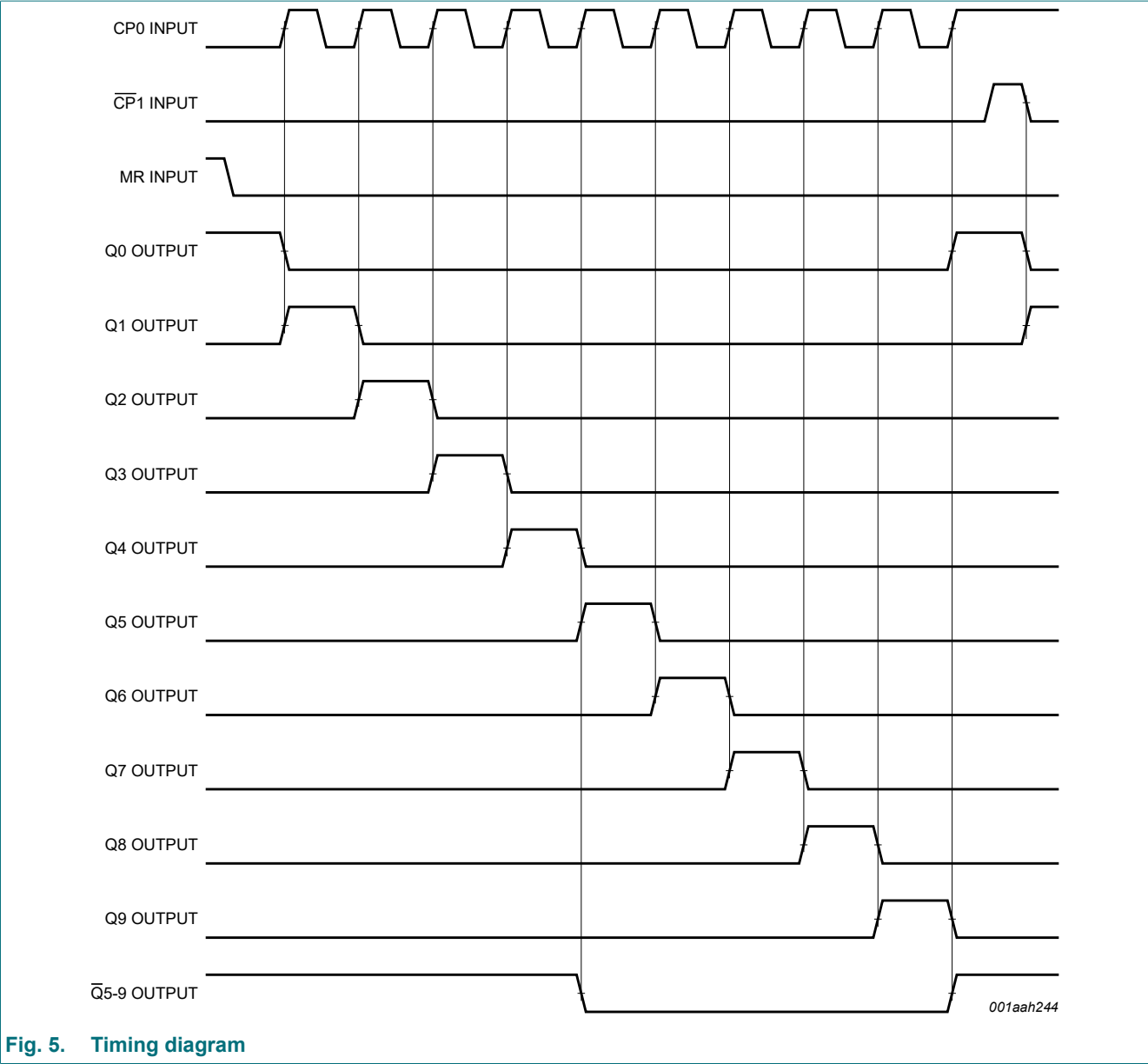
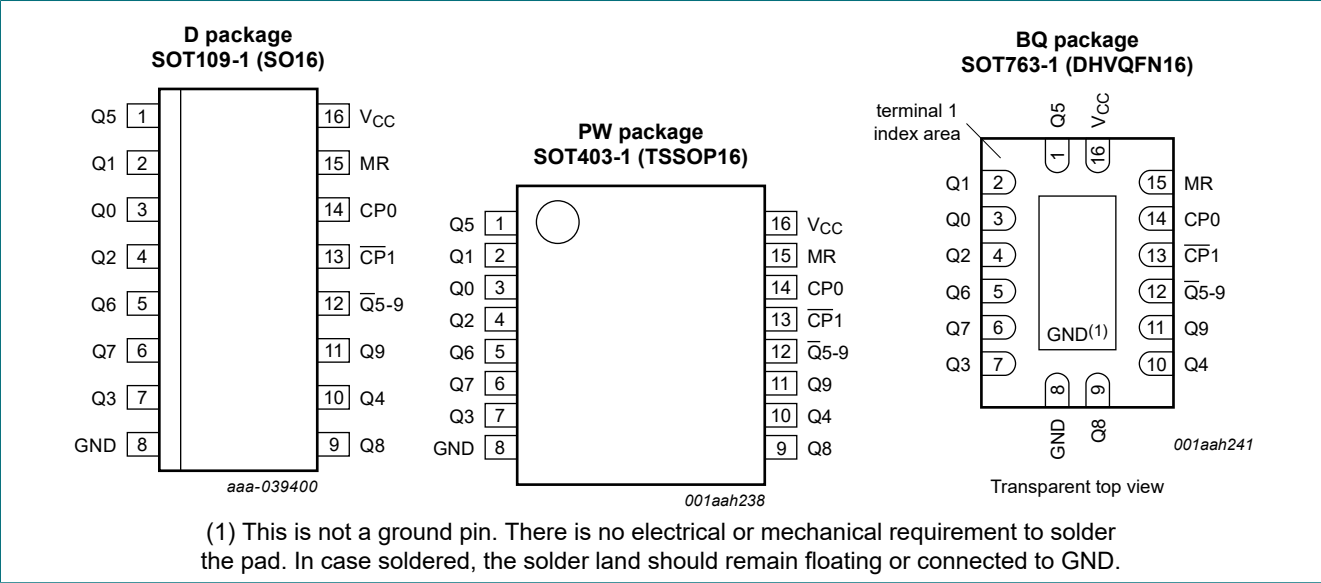


Fig. 5. Timing diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9	3, 2, 4, 7, 10, 1, 5, 6, 9, 11	decoded output
GND	8	ground (0 V)
Q5-9	12	carry output (active LOW)
CP1	13	clock input (HIGH-to-LOW edge-triggered)
CP0	14	clock input (LOW-to-HIGH edge-triggered)
MR	15	master reset input (active HIGH)
VCC	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;

MR	CP0	CP1	Operation
H	X	X	Q0 = Q5-9 = HIGH; Q1 to Q9 = LOW
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4017-Q100			74HCT4017-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4017-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4017-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		CP0 input	-	25	90	-	113	-	123	µA
		CP1 input	-	40	144	-	180	-	196	µA
		MR input	-	50	180	-	225	-	245	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; see Fig. 9.

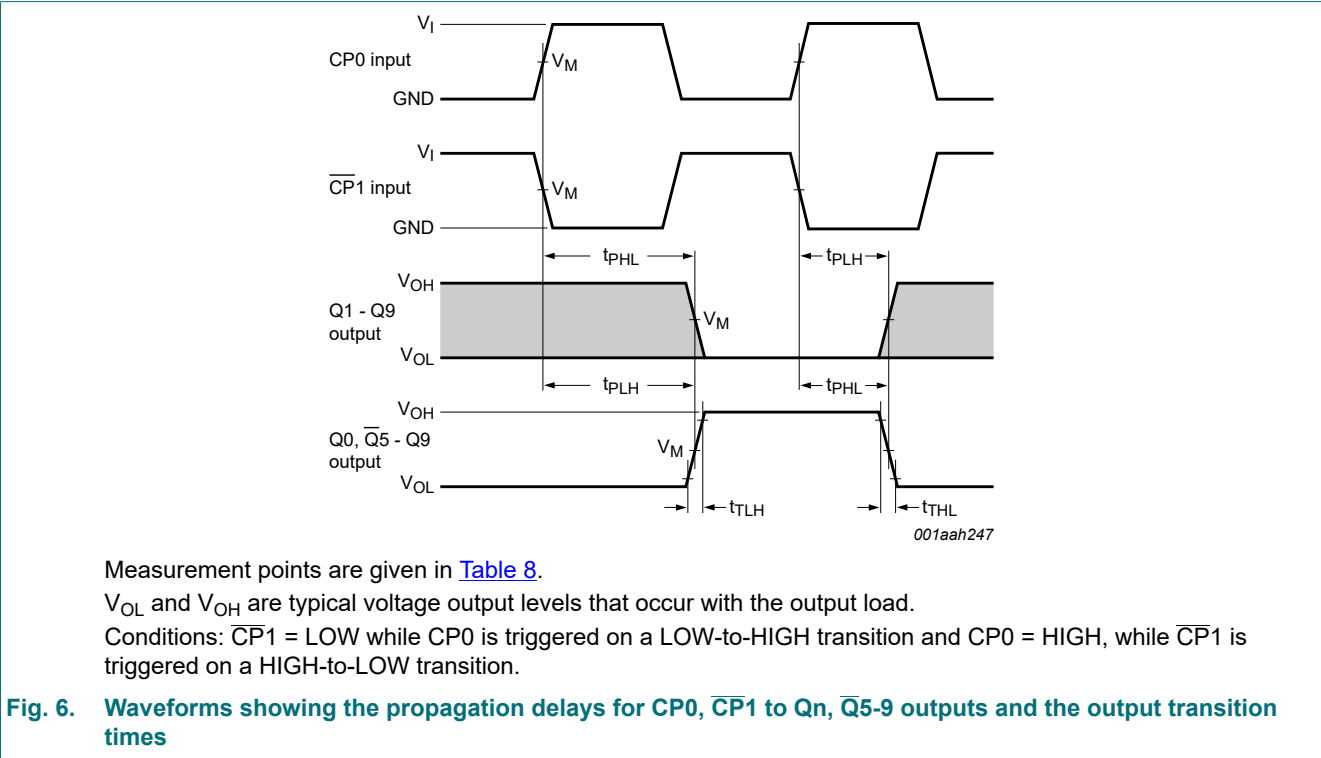
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4017-Q100										
t _{pd}	propagation delay	CP0 to Qn; CP0 to Q̄5-9; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	63	230	-	290	-	345	ns
		V _{CC} = 4.5 V	-	23	46	-	58	-	69	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	18	39	-	49	-	59	ns
		CP̄1 to Qn; CP̄1 to Q̄5-9; see Fig. 6								
		V _{CC} = 2.0 V	-	61	250	-	315	-	375	ns
		V _{CC} = 4.5 V	-	22	50	-	63	-	75	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	18	43	-	54	-	64	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 7								
		V _{CC} = 2.0 V	-	52	230	-	290	-	345	ns
		V _{CC} = 4.5 V	-	19	46	-	58	-	69	ns
		V _{CC} = 6.0 V	-	15	39	-	49	-	59	ns
t _{PLH}	LOW to HIGH propagation delay	MR to Q̄5-9, Q0; see Fig. 7								
		V _{CC} = 2.0 V	-	55	230	-	290	-	345	ns
		V _{CC} = 4.5 V	-	20	46	-	58	-	69	ns
		V _{CC} = 6.0 V	-	16	39	-	49	-	59	ns
t _t	transition time	see Fig. 6 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	CP0 and CP̄1 (HIGH or LOW); see Fig. 7								
		V _{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		MR (HIGH); see Fig. 7								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{su}	set-up time	CP̄1 to CP0; CP0 to CP̄1; see Fig. 8								
		V _{CC} = 2.0 V	50	-8	-	65	-	75	-	ns
		V _{CC} = 4.5 V	10	-3	-	13	-	15	-	ns
		V _{CC} = 6.0 V	9	-2	-	11	-	13	-	ns

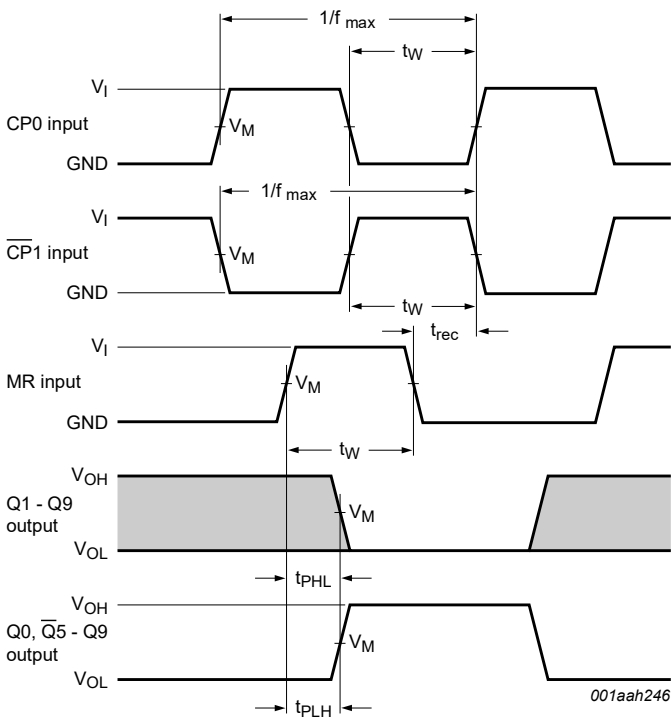
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	$\overline{CP}1$ to $CP0$; $CP0$ to $\overline{CP}1$; see Fig. 8								
		$V_{CC} = 2.0\text{ V}$	50	17	-	65	-	75	-	ns
		$V_{CC} = 4.5\text{ V}$	10	6	-	13	-	15	-	ns
		$V_{CC} = 6.0\text{ V}$	9	5	-	11	-	13	-	ns
t_{rec}	recovery time	MR to $CP0$ and MR to $\overline{CP}1$; see Fig. 7								
		$V_{CC} = 2.0\text{ V}$	5	-17	-	5	-	5	-	ns
		$V_{CC} = 4.5\text{ V}$	5	-6	-	5	-	5	-	ns
		$V_{CC} = 6.0\text{ V}$	5	-5	-	5	-	5	-	ns
f_{max}	maximum frequency	$CP0$ or $\overline{CP}1$; see Fig. 7								
		$V_{CC} = 2.0\text{ V}$	6.0	23	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5\text{ V}$	30	70	-	24	-	20	-	MHz
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	77	-	-	-	-	-	MHz
		$V_{CC} = 6.0\text{ V}$	25	83	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$; $V_{CC} = 5\text{ V}$; $f_i = 1\text{ MHz}$ [3]	-	35	-	-	-	-	-	pF
74HCT4017-Q100										
t_{pd}	propagation delay	$CP0$ to Q_n ; $CP0$ to $\overline{Q}5-9$; see Fig. 6 [1]								
		$V_{CC} = 4.5\text{ V}$	-	25	46	-	58	-	69	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	21	-	-	-	-	-	ns
		$\overline{CP}1$ to Q_n ; $\overline{CP}1$ to $\overline{Q}5-9$; see Fig. 6								
		$V_{CC} = 4.5\text{ V}$	-	25	50	-	63	-	75	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	21	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q_n ; see Fig. 7								
		$V_{CC} = 4.5\text{ V}$	-	22	46	-	58	-	69	ns
t_{PLH}	LOW to HIGH propagation delay	MR to $\overline{Q}5-9$, $Q0$; see Fig. 7								
		$V_{CC} = 4.5\text{ V}$	-	20	46	-	58	-	69	ns
t_t	transition time	see Fig. 6 [2]								
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
t_W	pulse width	$CP0$ and $\overline{CP}1$ (HIGH or LOW); see Fig. 7								
		$V_{CC} = 4.5\text{ V}$	16	7	-	20	-	24	-	ns
		MR (HIGH); see Fig. 7								
		$V_{CC} = 4.5\text{ V}$	16	4	-	20	-	24	-	ns
t_{su}	set-up time	$\overline{CP}1$ to $CP0$; $CP0$ to $\overline{CP}1$; see Fig. 8								
		$V_{CC} = 4.5\text{ V}$	10	-3	-	13	-	15	-	ns
t_h	hold time	$\overline{CP}1$ to $CP0$; $CP0$ to $\overline{CP}1$; see Fig. 8								
		$V_{CC} = 4.5\text{ V}$	10	6	-	13	-	15	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{rec}	recovery time	MR to CP0 and MR to $\overline{\text{CP1}}$; see Fig. 7								
		V _{CC} = 4.5 V	5	-5	-	5	-	5	-	ns
f _{max}	maximum frequency	CP0 or $\overline{\text{CP1}}$; see Fig. 7								
		V _{CC} = 4.5 V	30	61	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	67	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} - 1.5 V; V _{CC} = 5 V; f _i = 1 MHz [3]	-	36	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [2] t_i is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

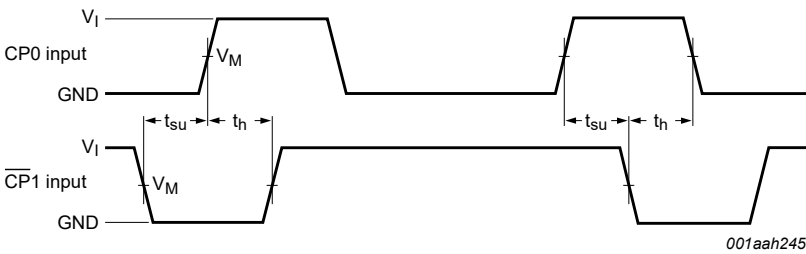
10.1. Waveforms and test circuit





Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the minimum pulse width for CP0, CP1 and MR input; the maximum frequency for CP0 and CP1 input; the recovery time for MR and the MR input to Qn and Q5-9 output propagation delays



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Waveforms showing the set-up and hold times for CP0 to CP1 and CP1 to CP0

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC4017-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4017-Q100	1.3 V	1.3 V

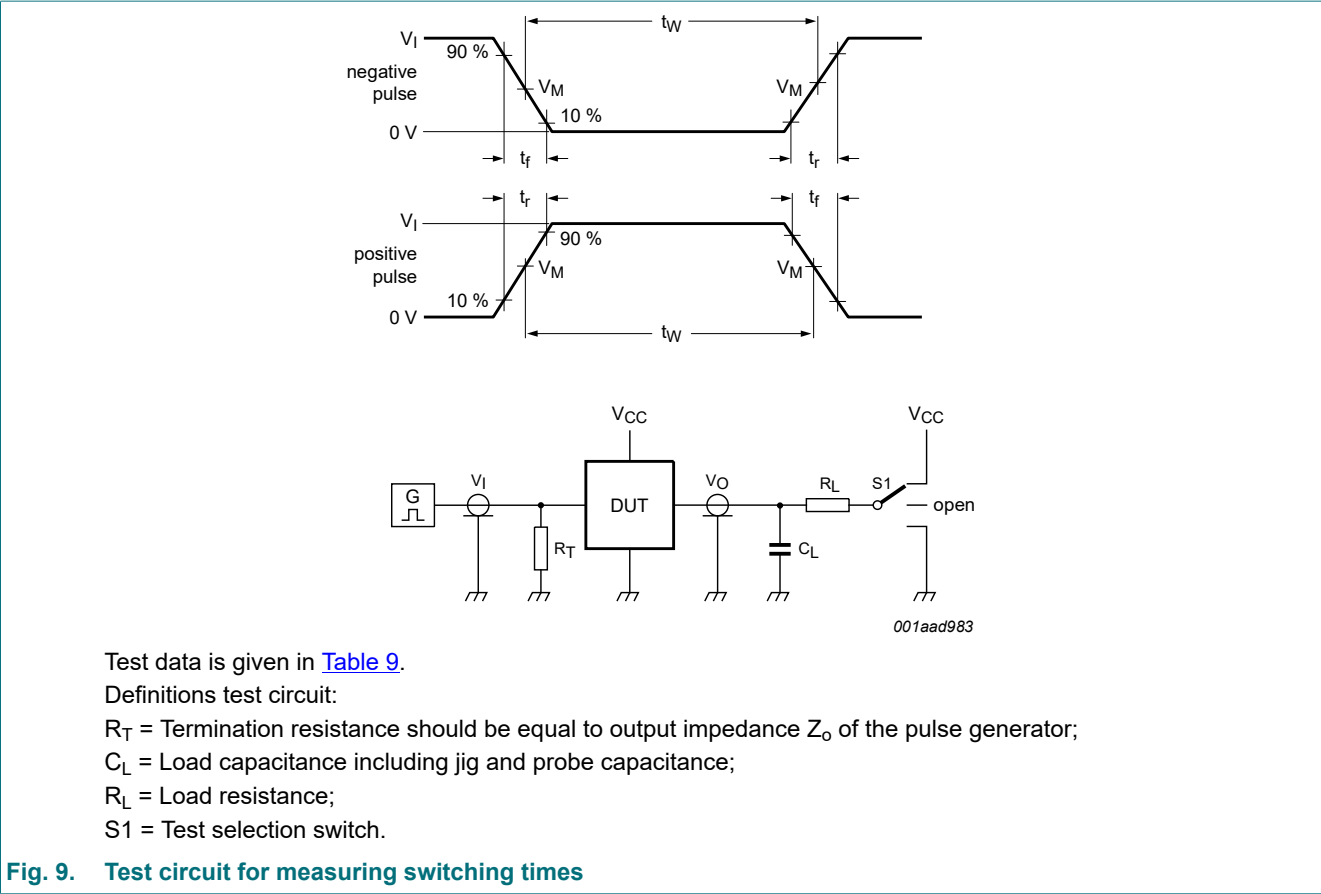


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC4017-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT4017-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Application information

Some examples of applications for the 74HC4017-Q100; 74HCT4017-Q100 are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Fig. 10 shows a technique for extending the number of decoded output states for the 74HC4017-Q100; 74HCT4017-Q100. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

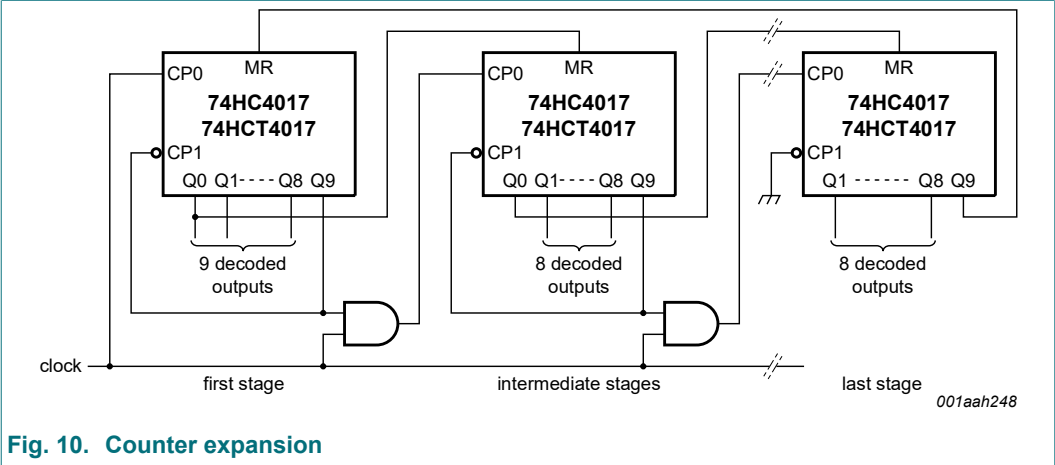


Fig. 10. Counter expansion

Remark: It is essential not to enable the counter on $\overline{CP1}$ when CP0 is HIGH, or on CP0 when $\overline{CP1}$ is LOW, as this would cause an extra count.

Fig. 11 shows an example of a divide-by 2 through divide-by 10 circuit using one 74HC4017-Q100; 74HCT4017-Q100. Since the 74HC4017-Q100; 74HCT4017-Q100 has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting an RC network at the MR input.

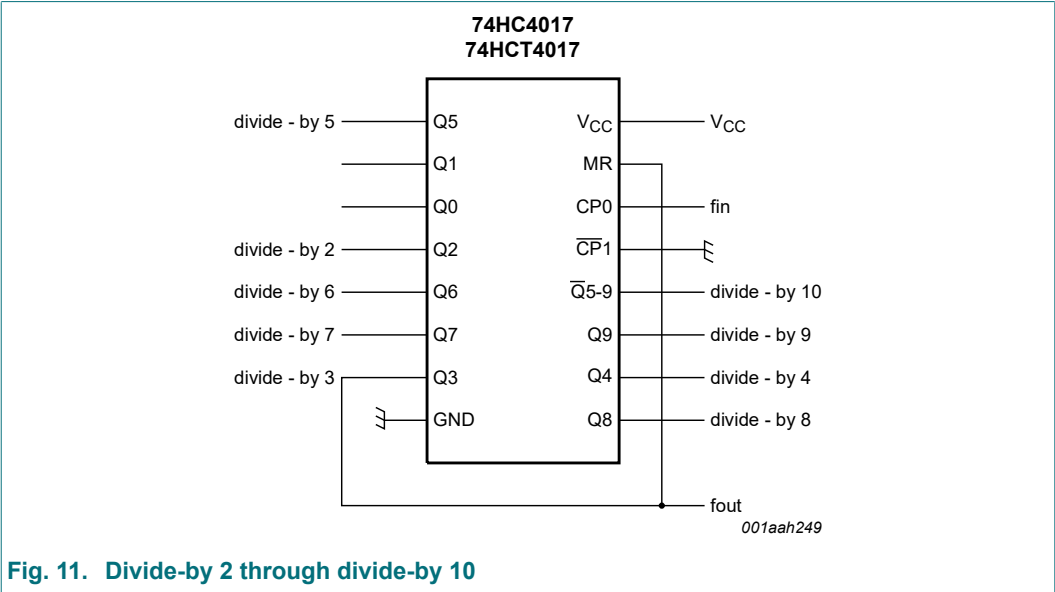


Fig. 11. Divide-by 2 through divide-by 10

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

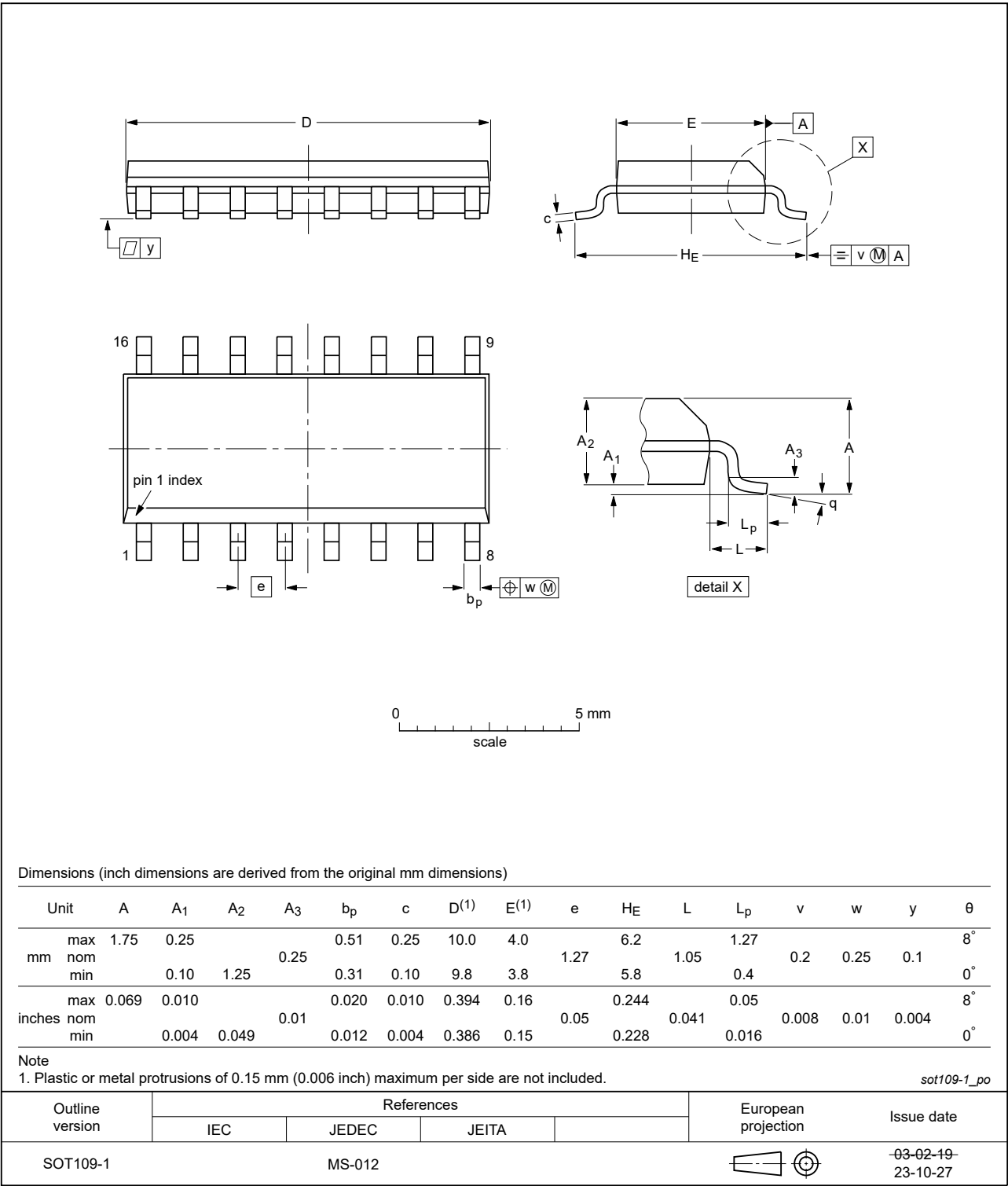


Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

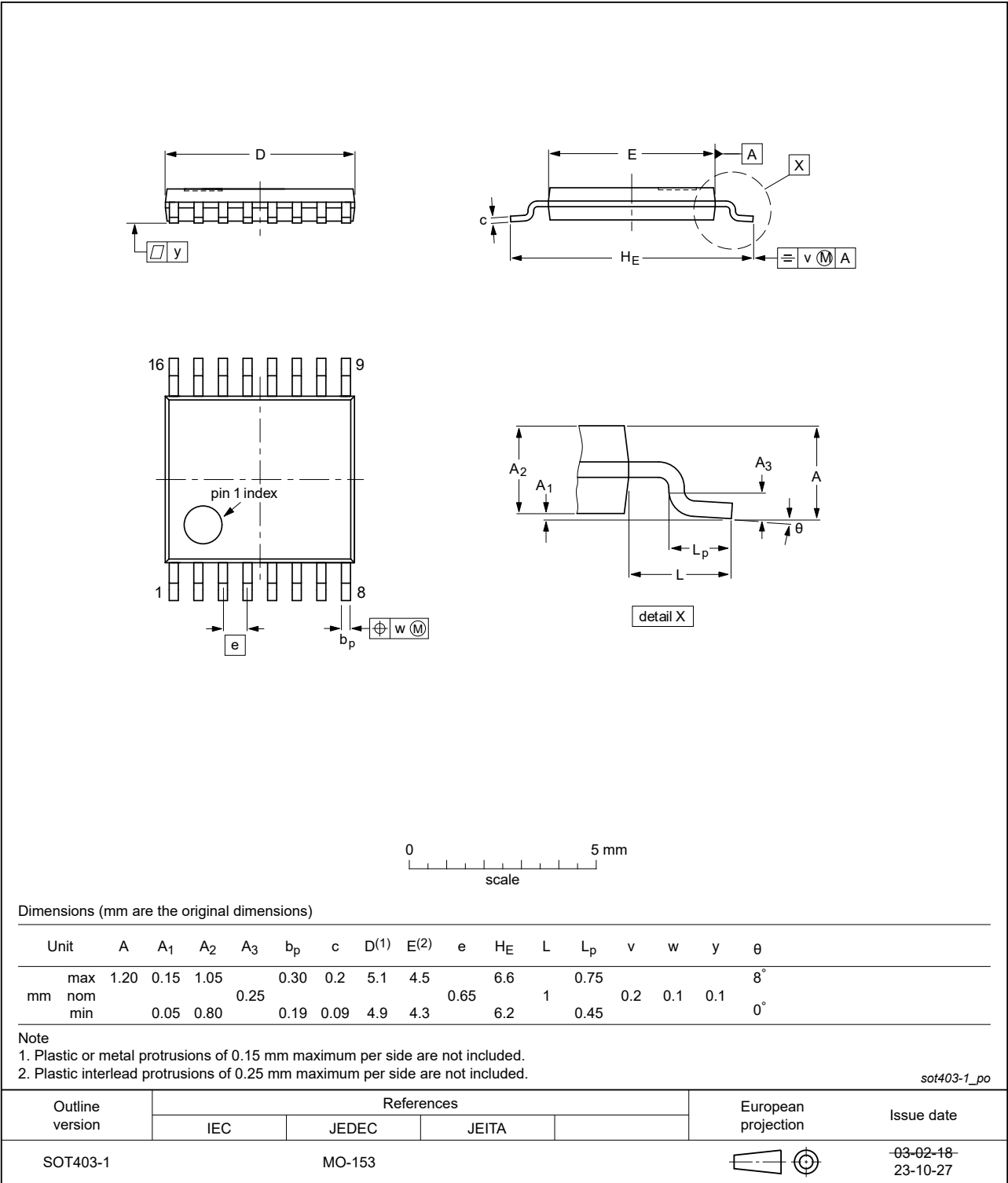


Fig. 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

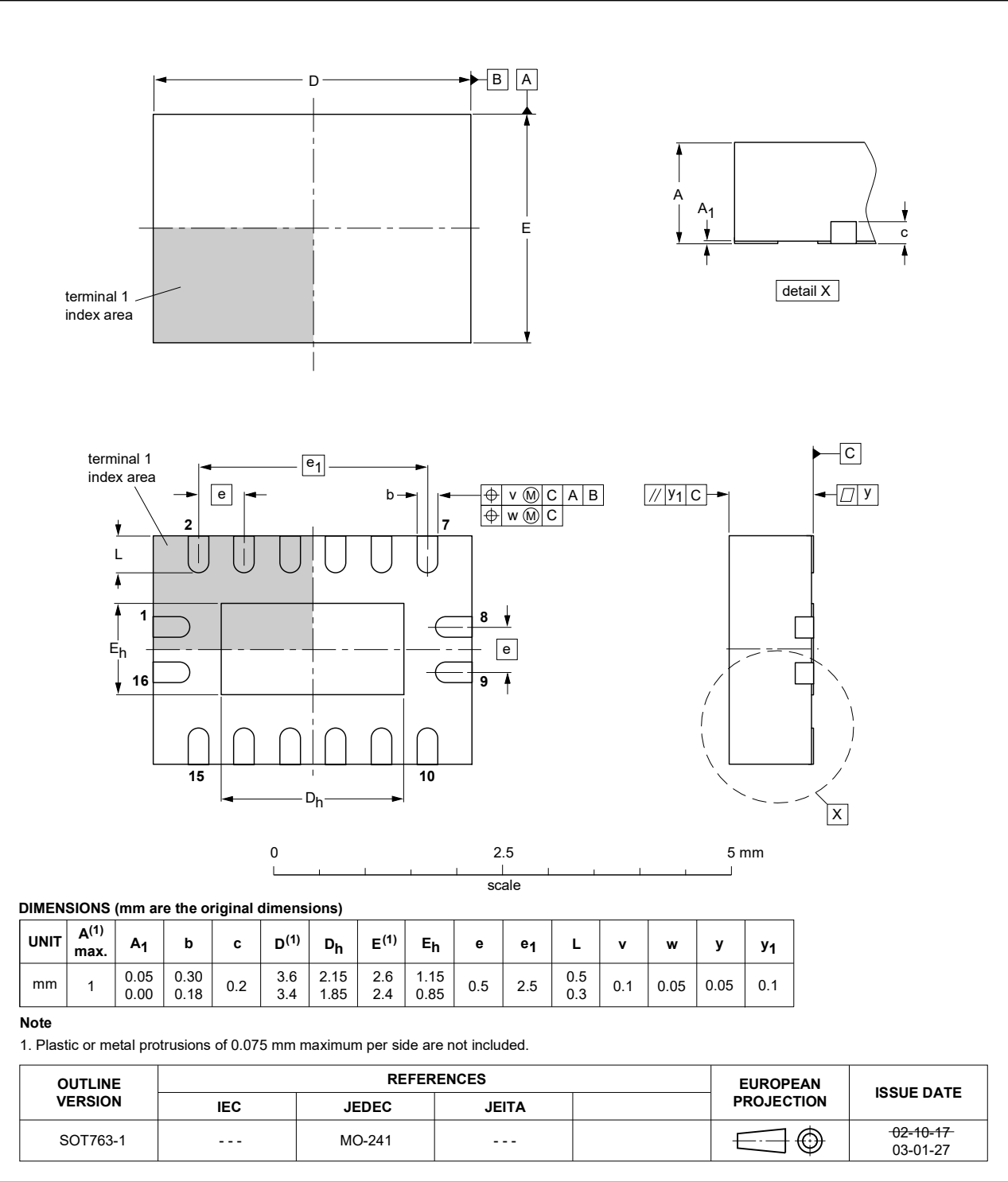


Fig. 14. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4017_Q100 v.3	20240327	Product data sheet	-	74HC_HCT4017_Q100 v.2
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.Fig. 12, Fig. 13: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC_HCT4017_Q100 v.2	20200701	Product data sheet	-	74HC_HCT4017_Q100 v.1
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Section 1 and Section 2 updated.Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT4017_Q100 v.1	20140324	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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