

# SIEMENS

## Microcomputer Components

8-Bit CMOS Single-Chip Microcontroller

### SAB 80C517/80C537

## High-Performance 8-Bit CMOS Single-Chip Microcontroller

**SAB 80C517/80C537**

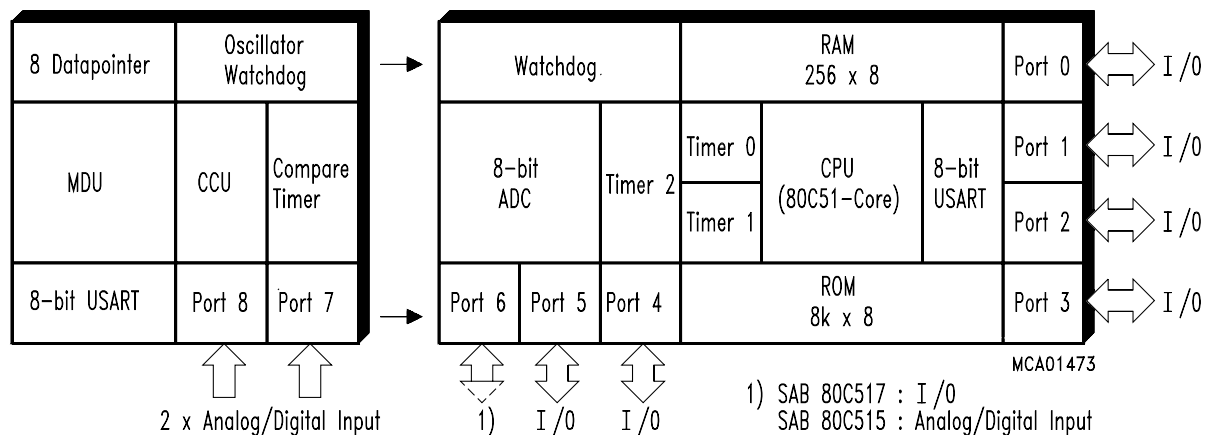
### Advanced Information

SAB 80C517  
SAB 80C537

Microcontroller with factory mask-programmable ROM  
Microcontroller for external ROM

- Versions for 12 MHz and 16 MHz operating frequency
- 8 K × 8 ROM (SAB 80C517 only)
- 256 × 8 on-chip RAM
- Superset of SAB 80C51 architecture:
  - 1 μs instruction cycle time at 12 MHz
  - 750 ns instruction cycle time at 16 MHz
  - 256 directly addressable bits
  - Boolean processor
  - 64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit 2 multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Fourteen interrupt vectors, four priority levels selectable
- 8-bit A/D converter with 12 multiplexed inputs and programmable ref. voltages
- Two full duplex serial interfaces
- Fully upward compatible with SAB 80C515
- Extended power saving modes
- Nine ports: 56 I/O lines, 12 input lines
- Two temperature ranges available:
  - 0 to 70 °C
  - 40 to 85 °C
- Plastic packages: P-LCC-84, P-MQFP-100-2

### SAB 80C517/80C537

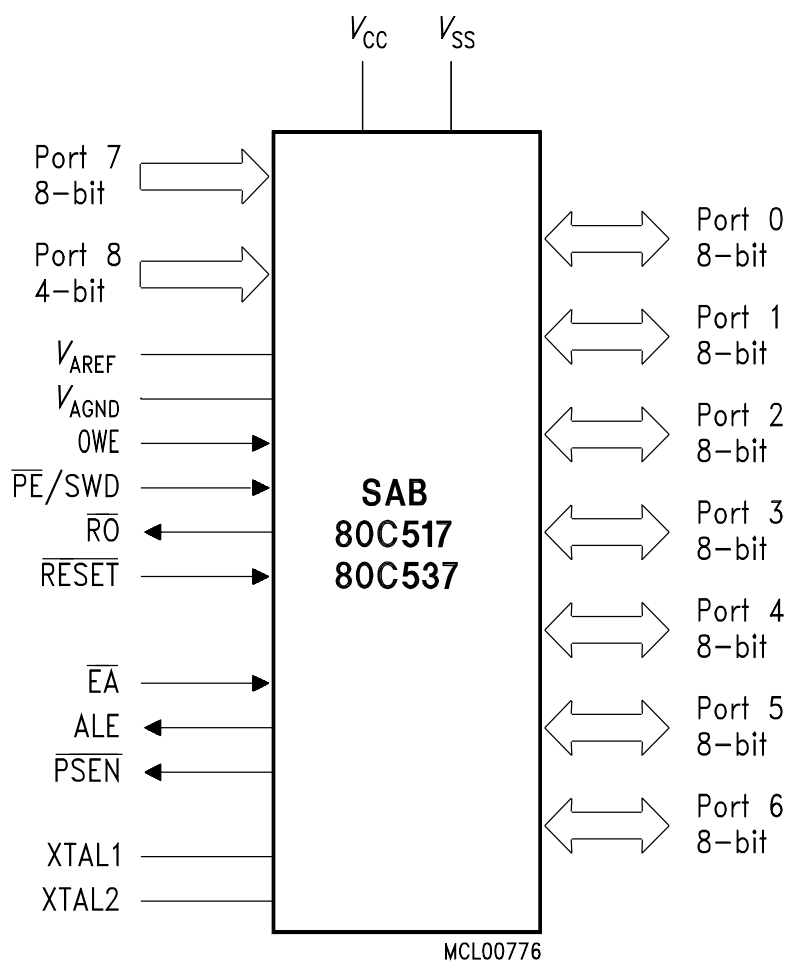


The SAB 80C517/80C537 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

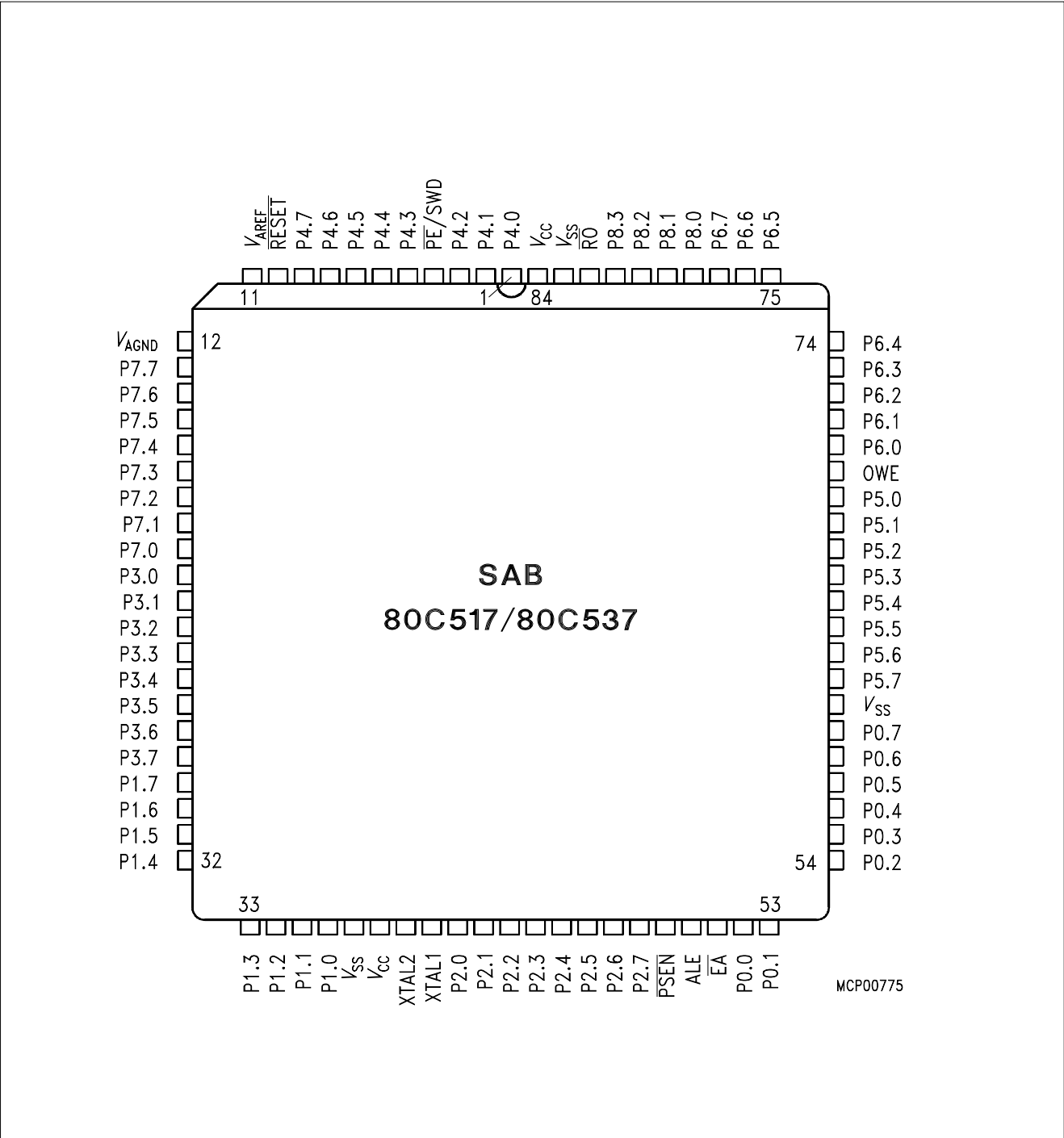
While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C517 is expanded in its arithmetic capabilities, "fail-safe" characteristics, analog signal processing and timer capabilities. The SAB 80C537 is identical with the SAB 80C517 except that it lacks the on-chip program memory. The SAB 80C517/SAB 80C537 is supplied in a 84 pin plastic leaded chip carrier package (P-LCC-84) and in a 100-pin plastic quad metric flat package (P-MQFP-100-2).

## Ordering Information

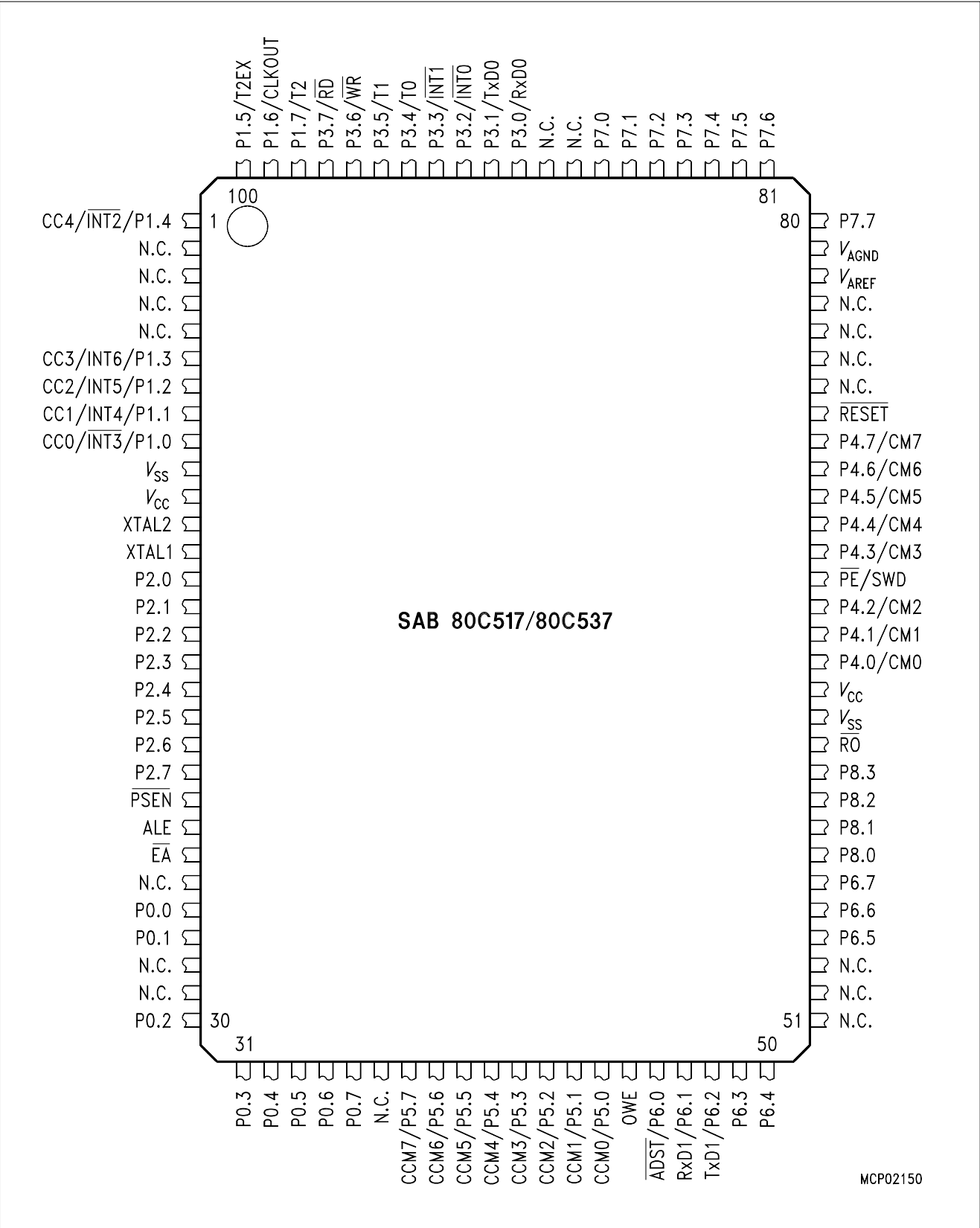
| Type                   | Ordering Code | Package      | Description<br>8-bit CMOS Microcontroller                                  |
|------------------------|---------------|--------------|----------------------------------------------------------------------------|
| SAB 80C517-N           | Q67120-C397   | P-LCC-84     | with factory mask-programmable ROM, 12 MHz                                 |
| SAB 80C517-M           | TBD           | P-MQFP-100-2 |                                                                            |
| SAB 80C537-N           | Q67120-C452   | P-LCC-84     | for external memory, 12 MHz                                                |
| SAB 80C537-M           | TBD           | P-MQFP-100-2 |                                                                            |
| SAB 80C517-N-T40/85    | Q67120-C483   | P-LCC-84     | with factory mask-programmable ROM, 12 MHz, ext. temperature – 40 to 85 °C |
| SAB 80C517-M-T40/85    | TBD           | P-MQFP-100-2 |                                                                            |
| SAB 80C537-N-T40/85    | Q67120-C484   | P-LCC-84     | for external ROM, 12 MHz, ext. temperature – 40 to 85 °C                   |
| SAB 80C537-M-T40/85    | TBD           | P-MQFP-100-2 |                                                                            |
| SAB 80C517-N16         | Q67120-C723   | P-LCC-84     | with mask-programmable ROM, 16 MHz ext. temperature – 40 to 110 °C         |
| SAB 80C517-M16         | TBD           | P-MQFP-100-2 |                                                                            |
| SAB 80C537-N16         | Q67120-C722   | P-LCC-84     | for external memory, 16 MHz                                                |
| SAB 80C537-M16         | TBD           | P-MQFP-100-2 |                                                                            |
| SAB 80C517-N16-T40/85  | Q67120-C724   | P-LCC-84     | with mask-programmable ROM, 16 MHz<br>ext. temperature – 40 to 85 °C       |
| SAB 80C517-16-N-T40/85 | Q67120-C725   | P-LCC-84     | with factory mask-programmable ROM, 12 MHz                                 |



## Logic Symbol



Pin Configuration  
(P-LCC-84)



Pin Configuration  
(P-MQFP-100-2)

## Pin Definitions and Functions

| Symbol              | Pin Number  |                     | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|-------------|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                     | P-LCC-84    | P-MQFP-100-2        |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| P4.0 – P4.7         | 1– 3, 5 – 9 | 64 - 66,<br>68 - 72 | I/O    | <p><b>Port 4</b></p> <p>is a bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors.</p> <p>This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows:</p> <ul style="list-style-type: none"> <li>– CM0 (P4.0): Compare Channel 0</li> <li>– CM1 (P4.1): Compare Channel 1</li> <li>– CM2 (P4.2): Compare Channel 2</li> <li>– CM3 (P4.3): Compare Channel 3</li> <li>– CM4 (P4.4): Compare Channel 4</li> <li>– CM5 (P4.5): Compare Channel 5</li> <li>– CM6 (P4.6): Compare Channel 6</li> <li>– CM7 (P4.7): Compare Channel 7</li> </ul> |
| $\overline{PE}/SWD$ | 4           | 67                  | I      | <p><b>Power saving modes enable/<br/>Start Watchdog Timer</b></p> <p>A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default.</p> <p>Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.</p>                                                                                                                                                                                                                                                                                                                                            |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol                    | Pin Number |              | I/O *) | Function                                                                                                                                                                                                                                                      |
|---------------------------|------------|--------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | P-LCC-84   | P-MQFP-100-2 |        |                                                                                                                                                                                                                                                               |
| $\overline{\text{RESET}}$ | 10         | 73           | I      | $\overline{\text{RESET}}$<br>A low level on this pin for the duration of one machine cycle while the oscillator is running resets the SAB 80C517. A small internal pull-up resistor permits power-on reset using only a capacitor connected to $V_{SS}$ .     |
| $V_{\text{AREF}}$         | 11         | 78           |        | <b>Reference voltage</b> for the A/D converter.                                                                                                                                                                                                               |
| $V_{\text{AGND}}$         | 12         | 79           |        | <b>Reference ground</b> for the A/D converter.                                                                                                                                                                                                                |
| P7.7 -P7.0                | 13 - 20    | 80 - 87      | I      | <b>Port 7</b><br>is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously. |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol      | Pin Number |              | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------|------------|--------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | P-LCC-84   | P-MQFP-100-2 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| P3.0 - P3.7 | 21 - 28    | 90 - 97      | I/O    | <p><b>Port 3</b> is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:</p> <ul style="list-style-type: none"> <li>– <math>R \times D0</math> (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface</li> <li>– <math>T \times D0</math> (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0</li> <li>– <math>\overline{INT0}</math> (P3.2): interrupt 0 input/timer 0 gate control</li> <li>– <math>\overline{INT1}</math> (P3.3): interrupt 1 input/timer 1 gate control</li> <li>– T0 (P3.4): counter 0 input</li> <li>– T1 (P3.5): counter 1 input</li> <li>– <math>\overline{WR}</math> (P3.6): the write control signal latches the data byte from port 0 into the external data memory</li> <li>– <math>\overline{RD}</math> (P3.7): the read control signal enables the external data memory to port 0</li> </ul> |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol      | Pin Number |                       | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------|------------|-----------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | P-LCC-84   | P-MQFP-100-2          |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| P1.7 - P1.0 | 29 - 36    | 98 - 100,<br>1, 6 - 9 | I/O    | <p><b>Port 1</b><br/>is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. It is used for the low order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows:</p> <ul style="list-style-type: none"> <li>– <math>\overline{INT3}/CC0</math> (P1.0): interrupt 3 input / compare 0 output / capture 0 input</li> <li>– <math>\overline{INT4}/CC1</math> (P1.1): interrupt 4 input / compare 1 output / capture 1 input</li> <li>– <math>\overline{INT5}/CC2</math> (P1.2): interrupt 5 input / compare 2 output / capture 2 input</li> <li>– <math>\overline{INT6}/CC3</math> (P1.3): interrupt 6 input / compare 3 output / capture 3 input</li> <li>– <math>\overline{INT2}/CC4</math> (P1.4): interrupt 2 input / compare 4 output / capture 4 input</li> <li>– T2EX (P1.5): timer 2 external reload trigger input</li> <li>– CLKOUT (P1.6): system clock output</li> <li>– T2 (P1.7): counter 2 input</li> </ul> |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol      | Pin Number |              | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------|------------|--------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | P-LCC-84   | P-MQFP-100-2 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| XTAL2       | 39         | 12           | —      | <b>XTAL2</b><br>Input to the inverting oscillator amplifier and input to the internal clock generator circuits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| XTAL1       | 40         | 13           | —      | <b>XTAL1</b><br>Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.                                                                                                                                                                                                                                                                                                         |
| P2.0 - P2.7 | 41 - 48    | 14 - 21      | I/O    | <b>Port 2</b><br>is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as in-puts. As inputs, port 2 pins being externally pulled low will source current ( $I_{IL}$ , in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register. |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol                   | Pin Number |                     | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------|------------|---------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                          | P-LCC-84   | P-MQFP-100-2        |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{\text{PSEN}}$ | 49         | 22                  | O      | The <b>Program Store Enable</b> output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.                                                                                                                                                                                                                                        |
| ALE                      | 50         | 23                  | O      | The <b>Address Latch Enable</b> output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access                                                                                                                                                                                                                                                                                                                   |
| $\overline{\text{EA}}$   | 51         | 24                  | I      | <b>External Access Enable</b><br>When held at high level, instructions are fetched from the internal ROM when the PC is less than 8192. When held at low level, the SAB 80C517 fetches all instructions from external program memory. For the SAB 80C537 this pin must be tied low                                                                                                                                                                                                                                                |
| P0.0 - P0.7              | 52 - 59    | 26 - 27,<br>30 - 35 | I/O    | <b>Port 0</b><br>is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1 s. Port 0 also outputs the code bytes during program verification in the SAB 83C517. External pull-up resistors are required during program verification. |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol      | Pin Number |              | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------|------------|--------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | P-LCC-84   | P-MQFP-100-2 |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| P5.7 - P5.0 | 61 - 68    | 37 - 44      | I/O    | <p><b>Port 5</b></p> <p>is a bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare". The secondary functions are assigned to the port 5 pins as follows:</p> <ul style="list-style-type: none"> <li>– CCM0 (P5.0): concurrent compare 0</li> <li>– CCM1 (P5.1): concurrent compare 1</li> <li>– CCM2 (P5.2): concurrent compare 2</li> <li>– CCM3 (P5.3): concurrent compare 3</li> <li>– CCM4(P5.4): concurrent compare 4</li> <li>– CCM5 (P5.5): concurrent compare 5</li> <li>– CCM6 (P5.6): concurrent compare 6</li> <li>– CCM7(P5.7): concurrent compare 7</li> </ul> |
| OWE         | 69         | 45           | I      | <p><b>Oscillator Watchdog Enable</b></p> <p>A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resistor. When held at low level the oscillator watchdog function is off.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

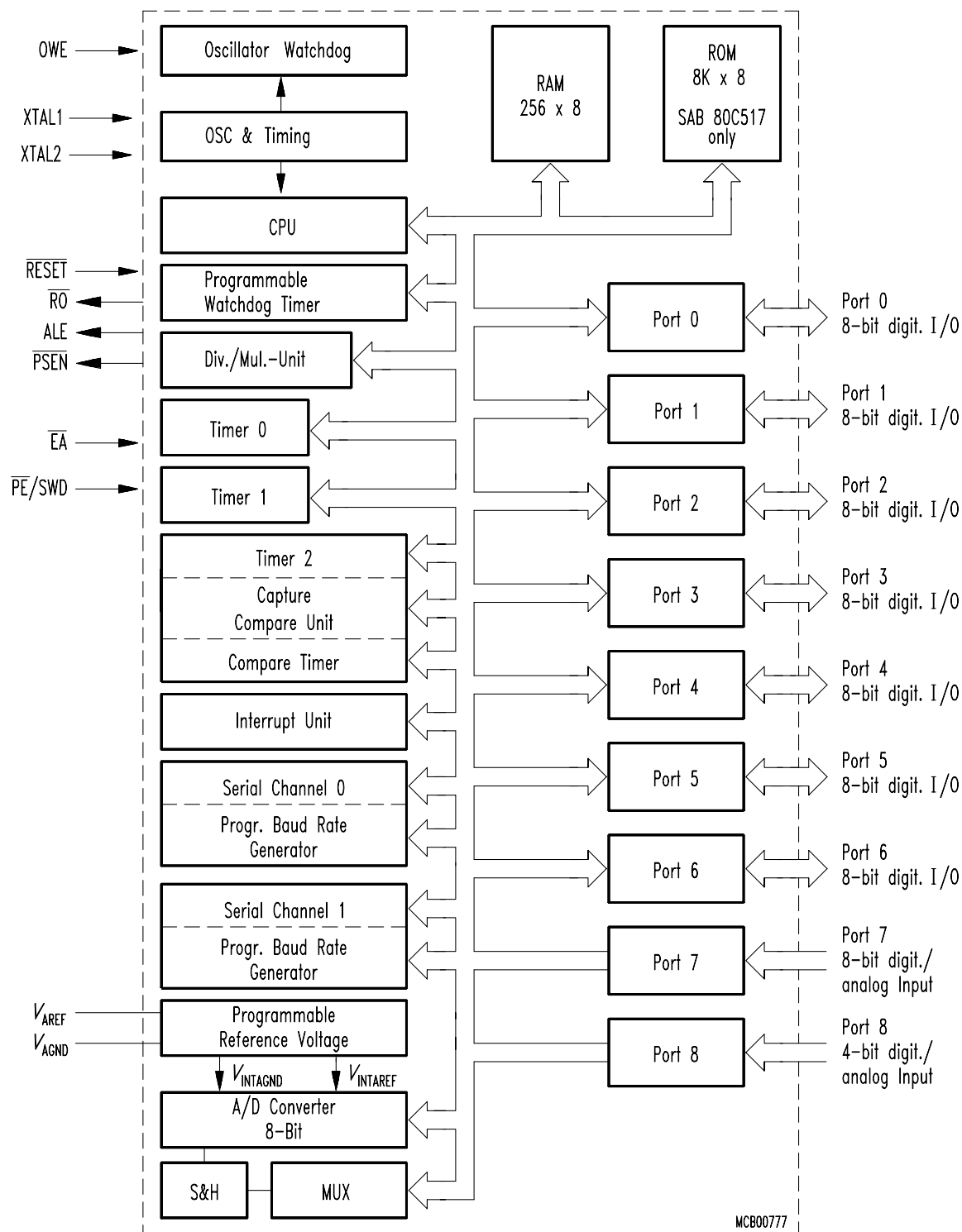
| Symbol      | Pin Number |                     | I/O *) | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------|------------|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | P-LCC-84   | P-MQFP-100-2        |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| P6.0 - P6.7 | 70 - 77    | 46 - 50,<br>54 - 56 | I/O    | <p><b>Port 6</b><br/>is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (<math>I_{IL}</math>, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows:</p> <ul style="list-style-type: none"> <li>– <math>\overline{ADST}</math> (P6.0): external A/D converter start pin</li> <li>– <math>R \times D1</math> (P6.1): receiver data input of serial interface 1</li> <li>– <math>T \times D1</math> (P6.2): transmitter data output of serial interface 1</li> </ul> |
| P8.0 - P8.3 | 78 - 81    | 57 - 60             | I      | <p><b>Port 8</b><br/>is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

\* I = Input  
O = Output

## Pin Definitions and Functions (cont'd)

| Symbol          | Pin Number |                                                                  | I/O *) | Function                                                                                                                                                                                                                                       |
|-----------------|------------|------------------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 | P-LCC-84   | P-MQFP-100-2                                                     |        |                                                                                                                                                                                                                                                |
| $\overline{RO}$ | 82         | 61                                                               | O      | <b>Reset Output</b><br>This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watch-dog reset. The reset output is active low. |
| $V_{SS}$        | 37, 60, 83 | 10, 62                                                           | —      | <b>Circuit ground potential</b>                                                                                                                                                                                                                |
| $V_{CC}$        | 38, 84     | 11, 63                                                           | —      | <b>Supply Terminal</b> for all operating modes                                                                                                                                                                                                 |
| N.C.            | —          | 2 - 5, 25,<br>28 - 29,<br>36,<br>51 - 53,<br>74 - 77;<br>88 - 89 | —      | Not connected                                                                                                                                                                                                                                  |

\* I = Input  
O = Output



**Figure 1**  
**Block Diagram**

## Functional Description

The SAB 80C517 is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being a significantly enhanced SAB 80C515. The SAB 80C517 is therefore 100 % compatible with code written for the SAB 80C515.

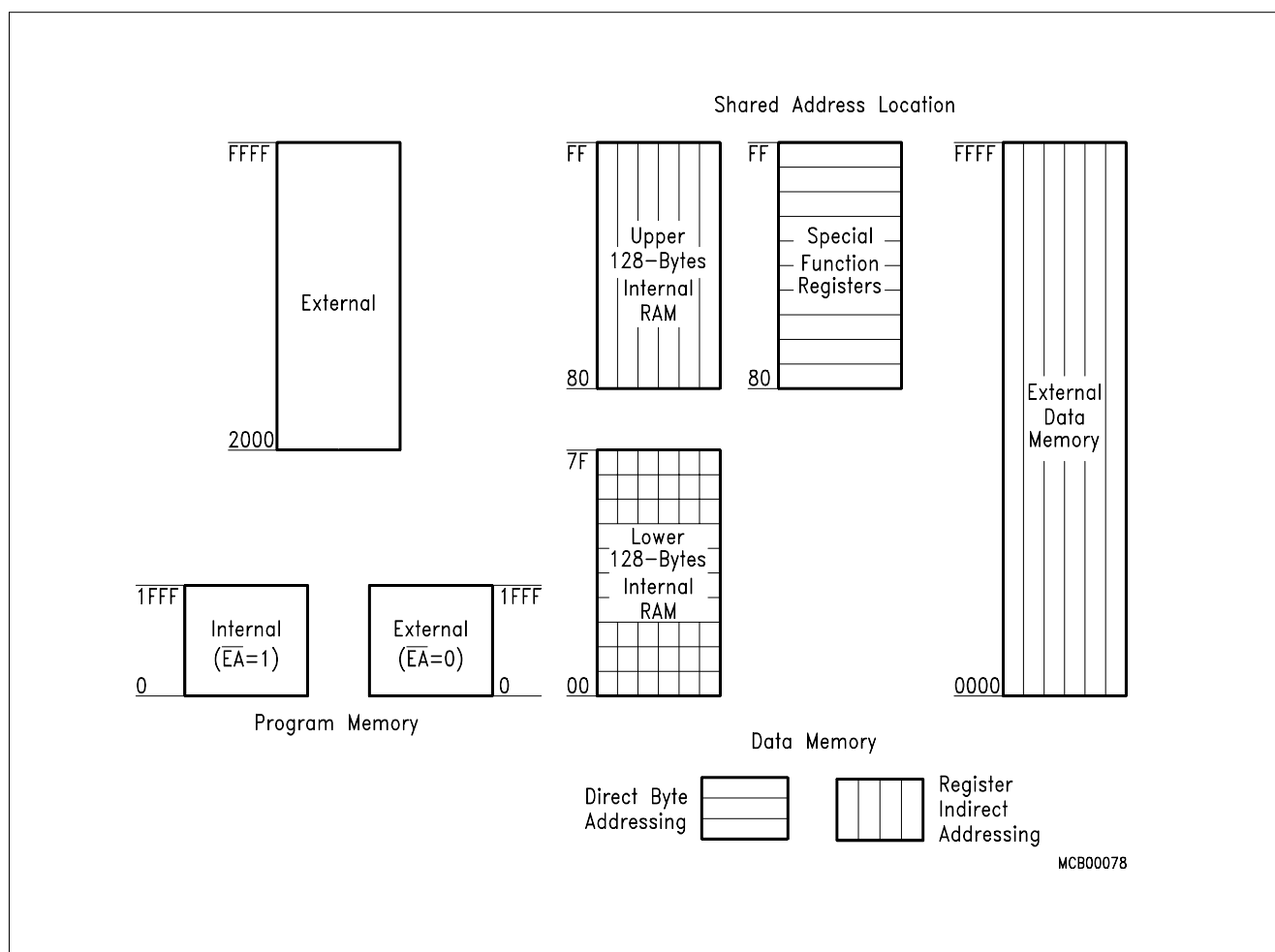
## CPU

Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517 is optimized for control applications. With a 12 MHz crystal, 58% of the instructions execute in 1  $\mu$ s.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

## Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517 has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.



**Figure 2**  
**Memory Mapping**

### **Program Memory**

The SAB 80C517 has 8 KByte of on-chip ROM, while the SAB 80C537 has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin  $\overline{EA}$  controls whether program fetches below address 2000<sub>H</sub> are done from internal or external memory.

### **Data Memory**

The data memory space consists of an internal and an external memory space.

### **External Data Memory**

Up to 64 KByte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions utilizing registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers.

### **Multiple Datapointers**

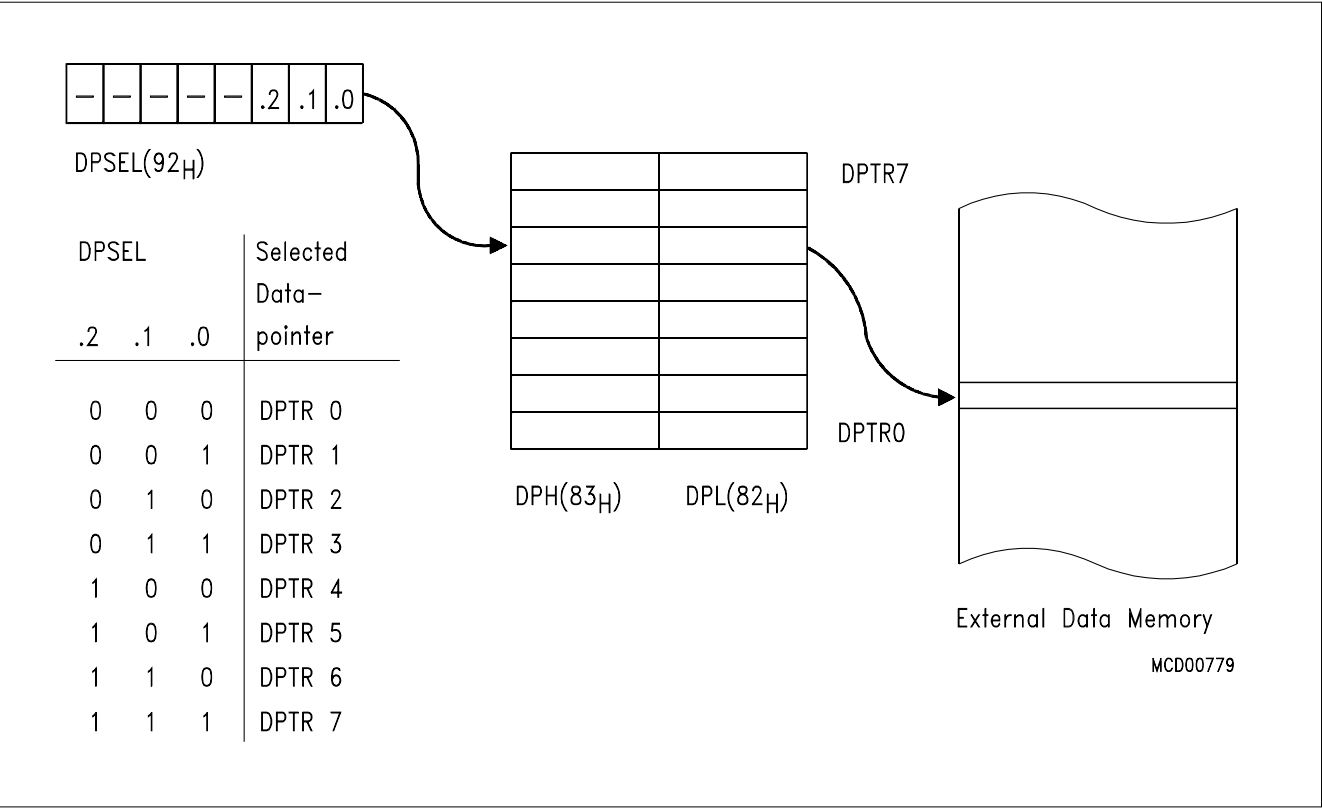
As a functional enhancement to standard 8051 controllers, the SAB 80C517 contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointers is done in special function register DPSEL (data pointer select, addr. 92<sub>H</sub>). **Figure 3** illustrates the addressing mechanism.

### **Internal Data Memory**

The internal data memory is divided into three physically distinct blocks:

- the lower 128 bytes of RAM including four banks of eight registers each
- the upper 128 byte of RAM
- the 128 byte special function register area.

A mapping of the internal data memory is also shown in **figure 2**. The overlapping address spaces are accessed by different addressing modes. The stack can be located anywhere in the internal data memory.



**Figure 3**  
**Addressing of External Data Memory**

## Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in **table 1**. In this table they are organized in groups which refer to the functional blocks of the SAB 80C517. Block names and symbols are listed in alphabetical order.

**Table 1**  
**Special Function Register**

| Address             | Register                   | Name                                      | Register                             | Contents after Reset                 |
|---------------------|----------------------------|-------------------------------------------|--------------------------------------|--------------------------------------|
| CPU                 | <b>ACC</b>                 | <b>Accumulator</b>                        | <b>0E0<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | <b>B</b>                   | <b>B-Register</b>                         | <b>0F0<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | DPH                        | Data Pointer, High Byte                   | 83 <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | DPL                        | Data Pointer, Low Byte                    | 82 <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | DPSEL                      | Data Pointer Select Register              | 92 <sub>H</sub>                      | XXXX.X000 <sub>B</sub> <sup>3)</sup> |
|                     | <b>PSW</b>                 | <b>Program Status Word Register</b>       | <b>0D0<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
| A/D-<br>Converter   | SP                         | Stack Pointer                             | 81 <sub>H</sub>                      | 07 <sub>H</sub>                      |
|                     | <b>ADCON0</b>              | <b>A/D Converter Control Register 0</b>   | <b>0D8<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | ADCON1                     | A/D Converter Control Register 1          | 0DC <sub>H</sub>                     | XXXX.0000 <sub>B</sub> <sup>3)</sup> |
|                     | ADDAT                      | A/D Converter Data Register               | 0D9 <sub>H</sub>                     | 00 <sub>H</sub>                      |
| Interrupt<br>System | DAPR                       | D/AConverter Program Register             | 0DA <sub>H</sub>                     | 00 <sub>H</sub>                      |
|                     | <b>IEN0</b>                | <b>Interrupt Enable Register 0</b>        | <b>0A8<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | CTCON <sup>2)</sup>        | Com. Timer Control Register               | 0E1 <sub>H</sub>                     | 0XXX.0000 <sub>B</sub>               |
|                     | <b>IEN1</b>                | <b>Interrupt Enable Register 1</b>        | <b>0B8<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | IEN2                       | Interrupt Enable Register 2               | 9A <sub>H</sub>                      | XXXX.00X0 <sub>B</sub> <sup>3)</sup> |
|                     | IP0                        | Interrupt Priority Register 0             | 0A9 <sub>H</sub>                     | 00 <sub>H</sub>                      |
|                     | IP1                        | Interrupt Priority Register 1             | 0B9 <sub>H</sub>                     | XX00 0000 <sub>B</sub>               |
|                     | <b>IRCON</b>               | <b>Interrupt Request Control Register</b> | <b>0C0<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | <b>TCON</b> <sup>2)</sup>  | <b>Timer Control Register</b>             | <b>88<sub>H</sub></b> <sup>1)</sup>  | <b>00<sub>H</sub></b>                |
|                     | <b>T2CON</b> <sup>2)</sup> | <b>Timer 2 Control Register</b>           | <b>0C8<sub>H</sub></b>               | <b>00<sub>H</sub></b>                |

<sup>1)</sup> Bit-addressable special function registers

<sup>2)</sup> This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

<sup>3)</sup> X means that the value is indeterminate and the location is reserved

**Table 1**  
**Special Function Register (cont'd)**

| Address      | Register | Name                               | Register         | Contents after Reset                 |
|--------------|----------|------------------------------------|------------------|--------------------------------------|
| MUL/DIV Unit | ARCON    | Arithmetic Control Register        | 0EF <sub>H</sub> | 0XXX.XXXX <sub>B</sub> <sup>3)</sup> |
|              | MD0      | Multiplication/Division Register 0 | 0E9 <sub>H</sub> | XX <sub>H</sub> <sup>3)</sup>        |
|              | MD1      | Multiplication/Division Register 1 | 0EA <sub>H</sub> | XX <sub>H</sub> <sup>3)</sup>        |
|              | MD2      | Multiplication/Division Register 2 | 0EB <sub>H</sub> | XX <sub>H</sub> <sup>3)</sup>        |
|              | MD3      | Multiplication/Division Register 3 | 0EC <sub>H</sub> | XX <sub>H</sub> <sup>3)</sup>        |
|              | MD4      | Multiplication/Division Register 4 | 0ED <sub>H</sub> | XX <sub>H</sub> <sup>3)</sup>        |
|              | MD5      | Multiplication/Division Register 5 | 0EE <sub>H</sub> | XX <sub>H</sub> <sup>3)</sup>        |

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

**Table 1**  
**Special Function Register (cont'd)**

| Address                            | Register     | Name                            | Register                            | Contents after Reset                 |
|------------------------------------|--------------|---------------------------------|-------------------------------------|--------------------------------------|
| Compare/<br>Capture-<br>Unit (CCU) | CCEN         | Comp./Capture Enable Reg.       | 0C1 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CC4EN        | Comp./Capture Enable 4 Reg.     | 0C9 <sub>H</sub>                    | X000.0000 <sub>B</sub> <sup>3)</sup> |
|                                    | CCH1         | Comp./Capture Reg. 1, High Byte | 0C3 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCH2         | Comp./Capture Reg. 2, High Byte | 0C5 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCH3         | Comp./Capture Reg. 3, High Byte | 0C7 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCH4         | Comp./Capture Reg. 4, High Byte | 0CF <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCL1         | Comp./Capture Reg. 1, Low Byte  | 0C2 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCL2         | Comp./Capture Reg. 2, Low Byte  | 0C4 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCL3         | Comp./Capture Reg. 3, Low Byte  | 0C6 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CCL4         | Comp./Capture Reg. 4, Low Byte  | 0CE <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMEN         | Compare Enable Register         | 0F6 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH0         | Compare Register 0, High Byte   | 0D3 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH1         | Compare Register 1, High Byte   | 0D5 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH2         | Compare Register 2, High Byte   | 0D7 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH3         | Compare Register 3, High Byte   | 0E3 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH4         | Compare Register 4, High Byte   | 0E5 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH5         | Compare Register 5, High Byte   | 0E7 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH6         | Compare Register 6, High Byte   | 0F3 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMH7         | Compare Register 7, High Byte   | 0F5 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML0         | Compare Register 0, Low Byte    | 0D2 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML1         | Compare Register 1, Low Byte    | 0D4 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML2         | Compare Register 2, Low Byte    | 0D6 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML3         | Compare Register 3, Low Byte    | 0E2 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML4         | Compare Register 4, Low Byte    | 0E4 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML5         | Compare Register 5, Low Byte    | 0E6 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML6         | Compare Register 6, Low Byte    | 0F2 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CML7         | Compare Register 7, Low Byte    | 0F4 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CMSEL        | Compare Input Select            | 0F7 <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CRCH         | Com./Rel./Capt. Reg. High Byte  | 0CB <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CRCL         | Com./Rel./Capt. Reg. Low Byte   | 0CA <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CTCON        | Com. Timer Control Reg.         | 0E1 <sub>H</sub>                    | 0XXX.0000 <sub>B</sub> <sup>3)</sup> |
|                                    | CTRELH       | Com. Timer Rel. Reg., High Byte | 0DF <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | CTRELL       | Com. Timer Rel. Reg., Low Byte  | 0DE <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | TH2          | Timer 2, High Byte              | 0CD <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | TL2          | Timer 2, Low Byte               | 0CC <sub>H</sub>                    | 00 <sub>H</sub>                      |
|                                    | <b>T2CON</b> | <b>Timer 2 Control Register</b> | <b>0C8<sub>H</sub><sup>1)</sup></b> | <b>00<sub>H</sub></b>                |

<sup>1)</sup> Bit-addressable special function registers

<sup>2)</sup> This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

<sup>3)</sup> X means that the value is indeterminate and the location is reserved

**Table 1**  
**Special Function Register (cont'd)**

| Address             | Register                    | Name                                     | Register                             | Contents after Reset                 |
|---------------------|-----------------------------|------------------------------------------|--------------------------------------|--------------------------------------|
| Ports               | <b>P0</b>                   | <b>Port 0</b>                            | <b>80<sub>H</sub></b> <sup>1)</sup>  | <b>FF<sub>H</sub></b>                |
|                     | <b>P1</b>                   | <b>Port 1</b>                            | <b>90<sub>H</sub></b> <sup>1)</sup>  | <b>FF<sub>H</sub></b>                |
|                     | <b>P2</b>                   | <b>Port 2</b>                            | <b>0A0<sub>H</sub></b> <sup>1)</sup> | <b>FF<sub>H</sub></b>                |
|                     | <b>P3</b>                   | <b>Port 3</b>                            | <b>0B0<sub>H</sub></b> <sup>1)</sup> | <b>FF<sub>H</sub></b>                |
|                     | <b>P4</b>                   | <b>Port 4</b>                            | <b>0E8<sub>H</sub></b> <sup>1)</sup> | <b>FF<sub>H</sub></b>                |
|                     | <b>P5</b>                   | <b>Port 5</b>                            | <b>0F8<sub>H</sub></b> <sup>1)</sup> | <b>FF<sub>H</sub></b>                |
|                     | P6                          | Port 6,                                  | 0FA <sub>H</sub>                     | FF <sub>H</sub>                      |
|                     | P7                          | Port 7, Analog/Digital Input             | 0DB <sub>H</sub>                     | XX <sub>H</sub> <sup>3)</sup>        |
|                     | P8                          | Port 8, Analog/Digital Input, 4-bit      | 0DD <sub>H</sub>                     | XX <sub>H</sub> <sup>3)</sup>        |
| Pow.Sav. Modes      | PCON                        | Power Control Register                   | 87 <sub>H</sub>                      | 00 <sub>H</sub>                      |
| Serial Channels     | <b>ADCON0</b> <sup>2)</sup> | <b>A/D Converter Control Reg.</b>        | <b>0D8<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | PCON <sup>2)</sup>          | Power Control Register                   | 87 <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | S0BUF                       | Serial Channel 0 Buffer Reg.             | 99 <sub>H</sub>                      | XX <sub>H</sub> <sup>3)</sup>        |
|                     | <b>S0CON</b>                | <b>Serial Channel 0 Control Reg.</b>     | <b>98<sub>H</sub></b> <sup>1)</sup>  | <b>00<sub>H</sub></b>                |
|                     | S0RELL <sup>4)</sup>        | Serial Channel 0, Reload Reg., low byte  | 0AA <sub>H</sub>                     | 0D9 <sub>H</sub>                     |
|                     | S0RELH <sup>4)</sup>        | Serial Channel 0, Reload Reg., high byte | 0BA <sub>H</sub>                     | XXXX.XX11 <sub>B</sub> <sup>3)</sup> |
|                     | S1BUF                       | Serial Channel 1 Buffer Reg.,            | 9C <sub>H</sub>                      | 0XX <sub>H</sub> <sup>3)</sup>       |
|                     | S1CON                       | Serial Channel 1 Control Reg.            | 9B <sub>H</sub>                      | 0X00.000 <sub>B</sub> <sup>3)</sup>  |
|                     | S1REL                       | Serial Channel 1 Reload Reg., low byte   | 9D <sub>H</sub>                      | 00 <sub>H</sub>                      |
| Timer 0/<br>Timer 1 | <b>TCON</b>                 | <b>Timer Control Register</b>            | <b>88<sub>H</sub></b> <sup>1)</sup>  | <b>00<sub>H</sub></b>                |
|                     | TH0                         | Timer 0, High Byte                       | 8C <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | TH1                         | Timer 1, High Byte                       | 8D <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | TL0                         | Timer 0, Low Byte                        | 8A <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | TL1                         | Timer 1, Low Byte                        | 8B <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     | TMOD                        | Timer Mode Register                      | 89 <sub>H</sub>                      | 00 <sub>H</sub>                      |
|                     |                             |                                          |                                      |                                      |
| Watchdog            | <b>IEN0</b> <sup>2)</sup>   | <b>Interrupt Enable Register 0</b>       | <b>0A8<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | <b>IEN1</b> <sup>2)</sup>   | <b>Interrupt Enable Register 1</b>       | <b>0B8<sub>H</sub></b> <sup>1)</sup> | <b>00<sub>H</sub></b>                |
|                     | IP0 <sup>2)</sup>           | Interrupt Priority Register 0            | 0A9 <sub>H</sub>                     | 00 <sub>H</sub>                      |
|                     | IP1 <sup>2)</sup>           | Interrupt Priority Register 1            | 0B9 <sub>H</sub>                     | XX00.0000 <sub>B</sub> <sup>3)</sup> |
|                     | WDTREL                      | Watchdog Timer Reload Reg.               | 86 <sub>H</sub>                      | 00 <sub>H</sub>                      |

<sup>1)</sup> Bit-addressable special function registers.

<sup>2)</sup> This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

<sup>3)</sup> X means that the value is indeterminate and the location is reserved.

<sup>4)</sup> These registers are available in the CA step and later steps.

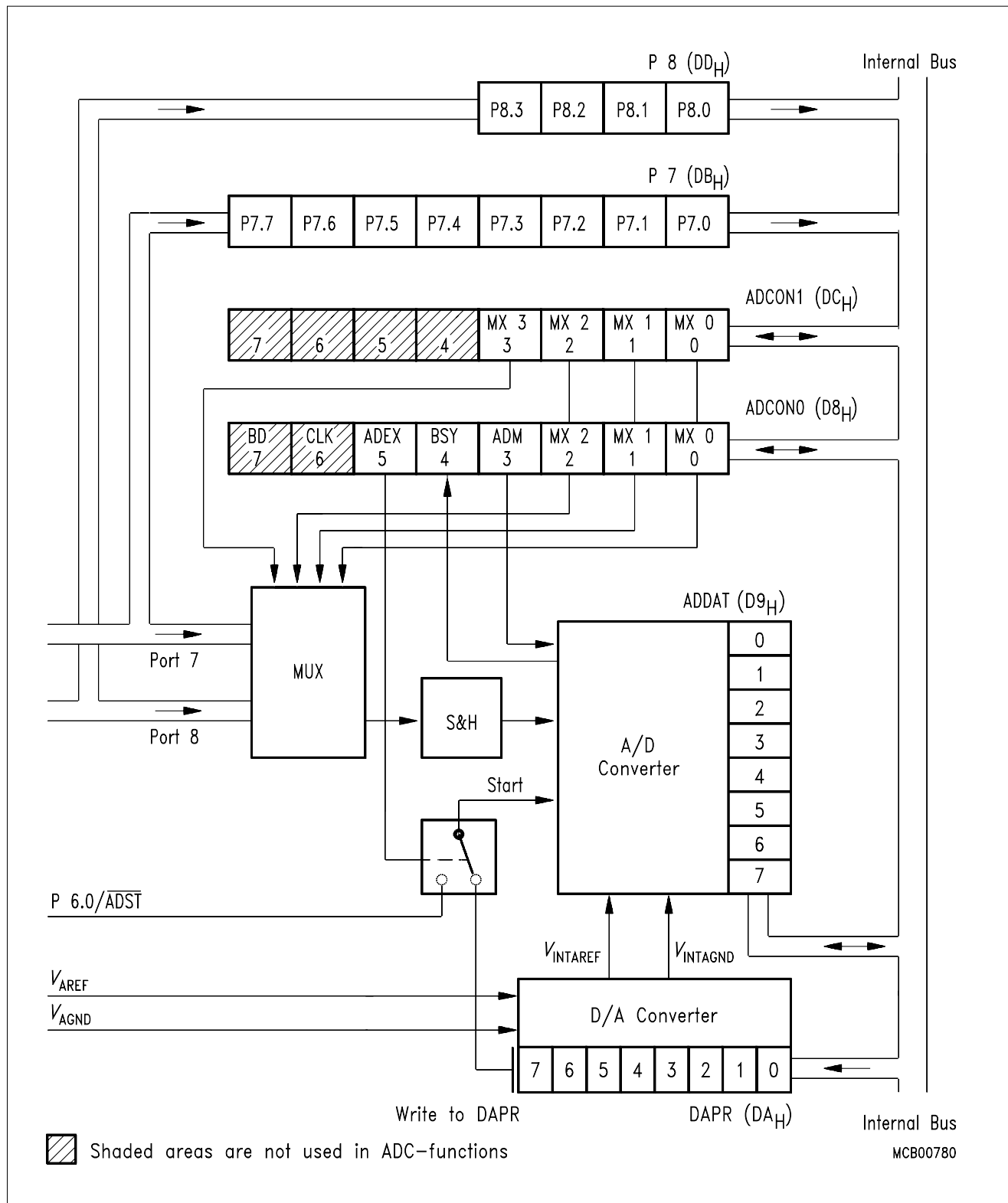
## A/D Converter

The SAB 80C517 contains an 8-bit A/D Converter with 12 multiplexed input channels which uses the successive approximation method. It takes 7 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 13 machine cycles (13  $\mu$ s at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages  $V_{IntAREF}$  and  $V_{IntAGND}$  for the A/D converter are both programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range (see **table 2**).

**Table 2**  
**Adjustable Internal Reference Voltages**

| Step | DAPR (.3-.0)<br>DAPR (.7-.4) | $V_{IntAGND}$ | $V_{IntAREF}$ |
|------|------------------------------|---------------|---------------|
| 0    | 0000                         | 0.0           | 5.0           |
| 1    | 0001                         | 0.3125        | —             |
| 2    | 0010                         | 0.625         | —             |
| 3    | 0011                         | 0.9375        | —             |
| 4    | 0100                         | 1.25          | 1.25          |
| 5    | 0101                         | 1.5625        | 1.5625        |
| 6    | 0110                         | 1.875         | 1.875         |
| 7    | 0111                         | 2.1875        | 2.1875        |
| 8    | 1000                         | 2.5           | 2.5           |
| 9    | 1001                         | 2.8125        | 2.8125        |
| 10   | 1010                         | 3.125         | 3.125         |
| 11   | 1011                         | 3.4375        | 3.4375        |
| 12   | 1100                         | 3.75          | 3.75          |
| 13   | 1101                         | —             | 4.0625        |
| 14   | 1110                         | —             | 4.375         |
| 15   | 1111                         | —             | 4.68754       |



**Figure 4**  
**Block Diagram A/D Converter**

### Compare/Capture Unit (CCU)

The compare capture unit is a complex timer/register array for applications that require high speed I/O, pulse width modulation and more timer/counter capabilities. The CCU contains

- one 16-bit timer/counter (**timer 2**) with 2-bit prescaler, reload capability and a max. clock frequency of  $f_{OSC}/12$  (1 MHz with a 12 MHz crystal).
- one 16-bit timer (**compare timer**) with 8-bit prescaler, reload capability and a max. clock frequency of  $f_{OSC}/2$  (6 MHz with a 12 MHz crystal).
- thirteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- seven interrupts which can be generated by CCU-events.

**Figure 5** shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in **figures 6 and 7**. The four compare/capture registers and the compare/reload/capture register are always connected to timer 2. Dependent on the register type and the assigned timer two compare modes can be selected. **Table 3** illustrates possible combinations and the corresponding output lines.

**Table 3**  
**CCU Configuration**

| Assigned Timer | Compare Register | Compare Output at                   | Possible Modes                        |
|----------------|------------------|-------------------------------------|---------------------------------------|
| Timer 2        | CRCH/CRCL        | P1.0/ $\overline{\text{INT3}}$ /CC0 | Comp. mode 0, 1 + Reload              |
|                | CC1H/CC1L        | P1.0/INT4/CC1                       | Comp. mode 0, 1                       |
|                | CC2H/CC2L        | P1.0/INT5/CC2                       | Comp. mode 0, 1                       |
|                | CC3H/CC3L        | P1.0/INT6/CC3                       | Comp. mode 0, 1                       |
|                | CC4H/CC4L        | P1.0/INT2/CC4                       | Comp. mode 0, 1                       |
|                | CC4H/CC4L        | P5.0/CCM0                           | Comp. mode 1                          |
|                | ⋮                | ⋮                                   | ⋮                                     |
|                | CC4H/CC4L        | P5.7/CCM7                           | Comp. mode 1                          |
|                | CM0H/CM0L        | P4.0/CM0                            | Comp. mode 1                          |
|                | ⋮                | ⋮                                   | ⋮                                     |
|                | CM7H/CM7L        | P4.7/CM7                            | Comp. mode 1                          |
| Compare timer  | CM0H/CM0L        | P4.0/CM0                            | Comp. mode 0<br>(with add. latches)   |
|                | ⋮                | ⋮                                   | ⋮                                     |
|                | CM7H/CM7L        | P4.7/CM7                            | Comp. mode 0<br>(with shadow latches) |



## Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

- Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when the timer overflows.
- Mode 1: The transition of the output signal can be determined by software. A timer overflow signal doesn't affect the compare-output.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. **Figure 8** shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

## Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers into a dedicated capture register.

- Mode 0: Capture is performed in response to a transition at the corresponding port pins CC0 to CC3.
- Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

## Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

- Mode 0: Reload is caused by a timer overflow (auto-reload).
- Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which also can request an interrupt.

## Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

- Mode 0: 8-bit timer/counter with 32:1 prescaler
- Mode 1: 16-bit timer/counter
- Mode 2: 8-bit timer/counter with 8-bit auto reload
- Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs  $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$  can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

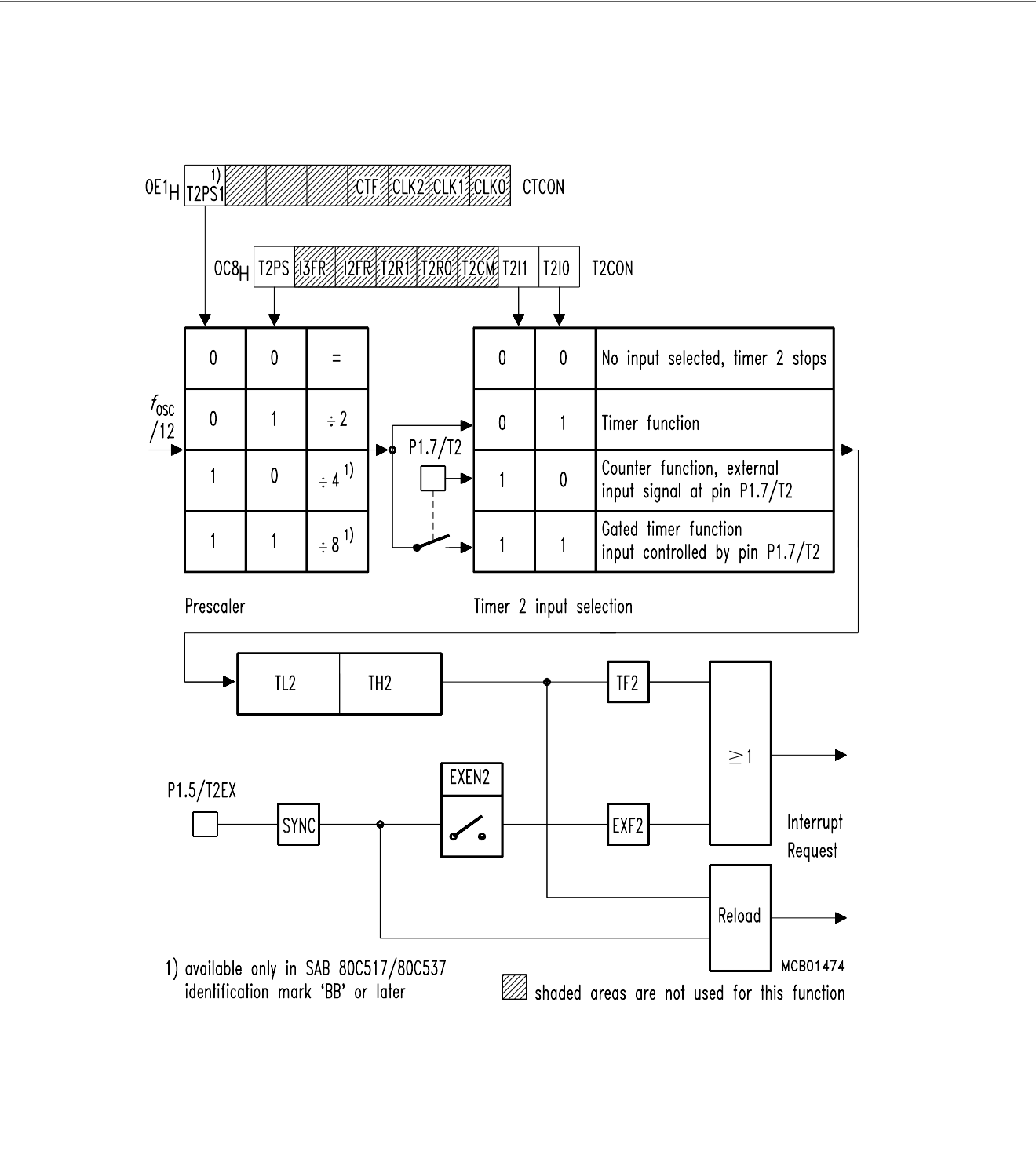
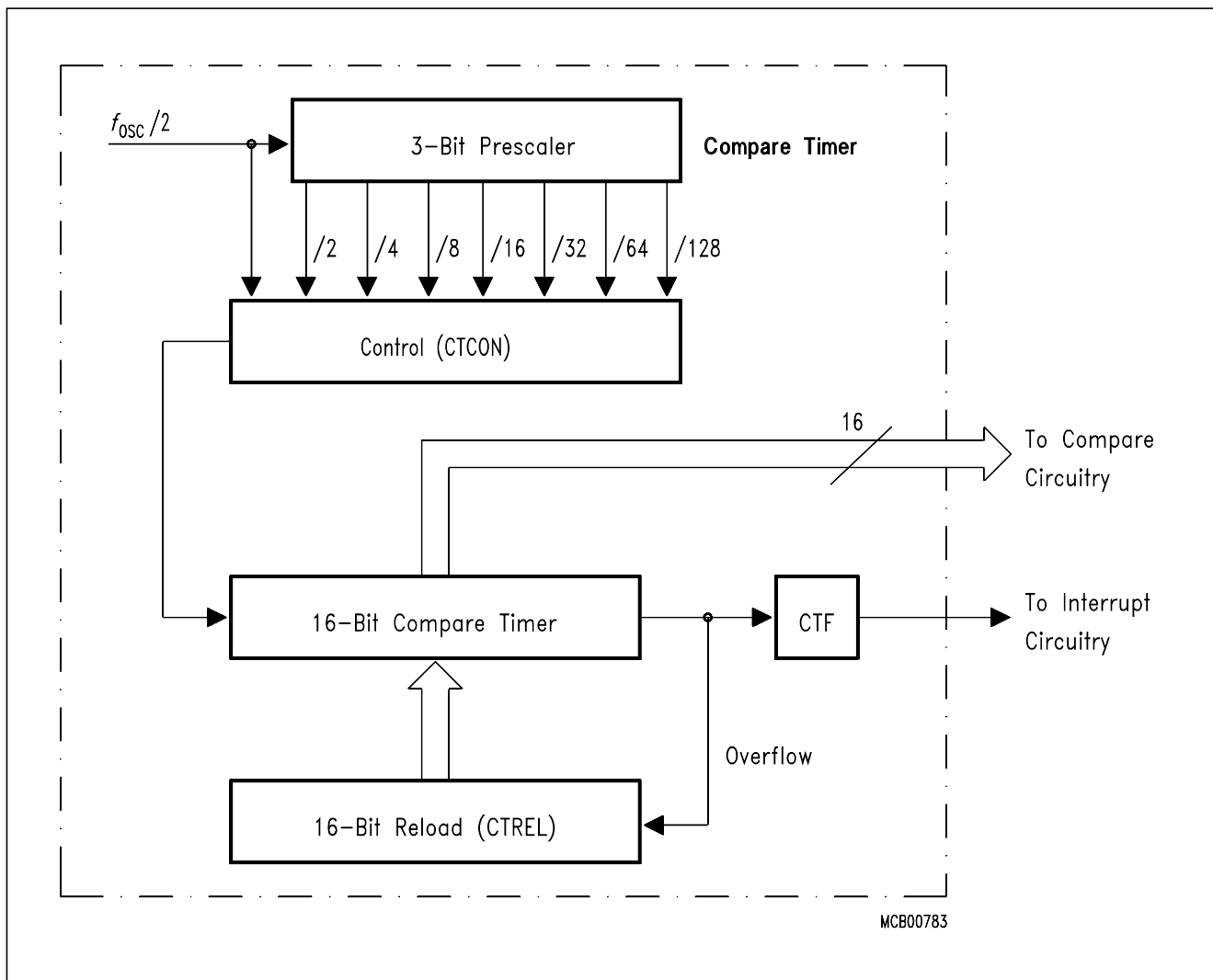
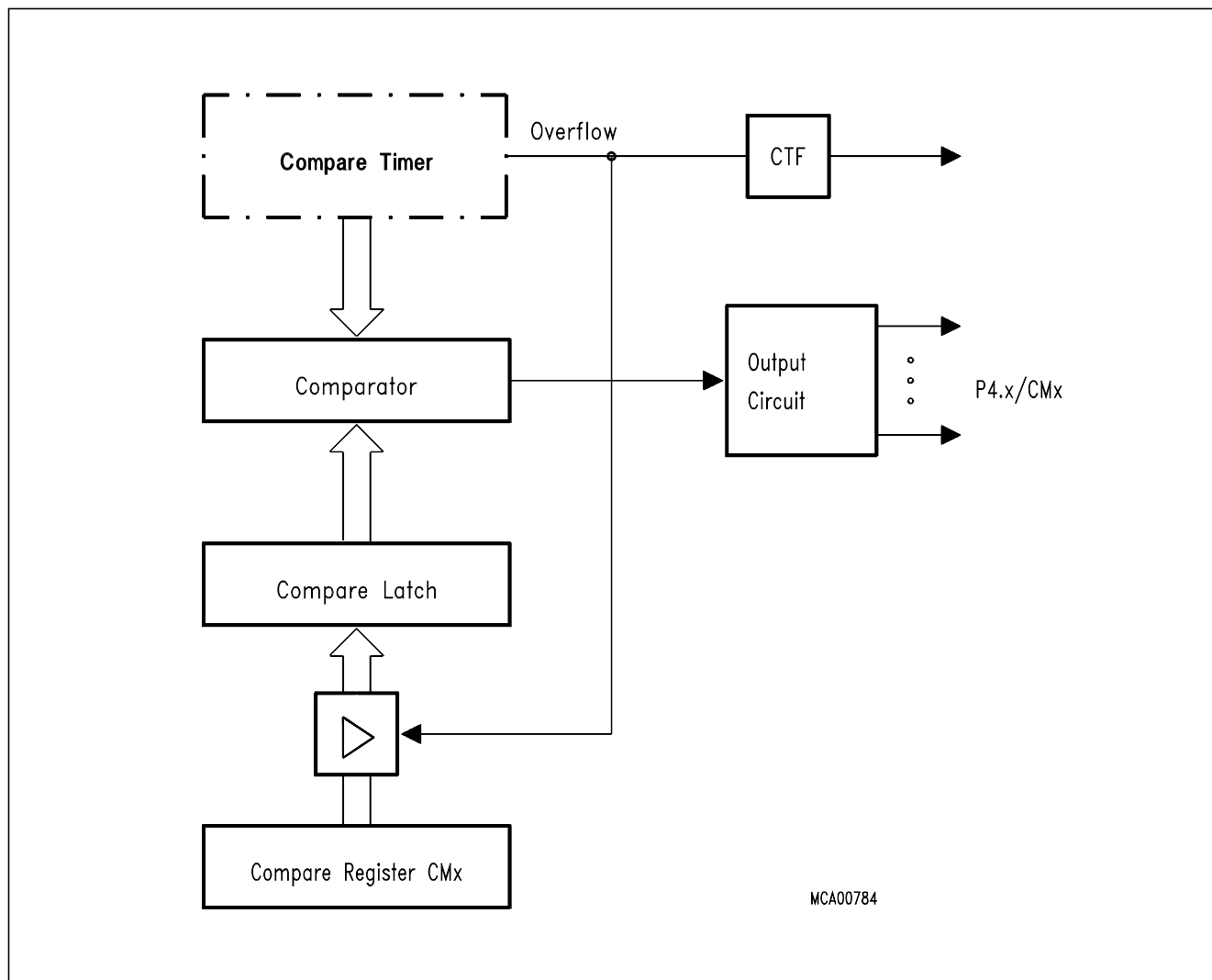


Figure 6  
Block Diagram of Timer 2



**Figure 7**  
**Block Diagram of the Compare Timer**



**Figure 8**  
**Compare-Mode 0 with Registers CM0 to CM7**

## Interrupt Structure

The SAB 80C517 has 14 interrupt vectors with the following vector addresses and request flags.

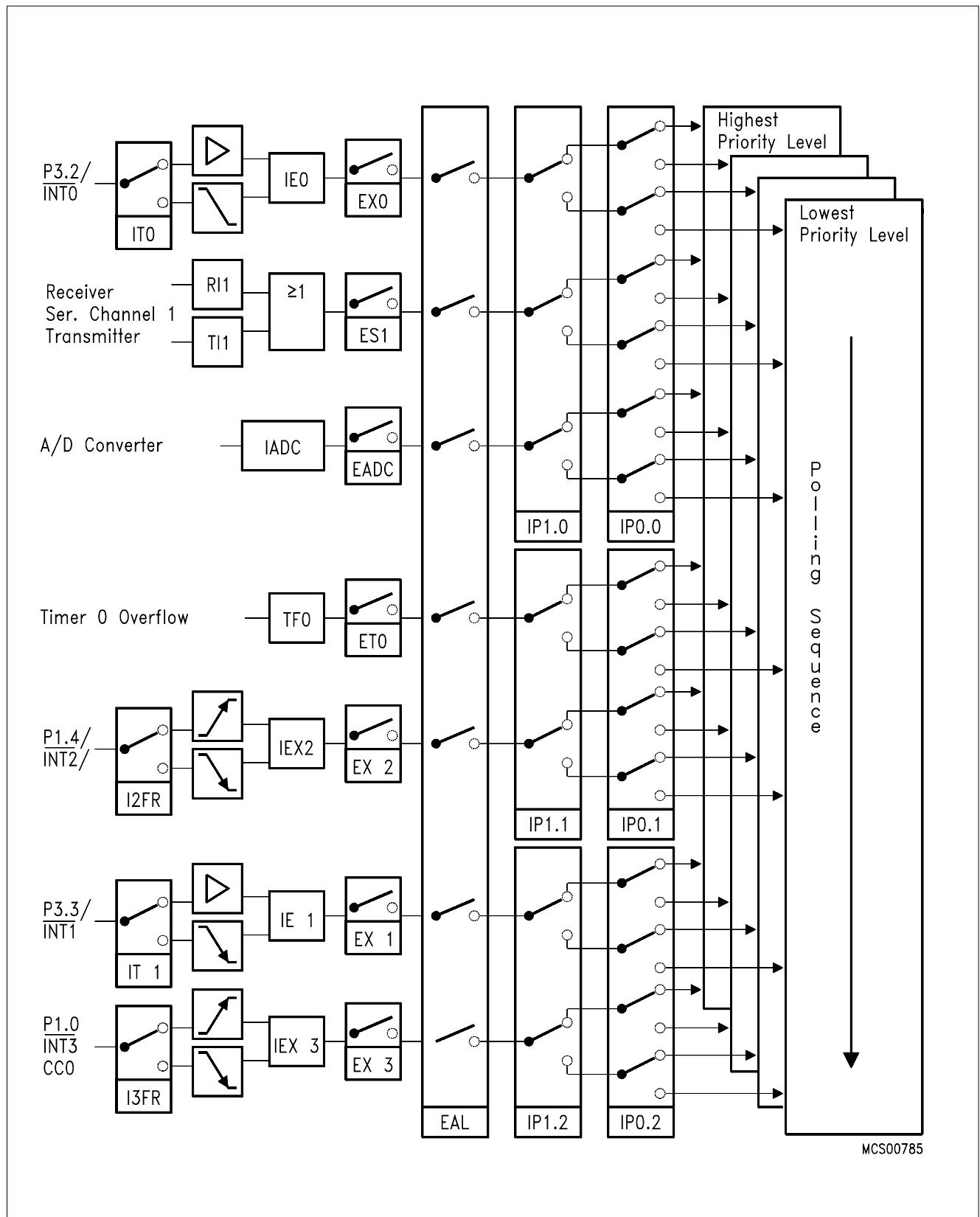
**Table 4**  
**Interrupt Sources and Vectors**

| Source (Request Flags) | Vector Address    | Vector                       |
|------------------------|-------------------|------------------------------|
| IE0                    | 0003 <sub>H</sub> | External interrupt 0         |
| TF0                    | 000B <sub>H</sub> | Timer 0 overflow             |
| IE1                    | 0013 <sub>H</sub> | External interrupt 1         |
| TF1                    | 001B <sub>H</sub> | Timer 1 overflow             |
| RI0/TI0                | 0023 <sub>H</sub> | Serial channel 0             |
| TF2 + EXF2             | 002B <sub>H</sub> | Timer 2 overflow/ext. reload |
| IADC                   | 0043 <sub>H</sub> | A/D converter                |
| IEX2                   | 004B <sub>H</sub> | External interrupt 2         |
| IEX3                   | 0053 <sub>H</sub> | External interrupt 3         |
| IEX4                   | 005B <sub>H</sub> | External interrupt 4         |
| IEX5                   | 0063 <sub>H</sub> | External interrupt 5         |
| IEX6                   | 006B <sub>H</sub> | External interrupt 6         |
| RI1/TI1                | 0083 <sub>H</sub> | Serial channel 1             |
| CTF                    | 009B <sub>H</sub> | Compare timer overflow       |

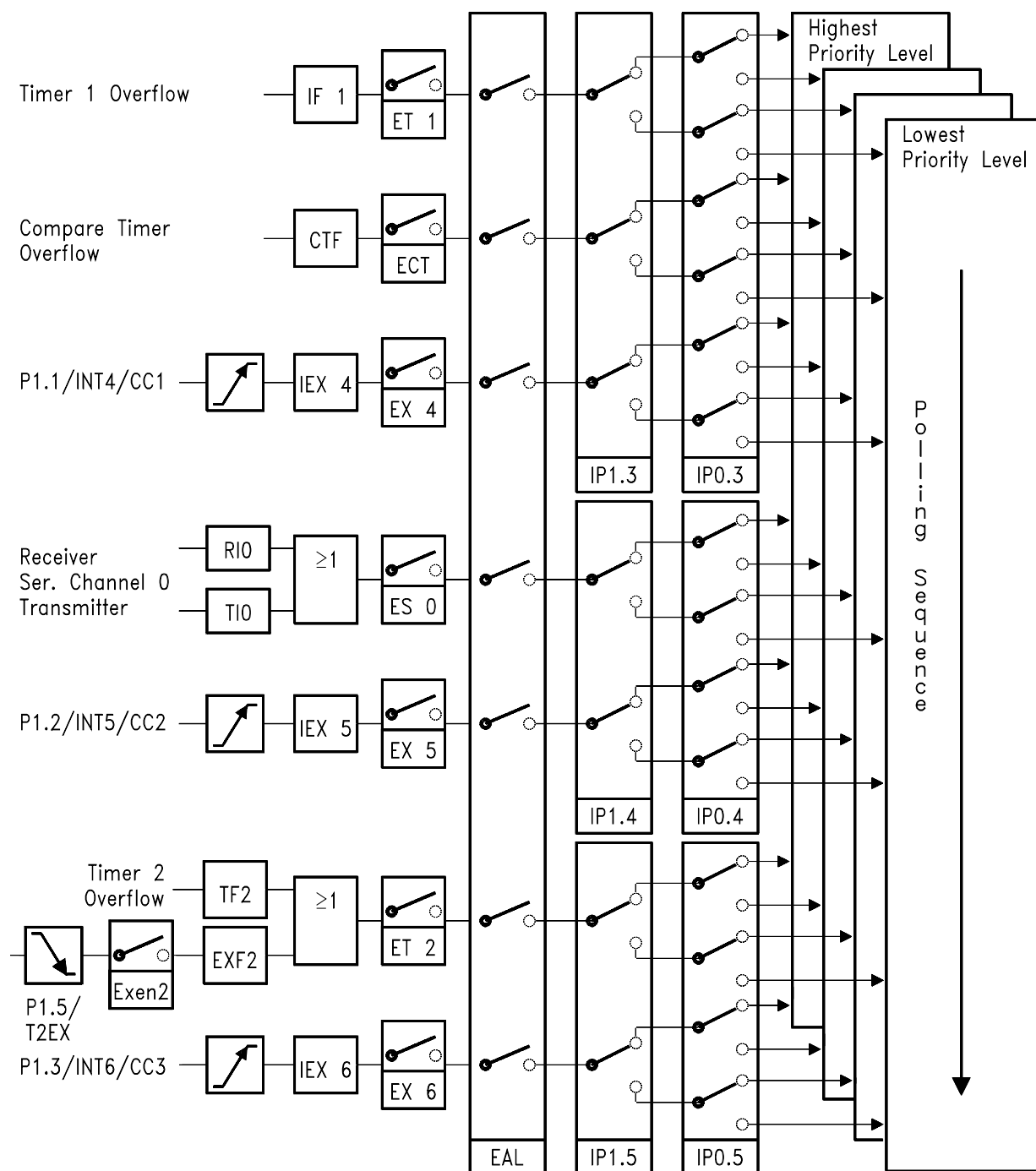
Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. **Figure 9** shows the interrupt request sources, the enabling and the priority level structure.



**Figure 9**  
**Interrupt Structure**



MCS00786

**Figure 9 (cont'd)**  
**Interrupt Structure**

### Multiplication/Division Unit

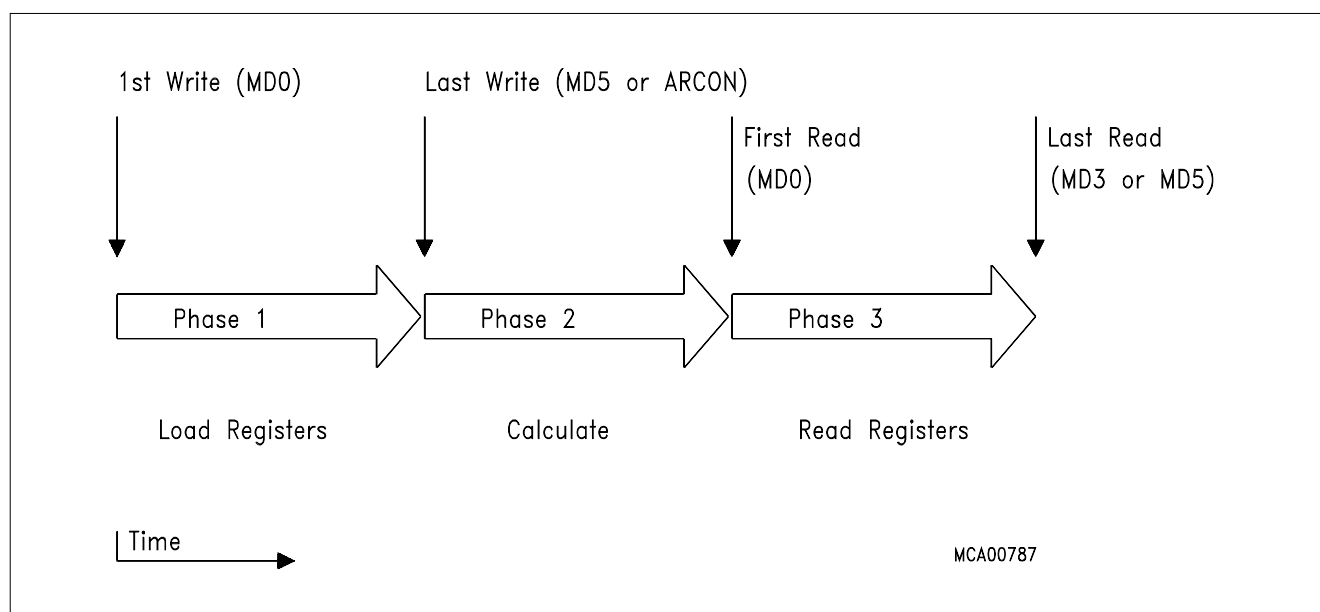
This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operations.

| Operation                      | Result           | Remainder        | Execution Time                |
|--------------------------------|------------------|------------------|-------------------------------|
| 32-bit/16-bit<br>16-bit/16-bit | 32-bit<br>16-bit | 16-bit<br>16-bit | $6 t_{cy}^{1)}$<br>$4 t_{cy}$ |
| 16-bit * 16-bit                | 32-bit           | —                | $4 t_{cy}$                    |
| 32-bit normalize               | —                | —                | $6 t_{cy}^{2)}$               |
| 32-bit shift left/right        | —                | —                | $6 t_{cy}^{2)}$               |

1)  $1 t_{cy} = 1 \mu s$  @ 12 MHz oscillator frequency.

2) The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:



**Figure 10**  
**Operation of the MDU**

To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (**see also the register description**).

**Table 5**  
**Programming the MDU for Multiplication and Division**

| Operation   | 32-Bit/16-Bit |        | 16-Bit/16-Bit |        | 16-Bit * 16-Bit |        |
|-------------|---------------|--------|---------------|--------|-----------------|--------|
| First Write | MD0           | D'endL | MD0           | D'endL | MD0             | M'andL |
|             | MD1           | D'end  | MD1           | D'end  | MD4             | M'orL  |
|             | MD2           | D'end  |               | D'end  |                 |        |
|             | MD3           | D'endH | MD4           | D'endH | MD1             | M'andH |
|             | MD4           | D'orL  |               | D'orL  |                 |        |
| Last Write  | MD5           | D'orH  | MD5           | D'orH  | MD5             | M'orH  |
| First Read  | MD0           | QuoL   | MD0           | QuoL   | MD0             | PrL    |
|             | MD1           | Quo    | MD1           | QuoH   | MD1             |        |
|             | MD2           | Quo    |               |        |                 |        |
|             | MD3           | QuoH   | MD4           | RemL   | MD2             |        |
|             | MD4           | RemL   |               |        |                 |        |
| Last Read   | MD5           | RemH   | MD5           | RemH   | MD3             | PrH    |

**Table 6**  
**Shift Operation with the CCU**

| Operation   | Normalize, Shift Left, Shift Right |                        |
|-------------|------------------------------------|------------------------|
| First Write | MD0                                | least significant byte |
|             | MD1                                |                        |
|             | MD2                                |                        |
|             | MD3                                | most significant byte  |
| Last Write  | ARCON                              | start of conversion    |
| First Read  | MD0                                | least significant byte |
|             | MD1                                |                        |
|             | MD2                                |                        |
| Last Read   | MD3                                | most significant byte  |

## Abbreviations

D'end : Dividend, 1st operand of division  
 D'or : Divisor, 2nd operand of division  
 M'and : Multiplicand, 1st operand of multiplication  
 M'or : Multiplier, 2nd operand of multiplication  
 Pr : Product, result of multiplication  
 Rem : Remainder  
 Quo : Quotient, result of division  
 ...L : means, that this byte is the least significant of the 16-bit or 32-bit operand  
 ...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

## I/O Ports

The SAB 80C517 has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Port 1, 3, 4, 5 and port 6 provide several alternate functions. **Please see the "Pin Description" for details.**

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit- addressable.

The SAB 80C517 has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels ( $V_{IL}$  and  $V_{IH}$ ) the port can also be used as digital input port.

## Power Saving Modes

The SAB 80C517 provides – due to Siemens AC MOS technology – three modes in which power consumption can be significantly reduced.

### – The **Slow Down Mode**

The controller keeps up the full operating functionality, but is driven with the eighth part of its normal operating frequency. Slowing down the frequency greatly reduces power consumption.

### – The **Idle Mode**

The CPU is gated off from the oscillator, but all peripherals are still supplied by the clock and able to work.

### – The **Power Down Mode**

Operation of the SAB 80C517 is stopped, the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current.

All of these modes are entered by software. Special function register PCON (power control register, address is 87<sub>H</sub>) is used to select one of these modes.

## Hardware Enable for Power Saving Modes

A dedicated Pin ( $\overline{\text{PE}}/\text{SWD}$ ) of the SAB 80C517 allows to block the power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer (see there for further description).

$\overline{\text{PE}}/\text{SWD} = V_{\text{IH}}$  (logic high level): Using of the power saving modes is not possible. The instruction sequences used for entering of these modes will not affect the normal operation of the device.

$\overline{\text{PE}}/\text{SWD} = V_{\text{IL}}$  (logic low level): All power saving modes can be activated by software. When left unconnected, Pin  $\overline{\text{PE}}/\text{SWD}$  is pulled to high level by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin  $\overline{\text{PE}}/\text{SWD}$  can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

## Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in **table 7**.

**Table 7**  
**Status of External Pins During Idle and Power Down**

| Outputs | Last instruction executed from internal code memory |                  | Last instruction executed from external code memory |                  |
|---------|-----------------------------------------------------|------------------|-----------------------------------------------------|------------------|
|         | Idle                                                | Power down       | Idle                                                | Power Down       |
| ALE     | High                                                | Low              | High                                                | Low              |
| PSEN    | High                                                | Low              | High                                                | Low              |
| Port 0  | Data                                                | Data             | Float                                               | Float            |
| Port 1  | Data/alternate outputs                              | Data/last output | Data/alternate outputs                              | Data/last output |
| Port 2  | Data                                                | Data             | Address                                             | Data             |
| Port 3  | Data/alternate outputs                              | Data/last output | Data/alternate outputs                              | Data/last output |
| Port 4  | Data/alternate outputs                              | Data/last output | Data/alternate outputs                              | Data/last output |
| Port 5  | Data/alternate outputs                              | Data/last output | Data/alternate outputs                              | Data/last output |
| Port 6  | Data/alternate outputs                              | Data/last output | Data/alternate outputs                              | Data/last output |

### Idle Mode

During idle mode all peripherals of the SAB 80C517 are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to entering the power down mode. The two bits IDLE and IDLS must be set by to consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and PSEN hold at logic high levels (see **table 7**).

**Table 8**  
**Baud Rate Generation**

| Function                  |                        | Serial Interface 0         |               | Serial Interface 1        |
|---------------------------|------------------------|----------------------------|---------------|---------------------------|
| 8-Bit synchronous channel | <b>Mode</b>            | <b>Mode 0</b>              |               | –                         |
|                           | Baud rate *)           | 1 MHz @ $f_{OSC} = 12$ MHz |               | –                         |
|                           | Baud rate derived from | $f_{OSC}$                  |               | –                         |
| 8-Bit UART                | <b>Mode</b>            | <b>Mode 1</b>              |               | <b>Mode B</b>             |
|                           | Baud rate *)           | 1 – 62.5 K                 | 4800, 9600    | 1.5 – 375 K               |
|                           | Baud rate derived from | Timer 1                    | BD            | 8-bit baud rate generator |
| 9-Bit UART                | <b>Mode</b>            | <b>Mode 2</b>              | <b>Mode 3</b> | <b>Mode A</b>             |
|                           | Baud rate *)           | 187.5 K/<br>375 K          | 1 – 62.5 K    | 1.5 – 375 K               |
|                           | Baud rate derived from | $f_{OSC}/2$                | Timer 1       | 8-bit baud rate generator |

\*) Baud rate values are given for 12 MHz oscillator frequency.

## Serial Interface 0

Serial Interface 0 can operate in 4 modes:

- Mode 0: Shift register mode:  
Serial data enters and exits through RXD0. TXD0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.
- Mode 1: 8-bit UART, variable baud rate:  
10-bit are transmitted (through RXD0) or received (through RXD0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.
- Mode 2: 9-bit UART, fixed baud rate:  
11-bit are transmitted (through TXD0) or received (through RXD0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.
- Mode 3: 9-bit UART, variable baud rate:  
11-bit are transmitted (through TXD0) or received (through RXD0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

## Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or from the oscillator via a special prescaler ("BD").

Timer 1 may be operated in mode 1 (to generate slow baud rates) or mode 2. The dedicated baud rate generator "BD" provides the two standard baud rates 4800 or 9600 baud with 0.16% deviation. **Table 8** shows possible configurations and the according baud rates.

SAB 80C517 devices with stepping code "CA" or later provide a dedicated baud rate generator for the serial interface 0. This baud rate genertaor is a free running 10-bit timer with programmable reload registers.

$$\text{Mode 1.3 baud rate} = \frac{2^{\text{SMOD}} \times f_{\text{OSC}}}{64 \times (2^{10} - \text{S0REL})}$$

The default value after reset in the reload registers S0RELL and S0RELH provide a baud rate of 4.8 kBaud (SMOD = 0) or 9.6 kBaud (SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C517 older steppings.

## Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

- Mode A: 9-bit UART, variable baud rate.  
11 bits are transmitted (through TXD0) or received (through RXD0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9<sup>th</sup> data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9<sup>th</sup> data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.
- Mode B: 8-bit UART, variable baud rate.  
10 bits are transmitted (through TXD1) or received (through RXD1): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

## Variable Baud Rates for Serial Interface 1

Variable baud rates for modes A and B of serial interface 1 can be derived from a dedicated baud rate generator.

The baud rate clock (baud rate =  $\frac{\text{baud rate clock}}{16}$ ) is generated by a 8-bit free

running timer with programmable reload register. SAB 80C517 devices with stepping code "CA" or later provide a 10-bit free running timer for baud rate generation.

$$\text{Mode A, B baud rate} = \frac{f_{\text{osc}}}{32 \times (2^{10} - \text{Reload Value})}$$

## Watchdog Units

The SAB 80C517 offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

- programmable watchdog timer (WDT), variable from 512 ms up to about 1.1 s time out period @12 MHz. Upward compatible to SAB 80515 watchdog.
- oscillator watchdog (OWD), monitors the on-chip oscillator and forces the microcontroller to go into reset state, in case the on-chip oscillator fails.

## Programmable Watchdog Timer

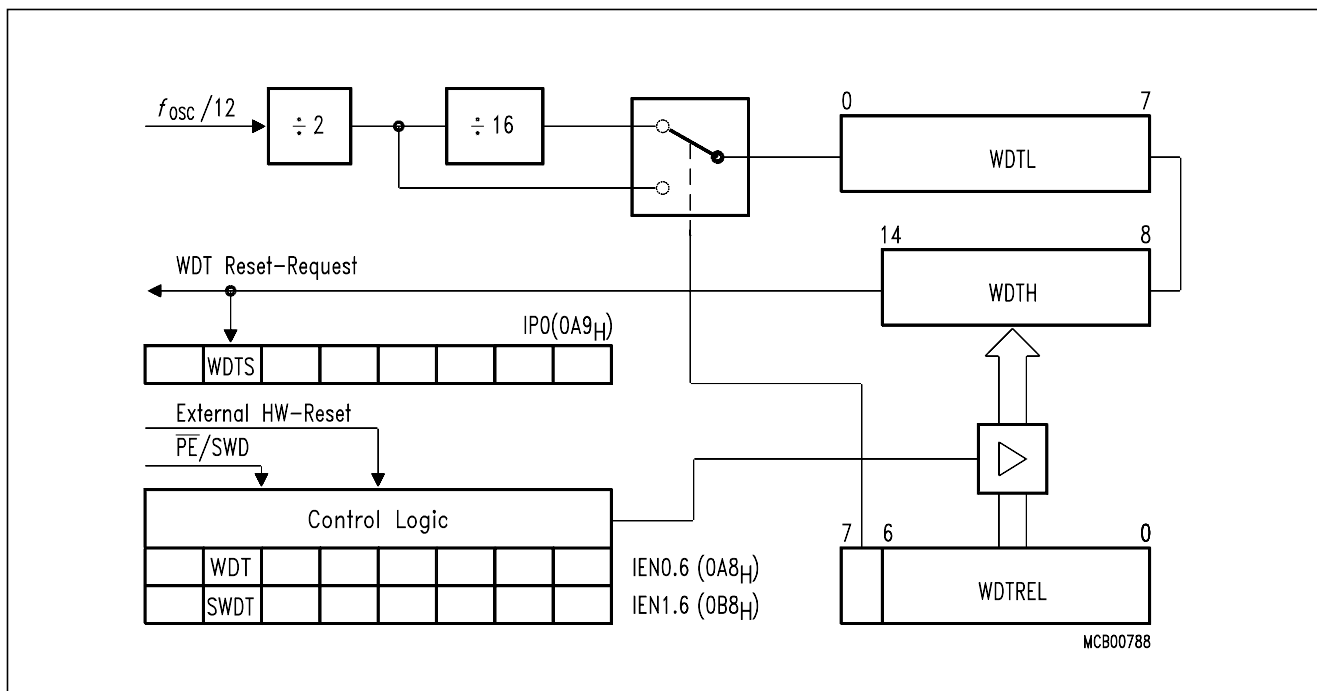
The WDT can be activated by hardware or software.

Hardware initialization is done when pin  $\overline{\text{PE/SWD}}$  (Pin 4) is held high during RESET. The SAB 80C517 then starts program execution with the WDT running. Pin  $\overline{\text{PE/SWD}}$  doesn't allow dynamic switching of the WDT.

Software initialization is done by setting bit SWDT. A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in **figure 11**.

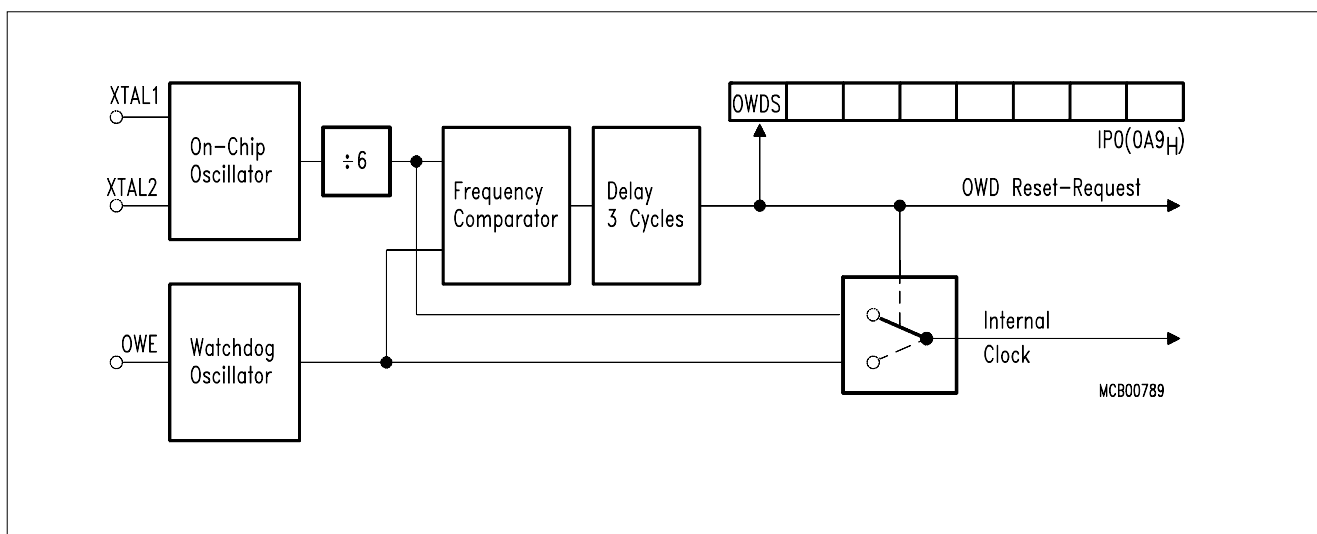
When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be manipulated by software.



### Figure 11 Block Diagram of the Programmable Watchdog Timer

## Oscillator Watchdog

The oscillator watchdog monitors the on-chip quartz oscillator. A detected oscillator failure ( $f_{\text{OSC}} < \text{appr. } 300 \text{ kHz}$ ) causes a hardware reset. The reset state is held until the on-chip oscillator is working again. The oscillator watchdog feature is enabled by a high level at pin OWE (pin 69). An oscillator watchdog reset sets status flag OWDS which can be examined and modified by software. **Figure 12** shows a block diagram of the oscillator watchdog.



### Figure 12

#### Functional Block Diagram of the Oscillator Watchdog

### Instruction Set Summary

The SAB 80C517/80C537 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

### Literature Information

| Title                                        | Ordering No.        |
|----------------------------------------------|---------------------|
| Microcontroller Family SAB 8051 Pocket Guide | B158-H6497-X-X-7600 |

## Absolute Maximum Ratings

Ambient temperature under bias

SAB 80C517/83C537 ..... 0 to 70 °C

SAB 80C517/83C537-T40/85 ..... – 40 to 85 °C

Storage temperature  $T_{ST}$  ..... – 65 to 150 °C

Voltage on  $V_{CC}$  pins with respect to ground ( $V_{SS}$ ) ..... – 0.5 V to 6.5 V

Voltage on any pin with respect to ground ( $V_{SS}$ ) ..... – 0.5 to  $V_{CC} + 0.5$  V

Input current on any pin during overload condition ..... – 10mA to +10mA

Absolute sum of all input currents during overload condition ..... |100mA|

Power dissipation ..... 2 W

**Note** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ( $V_{IN} > V_{CC}$  or  $V_{IN} < V_{SS}$ ) the Voltage on  $V_{CC}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

## DC Characteristics

$V_{CC} = 5 \text{ V} \pm 10 \%$ ;  $V_{SS} = 0 \text{ V}$ ;

$T_A = 0 \text{ to } 70 \text{ °C}$  for the SAB 80C517/83C537

$T_A = -40 \text{ to } 85 \text{ °C}$  for the SAB 80C517-/83C537-T40/85

| Parameter                                   | Symbol    | Limit Values       |                    | Unit | Test Condition                 |
|---------------------------------------------|-----------|--------------------|--------------------|------|--------------------------------|
|                                             |           | min.               | max.               |      |                                |
| Input low voltage (except $\overline{EA}$ ) | $V_{IL}$  | – 0.5              | $0.2 V_{CC} - 0.1$ | V    | –                              |
| Input low voltage ( $\overline{EA}$ )       | $V_{IL1}$ | – 0.5              | $0.2 V_{CC} - 0.3$ | V    | –                              |
| Input high voltage                          | $V_{IH}$  | $0.2 V_{CC} + 0.9$ | $V_{CC} + 0.5$     | V    | –                              |
| Input high voltage to XTAL2                 | $V_{IH1}$ | $0.7 V_{CC}$       | $V_{CC} + 0.5$     | V    | –                              |
| Input high voltage to $\overline{RESET}$    | $V_{IH2}$ | $0.6 V_{CC}$       | $V_{CC} + 0.5$     | V    | –                              |
| Output low voltage (ports 1, 2, 3, 4, 5, 6) | $V_{OL}$  | –                  | 0.45               | V    | $I_{OL} = 1.6 \text{ mA}^{1)}$ |

Notes see page 47.

## DC Characteristics (cont'd)

| Parameter                                                                                                        | Symbol    | Limit Values        |         | Unit          | Test Condition                                                      |
|------------------------------------------------------------------------------------------------------------------|-----------|---------------------|---------|---------------|---------------------------------------------------------------------|
|                                                                                                                  |           | min.                | max.    |               |                                                                     |
| Output low voltage<br>(ports ALE, $\overline{\text{PSEN}}$ , $\overline{\text{RO}}$ )                            | $V_{OL1}$ | –                   | 0.45    | V             | $I_{OL} = 3.2\text{mA}^{1)}$                                        |
| Output high voltage<br>(ports 1, 2, 3, 4, 5, 6)                                                                  | $V_{OH}$  | 2.4<br>$0.9 V_{CC}$ | –<br>–  | V<br>V        | $I_{OH} = -80 \mu\text{A}$<br>$I_{OH} = -10 \mu\text{A}$            |
| Output high voltage<br>(port 0 in external bus mode,<br>ALE, $\overline{\text{PSEN}}$ , $\overline{\text{RO}}$ ) | $V_{OH1}$ | 2.4<br>$0.9 V_{CC}$ | –<br>–  | V<br>V        | $I_{OH} = -800 \mu\text{A}^{2)}$<br>$I_{OH} = -80 \mu\text{A}^{2)}$ |
| Logic 0 input current<br>(ports 1, 2, 3, 4, 5, 6)                                                                | $I_{IL}$  | – 10                | – 70    | $\mu\text{A}$ | $V_{IN} = 0.45 \text{ V}$                                           |
| Input low current to $\overline{\text{RESET}}$<br>for reset                                                      | $I_{IL2}$ | – 10                | –100    | $\mu\text{A}$ | $V_{IN} = 0.45 \text{ V}$                                           |
| Input low current (XTAL2)                                                                                        | $I_{IL3}$ | –                   | – 15    | $\mu\text{A}$ | $V_{IN} = 0.45 \text{ V}$                                           |
| Input low current<br>(OWE, PE/SWD)                                                                               | $I_{IL4}$ | –                   | – 20    | $\mu\text{A}$ | $V_{IN} = 0.45 \text{ V}$                                           |
| Logical 1-to-0 transition current<br>(ports 1, 2, 3, 4, 5, 6)                                                    | $I_{TL}$  | – 65                | – 650   | $\mu\text{A}$ | $V_{IN} = 2 \text{ V}$                                              |
| Input leakage current<br>(port 0, EA, ports 7, 8)                                                                | $I_{LI}$  | –                   | $\pm 1$ | $\mu\text{A}$ | $0.45 < V_{IN} < V_{CC}^{10)}$                                      |
| Pin capacitance                                                                                                  | $C_{IO}$  | –                   | 10      | pF            | $f_C = 1 \text{ MHz}$<br>$T_A = 25^\circ\text{C}$                   |
| Power supply current:<br>Active mode, 12 MHz <sup>6)</sup>                                                       | $I_{CC}$  | –                   | 40      | mA            | $V_{CC} = 5 \text{ V},^{4)}$                                        |
| Idle mode, 12 MHz <sup>6)</sup>                                                                                  |           | –                   | 15      | mA            | $V_{CC} = 5 \text{ V},^{5)}$                                        |
| Slow down mode, 12 MHz <sup>6)</sup>                                                                             |           | –                   | 15      | mA            | $V_{CC} = 5 \text{ V},^{5)}$                                        |
| Active mode, 16 MHz <sup>6)</sup>                                                                                | $I_{CC}$  | –                   | 52.3    | mA            | $V_{CC} = 5 \text{ V},^{4)}$                                        |
| Idle mode, 16 MHz <sup>6)</sup>                                                                                  |           | –                   | 19      | mA            | $V_{CC} = 5 \text{ V},^{5)}$                                        |
| Slow down mode, 16MHz <sup>6)</sup>                                                                              |           | –                   | 19      | mA            | $V_{CC} = 5 \text{ V},^{5)}$                                        |
| Power down Mode                                                                                                  | $I_{PD}$  | –                   | 50      | $\mu\text{A}$ | $V_{CC} = 2...5.5 \text{ V}^{3)}$                                   |

Notes see page 47.

## A/D Converter Characteristics

$V_{CC} = 5 \text{ V} \pm 10 \%$ ;  $V_{SS} = 0 \text{ V}$

$V_{AREF} = V_{CC} \pm 5\%$ ;  $V_{AGND} = V_{SS} \pm 0.2 \text{ V}$ ;  $V_{IntAREF} - V_{IntAGND} \geq 1 \text{ V}$

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$  for the SAB 80C517/83C537

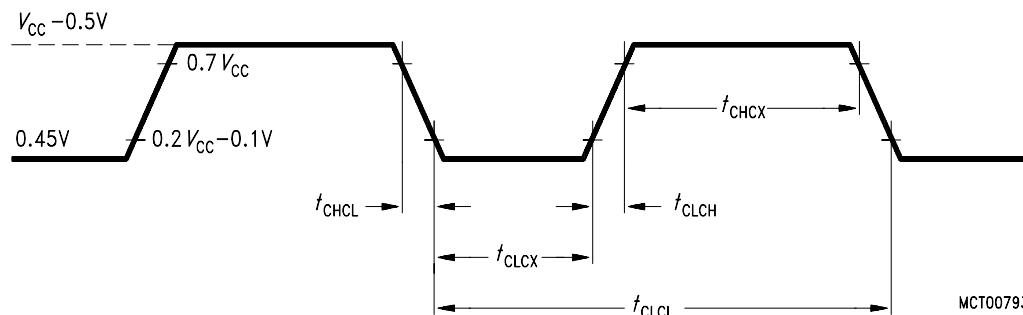
$T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$  for the SAB 80C517/83C537-T40/875

| Parameter                           | Symbol          | Limit values     |      |                  | Unit          | Test Condition                                 |
|-------------------------------------|-----------------|------------------|------|------------------|---------------|------------------------------------------------|
|                                     |                 | min.             | typ. | max.             |               |                                                |
| Analog input voltage                | $V_{AINPUT}$    | $V_{AGND} - 0.2$ | —    | $V_{AREF} + 0.2$ | V             | 9)                                             |
| Analog input capacitance            | $C_I$           | —                | 25   | 60               | pF            | 7)                                             |
| Load time                           | $t_L$           | —                | —    | $2 t_{CY}$       | $\mu\text{s}$ | 7)                                             |
| Sample time (incl. load time)       | $t_S$           | —                | —    | $7 t_{CY}$       | $\mu\text{s}$ | 7)                                             |
| Conversion time (incl. sample time) | $t_C$           | —                | —    | $13 t_{CY}$      | $\mu\text{s}$ | 7)                                             |
| Total unadjusted error              | TUE             | —                | —    | $\pm 2$          | LSB           | $V_{AREF} = V_{CC}$<br>$V_{AGND} = V_{SS}$ 11) |
| Internal reference error            | $V_{IntREFERR}$ | —                | —    | $\pm 30$         | mV            | 8)                                             |
| $V_{AREF}$ supply current           | $I_{REF}$       | —                | —    | 5                | mA            | 8)                                             |

Notes see page 47.

**Notes** for pages 44, 45 and 46:

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$  of ALE and ports 1, 3, 4, 5 and 6. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.  
In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt- trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and  $\overline{PSEN}$  to momentarily fall below the 0.9  $V_{CC}$  specification when the address lines are stabilizing.
- 3) Power down  $I_{PD}$  is measured with all output pins disconnected;  
 $\overline{EA} = \overline{RESET} = V_{CC}$ ; Port 0 = Port 7 = Port 8 =  $V_{CC}$ ; XTAL1 = N.C.; XTAL2 =  $V_{SS}$ ;  
 $V_{AGND} = N.C.$ ;  $V_{AREF} = V_{CC}$ ;  $\overline{PE}/SWD = OWE = V_{SS}$ .
- 4)  $I_{CC}$  (active mode) is measured with all output pins disconnected; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;  
 $\overline{EA} = OWE = \overline{PE}/SWD = V_{CC}$ ; Port 0 = Port 7 = Port 8 =  $V_{CC}$ ;  
 $\overline{RESET} = V_{SS}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator is used.
- 5)  $I_{CC}$  (idle mode,) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;  
 $\overline{RESET} = OWE = V_{CC}$ ; Port 0 = Port 7 = Port 8 =  $V_{CC}$ ;  $\overline{EA} = \overline{PE}/SWD = V_{SS}$ .  
 $I_{CC}$  (slow down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL = N.C.;  
Port 7 = Port 8 =  $V_{CC}$ ;  $\overline{EA} = \overline{PE}/SWD = V_{SS}$ .
- 6)  $I_{CC}$  (max.) at other frequencies is given by: active mode:  $I_{CC} \text{ max} = 3.1 * f_{OSC} + 3.0$   
idle mode:  $I_{CC} \text{ max} = 1.0 * f_{OSC} + 3.0$   
Where  $f_{OSC}$  is the oscillator frequency in MHz.  $I_{CC}$  values are given in mA and measured at  $V_{CC} = 5 \text{ V}$  (**see also notes 4 and 5**).
- 7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance ( $C_I$ ) during load time ( $T_L$ ). After charging of the internal capacitance ( $C_I$ ) in the load time ( $T_L$ ) the analog input must be held constant for the rest of the sample time ( $T_S$ ).
- 8) The differential impedance  $R_D$  of the analog reference voltage source must be less than 1 k $\Omega$  at reference supply voltage.
- 9) Exceeding the limit values at one or more input channels will cause additional current which is sunk/sourced at these channels. This may also affect the accuracy of other channels which are operated within the specification.
- 10) Only valid for not selected analog inputs.
- 11) No missing code.



**Clock of Waveform for  $I_{CC}$  Tests in Active, Idle Mode and Slow Down Mode**

## AC Characteristics

$V_{CC} = 5 \text{ V} \pm 10 \%$ ;  $V_{SS} = 0 \text{ V}$   $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$  for the SAB 80C517/83C537  
 $T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$  for the SAB 80C517/83C537-T40/85  
( $C_L$  for port 0, ALE and PSEN outputs = 100 pF;  $C_L$  for all other outputs = 80 pF)

| Parameter | Symbol | Limit Values |      |                                                           |      | Unit |
|-----------|--------|--------------|------|-----------------------------------------------------------|------|------|
|           |        | 12 MHz Clock |      | Variable Clock<br>1/t <sub>CLCL</sub> = 3.5 MHz to 12 MHz |      |      |
|           |        | min          | max. | min.                                                      | max. |      |

## Program Memory Characteristics

|                                                           |                 |     |     |                   |                   |    |
|-----------------------------------------------------------|-----------------|-----|-----|-------------------|-------------------|----|
| ALE pulse width                                           | $t_{LHLL}$      | 127 | –   | $2 t_{CLCL} - 40$ | –                 | ns |
| Address setup to ALE                                      | $t_{AVLL}$      | 53  | –   | $t_{CLCL} - 30$   | –                 | ns |
| Address hold after ALE                                    | $t_{LLAX}$      | 48  | –   | $t_{CLCL} - 35$   | –                 | ns |
| ALE to valid instruction in                               | $t_{LLIV}$      | –   | 233 | –                 | $4t_{CLCL} - 100$ | ns |
| ALE to $\overline{\text{PSEN}}$                           | $t_{LLPL}$      | 58  | –   | $t_{CLCL} - 25$   | –                 | ns |
| $\overline{\text{PSEN}}$ pulse width                      | $t_{PLPH}$      | 215 | –   | $3 t_{CLCL} - 35$ | –                 | ns |
| $\overline{\text{PSEN}}$ to valid instruction in          | $t_{PLIV}$      | –   | 150 | –                 | $3t_{CLCL} - 100$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$     | $t_{PXIX}$      | 0   | –   | 0                 |                   | ns |
| Input instruction float after $\overline{\text{PSEN}}$ *) | $t_{PXIX}^{*)}$ | –   | 63  | –                 | $t_{CLCL} - 20$   | ns |
| Address valid after $\overline{\text{PSEN}}$ *)           | $t_{PXAV}^{*)}$ | 75  | –   | $t_{CLCL} - 8$    | –                 | ns |
| Address to valid instruction in                           | $t_{AVIV}$      | –   | 302 | 0                 | $5t_{CLCL} - 115$ | ns |
| Address float to $\overline{\text{PSEN}}$                 | $t_{AZPL}$      | –   | –   | –                 |                   | ns |

\*) Interfacing the SAB 80C517 to devices with float times up to 75 ns is permissible.  
This limited bus contention will not cause any damage to port 0 drivers.

## AC Characteristics (cont'd)

| Parameter | Symbol | Limit Values |      |                                                           |      | Unit |
|-----------|--------|--------------|------|-----------------------------------------------------------|------|------|
|           |        | 12 MHz Clock |      | Variable Clock<br>1/t <sub>CLCL</sub> = 3.5 MHz to 12 MHz |      |      |
|           |        | min          | max. | min.                                                      | max. |      |

## External Data Memory Characteristics

|                                                                   |             |     |     |                    |                    |    |
|-------------------------------------------------------------------|-------------|-----|-----|--------------------|--------------------|----|
| $\overline{\text{RD}}$ pulse width                                | $t_{RLRH}$  | 400 | —   | $6 t_{CLCL} - 100$ | —                  | ns |
| $\overline{\text{WR}}$ pulse width                                | $t_{WLWH}$  | 400 | —   | $6 t_{CLCL} - 100$ | —                  | ns |
| Address hold after ALE                                            | $t_{LLAX2}$ | 132 | —   | $2 t_{CLCL} - 30$  | —                  | ns |
| $\overline{\text{RD}}$ to valid instr in                          | $t_{RLDV}$  | —   | 252 | —                  | $5 t_{CLCL} - 165$ | ns |
| Data hold after $\overline{\text{RD}}$                            | $t_{RHDX}$  | 0   | —   | 0                  | —                  | ns |
| Data float after $\overline{\text{RD}}$                           | $t_{RHDZ}$  | —   | 97  | —                  | $2 t_{CLCL} - 70$  | ns |
| ALE to valid data in                                              | $t_{LLDV}$  | —   | 517 | —                  | $8 t_{CLCL} - 150$ | ns |
| Address to valid data in                                          | $t_{AVDV}$  | —   | 585 | —                  | $9 t_{CLCL} - 165$ | ns |
| ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$           | $t_{LLWL}$  | 200 | 300 | $3 t_{CLCL} - 50$  | $3 t_{CLCL} + 50$  | ns |
| $\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high | $t_{WHLH}$  | 43  | 123 | $t_{CLCL} - 40$    | $t_{CLCL} + 40$    | ns |
| Address valid to $\overline{\text{WR}}$                           | $t_{AVWL}$  | 203 | —   | $4 t_{CLCL} - 130$ | —                  | ns |
| Data valid to $\overline{\text{WR}}$ transition                   | $t_{QVWX}$  | 33  | —   | $t_{CLCL} - 50$    | —                  | ns |
| Data setup before $\overline{\text{WR}}$                          | $t_{QVWX}$  | 433 | —   | $7 t_{CLCL} - 150$ | —                  | ns |
| Data hold after $\overline{\text{WR}}$                            | $t_{WHQX}$  | 33  | —   | $t_{CLCL} - 50$    | —                  | ns |
| Address float after $\overline{\text{RD}}$                        | $t_{RLAZ}$  | —   | 0   | —                  | 0                  | ns |

## AC Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$ ;  $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$  for the SAB 80C517-16/83C537-16

$T_A = -40\text{ to }85\text{ }^\circ\text{C}$  for the SAB 80C517-16/83C537-16-T40/85

( $C_L$  for port 0, ALE and PSEN outputs = 100pF;  $C_L$  for all outputs = 80 pF)

| Parameter | Symbol | Limit Values |      |                                                           |      | Unit |
|-----------|--------|--------------|------|-----------------------------------------------------------|------|------|
|           |        | 16 MHz Clock |      | Variable Clock<br>1/t <sub>CLCL</sub> = 3.5 MHz to 16 MHz |      |      |
|           |        | min          | max. | min.                                                      | max. |      |

## Program Memory Characteristics

|                                                           |            |     |     |                   |                   |    |
|-----------------------------------------------------------|------------|-----|-----|-------------------|-------------------|----|
| ALE pulse width                                           | $t_{LHLL}$ | 85  | —   | $2 t_{CLCL} - 40$ | —                 | ns |
| Address setup to ALE                                      | $t_{AVLL}$ | 33  | —   | $t_{CLCL} - 30$   | —                 | ns |
| Address hold after ALE                                    | $t_{LLAX}$ | 28  | —   | $t_{CLCL} - 35$   | —                 | ns |
| ALE to valid instr. in                                    | $t_{LLIV}$ | —   | 150 | —                 | $4t_{CLCL} - 100$ | ns |
| ALE to $\overline{\text{PSEN}}$                           | $t_{LLPL}$ | 38  | —   | $t_{CLCL} - 25$   | —                 | ns |
| $\overline{\text{PSEN}}$ pulse width                      | $t_{PLPH}$ | 153 | —   | $3 t_{CLCL} - 35$ | —                 | ns |
| $\overline{\text{PSEN}}$ to valid instr. in               | $t_{PLIV}$ | —   | 88  | —                 | $3t_{CLCL} - 100$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$     | $t_{PXIX}$ | 0   | —   | 0                 | —                 | ns |
| Input instruction float *) after $\overline{\text{PSEN}}$ | $t_{PXIZ}$ | —   | 43  | —                 | $t_{CLCL} - 20$   | ns |
| Address valid after $\overline{\text{PSEN}}$ *)           | $t_{PXAV}$ | 55  | —   | $t_{CLCL} - 8$    | —                 | ns |
| Address to valid instr. in                                | $t_{AVIV}$ | —   | 198 | 0—                | $5t_{CLCL} - 115$ | ns |
| Address float to $\overline{\text{PSEN}}$                 | $t_{AZPL}$ | 0   | —   | 0                 | —                 | ns |

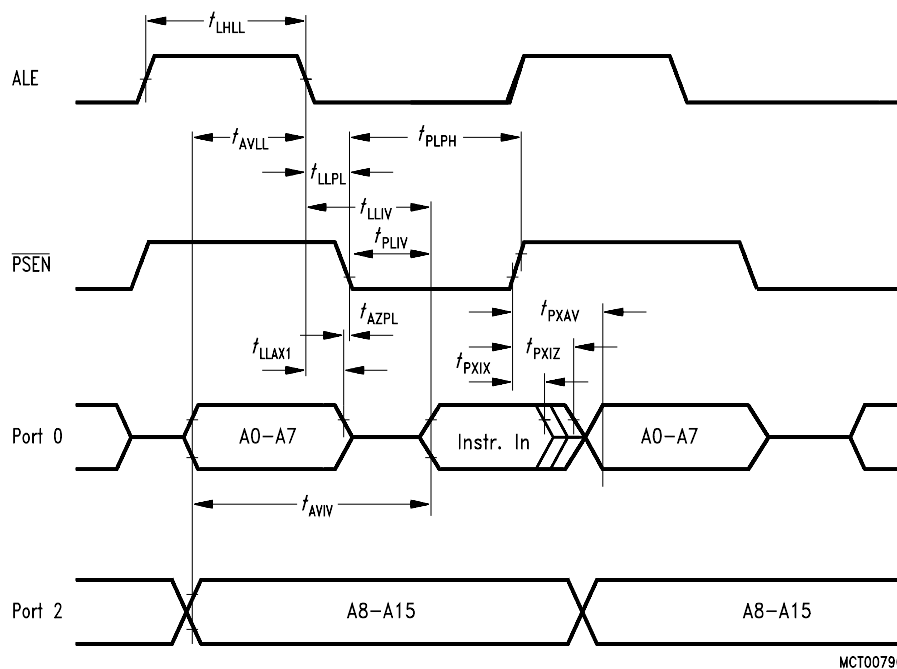
\*) Interfacing the SAB 80C517 to devices with float times up to 55 ns is permissible.  
This limited bus contention will not cause any damage to port 0 drivers.

## AC Characteristics (cont'd)

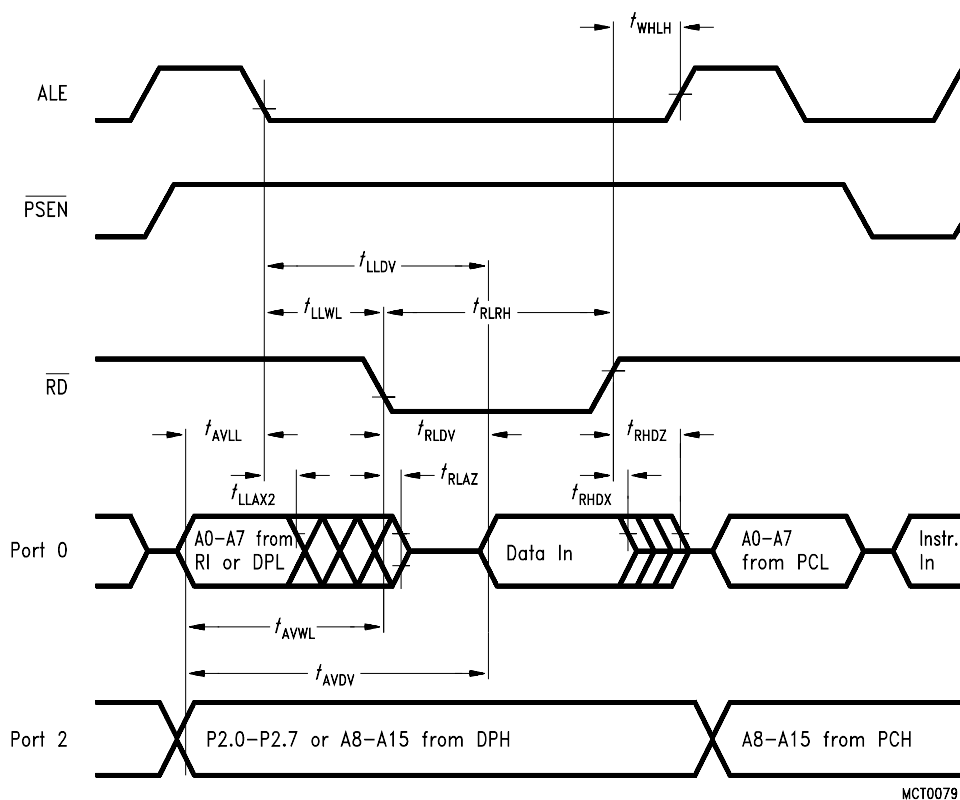
| Parameter | Symbol | Limit Values |      |                                                           |      | Unit |
|-----------|--------|--------------|------|-----------------------------------------------------------|------|------|
|           |        | 16 MHz Clock |      | Variable Clock<br>1/t <sub>CLCL</sub> = 3.5 MHz to 16 MHz |      |      |
|           |        | min          | max. | min.                                                      | max. |      |

## External Data Memory Characteristics

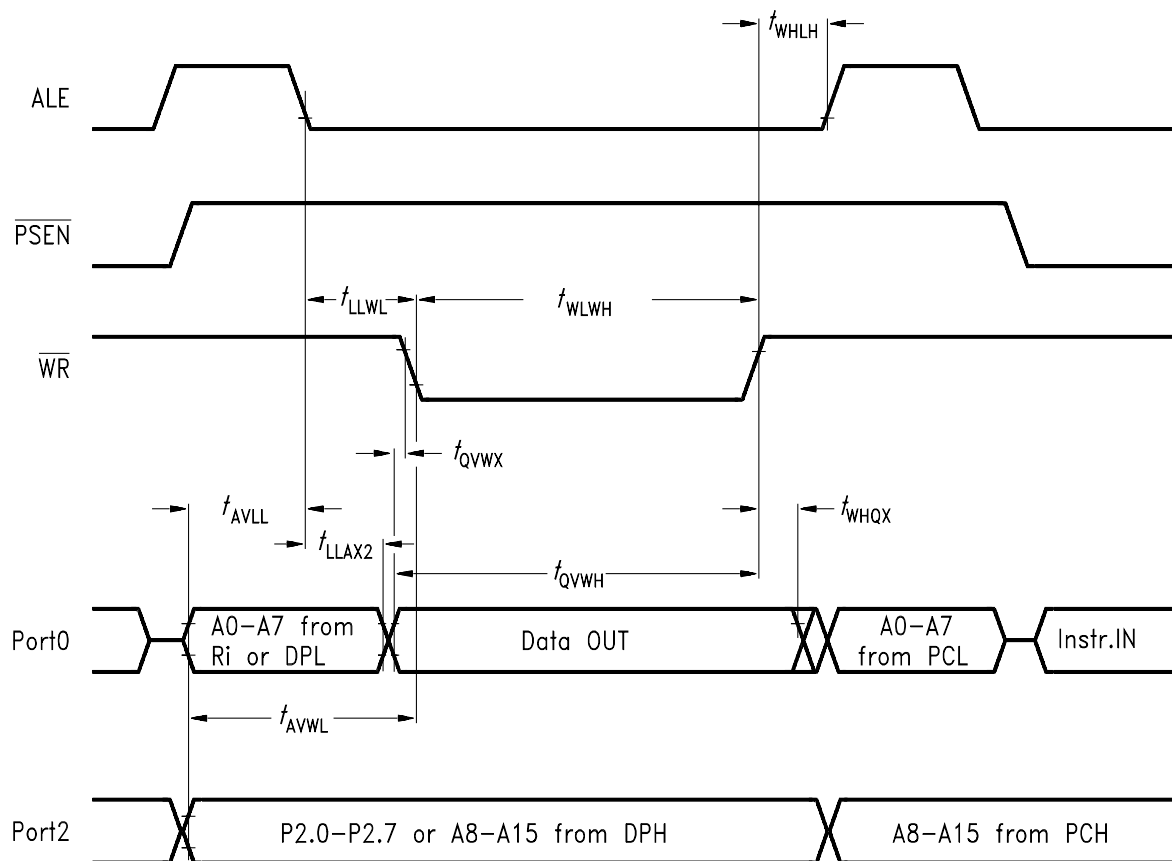
|                                                     |             |     |     |                    |                    |    |
|-----------------------------------------------------|-------------|-----|-----|--------------------|--------------------|----|
| $\overline{RD}$ pulse width                         | $t_{RLRH}$  | 275 | –   | $6 t_{CLCL} - 100$ | –                  | ns |
| $\overline{WR}$ pulse width                         | $t_{WLWH}$  | 275 | –   | $6 t_{CLCL} - 100$ | –                  | ns |
| Address hold after ALE                              | $t_{LLAX2}$ | 90  | –   | $2 t_{CLCL} - 35$  | –                  | ns |
| $\overline{RD}$ to valid data in                    | $t_{RLDV}$  | –   | 148 | –                  | $5 t_{CLCL} - 165$ | ns |
| Data hold after $\overline{RD}$                     | $t_{RHDX}$  | 0   | –   | 0                  | –                  | ns |
| Data float after $\overline{RD}$                    | $t_{RHDZ}$  | –   | 55  | –                  | $2 t_{CLCL} - 70$  | ns |
| ALE to valid data in                                | $t_{LLDV}$  | –   | 350 | –                  | $8 t_{CLCL} - 150$ | ns |
| Address to valid data in                            | $t_{AVDV}$  | –   | 398 | –                  | $9 t_{CLCL} - 165$ | ns |
| ALE to $\overline{WR}$ or $\overline{RD}$           | $t_{LLWL}$  | 138 | 238 | $3 t_{CLCL} - 50$  | $3 t_{CLCL} + 50$  | ns |
| $\overline{WR}$ or $\overline{RD}$ high to ALE high | $t_{WHLH}$  | 23  | 103 | $t_{CLCL} - 40$    | $t_{CLCL} + 40$    | ns |
| Address valid to $\overline{WR}$                    | $t_{AVWL}$  | 120 | –   | $4 t_{CLCL} - 130$ | –                  | ns |
| Data valid to $\overline{WR}$ transition            | $t_{QVWX}$  | 13  | –   | $t_{CLCL} - 50$    | –                  | ns |
| Data setup before $\overline{WR}$                   | $t_{QVWH}$  | 288 | –   | $7 t_{CLCL} - 150$ | –                  | ns |
| Data hold after $\overline{WR}$                     | $t_{WHQX}$  | 13  | –   | $t_{CLCL} - 50$    | –                  | ns |
| Address float after $\overline{RD}$                 | $t_{RLAZ}$  | –   | 0   | –                  | 0                  | ns |



## Program Memory Read Cycle



## Data Memory Read Cycle



MCT00098

## Data Memory Write Cycle

## AC Characteristics (cont'd)

| Parameter | Symbol | Limit Values                                 |      | Unit |
|-----------|--------|----------------------------------------------|------|------|
|           |        | Variable Clock<br>Frequ. = 3.5 MHz to 12 MHz |      |      |
|           |        | min                                          | max. |      |

## External Clock Drive

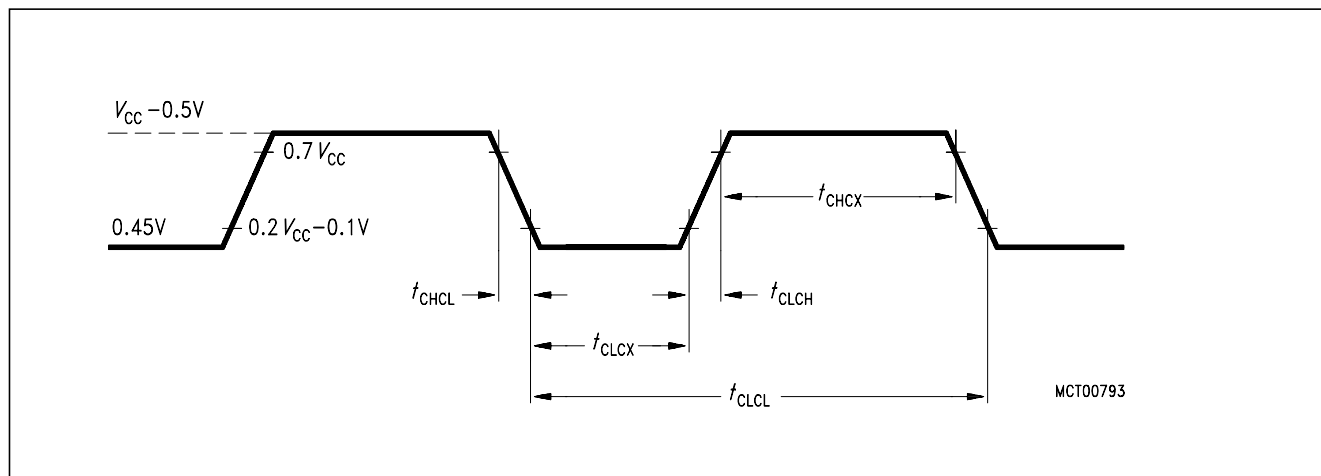
|                      |              |      |     |     |
|----------------------|--------------|------|-----|-----|
| Oscillator period    | $t_{CLCL}$   | 83.3 | 285 | ns  |
| Oscillator frequency | $1/t_{CLCL}$ | 3.5  | 12  | MHz |
| High time            | $t_{CHCX}$   | 20   | —   | ns  |
| Low time             | $t_{CLCX}$   | 20   | —   | ns  |
| Rise time            | $t_{CLCH}$   | —    | 20  | ns  |
| Fall time            | $t_{CHCL}$   | —    | 20  | ns  |

## AC Characteristics (cont'd)

| Parameter | Symbol | Limit Values                               |      | Unit |
|-----------|--------|--------------------------------------------|------|------|
|           |        | Variable Clock<br>Frequ. = 1 MHz to 16 MHz |      |      |
|           |        | min                                        | max. |      |

## External Clock Drive

|                      |              |      |     |     |
|----------------------|--------------|------|-----|-----|
| Oscillator period    | $t_{CLCL}$   | 62.5 | 285 | ns  |
| Oscillator frequency | $1/t_{CLCL}$ | 3.5  | 16  | MHz |
| High time            | $t_{CHCX}$   | 25   | —   | ns  |
| Low time             | $t_{CLCX}$   | 25   | —   | ns  |
| Rise time            | $t_{CLCH}$   | —    | 20  | ns  |
| Fall time            | $t_{CHCL}$   | —    | 20  | ns  |



## External Clock Cycle

## AC Characteristics (cont'd)

| Parameter | Symbol | Limit Values |      |                                                          |      | Unit |
|-----------|--------|--------------|------|----------------------------------------------------------|------|------|
|           |        | 12 MHz Clock |      | Variable Clock<br>1/t <sub>CLCL</sub> =3.5 MHz to 12 MHz |      |      |
|           |        | min.         | max. | min.                                                     | max. |      |

## System Clock Timing

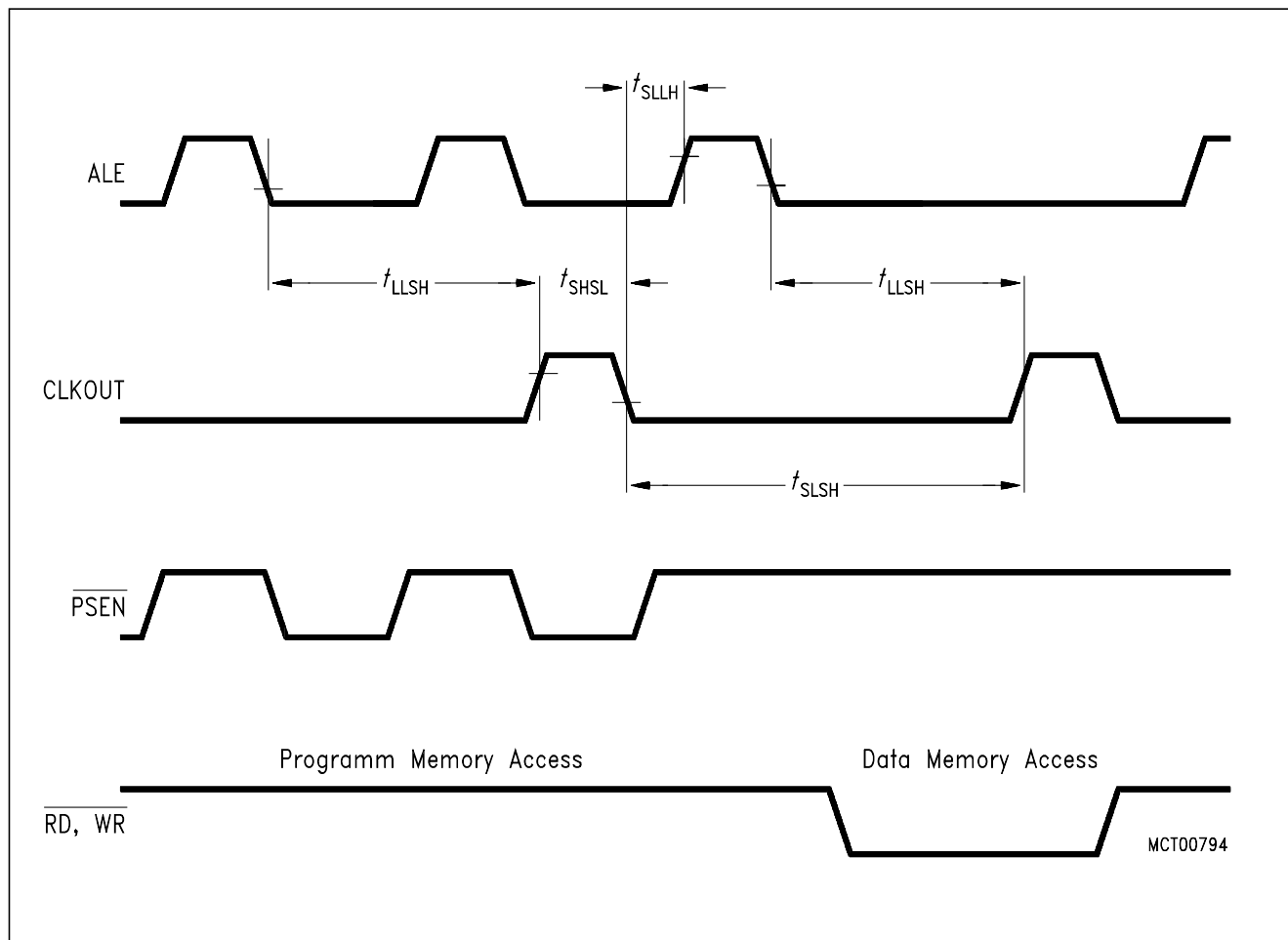
|                        |            |     |     |                   |                 |    |
|------------------------|------------|-----|-----|-------------------|-----------------|----|
| ALE to CLKOUT          | $t_{LLSH}$ | 543 | —   | $7t_{CLCL} - 40$  | —               | ns |
| CLKOUT high time       | $t_{SHSL}$ | 127 | —   | $2t_{CLCL} - 40$  | —               | ns |
| CLKOUT low time        | $t_{SLSH}$ | 793 | —   | $10t_{CLCL} - 40$ | —               | ns |
| CLKOUT low to ALE high | $t_{SLLH}$ | 43  | 123 | $t_{CLCL} - 40$   | $t_{CLCL} + 40$ | ns |

## AC Characteristics (cont'd)

| Parameter | Symbol | Limit Values |      |                                                           |      | Unit |
|-----------|--------|--------------|------|-----------------------------------------------------------|------|------|
|           |        | 16 MHz Clock |      | Variable Clock<br>1/t <sub>CLCL</sub> = 3.5 MHz to 16 MHz |      |      |
|           |        | min.         | max. | min.                                                      | max. |      |

## System Clock Timing

|                        |            |     |     |                   |                 |    |
|------------------------|------------|-----|-----|-------------------|-----------------|----|
| ALE to CLKOUT          | $t_{LLSH}$ | 398 | —   | $7t_{CLCL} - 40$  | —               | ns |
| CLKOUT high time       | $t_{SHSL}$ | 85  | —   | $2t_{CLCL} - 40$  | —               | ns |
| CLKOUT low time        | $t_{SLSH}$ | 585 | —   | $10t_{CLCL} - 40$ | —               | ns |
| CLKOUT low to ALE high | $t_{SLLH}$ | 23  | 103 | $t_{CLCL} - 40$   | $t_{CLCL} + 40$ | ns |



## System Clock Timing

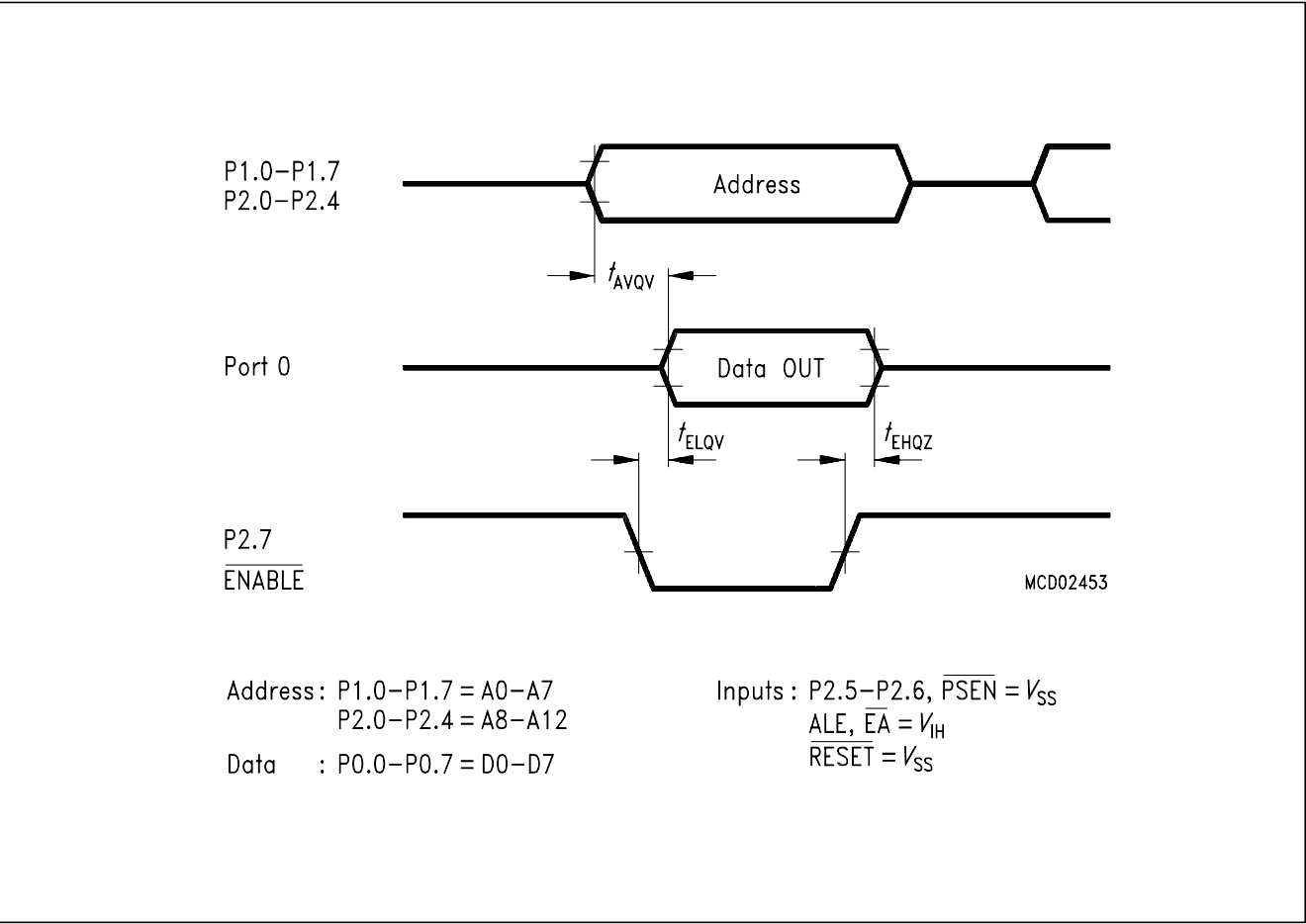
ROM Verification Characteristics

$T_A = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}; V_{CC} = 5\text{ V} \pm 10\%; V_{SS} = 0\text{ V}$

| Parameter | Symbol | Limit values |      | Unit |
|-----------|--------|--------------|------|------|
|           |        | min          | max. |      |

ROM Verification

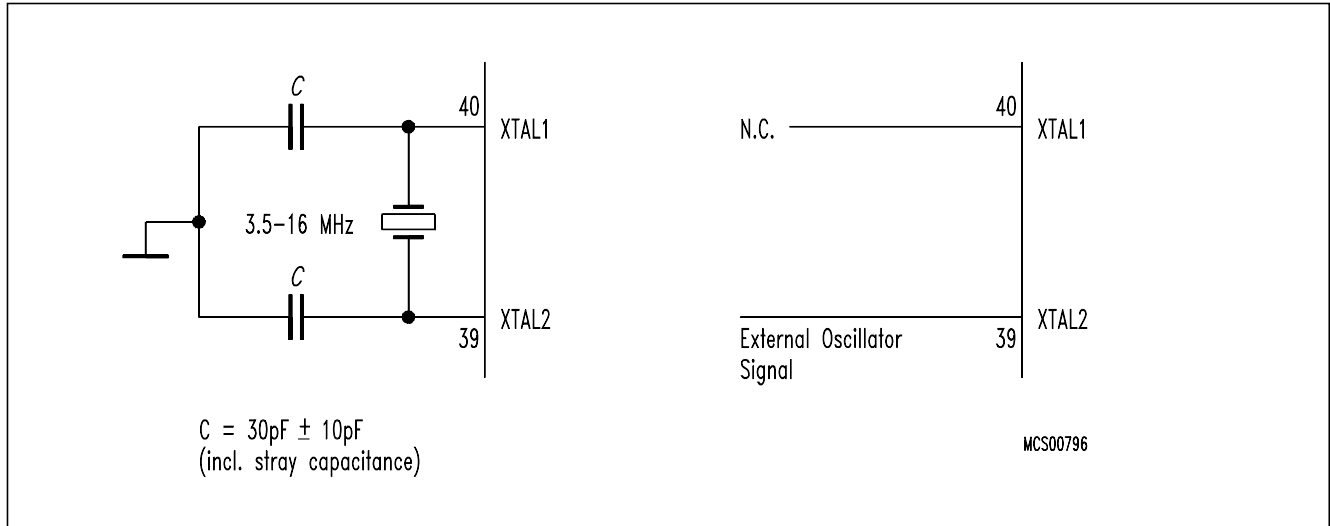
|                         |              |   |                |     |
|-------------------------|--------------|---|----------------|-----|
| Address to valid data   | $t_{AVQV}$   | — | $48\ t_{CLCL}$ | ns  |
| ENABLE to valid data    | $t_{ELQV}$   | — | $48\ t_{CLCL}$ | ns  |
| Data float after ENABLE | $t_{EHQZ}$   | 0 | $48\ t_{CLCL}$ | ns  |
| Oscillator frequency    | $1/t_{CLCL}$ | 4 | 6              | MHz |



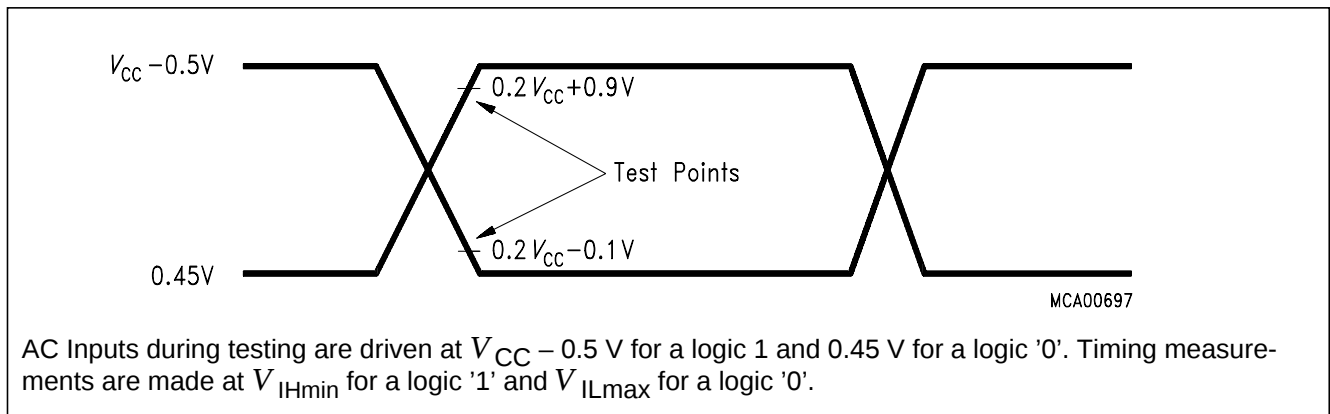
ROM Verification

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20\text{ mA}$ .

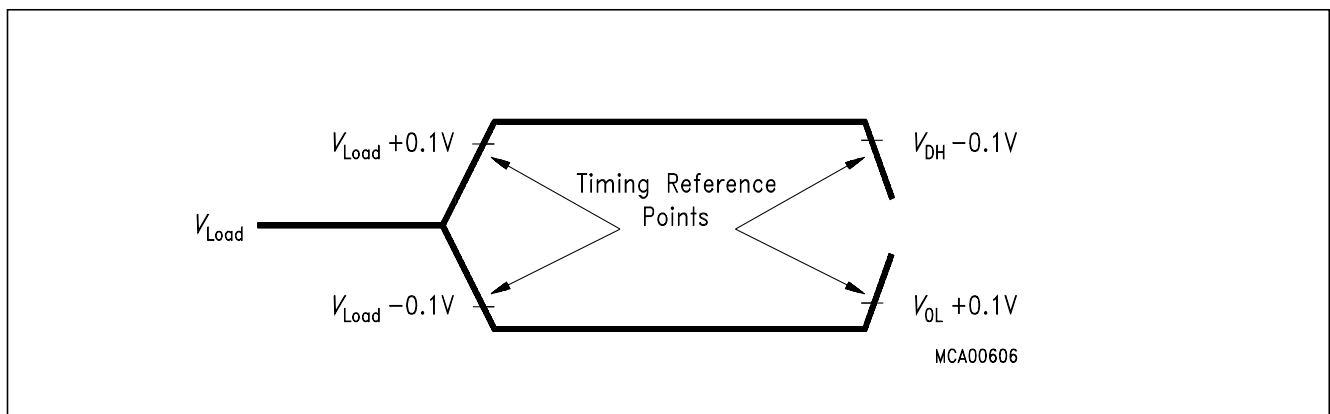
## Recommended Oscillator Circuits



## AC Testing



## Input, Output Waveforms



## Float Waveforms