M58LSW32A
M58LSW32B

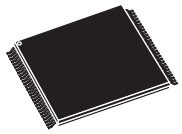
32 Mbit (2Mb x16 or 1Mb x32, Uniform Block) 3V Supply Flash Memories

PRELIMINARY DATA

FEATURES SUMMARY

- WIDE x16/x32 DATA BUS for HIGH BANDWIDTH
  - M58LSW32A x16 DATA BITS
  - M58LSW32B x16/x32 DATA BITS
- SUPPLY VOLTAGE
  - V_{DD} = 2.7 to 3.6V core supply voltage for Program, Erase and Read operations
  - V_{DDQ} = 1.8 to V_{DD} for I/O Buffers
- SYNCHRONOUS/ASYNCHRONOUS READ
  - Synchronous Burst read (x16)
  - Pipelined Synchronous Burst Read (x16)
  - Asynchronous Random Read (x16/x32)
  - Asynchronous Address Latch Controlled Read (x16/x32)
  - Page Read (x16)
- ACCESS TIME
  - Synchronous Burst Read up to 66MHz
  - Asynchronous Page Mode Read 120/25ns, 150/25ns
  - Random Read 120ns, 150ns
- PROGRAMMING TIME
  - 8 Word or 4 Double-Word Write Buffer
  - 24µs Word effective programming time
- 64 UNIFORM 32 KWord MEMORY BLOCKS
- BLOCK PROTECTION/ UNPROTECTION
- PROGRAM and ERASE SUSPEND
- OTP SECURITY AREA
- COMMON FLASH INTERFACE
- 10,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code M58LSW32A: 16h
  - Device Code M58LSW32B: 15h

Figure 1. Packages



TSOP56 (N)
14 x 20 mm

TBGA64 (ZA)
8x8 ball array

TBGA80 (ZA)
8x10 ball array

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M58LSW32 is a 32 Mbit (2Mb x16 or 1Mb x32) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7V to 3.6V) core supply. On power-up the memory defaults to Read mode with an asynchronous bus where it can be read in the same way as a non-burst Flash memory.

The memory is divided into 64 blocks of 512Kbit that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The Write Buffer allows the microprocessor to program from 1 to 8 Words (or from 1 to 4 Double Words) in parallel, both speeding up the programming and freeing up the microprocessor to perform other work.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 10,000 cycles.

Individual block protection against Program or Erase is provided for data security. All blocks are protected during power-up. The protection of the blocks is non-volatile; after power-up the protection status of each block is restored to the state when power was last removed. Software commands are provided to allow protection of some or all of the blocks and to cancel all block protection bits simultaneously. All Program or Erase operations are blocked when the Program Erase Enable input Vpp is low.

The Reset/Power-Down pin is used to apply a Hardware Reset to the memory and to set the device in deep power-down mode. It can also be used to temporarily disable the protection mechanism.

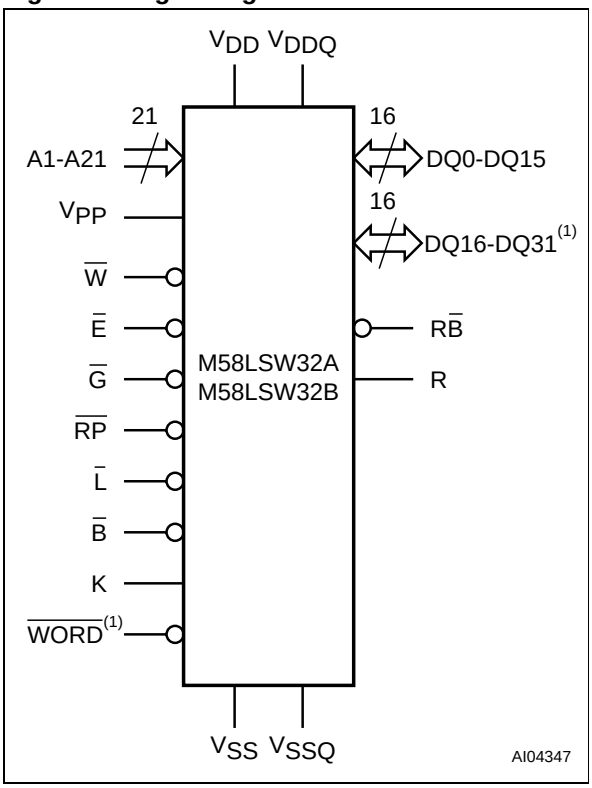
In asynchronous mode Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. An Address Latch input can be used to latch addresses in Latch Controlled mode. Together they allow simple, yet powerful, connection to most microprocessors, often without additional logic.

In synchronous mode all Bus Read operations are synchronous with the Clock. Chip Enable and Output Enable select the Bus Read operation; the address is Latched using the Latch Enable inputs and the address is advanced using Burst Address Advance. The signals are compatible with most microprocessor burst interfaces.

A One Time Programmable (OTP) area is included for security purposes. Either 2K Words (x16 Bus Width) or 1K Double-Words (x32 Bus Width) is available in the OTP area. The process of reading from and writing to the OTP area is not published for security purposes; contact STMicroelectronics for details on how to use the OTP area.

The memory is offered in various packages. The M58LSW32A is available in TSOP56 (14 x 20 mm) and TBGA64 (1mm pitch). The M58LSW32B is available in TBGA80 (1mm pitch).

Figure 2. Logic Diagram



Note: 1. M58LSW32B only.

Table 1. Signal Names

A1	Address Input (x16 Bus Width only)
A2-A21	Address inputs
DQ0-DQ15	Data Inputs/Outputs
DQ16-DQ31	Data Inputs/Outputs (x32 Bus Width of M58LSW32B only)
$\overline{B}$	Burst Address Advance
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
K	Clock
$\overline{L}$	Latch Enable
R	Valid Data Ready
$R\overline{B}$	Ready/Busy
$\overline{RP}$	Reset/Power-Down
V_{PP}	Program/Erase Enable
$\overline{W}$	Write Enable
$\overline{WORD}$	Word Organization (M58LSW32B only)
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally

Figure 3. TSOP56 Connections

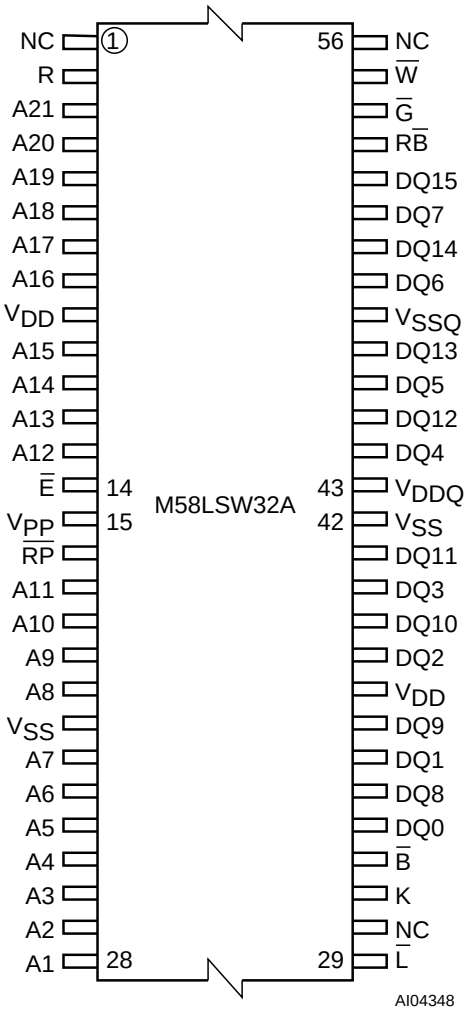


Figure 4. TBGA64 Connections for M58LSW32A (Top view through package)

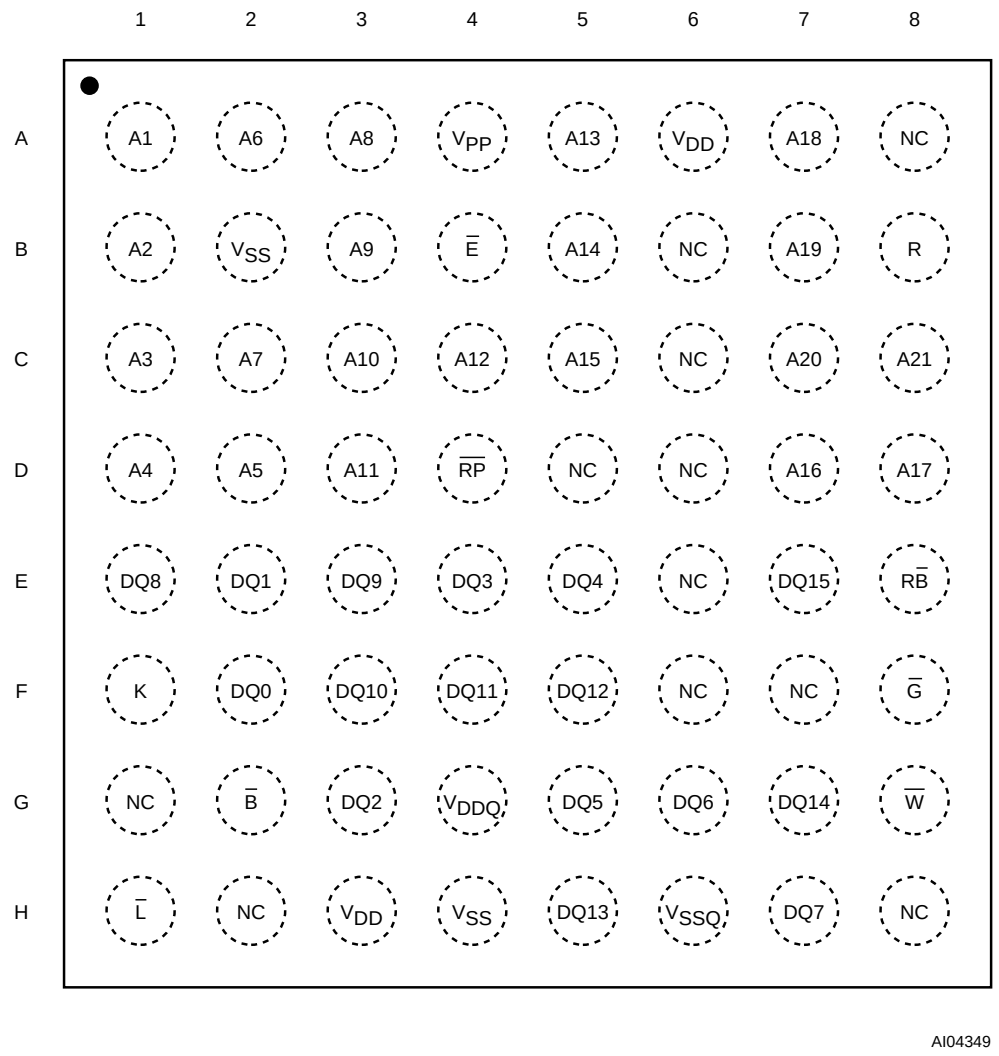


Figure 5. TBGA80 Connections for M58LSW32B (Top view through package)

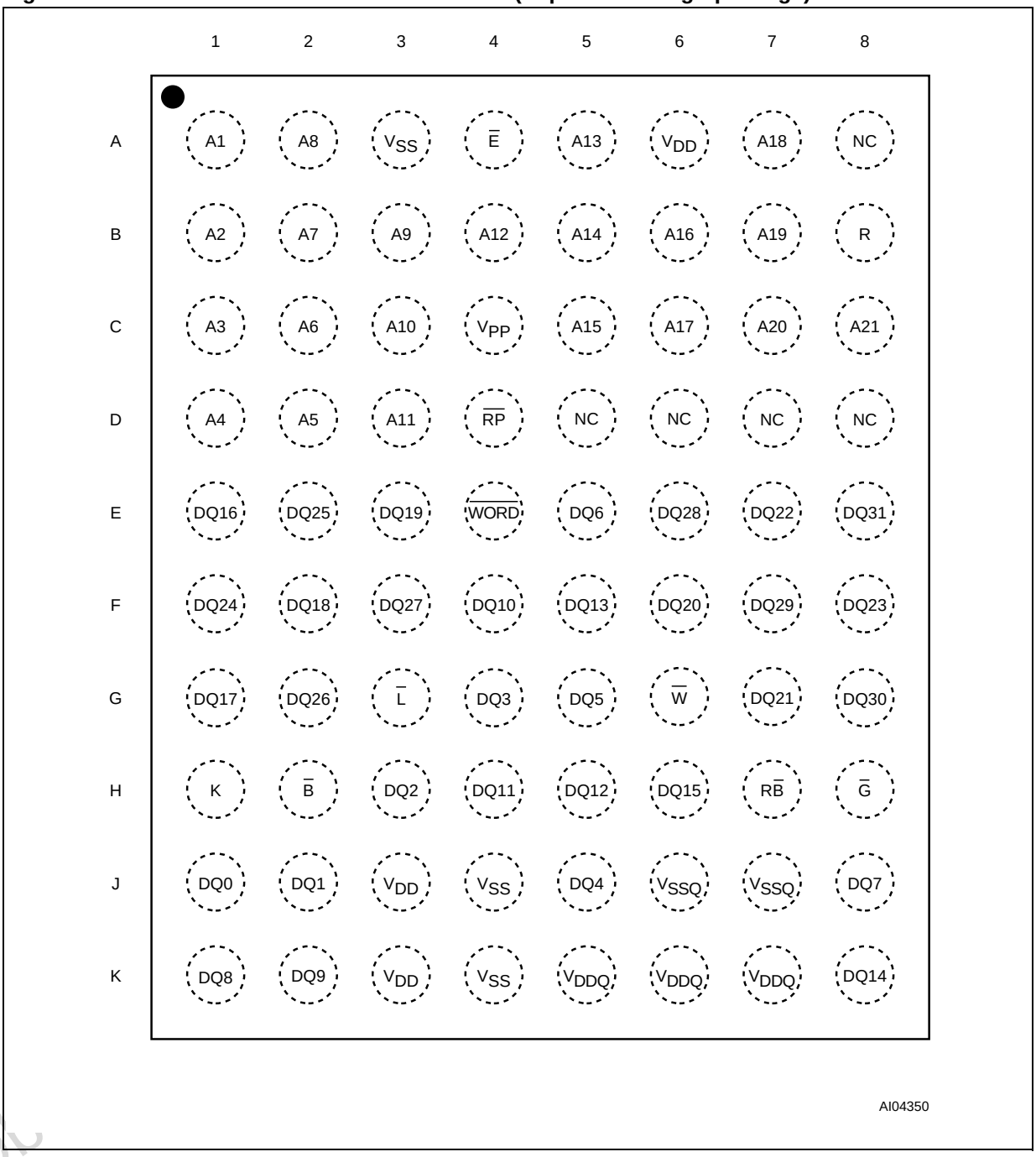
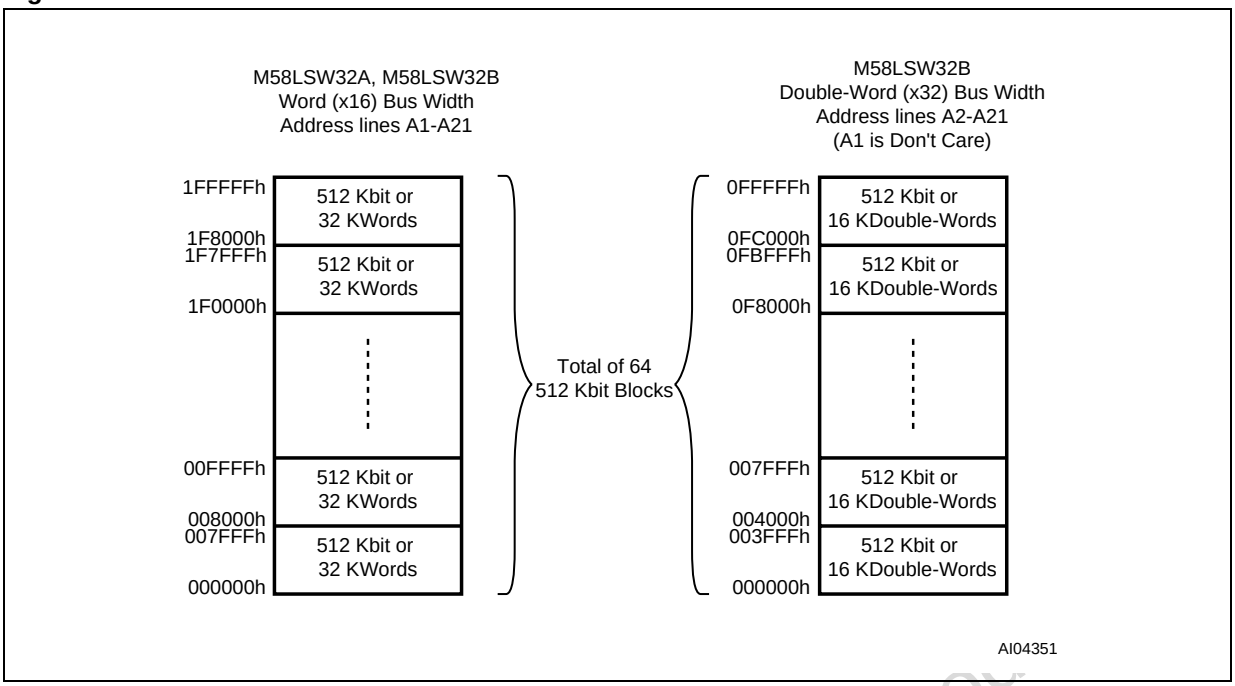


Figure 6. Block Addresses



Note: Also see Appendix A, Table 28 for a full listing of the Block Addresses

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A1-A21). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. Chip Enable must be low when selecting the addresses.

The address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a Write operation. The address latch is transparent when Latch Enable is low, V_{IL}. The address is internally latched in an Erase or Program operation.

With a x32 Bus Width, $\overline{WORD} = V_{IH}$, Address Input A1 is ignored; the Least Significant Word is output on DQ0-DQ15 and the Most Significant Word is output on DQ16-DQ31. With a x16 Bus Width, $\overline{WORD} = V_{IL}$, the Least Significant Word is output on DQ0-DQ15 when A1 is low, V_{IL}, and the Most Significant Word is output on DQ0-DQ15 when A1 is high, V_{IH}.

Data Inputs/Outputs (DQ0-DQ31). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both low, V_{IL}, the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the chip is deselected, Output Enable is low, V_{IL}, or the Reset/Power-Down signal is low, V_{IL}. When the Program/Erase Controller is active the Ready/Busy status is given on DQ7 while DQ0-DQ6 and DQ8-DQ31 are high impedance.

With a x16 Bus Width, $\overline{WORD} = V_{IL}$, DQ16-DQ31 are not used and are high impedance.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the Standby level, I_{DD1}.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation. When Output Enable, $\overline{G}$, is at V_{IH} the outputs are high impedance. Output Enable, $\overline{G}$, can be used to inhibit the data output during a burst read operation.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, $\overline{L}$).

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all blocks that have been protected.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL}, for at least t_{PLPH}. When Reset/Power-Down is Low, V_{IL}, the Status Register information is cleared and the power consumption is reduced to deep power-down level. The device is deselected and outputs are high impedance. If Reset/Power-Down goes low, V_{IL}, during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect the operation is aborted and the data may be corrupted. In this case the Ready/Busy pin stays low, V_{IL}, for a maximum timing of $t_{PLPH} + t_{PHRH}$, until the completion of the Reset/Power-Down pulse.

After Reset/Power-Down goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. Note that Ready/Busy does not fall during a reset, see Ready/Busy Output section.

During power-up Reset/Power-Down must be held Low, V_{IL}. Furthermore it must stay low for t_{VDHPH} after the Supply Voltage inputs become stable. The device will then be configured in Asynchronous Random Read mode.

See Table 22 and Figure 21, Reset, Power-Down and Power-up Characteristics, for more details.

Holding $\overline{RP}$ at V_{HH} will temporarily unprotect the protected blocks in the memory. Program and Erase operations on all blocks will be possible.

In an application, it is recommended to associate Reset/Power-Down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an Erase or Program operation, the memory may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

Latch Enable ($\overline{L}$). The Bus Interface can be configured to latch the Address Inputs on the rising edge of Latch Enable, $\overline{L}$. In synchronous bus operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL}. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent.

Clock (K). The Clock, K, is used to synchronize the memory with the external bus during Synchronous Bus Read operations. The Clock can be configured to have an active rising or falling edge. Bus signals are latched on the active edge of the Clock during synchronous bus operations. In Synchronous Burst Read mode the address is latched on the first active clock edge when Latch Enable is low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During asynchronous bus operations the Clock is not used.

Burst Address Advance ($\overline{B}$). The Burst Address Advance, $\overline{B}$, controls the advancing of the address by the internal address counter during synchronous bus operations.

Burst Address Advance, $\overline{B}$, is only sampled on the active clock edge of the Clock when the X- or Y-latency time has expired. If Burst Address Advance is Low, V_{IL}, the internal address counter advances. If Burst Address Advance is High, V_{IH}, the internal address counter does not change; the same data remains on the Data Inputs/Outputs and Burst Address Advance is not sampled until the Y-latency expires.

The Burst Address Advance, $\overline{B}$, may be tied to V_{IL}.

Valid Data Ready (R). The Valid Data Ready output, R, is an open drain output that can be used to identify if the memory is ready to output data or not. The Valid Data Ready output is only active during Synchronous Burst Read operations when the Burst Length is set to Continuous. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready Low, V_{OL}, indicates that the data is not, or will not be valid. Valid Data Ready in a high-impedance state indicates that valid data is or will be available.

If the memory is configured for Synchronous Burst Read operations with Burst Length set to Continuous then the value of Valid Data Ready, will depend on the starting address. If the starting address is aligned to a four Word boundary then the continuous burst mode will run without activating the Valid Data Ready output. If the starting address is not aligned to a four Word boundary, Valid Data Ready is Low at the beginning of the continuous burst read to indicate that the memory needs an internal delay to read the content of the four successive words in the array.

Unless the Burst Length is set to Continuous and Synchronous Burst Read has been selected, Valid Data Ready is high-impedance. It may be tied to other components with the same Valid Data Ready signal to create a unique System Ready signal.

When the system clock frequency is between 33MHz and 50MHz and the Y latency is set to 2, values of $\overline{B}$ sampled on odd clock cycles, starting from the first read are not considered.

The Valid Data Ready, R, output has an internal pull-up resistor of approximately 1 MΩ powered from V_{DDQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for Valid Data Ready rising.

Word Organization ($\overline{WORD}$). The Word Organization input, $\overline{WORD}$, selects the x16 or x32 Bus Width on the M58LSW32B. The Word Organization input is not available on the M58LSW32A.

When $\overline{WORD}$ is Low, V_{IL}, Word-wide x16 Bus Width is selected; data is read and written to DQ0-DQ15; DQ16-DQ31 are at high impedance and A1 is the LSB of the address bus. When $\overline{WORD}$ is High, V_{IH}, the Double-Word wide x32 Bus Width is selected and the data is read and written to on DQ0-DQ31; A2 is the LSB of the address bus and A1 is don't care.

Ready/Busy ($R\overline{B}$). The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the Program/Erase Controller is currently active. When Ready/Busy is high impedance, the memory is ready for any Read, Program or Erase operation. Ready/Busy is Low, V_{OL}, during Program and Erase operations. When the device is busy it will not accept any additional Program or Erase commands except Program/Erase Suspend. When the Program/Erase Controller is idle, or suspended, Ready Busy can float High through a pull-up resistor.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Ready/Busy is not Low during a reset unless the reset was applied when the Program/Erase Controller was active; Ready/Busy can rise before Reset/Power-Down rises.

Program/Erase Enable (V_{PP}). The Program/Erase Enable input, V_{PP}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.

When Program/Erase Enable is Low, V_{IL}, any Program or Erase operations sent to the command interface will cause the V_{PP} Status bit in the Status Register to be set. When Program/Erase Enable is High, V_{IH}, Program and Erase operations can be performed on unprotected blocks.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. The Supply Voltage, V_{DD}, is the core power supply. All internal circuits draw

their current from the V_{DD} pin, including the Program/Erase Controller.

A 0.1µF capacitor should be connected between the Supply Voltage, V_{DD}, and the Ground, V_{SS}, to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during all operations of the parts, see Table 15, DC Characteristics, for maximum current supply requirements.

Input/Output Supply Voltage (V_{DDQ}). The Input/Output Supply Voltage, V_{DDQ}, is the input/output buffer power supply. All input and output pins and voltage references are powered and measured relative to the Input/Output Supply Voltage pin, V_{DDQ}.

The Input/Output Supply Voltage, V_{DDQ}, must always be equal or less than the V_{DD} Supply Voltage, including during Power-Up.

A 0.1µF capacitor should be connected between the Input/Output Supply Voltage, V_{DDQ}, and the Ground, V_{SSQ}, to decouple the current surges from the power supply. If V_{DDQ} and V_{DD} are connected together then only one decoupling capacitor is required.

Ground (V_{SS}). Ground, V_{SS}, is the reference for all core power supply voltages.

Ground (V_{SSQ}). Ground, V_{SSQ}, is the reference for input/output voltage measurements. It is essential to connect V_{SS} and V_{SSQ} to the same ground.

BUS OPERATIONS

There are 12 bus operations that control the memory. Each of these is described in this section, see Tables 2 and 3, Bus Operations, for a summary. The bus operation is selected through the Burst Configuration Register; the bits in this register are described at the end of this section.

On Power-up or after a Hardware Reset the memory defaults to Asynchronous Bus Read and Asynchronous Bus Write, no other bus operation can be performed until the Burst Control Register has been configured.

Synchronous Read operations and Latch Controlled Bus Read operations can only be used to read the memory array. The Electronic Signature, CFI or Status Register will be read in asynchronous mode regardless of the Burst Control Register settings.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Asynchronous Bus Operations

For asynchronous bus operations refer to Table 3 together with the text below.

Asynchronous Bus Read. Asynchronous Bus Read operations read from the memory cells, or specific registers (Electronic Signature, Status Register, CFI and Block Protection Status) in the Command Interface. A valid bus operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 12, Asynchronous Bus Read AC Waveforms, and Table 16, Asynchronous Bus Read AC Characteristics, for details of when the output becomes valid.

Asynchronous Latch Controlled Bus Read. Asynchronous Latch Controlled Bus Read operations read from the memory cells or specific registers in the Command Interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses. Asynchronous Latch Controlled Bus Read is available for x16 and x32 bus widths.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Address Latch Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Address Latch. Once latched, the Address Inputs can change. Set Output Enable Low, V_{IL}, to read the data on the Data Inputs/Outputs; see Figure 13, Asynchronous Latch Controlled Bus Read AC Waveforms and Table 17, Asynchronous Latch Controlled Bus Read AC Characteristics for details on when the output becomes valid.

Note that, since the Latch Enable input is transparent when set Low, V_{IL}, Asynchronous Bus Read operations can be performed when the memory is configured for Asynchronous Latch Enable bus operations by holding Latch Enable Low, V_{IL} throughout the bus operation.

Asynchronous Page Read. Asynchronous Page Read operations are used to read from several addresses within the same memory page. Each memory page is 2 Words and has the same A2-A21, only A1 may change. Asynchronous Page Read is only available for x16 bus width.

Valid bus operations are the same as Asynchronous Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. See Figure 14, Asynchronous Page Read AC Waveforms and Table 18, Asynchronous Page Read AC Characteristics for details on when the outputs become valid.

Asynchronous Bus Write. Asynchronous Bus Write operations write to the Command Interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Bus Write operation begins by setting the desired address on the Address Inputs and setting Latch Enable Low, V_{IL}. The Address Inputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Asynchronous Bus Write operation. See Figures 15, and 17, Asynchronous Write AC Waveforms, and Tables 19 and 20, Asynchronous Write and Latch Controlled Write AC Characteristics, for details of the timing requirements.

Asynchronous Latch Controlled Bus Write. Asynchronous Latch Controlled Bus Write operations write to the Command Interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Latch Controlled Bus Write operation begins by setting the desired address on the Address Inputs and pulsing Latch Enable Low, V_{IL}. The Address Inputs are latched by the Com-

mand Interface on the rising edge of Latch Enable. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Asynchronous Bus Write operation. See Figures 16 and 18 Asynchronous Latch Controlled Write AC Waveforms, and Tables 19 and 20, Asynchronous Write and Latch Controlled Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when the Output Enable is High.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high impedance state regardless of Output Enable or Write Enable. The Supply Current is reduced to the Standby Supply Current, I_{DD1}.

During Program or Erase operations the memory will continue to use the Program/Erase Supply Current, I_{DD3}, for Program or Erase operations until the operation completes.

Automatic Low Power. If there is no change in the state of the bus for a short period of time during Asynchronous Bus Read operations the memory enters Auto Low Power mode where the internal Supply Current is reduced to the Auto-Standby Supply Current, I_{DD5}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Automatic Low Power is only available in Asynchronous Read modes.

Power-Down. The memory is in Power-Down mode when Reset/Power-Down, $\overline{RP}$, is Low. The power consumption is reduced to the Power-Down level, I_{DD2}, and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Table 2. Asynchronous Bus Operations

Bus Operation	Step	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	M3[2]	$\overline{L}$	A1-A22	DQ0-DQ31
Asynchronous Bus Read		V_{IL}	V_{IL}	V_{IH}	High	0	X	Address	Data Output
Asynchronous Latch Controlled Bus Read	Address Latch	V_{IL}	V_{IL}	V_{IH}	High	1	V_{IL}	Address	High Z
	Read	V_{IL}	V_{IL}	V_{IH}	High	1	V_{IH}	X	Data Output
Asynchronous Page Read		V_{IL}	V_{IL}	V_{IH}	High	0	X	Address	Data Output
Asynchronous Bus Write		V_{IL}	V_{IH}	V_{IL}	High	X	V_{IL}	Address	Data Input
Asynchronous Latch Controlled Bus Write	Address Latch	V_{IL}	V_{IH}	V_{IL}	High	X	V_{IL}	Address	Data Input
Output Disable		V_{IL}	V_{IH}	V_{IH}	High	X	X	X	High Z
Standby		V_{IH}	X	X	High	X	X	X	High Z
Power-Down		X	X	X	V_{IL}	X	X	X	High Z

Note: 1. X = Don't Care V_{IL} or V_{IH}. High = V_{IH} or V_{HH}.
2. M15 = 1, Bits M15 and M3 are in the Burst Configuration Register.

Synchronous Bus Operations

For synchronous bus operations refer to Table 3 together with the text below.

Synchronous Burst Read. Synchronous Burst Read operations are used to read from the memory at specific times synchronized to an external reference clock. The burst type, length and latency can be configured. The different configurations for Synchronous Burst Read operations are described in the Burst Configuration Register section. Synchronous Burst Read is only available for x16 bus width.

A valid Synchronous Burst Read operation begins when the address is set on the Address Inputs, Write Enable is High, V_{IH}, and Chip Enable and Latch Enable are Low, V_{IL}, during the active edge of the Clock. The address is latched on the first active clock edge when Latch Enable is low, or on the rising edge of Latch Enable, whichever occurs first. The data becomes available for output after the X-latency specified in the Burst Control Register has expired. The output buffers are activated by setting Output Enable Low, V_{IL}. See Figure 7 for an example of a Synchronous Burst Read operation.

The Burst Address Advance input and the Y-latency specified in the Burst Control Register determine whether the internal address counter is advanced on the active edge of the Clock. When the internal address counter is advanced the Data Inputs/Outputs change to output the value for the next address.

In Continuous Burst mode (Burst Length Bit M2-M0 is set to '111'), one Burst Read operation can access the entire memory sequentially and wrap at the last address. The Burst Address Advance, $\overline{B}$, must be kept low, V_{IL}, for the appropriate number of clock cycles. If Burst Address Advance, $\overline{B}$, is pulled High, V_{IH}, the Burst Read will be suspended.

In Continuous Burst Mode, if the starting address is not associated with a page (2 Word) boundary the Valid Data Ready, R, output goes Low, V_{IL}, to indicate that the data will not be ready in time and additional wait-states are required. The Valid Data Ready output timing (bit M8) can be changed in the Burst Configuration Register.

The Synchronous Burst Read timing diagrams and AC Characteristics are described in the AC and DC Parameters section. See Figures 19, 20 and Table 21.

Synchronous Pipelined Burst Read. Synchronous Burst Read operations can be overlapped to avoid or reduce the X-latency. Pipelined operations should only be used with Burst Configuration Register bit M9 = 0 (Y-latency setting).

A valid Synchronous Pipelined Burst Read operation occurs during a Synchronous Burst Read operation when the new address is set on the Address Inputs and a Low pulse is applied to Latch Enable. The data for the new address becomes valid after the X-latency specified in the Burst Configuration Register has expired.

For optimum operation the address should be latched on the correct clock cycle. Table 4 gives the clock cycle for each valid X- and Y-latency setting. Only these settings are valid, other settings must not be used. There is always one Y-Latency period where the data is not valid. If the address is latched later than the clock cycle specified in Tables 4 then additional cycles where the data is not valid are inserted. Synchronous Pipelined Burst Read operations should only be performed on Burst Lengths of 4 with a x16 bus width.

Suspending a Pipelined Synchronous Burst Read operation is not recommended.

Synchronous Burst Read Suspend. During a Synchronous Burst Read operation it is possible to suspend the operation, freeing the data bus for other higher priority devices.

A valid Synchronous Burst Read operation is suspended when both Output Enable and Burst Address Advance are High, V_{IH}. The Burst Address Advance going High, V_{IH}, stops the burst counter and the Output Enable going High, V_{IH}, inhibits the data outputs. The Synchronous Burst Read operation can be resumed by setting Output Enable Low. See Figure 7 for an example of a Synchronous Burst Read Suspend operation.

Table 3. Synchronous Burst Read Bus Operations

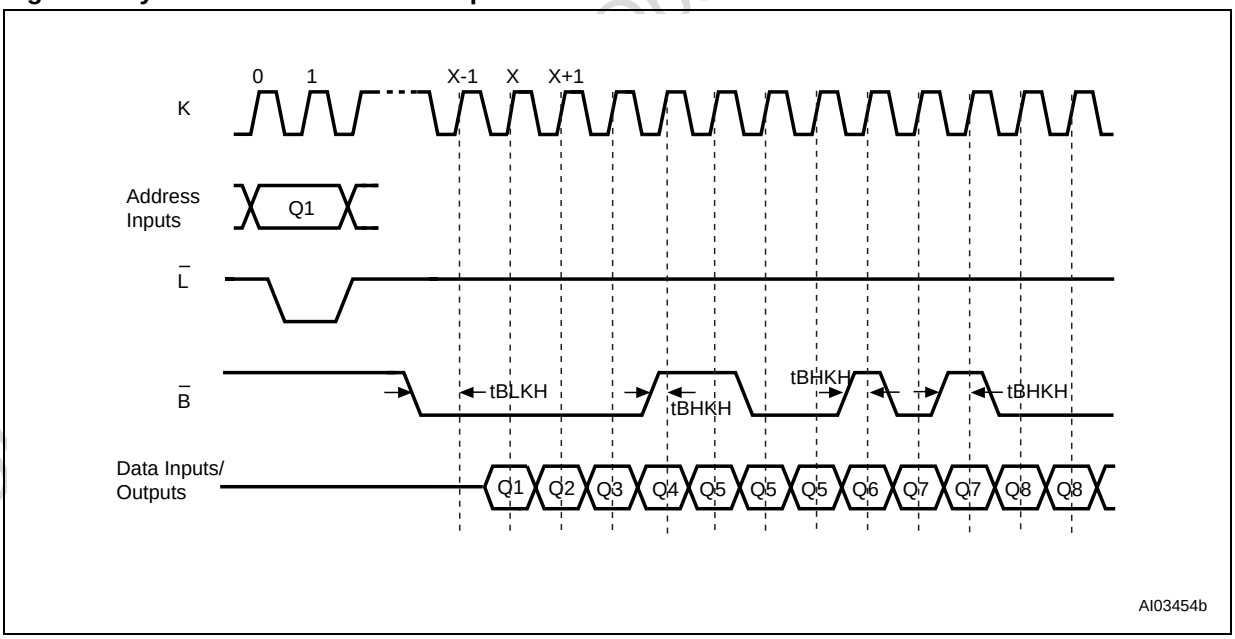
Bus Operation	Step	$\overline{E}$	$\overline{G}$	$\overline{RP}$	K(3)	$\overline{L}$	$\overline{B}$	A1-A21 DQ0-DQ31
Synchronous Burst Read Pipelined Synchronous Burst Read	Address Latch	V_{IL}	X	V_{IH}	T	V_{IL}	X	Address Input
	Read (no address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IH}	Data Output
	Read (with address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IL}	Data Output
	Read Suspend	V_{IL}	V_{IH}	V_{IH}	X	X	V_{IH}	High Z
	Read Resume (no address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IH}	Data Output
	Read Resume (with address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IL}	Data Output
	Read Abort	V_{IH}	X	V_{IH}	X	X	X	High Z

Note: 1. X = Don't Care, V_{IL} or V_{IH}.
2. M15 = 0, Bit M15 is in the Burst Configuration Register.
3. T = transition, see M6 in the Burst Configuration Register for details on the active edge of K.

Table 4. Address Latch Cycle for Optimum Pipelined Synchronous Burst Read

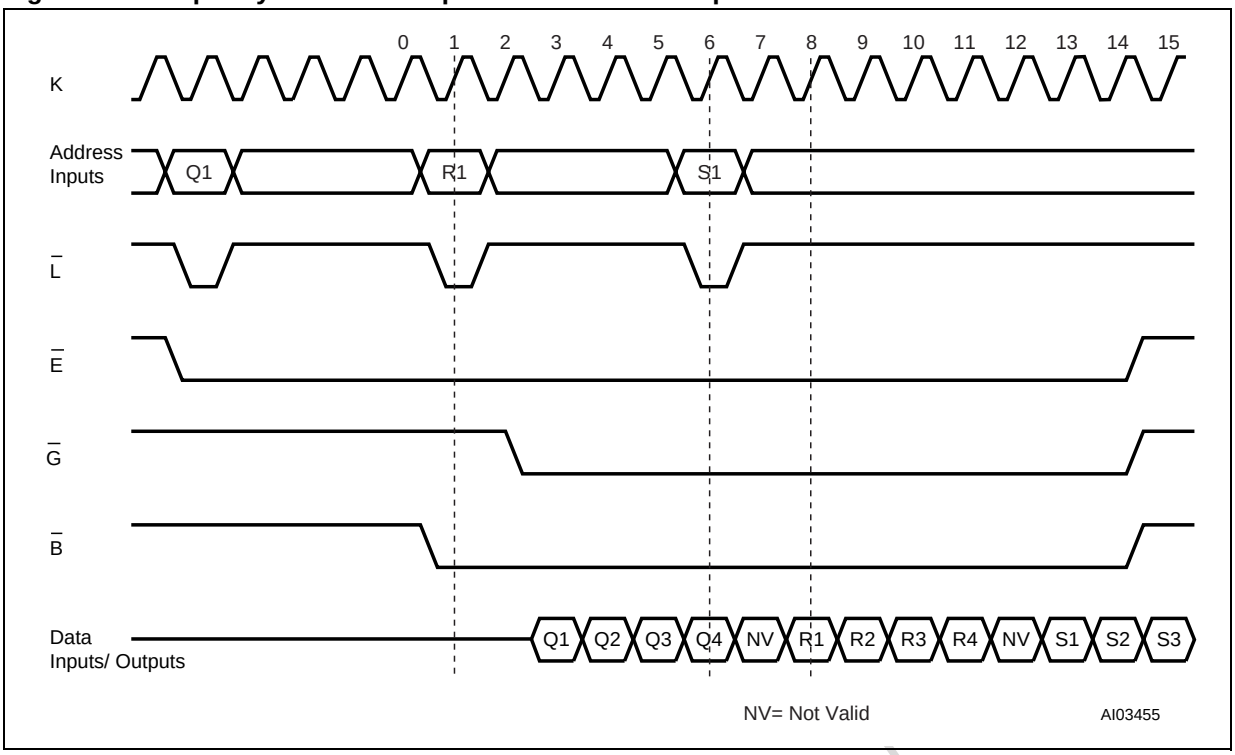
X-Latency	Y-Latency	Address Latch Clock Cycle
		Burst Length = 4
8	1	6
9	1	7
15	2	11

Figure 7. Synchronous Burst Read Operation



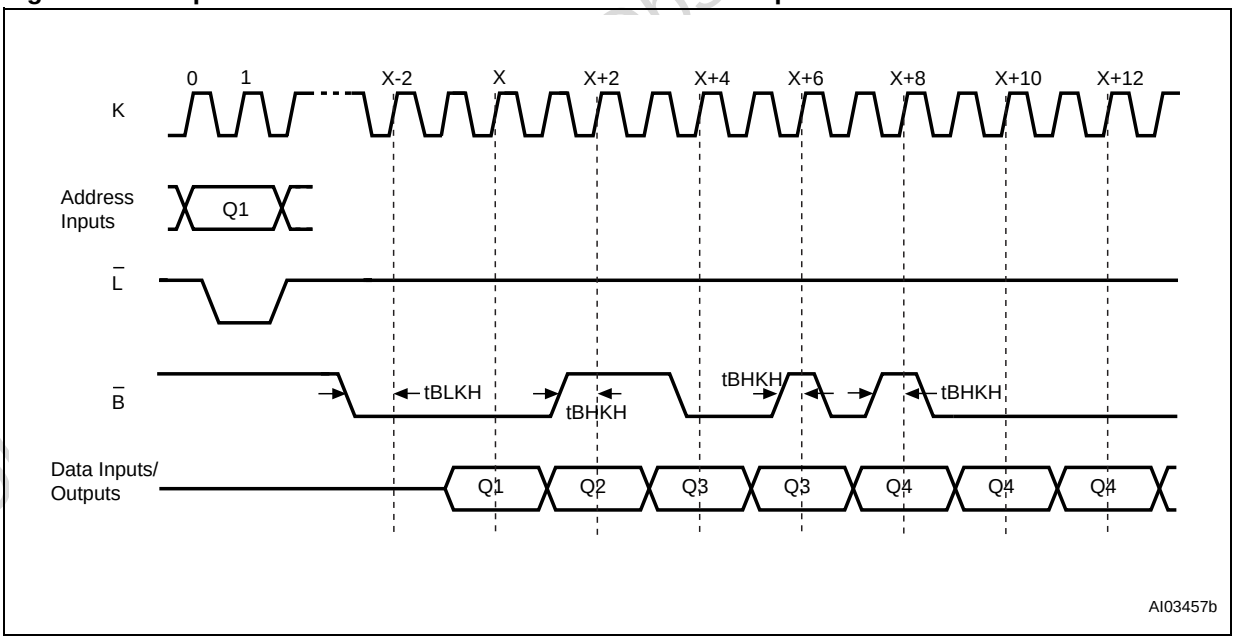
Note: In this example the Burst Configuration Register is set with M2-M0 = 001 (Burst Length = 4 Words), M6 = 1 (Valid Clock Edge = Rising Clock Edge), M7 = 0 or 1 (Burst Type = Interleaved or Sequential), M9 = 0 (Y-Latency = 1), M14-M11 = 0011 (X-Latency = 8) and M15 = 0 (Read Select = Synchronous Burst Read), other bits are don't care.

Figure 8. Example Synchronous Pipelined Burst Read Operation



Note: In this example the Burst Configuration Register is set with M2-M0 = 001 (Burst Length = 4 Words or Double Words), M6 = 1 (Valid Clock Edge = Rising Clock Edge), M7 = 0 or 1 (Burst Type = Interleaved or Sequential), M9 = 0 (Y-Latency = 1), M14-M11 = 0011 (X-Latency = 8) and M15 = 0 (Read Select = Synchronous Burst Read), other bits are don't care.

Figure 9. Example Burst Address Advance and Burst Abort operations



Note: 1. In this example the Burst Configuration Register is set with M2-M0 = 001 (Burst Length = 4 Words), M6 = 1 (Valid Clock Edge = Rising Clock Edge), M7 = 0 or 1 (Burst Type = Interleaved or Sequential), M9 = 1 (Y-Latency = 2), M14-M11 = 0011 (X-Latency = 8) and M15 = 0 (Read Select = Synchronous Burst Read), other bits are don't care.
2. When the system clock frequency is between 33MHz and 50MHz and the Y latency is set to 2, values of $\overline{B}$ sampled on odd clock cycles, starting from the first read are not considered.

Burst Configuration Register

The Burst Configuration Register is used to configure the type of bus access that the memory will perform.

The Burst Configuration Register is set through the Command Interface and will retain its information until it is re-configured, the device is reset, or the device goes into Reset/Power-Down mode. The Burst Configuration Register bits are described in Table 5. They specify the selection of the burst length, burst type, burst X and Y latencies and the Read operation.

Read Select Bit (M15). The Read Select bit, M15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to '1', Bus Read operations are asynchronous; when the Read Select but is set to '0', Bus Read operations are synchronous.

On reset or power-up the Read Select bit is set to'1' for asynchronous accesses.

X-Latency Bits (M14-M11). The X-Latency bits are used during Synchronous Bus Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in Table 5, Burst Configuration Register. The X-Latency bits should also be selected in conjunction with Table 7, Burst Performance to ensure valid settings.

Y-Latency Bit (M9). The Y-Latency bit is used during Synchronous Bus Read operations to set the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in M9.

When the Y-Latency is 1 the data changes each clock cycle; when the Y-Latency is 2 the data changes every second clock cycle. See Table 5, Burst Configuration Register and Table 7, Burst Performance, for valid combinations of the Y-Latency, the X-Latency and the Clock frequency.

Valid Data Ready Bit (M8). The Valid Data Ready bit controls the timing of the Valid Data Ready output pin, R. When the Valid Data Ready bit is '0' the Valid Data Ready output pin is driven Low for the active clock edge when invalid data is output on the bus. When the Valid Data Ready bit is '1' the Valid Data Ready output pin is driven Low one clock cycle prior to invalid data being output on the bus.

Burst Type Bit (M7). The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' the memory outputs from sequential addresses. See Table 6, Burst Type Definition, for the sequence of addresses output from a given starting address.

Valid Clock Edge Bit (M6). The Valid Clock Edge bit, M6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

Latch Enable Bit (M3). The Latch Enable bit is used to select between Asynchronous Random Read and Asynchronous Latch Enable Controlled Read. When the Latch Enable bit is set to '0' Random read is selected; when it is set to '1' Latch Enable Controlled Read is selected. To enable these Asynchronous Read configurations M15 must be set to '1'.

Burst Length Bit (M2-M0). The Burst Length bits set the maximum number of Words or Double-Words that can be output during a Synchronous Burst Read operation before the address wraps.

Table 5, Burst Configuration Register gives the valid combinations of the Burst Length bits that the memory accepts; Table 6, Burst Type Definition, gives the sequence of addresses output from a given starting address for each length.

M10, M5 and M4 are reserved for future use.

Table 5. Burst Configuration Register (x16 Bus Width)

Address Bit	Mnemonic	Bit Name	Reset Value	Value	Description
16	M15	Read Select	1	0	Synchronous Burst Read
				1	Asynchronous Bus Read
15 to 12	M14-M11	X-Latency	XXXX	0010	X-Latency = 7, use only with Continuous Burst Length
				0011	X-Latency = 8
				0100	X-Latency = 9
				1011	X-Latency = 14, use only with Continuous Burst Length
				1101	X-Latency = 15
				Others	Reserved, Do Not Use.
10	M9	Y-Latency	X	0	When X-Latency < 13, Y-Latency = 1 When X-Latency ≥ 13, Y-Latency = 2
				1	When X-Latency < 13, Y-Latency = 2 When X-Latency ≥ 13, do not use.
9	M8	Valid Data Ready	X	0	R valid Low during valid Clock edge
				1	R valid Low one cycle before valid Clock edge
8	M7	Burst Type	X	0	Interleaved
				1	Sequential
7	M6	Valid Clock Edge	X	0	Falling Clock edge
				1	Rising Clock edge
5	M3	Latch Enable	0	0	Random Read
				1	Latch Enable Controlled Read
3 to 1	M2-M0	Burst Length	XXX	100	1 Word
				101	2 Words
				001	4 Words
				111	Continuous
				Others	Reserved, Do Not Use.

Table 6. Burst Type Definition (x16 Bus Width)

Burst Length	Starting Address (binary)	Sequential (decimal)	Interleaved (decimal)
	A2 A1		
2	X0	0, 1	0, 1
	X1	1, 0	1, 0
4	00	0, 1, 2, 3	0, 1, 2, 3
	01	1, 2, 3, 0	1, 0, 3, 2
	10	2, 3, 0, 1	2, 3, 0, 1
	11	3, 0, 1, 2	3, 2, 1, 0
Continuous	A	A, A+1, A+2...	Not Valid

Note: X = 0 or 1.

Table 7. Burst Performance

Clock Frequency	Continuous Burst Length		Other Burst Length	
	X-Latency	Y-Latency	X-Latency	Y-Latency
≤33 MHz	≥ 7	1 or 2	≥ 8	1 or 2
33 MHz ≤ f ≤66 MHz	≥ 13	2	15	2

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. The Commands are summarized in Table 8, Commands. Refer to Table 8 in conjunction with the text descriptions below.

After power-up or a Reset operation the memory enters Read mode.

Synchronous Read operations and Latch Controlled Bus Read operations can only be used to read the memory array. The Electronic Signature, CFI or Status Register will be read in asynchronous mode regardless of the Burst Control Register settings. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Burst Configuration Register automatically.

Read Memory Array Command. The Read Memory Array command returns the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read commands will access the memory array.

While the Program/Erase Controller is executing a Program, Erase, Block Protect or Blocks Unprotect operation the memory will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code or the Block Protection Status until another command is issued; see Table 9, Read Electronic Signature.

Read Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Tables 29, 30, 31, 32, 33 and 34 for details on the information contained in the Common Flash Interface (CFI) memory area.

Note that the addresses for the Common Flash Interface Memory Area are A1-A21 for the M58LSW32A and A2-A21 for the M58LSW32B, regardless of the bus width selected.

Read Status Register Command. The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ1-DQ7) when both Chip Enable and Output Enable are low, V_{IL}. In Synchronous Burst mode the Status Register information is output on the active clock edge when Latch Enable is low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

See the section on the Status Register and Table 11 for details on the definitions of the Status Register bits

Clear Status Register Command. The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent Bus Read operations continue to output the same data.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Write to Buffer and Program, Erase, Block Protect or Block Unprotect command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Erase times are given in Table 10.

See Appendix C, Figure 27, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Block Erase command.

Write to Buffer and Program Command. The Write to Buffer and Program command is used to program the memory array. Up to 8 Words (or 4

Double Words) can be loaded into the Write Buffer and programmed into the memory. Each Word has the same A5-A21.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words (x16 Bus Width) or Double Words (x32 Bus Width) to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word or Double Word into the Write Buffer. See the constraints on the address combinations listed below. The addresses must have the same A5-A21.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command or by using the Blocks Temporary Unprotect feature of the Reset/ Power-Down pin, $\overline{RP}$.

See Appendix C, Figure 25, Write to Buffer and Program Flowchart and Pseudo Code, for a suggested flowchart on using the Write to Buffer and Program command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Write to Buffer and Program or Erase operation. The command will only be accepted during a Program or an Erase operation. It can be issued at any time during an Erase operation but will only be accepted during a Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (bit 7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/ Erase Controller has paused. After the Program/ Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/ Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (bit 7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (bit 2) or the Erase Suspend Status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 10.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Write to Buffer and Program, and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See Appendix C, Figure 26, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 28, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Set Burst Configuration Register Command.

The Set Burst Configuration Register command is used to write a new value to the Burst Configuration Control Register which defines the burst length, type, X and Y latencies, Synchronous/ Asynchronous Read mode and the valid Clock edge configuration.

One Bus Write cycle is required to issue the Set Burst Configuration Register command. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Burst Configuration Register is always presented on A2-A17, regardless of the bus width that is selected. M0 is on A2, M1 on A3, etc.; the other address bits are ignored.

Block Protect Command. The Block Protect command is used to protect a block and prevent Program or Erase operations from changing the data in it. Two Bus Write cycles are required to issue the Block Protect command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

The Block Protection bits are non-volatile, once set they remain set through reset and power-down/power-up. They are cleared by a Blocks Unprotect command or temporary disabled by raising the Reset/Power-Down pin to V_{HH} and holding it at that level throughout a Block Erase or Write to Buffer and Program command.

Blocks Unprotect Command. The Blocks Unprotect command is used to unprotect all of the blocks. Two Bus Write cycles are required to issue the Blocks Unprotect command; the second Bus Write cycle starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

Table 8. Commands

Command	Cycles	Bus Write Operations							
		1st		2nd		Subsequent		Final	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read Memory Array	1	X	FFh						
Read Electronic Signature	1	X	90h						
Read Query	1	X	98h						
Read Status Register	1	X	70h						
Clear Status Register	1	X	50h						
Block Erase	2	X	20h	BA	D0h				
Write to Buffer and Program	4 + N	BA	E8h	BA	N	PA	PD	X	D0h
Program/Erase Suspend	1	X	B0h						
Program/Erase Resume	1	X	D0h						
Set Burst Configuration Register	2	BCR	60h	BCR	03h				
Block Protect	2	BA	60h	BA	01h				
Blocks Unprotect	2	X	60h	X	D0h				

Note: X Don't Care; PA Program Address; PD Program Data; BA Any address in the Block; N+1 Number of Addresses to Program; BCR Burst Configuration Register value.

Table 9. Read Electronic Signature

Code	Address (A21-A1, x16 Bus Width)	Address (A21-A2, x32 Bus Width)	Data (DQ31-DQ8)	Data (DQ7-DQ0)
Manufacturer Code	000000h	000000h	000000h	20h
Device Code	000001h	000001h	000000h	16h (M58LSW32A) 15h (M58LSW32B)
Block Protection Status(1)	BA OR 02h	BA OR 02h	000000h	00h (Block Unprotected) 01h (Block Protected)

Note: BA is any address in the block. Use the Logical OR operator to ensure that the two LSBs of the address are '1'.

Table 10. Program, Erase Times and Program Erase Endurance Cycles

Parameters	M58LSW32A/B				Unit
	Min	Typ	Typical after 10k W/E Cycles	Max	
Block (512 Kbit) Erase		0.75	0.75	5	s
Chip Program		54	54		s
Program Write Buffer		192	192		µs
Program Suspend Latency Time		3		10	µs
Erase Suspend Latency Time		10		30	µs
Block Protect Time		192			µs
Blocks Unprotect Time		0.75			s
Program/Erase Cycles (per Block)	10,000				cycles

Note: (T_A = 0 to 70°C; V_{DD} = 2.7V to 3.6V; V_{DDQ} =1.8V)

STATUS REGISTER

The Status Register provides information on the current or previous Program, Erase, Block Protect or Blocks Unprotect operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Blocks Unprotect and Program/Erase Resume commands. The Status Register can be read from any address.

The Status Register can only be read using Asynchronous Bus Read operations. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Burst Configuration Register automatically.

The contents of the Status Register can be updated during an Erase or Program operation by toggling the Output Enable pin or by dis-activating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}) the device.

The Status Register bits are summarized in Table 11, Status Register Bits. Refer to Table 11 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low, V_{OL}, the Program/Erase Controller is active; when the bit is High, V_{OH}, the Program/Erase Controller is inactive.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, Block Protect and Blocks Unprotect operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly or that all blocks have been unprotected successfully. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Erase Status bit is Low, V_{OL}, the memory has successfully verified that the block has erased correctly or all blocks have been unprotected successfully. When the Erase Status bit is High, V_{OH}, the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly or that all the blocks have been unprotected successfully.

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program or Block Protect failure. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Status bit is Low, V_{OL}, the memory has successfully verified that the Write Buffer has programmed correctly or the block is protected. When the Program Status bit is High, V_{OH}, the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the Write Buffer has programmed correctly or that the Block is protected.

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3). The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program, Erase, Block Protect and Blocks Unprotect operations. The V_{PP} pin is only sampled at the beginning of a Program, Erase Block Protect or Blocks Unprotect operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low, V_{OL}, the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is High, V_{OH}, the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected; Program Erase, Block Protect and Blocks Unprotect operation cannot be performed.

Once set High, the V_{PP} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program, Erase, Block Protect or Blocks Unprotect command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/ Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is Low, V_{OL}, no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is High, V_{IH}, a Program or Erase operation has been attempted on a protected block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value should be masked.

Table 11. Status Register Bits

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	$R\overline{B}$
Program/Erase Controller Active	'0'	Not Valid						V_{OL}
Write Buffer not ready	'0'	Not Valid						V_{OL}
Write Buffer ready	'1'	X(1)	'0'	'0'	'0'	'0'	'0'	Hi-Z
Program suspended	'1'	X(1)	'0'	'0'	'0'	'1'	'0'	Hi-Z
Program/Block Protect completed successfully	'1'	X(1)	'0'	'0'	'0'	'0'	'0'	Hi-Z
Program/Block Protect failure due to incorrect command sequence	'1'	X(1)	'1'	'1'	'0'	'0'	'0'	Hi-Z
Program/Block Protect failure due to V_{PP} Error	'1'	X(1)	'0'	'1'	'1'	'0'	'0'	Hi-Z
Program failure due to Block Protection	'1'	X(1)	'0'	'1'	'0'	'0'	'1'	Hi-Z
Program/Block Protect failure due cell failure or unerased cell	'1'	X(1)	'0'	'1'	'0'	'0'	'0'	Hi-Z
Erase suspended	'1'	'1'	'0'	'0'	'0'	'0'	'0'	Hi-Z
Erase/Blocks Unprotect completed successfully	'1'	'0'	'0'	'0'	'0'	'0'	'0'	Hi-Z
Erase/Blocks Unprotect failure due to V_{PP} Error	'1'	'0'	'0'	'1'	'1'	'0'	'0'	Hi-Z
Erase failure due to Block Protection	'1'	'0'	'0'	'0'	'1'	'0'	'1'	Hi-Z
Erase/Blocks Unprotect failure due to failed cell(s) in block	'1'	'0'	'1'	'0'	'0'	'0'	'0'	Hi-Z

Note: 1. For Program operations during Erase Suspend Bit 6 is '1', otherwise Bit 6 is '0'.

MAXIMUM RATING

Stressing the device above the ratings listed in Table 12, Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	150	°C
T_{LEAD}	Maximum TLEAD Temperature during soldering		t.b.a.	°C
V_{IO}	Input or Output Voltage	–0.6	V_{DDQ} +0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6	5.0	V
V_{HH}	$\overline{RP}$ Hardware Block Unlock Voltage	–0.6	10 (1)	V

Note: 1. Cumulative time at a high voltage level of 10V should not exceed 80 hours on $\overline{RP}$ pin.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 13, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating and AC Measurement Conditions

Parameter		M58LSW32				Units
		120		150		
		Min	Max	Min	Max	
Supply Voltage (V_{DD})		2.7	3.6	2.7	3.6	V
Input/Output Supply Voltage (V_{DDQ})		1.8	V_{DD}	1.8	V_{DD}	V
Ambient Temperature (T_A)	Grade 1	0	70	0	70	°C
	Grade 6	–40	85	–40	85	°C
Load Capacitance (C_L)		30		30		pF
Clock Rise and Fall Times			3		3	ns
Input Rise and Fall Times			4		4	ns
Input Pulses Voltages		0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages		0.5 V_{DDQ}		0.5 V_{DDQ}		V

Figure 10. AC Measurement Input Output Waveform

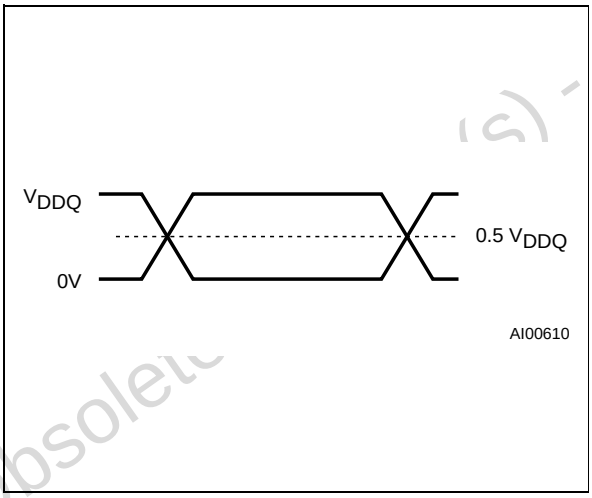


Figure 11. AC Measurement Load Circuit

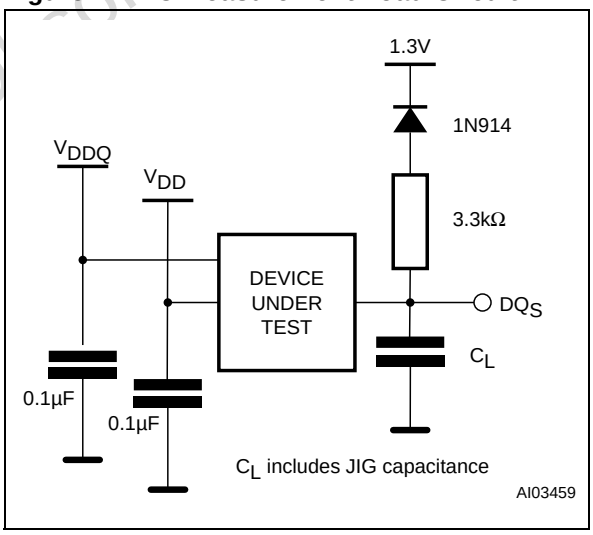


Table 14. Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

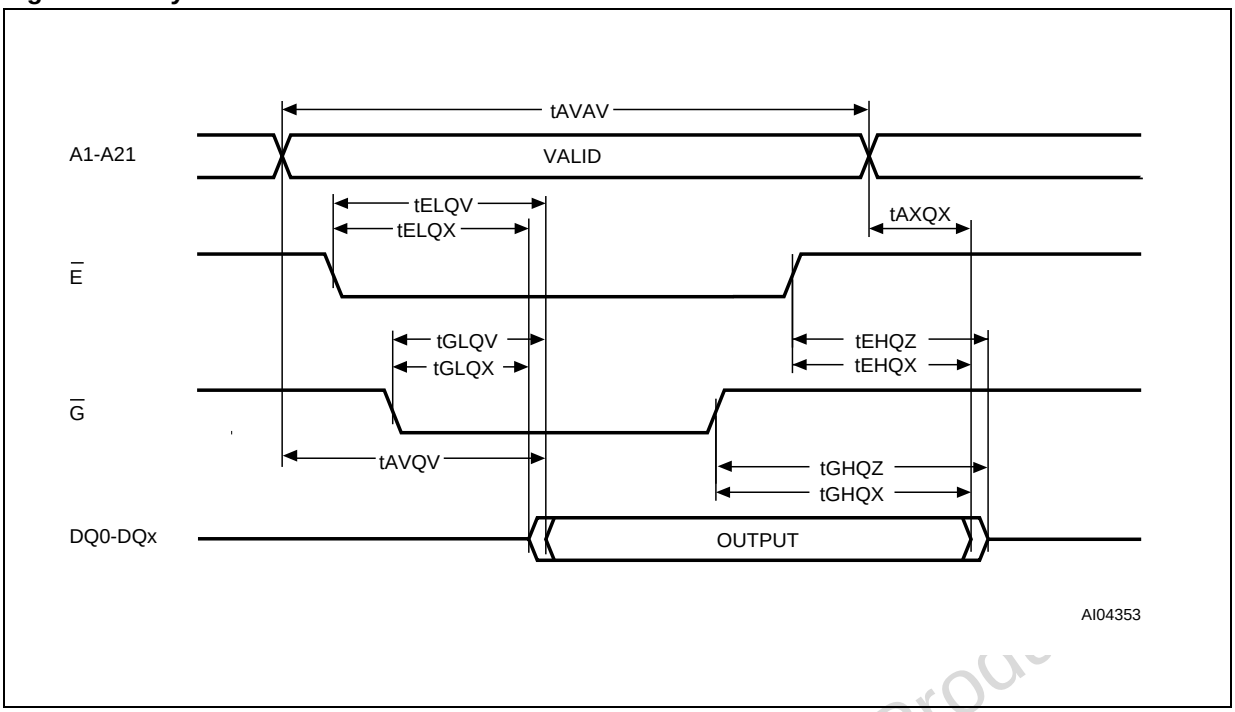
Note: 1. T_A = 25°C, f = 1 MHz
2. Sampled only, not 100% tested.

Table 15. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$		±5	µA
I_{DD}	Supply Current (Random Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{add} = 6MHz		30	mA
I_{DDB}	Supply Current (Burst Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{clock} = 50MHz		50	mA
I_{DD1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		40	µA
I_{DD5}	Supply Current (Auto Low-Power)	$\overline{E} = V_{IL}$, $\overline{RP} = V_{IH}$		2	mA
I_{DD2}	Supply Current (Reset/Power-Down)	$\overline{RP} = V_{IL}$		1	µA
I_{DD3}	Supply Current (Program or Erase, Set Lock Bit, Erase Lock Bit)	Program or Erase operation in progress		50	mA
I_{DD4}	Supply Current (Erase/Program Suspend)	$\overline{E} = V_{IH}$		50	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		V_{DDQ} –0.8	V_{DDQ} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.1		V
V_{HH} (1)	$\overline{RP}$ Hardware Block Unprotect Voltage	Block Erase in progress, Write to Buffer and Program	8.5	9.5	V
I_{HH}	$\overline{RP}$ Hardware Block Unprotect Current	$\overline{RP} = V_{HH}$		1	µA
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)			2.2	V

Note: 1. Biasing $\overline{RP}$ pin to V_{HH} is allowed for a maximum cumulative period of 80 hours.

Figure 12. Asynchronous Bus Read AC Waveforms

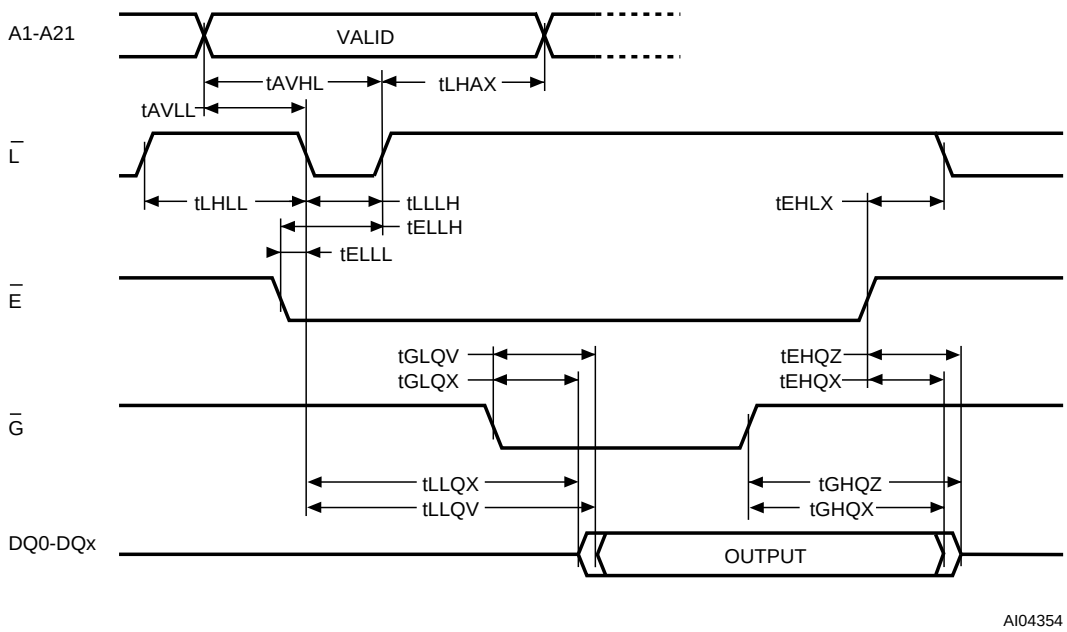


Note: Asynchronous Read (M15 = 1), Random Read (M3 = 0)

Table 16. Asynchronous Bus Read AC Characteristics.

Symbol	Parameter	Test Condition		M58LSW32		Unit
				120	150	
t_{AVAV}	Address Valid to Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	120	150	ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	120	150	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	120	150	ns
t_{GLQX}	Output Enable to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	50	50	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	10	10	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	10	10	ns

Figure 13. Asynchronous Latch Controlled Bus Read AC Waveforms



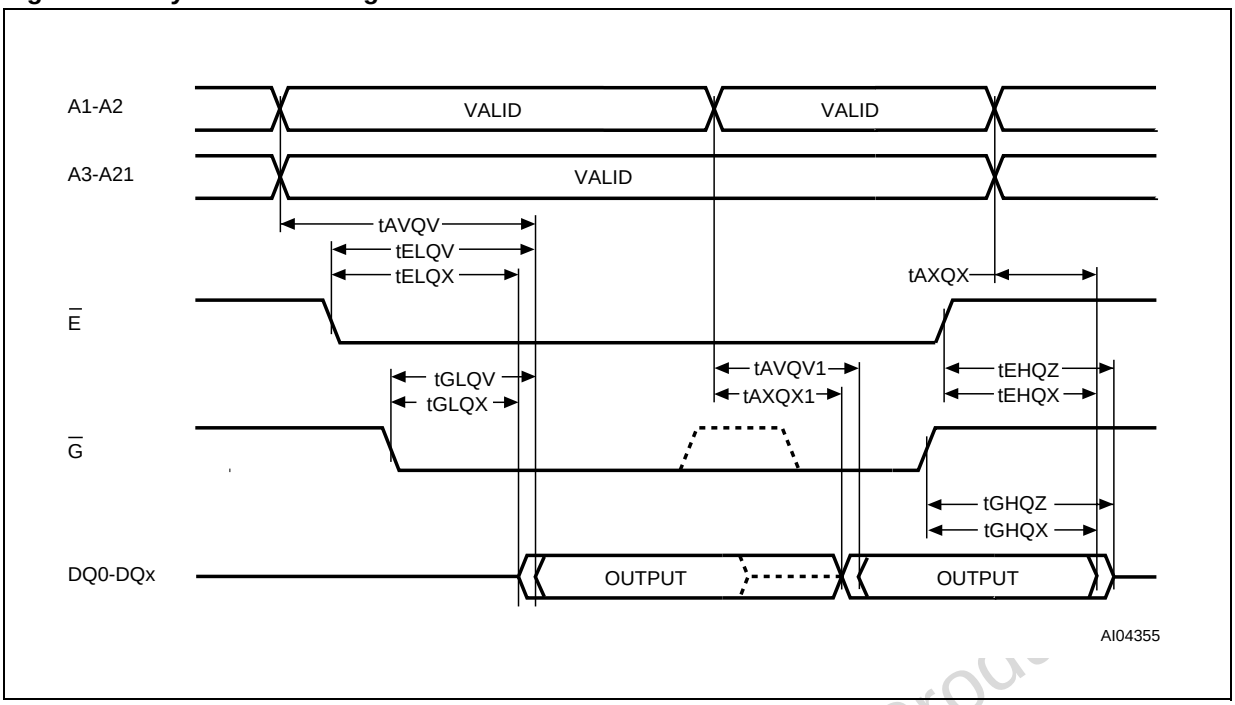
Note: Asynchronous Read (M15 = 1), Latch Enable Controlled (M3 = 1)

Table 17. Asynchronous Latch Controlled Bus Read AC Characteristics

Symbol	Parameter	Test Condition		M58LSW32		Unit
				120	150	
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{AVLH}	Address Valid to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{LHLL}	Latch Enable High to Latch Enable Low		Min	10	10	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	ns
t_{ELLH}	Chip Enable Low to Latch Enable High		Min	10	10	ns
t_{LLQX}	Latch Enable Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{LLQV}	Latch Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	120	150	ns
t_{LHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	20	20	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 14. Asynchronous Page Read AC Waveforms



Note: Asynchronous Read (M15 = 1), Random (M3 = 0)

Table 18. Asynchronous Page Read AC Characteristics

Symbol	Parameter	Test Condition		M58LSW32		Unit
				120	150	
t_{AXQX1}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	6	6	ns
t_{AVQV1}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	25	25	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 15. Asynchronous Write AC Waveform, Write Enable Controlled

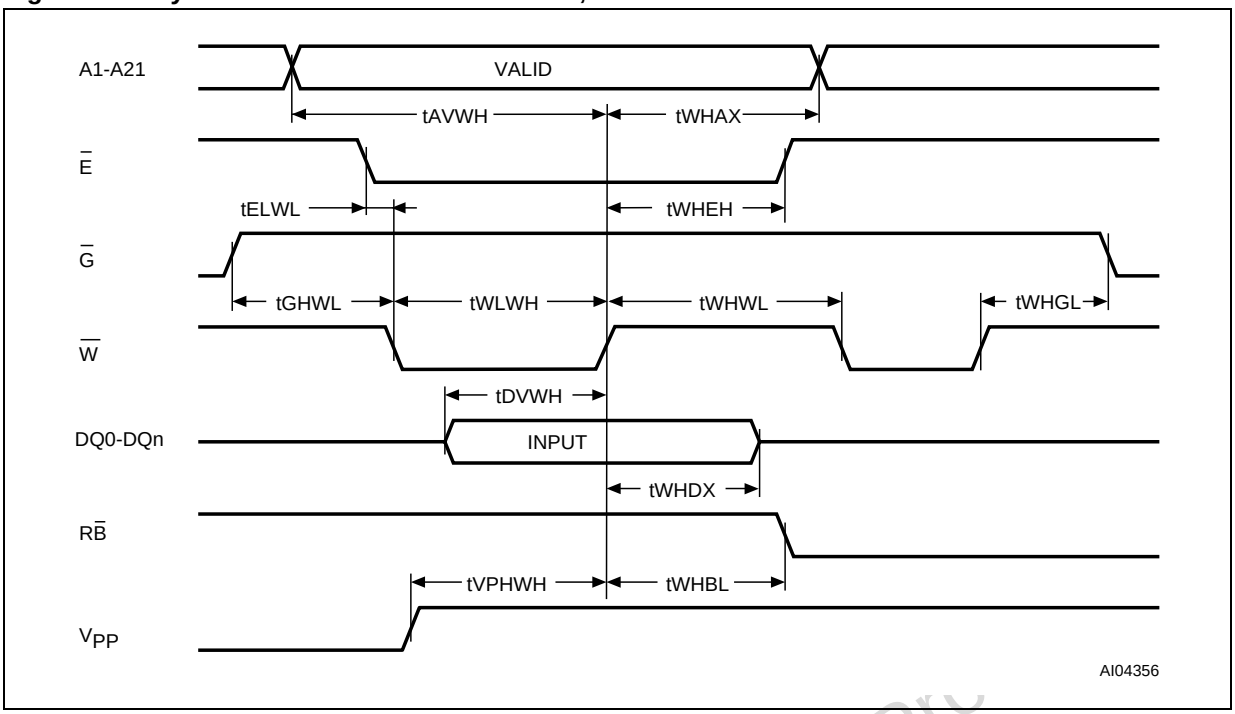


Figure 16. Asynchronous Latch Controlled Write AC Waveform, Write Enable Controlled

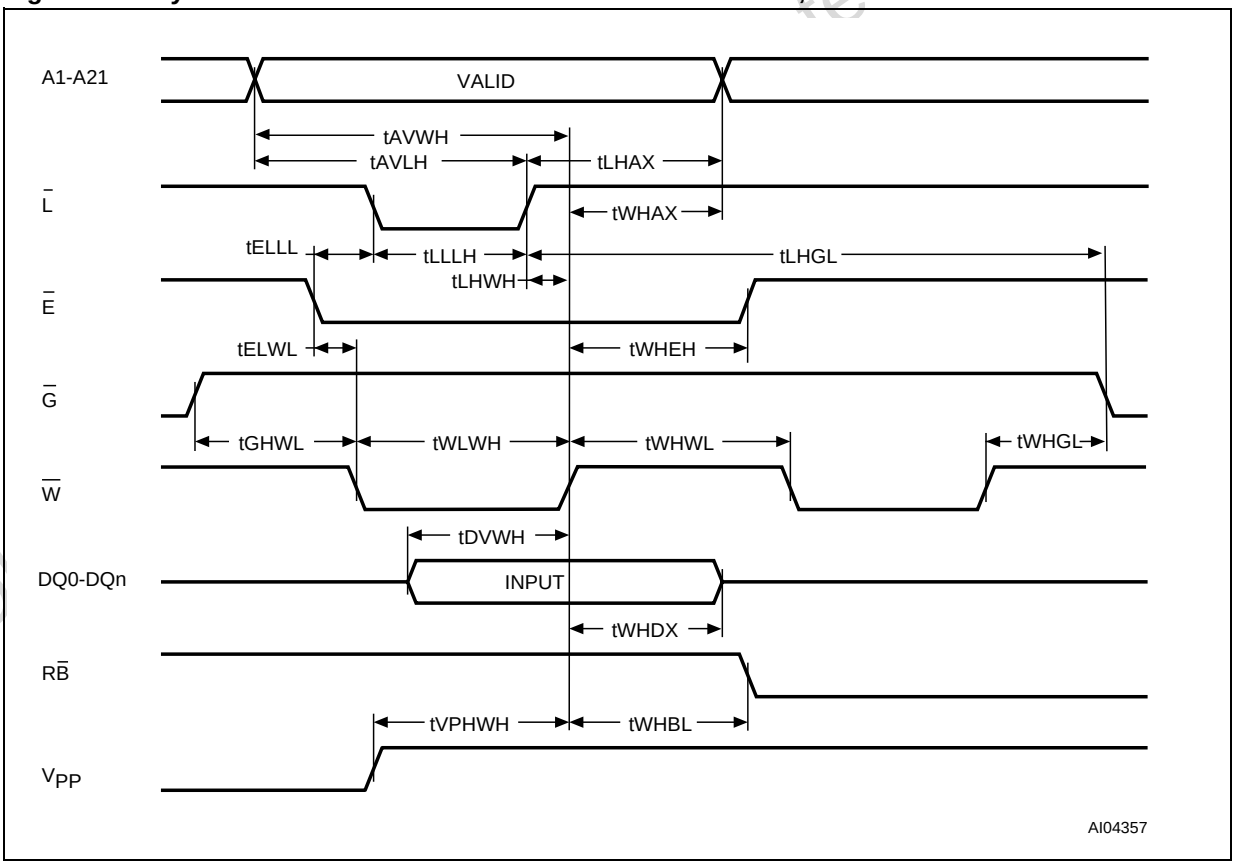


Table 19. Asynchronous Write and Latch Controlled Write AC Characteristics, Write Enable Controlled.

Symbol	Parameter	Test Condition		M58LSW32		Unit
				120	150	
t_{AVLH}	Address Valid to Latch Enable High		Min	10	10	ns
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	0	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	3	3	ns
t_{LHGL}	Latch Enable High to Output Enable Low		Min	35	35	ns
t_{LHWH}	Latch Enable High to Write Enable High		Min	0	0	ns
t_{LLLH}	Latch Enable low to Latch Enable High		Min	10	10	ns
t_{LLWH}	Latch Enable Low to Write Enable High		Min	50	50	ns
t_{VPHWH}	Program/Erase Enable High to Write Enable High		Min	0	0	ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{WHBL}	Write Enable High to Ready/Busy low		Max	90	90	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	0	ns
t_{GHWL}	Output Enable High to Write Enable Low		Min	20	20	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	35	35	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	30	30	ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	70	70	ns

Figure 17. Asynchronous Write AC Waveforms, Chip Enable Controlled

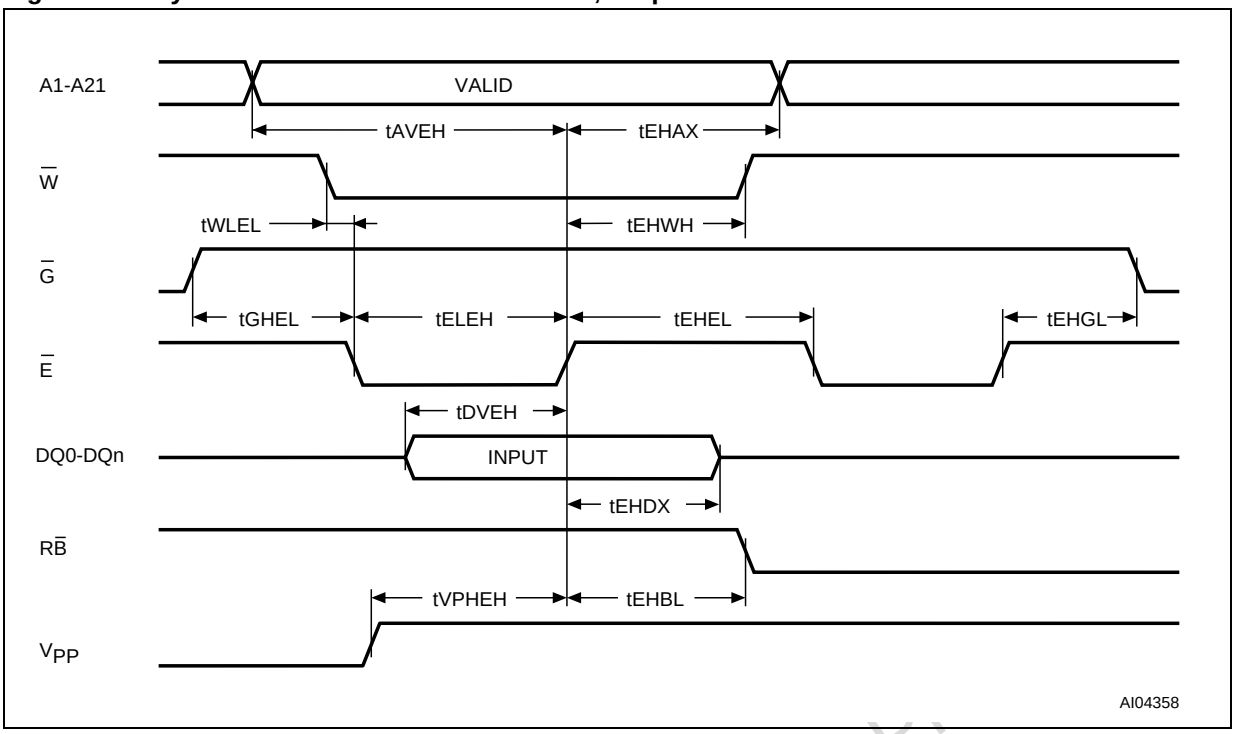


Figure 18. Asynchronous Latch Controlled Write AC Waveforms, Chip Enable Controlled

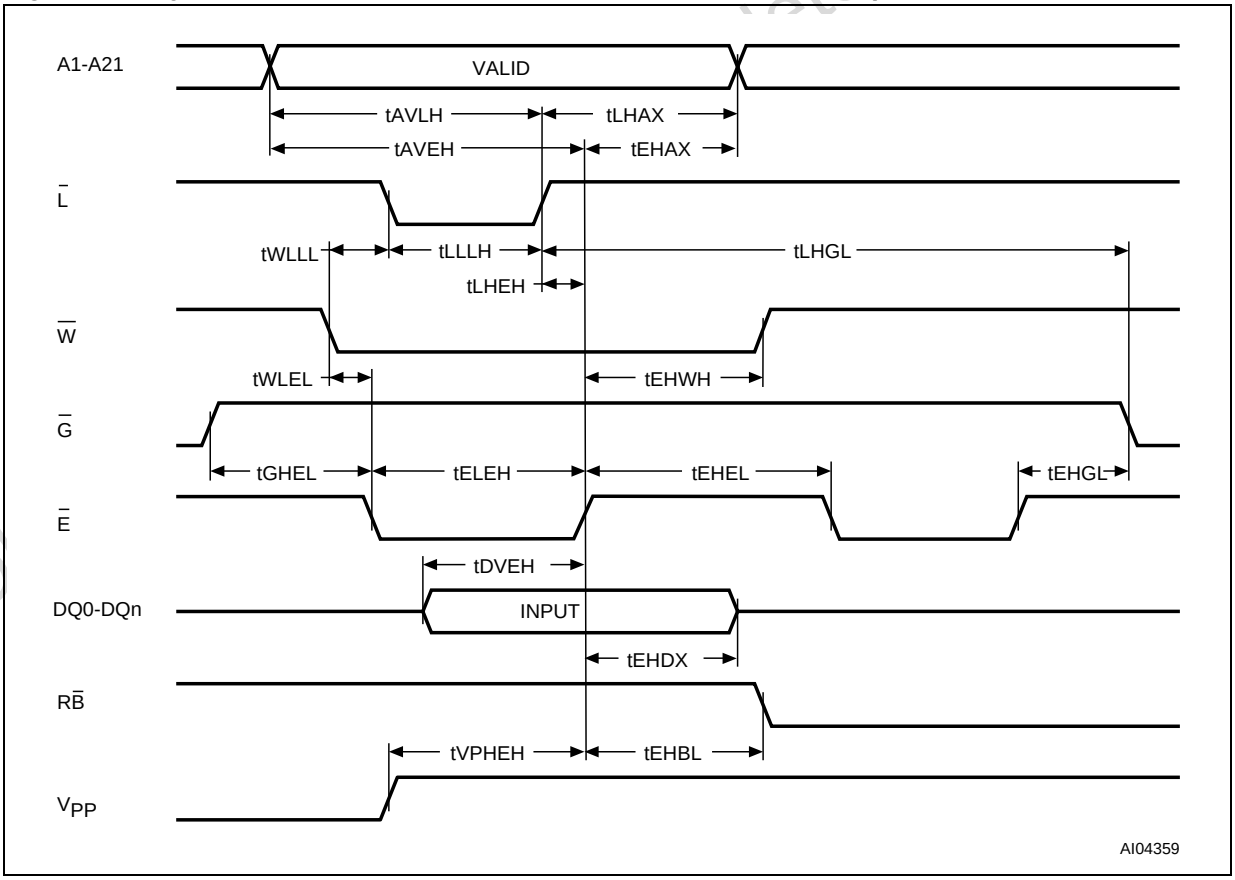
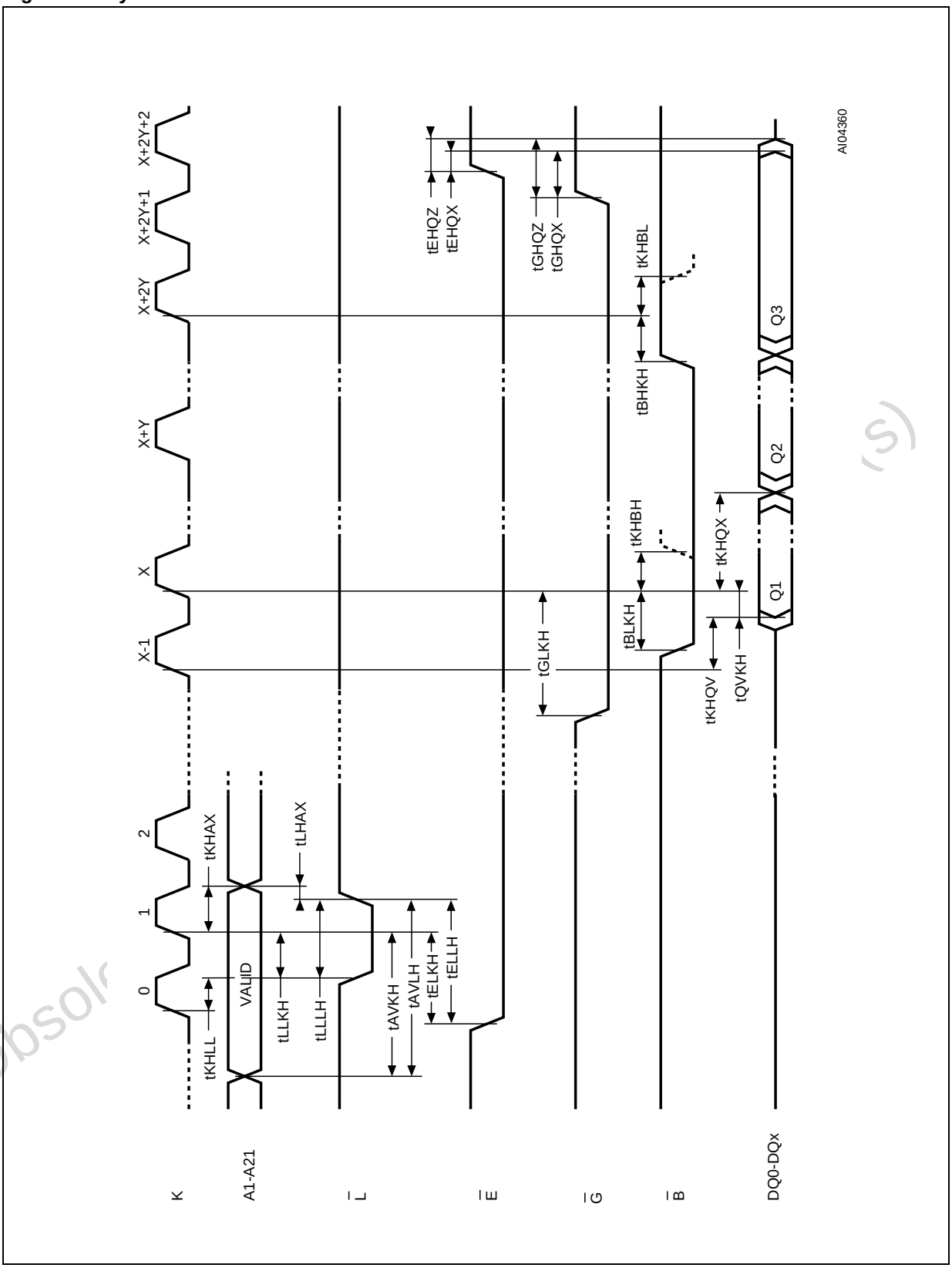


Table 20. Asynchronous Write and Latch Controlled Write AC Characteristics, Chip Enable Controlled

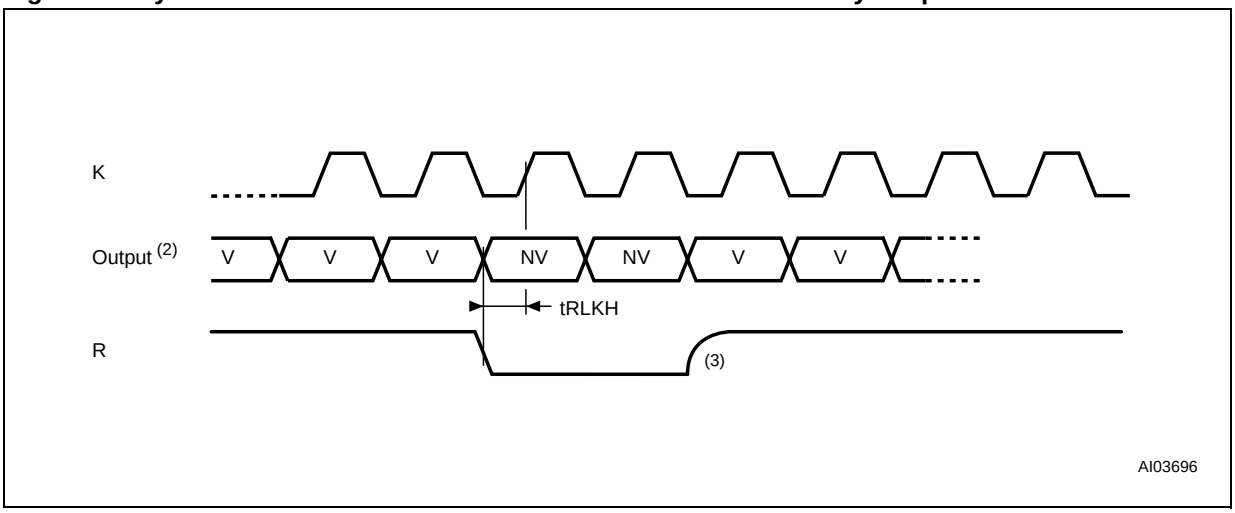
Symbol	Parameter	Test Condition		M58LSW32		Unit
				120	150	
t_{AVLH}	Address Valid to Latch Enable High		Min	10	10	ns
t_{AVEH}	Address Valid to Chip Enable High	$\overline{W} = V_{IL}$	Min	50	50	ns
t_{DVEH}	Data Input Valid to Chip Enable High	$\overline{W} = V_{IL}$	Min	50	50	ns
t_{WLEL}	Write Enable Low to Chip Enable Low		Min	0	0	ns
t_{WLLL}	Write Enable Low to Latch Enable Low		Min	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	3	3	ns
t_{LHGL}	Latch Enable High to Output Enable Low		Min	35	35	ns
t_{LHEH}	Latch Enable High to Chip Enable High		Min	0	0	ns
t_{LLLH}	Latch Enable low to Latch Enable High		Min	10	10	ns
t_{LLEH}	Latch Enable Low to Chip Enable High		Min	50	50	ns
t_{VPHEH}	Program/Erase Enable High to Chip Enable High		Min	0	0	ns
t_{EHAX}	Chip Enable High to Address Transition	$\overline{W} = V_{IL}$	Min	10	10	ns
t_{EHBL}	Chip Enable High to Ready/Busy low		Max	90	90	ns
t_{EHDX}	Chip Enable High to Input Transition	$\overline{W} = V_{IL}$	Min	10	10	ns
t_{EHWH}	Chip Enable High to Write Enable High		Min	0	0	ns
t_{GHEL}	Output Enable High to Chip Enable Low		Min	20	20	ns
t_{EHGL}	Chip Enable High to Output Enable Low		Min	35	35	ns
t_{EHEL}	Chip Enable High to Chip Enable Low		Min	30	30	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	$\overline{W} = V_{IL}$	Min	70	70	ns

Figure 19. Synchronous Burst Read AC Waveform



Note: Valid Clock Edge = Rising (M6 = 1)

Figure 20. Synchronous Burst Read - Continuous - Valid Data Ready Output



Note: 1. Valid Data Ready = Valid Low during valid clock edge (M8 = 0)
2. V= Valid output, NV= Not Valid output.
3. R is an open drain output with an internal pull up resistor of 1MΩ Depending on the Valid Data Ready pin capacitance load an external pull up resistor must be chosen according to the system clock period.
4. When the system clock frequency is between 33MHz and 50MHz and the Y latency is set to 2, values of $\overline{B}$ sampled on odd clock cycles, starting from the first read are not considered.

Table 21. Synchronous Burst Read AC Characteristics

Symbol	Parameter	Test Condition		M58LSW32		Unit
				120	150	
t_{AVKH}	Address Valid to Active Clock Edge	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{AVLH}	Address Valid to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{BHKH}	Burst Address Advance High to Active Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	10	10	ns
t_{BLKH}	Burst Address Advance Low to Active Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	10	10	ns
t_{ELKH}	Chip Enable Low to Active Clock Edge	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{ELLH}	Chip Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{GLKH}	Output Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{L} = V_{IH}$	Min	20	20	ns
t_{KHAX}	Valid Clock Edge to Address Transition	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{KHLH}	Valid Clock Edge to Latch Enable High	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{KHQX}	Valid Clock Edge to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	3	3	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{KHQV}	Valid Clock Edge to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Max	20	20	ns
t_{QVKH}	Output Valid to Active Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	5	5	ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	5	5	ns
t_{KHBL}	Active Clock Edge to Burst Address Advance Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	0	0	ns
t_{KHBH}	Active Clock Edge to Burst Address Advance High	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	Min	0	0	ns

Note: For other timings see Table 16, Asynchronous Bus Read Characteristics.

Figure 21. Reset, Power-Down and Power-up AC Waveform

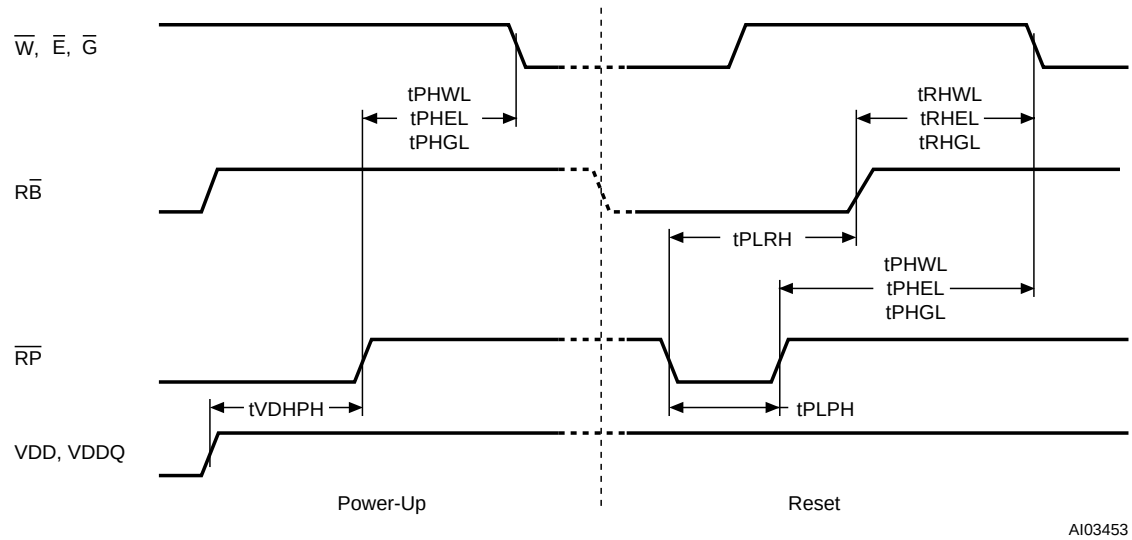
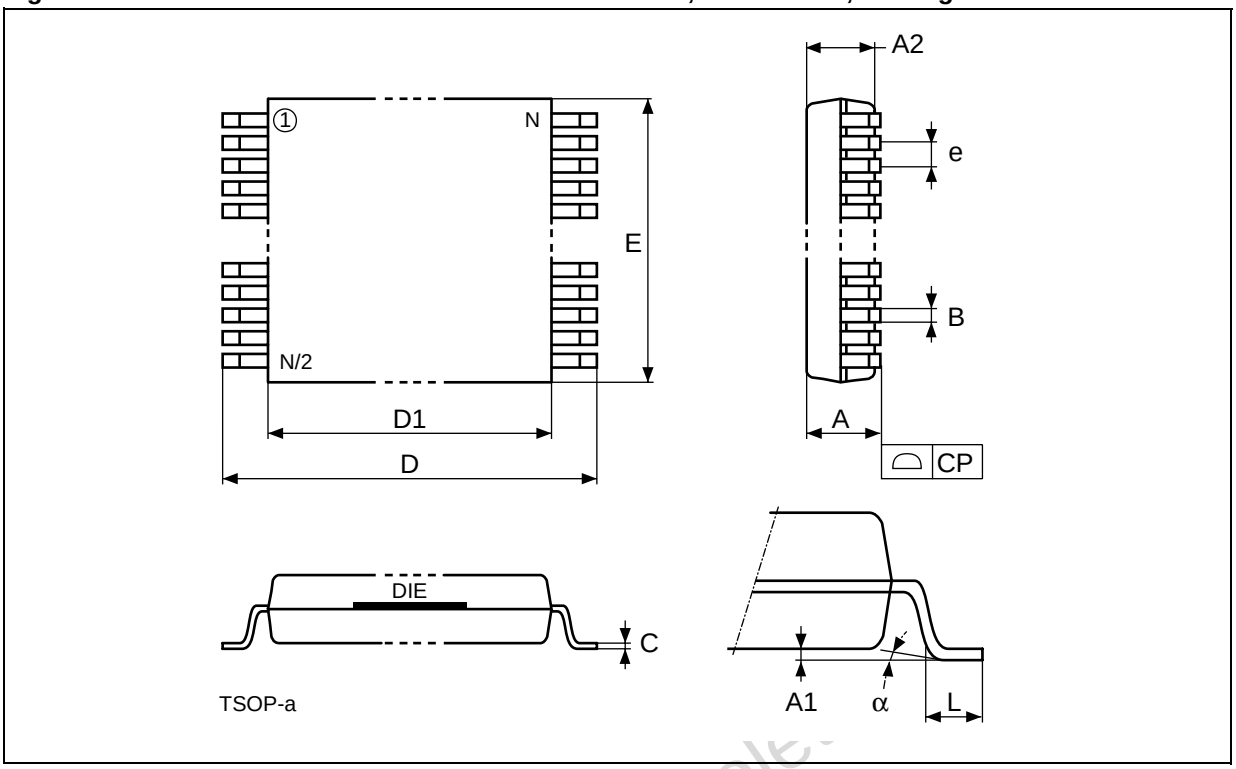


Table 22. Reset, Power-Down and Power-up AC Characteristics

Symbol	Parameter		M58LSW32		Unit
			120	150	
t_{PHWL} t_{PHEL} t_{PHGL}	Reset/Power-Down High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	10	10	µs
t_{RHWL} t_{RHEL} t_{RHGL}	Ready/Busy High to Write Enable Low, Chip Enable Low, Output Enable Low (Program/Erase Controller Active)	Min	10	10	µs
t_{PLPH}	Reset/Power-Down Low to Reset/Power-Down High	Min	100	100	ns
t_{PLRH}	Reset/Power-Down Low to Ready High	Max	30	30	µs
t_{VDHPH}	Supply Voltages High to Reset/Power-Down High	Min	1	1	µs

PACKAGE MECHANICAL

Figure 22. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Outline

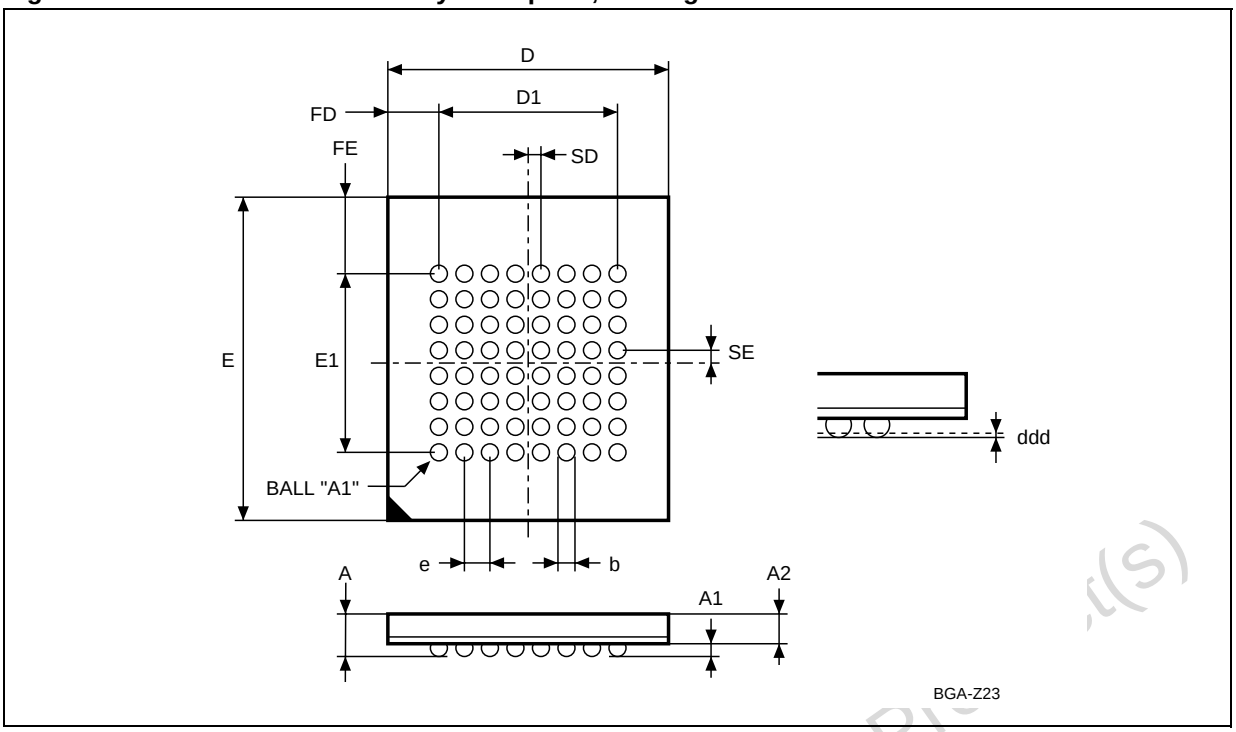


Note: Drawing is not to scale.

Table 23. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		13.90	14.10		0.5472	0.5551
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	56			56		
CP			0.10			0.0039

Figure 23. TBGA64 - 8 x 8 ball array 1mm pitch, Package Outline

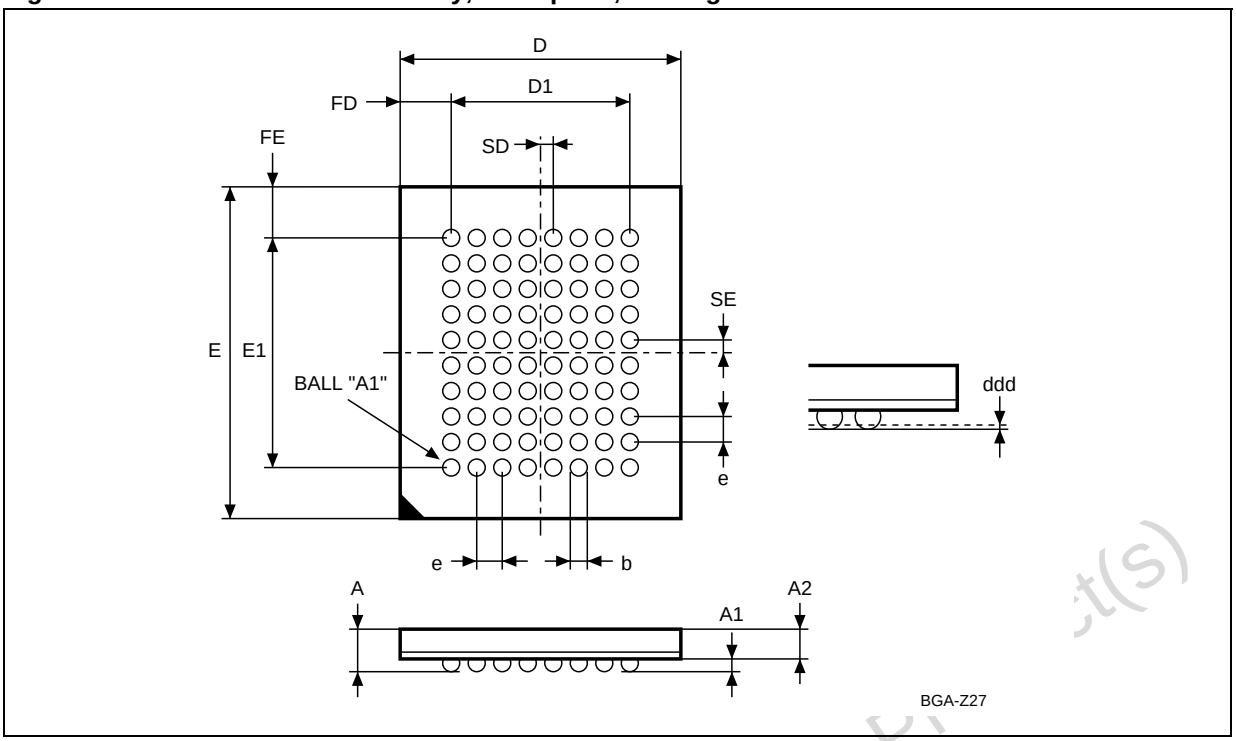


Note: Drawing is not to scale.

Table 24. TBGA64 - 8 x 8 ball array, 1 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2			0.850			0.0335
b		0.400	0.500		0.0157	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000	–	–	0.2756	–	–
ddd			0.100			0.0039
e	1.000	–	–	0.0394	–	–
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	7.000	–	–	0.2756	–	–
FD	1.500	–	–	0.0591	–	–
FE	3.000	–	–	0.1181	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

Figure 24. TBGA80 - 8 x 10 ball array, 1mm pitch, Package Outline



Note: Drawing is not to scale.

Table 25. TBGA80 - 8 x 10 ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2			0.850			0.0335
b		0.400	0.500		0.0157	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000	–	–	0.2756	–	–
ddd			0.100			0.0039
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	9.000	–	–	0.3543	–	–
e	1.000	–	–	0.0394	–	–
FD	1.500	–	–	0.0591	–	–
FE	2.000	–	–	0.0787	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

PART NUMBERING

Table 26. Ordering Information Scheme

Example: M58LSW32A 120 N 1 T

Device Type
M58

Architecture
L = Multi-Bit Cell or Multi-Bit Compatible, Burst Mode, Page Mode
S = Special

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = 1.8 to V_{DD}

Device Function
32A = 32 Mbit (x16), Equal Block, Boot Block
32B = 32 Mbit (x16/x32), Equal Block, Boot Block

Speed
120 = 120 ns
150 = 150 ns

Package
N = TSOP56: 14 x 20 mm (M58LSW32A)
ZA = TBGA64: 1mm pitch (M58LSW32A)
ZA = TBGA80: 1mm pitch (M58LSW32B)

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’.
For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 27. Document Revision History

Date	Version	Revision Details
06-Apr-2001	-01	First Issue.
05-Jun-2001	-02	150ns speed class added, corrections Figures 7 , 8, 9, 15, 16, 17 and 18.

APPENDIX A. BLOCK ADDRESS TABLE

Table 28. Block Addresses

Block Number	Address Range (x16 Bus Width)	Address Range (x32 Bus Width)
64	1F8000h-1FFFFFh	0FC000h-0FFFFFh
63	1F0000h-1F7FFFh	0F8000h-0FBFFFh
62	1E8000h-1EFFFFh	0F4000h-0F7FFFh
61	1E0000h-1E7FFFh	0F0000h-0F3FFFh
60	1D8000h-1DFFFFh	0EC000h-0EFFFFh
59	1D0000h-1D7FFFh	0E8000h-0EBFFFh
58	1C8000h-1CFFFFh	0E4000h-0E7FFFh
57	1C0000h-1C7FFFh	0E0000h-0E3FFFh
56	1B8000h-1BFFFFh	0DC000h-0DFFFFh
55	1B0000h-1B7FFFh	0D8000h-0DBFFFh
54	1A8000h-1AFFFFh	0D4000h-0D7FFFh
53	1A0000h-1A7FFFh	0D0000h-0D3FFFh
52	198000h-19FFFFh	0CC000h-0CFFFFh
51	190000h-197FFFh	0C8000h-0CBFFFh
50	188000h-18FFFFh	0C4000h-0C7FFFh
49	180000h-187FFFh	0C0000h-0C3FFFh
48	178000h-17FFFFh	0BC000h-0BFFFFh
47	170000h-177FFFh	0B8000h-0BBFFFh
46	168000h-16FFFFh	0B4000h-0B7FFFh
45	160000h-167FFFh	0B0000h-0B3FFFh
44	158000h-15FFFFh	0AC000h-0AFFFFh
43	150000h-157FFFh	0A8000h-0ABFFFh
42	148000h-14FFFFh	0A4000h-0A7FFFh
41	140000h-147FFFh	0A0000h-0A3FFFh
40	138000h-13FFFFh	09C000h-09FFFFh
39	130000h-137FFFh	098000h-09BFFFh
38	128000h-12FFFFh	094000h-097FFFh
37	120000h-127FFFh	090000h-093FFFh
36	118000h-11FFFFh	08C000h-08FFFFh
35	110000h-117FFFh	088000h-08BFFFh
34	108000h-10FFFFh	084000h-087FFFh
33	100000h-107FFFh	080000h-083FFFh
32	0F8000h-0FFFFFh	07C000h-07FFFFh
31	0F0000h-0F7FFFh	078000h-07BFFFh
30	0E8000h-0EFFFFh	074000h-077FFFh
29	0E0000h-0E7FFFh	070000h-073FFFh
28	0D8000h-0DFFFFh	06C000h-06FFFFh
27	0D0000h-0D7FFFh	068000h-06BFFFh
26	0C8000h-0CFFFFh	064000h-067FFFh
25	0C0000h-0C7FFFh	060000h-063FFFh
24	0B8000h-0BFFFFh	05C000h-05FFFFh
23	0B0000h-0B7FFFh	058000h-05BFFFh
22	0A8000h-0AFFFFh	054000h-057FFFh
21	0A0000h-0A7FFFh	050000h-053FFFh
20	098000h-09FFFFh	04C000h-04FFFFh
19	090000h-097FFFh	048000h-04BFFFh
18	088000h-08FFFFh	044000h-047FFFh
17	080000h-087FFFh	040000h-043FFFh
16	078000h-07FFFFh	03C000h-03FFFFh
15	070000h-077FFFh	038000h-03BFFFh
14	068000h-06FFFFh	034000h-037FFFh
13	060000h-067FFFh	030000h-033FFFh
12	058000h-05FFFFh	02C000h-02FFFFh
11	050000h-057FFFh	028000h-02BFFFh
10	048000h-04FFFFh	024000h-027FFFh
9	040000h-047FFFh	020000h-023FFFh
8	038000h-03FFFFh	01C000h-01FFFFh
7	030000h-037FFFh	018000h-01BFFFh
6	028000h-02FFFFh	014000h-017FFFh
5	020000h-027FFFh	010000h-013FFFh
4	018000h-01FFFFh	00C000h-00FFFFh
3	010000h-017FFFh	008000h-00BFFFh
2	008000h-00FFFFh	004000h-007FFFh
1	000000h-007FFFh	000000h-003FFFh

APPENDIX B. COMMON FLASH INTERFACE - CFI

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 29, 30, 31, 32, 33 and 34 show the addresses used to retrieve the data.

Table 29. Query Structure Overview

Offset	Sub-section Name	Description
00h		Manufacturer Code
01h		Device Code
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash memory layout
P(h)(1)	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A(h)(2)	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)
(BA+2)h	Block Status Register	Block-related Information

Note: 1. Offset 15h defines P which points to the Primary Algorithm Extended Query Address Table.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.

Table 30. CFI - Query Address and Data Output

Address (4) A21-A1 (M58LSW32A) A21-A2 (M58LSW32B)	Data		Instruction
10h	51h	"Q"	Query ASCII String 51h; "Q" 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	20h		Primary Vendor: Command Set and Control Interface ID Code
14h	00h		
15h	31h		Primary algorithm extended Query Address Table: P(h)
16h	00h		
17h	00h		Alternate Vendor: Command Set and Control Interface ID Code
18h	00h		
19h	31h		Alternate Algorithm Extended Query address Table
1Ah(5)	00h		

Note: 1. The x8 or Byte Address mode is not available.
2. With the x16 Bus Width, the value of the address location of the CFI Query is independent of A1 pad (M58LSW32B).
3. Query Data are always presented on DQ7-DQ0. DQ31-DQ8 are set to '0'.
4. For M58LSW32B, A1 = Don't Care.
5. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.

Table 31. CFI - Device Voltage and Timing Specification

Address (4) A21-A1 (M58LSW32A) A21-A2 (M58LSW32B)	Data	Description
1Bh	27h (1)	V_{DD} Min, 2.7V
1Ch	36h (1)	V_{DD} max, 3.6V
1Dh	00h (2)	V_{PP} min – Not Available
1Eh	00h (2)	V_{PP} max – Not Available
1Fh	00h (3)	2^n ms typical time-out for Word, DWord prog – Not Available
20h	07h	2^n ms, typical time-out for max buffer write
21h	0Ah	2^n ms, typical time-out for Erase Block
22h	00h (3)	2^n ms, typical time-out for chip erase – Not Available
23h	00h (3)	2^n x typical for Word Dword time-out max – Not Available
24h	04h	2^n x typical for buffer write time-out max
25h	04h	2^n x typical for individual block erase time-out maximum
26h	00h (3)	2^n x typical for chip erase max time-out – Not Available

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.
2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volts while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
3. Not supported.
4. For M58LSW32B, A1 = Don't Care.

Table 32. Device Geometry Definition

Address (1) A21-A1 (M58LSW32A) A21-A2 (M58LSW32B)	Data	Description
27h	17h	2^n number of bytes memory Size
28h	01h.	Device Interface Sync./Async.
29h	00h	Organization Sync./Async.
2Ah	05h	Maximum number of bytes in Write Buffer, 2^n
2Bh	00h	
2Ch	01h	Bit7-0 = number of Erase Block Regions in device
2Dh	3Fh	Number (n-1) of Erase Blocks of identical size; n=64
2Eh	00h	
2Fh	00h	Erase Block Region Information Erase block (64K bytes)
30h	02h	

Note: 1. For M58LSW32B, A1 = Don't Care.

Table 33. Block Status Register

Address A21-A1 (M58LSW32A) A21-A2 (M58LSW32B)	Data		Selected Block Information
(BA+2)h[1]	bit0	0	Block Unlocked
		1	Block Locked
	bit1	0	Last erase operation ended successfully [2]
		1	Last erase operation not ended successfully [2]
	bit7-2	0	Reserved for future features

Note: 1. BA specifies the block address location, A21-A17.
2. Not Supported.

Table 34. Extended Query information

	M58LSW32B – x32 Bus Width M58LSW32A – x16 Bus Width			M58LSW32B – x16 Bus Width		Description
Address offset	Address A21-A2	Data (Hex) x32 Bus Width		Address A21-A1	Data	
(P)h	31h	50h	"P"	62h, 63h	50h	Query ASCII string - Extended Table
(P+1)h	32h	52h	"R"	64h, 65h	52h	
(P+2)h	33h	49h	"Y"	66h, 67h	49h	
(P+3)h	34h	31h		68h, 69h	31h	Major version number
(P+4)h	35h	31h		6Ah, 6Bh	31h	Minor version number
(P+5)h	36h	0Eh		6Ch, 6Dh	0Eh	Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Lock/Unlock Supported (1=yes) bit4, Queue Erase Supported (0=no) Bit 31-5 reserved for future use
(P+6)h	37h	00h		6Eh, 6Fh	00h	Optional Features
(P+7)h	38h	00h		70h, 71h	00h	
(P+8)h	39h	00h		72h, 73h	00h	
(P+9)h	3Ah	01h		74h, 75h	00h	Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h	3Bh	00h [2]		76h, 77h	00h [2]	Block Status Register Mask
(P+C)h	3Ch	33h		78h, 79h	33h	V_{DD} OPTIMUM Program/Erase voltage conditions
(P+D)h	3Dh	50h		7Ah, 7Bh	50h	V_{PP} OPTIMUM Program/Erase voltage conditions
(P+E)h	3Eh	00h		7Ch, 7Dh	00h	Reserved for future use
(P+F)h	3Fh	00h		7Dh, 7Fh	00h	Reserved for future use

Note: 1. Bit7 to bit4 are coded in Hexadecimal and scaled in Volt while bit3 to bit0 are in Binary Code Decimal and scaled in mV.
2. Not supported.

APPENDIX C. FLOW CHARTS

Figure 25. Write to Buffer and Program Flowchart and Pseudo Code

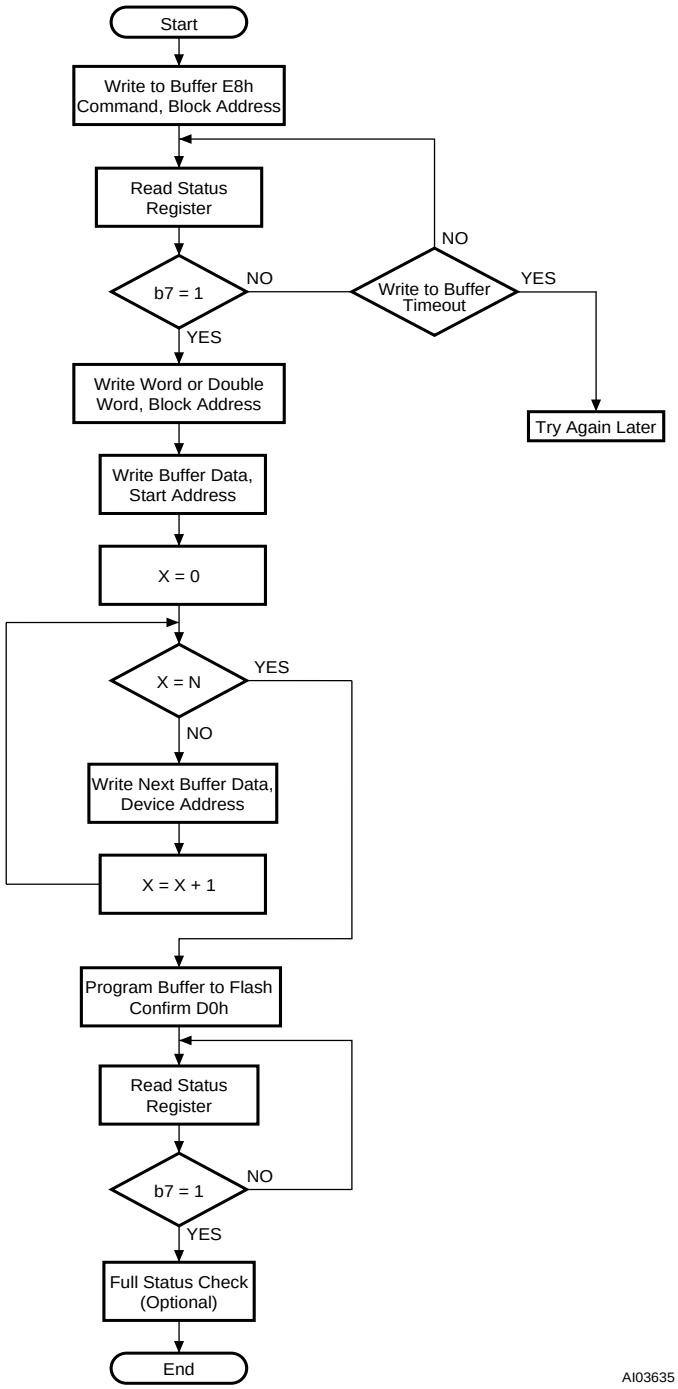
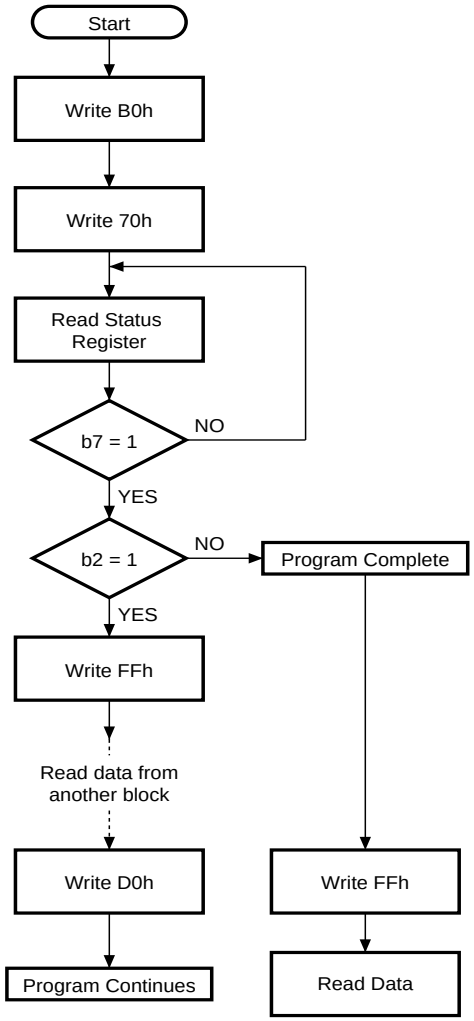


Figure 26. Program Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while b7 = 1

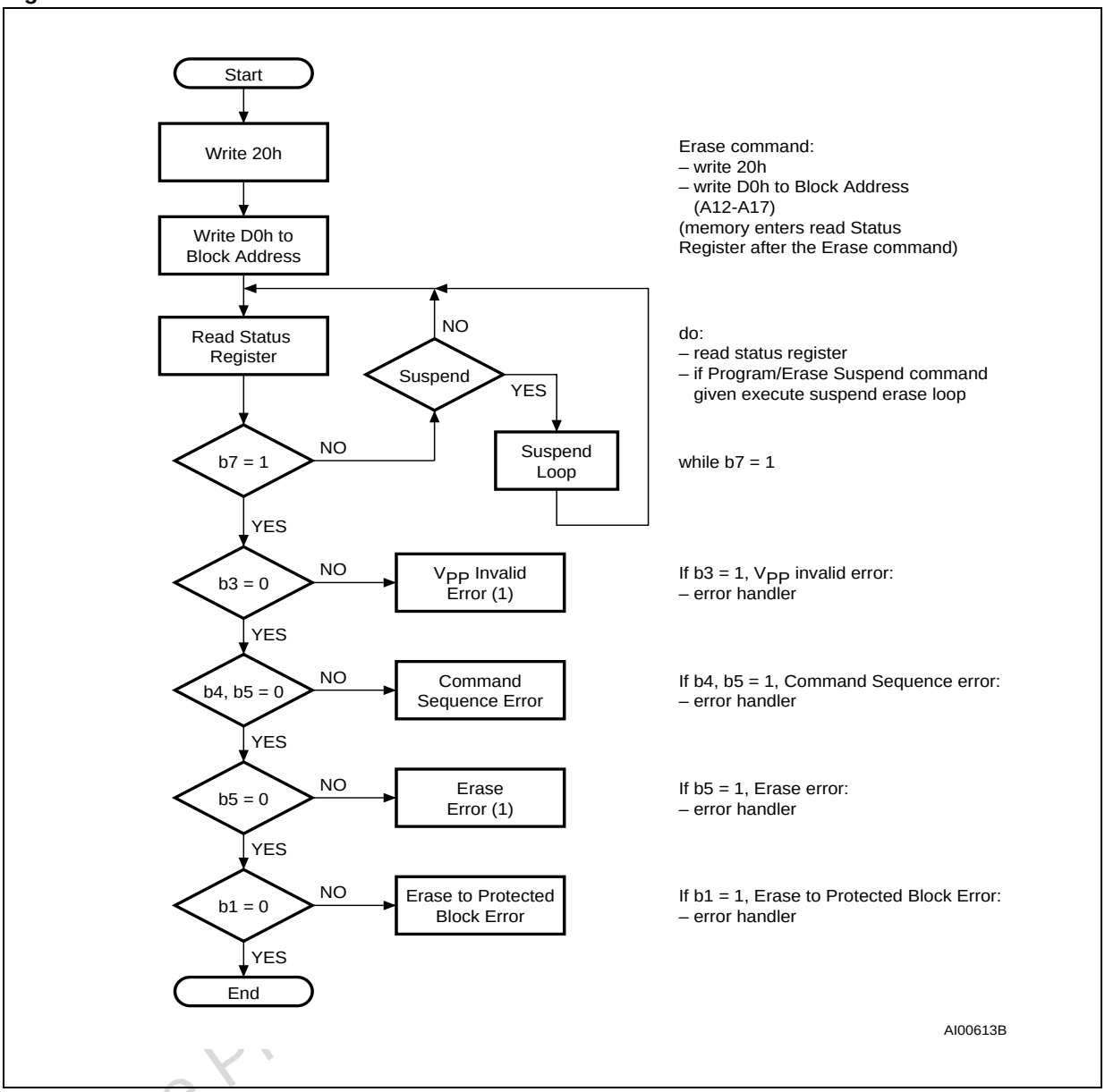
If b4 = 0, Program completed

Read Memory Array instruction:
– write FFh
– one or more data reads from other blocks

Program Erase Resume Command:
– write D0h to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase Suspend command was not issued).

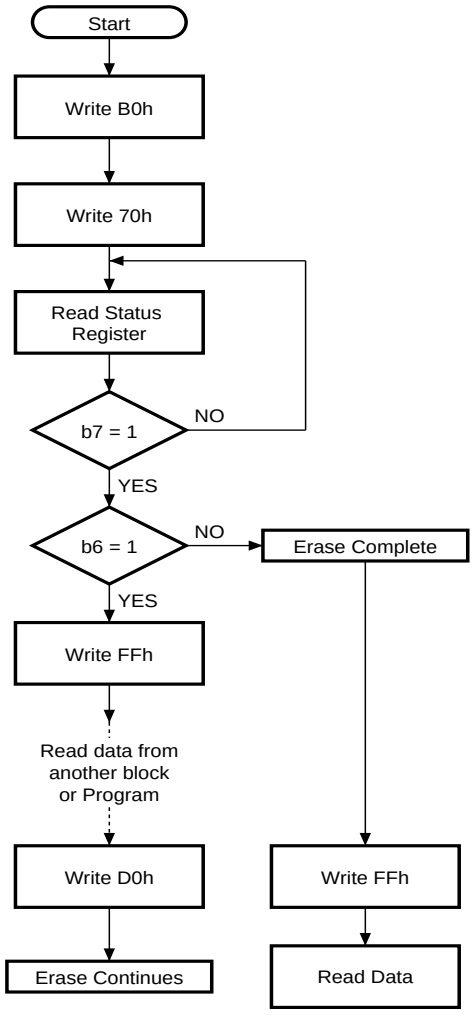
AI00612

Figure 27. Erase Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (Clear Status Register Command) before further Program or Erase operations.

Figure 28. Erase Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while b7 = 1

If b6 = 0, Erase completed

Read Memory Array command:
– write FFh
– one o more data reads from other blocks

Program/Erase Resume command:
– write D0h to resume the Erase operation
– if the Program operation completed then this is not necessary. The device returns to Read mode as normal (as if the Program/Erase suspend was not issued).

AI00615

Figure 29. Command Interface and Program Erase Controller Flowchart (a)

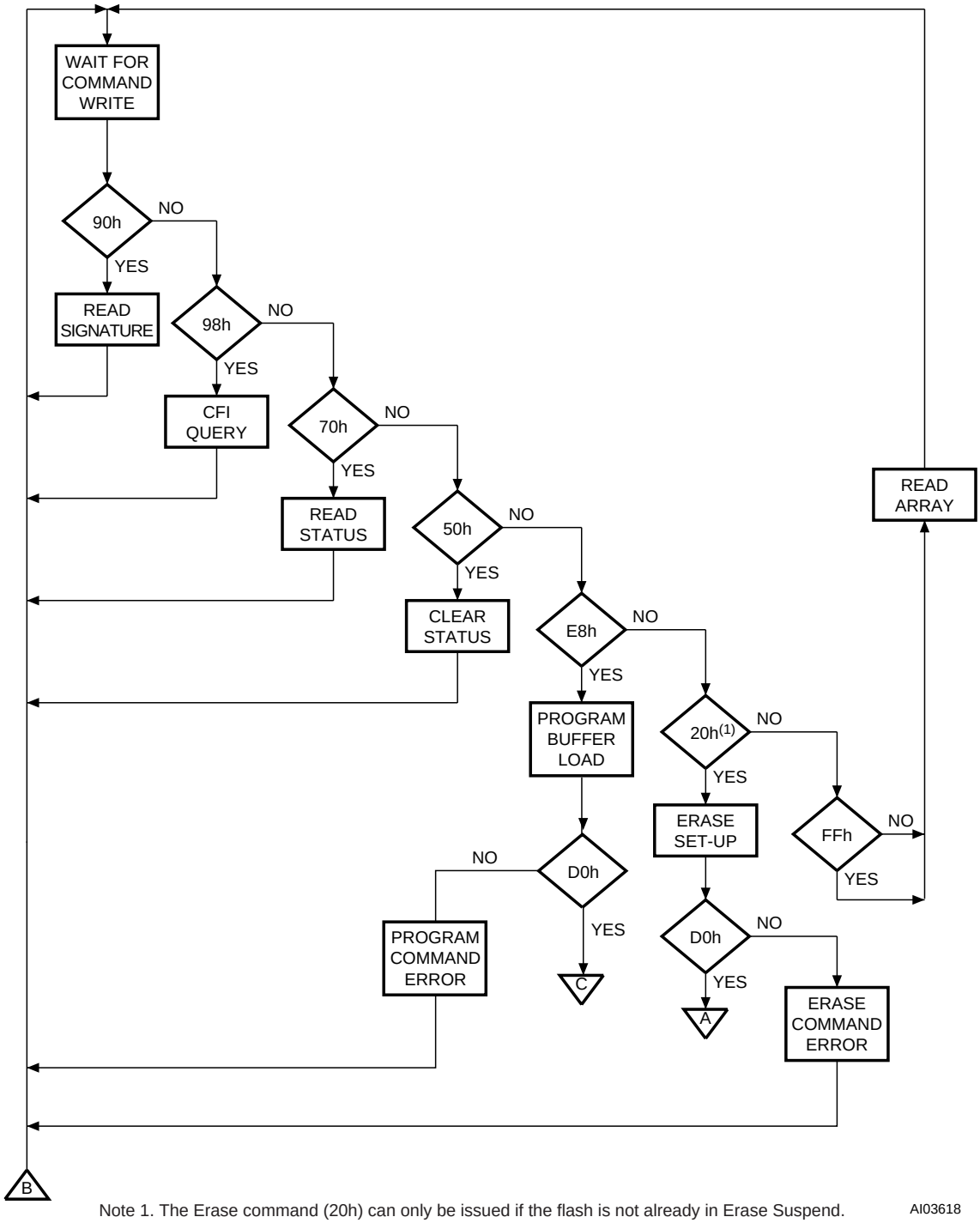


Figure 30. Command Interface and Program Erase Controller Flowchart (b)

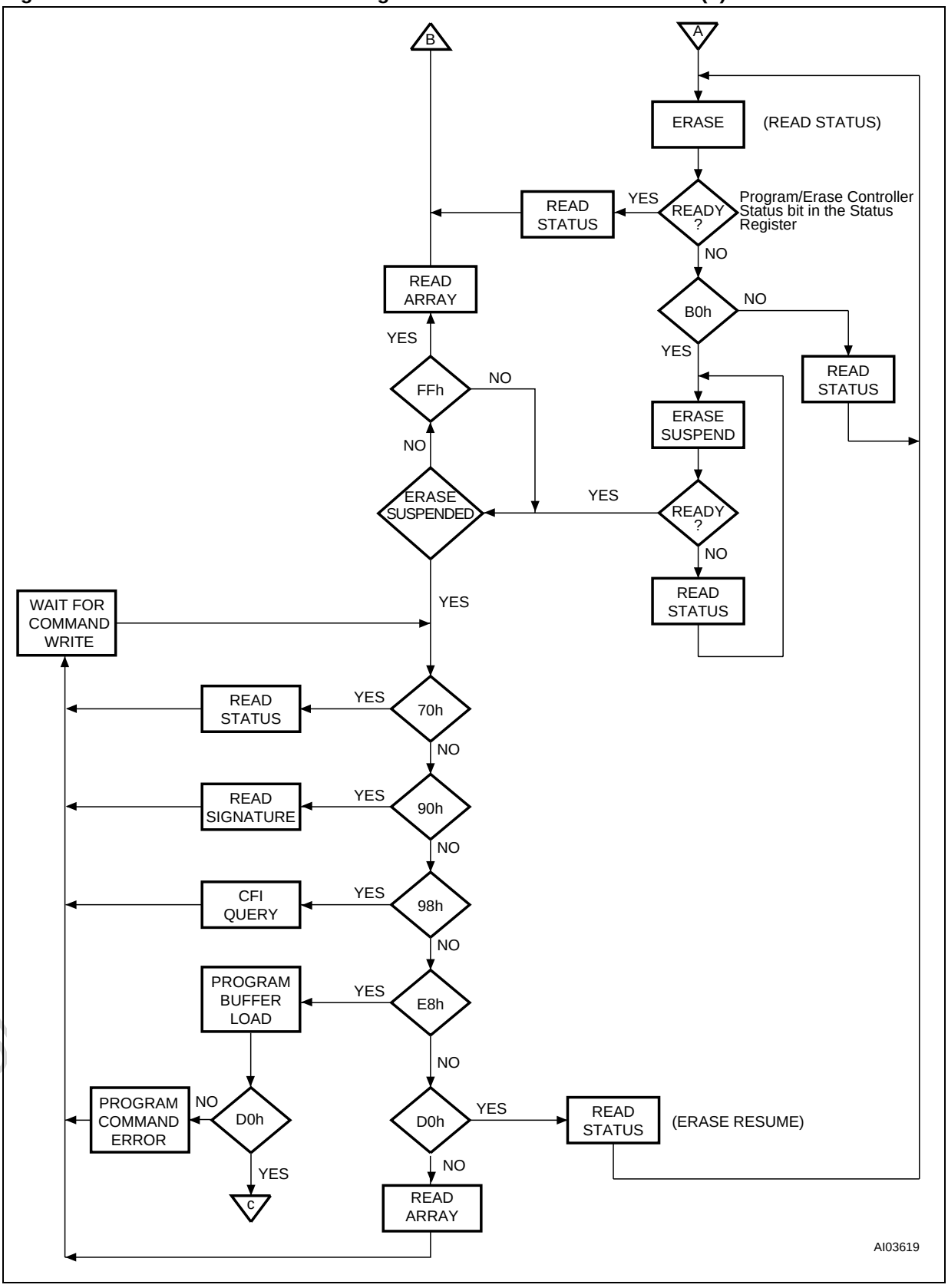


Figure 31. Command Interface and Program Erase Controller Flowchart (c).