

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC174FN

Hex D-Type Flip Flop with Clear

The TC74VHC174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

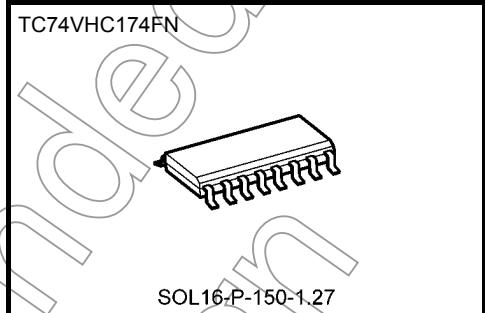
When the CLR input is held low, the Q output are in the low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

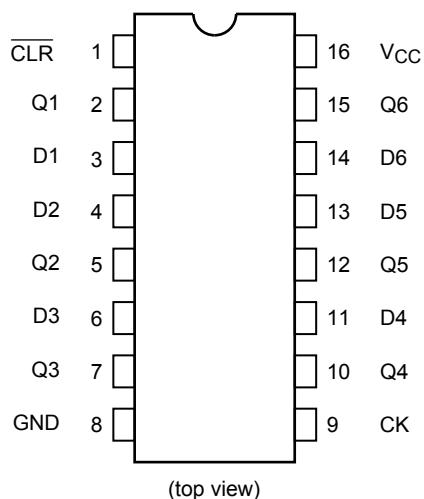
- High speed: $f_{max} = 175$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC(\text{opr})} = 2$ to 5.5 V
- Low noise: $V_{OLP} = 0.8$ V (max)
- Pin and function compatible with 74ALS174

Note: xxxFN (JEDEC SOP) is not available in Japan.

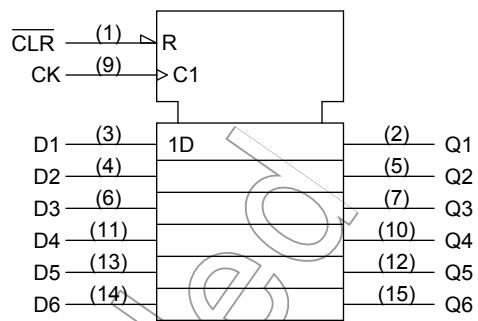


Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

Pin Assignment



IEC Logic Symbol

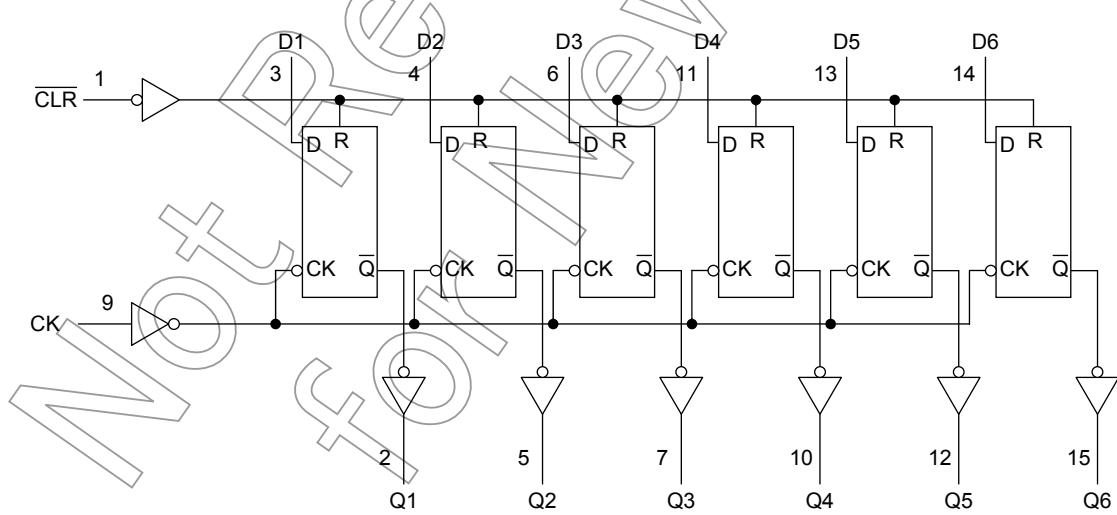


Truth Table

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{STG}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{OPR}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min	Max		
High-level input voltage	V _{IH}	—	—	2.0 3.0 to 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V	
Low-level input voltage	V _{IL}	—	—	2.0 3.0 to 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA I _{OH} = -4 mA I _{OH} = -8 mA	2.0	1.9	2.0	—	1.9	—	V	
				3.0	2.9	3.0	—	2.9	—		
				4.5	4.4	4.5	—	4.4	—		
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	3.0	2.58	—	—	2.48	—	V	
				4.5	3.94	—	—	3.80	—		
			I _{OL} = 4 mA I _{OL} = 8 mA	3.0	—	—	0.36	—	0.44		
				4.5	—	—	0.36	—	0.44		
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	µA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	µA	

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition			Ta = 25°C		Ta = -40 to 85°C		Unit
				V _{CC} (V)	Typ.	Limit	Limit	Limit	
Minimum pulse width (CK)	t _w (L) t _w (H)	—	—	3.3 ± 0.3	—	5.0	5.0	ns	ns
				5.0 ± 0.5	—	5.0	5.0	5.0	
Minimum pulse width (CLR)	t _w (L)	—	—	3.3 ± 0.3	—	5.0	5.0	ns	ns
				5.0 ± 0.5	—	5.0	5.0	5.0	
Minimum set-up time	t _s	—	—	3.3 ± 0.3	—	5.0	6.0	ns	ns
				5.0 ± 0.5	—	4.5	4.5	4.5	
Minimum hold time	t _h	—	—	3.3 ± 0.3	—	0.0	0.0	ns	ns
				5.0 ± 0.5	—	0.5	0.5	0.5	
Minimum removal time (CLR)	t _{rem}	—	—	3.3 ± 0.3	—	3.0	3.0	ns	ns
				5.0 ± 0.5	—	2.5	2.5	2.5	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			$T_a = 25^\circ C$			$T_a = -40$ to $85^\circ C$		Unit	
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (CK-Q)	t_{pLH}	—	3.3 ± 0.3	15	—	7.2	11.0	1.0	13.0	ns	
				50	—	9.7	14.5	1.0	16.5		
	t_{pHL}		5.0 ± 0.5	15	—	4.9	7.2	1.0	8.5		
				50	—	6.4	9.2	1.0	10.5		
Propagation delay time (\overline{CLR} -Q)	t_{pHL}	—	3.3 ± 0.3	15	—	7.4	11.4	1.0	13.5	ns	
				50	—	9.9	14.9	1.0	17.0		
	t_{pHL}		5.0 ± 0.5	15	—	5.1	7.6	1.0	9.0		
				50	—	6.6	9.6	1.0	11.0		
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	95	150	—	80	—	MHz	
				50	55	85	—	50	—		
	f_{max}		5.0 ± 0.5	15	130	175	—	110	—		
				50	90	120	—	80	—		
Output to output skew	t_{osLH}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns	
			5.5 ± 0.5	50	—	—	1.0	—	1.0		
Input capacitance	C_{IN}	—		—	4	10	—	10	pF		
Power dissipation capacitance	C_{PD}		(Note 2)	—	29	—	—	—	pF		

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

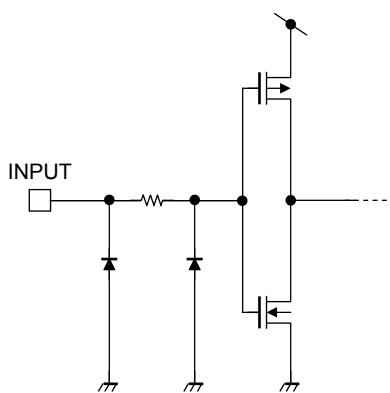
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of flip flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 19 + 10 \cdot n$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			$T_a = 25^\circ C$		Unit
			V_{CC} (V)	Typ.	Max		
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	5.0	0.4	0.8	V	
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	5.0	-0.4	-0.8	V	
Minimum high level dynamic input voltage	V_{IHd}	$C_L = 50$ pF	5.0	—	3.5	V	
Maximum low level dynamic input voltage	V_{ILd}	$C_L = 50$ pF	5.0	—	1.5	V	

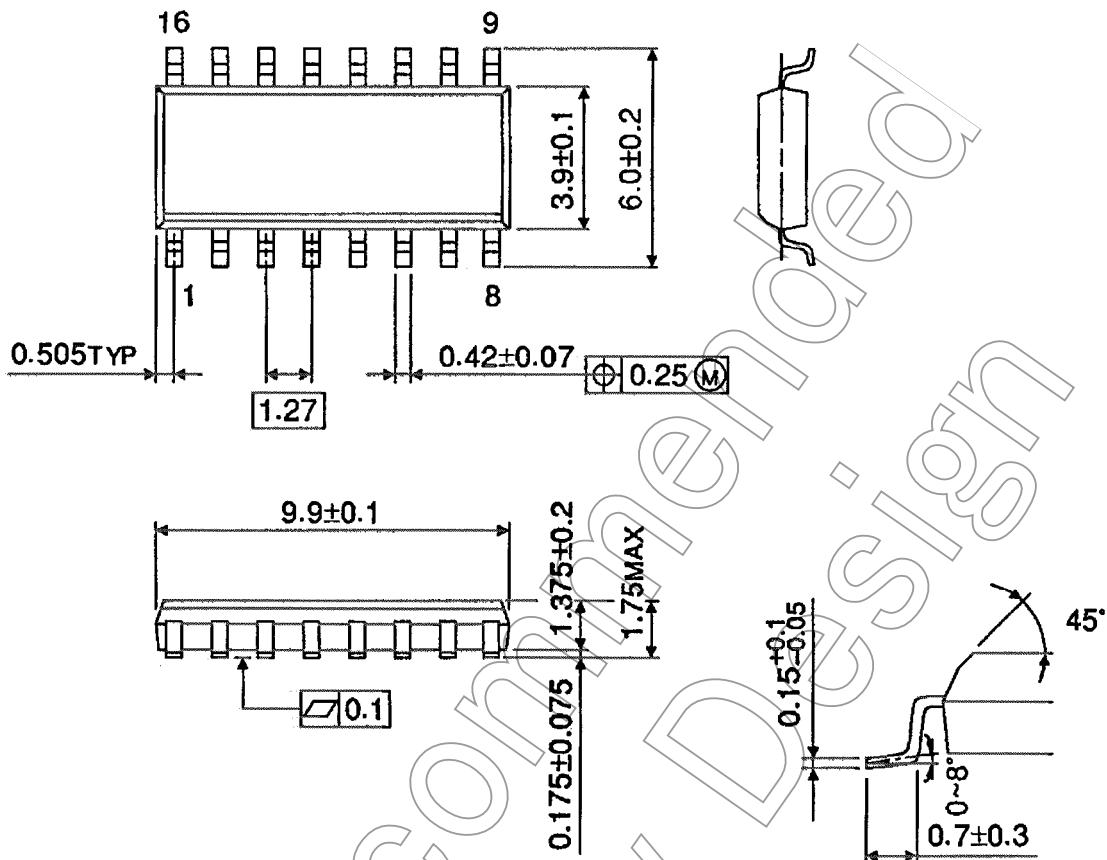
Input Equivalent Circuit

Not Recommended
for New Design

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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