# IXDI509 / IXDN509

## 9 Ampere Low-Side Ultrafast MOSFET Drivers

### Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected up to 9 Amps
- High 9A peak output current
- Wide operating range: 4.5V to 30V
- -55°C to +125°C extended operating temperature
- High capacitive load drive capability: 1800pF in <15ns
- Matched rise and fall times
- Low propagation delay time
- Low output impedance
- Low supply current

### Applications

- Driving MOSFETs and IGBTs
- Motor controls
- Line drivers
- Pulse generators
- Local power ON/OFF switch
- Switch Mode Power Supplies (SMPS)
- DC to DC converters
- Pulse transformer driver
- Class D switching amplifiers
- Power charge pumps

### General Description

The IXDI509 and IXDN509 are high speed high current gate drivers specifically designed to drive the largest IXYS MOSFETs & IGBTs to their minimum switching time and maximum practical frequency limits. The IXDI509 and IXDN509 can source and sink 9 Amps of peak current while producing voltage rise and fall times of less than 30ns. The inputs of the drivers are compatible with TTL or CMOS and are virtually immune to latch up over the entire operating range. Patented* design innovations eliminate cross conduction and current "shoot-through". Improved speed and drive capabilities are further enhanced by matched rise and fall times.

The IXDI509 is configured as a Inverting Gate Driver, and the IXDN509 is configured as a Non-Inverting Gate Driver.

The IXDI509 and IXDN509 are each available in the 8-Pin P-DIP (PI) package, the 8-Pin SOIC (SIA) package, and the 6-Lead DFN (D1) package, (which occupies less than 65% of the board area of the 8-Pin SOIC).

*United States Patent 6,917,227

### Ordering Information

| Part Number | Description | Package Type | Packing Style | Pack Qty | Configuration |
|---|---|---|---|---|---|
| IXDI509PI | 9A Low Side Gate Driver I.C. | 8-Pin PDIP | Tube | 50 | Inverting |
| IXDI509SIA | 9A Low Side Gate Driver I.C. | 8-Pin SOIC | Tube | 94 | |
| IXDI509SIAT/R | 9A Low Side Gate Driver I.C. | 8-Pin SOIC | 13” Tape and Reel | 2500 | |
| IXDI509D1 | 9A Low Side Gate Driver I.C. | 6-Lead DFN | 2” x 2” Waffle Pack | 56 | |
| IXDI509D1T/R | 9A Low Side Gate Driver I.C. | 6-Lead DFN | 13” Tape and Reel | 2500 | |
| IXDN509PI | 9A Low Side Gate Driver I.C. | 8-Pin PDIP | Tube | 50 | Non-Inverting |
| IXDN509SIA | 9A Low Side Gate Driver I.C. | 8-Pin SOIC | Tube | 94 | |
| IXDN509SIAT/R | 9A Low Side Gate Driver I.C. | 8-Pin SOIC | 13” Tape and Reel | 2500 | |
| IXDN509D1 | 9A Low Side Gate Driver I.C. | 6-Lead DFN | 2” x 2” Waffle Pack | 56 | |
| IXDN509D1T/R | 9A Low Side Gate Driver I.C. | 6-Lead DFN | 13” Tape and Reel | 2500 | |

**NOTE:** All parts are lead-free and RoHS Compliant

**Figure 1 - IXDI509 Inverting 9A Gate Driver Functional Block Diagram**

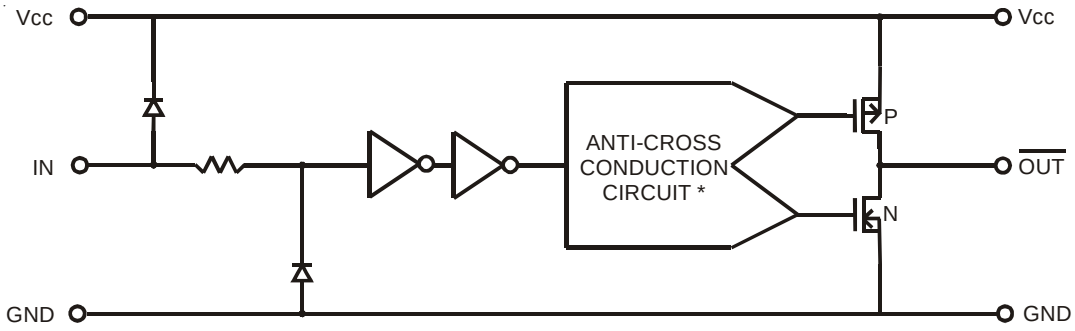
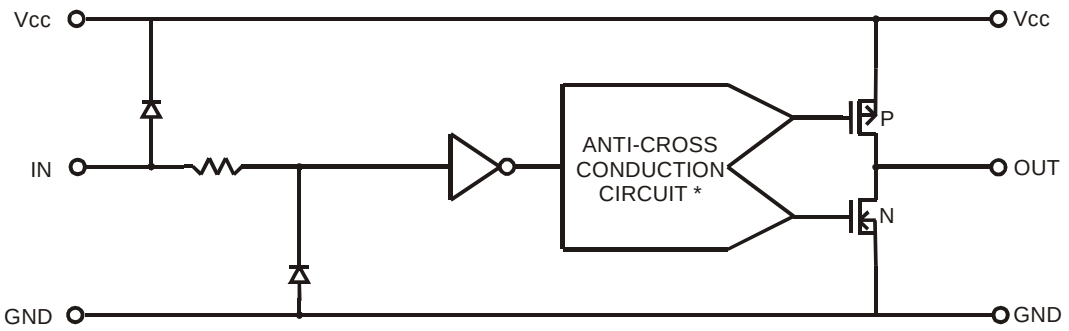



**Figure 2 - IXDN509 Non-Inverting 9A Gate Driver Functional Block Diagram**




*** United States Patent 6,917,227**

## Absolute Maximum Ratings (1)

| Parameter | Value |
|---|---|
| Supply Voltage | 35 V |
| All Other Pins | -0.3 V to $V_{CC}$ + 0.3V |
| Junction Temperature | 150 °C |
| Storage Temperature | -65 °C to 150 °C |
| Lead Temperature (10 Sec) | 300 °C |

## Operating Ratings (2)

| Parameter | | | Value |
|---|---|---|---|
| Operating Supply Voltage | | | 4.5V to 30V |
| Operating Temperature Range | | | -55 °C to 125 °C |
| Package Thermal Resistance * | | | |
| 8-Pin PDIP | (PI) | $\theta_{J-A}$ (typ) | 125 °C/W |
| 8-Pin SOIC | (SIA) | $\theta_{J-A}$ (typ) | 200 °C/W |
| 6-Lead DFN | (D1) | $\theta_{J-A}$ (typ) | 125-200 °C/W |
| 6-Lead DFN | (D1) | $\theta_{J-C}$ (max) | 2.0 °C/W |
| 6-Lead DFN | (D1) | $\theta_{J-S}$ (typ) | 6.3 °C/W |

## Electrical Characteristics @ $T_A$ = 25 °C (3)

Unless otherwise noted, $4.5V \le V_{CC} \le 30V$.
All voltage measurements with respect to GND. IXD_509 configured as described in *Test Conditions*. **(4)**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High input voltage | $4.5V \le V_{CC} \le 18V$ | 2.4 | | | V |
| $V_{IL}$ | Low input voltage | $4.5V \le V_{CC} \le 18V$ | | | 0.8 | V |
| $V_{IN}$ | Input voltage range | | -5 | | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input current | $0V \le V_{IN} \le V_{CC}$ | -10 | | 10 | µA |
| $V_{OH}$ | High output voltage | | $V_{CC}$ - 0.025 | | | V |
| $V_{OL}$ | Low output voltage | | | | 0.025 | V |
| $R_{OH}$ | High state output resistance | $V_{CC}$ = 18V | | 0.6 | 1 | Ω |
| $R_{OL}$ | Low state output resistance | $V_{CC}$ = 18V | | 0.4 | 0.8 | Ω |
| $I_{PEAK}$ | Peak output current | $V_{CC}$ = 15V | | 9 | | A |
| $I_{DC}$ | Continuous output current | Limited by package power dissipation | | | 2 | A |
| $t_R$ | Rise time | $C_{LOAD}$ =10,000pF $V_{CC}$=18V | | 25 | 45 | ns |
| $t_F$ | Fall time | $C_{LOAD}$ =10,000pF $V_{CC}$=18V | | 23 | 40 | ns |
| $t_{ONDLY}$ | On-time propagation delay | $C_{LOAD}$ =10,000pF $V_{CC}$=18V | | 18 | 35 | ns |
| $t_{OFFDLY}$ | Off-time propagation delay | $C_{LOAD}$ =10,000pF $V_{CC}$=18V | | 19 | 30 | ns |
| $V_{CC}$ | Power supply voltage | | 4.5 | 18 | 30 | V |
| $I_{CC}$ | Power supply current | $V_{CC}$ = 18V, $V_{IN}$ =0V | | | 75 | µA |
| | | $V_{IN}$ = 3.5V | | 1 | 3 | mA |
| | | $V_{IN}$ = $V_{CC}$ | | | 75 | mA |

## Electrical Characteristics @ temperatures over -55 °C to 125 °C (3)

Unless otherwise noted, $4.5V \le V_{CC} \le 30V$ , Tj < 150ºC
All voltage measurements with respect to GND. IXD_502 configured as described in *Test Conditions*. All specifications are for one channel. **(4)**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High input voltage | $4.5V \le V_{CC} \le 18V$ | 2.4 | | | V |
| $V_{IL}$ | Low input voltage | $4.5V \le V_{CC} \le 18V$ | | | 0.8 | V |
| $V_{IN}$ | Input voltage range | | -5 | | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input current | $0V \le V_{IN} \le V_{CC}$ | -10 | | 10 | µA |
| $V_{OH}$ | High output voltage | | $V_{CC}$ – 0.025 | | | V |
| $V_{OL}$ | Low output voltage | | | | 0.025 | V |
| $R_{OH}$ | High state output resistance | $V_{CC}$ = 18V | | | 2 | Ω |
| $R_{OL}$ | Low state output resistance | $V_{CC}$ = 18V | | | 1.5 | Ω |
| $I_{DC}$ | Continuous output current | | | | 1 | A |
| $t_R$ | Rise time | $C_{LOAD}$ =10,000pF $V_{CC}$ =18V | | | 60 | ns |
| $t_F$ | Fall time | $C_{LOAD}$ =10,000pF $V_{CC}$ =18V | | | 60 | ns |
| $t_{ONDLY}$ | On-time propagation delay | $C_{LOAD}$ =10,000pF $V_{CC}$ =18V | | | 55 | ns |
| $t_{OFFDLY}$ | Off-time propagation delay | $C_{LOAD}$ =10,000pF $V_{CC}$ =18V | | | 40 | ns |
| $V_{CC}$ | Power supply voltage | | 4.5 | 18 | 30 | V |
| $I_{CC}$ | Power supply current | $V_{CC}$ =18V, $V_{IN}$ = 0V | | | 0.13 | µA |
| | | $V_{IN}$ = 3.5V | | | 3 | mA |
| | | $V_{IN}$ = $V_{CC}$ | | | 0.13 | mA |

**Notes:**

1. Operating the device beyond the parameters listed as “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The device is not intended to be operated outside of the Operating Ratings.
3. Electrical Characteristics provided are associated with the stated Test Conditions.
4. Typical values are presented in order to communicate how the device is expected to perform, but not necessarily to highlight any specific performance limits within which the device is guaranteed to function.

***** The following notes are meant to define the conditions for the $\theta_{J-A}$, $\theta_{J-C}$ and $\theta_{J-S}$ values:

1) The $\theta_{J-A}$ (typ) is defined as junction to ambient. The $\theta_{J-A}$ of the standard single die 8-Lead PDIP and 8-Lead SOIC are dominated by the resistance of the package, and the IXD_5XX are typical. The values for these packages are natural convection values with vertical boards and the values would be lower with forced convection. For the 6-Lead DFN package, the $\theta_{J-A}$ value supposes the DFN package is soldered on a PCB. The $\theta_{J-A}$ (typ) is 200 °C/W with no special provisions on the PCB, but because the center pad provides a low thermal resistance to the die, it is easy to reduce the $\theta_{J-A}$ by adding connected copper pads or traces on the PCB. These can reduce the $\theta_{J-A}$ (typ) to 125 °C/W easily, and potentially even lower. The $\theta_{J-A}$ for DFN on PCB without heatsink or thermal management will vary significantly with size, construction, layout, materials, etc. This typical range tells the user what he is likely to get if he does no thermal management.

2) $\theta_{J-C}$ (max) is defined as juction to case, where case is the large pad on the back of the DFN package. The $\theta_{J-C}$ values are generally not published for the PDIP and SOIC packages. The $\theta_{J-C}$ for the DFN packages are important to show the low thermal resistance from junction to the die attach pad on the back of the DFN, -- and a guardband has been added to be safe.

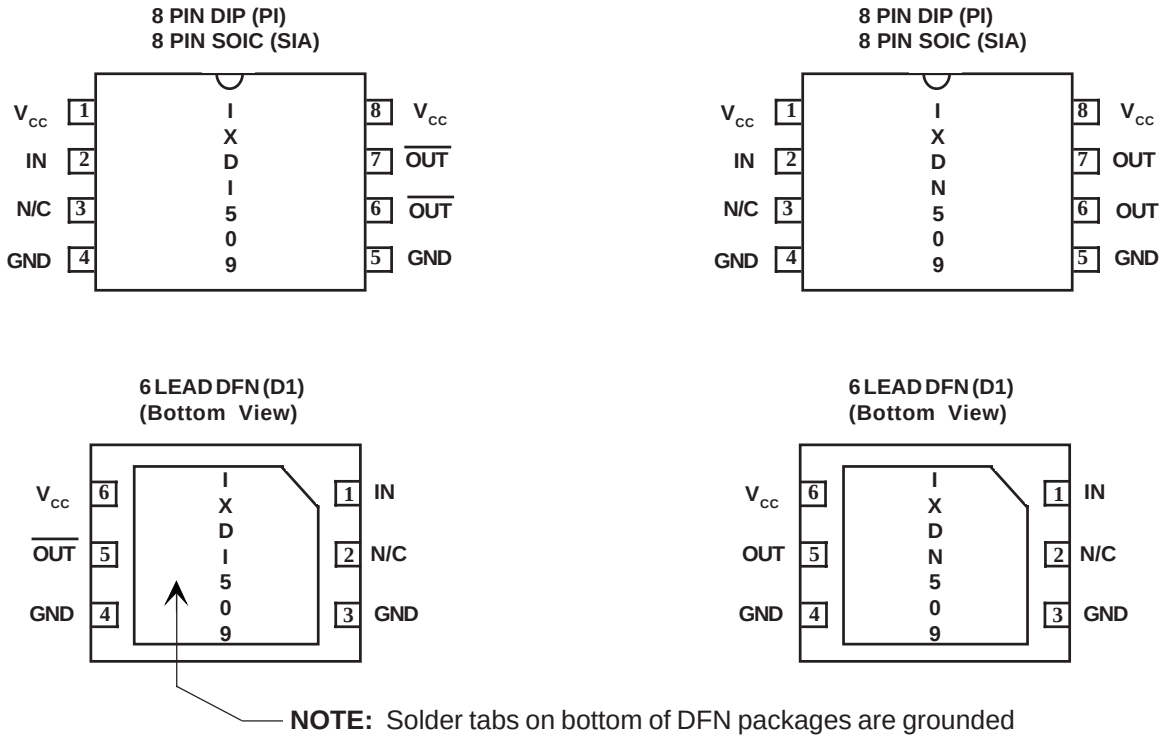
3) The $\theta_{J-S}$ (typ) is defined as junction to heatsink, where the DFN package is soldered to a thermal substrate that is mounted on a heatsink. The value must be typical because there are a variety of thermal substrates. This value was calculated based on easily available IMS in the U.S. or Europe, and not a premium Japanese IMS. A 4 mil dialectric with a thermal conductivity of 2.2W/mC was assumed. The result was given as typical, and indicates what a user would expect on a typical IMS substrate, and shows the potential low thermal resistance for the DFN package.

## Pin Description

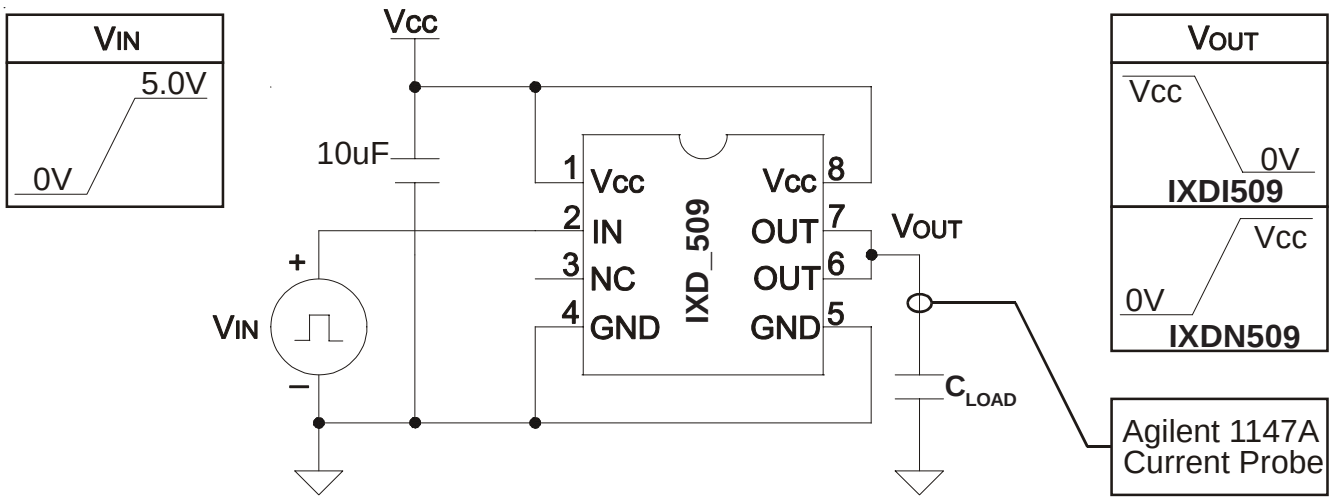
| PIN | SYMBOL | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1, 8 | $V_{CC}$ | Supply Voltage | Power supply input voltage. These pins provide power to the entire device. The range for this voltage is 4.5V to 30V. |
| 2 | IN | Input | Input drive signal, TTL or CMOS compatible. |
| 6, 7 | OUT | Output | Driver output. For application purposes, these pins are connected, through a resistor, to the gate of a MOSFET/IGBT. |
| 4, 6 | GND | Ground | The device ground pins. Internally connected to all circuitry, these pins provide ground reference for the entire chip and should be connected to a low noise analog ground plane for optimum performance. |

**CAUTION: Follow proper ESD procedures when handling and assembling this component.**

## Pin Configurations

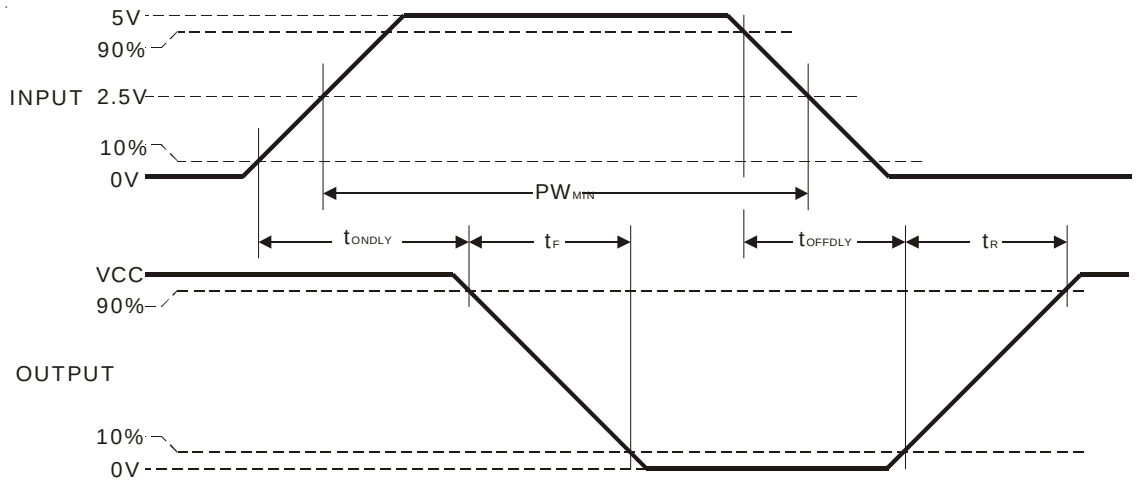



## Figure 3 - Characteristics Test Diagram

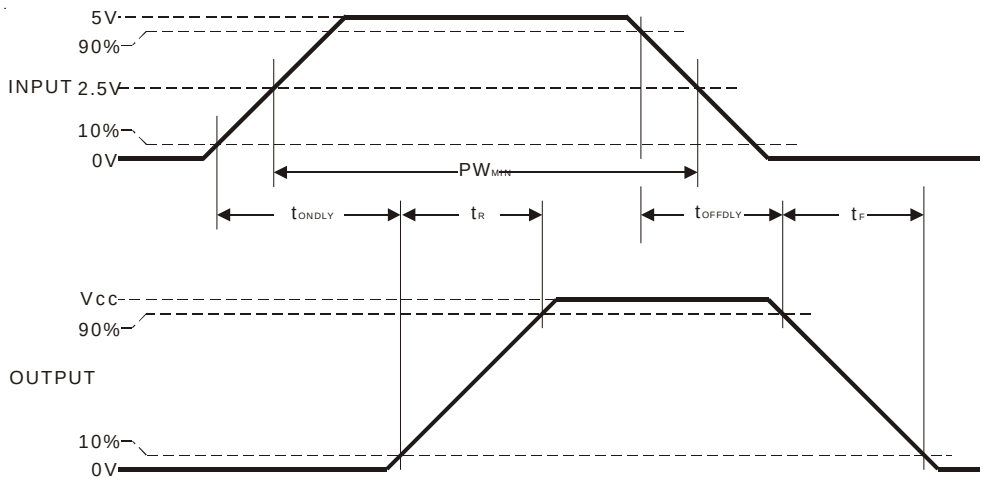


## Figure 4 - Timing Diagrams

### Inverting (IXDI509) Timing Diagram




### Non-Inverting (IXDN509) Timing Diagram



## Typical Performance Characteristics

Fig. 5

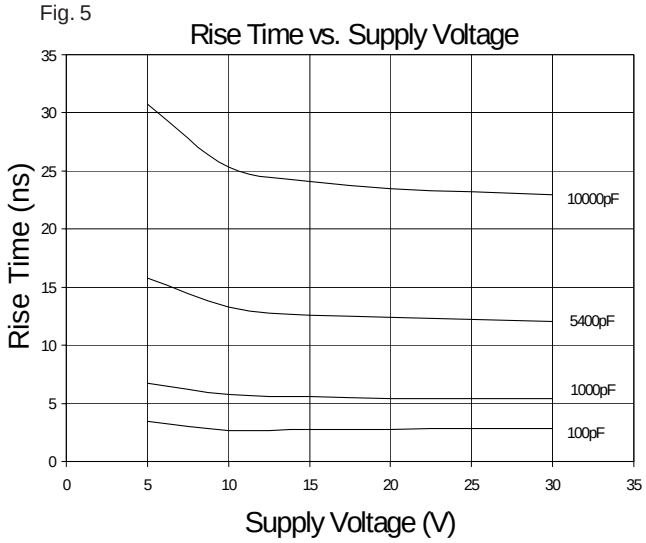



Fig. 6

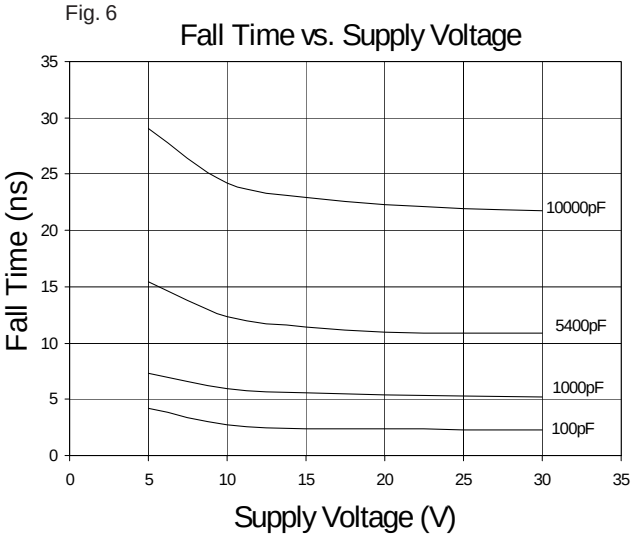



Fig. 7

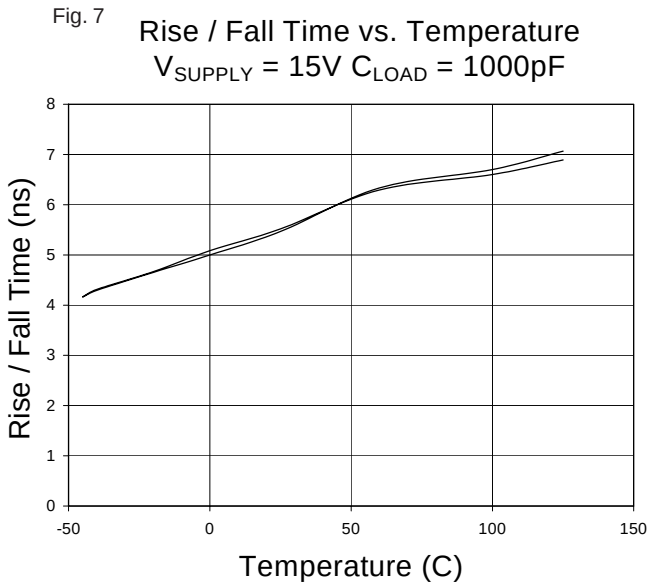



Fig. 8

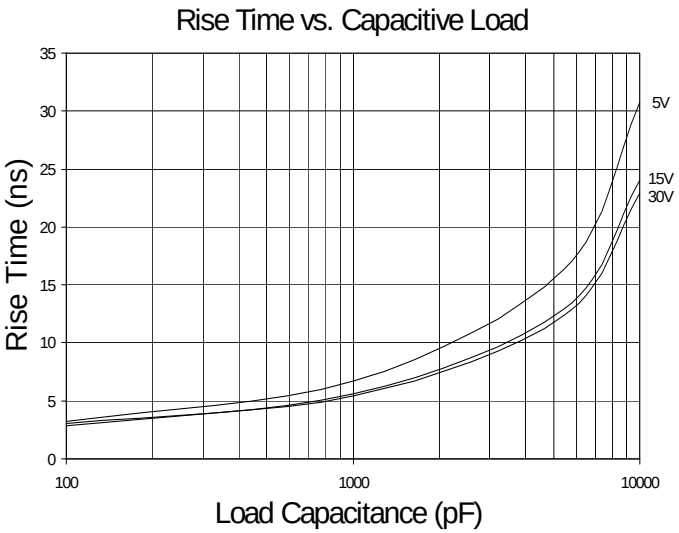



Fig. 9

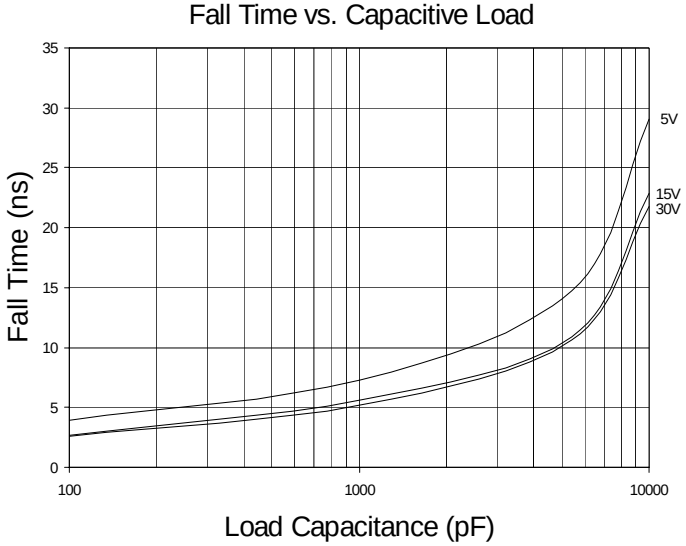



Fig. 10

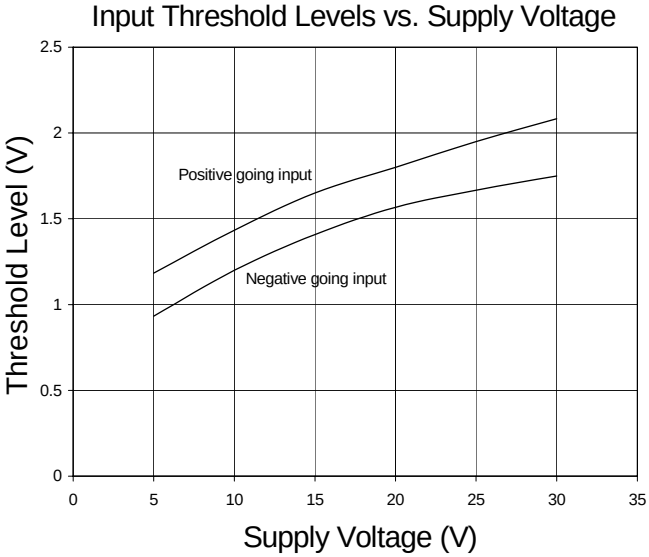


Fig. 11

Input Threshold Levels vs. Temperature
$V_{SUPPLY}$ = 15V

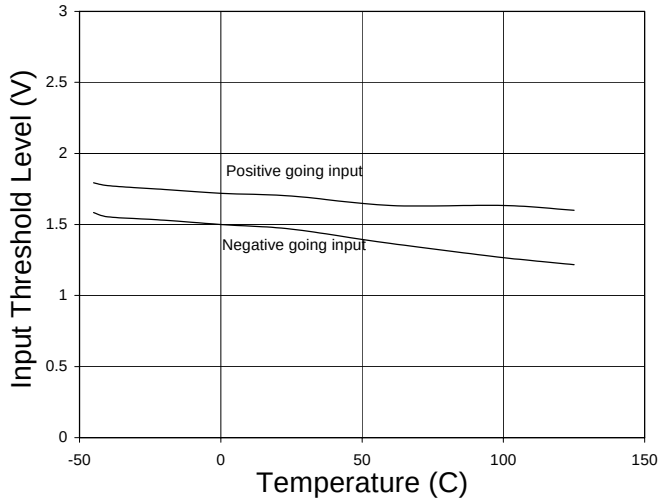



Fig. 12

Propagation Delay vs. Supply Voltage
Rising Input, $C_{LOAD}$ = 1000pF

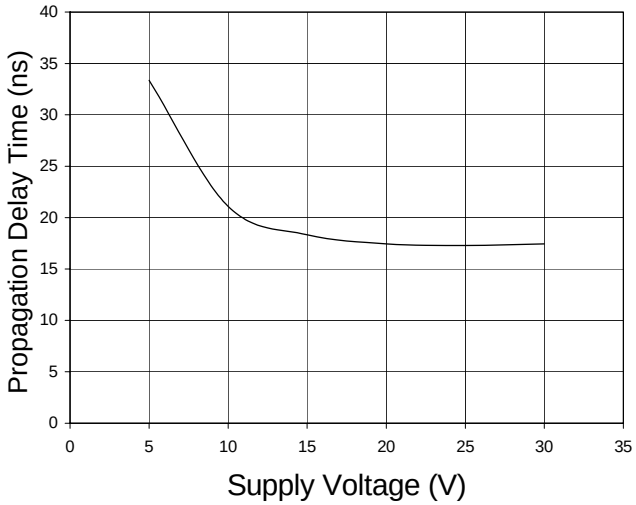



Fig. 13

Propagation Delay vs. Supply Voltage
Falling Input, $C_{LOAD}$ = 1000pF

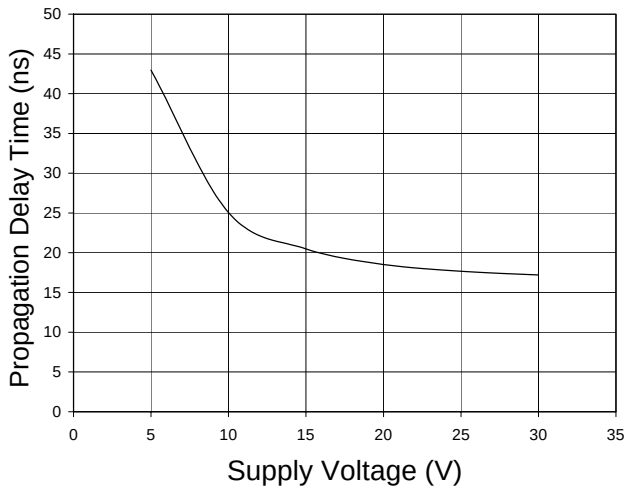



Fig. 14

Propagation Delay vs. Temperature
$V_{SUPPLY}$ = 15V $C_{LOAD}$ = 1000pF

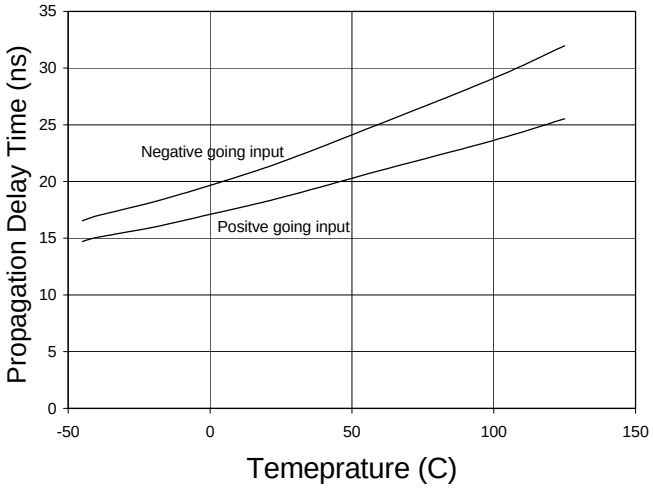



Fig. 15

Quiescent Current vs. Supply Voltage

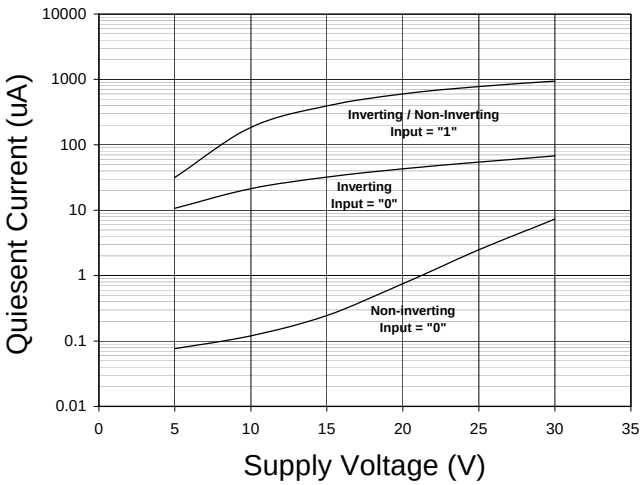



Fig. 16

Quiescent Current vs. Temperature
$V_{SUPPLY}$ = 15V

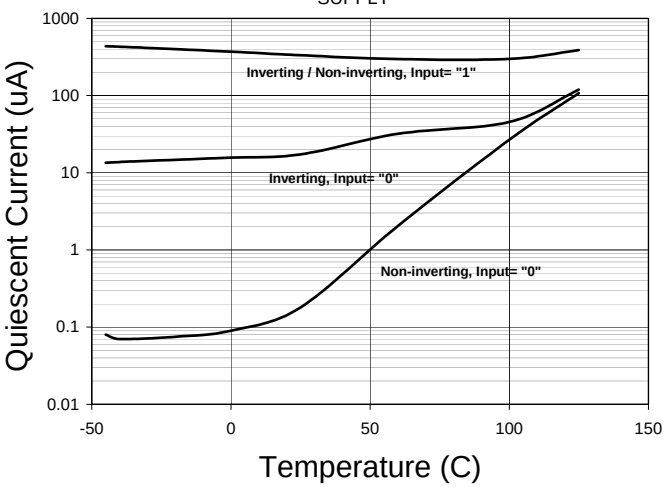


Fig. 17 Supply Current vs. Capacitive Load
$V_{SUPPLY}$ = 5V

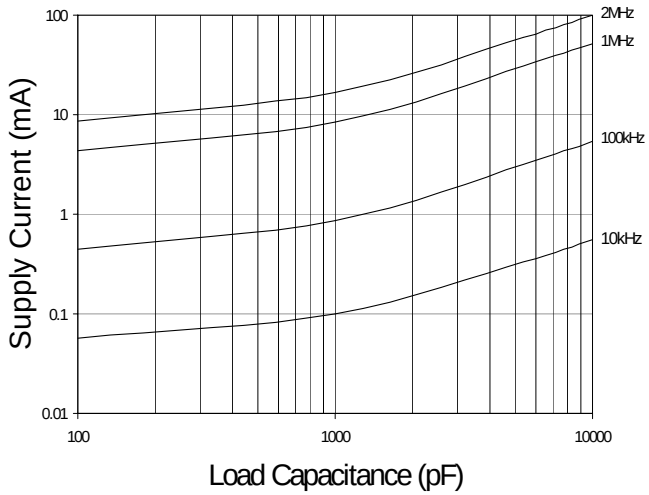



Fig. 18 Supply Current vs. Frequency
$V_{SUPPLY}$ = 5V

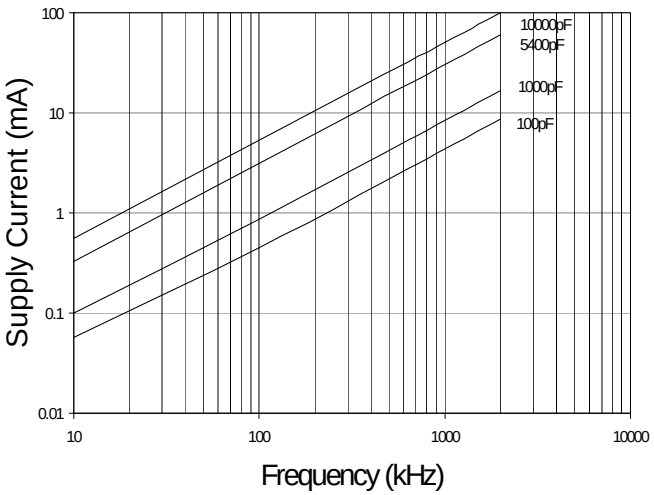



Fig. 19 Supply Current vs. Capacitive Load
$V_{SUPPLY}$ = 15V

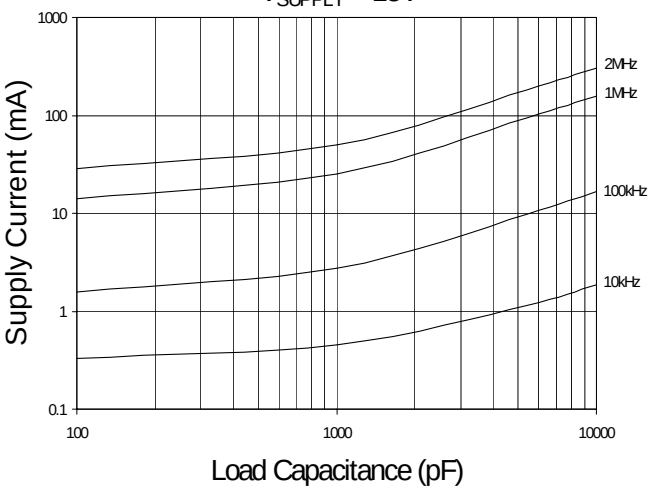



Fig. 20 Supply Current vs. Frequency
$V_{SUPPLY}$ = 15V

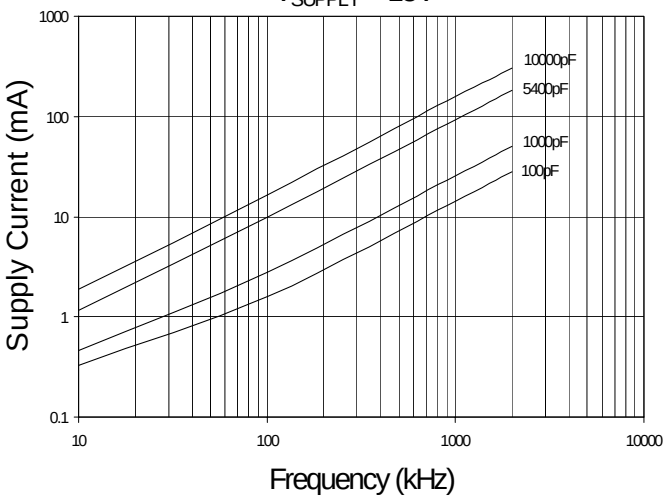



Fig. 21 Supply Current vs. Capacitive Load
$V_{SUPPLY}$ = 30V

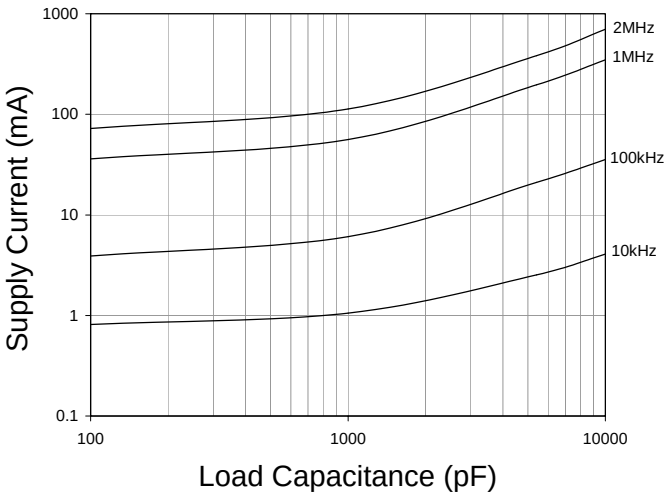



Fig. 22 Supply Current vs. Frequency
$V_{SUPPLY}$ = 30V

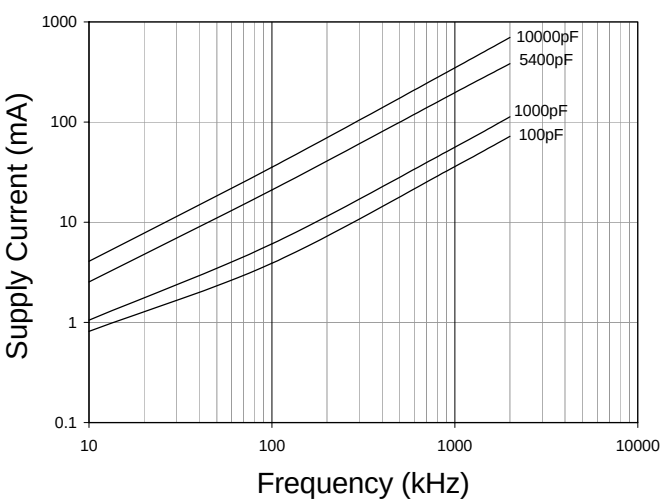


Fig. 23

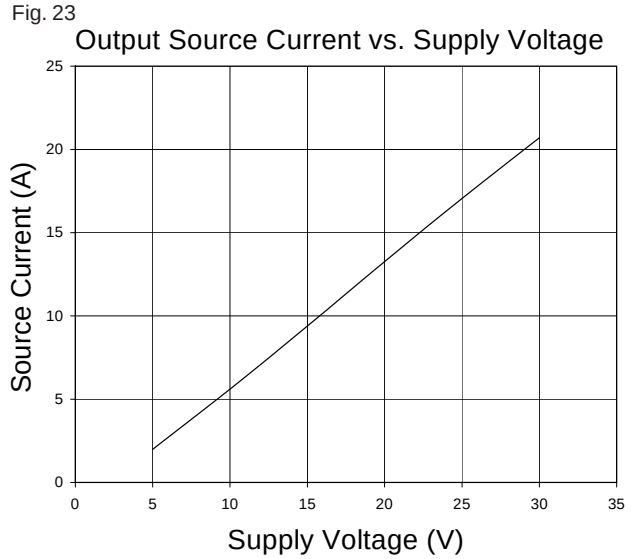



Fig. 24

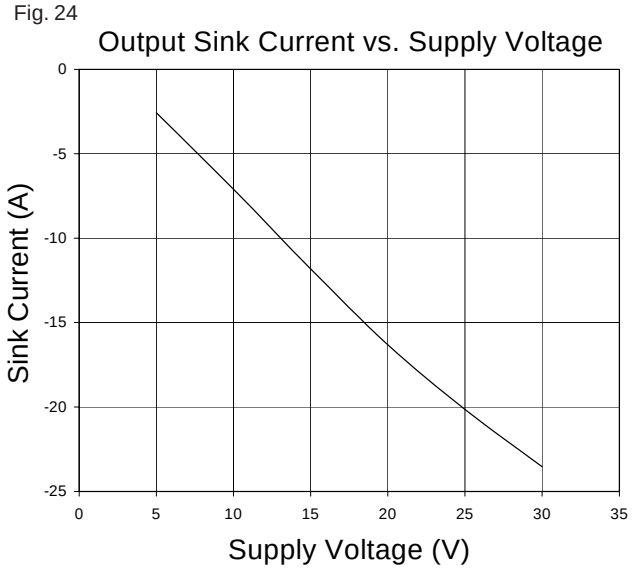



Fig. 25

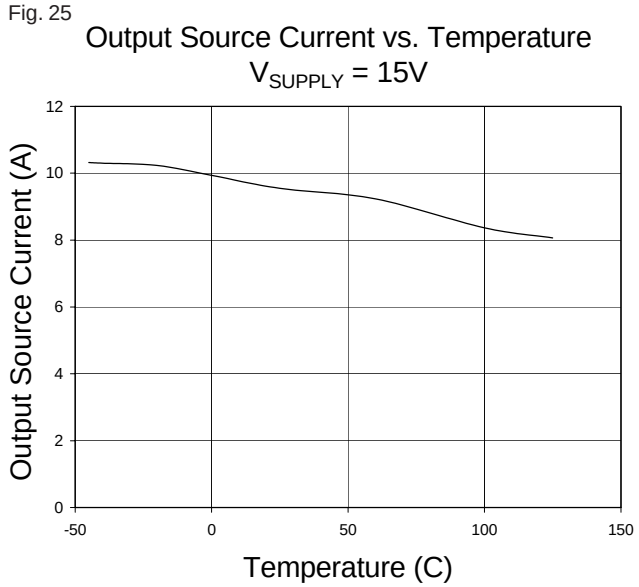



Fig. 26

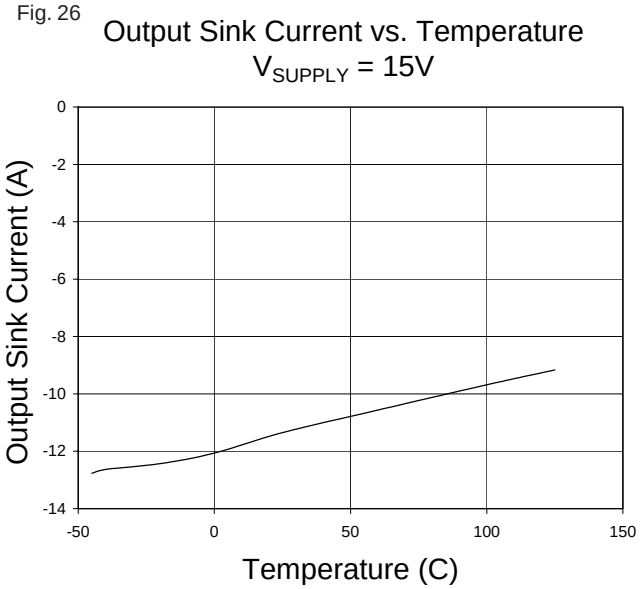



Fig. 27

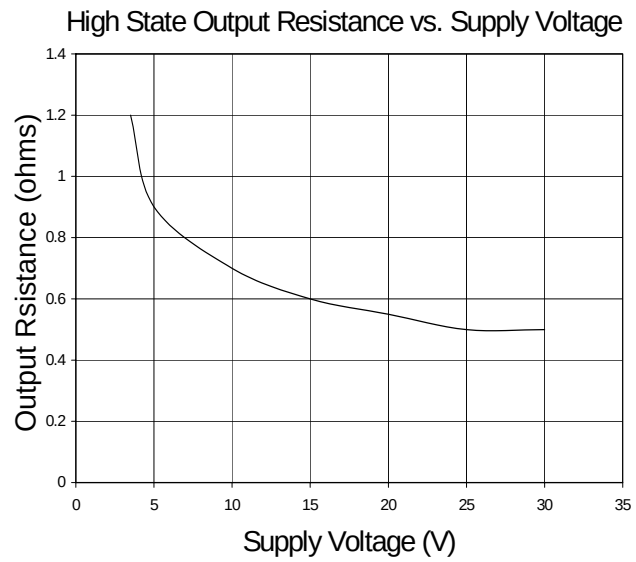
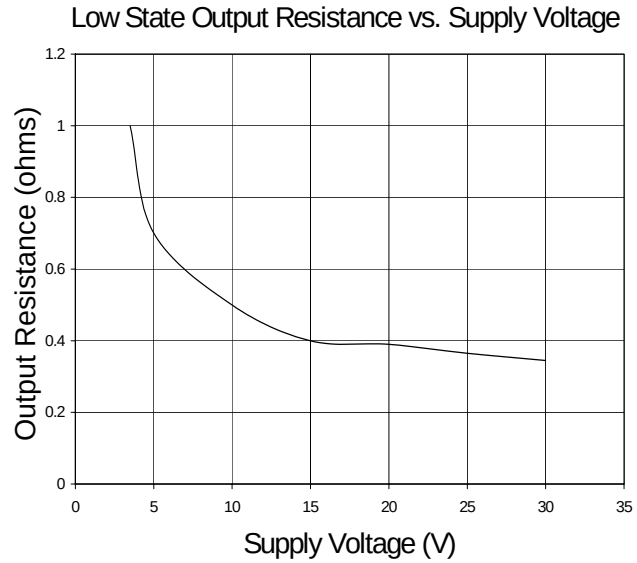



Fig. 28



## Supply Bypassing, Grounding Practices And Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXD_509, it is very important to observe certain design criteria in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXD_509 to charge a 5000pF capacitive load from 0 to 25 volts in 25ns.

Using the formula: $I_C=C(\Delta V/\Delta t)$, where $\Delta V=25V$ $C=5000pF$ & $\Delta t=25ns$, we can determine that to charge 5000pF to 25 volts in 25ns will take a constant current of 5A. (In reality, the charging current won't be constant, and will peak somewhere around 8A).

**SUPPLY BYPASSING**

In order for our design to turn the load on properly, the IXD_509 must be able to draw this 5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is an order of magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected and should have low inductance, low resistance and high-pulse current-service ratings). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXD_509 to an absolute minimum.

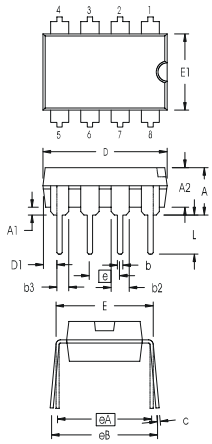
**GROUNDING**

In order for the design to turn the load off properly, the IXD_509 must be able to drain this 5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXD_509 and its load. Path #2 is between the IXD_509 and its power supply. Path #3 is between the IXD_509 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXD_509.

**OUTPUT LEAD INDUCTANCE**

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible. If the driver must be placed farther than 0.2" (5mm) from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connected directly to the ground terminal of the load.

| REV | DATE | ECN NO | DESCRIPTION | APR |
|---|---|---|---|---|
| | | | | |

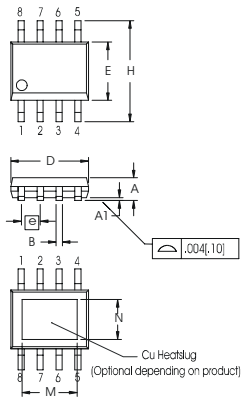



| SYM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .140 | .180 | 3.56 | 4.57 |
| A1 | .015 | .040 | 0.38 | 1.02 |
| A2 | .125 | .145 | 3.18 | 3.68 |
| b | .015 | .020 | 0.38 | 0.51 |
| b2 | .055 | .065 | 1.40 | 1.65 |
| b3 | .035 | .045 | 0.89 | 1.14 |
| c | .009 | .012 | 0.23 | 0.30 |
| D | .355 | .400 | 9.02 | 10.16 |
| D1 | .010 | .040 | 0.25 | 1.02 |
| E | .300 | .325 | 7.62 | 8.26 |
| E1 | .240 | .270 | 6.10 | 6.86 |
| e | .100 BSC | | 2.54 BSC | |
| eA | .300 BSC | | 7.62 BSC | |
| eB | .300 | .430 | 7.62 | 10.92 |
| L | .120 | .140 | 3.05 | 3.56 |

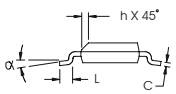
NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 BA.

| IXYS Corp 3540 Bassett St, Santa Clara, CA 95054 | TOLERANCE Unless Otherwise Specified .X=+/-.05 .XX=+/-.005 .XX=+/-.01 ANGLE=+/-5 | DATE: 8/18/94 | DWN: K. R. Choi | TITLE: CASE OUTLINE OF 8 LEAD 0.3"W P-DIP | DRAWING NO: CO 0035 | REV: 0 |
|---|---|---|---|---|---|---|
| | | UNIT: INCH [MM] | APR: | | | |
| | | SACLE: 4 X | APR: | | | |

| REV | DATE | ECN NO | DESCRIPTION | APR |
|---|---|---|---|---|
| A | 3/08/2 | | Added bottom heatslug dimension. | K. R. Choi |



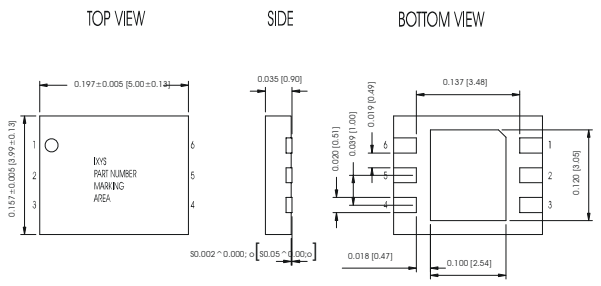

| SYM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .053 | .069 | 1.35 | 1.75 |
| A1 | .004 | .010 | 0.10 | 0.25 |
| B | .013 | .020 | 0.33 | 0.51 |
| C | .008 | .010 | 0.19 | 0.25 |
| D | .189 | .197 | 4.80 | 5.00 |
| E | .150 | .157 | 3.80 | 4.00 |
| e | .050 BSC | | 1.27 BSC | |
| H | .228 | .244 | 5.80 | 6.20 |
| h | .010 | .020 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| M | .135 | .155 | 3.43 | 3.94 |
| N | .095 | .115 | 2.41 | 2.92 |
| α | 0° | 8° | 0° | 8° |




NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

| IXYS Corp 3540 Bassett St, Santa Clara, CA 95054 | TOLERANCE Unless Otherwise Specified .X=+/-.05 .XX=+/-.005 .XX=+/-.01 ANGLE=+/-5 | DATE: 1/24/95 | DWN: K. R. Choi | TITLE: CASE OUTLINE SOP-8 (.150"W) | DRAWING NO: CO 0044 | REV: A |
|---|---|---|---|---|---|---|
| | | UNIT: INCH [MM] | APR: | | | |
| | | SCALE: 5X | APR: | | | |

| REV | DATE | ECN NO | DESCRIPTION | APPROVAL |
|---|---|---|---|---|
| A | 5/31/05 | | Changed thickness from max 0.030[0.75] to max 0.035[0.90]. | K. R. Choi |




| IXYS Corporation | TOLERANCE Unless Otherwise Specified | DATE: 4/20/06 | DWN: K. R. Choi | MATERIAL: | TITLE: CASE OUTLINE 6 LEAD DFN (4 X 5 MM) (DRIVER CHIP) | DRAWING NO: CO 0215 | REV: A |
|---|---|---|---|---|---|---|---|
| | | UNIT: inch [mm] | APR: | | | | |
| | | SCALE: 10 X | APR: | | | SHEET NO: 1 OF 1 | |

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