

# Signetics

## Integrated Circuits – Low Power Schottky TTL

### 74LS Series – Low Power Schottky TTL

#### INTRODUCTION

Low Power Schottky TTL offers the same speed as Standard TTL at 1/5 the power. The power savings and LSI potential result in Low Power Schottky being the preferred range in most new system designs. The series offers gate propagation delays of typically 10ns at 2 mW (1/5 of standard 74 series power). Flip Flop Toggle rate of 30 MHz and MSI 4-Bit Add Time of 21ns.

Care must be taken however when designing in 74LS as follows:

- Check the fan-out requirements at each output node where a 74LS device may have to drive a 74 device. Do not exceed five 7400 loads.
- Check the system set-up and hold times for sequential functions to ensure that data is available at the correct time for Low-Power Schottky functions. For 74LS these specifications sometimes differ slightly from those of the corresponding 74 type.
- Use standard 74 where necessary to drive capacitive loads greater than about 100 pF.

74LS does offer the following benefits when upgrading standard 74 series to 74LS:

- Elimination of heating problems in systems such as terminals, point-of-sale systems, etc. in which it is necessary to put a lot of logic in a small package. Simply plugging in 74LS cuts heat generation dramatically.
- Reduced power supply cost.
- Possibility of upgrading system capability by adding plug-in logic boards without having to redesign the power supply.

#### MAXIMUM RATINGS

Supply Voltage,  $V_{CC}$  7.0V  
 Input Voltage,  $V_{IN}$  7.0V  
 Inter Emitter Voltage 5.5V  
 Operating Temperature  $T_A$  0 to +70°C  
 Storage Temperature  $T_S$  -65 to +150°C  
 Short Circuit Output Current,  $I_{OS}$  -15 to -100 mA  
 DC Noise Margin Logic '1' 0.5V  
 Logic '0' 0.3V

#### REFERENCE TABLE

TYPE NO.	DESCRIPTION	STOCK NO.	OUTLINE DRWG. NO.	CONNECTION DIAG. NO.
N74LS00N	Quad 2-Input NAND Gate	55645E	1	B1
N74LS01N	Quad 2-Input NAND Gate with o/c	55646C	1	B2
N74LS02N	Quad 2-Input NOR Gate	55647A	1	B3
N74LS03N	Quad 2-Input NAND Gate with o/c	55648X	1	B4
N74LS04N	Hex Inverter	55649H	1	B5
N74LS05N	Hex Inverter with o/c	55650X	1	B6
N74LS07N	Hex Buffer/Driver with o/c	55651R	1	B8
N74LS08N	Quad 2-Input AND Gate	55652G	1	B9
N74LS09N	Quad 2-Input AND Gate with o/c	55653E	1	B10
N74LS10N	Triple 3-Input NAND Gate	55654C	1	B11
N74LS11N	Triple 3-Input NAND Gate	55655A	1	B12
N74LS12N	Triple 3-Input NAND Gate with o/c	55656X	1	B13
N74LS13N	Dual NAND Schmitt Trigger	55657H	1	B14
N74LS14N	Hex Schmitt Trigger	55658F	1	B15
N74LS15N	Triple 3-Input AND Gate with o/c	55659D	1	B175
N74LS20N	Dual 4-Input NAND Gate	55660G	1	B19
N74LS21N	Dual 4-Input AND Gate	55661E	1	B20
N74LS22N	Dual 4-Input NAND Gate with o/c	55662C	1	B217
N74LS26N	Quad 2-Input NAND Gate with o/c	55663A	1	B22
N74LS27N	Triple 3-Input NOR Gate	55664X	1	B23
N74LS28N	Quad 2-Input NOR Buffer	55665H	1	B24
N74LS30N	8-Input NAND Gate	55666F	1	B25
N74LS32N	Quad 2-Input OR Gate	55667D	1	B26
N74LS33N	Quad 2-Input NOR Buffer	55668B	1	B27
N74LS37N	Quad 2-Input NAND Buffer	55669X	1	B28
N74LS38N	Quad 2-Input NAND Buffer with o/c	55670C	1	B29
N74LS40N	Dual 4-Input NAND Buffer	55671A	1	B30
N74LS42N	BCD-to-Decimal Decoder	55672X	2	B31



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## Outline Drawings



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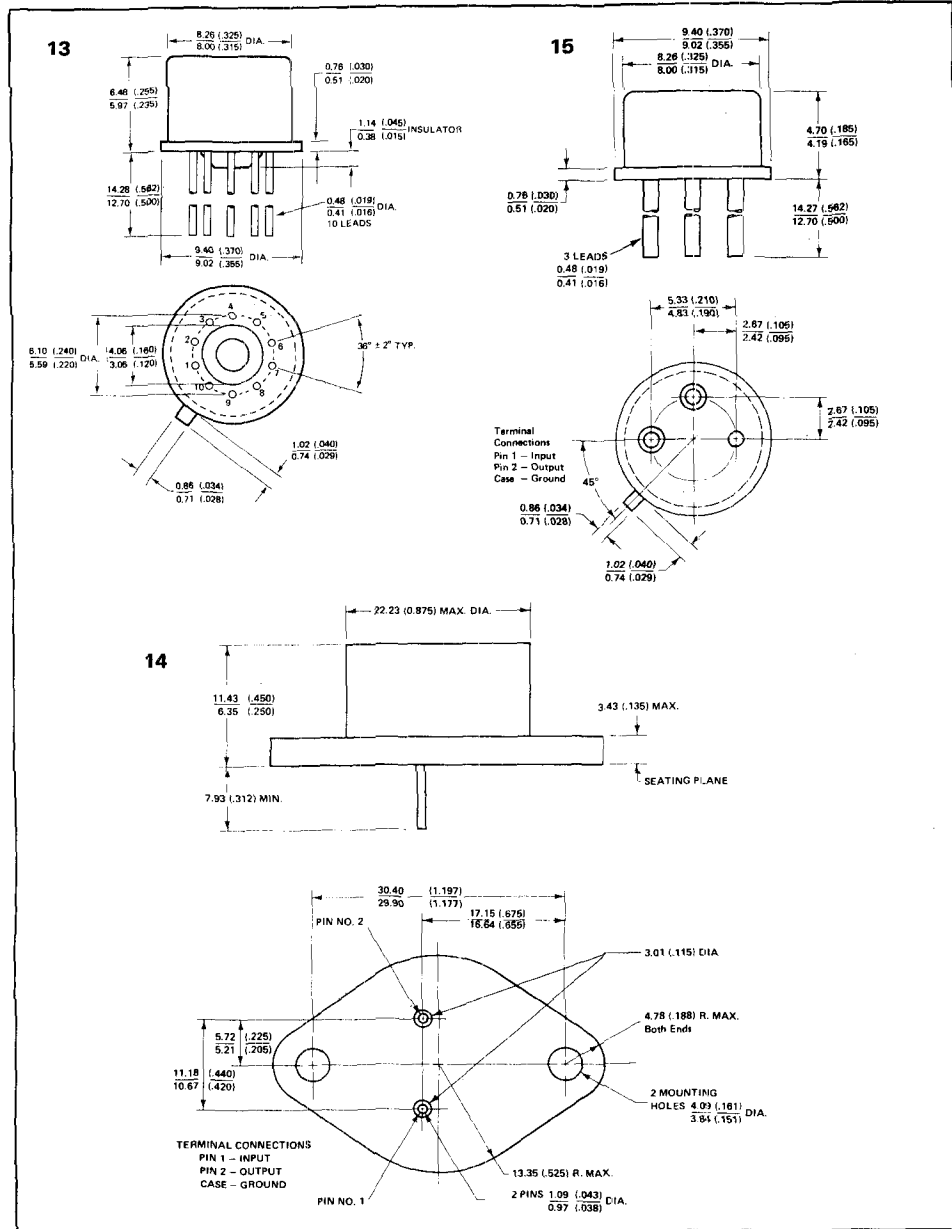


PLEASE QUOTE STOCK NO.  
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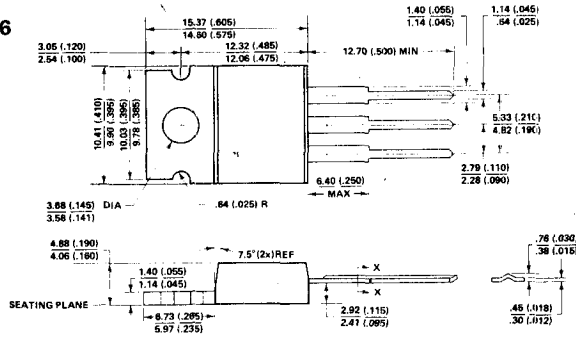
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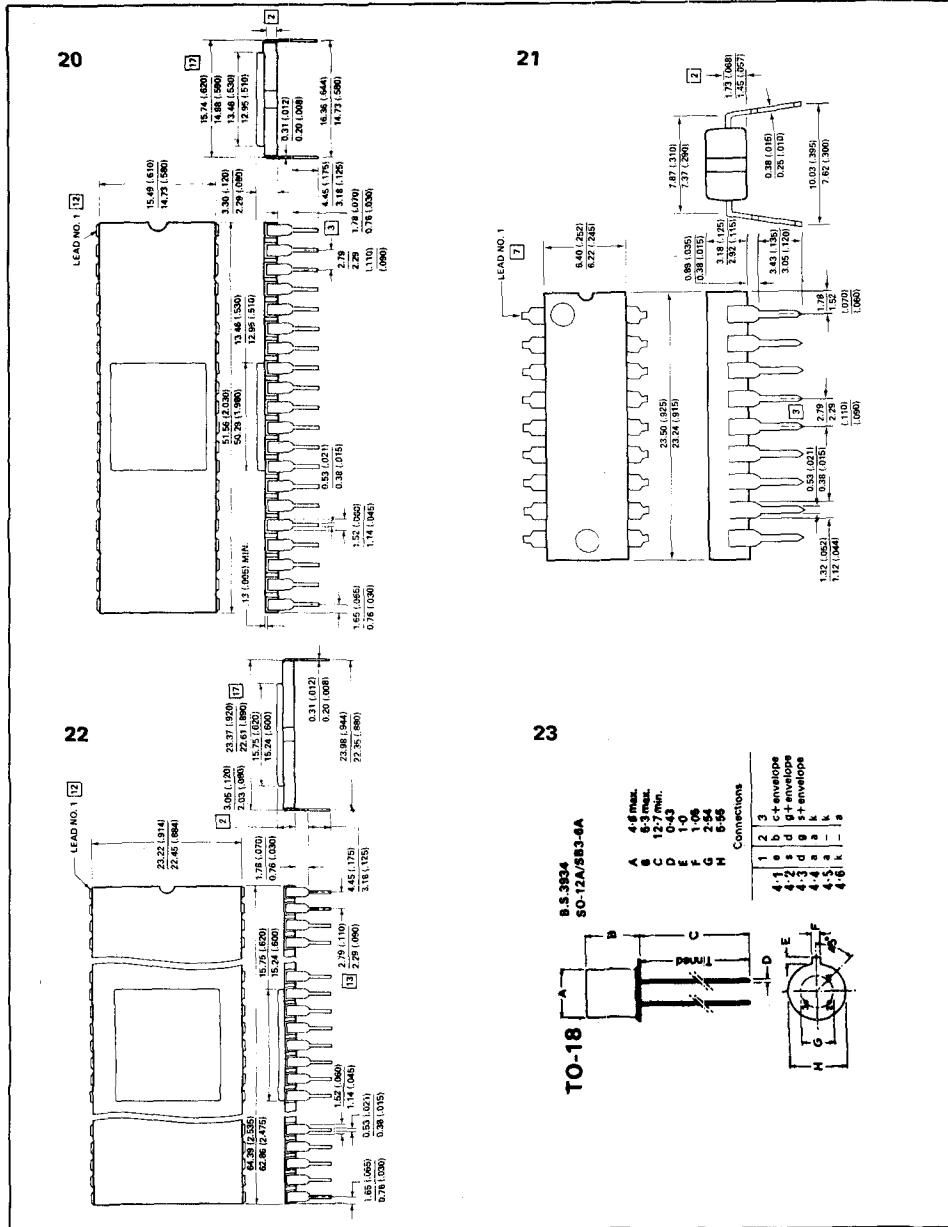


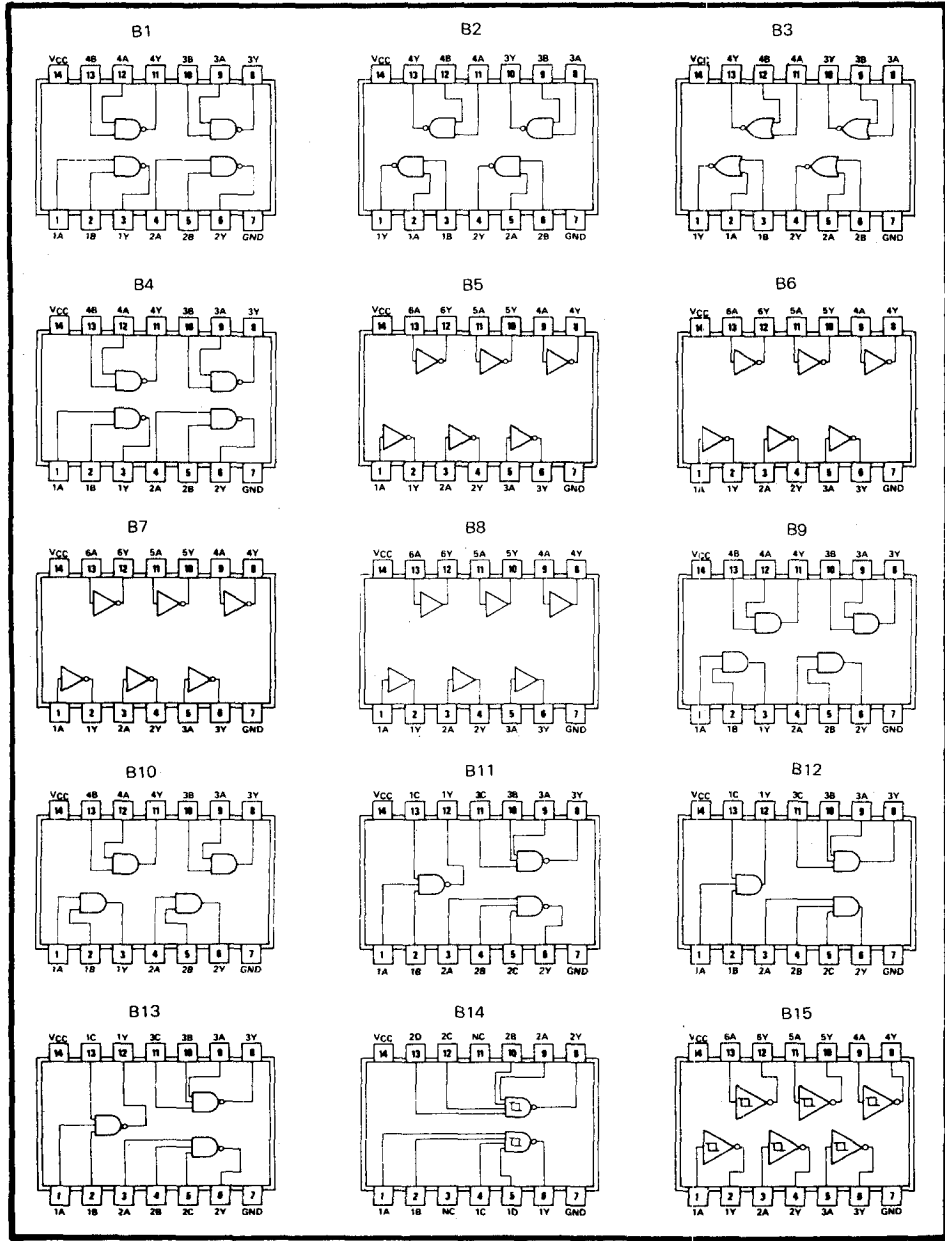
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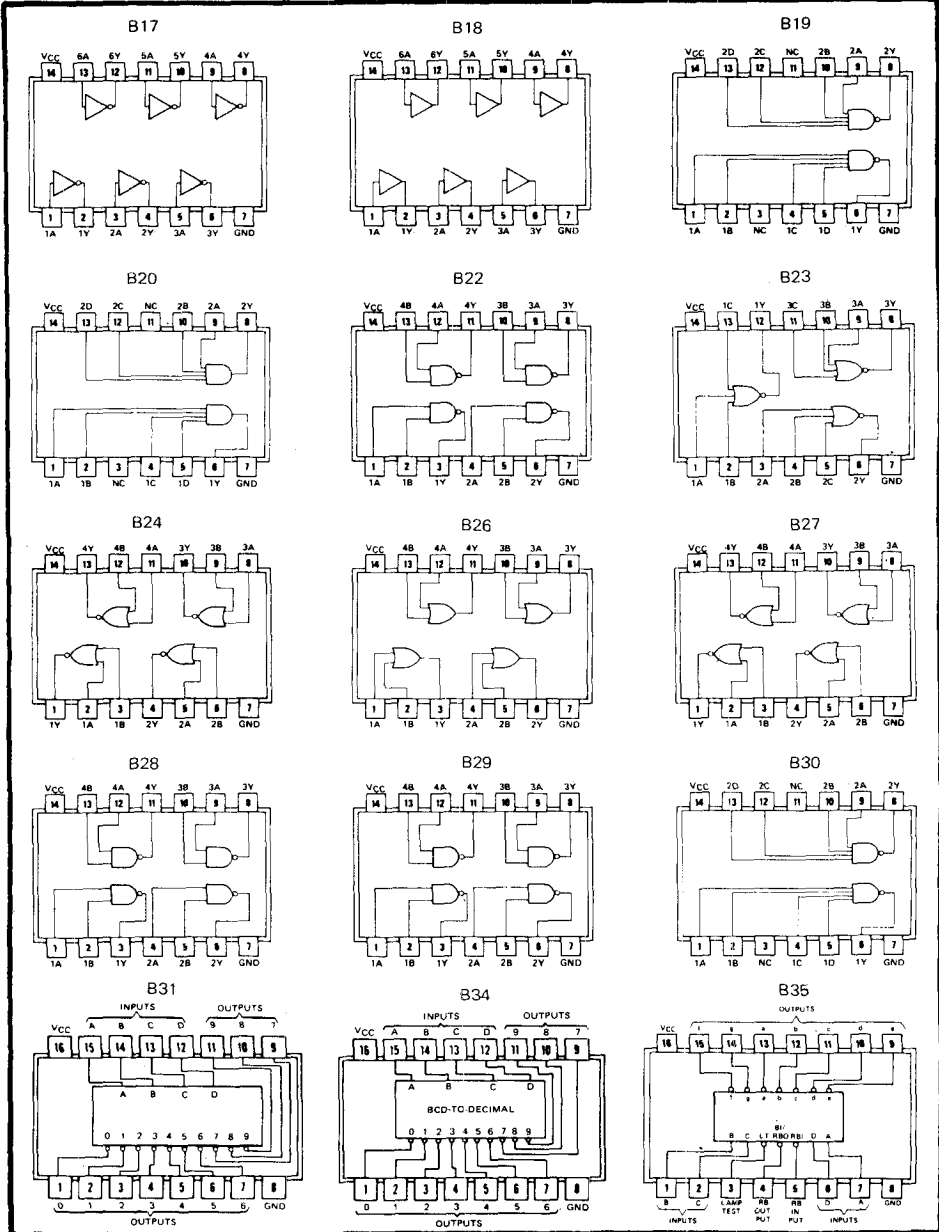
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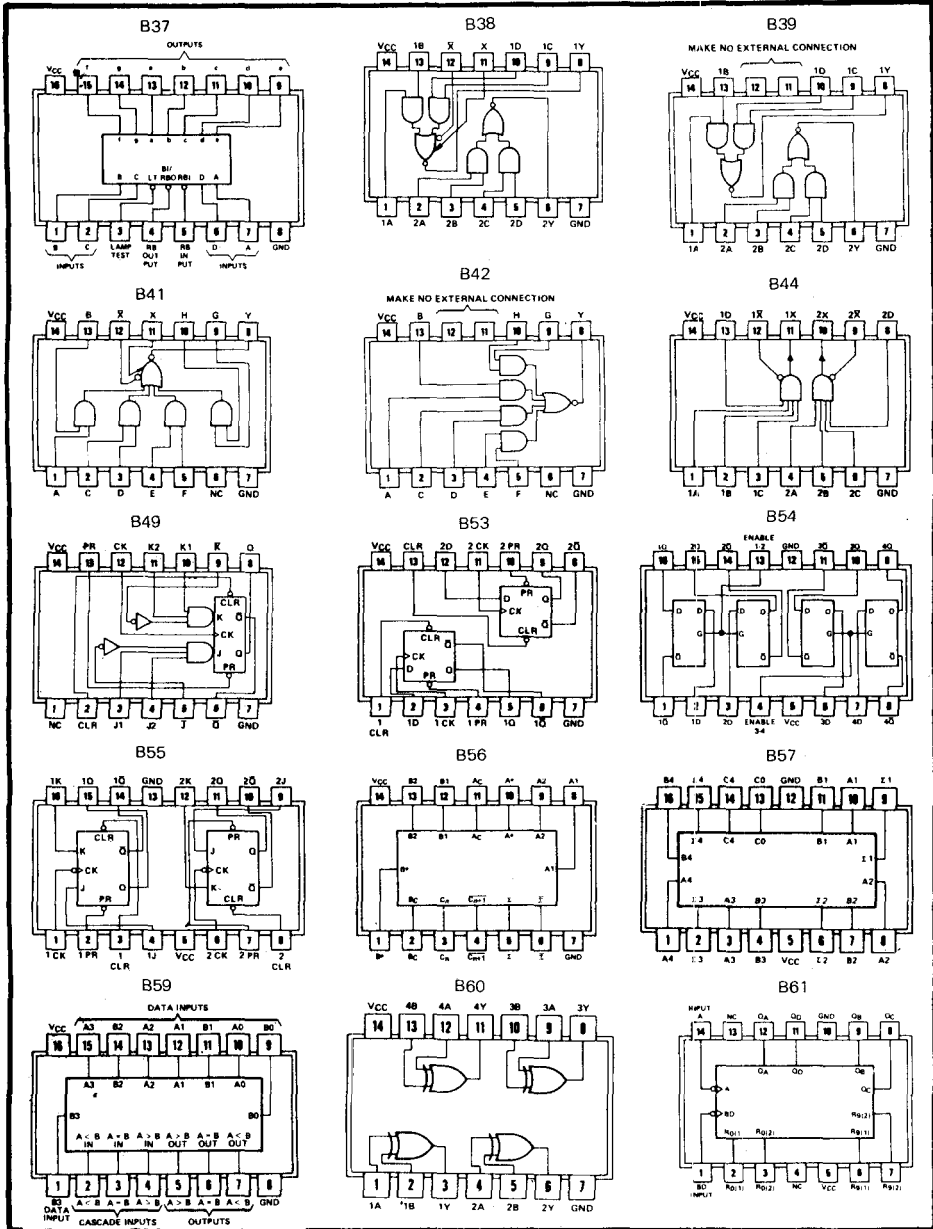
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## Connection Diagram



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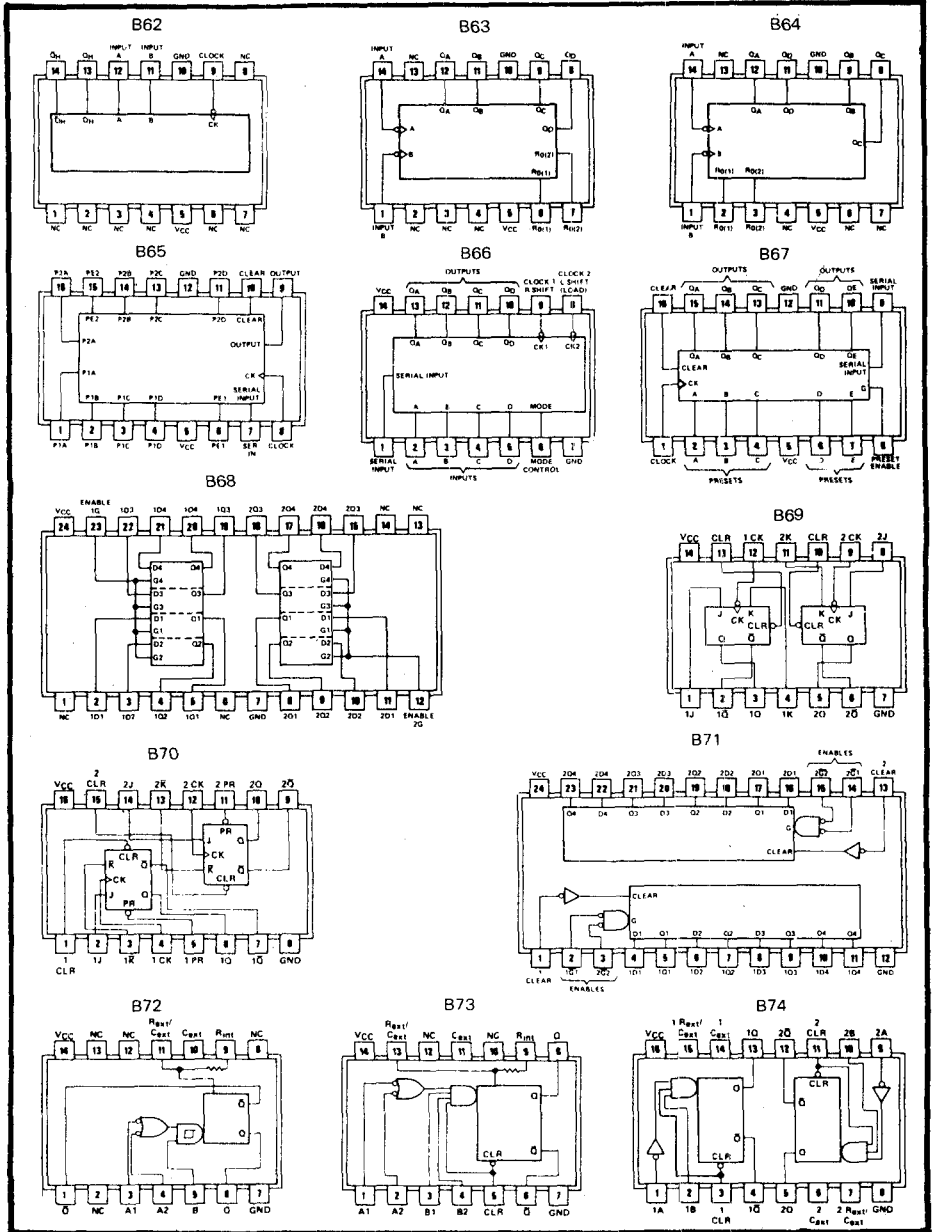


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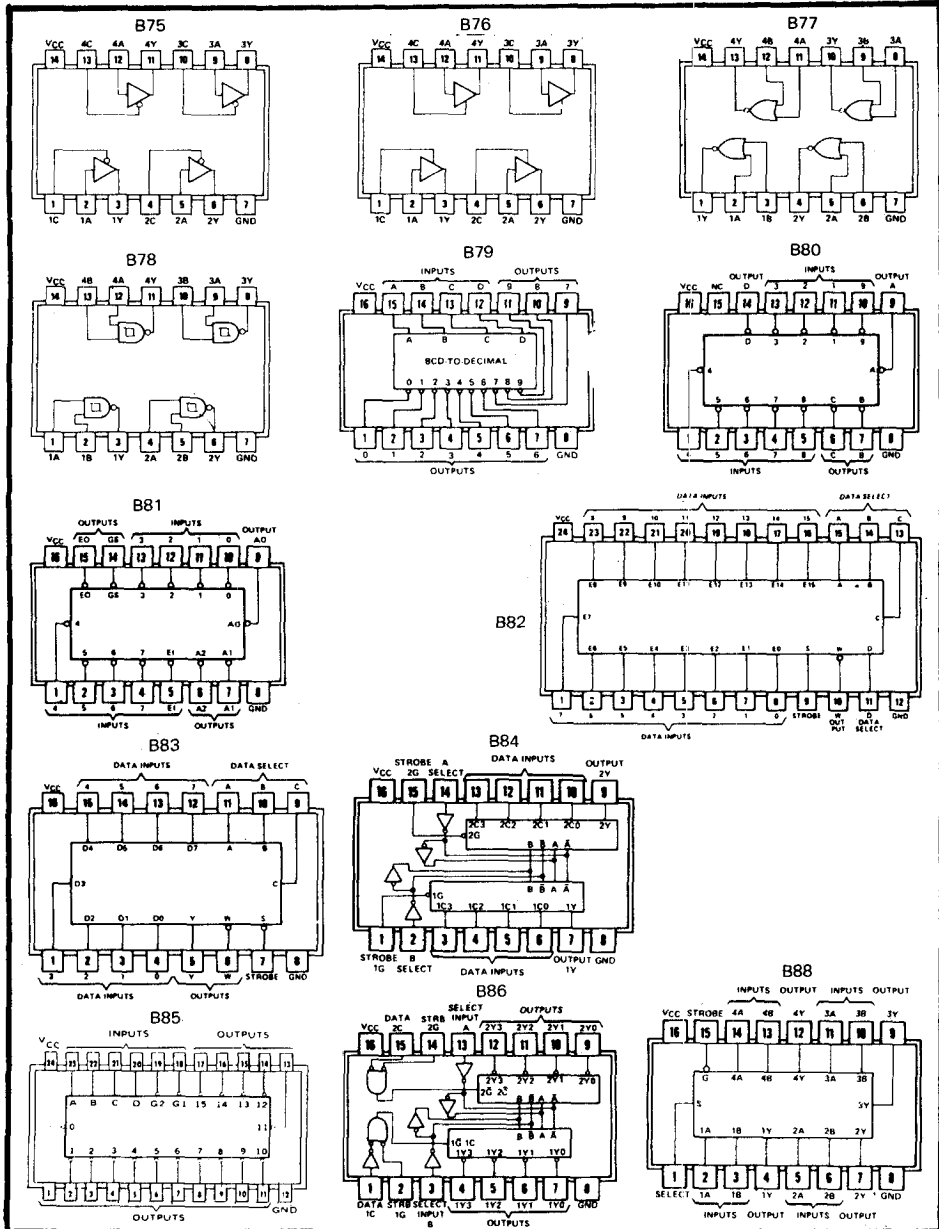
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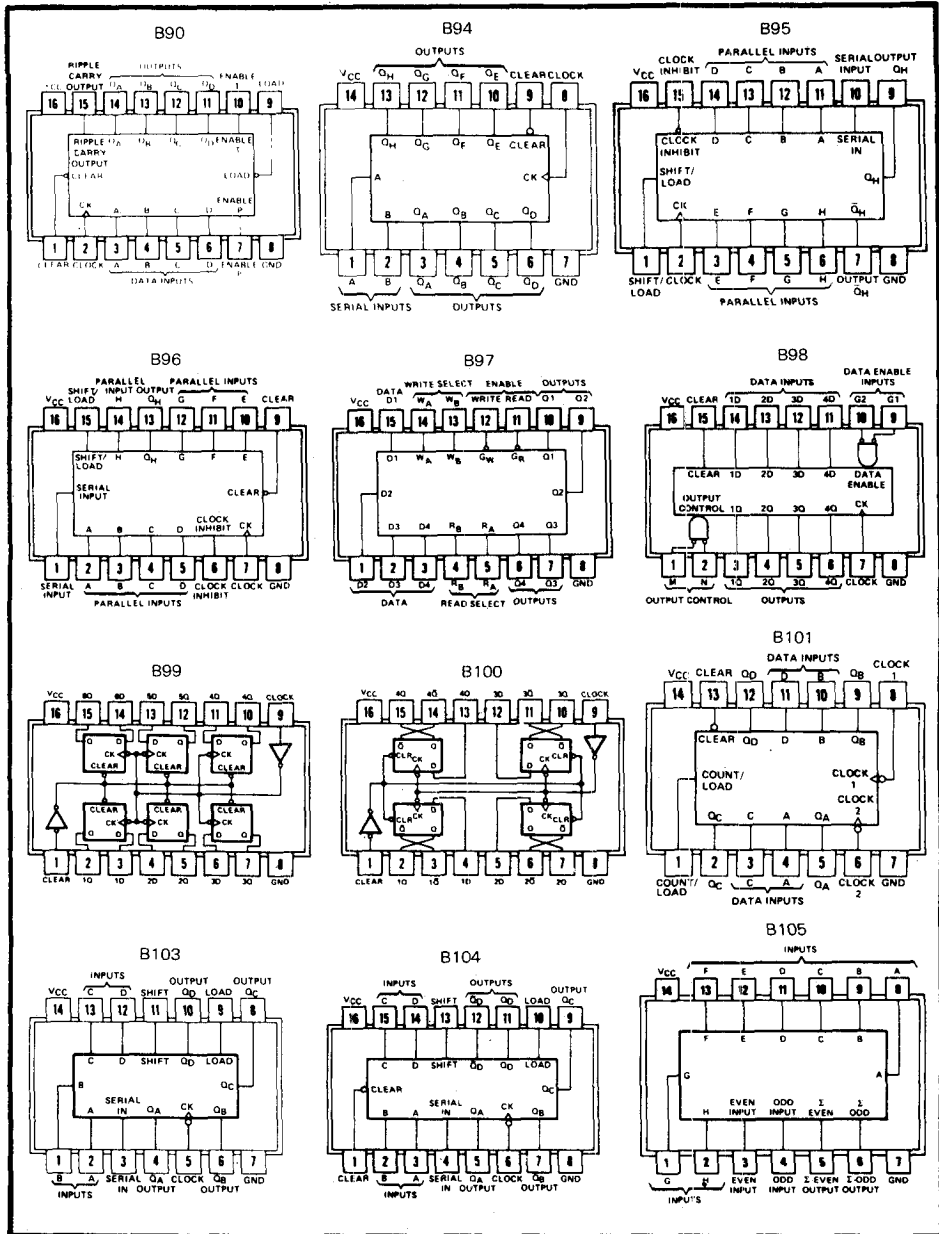


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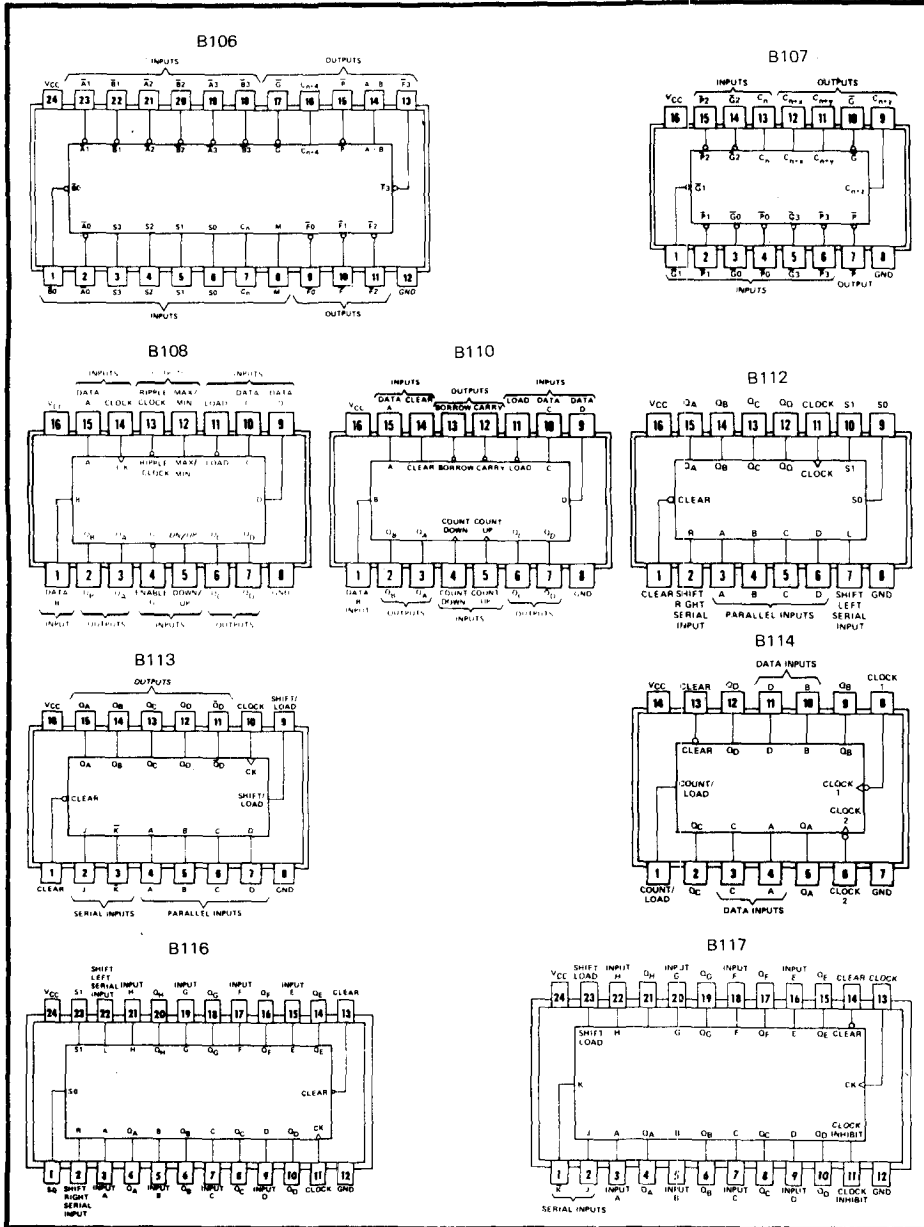


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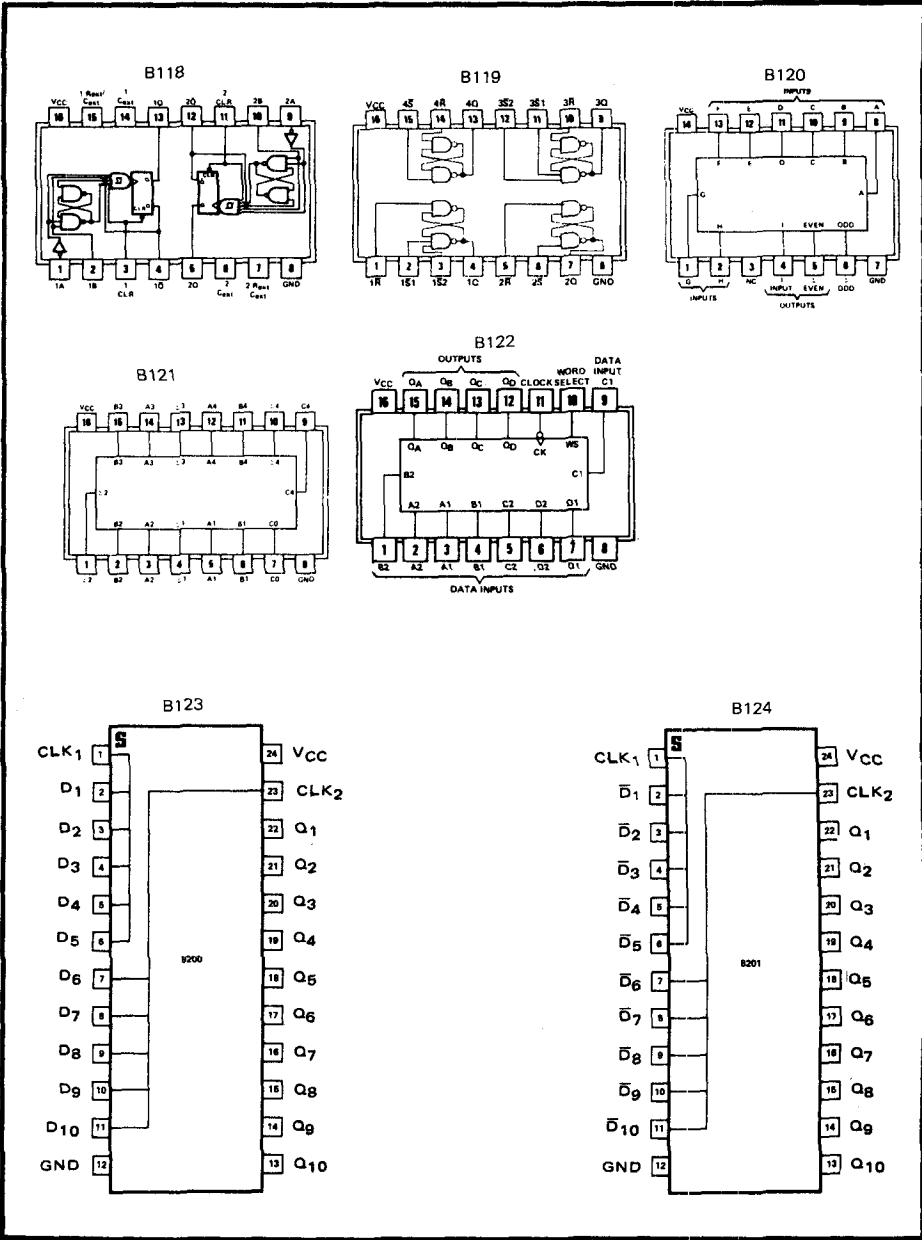


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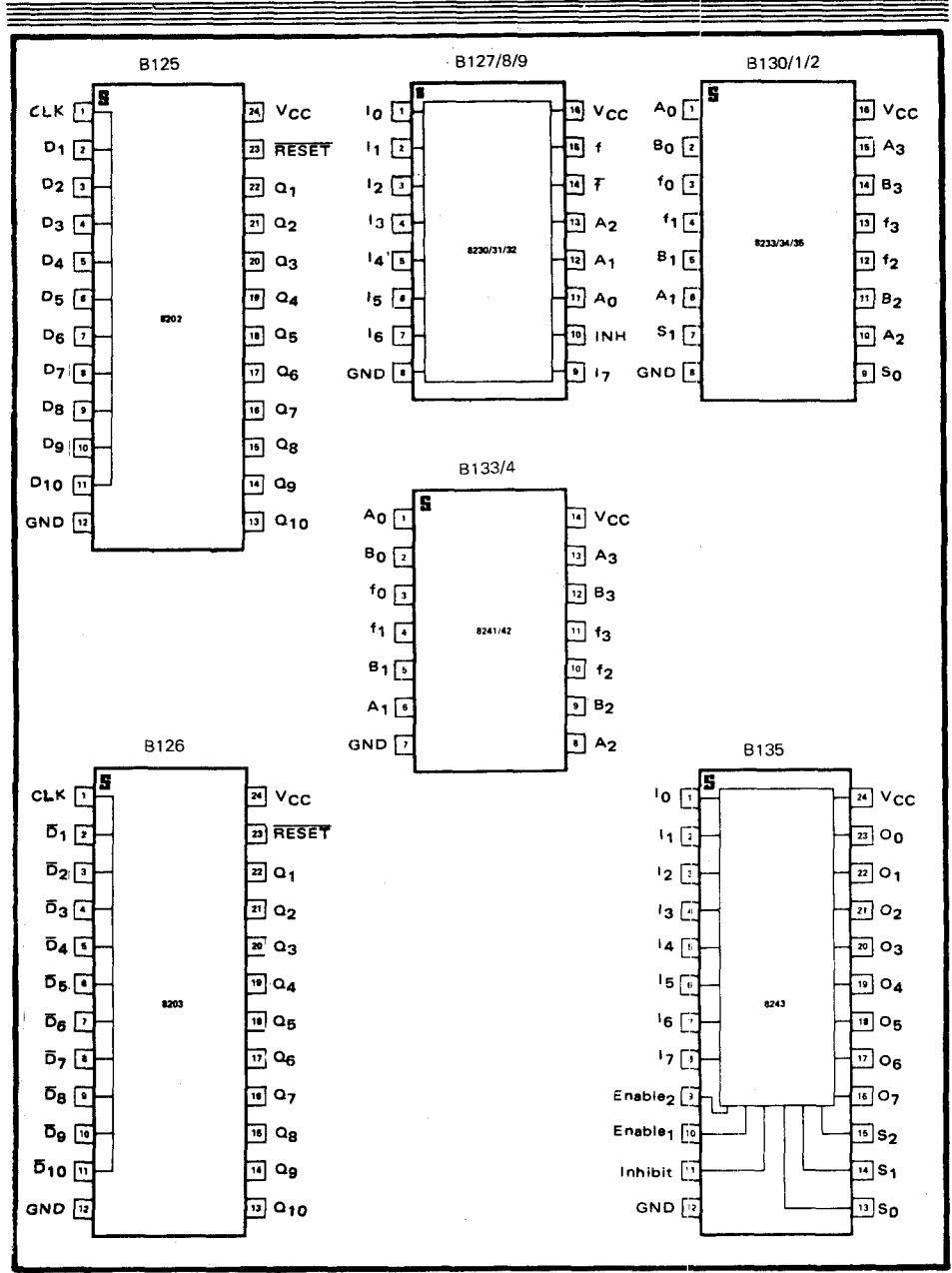


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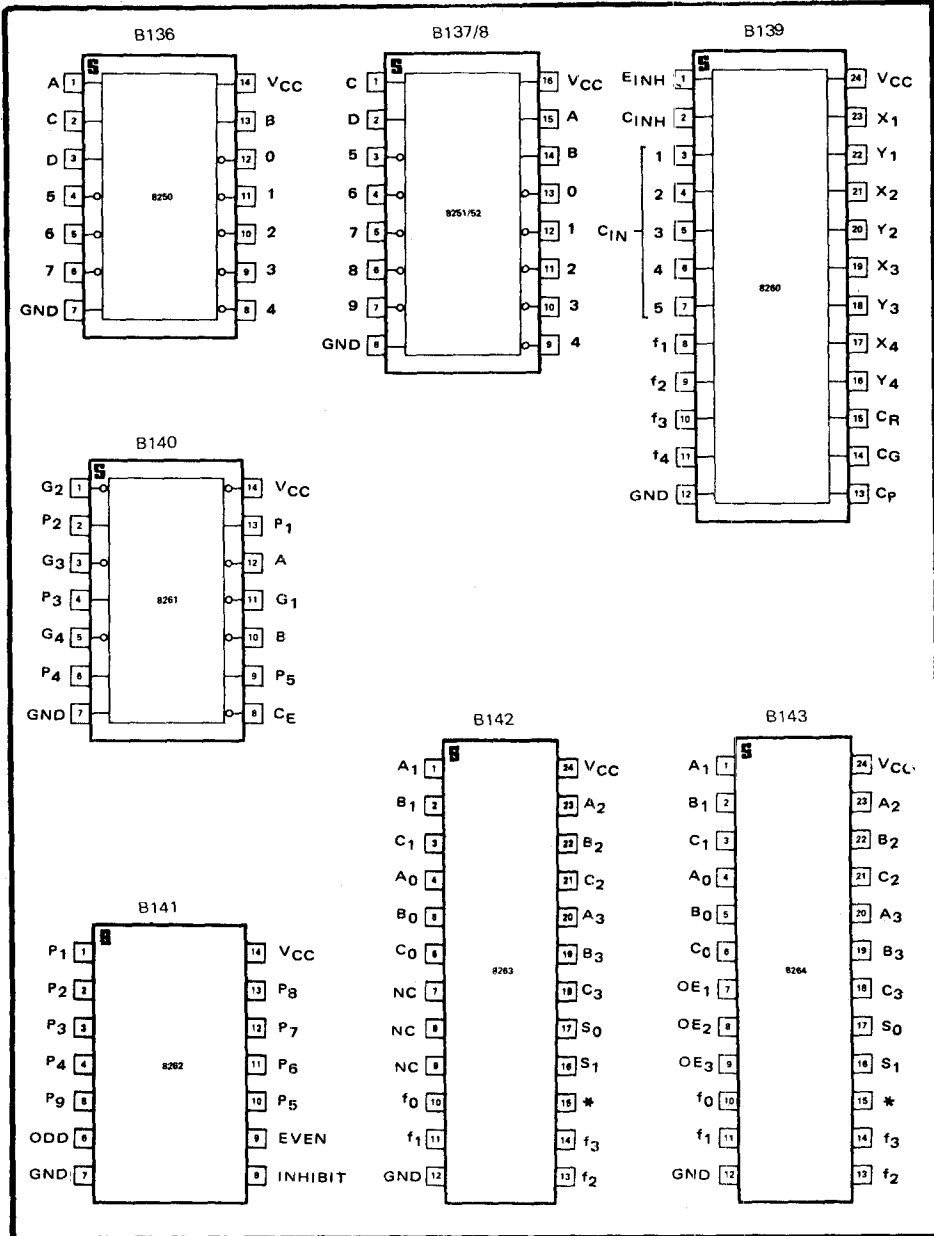
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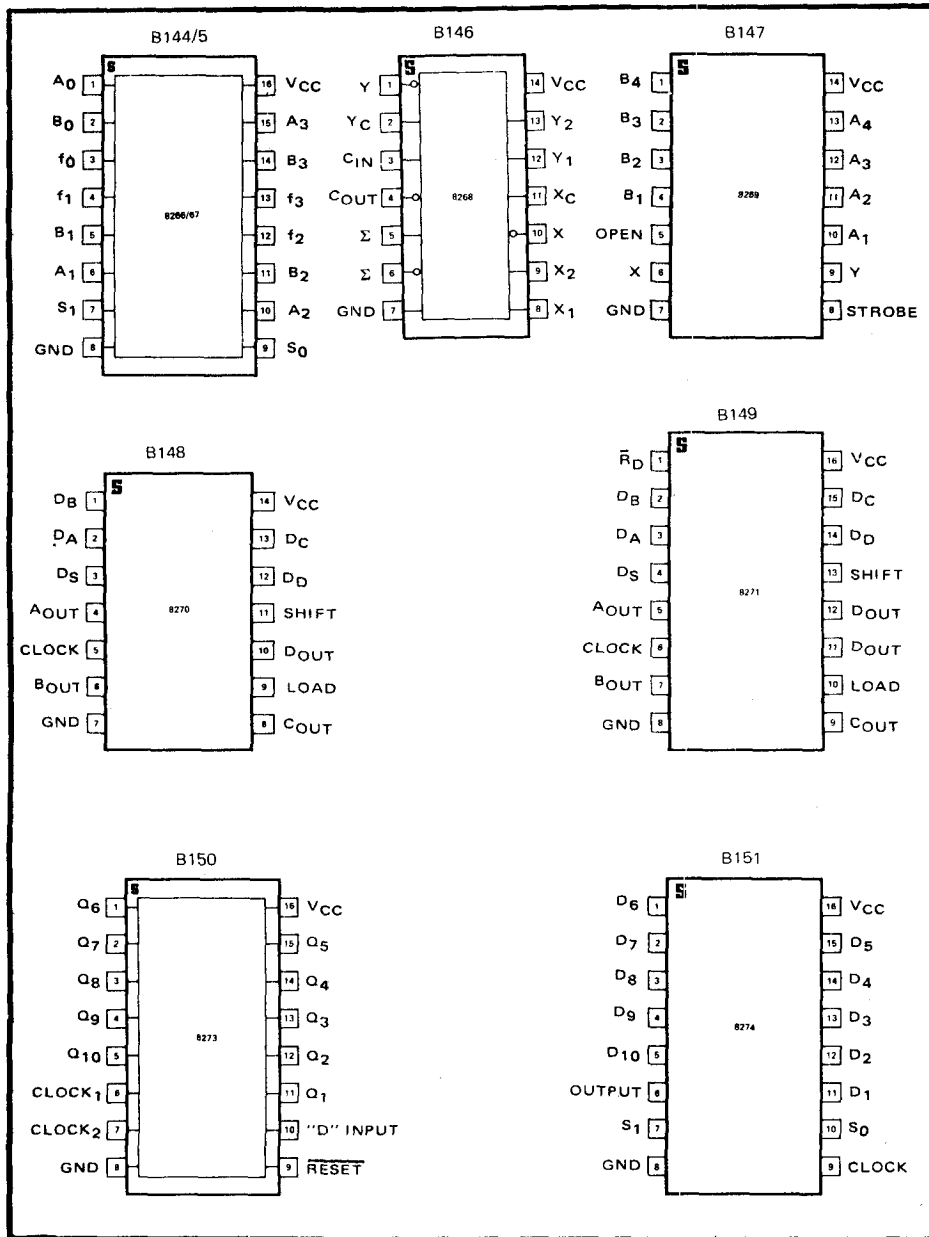


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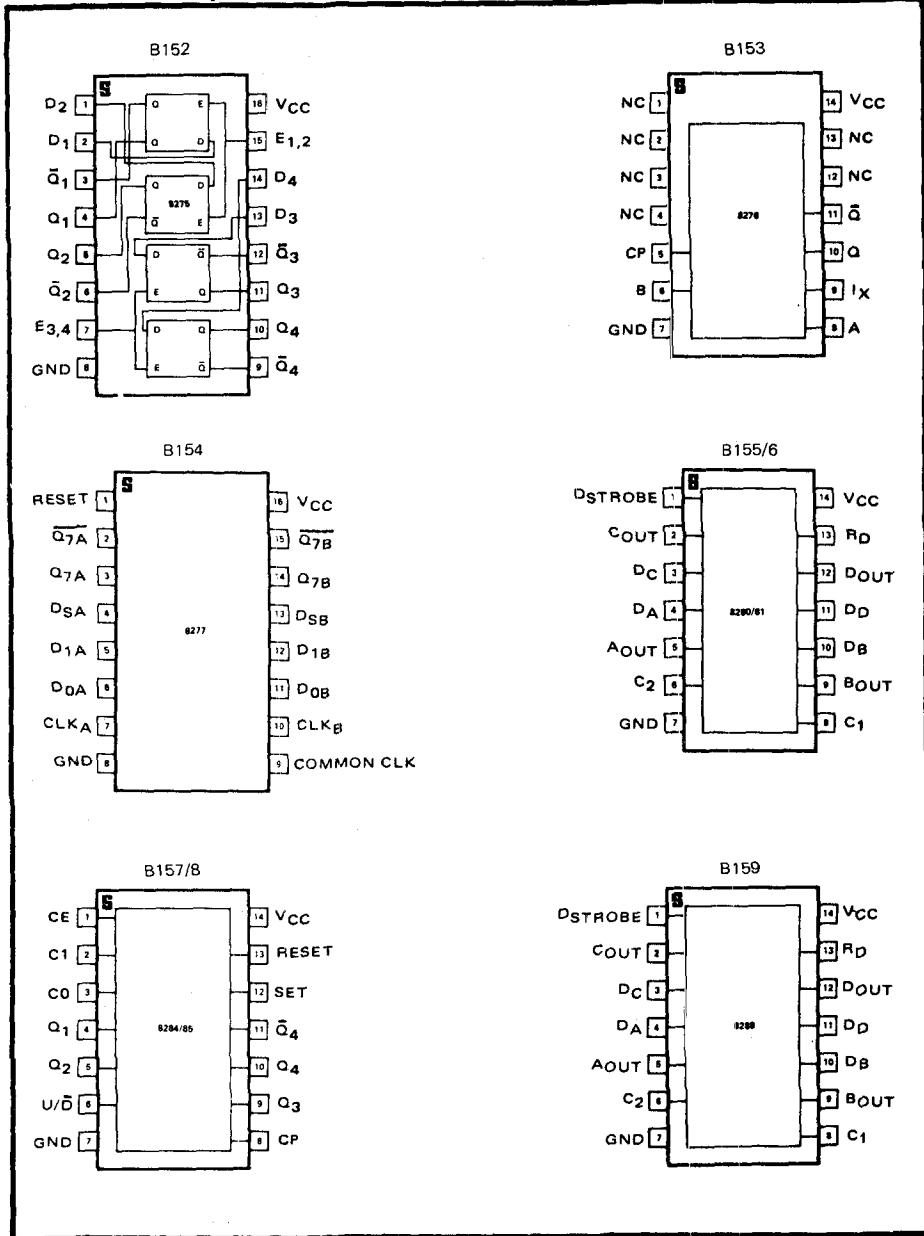


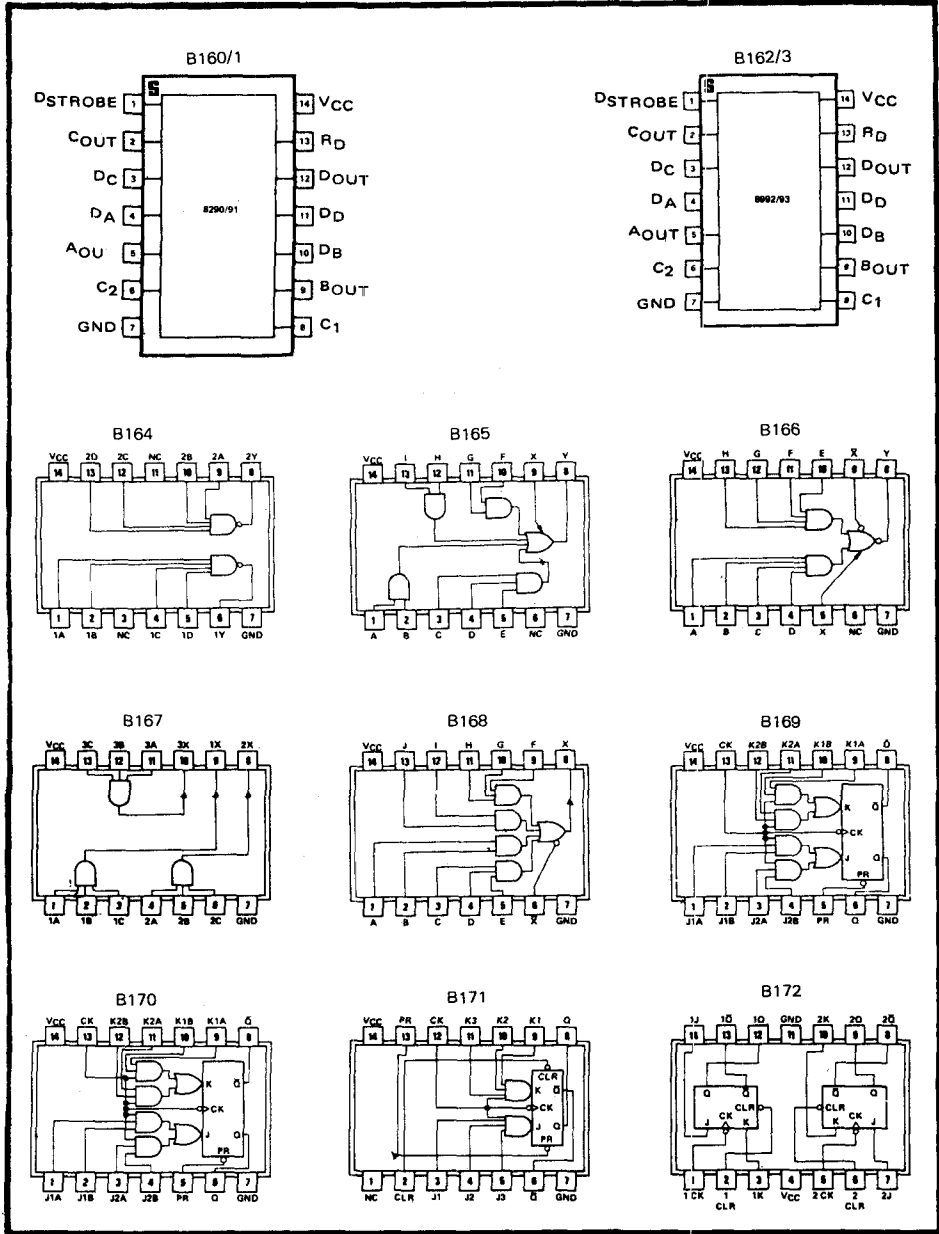
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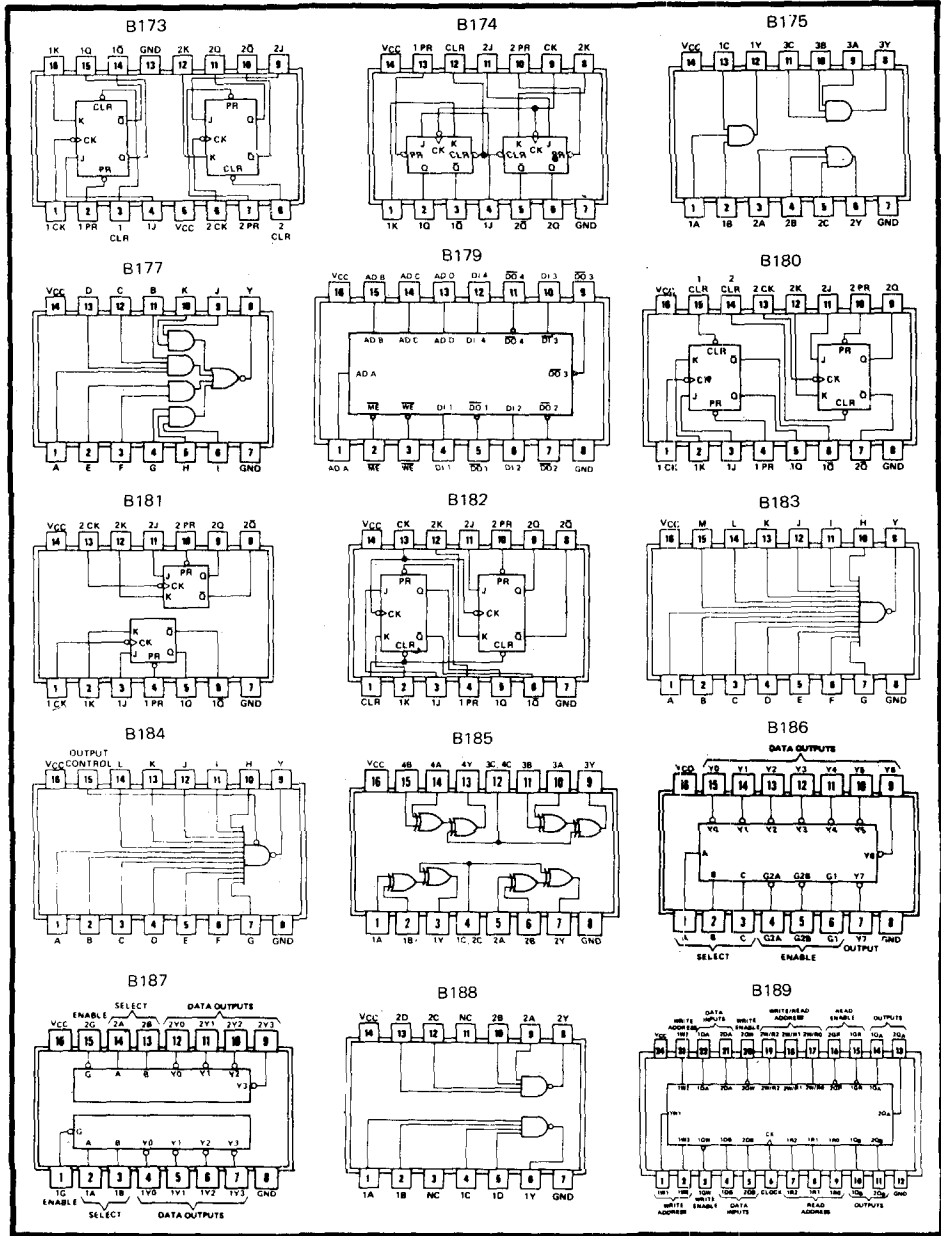


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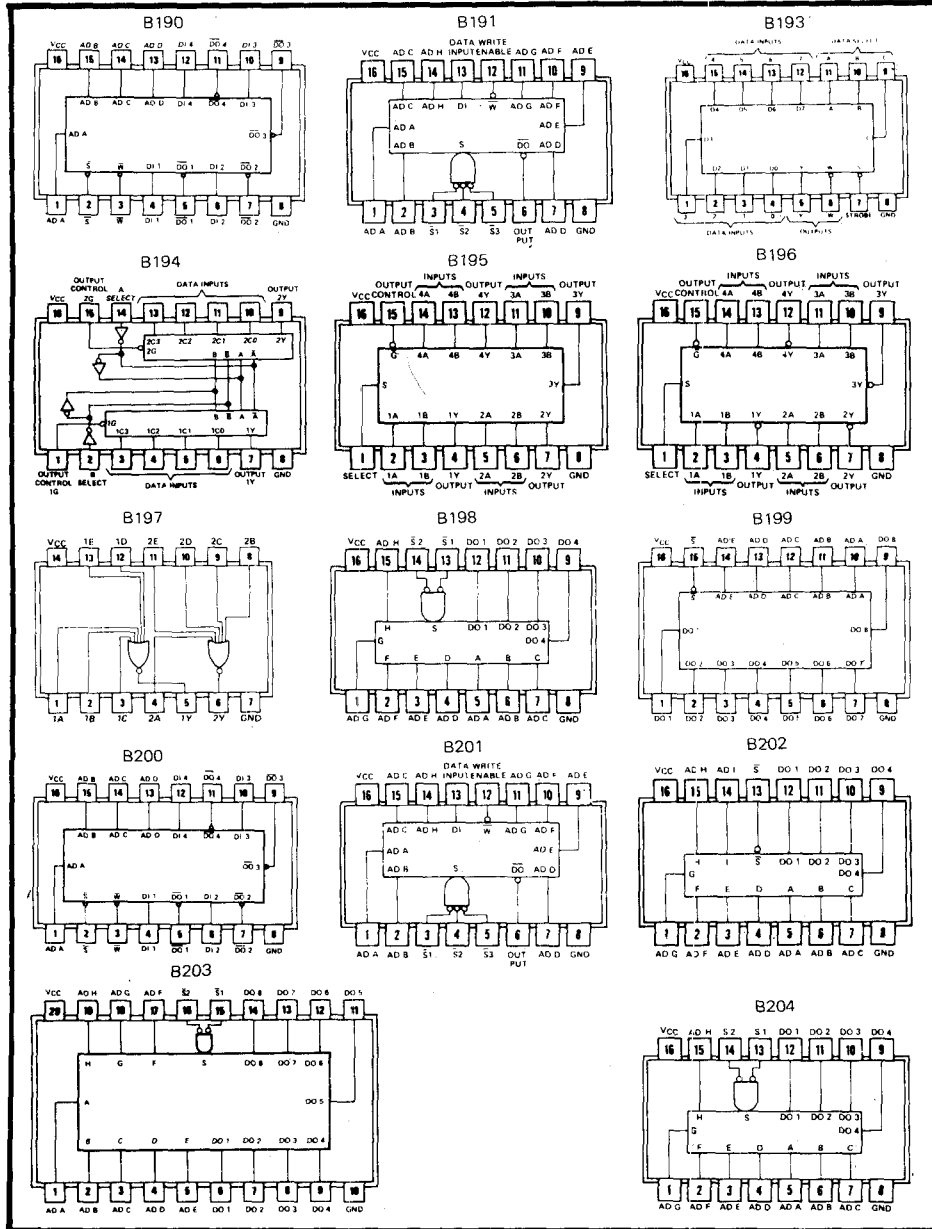
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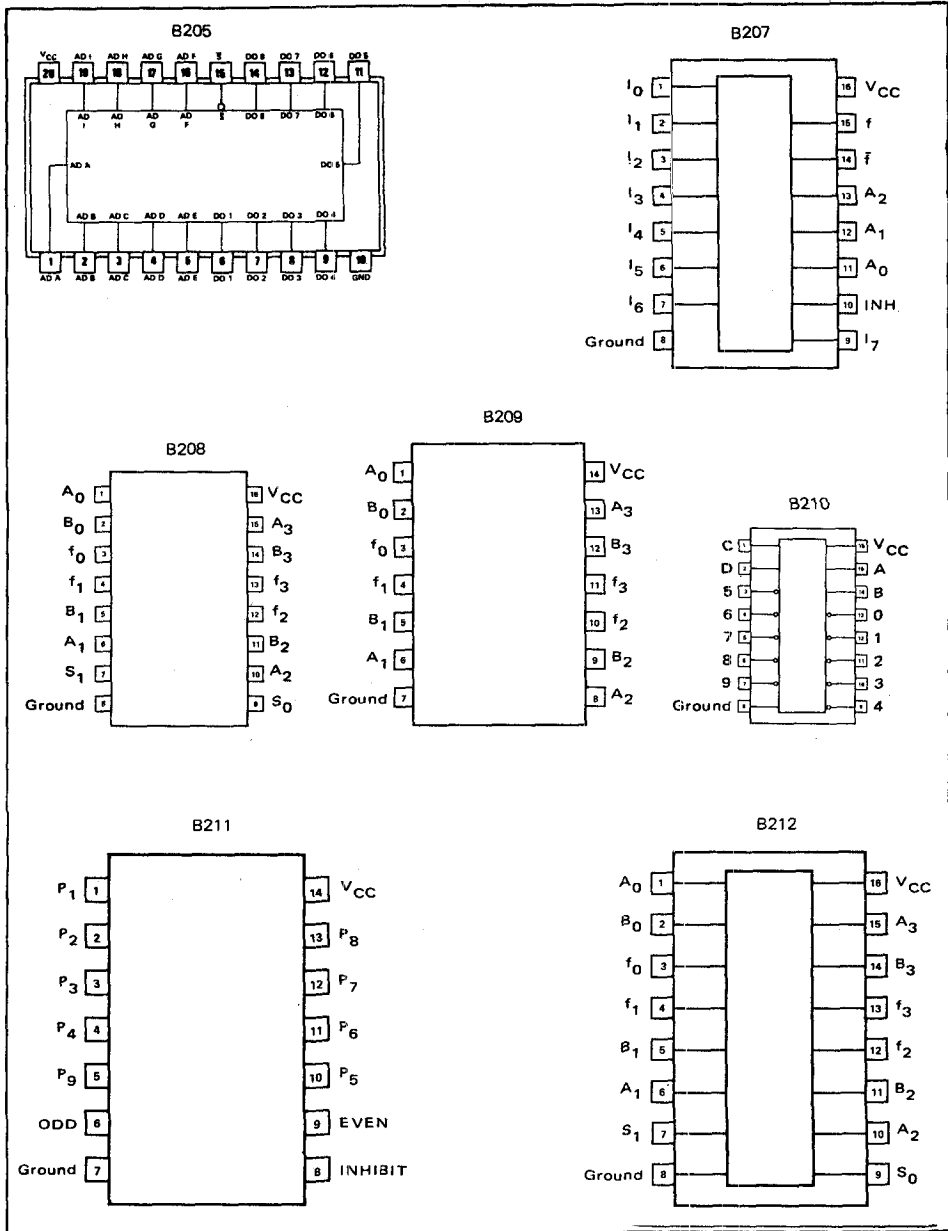


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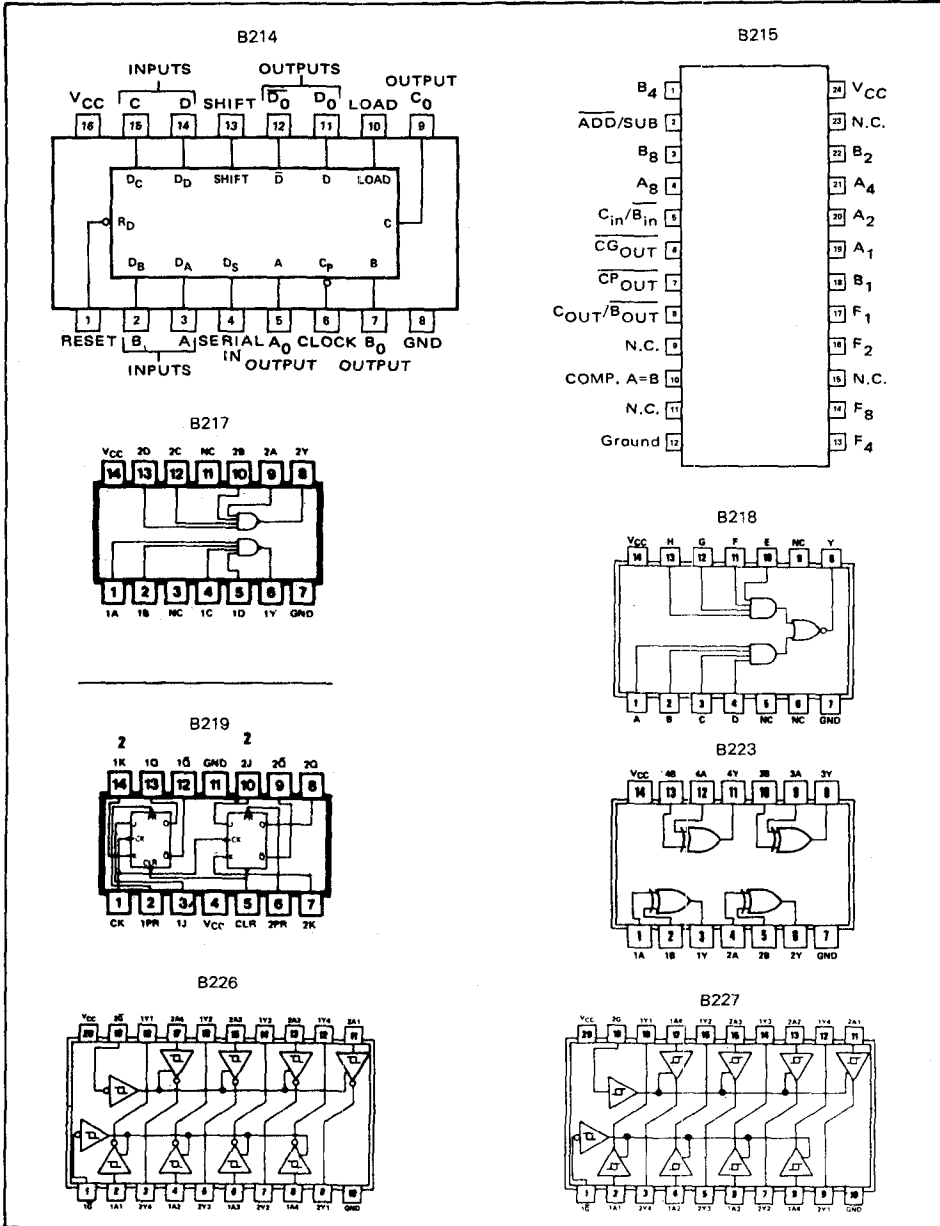
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### B219

2 2

1K 1D 1C GND 2J 2G 2O

14 13 12 11 10 9 8

1 2 3 4 5 6 7

1K 1PR 1J V<sub>CC</sub> CLR 2PR 2K

### B223

V<sub>CC</sub> 4B 4A 4Y 3B 3A 3Y

13 12 11 10 9 8

1 2 3 4 5 6 7

1A 1B 1Y 2A 2B 2Y GND

### B226

V<sub>CC</sub> 8E 1Y1 3M 1Y2 3A3 1Y3 3B3 2R 2R 3A1

14 13 12 11 10 9 8

1 2 3 4 5 6 7 8 9

1E 1A1 2Y4 1A2 1A3 2Y3 1A4 2Y1 GND

### B227

V<sub>CC</sub> 2G 1W 1W 1W 2A3 1W 2A2 1W 2A1

14 13 12 11 10 9 8

1 2 3 4 5 6 7 8 9

1E 1A1 2Y4 1A2 1A3 2Y3 1A4 2Y1 GND

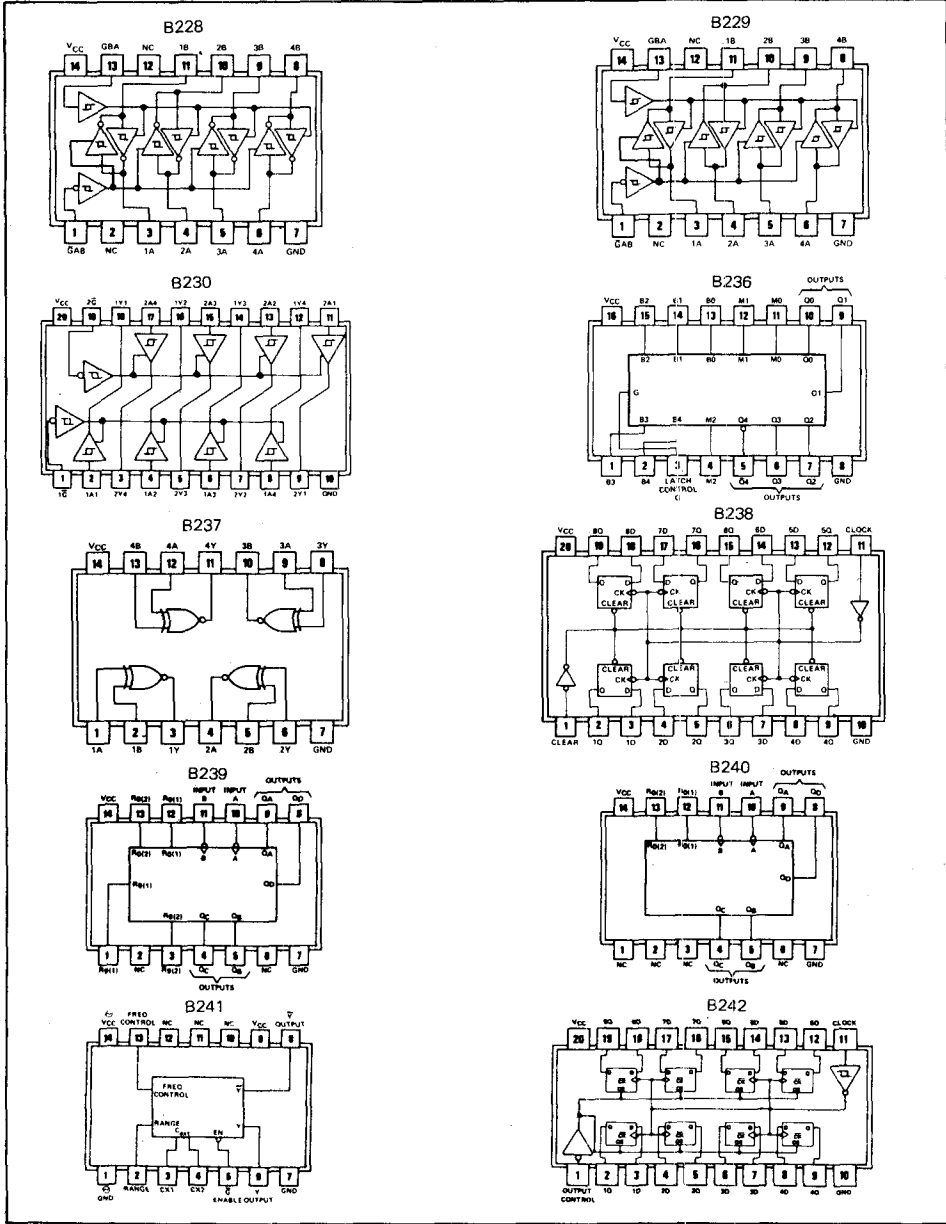
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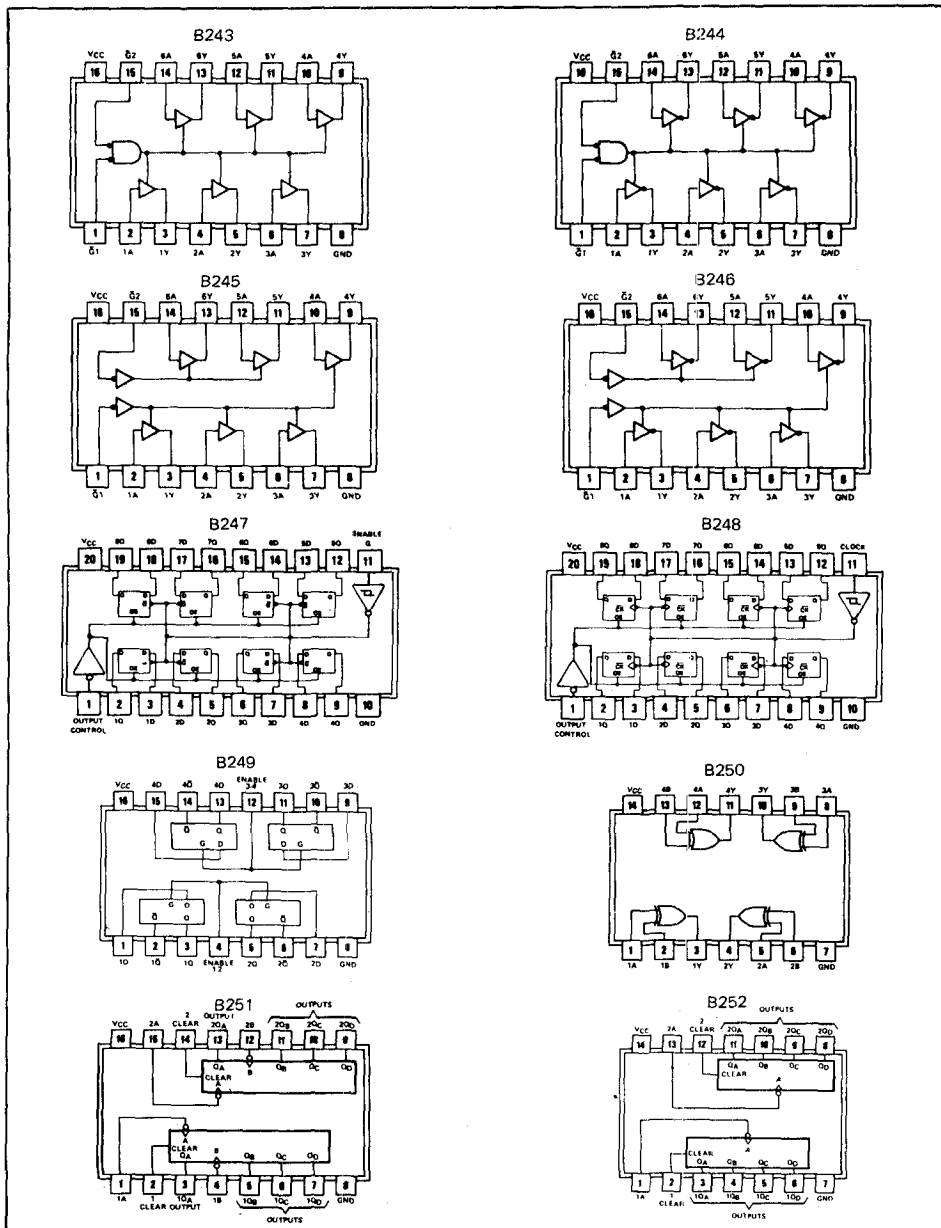


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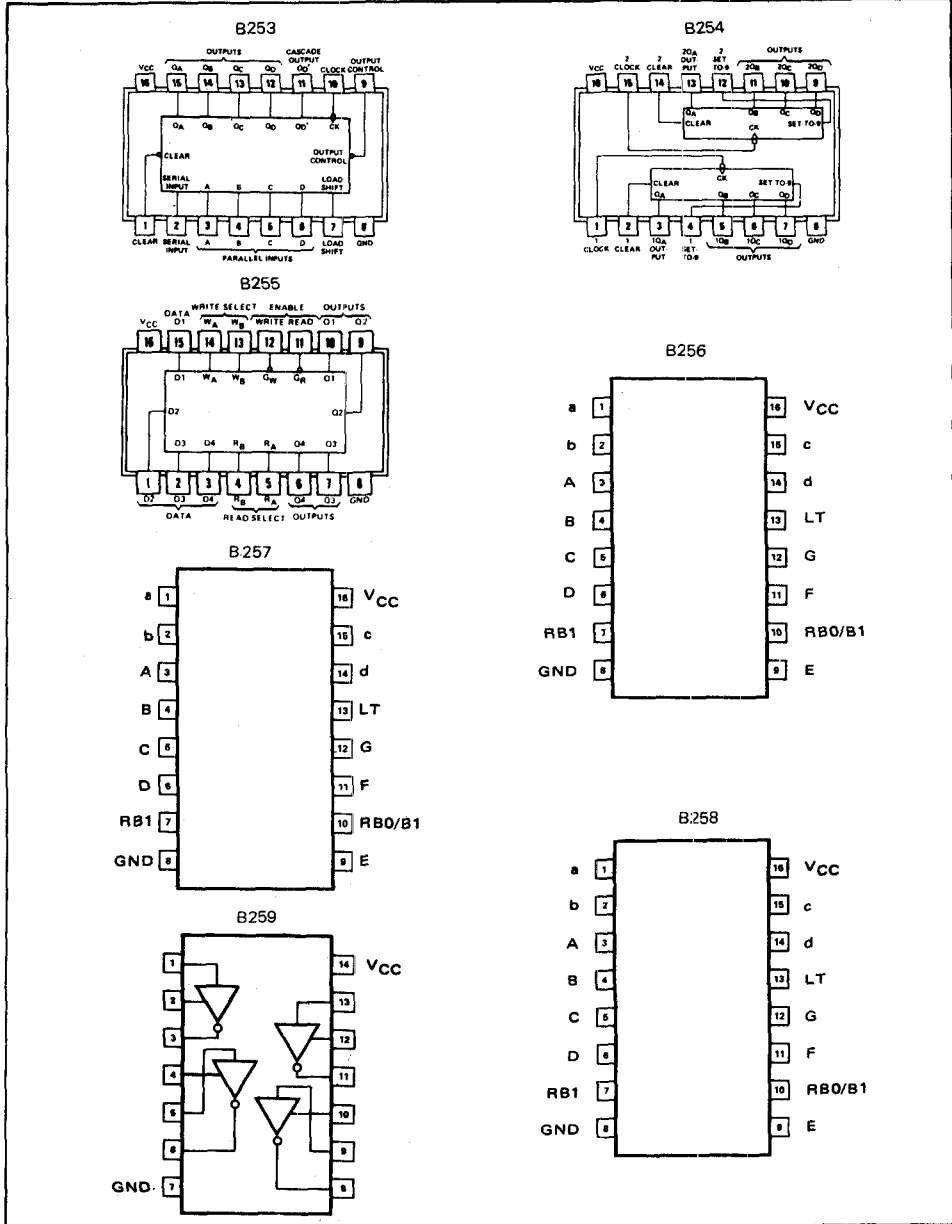


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