TPS22924EVM-532

This user's guide describes the characteristics, operation, and use of the TPS22924EVM-532 evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS22924 load switch with controlled turn on. The input voltage range of the TPS22924 is 0.75 V to 3.6 V. An integrated charge pump biases the NMOS switch to achieve a minimum switch ON resistance. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals. This user's guide includes setup instructions, schematic diagram, bill of materials, and printed-circuit board layout drawings for the EVM.

1 Introduction

The TPS22924EVM-532 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS22924 load switch. The board features the small 6-pin CSP package for a small solution size.

Table 1. TPS22924 VOUT Rise Time Options

EVM	Device	Rise Time (µs) Typical	VIN (V)	Max. Continuous Current	Enable (ON Pin)	Quick Output Discharge
HPA532-001	TPS22924B	100	3.6	2-A	Active High	Yes
HPA532-002	TPS22924C	840	3.6	2-A	Active High	Yes
HPA532-003	TPS22924D	6200	3.6	2-A	Active High	Yes

1.1 Related Documentation From Texas Instruments

TPS22924, ULTRA-SMALL, LOW-INPUT-VOLTAGE, LOW r_{ON} LOAD SWITCH data sheets (SLVSA52, SLVSAR3, SLVSBT4)

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS22924EVM-532.

2.1 J1/J3 – Input Connections

This is the connection for the leads from the input source. Connect the positive connection to the VIN J1 and the negative connection to the GND J3.

2.2 J4/J6 – Output Connections

This is the connection for the output of the TPS22924EVM. Connect the positive connection of the load to the VOUT J4 and the negative connection to the GND J6.

2.3 JP3 – EN

This is the enable input for the device. Place a shorting jumper across the HI and EN pins of JP3 to enable the integrated circuit (IC). Place a shorting jumper across the LO and EN pins of JP3 to disable the IC. A shorting jumper must be installed on JP3 in either the ON or OFF positions, and EN must not be left unconnected. An external enable source can be applied to the TPS22924 by removing the shunt and connecting a signal to the center pin of JP3. EN ≥ 0.75V is required for the ACTIVE or ON state of the device. A switching signal may also be used and connected at this point.

2.4 J2/J5 – V_{IN} Sense and V_{OUT} Sense

These two connectors are used when very accurate measurements of input or output voltage are required, Ron measurements should be made using these sense connections and measuring the voltage drop from VIN to VOUT and then calculating the resistance.

3 Operation

Connect the positive input of the power supply to the VIN J1 and the negative lead of the power supply to GND J3. The input voltage range of the TPS22924 is 0.75 V to 3.6 V.

Output load can be applied by connecting between J4 VOUT and J6 GND. The TPS22924 is rated for a maximum continuous current of 2A. Additional output load can be selected using JP6, JP7, and JP8. Shorting across JP6 selects R1 an 36 ohm on board resistor. JP7 selects R2 an 11 ohm on board resistor. JP8 selects R3 which is open for customer selection. R1, 2 and 3 are intended for light loads of the output, observe the 1/8W power rating for these parts. Configure jumper JP3 as required. JP3 must be installed for proper operation. ON is normal operation. While operating in the ON state the rise time of the device is internally controlled to avoid inrush current. Different rise times are selected by device types as shown above in Table 1. In the OFF position, the device is shut down and a 1250-Ω on-chip load resistor is added for output quick discharge.

4 Test Results

See the *Typical Characteristics* section of the TPS22924 data sheet.

5 Test Configurations

5.1 On State Resistance (rON) Test Setup

Figure 1 shows a typical setup for measuring On State Resistance. The voltage drop across the switch is measured using the sense connections then divided by the current into the load yielding the r_{ON} resistance

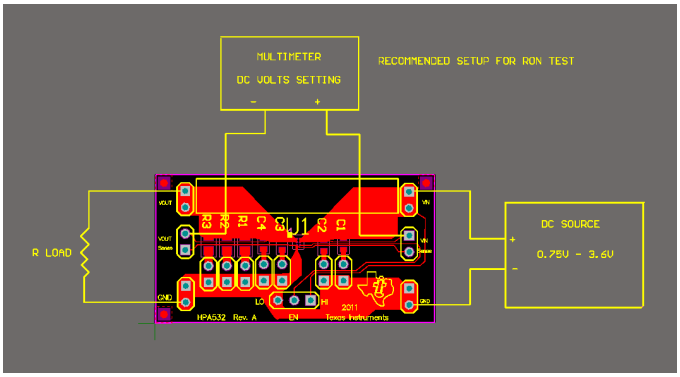

Figure 1. r_{ON} Setup

5.2 Slew Rate Test Setup

Figure 2 shows a test setup for measuring the Slew Rate of the Load Switch. Controlling the ON pin of the switch with a signal source and then measuring the output with a scope shows the switches ability to avoid inrush current.

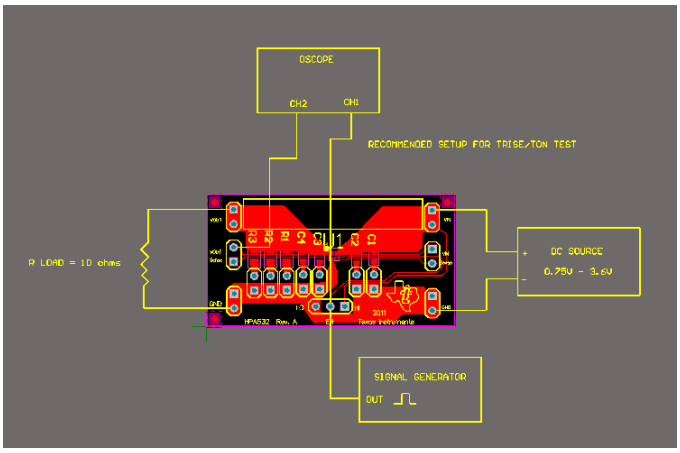

Figure 2. Slew Rate Setup

6 Board Layout, Schematic, and Bill of Materials

This section provides the TPS22924EVM-532 board layout, schematic, and bill of materials.

6.1 Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance Figure 3 and Figure 4 show the board layout for the TPS22924EVM-532 PCB.

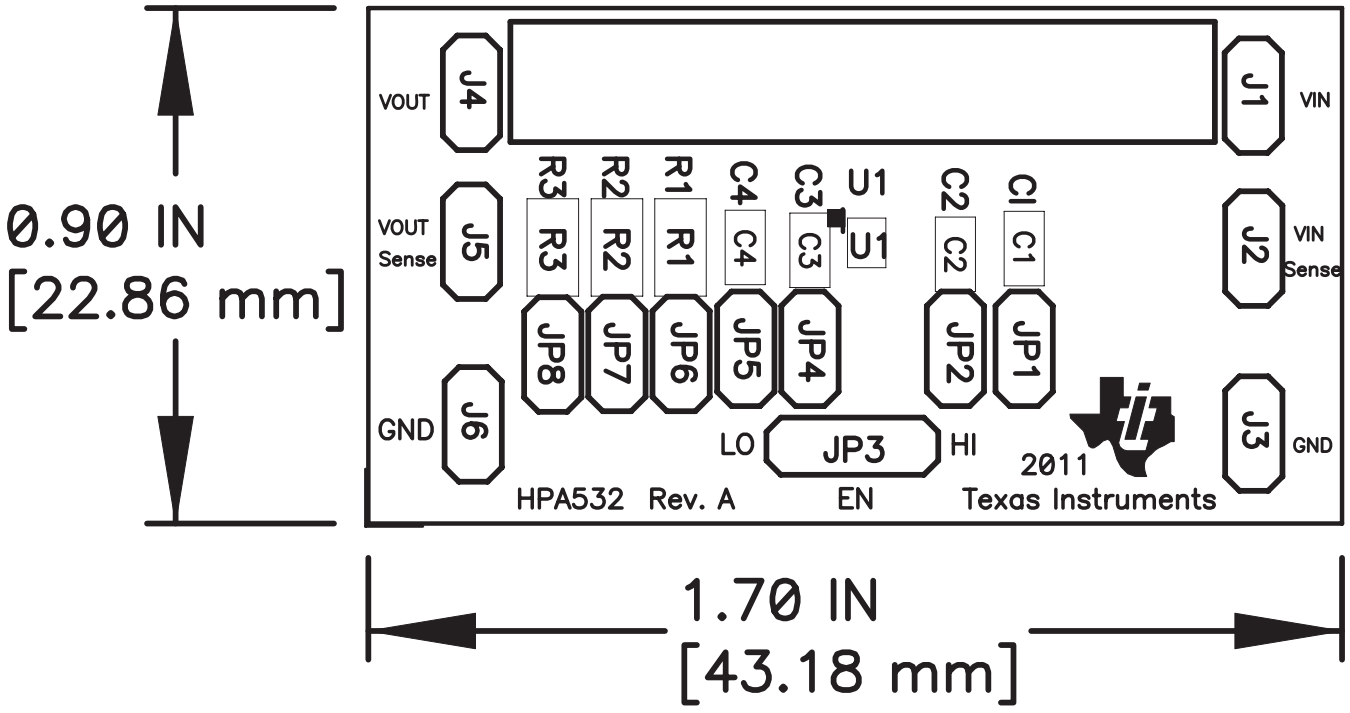

Figure 3. Top Assembly Layer

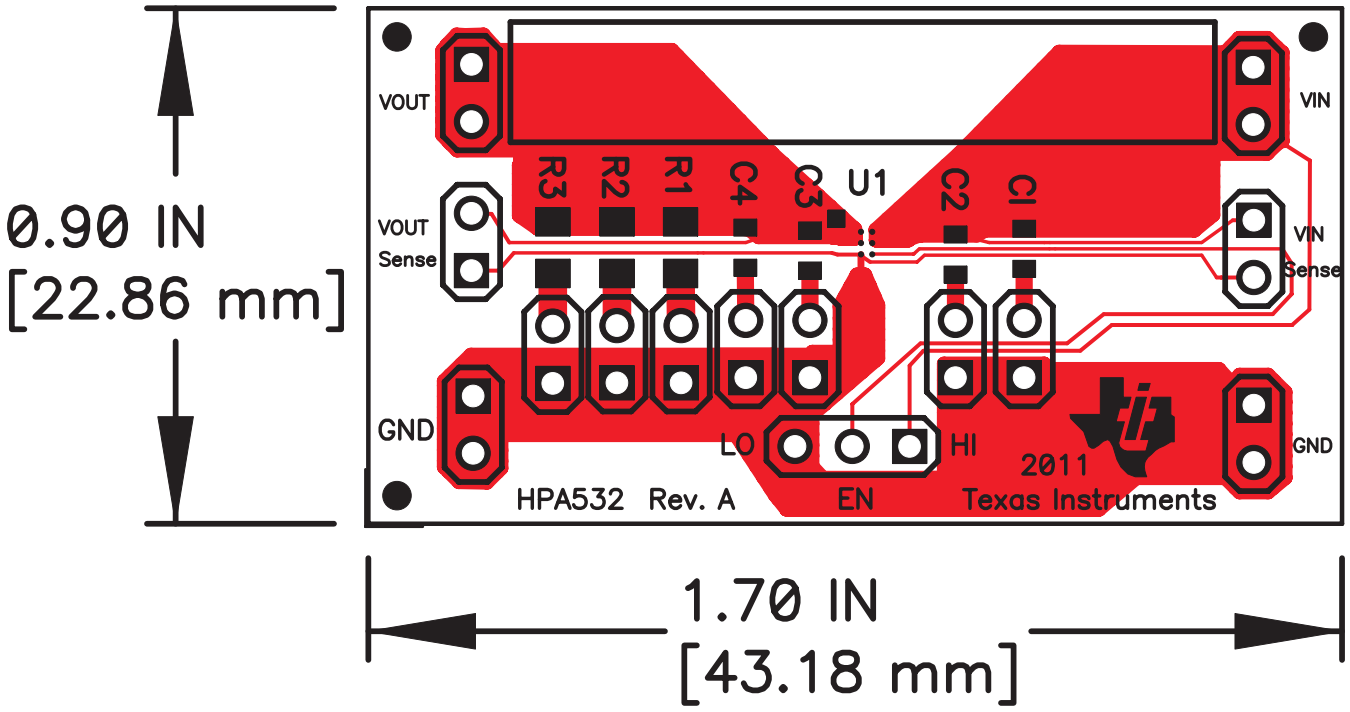

Figure 4. Top Layer

6.2 Schematic and Bill of Materials

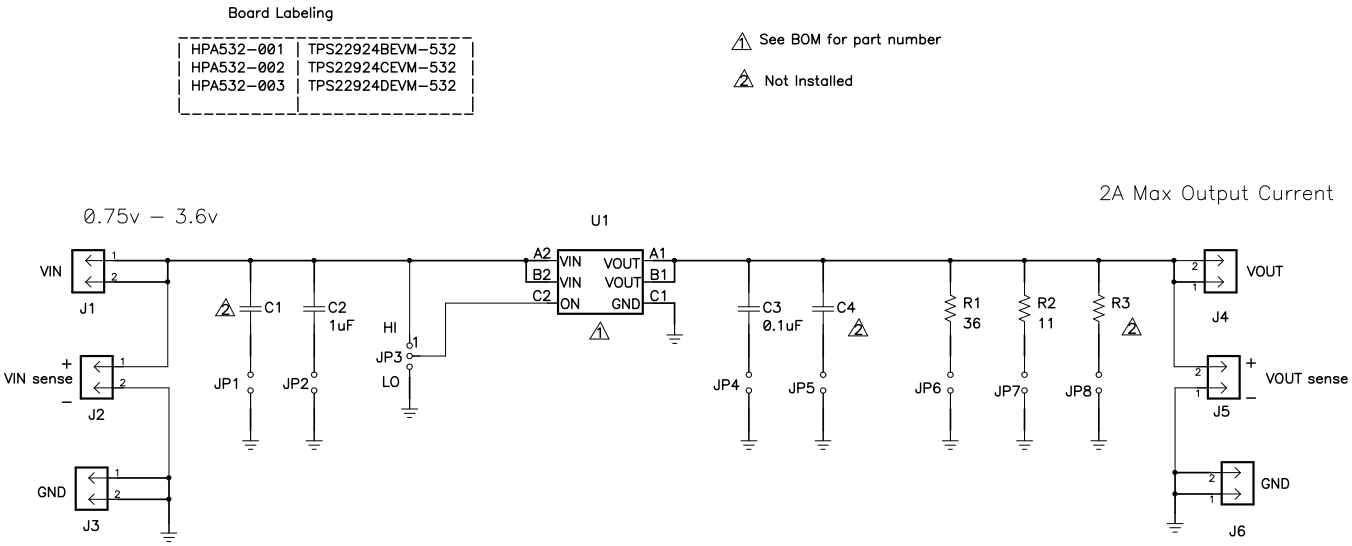

Figure 5. TPS22924EVM-532 Schematic

Table 2. Bill of Materials(1)(2)(3)(4)

-001 COUNT	-002 COUNT	-003 COUNT	RefDes	Value	Description	SIZE	Part Number	MFR
1	1	1	--		PCB, 0.9 In x 1.7 In x 0.062 In		HPA532	Any
1	1	1	C3	0.1uF	Capacitor, Ceramic, 50-V, Y5V	603	GRM188F51H104ZA01D	MuRata
1	1	1	C2	1uF	Capacitor, Ceramic, 25-V, Y5V	603	GRM188F51E105A12D	MuRata
0	0	0	C1, C4	OPEN	Capacitor, Ceramic	603	Std	Std
1	1	1	R1	36	Resistor, 5% 1/8W	805	ERJ-6GEYJ360V	Panasonic
1	1	1	R2	11	Resistor, 5% 1/8W	805	ERJ-6GEYJ110V	Panasonic
0	0	0	R3	OPEN	Resistor, 5% 1/8W	805	Std	Std
13	13	13	J1-J6,JP1-2,JP4-8	PEC02SAAN	Header,2pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	1	1	JP3	PEC03SAAN	Header,3pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	0	0	U1	TPS22924BYZ	IC, Single Chip, Low Input Voltage Current-Limited Load Switch with Shut Off Auto-Restart	YZ	TPS22924BYZ	TI
0	1	0	U1	TPS22924CYZP	IC, Single Chip, Low Input Voltage Current-Limited Load Switch with Shut Off Auto-Restart	YZP	TPS22924CYZP	TI
0	0	1	U1	TPS22924DYZP	IC, Single Chip, Low Input Voltage Current-Limited Load Switch with Shut Off Auto-Restart	YZP	TPS22924DYZP	TI
1	1	1			Label (See note 5)	1.25 x 0.25 inch	THT-13-457-10	Brady
3	3	3	NA	NA	Shunt, 100-mil, Black	0.100	929950-00	3M

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent components.

Table 3.

Table 3	
Assembly number	Text
HPA532-001	TPS22924BEVM-532

Table 3. (continued)

Table 3	
HPA532-002	TPS22924CEVM-532
HPA532-003	TPS22924DEVM-532

5.3 VOUT Rise Time and TON Response

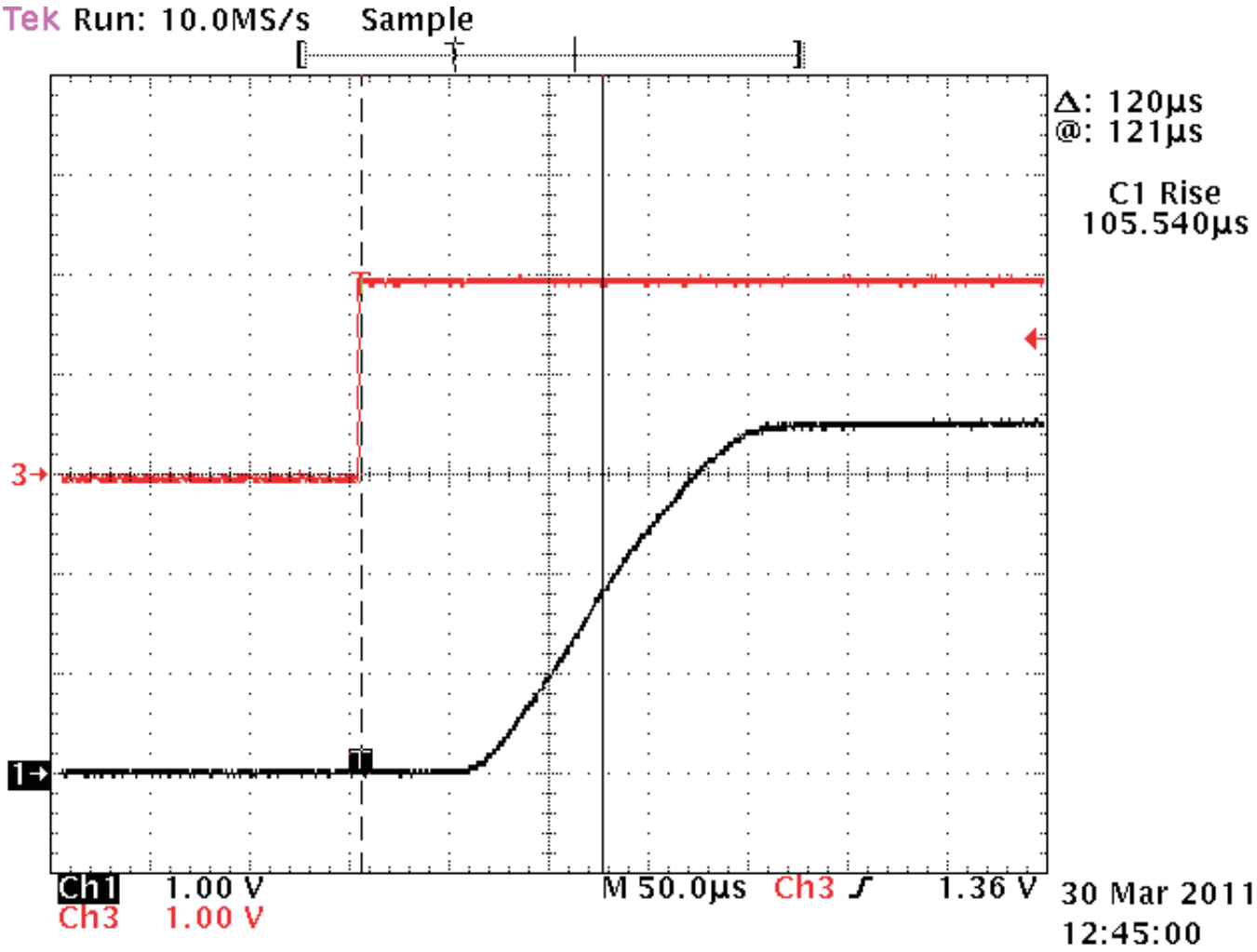

Figure 6. TPS22924B TON and Trise Example

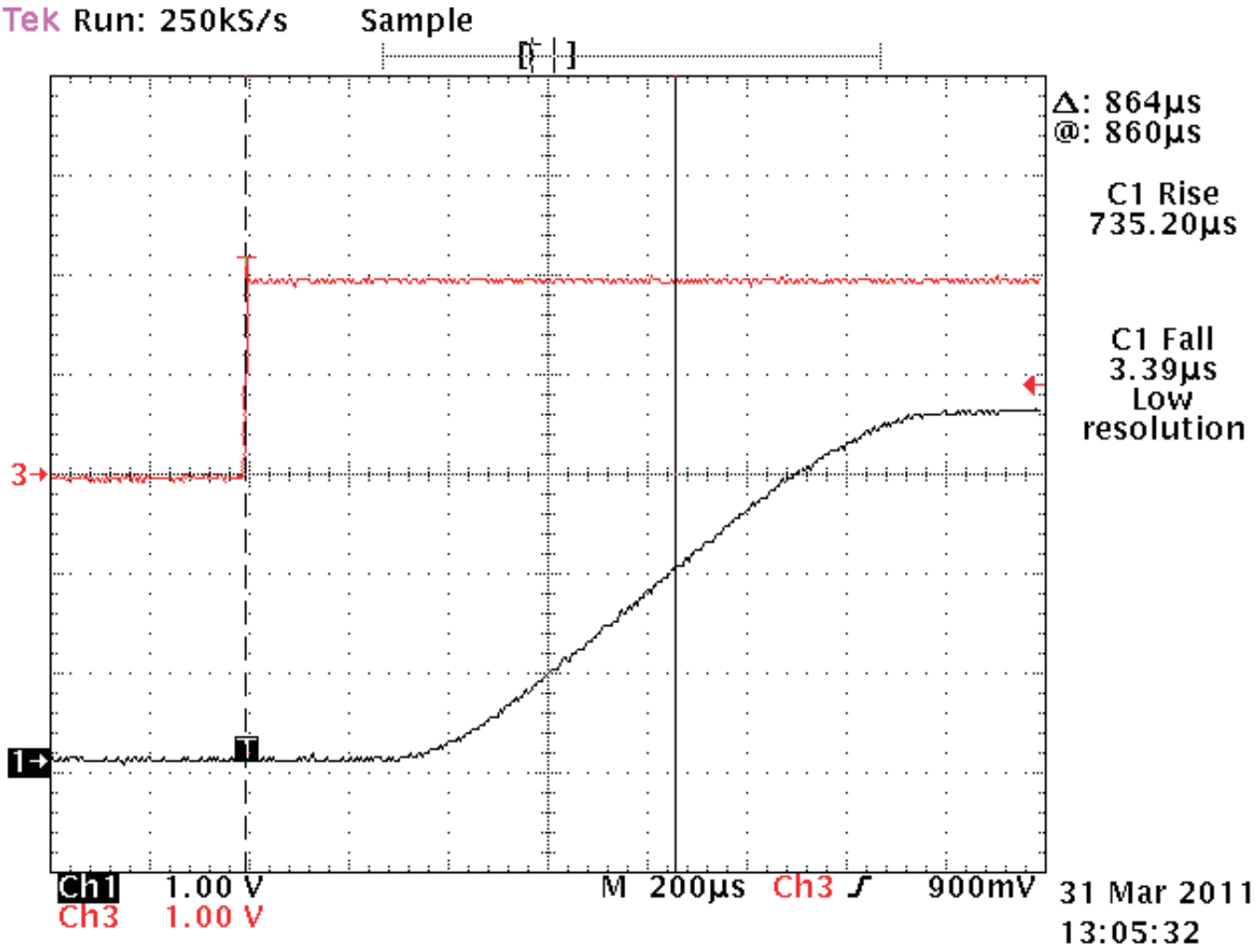

Figure 7. TPS22924C TON and Trise Example

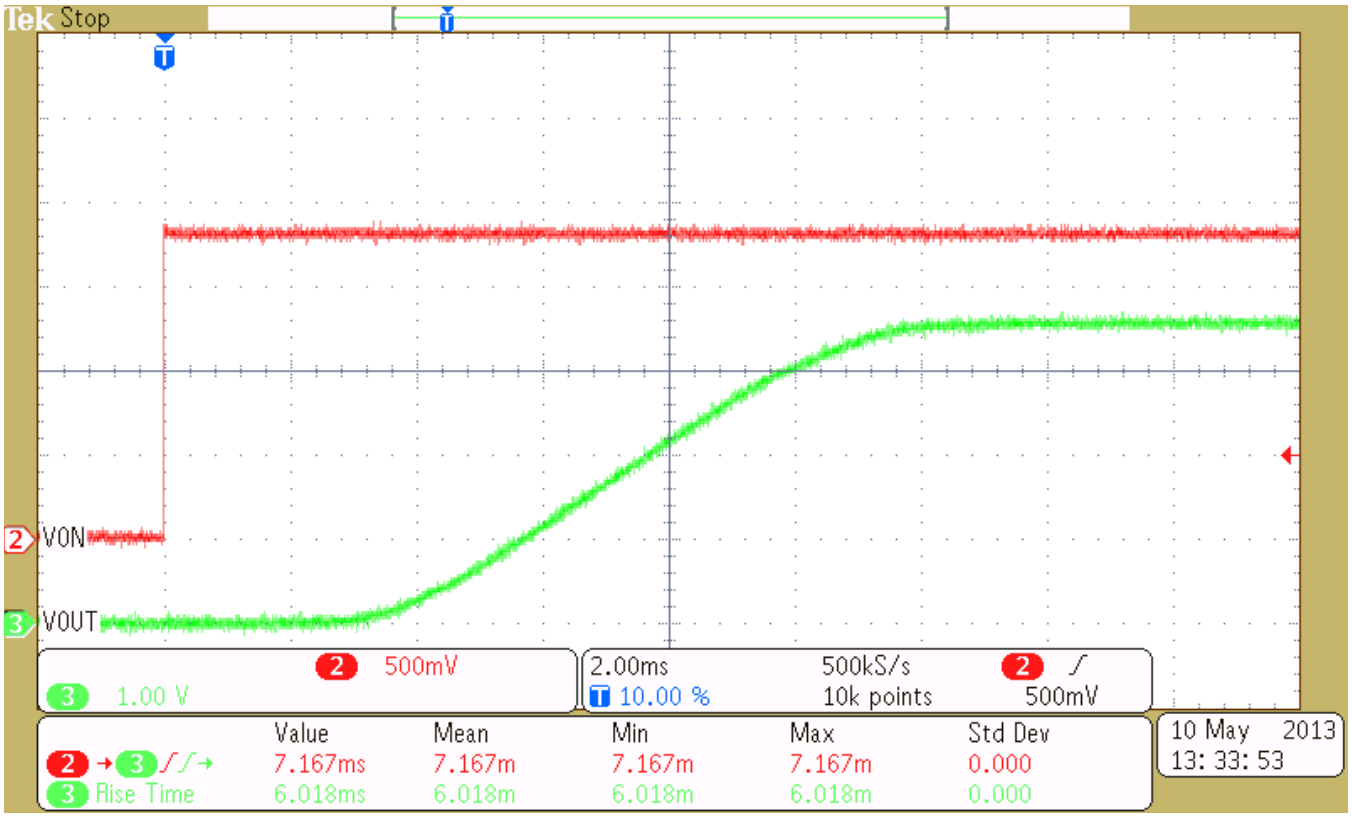

Figure 8. TPS22924D TON and Trise Example

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0.75 V to 3.6 V and the output voltage range of .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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