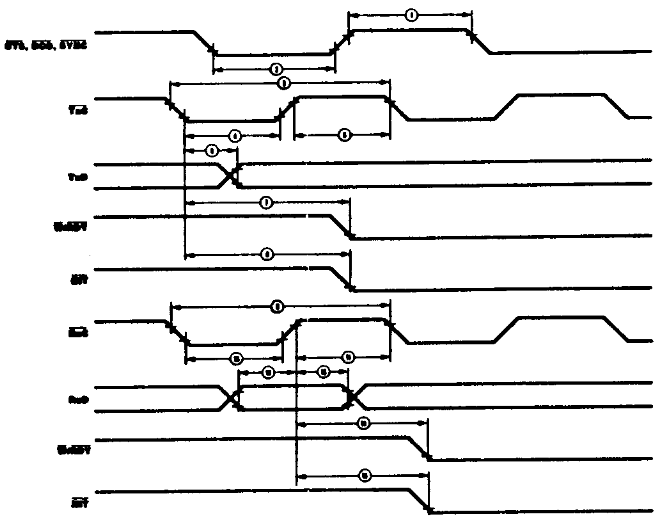
AC CHARACTERISTICS TIMING (Continued)



Z80 is a registered trademark of Zilog, Inc.

Zilog, Inc 1315 Dell Ave., Campbell, California 95008
Telephone (408)370-8000 TWX 910-338-7621

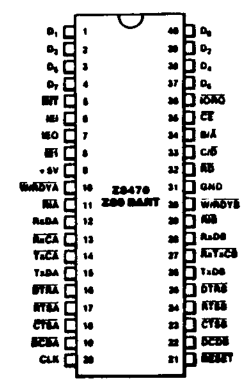
00-2847-01

Zilog

Z08470 Customer
Procurement Spec (CPS)

GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.



40-Pin Dual-In-Line Package (DIP), Pin Assignments

(MARCOM) DC2847 DOCUMENT CONTROL
MASTER

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3[a]	+0.45[a]	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−0.6[a]	+5.5[a]	V	
V_{IL}	Input Low Voltage	−0.3[a]	+0.8[a]	V	
V_{IH}	Input High Voltage	+2.0[a]	+5.5[a]	V	
V_{OL}	Output Low Voltage		+0.4[a]	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4[a]		V	I_{OH} = −250 µA
I_L	Input/3-State Output Leakage Current	−10[a]	+10[a]	µA	0.4 < V_{IN} < 2.4V
$I_{L(RI)}$	RI Pin Leakage Current	−40[a]	+10[a]	µA	0.4 < V_{IN} < 2.4V
I_{CC}	Power Supply Current		100[a]	mA	

T_A = 0°C to 70°C, V_{CC} = +5V, ±5%

a Tested
b Guaranteed by Design
c Guaranteed by Characterization

AC CHARACTERISTICS*

Number	Symbol	Parameter	Z80-4 DART Min	Z80-4 DART Max	Z80-6 DART Min	Z80-6 DART Max
1	TcC	Clock Cycle Time	250[a]	4000[a]	165[a]	4000[a]
2	TwCh	Clock Width (High)	105[a]	2000[a]	70[a]	2000[a]
3	TfC	Clock Fall Time		30[a]		15[a]
4	TrC	Clock Rise Time		30[a]		15[a]
5	TwCl	Clock Width (Low)	105[a]	2000[a]	70[a]	2000[a]
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	145[a]		60[a]	
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	115[a]		60[a]	
8	TdC(DO)	Clock ↑ to Data Out Delay		220[a]		150[a]
9	TsDI(C)	Data In to Clock ↑ Setup (Write or M1 Cycle)	50[a]		30[a]	
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		110[c]		90[c]
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		160[c]		100[c]
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	90[a]		75[a]	
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	140[c]		120[c]	
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before M1)		190[c]		160[c]
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		100[c]		70[c]
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		100[a]		70[a]
17	TdC(INT)	Clock ↑ to INT ↓ Delay		200[a]		150[a]
18	TdIO(W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Wait Mode)		210[c]		175[c]
19	TdC(W/RR)	Clock ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)		120[a]		100[c]
20	TdC(W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		130[c]		110[c]

*Units in nanoseconds (ns).

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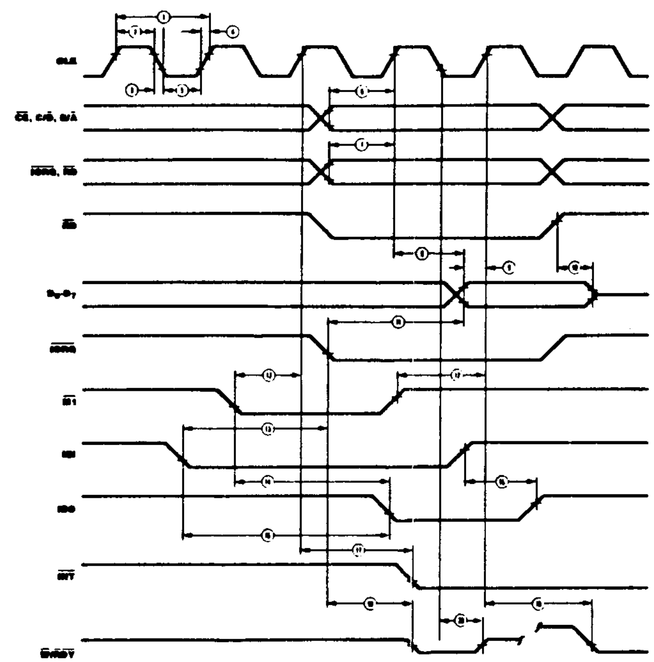

AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	Z80-4 DART Min	Z80-4 DART Max	Z80-6 DART Min	Z80-6 DART Max	Notes*
1	TwPh	Pulse Width (High)	200[c]		200[c]		2
2	TwPl	Pulse Width (Low)	200[c]		200[c]		2
3	TcTxC	$\overline{TxC}$ Cycle Time	400[c]	∞[c]	330[c]	∞[c]	2
4	TwTxCl	$\overline{TxC}$ Width (Low)	180[c]	∞[c]	100[c]	∞[c]	2
5	TwTxCh	$\overline{TxC}$ Width (High)	180[c]	∞[c]	100[c]	∞[c]	2
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay		300[a]		220[a]	2
7	TdTxC(W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5[c]	9[c]	5[c]	9[c]	1
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5[c]	9[c]	5[c]	9[c]	1
9	TcRxC	$\overline{RxC}$ Cycle Time	400[c]	∞[c]	330[c]	∞[c]	2
10	TwRxCl	$\overline{RxC}$ Width (Low)	180[c]	∞[c]	100[c]	∞[c]	2
11	TwRxCh	$\overline{RxC}$ Width (High)	180[c]	∞[c]	100[c]	∞[c]	2
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0[c]		0[c]		2
13	ThRxD(RxC)	RxD Hold Time (x1 Mode)	140[c]		100[c]		2
14	TdRxC(W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10[c]	13[c]	10[c]	13[c]	1
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10[c]	13[c]	10[c]	13[c]	1

* In all modes, the System Clock rate must be at least five times the maximum data rate. $\overline{RESET}$ must be active a minimum of one complete clock cycle.
1 Units equal to System Clock Periods.
2 Units in nanoseconds (ns).

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