UJA1162

Self-supplied high-speed CAN transceiver with Sleep mode

Rev. 1 — 26 September 2013 Product data sheet

1. General description

The UJA1162 is a ‘self-supplied’ high-speed CAN transceiver integrating an ISO 11898-2/5 compliant HS-CAN transceiver and an internal 5 V CAN supply. The only supply input is a battery connection. The UJA1162 can be operated in a very low-current Sleep mode with local and bus wake-up capability.

2. Features and benefits

2.1 General

- Self-supplied high-speed CAN transceiver
- ISO 11898-2 and ISO 11898-5 compliant
- Autonomous bus biasing according to ISO 11898-6
- Fully integrated 5 V supply (V_{BUF}) for the CAN transmitter/receiver
- VIO input allows for direct interfacing with 3.3 V to 5 V microcontrollers
- Bus connections are truly floating when power to pin BAT is off

2.2 Designed for automotive applications

- ±8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins
- ±6 kV ESD protection, according to IEC 61000-4-2 on the CAN bus pins and on pins BAT and WAKE
- CAN bus pins short-circuit proof to ±58 V
- Battery and CAN bus pins are protected against automotive transients according to ISO 7637-3
- Very low quiescent current in Sleep mode
- Leadless HVSON14 package (3 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Integrated supply voltage for the CAN transceiver (V_{BUF})

- 5 V nominal output; ±2 % accuracy
- Undervoltage detection at 90 % of nominal value
- Excellent response with a 4.7 µF ceramic output load capacitor
- Turned off in Sleep mode

2.4 Power Management

- Sleep mode featuring very low supply current
- Remote wake-up capability via standard CAN wake-up pattern
- Local wake-up capability via the WAKE pin
- Entire node can be powered down via the inhibit output, INH

2.5 System control and diagnostic features

- Mode control via SLPN pin
- Overtemperature shutdown
- Transmit data (TXD) dominant time-out function

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UJA1162TK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

4. Block diagram

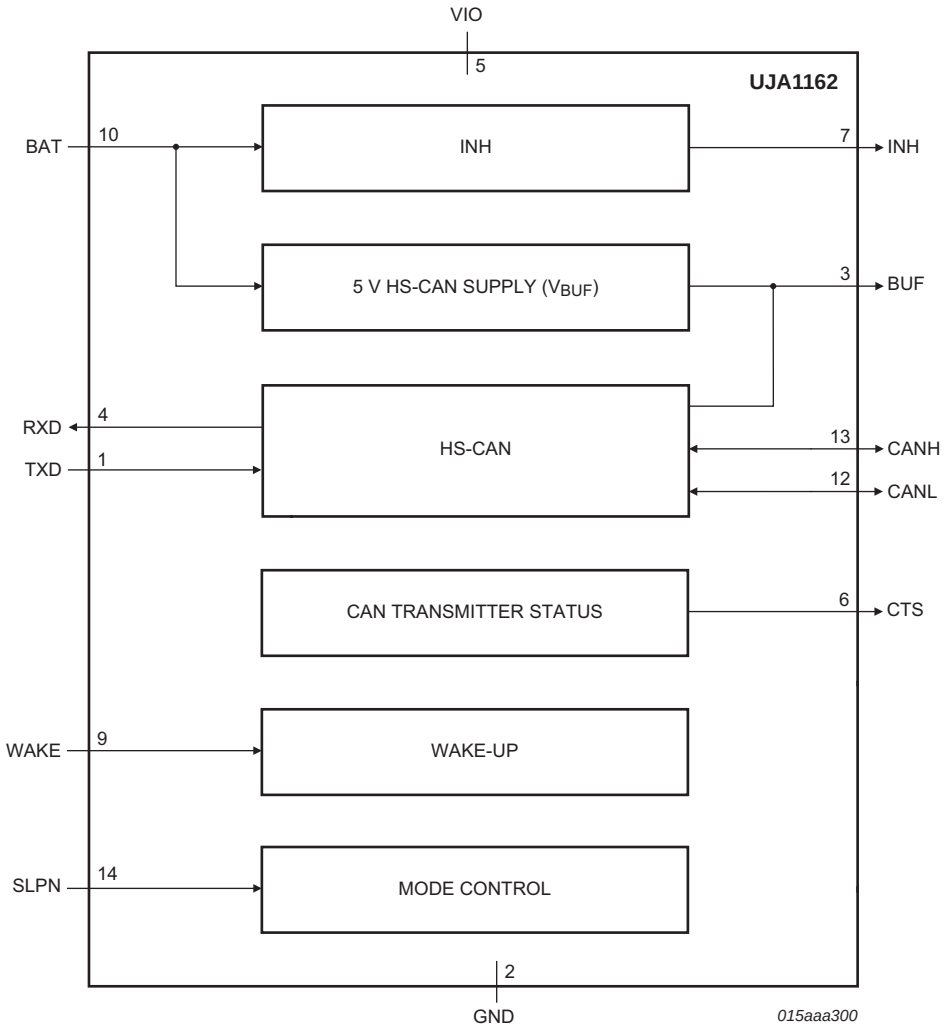


Fig 1. Block diagram of UJA1162

5. Pinning information

5.1 Pinning

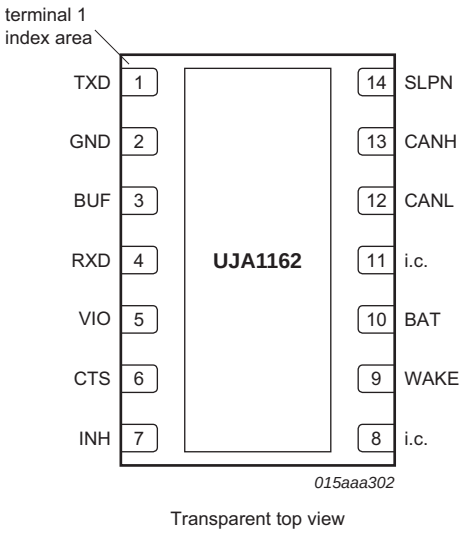


Fig 2. Pin configuration diagram

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground
BUF	3	5 V transceiver supply voltage
RXD	4	receive data output; reads out data from the bus lines
VIO	5	supply voltage for I/O level adaptor
CTS	6	CAN transmitter status
INH	7	inhibit output for switching external voltage regulators
i.c.	8	internally connected; should be left floating or connected to GND
WAKE	9	local wake-up input
BAT	10	battery supply voltage
i.c.	11	internally connected; should be left floating or connected to GND
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
SLPN	14	Sleep mode control input (active LOW)

[1] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended to also solder the exposed center pad to board ground.

6. Functional description

The UJA1162 is a self-supplied high-speed CAN transceiver incorporating a 5 V CAN supply. A variety of fail-safe and diagnostic features offer enhanced system reliability and advanced power management.

6.1 System controller

The system controller is a state machine that manages register configuration and controls the internal functions of the UJA1162. UJA1162 operating modes and state transitions are illustrated in Figure 3. These modes are discussed in more detail in the following sections.

6.1.1 Operating modes

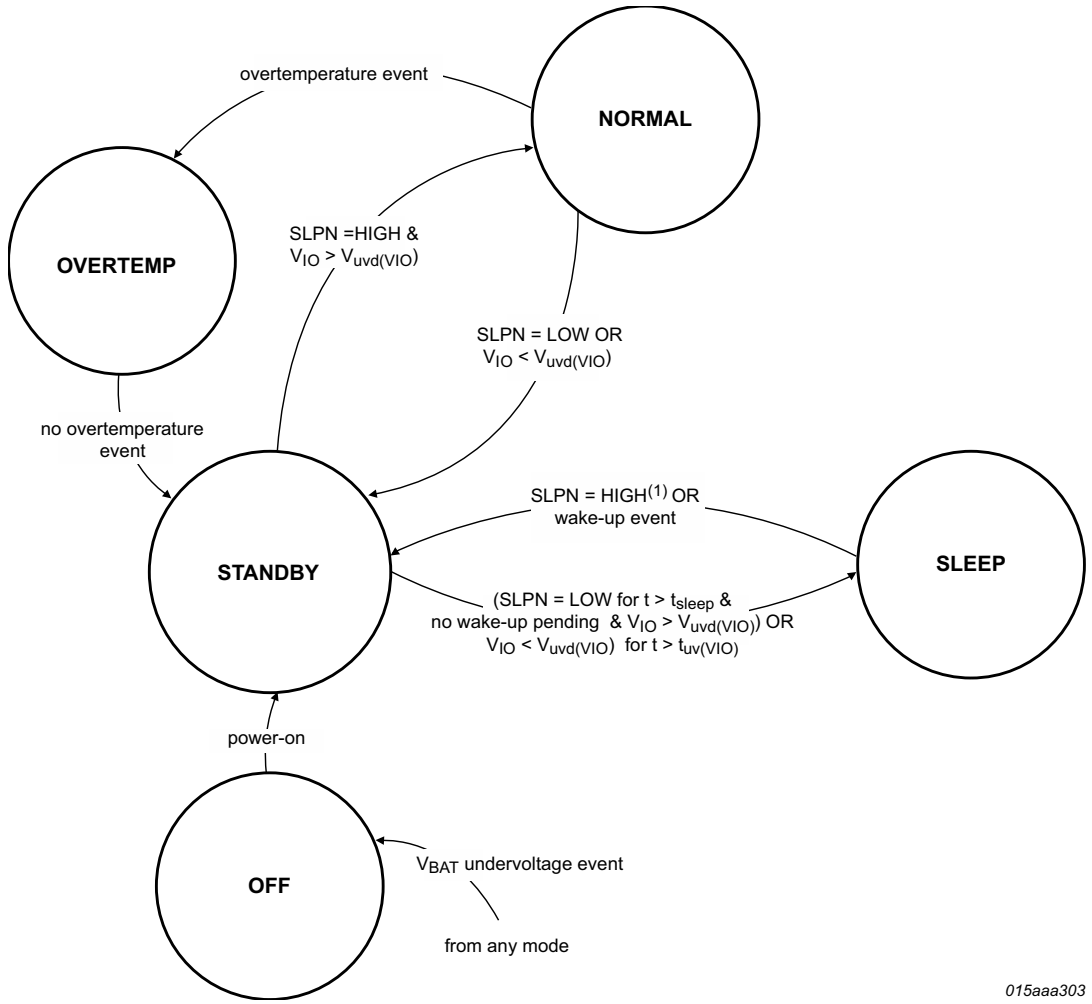
The UJA1162 supports five operating modes: Normal, Standby, Sleep, Overtemp and Off.

6.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, the UJA1162 is fully operational. Normal mode can be selected from Standby and Sleep (via Standby) modes by setting pin SLPN HIGH, provided $V_{IO} > V_{uvd(VIO)}$. The UJA1162 exits Normal mode:

- if the microcontroller selects Standby mode by setting pin SLPN LOW
- if the UJA1162 detects an undervoltage on VIO, causing the UJA1162 to switch to Standby mode
- if the chip temperature rises above $T_{th(act)otp}$, causing the UJA1162 to switch to Overtemp mode
- if the battery supply voltage drops below $V_{th(det)poff}$, causing the UJA1162 to switch to Off mode

All pending wake-up events (power-on, CAN bus wake-up, local wake-up via the WAKE pin) are cleared when the UJA1162 enters Normal mode.



(1) SLPN = HIGH is only possible in Sleep mode if a valid V_{IO} supply voltage is connected

Fig 3. UJA1162 system controller state diagram

6.1.1.2 Standby mode

Standby mode is a transitional mode between Normal and Sleep modes. The transceiver is unable to transmit or receive data in Standby mode, but pin INH is active.

The receiver monitors bus activity for a wake-up request in Standby mode. The bus pins are biased at GND level (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing). Wake-up can be triggered remotely via a standard wake-up pattern on the CAN bus (see Section 6.3.2) or locally via the WAKE pin. Pin RXD is forced LOW when a bus or local wake-up event is detected.

The UJA1162 switches to Standby mode:

- from Normal mode if pin SLPN goes LOW or and undervoltage is detected on VIO
- from Sleep mode in the event of a local or remote wake-up event or if SLPN = HIGH (with a valid voltage on VIO)

6.1.1.3 Sleep mode

Sleep mode is the UJA1162's power saving mode. In Sleep mode, the transceiver behaves like in Standby Mode with the exception that pin INH is set floating. Voltage regulators controlled by this pin will be switched off, and the current into pin BAT will be reduced to a minimum.

A HIGH level on SLPN (provided a valid voltage is present on VIO), a local wake-up via the WAKE pin or a remote CAN bus wake-up will cause the UJA1162 to wake up from Sleep mode and switch to Standby mode. Pin RXD is forced LOW when a local wake-up via WAKE or a remote bus wake-up is detected.

The UJA1162 can be set to Sleep mode by holding pin SLPN LOW for $t > t_{sleep}$ (provided there are no wake-up events pending). If one or more wake-up events is pending, the UJA1162 will remain in Standby mode. The UJA1162 must be switched to Normal mode to clear pending wake-up events.

The UJA1162 will also be forced to Sleep mode if an undervoltage lasting longer than $t_{d(uvd-slp)}$ is detected on VIO ($V_{IO} < V_{uvd(VIO)}$). In this event, all pending wake-up events will be cleared automatically.

6.1.1.4 Off mode

The UJA1162 switches to Off mode from any mode when $V_{BAT} < V_{th(det)poff}$. Only power-on detection is enabled; all other modules are inactive. The UJA1162 starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ (triggering an initialization process) and switches to Standby mode after $t_{startup}$. Pin RXD is driven LOW when the UJA1162 switches from Off mode to Standby mode, to indicate a power-on event has occurred.

In Off mode, the CAN pins disengage from the bus (zero load; high-ohmic).

6.1.1.5 Overtemp mode

Overtemp mode is provided to prevent the UJA1162 being damaged by excessive temperatures. The UJA1162 switches immediately to Overtemp mode from Normal mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. V_{BUF} is off in Overtemp mode.

The UJA1162 exits Overtemp mode:

- and switches to Standby mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

6.1.1.6 Hardware characterization for the UJA1162 operating modes

Table 3. Hardware characterization by functional block

Block	Operating mode				
	Off	**Standby**	**Normal**	**Overtemp**	**Sleep**
V_{BUF}	off	on/off[1]	on	off	off
CAN	floating	Offline	Active	floating	offline
RXD	V_{IO} level	V_{IO} level/LOW if wake-up detected	CAN bit stream	V_{IO} level/LOW if wake-up detected	V_{IO} level/LOW if wake-up detected
INH	off	V_{BAT} level	V_{BAT} level	V_{BAT} level	off

[1] V_{BUF} is switched on in Standby mode if a CAN wake-up pattern is detected on the bus; if pin SLPN does not go HIGH within $t_{to(silence)}$, V_{BUF} is switched off again. V_{BUF} is also switched on in Standby mode if SLPN goes HIGH to select Normal mode.

6.1.2 Mode control via pin SLPN

The UJA1162 can be switched between Normal and Standby/Sleep modes via the SLPN control input (see Figure 3). When SLPN goes LOW, the UJA1162 switches to Standby mode. If SLPN remains low for t_{sleep}, the UJA1162 then switches to Sleep mode (if no wake-up is pending). When SLPN goes HIGH, the UJA1162 switches to Normal mode.

6.2 Power supplies

6.2.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device needs to be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the UJA1162 switches to Off mode, which means that the internal 5 V CAN supply and other internal logic (except for power-on detection) are shut down.

The UJA1162 switches from Off mode to Standby mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. A power-on event is indicated by a LOW level on pin RXD. RXD remains LOW from the moment UJA1162 exits Off mode until it switches to Normal mode.

6.2.2 CAN supply voltage (V_{BUF})

V_{BUF} provides the internal CAN transceiver with a 5 V supply. The output voltage on BUF is monitored. If V_{BUF} falls below the 90 % undervoltage threshold (90 % of the nominal V_{BUF} output voltage), the CAN transceiver switches to (or remains in) Offline mode.

6.3 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2 and ISO 11898-5 compliant. The CAN transmitter is supplied from V_{BUF}.

The CAN transceiver supports autonomous CAN biasing as defined in ISO 11898-6, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the UJA1162 is in Normal mode with V_{BUF} > 90 % threshold. Autonomous biasing is active when the UJA1162 is in Standby or Sleep mode with the CAN transceiver in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there

is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode). This is useful when the node is disabled due to a malfunction in the microcontroller. The transceiver ensures that the CAN bus is correctly biased to avoid disturbing ongoing communication between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

6.3.1 CAN operating modes

The integrated CAN transceiver supports three operating modes: Active, Offline and Offline Bias (see Figure 5). The CAN transceiver operating mode depends on the UJA1162 operating mode and the output voltage on pin BUF.

6.3.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

The CAN transceiver is in Active mode when:

- the UJA1162 is in Normal mode (SLPN = 1) AND
- $V_{BUF} > V_{uvd(BUF)}$ AND
- $V_{IO} > V_{uvd(VIO)}$

In CAN Active mode, the CAN bias voltage is derived from V_{BUF}. If V_{BUF} falls below $V_{uvd(BUF)}$, the UJA1162 exits CAN Active mode and enters CAN Offline Bias mode with autonomous CAN voltage biasing via pin BAT.

If pin TXD is LOW when the transceiver switches to CAN Active mode (UJA1162 in Normal mode; V_{BUF} and V_{IO} ok), the transmitter and receiver will remain disabled until TXD goes HIGH. This prevents network traffic being blocked for $t_{to(dom)TXD}$ (i.e. while the TXD dominant time-out timer is running; see Section 6.7.1) every time the transceiver enters Active mode, if the TXD pin is clamped permanently LOW.

6.3.1.2 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event. CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver will switch from CAN Active mode to CAN Offline Bias mode if:

- the UJA1162 switches to Standby/Sleep mode while the CAN bus had been inactive for less than $t_{to(silence)}$ OR
- $V_{BUF} < V_{uvd(BUF)}$ OR $V_{IO} < V_{uvd(VIO)}$

The CAN transceiver will switch directly from CAN Active mode to CAN Offline mode if:

- the UJA1162 switches to Standby/Sleep mode after the CAN bus had been inactive for more than $t_{to(silence)}$

The CAN transceiver switches from CAN Offline Bias mode to CAN Offline mode:

- when the UJA1162 is in Standby/Sleep mode AND
- no activity has been detected on the bus for $t > t_{to(silence)}$

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a wake-up event is detected on the CAN bus OR
- the UJA1162 switches to Normal mode while $V_{BUF} < V_{uvd(BUF)}$ OR $V_{IO} < V_{uvd(VIO)}$

6.3.1.3 CAN off

The CAN transceiver is switched off completely with the bus lines floating when:

- the UJA1162 switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage release threshold and the UJA1162 is no longer in Off/Overtemp mode.

6.3.2 CAN standard wake-up

The UJA1162 monitors the bus for a wake-up pattern when the CAN transceiver is in Offline mode.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 4; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

Pin RXD is driven LOW when a valid CAN wake-up pattern is detected on the bus.

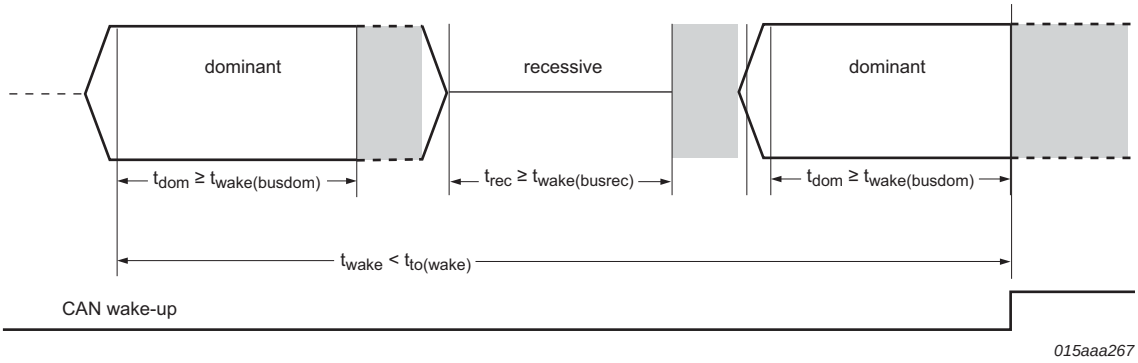


Fig 4. CAN wake-up timing

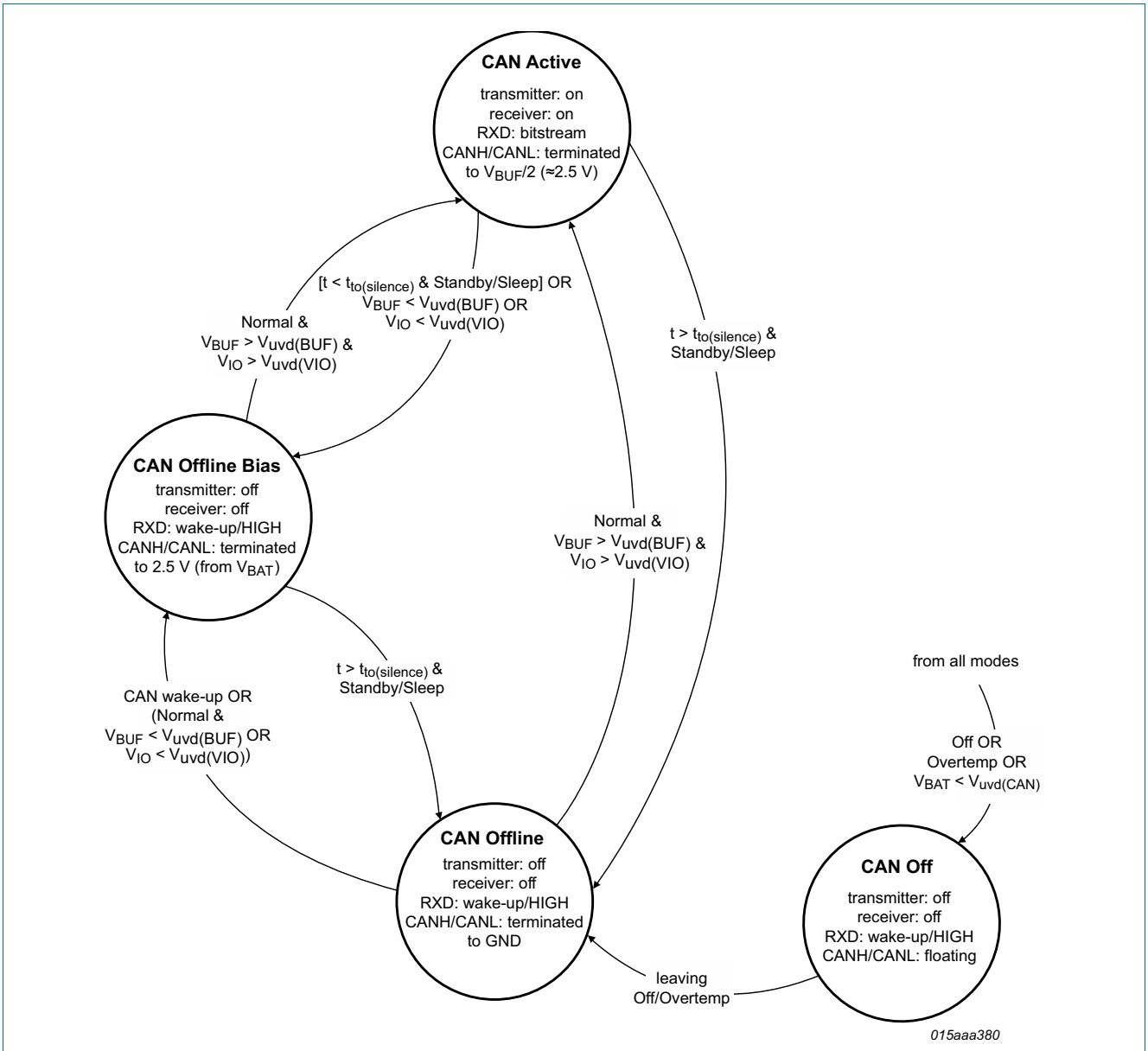


Fig 5. CAN transceiver state machine

6.4 WAKE pin

In Standby and Sleep modes, a local wake-up event is triggered by a LOW-to-HIGH or a HIGH-to-LOW transition on the WAKE pin. In applications that don't make use of the local wake-up facility, the WAKE pin should be connected to GND for optimal EMI performance.

6.5 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels on TXD, RXD, SLPN and CTS to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

6.6 CAN transmit status pin (CTS)

Pin CTS is driven HIGH to indicate to the microcontroller that the transmitter is fully enabled and data can be transmitted via the TXD pin.

Pin CTS is actively driven LOW:

- while the transmitter is starting up (e.g. during a transition from Standby to Normal mode) or
- if pin TXD is clamped LOW for $t > t_{to(dom)TXD}$ or
- if an undervoltage is detected on VIO or BUF

6.7 CAN fail-safe features

6.7.1 TXD dominant timeout

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network traffic). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

6.7.2 Pull-up on TXD pin

Pin TXD has an internal pull-up (towards V_{IO}) to ensure a safe defined recessive driver state in case the pin is left floating.

6.7.3 Pull-down on SLPN pin

Pin SLPN has an internal pull-down (to GND) to ensure the UJA1162 switches to Sleep mode if SLPN is left floating.

6.7.4 Loss of power at pin BAT

A loss of power at pin BAT has no impact on the bus lines or on the microcontroller. No reverse currents flow from the bus.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x	DC value				
		pins BUF[1], VIO		–0.2	+6	V
		pins TXD, RXD, SLPN, CTS		–0.2	V_{IO} + 0.2	V
		pins WAKE, INH		–18	+40	V
		pin BAT		–0.2	+40	V
		pins CANH and CANL with respect to any other pin		–58	+58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL			–40	+40	V
V_{trt}	transient voltage	on pins	[2]	–150	+100	V
		BAT: via reverse polarity diode and capacitor to ground				
		CANL, CANH, WAKE: coupling via 1 nF capacitors				
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2	[3]			
		on pins CANH and CANL; pin BAT with capacitor; pin WAKE with 10 nF capacitor and 10 kΩ resistor		–6	+6	kV
		HBM	[4]			
		on pins CANH, CANL	[5]	–8	+8	kV
		on pins BAT, WAKE		–4	+4	kV
		on any other pin		–2	+2	kV
		MM	[6]			
		on any pin		–100	+100	V
		CDM	[7]			
		on corner pins		–750	+750	V
		on any other pin		–500	+500	V
T_{vj}	virtual junction temperature		[8]	–40	+150	°C
T_{stg}	storage temperature			–55	+175	°C

[1] When the device is not powered up, $I_{BUF(max)}$ = 25 mA.

[2] Verified by an external test house to ensure pins can withstand ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.

[3] ESD performance according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house; the result was equal to or better than ±6 kV.

[4] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[5] Pins BUF, VIO and BAT connected to GND, emulating the application circuit.

[6] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[7] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient		[1]	60	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

9. Static characteristics

Table 6. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; $R_{(CANH-CANL)}$ =60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} rising	4.2	-	4.55	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} rising	4.5	-	5	V
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	V_{BAT} falling	4.2	-	4.55	V
I_{BAT}	battery supply current	Standby mode; CAN Offline mode; −40 °C < T_{vj} < +85 °C; V_{BAT} = 7 V to 18 V	-	58	81	μA
		Sleep mode; CAN Offline mode; −40 °C < T_{vj} < +85 °C; V_{BAT} = 7 V to 18 V	-	44	62	μA
		additional current in CAN Offline Bias mode; −40 °C < T_{vj} < 85 °C	-	46	63	μA
		Normal mode; CAN Active mode; CAN recessive; V_{TXD} = V_{IO}	-	4	7.5	mA
		Normal mode; CAN Active mode; CAN dominant; V_{TXD} = 0 V	-	46	67	mA
Voltage source; pin BUF						
V_O	output voltage	V_{BAT} = 5.5 V to 18 V	4.9	5	5.1	V
V_{uvd}	undervoltage detection voltage		4.5	-	4.75	V
$I_{O(sc)}$	short-circuit output current		−300	-	−150	mA
Supply; pin VIO						
V_{uvd}	undervoltage detection voltage		2.7	-	2.85	V
$I_{I(VIO)}$	input current on pin VIO	Standby/Normal mode; −40 °C < T_{vj} < 85 °C	-	7.1	11	μA
		Sleep mode; −40 °C < T_{vj} < 85 °C	-	5.9	9.5	μA

Table 6. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; $R_{(CANH-CANL)}$ =60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Sleep mode control input; pin SLPN							
$V_{th(sw)}$	switching threshold voltage			$0.25V_{IO}$	-	$0.75V_{IO}$	V
R_{pd}	pull-down resistance			40	60	80	kΩ
Inhibit output: pin INH							
V_O	output voltage	I_{INH} = −180 µA		V_{BAT} − 0.8	-	V_{BAT}	V
R_{pd}	pull-down resistance	Sleep mode		3	4	5	MΩ
CAN transmit data input; pin TXD							
$V_{th(sw)}$	switching threshold voltage			$0.25V_{IO}$	-	$0.75V_{IO}$	V
R_{pu}	pull-up resistance			40	60	80	kΩ
CAN transmitter status; pin CTS							
I_{OH}	HIGH-level output current	V_{CTS} = V_{IO} − 0.4 V; transmitter on		-	-	−4	mA
I_{OL}	LOW-level output current	V_{CTS} = 0.4 V; transmitter off		4	-	-	mA
CAN receive data output; pin RXD							
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		V_{IO} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
R_{pu}	pull-up resistance	CAN Offline mode		40	60	80	kΩ
Local wake input; pin WAKE							
$V_{th(sw)r}$	rising switching threshold voltage			2.8	-	4.1	V
$V_{th(sw)f}$	falling switching threshold voltage			2.4	-	3.75	V
$V_{hys(i)}$	input hysteresis voltage			250	-	800	mV
I_i	input current	T_{vj} = −40 °C to +85 °C		-	-	1.5	µA
High-speed CAN bus lines; pins CANH and CANL							
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{TXD} = 0 V; V_{BAT} > 5.5 V					
		pin CANH		2.75	3.5	4.5	V
		pin CANL		0.5	1.5	2.25	V
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; f_{TXD} = 250 kHz; C_{SPLIT} = 4.7 nF	[1] [2]	$0.9V_{BUF}$	-	$1.1V_{BUF}$	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{BUF} − V_{CANH} − V_{CANL}; V_{BAT} > 5.5 V		−400	-	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	CAN Active mode (dominant); V_{TXD} = 0 V; V_{BAT} > 5.5 V $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω;		1.5	-	3.0	V
		CAN Active mode (recessive); CAN Offline mode; V_{TXD} = V_{IO}; $R_{(CANH-CANL)}$ = no load; V_{BAT} > 5.5 V; T_{vj} < 150 °C		−50	-	+50	mV

Table 6. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; $R_{(CANH-CANL)}$ =60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(rec)}$	recessive output voltage	CAN Active mode; $V_{TXD} = V_{IO}$; V_{BAT} > 5.5 V; $R_{(CANH-CANL)}$ = no load	2	0.5V_{BUF}	3	V
		CAN Offline mode; V_{BAT} > 5.5 V; $R_{(CANH-CANL)}$ = no load	−0.1	-	+0.1	V
		CAN Offline Bias mode; $R_{(CANH-CANL)}$ = no load	2	2.5	3	V
$I_{O(dom)}$	dominant output current	CAN Active mode; V_{BAT} > 5.5 V; V_{TXD} = 0 V				
		pin CANH; V_{CANH} = 0 V	−50	-	-	mA
		pin CANL; V_{CANL} = 5 V	-	-	52	mA
$I_{O(rec)}$	recessive output current	$V_{CANL} = V_{CANH}$ = −27 V to +32 V; $V_{TXD} = V_{IO}$	−3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	CAN Active mode; $V_{CANL} = V_{CANH}$ = −12 V to +12 V; V_{BAT} > 5.5 V	0.5	0.7	0.9	V
		CAN Offline mode; $V_{CANL} = V_{CANH}$ = −12 V to +12 V; V_{BAT} > 5.5 V	0.4	0.7	1.15	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active mode; $V_{CANL} = V_{CANH}$ = −12 V to +12 V; V_{BAT} > 5.5 V	50	200	400	mV
$R_{i(cm)}$	common-mode input resistance		9	15	28	kΩ
ΔR_i	input resistance deviation		−1	-	+1	%
$R_{i(dif)}$	differential input resistance		19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[1]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[1]	-	-	10	pF
I_{LI}	input leakage current	$V_{BAT} = V_{BUF}$ = 0 V or $V_{BAT} = V_{BUF}$ = shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V	−5	-	+5	µA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		167	177	187	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		127	137	147	°C

[1] Not tested in production; guaranteed by design.

[2] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 9.

10. Dynamic characteristics

Table 7. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; $R_{(CANH-CANL)}$ = 60 Ω; $C_{(CANH-CANL)}$ = 100 pF; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage sources; pins BUF and VIO						
$t_{startup}$	start-up time	from V_{BAT} exceeding the power-on detection threshold until V_{BUF} > 90 % undervoltage threshold	-	2.8	4.7	ms
$t_{d(uvd)}$	undervoltage detection delay time		6	-	39	µs
$t_{d(uvd-sleep)}$	delay time from undervoltage detection to sleep mode	from undervoltage detection on VIO until UJA1162 forced to Sleep mode	200	-	400	ms
Mode control: pin SLPN						
$t_{fltr(sleep)}$	sleep filter time		2.5	-	13.5	µs
$t_{d(sleep)}$	sleep delay time	minimum LOW time to trigger a transition to Sleep mode	21	-	36	µs
Pin WAKE						
$t_{det(wake)}$	wake-up detection time		7	-	42	µs
CAN transceiver timing; pins CANH, CANL, TXD and RXD						
$t_{d(TXD-RXD)}$	delay time from TXD to RXD	50 % V_{TXD} to 50 % V_{RXD}; C_{RXD} = 15 pF; f_{TXD} = 250 kHz	-	-	255	ns
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant		-	80	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive		-	80	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	C_{RXD} = 15 pF	-	105	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	C_{RXD} = 15 pF	-	120	-	ns
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	3.0	µs
		second pulse for wake-up on pins CANH and CANL	0.5	-	3.0	µs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	3.0	µs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	3.0	µs
$t_{to(wake)}$	wake-up time-out time	between first and second dominant pulses; CAN Offline mode	570	-	1200	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; V_{TXD} = 0 V	2.7	-	3.3	ms

Table 7. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; $R_{(CANH-CANL)}$ = 60 Ω; $C_{(CANH-CANL)}$ = 100 pF; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes; R_L = 120 Ω	0.95	-	1.17	s
$t_{d(busact-bias)}$	delay time from bus active to bias		-	-	200	µs
$t_{startup(CAN)}$	CAN start-up time	when switching to Active mode (CTS = 1)	-	-	220	µs

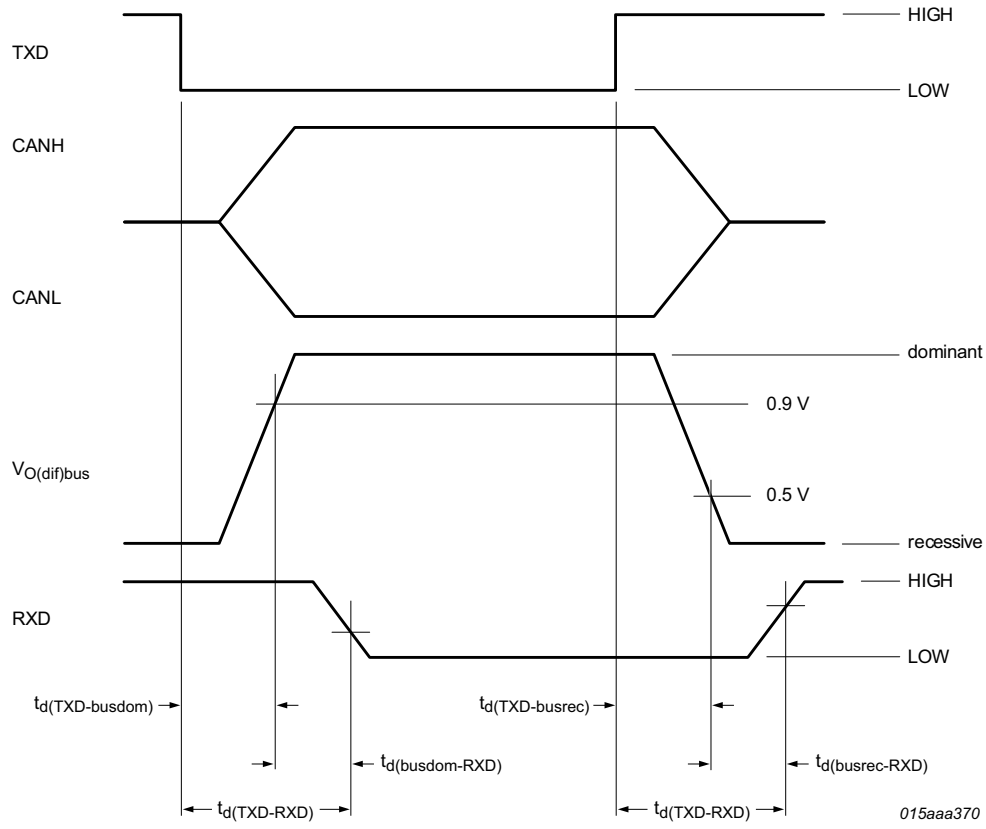
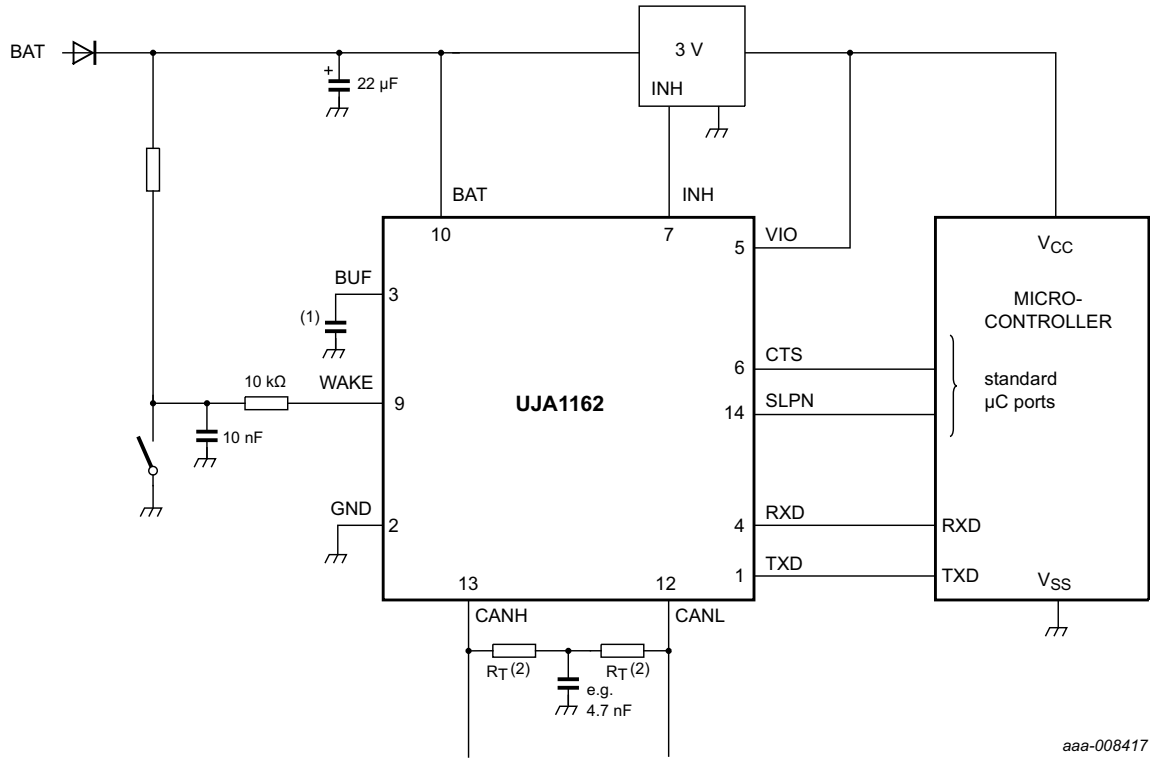


Fig 6. CAN transceiver timing diagram

11. Application information

11.1 Application diagram



(1) Actual capacitance value must be a least 1.76 µF with 5 V DC offset (recommended capacitor value is 4.7 µF)

(2) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 7. Typical application using the UJA1162

12. Test information

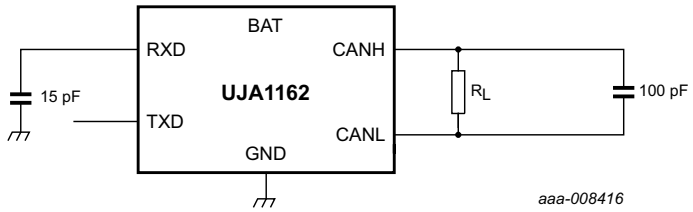


Fig 8. Timing test circuit for CAN transceiver

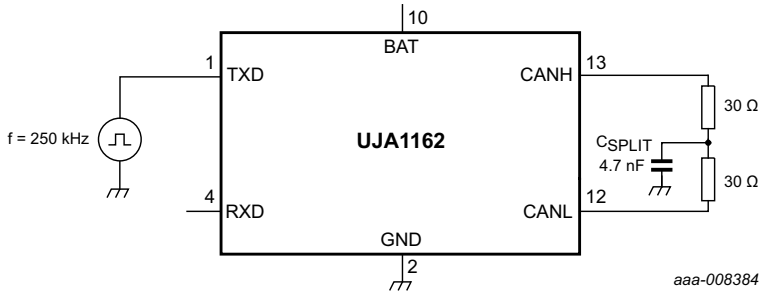


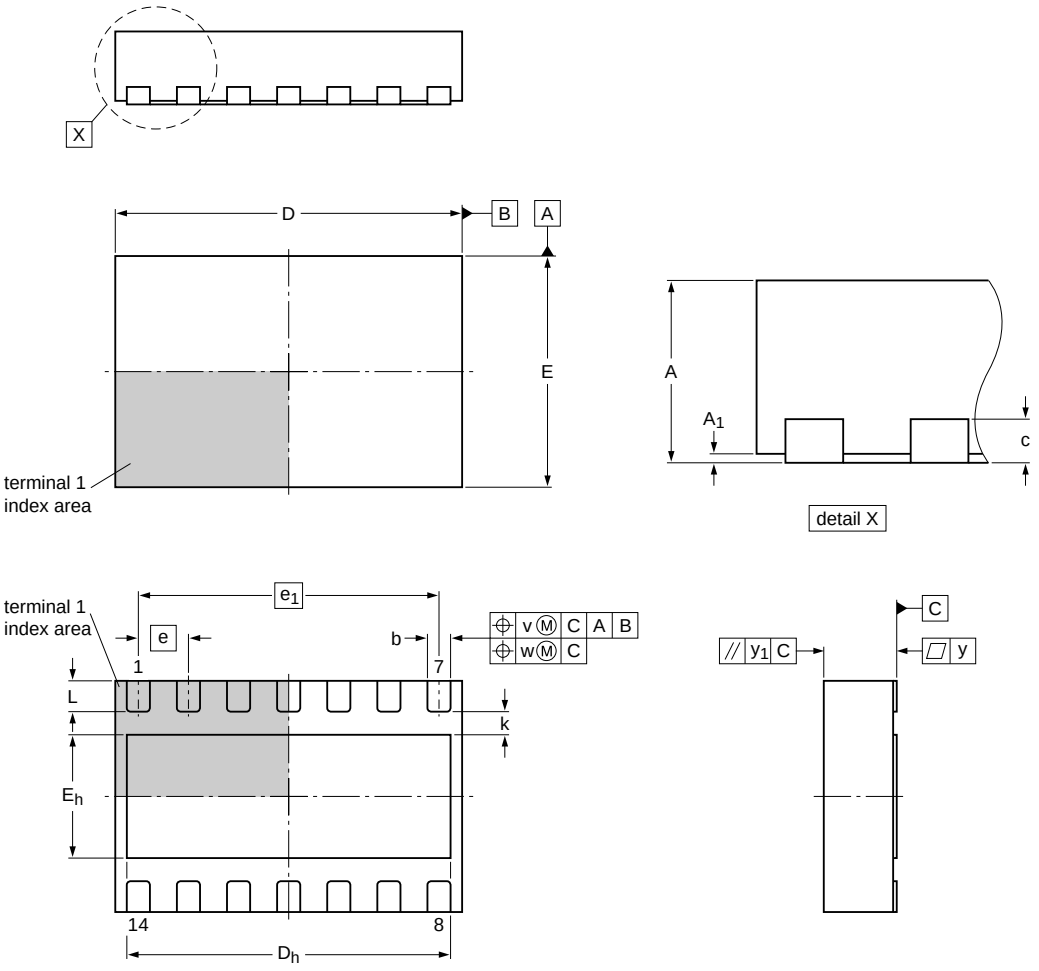
Fig 9. Test circuit for measuring transceiver driver symmetry

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13. Package outline

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Fig 10. Package outline SOT1086-2 (HVSON14)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020D)

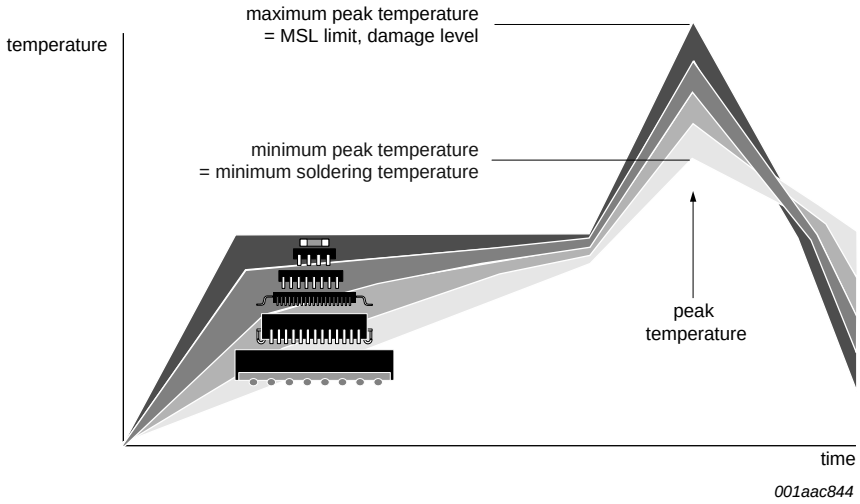
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Soldering of HVSON packages

Section 15 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UJA1162 v.1	20130926	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

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