



**Advanced Power
Electronics Corp.**

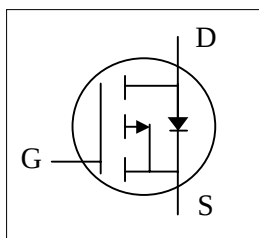
AP4435GH/J-HF

Halogen-Free Product

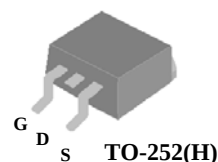
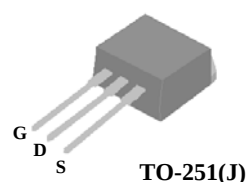
P-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



BV_{DS}	-30V
$R_{DS(ON)}$	20m Ω
I_D	-40A



Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters. The through-hole version (AP4435GJ) is available for low-profile applications.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	-40	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	-25	A
I_{DM}	Pulsed Drain Current ¹	-150	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	44.6	W
	Linear Derating Factor	0.36	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	2.8	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	62.5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	110	$^\circ\text{C}/\text{W}$



AP4435GH/J-HF

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.02	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-26A	-	-	20	mΩ
		V _{GS} =-4.5V, I _D =-16A	-	-	36	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-26A	-	31	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =-24V, V _{GS} =0V	-	-	-250	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-26A	-	16.5	32	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-25V	-	2.7	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	11	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-15V	-	7.5	-	ns
t _r	Rise Time	I _D =-26A	-	64	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =-10V	-	24	-	ns
t _f	Fall Time	R _D =0.58Ω	-	92	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1160	1970	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	195	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	175	-	pF
R _g	Gate Resistance	f=1.0MHz	-	5	17	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =-26A, V _{GS} =0V	-	-	-1.3	V
t _{rr}	Reverse Recovery Time ²	I _S =-10A, V _{GS} =0V,	-	25	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	15	-	nC

Notes:

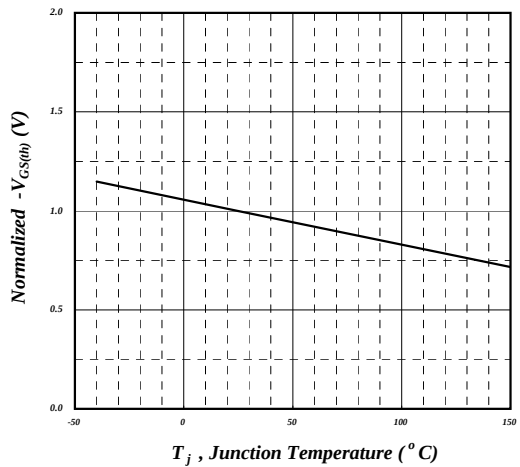
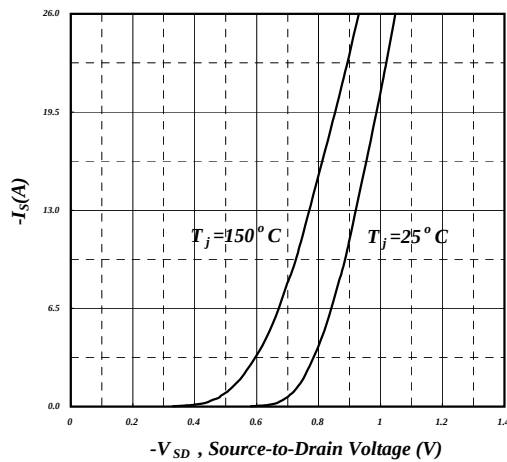
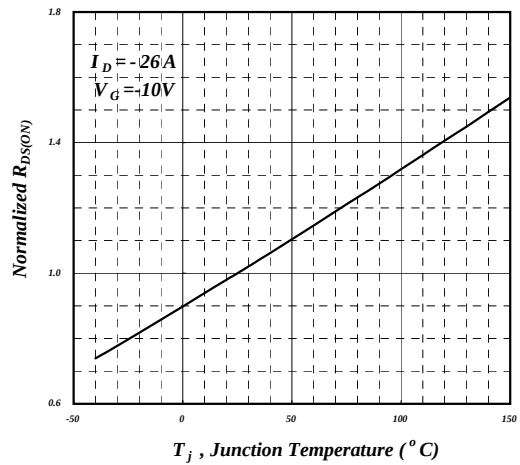
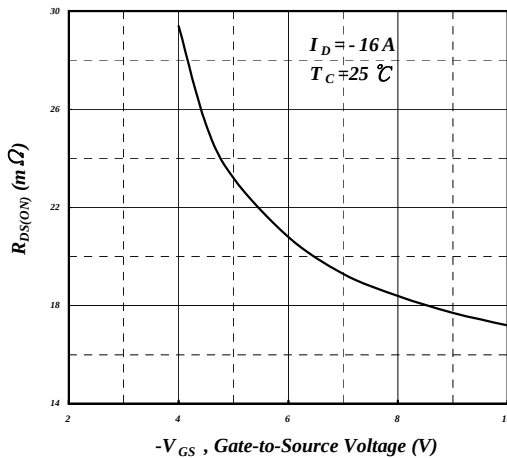
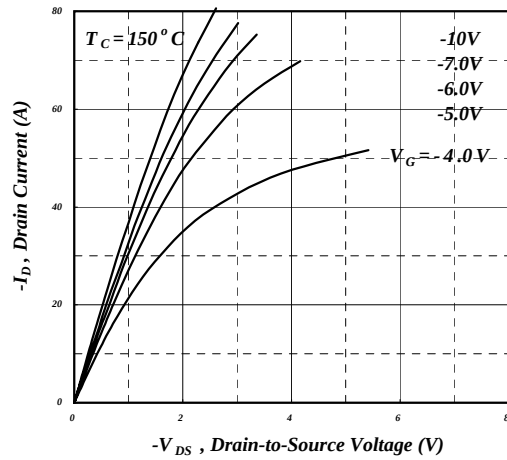
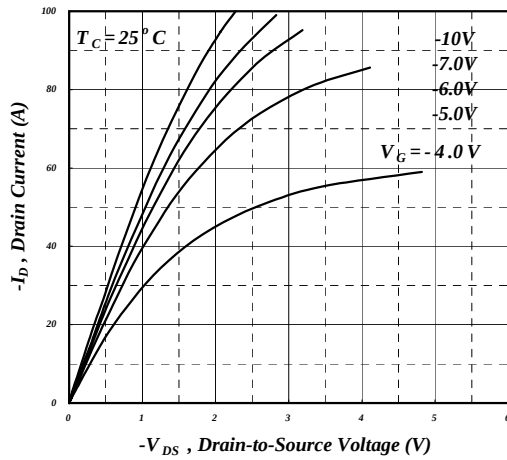
- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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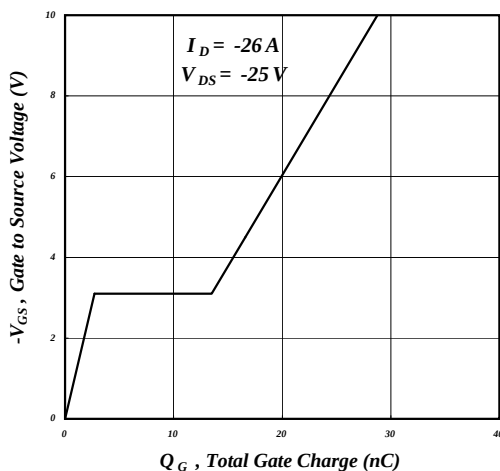


Fig 7. Gate Charge Characteristics

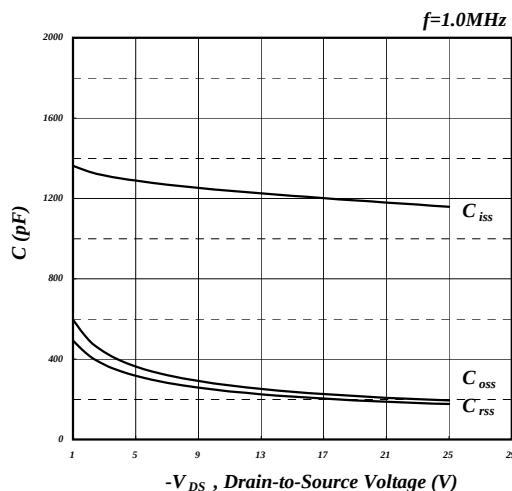


Fig 8. Typical Capacitance Characteristics

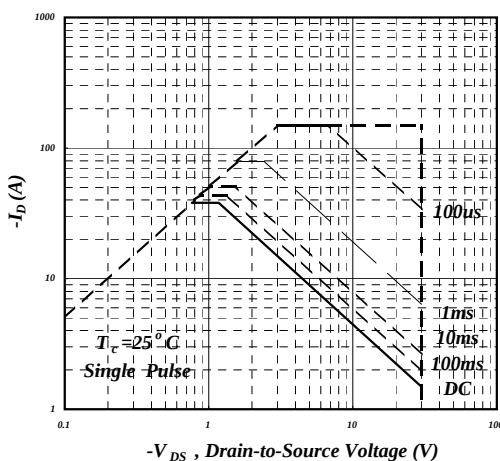


Fig 9. Maximum Safe Operating Area

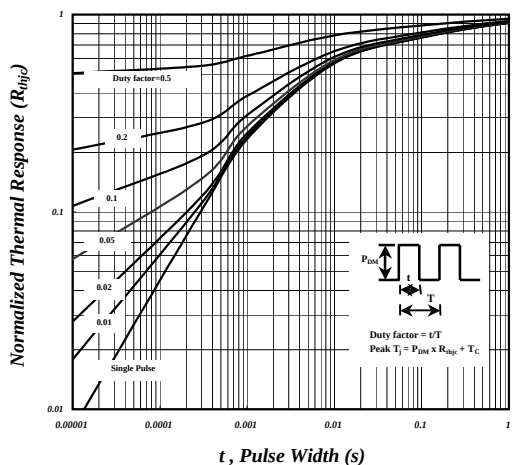


Fig 10. Effective Transient Thermal Impedance

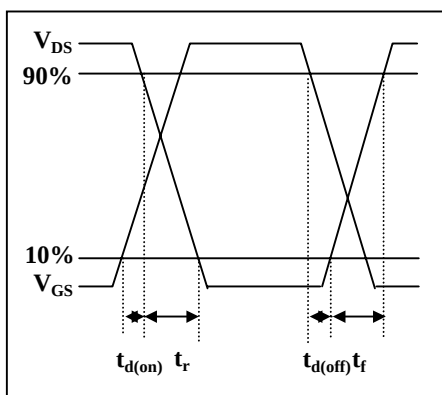


Fig 11. Switching Time Waveform

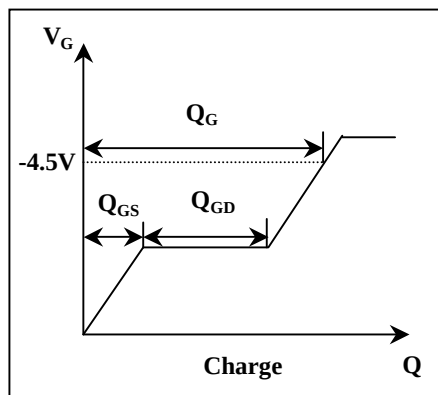


Fig 12. Gate Charge Waveform