

2N7002E

N-channel TrenchMOS FET

Rev. 03 — 28 April 2006

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level threshold compatible
- Surface-mounted package
- Very fast switching
- TrenchMOS technology

1.3 Applications

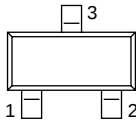
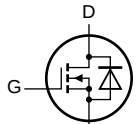
- Logic level translator
- High-speed line driver

1.4 Quick reference data

- $V_{DS} \leq 60 \text{ V}$
- $R_{DS(on)} \leq 3 \Omega$
- $I_D \leq 385 \text{ mA}$
- $P_{tot} \leq 0.83 \text{ W}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	 SOT23	 mbb076
2	source (S)		
3	drain (D)		

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3. Ordering information

Table 2: Ordering information

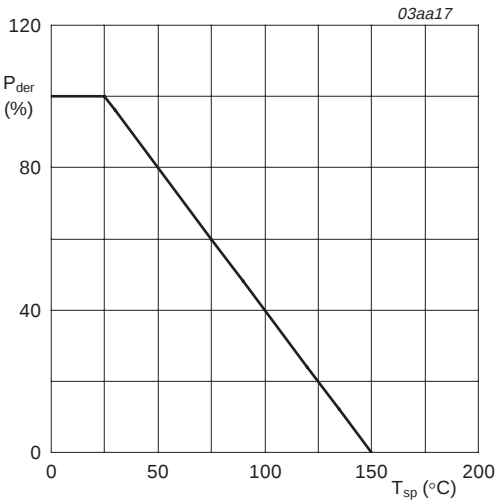
Type number	Package		
	Name	Description	Version
2N7002E	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Limiting values

Table 3: Limiting values

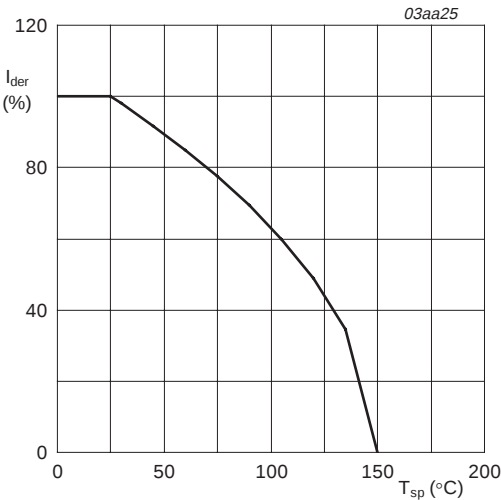
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-	± 30	V
V_{GSM}	peak gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$; pulsed; duty cycle = 25 %	-	± 40	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	385	mA
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	245	mA
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	1.5	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	0.83	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	385	mA
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	1.5	mA



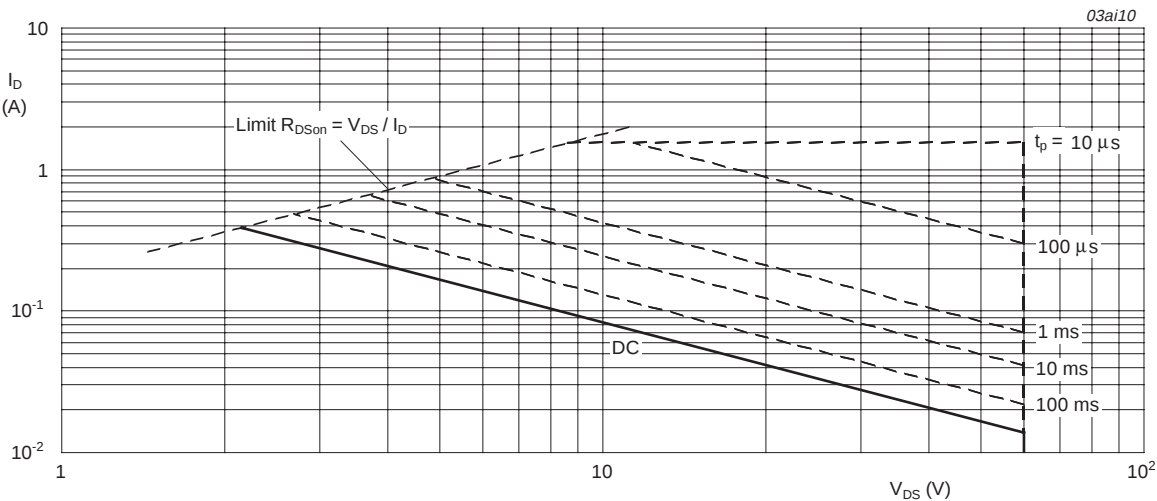
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

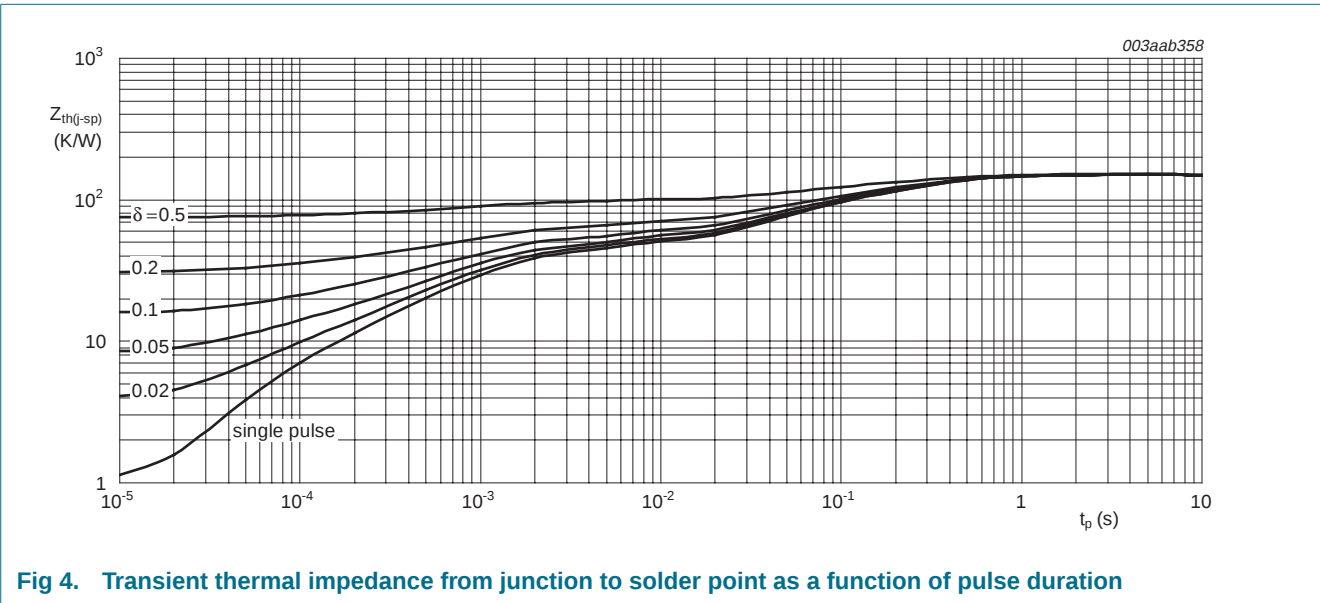
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	350	K/W

[1] Mounted on a printed-circuit board; minimum footprint; vertical in still air

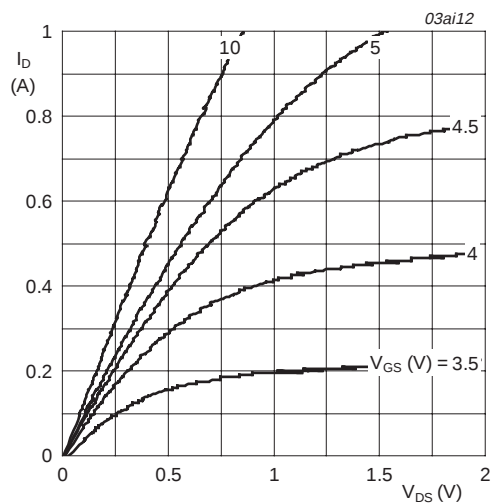


6. Characteristics

Table 5: Characteristics

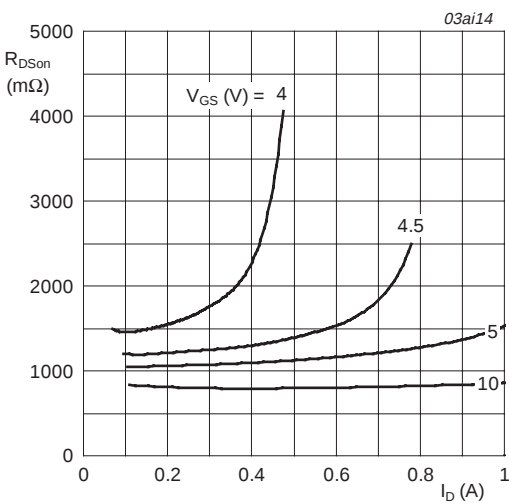
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	60	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	1	2	2.5	V
		$T_j = 150\text{ }^{\circ}\text{C}$	0.6	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	2.75	V
I_{DSS}	drain leakage current	$V_{DS} = 48\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^{\circ}\text{C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 500\text{ mA}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	0.78	3	Ω
		$T_j = 150\text{ }^{\circ}\text{C}$	-	1.45	5.5	Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 75\text{ mA}$; see Figure 6 and 8	-	1.2	4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 300\text{ mA}$; $V_{DS} = 30\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 11 and 12	-	0.69	-	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.27	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$; see Figure 14	-	31	50	pF
C_{oss}	output capacitance		-	6.8	30	pF
C_{rss}	reverse transfer capacitance		-	3.5	10	pF
t_{on}	turn-on time	$V_{DS} = 50\text{ V}$; $R_L = 250\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 50\text{ }\Omega$; $R_{GS} = 50\text{ }\Omega$	-	2.5	10	ns
t_{off}	turn-off time		-	11	15	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 300\text{ mA}$; $V_{GS} = 0\text{ V}$; see Figure 13	-	0.85	1.5	V
t_{rr}	reverse recovery time	$I_S = 300\text{ mA}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	30	-	ns
Q_r	recovered charge		-	30	-	nC



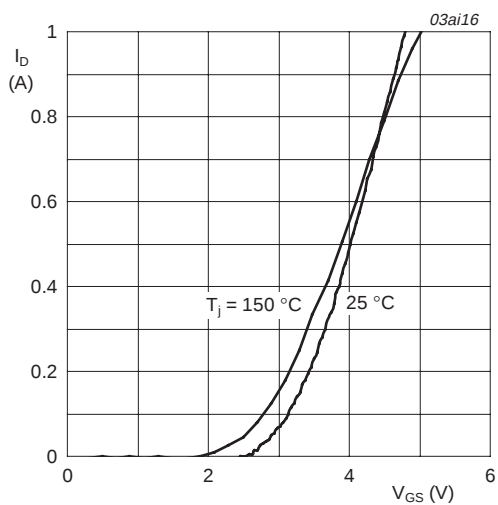
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



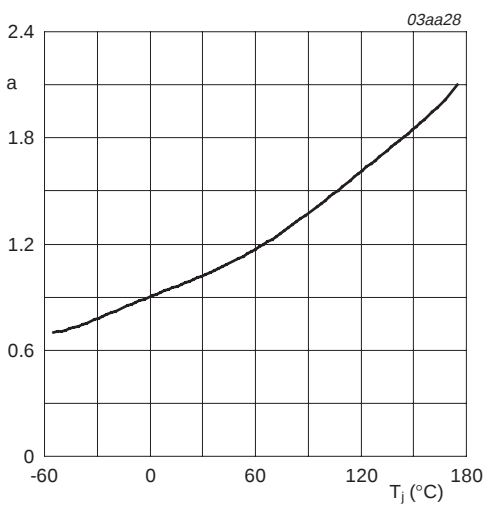
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



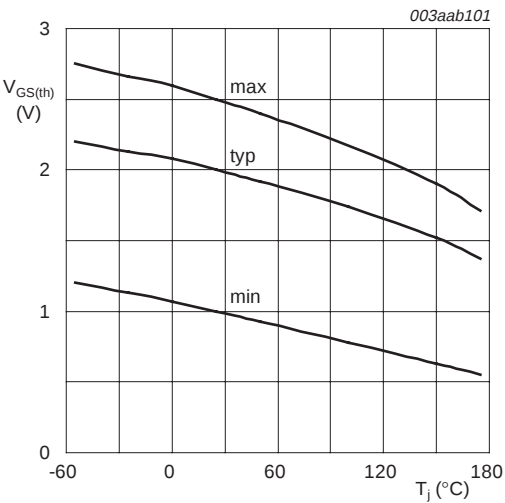
T_j = 25 °C and 150 °C; V_{DS} > I_D × R_{DSon}

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



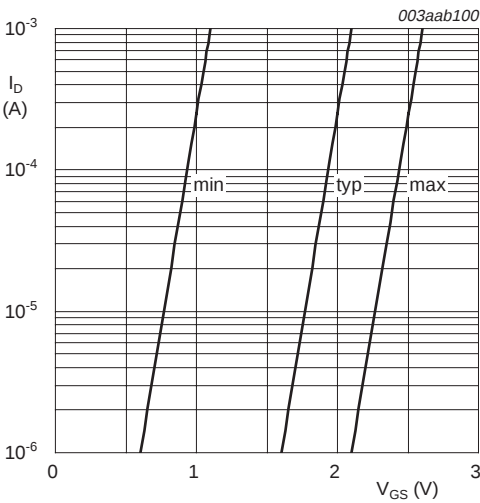
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



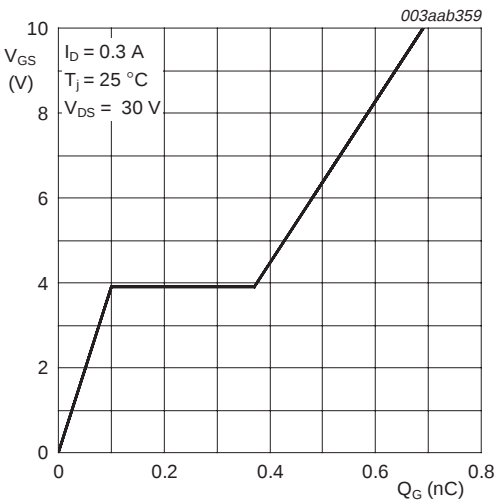
$I_D = 0.25 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ °C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 0.3 \text{ A}$; $V_{DS} = 30 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

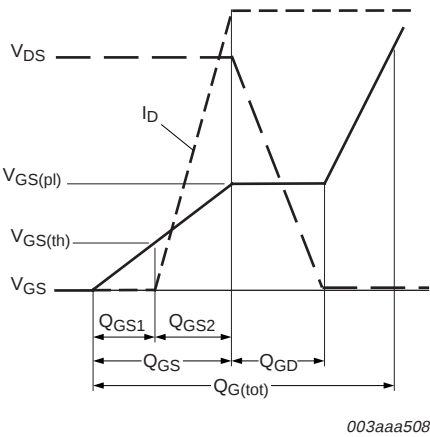
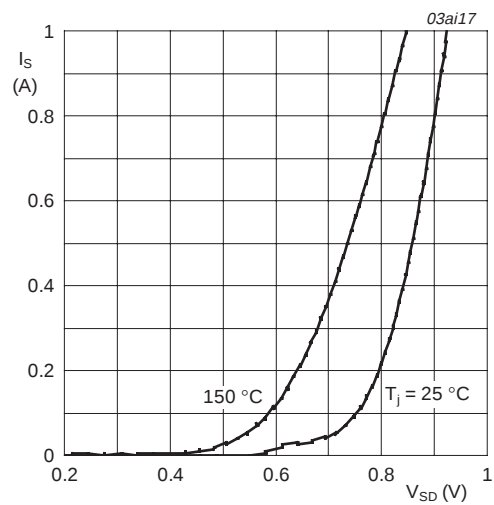
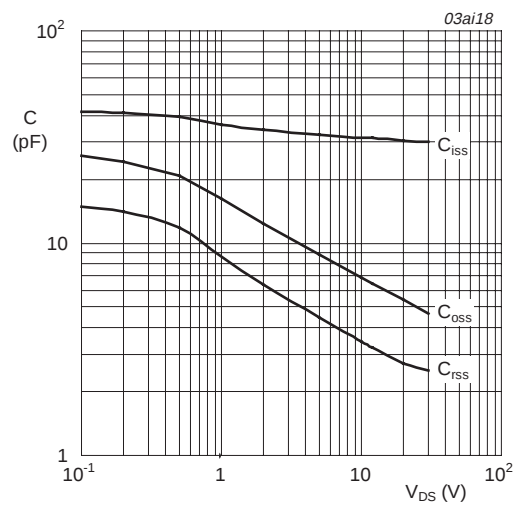


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface-mounted package; 3 leads

SOT23

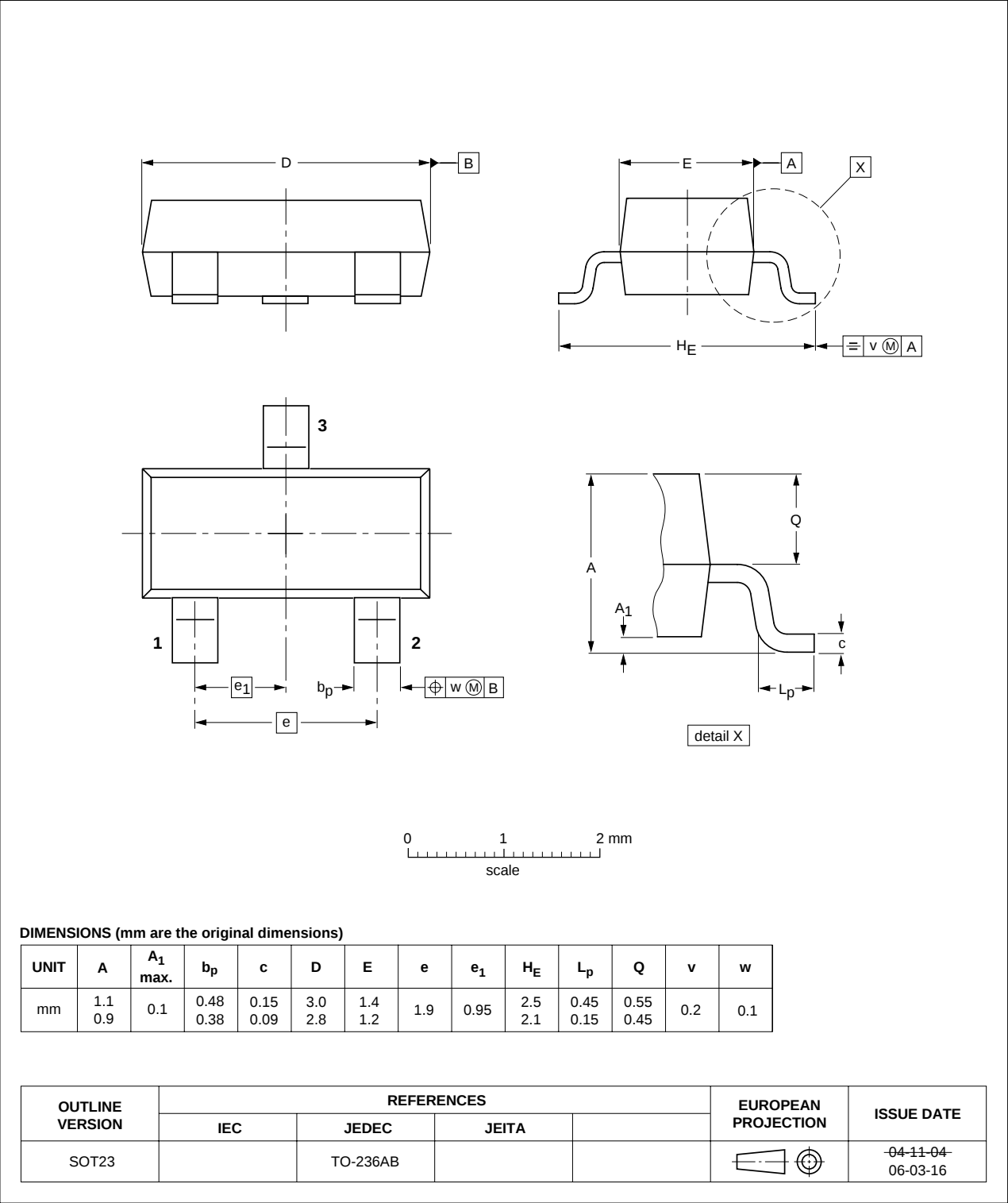


Fig 15. Package outline SOT23

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
2N7002E_3	20060428	Product data sheet	-	-	2N7002E_2
Modifications:	• Table 5 “Characteristics”: $V_{GS(th)}$ I_D condition modified • Table 5 “Characteristics”: $V_{GS(th)}$ maximum limits modified • Table 5 “Characteristics”: $R_{DS(on)}$ typical values modified • Table 5 “Characteristics”: g_{fs} removed • Table 5 “Characteristics”: Addition of $Q_{G(tot)}$, Q_{GS} and Q_{GD} • Table 5 “Characteristics”: C_{iss}, C_{oss} and C_{rss} values modified • Table 5 “Characteristics”: t_{on} and t_{off} typical values modified • Figure 3, 4, 5, 6, 7, 9, 10, 13 and 14: modified • Figure 11: added				
2N7002E_2	20050426	Product data sheet	-	9397 750 14944	2N7002E-01
2N7002E-01	20020211	Product data	-	9397 750 09095	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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14. Contents

1	Product profile	1
1.1	General description.....	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data.....	1
2	Pinning information.....	1
3	Ordering information.....	2
4	Limiting values.....	2
5	Thermal characteristics.....	4
6	Characteristics.....	5
7	Package outline	9
8	Revision history.....	10
9	Data sheet status	11
10	Definitions	11
11	Disclaimers.....	11
12	Trademarks.....	11
13	Contact information	11



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