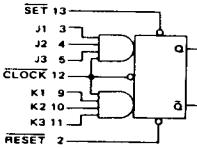
# MC5472L*
# MC7472P,L*




| $t_n$ | | $t_{n+1}$ |
|---|---|---|
| J | K | Q |
| 0 | 0 | $Q_n$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\bar{Q}_n$ |

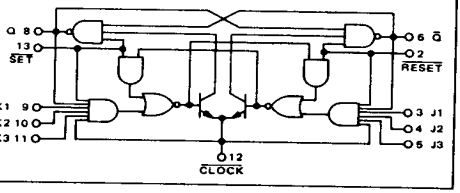
J = J1 · J2 · J3
K = K1 · K2 · K3

Input Loading Factor:
J, K = 1
CLOCK, SET, RESET = 2
Output Loading Factor = 10

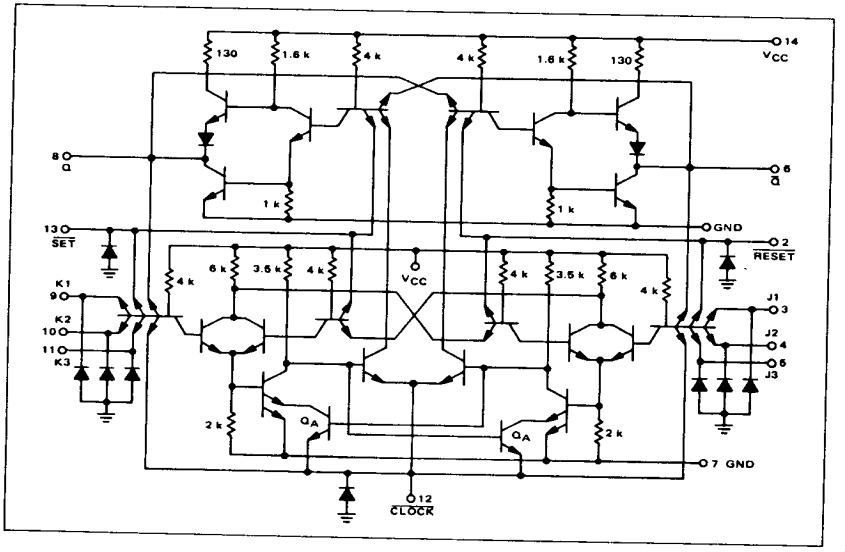
Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 15 MHz typ

This negative-edge-clocked J-K flip-flop operates on the master-slave principle. Three K inputs are ANDed together, and three J inputs are ANDed together. SET and RESET inputs are also available. The device helps minimize package count in J-K flip-flop applications requiring AND gating into the J or K inputs.

LOGIC DIAGRAM

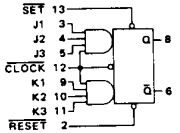



*L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, plus the $\overline{SET}$, $\overline{RESET}$, and $\overline{CLOCK}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.




| | TEST CURRENT/VOLTAGE VALUES (All Temperatures) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | mA | | Volts | | | | | | | | |
| | $I_{OL}$ | $I_{OH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IHH}$ | $V_R$ | $V_{th1}$ | $V_{th0}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ |
| MC5472 | 16 | -0.4 | 0.4 | 2.4 | 5.5 | 4.5 | 2.0 | 0.8 | 5.0 | 4.5 | 5.5 |
| MC7472 | 16 | -0.4 | 0.4 | 2.4 | 5.5 | 4.5 | 2.0 | 0.8 | 5.0 | 4.75 | 5.25 |

| Characteristic | | Symbol | Pin Under Test | MC5472 Test Limits −55 to +125°C Min | Max | Unit | MC7472 Test Limits 0 to +70°C Min | Max | Unit | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL}$ | $I_{OH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IHH}$ | $V_R$ | $V_{th1}$ | $V_{th0}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input** | | | | | | | | | | | | | | | | | | | | | |
| Forward Current | J | $I_F$ | 3 | - | -1.6 | mAdc | - | -1.6 | mAdc | - | - | 3 | - | - | 2*,4,5,12 | - | - | - | - | 14 | 7 |
| | K | | 9 | - | -1.6 | | - | -1.6 | | - | - | 9 | - | - | 10,11,12,13* | - | - | - | - | | |
| | $\overline{Set}$ | | 13 | - | -3.2 | | - | -3.2 | | - | - | 13 | - | - | 3,4,5,9,10,11,12 | - | - | - | - | | |
| | $\overline{Reset}$ | | 2 | - | ↓ | | - | ↓ | | - | - | 2 | - | - | 3,4,5,9,10,11,12 | - | - | - | - | | |
| | Clock | | 12 | - | | | - | | | - | - | 12 | - | - | 2*,3,4,5,9,10,11 | - | - | - | - | | |
| | | | 12 | - | | | - | | | - | - | 12 | - | - | 3,4,5,9,10,11,13* | - | - | - | - | | |
| Leakage Current | J | $I_{R1}$ | 3 | - | 40 | μAdc | - | 40 | μAdc | - | - | - | 3 | - | - | - | - | - | - | 14 | 2,4,5,7,12 |
| | K | | 9 | - | 40 | | - | 40 | | - | - | - | 9 | - | - | - | - | - | - | | 7,10,11,12,13 |
| | $\overline{Set}$ | | 13 | - | 80 | | - | 80 | | - | - | - | 13 | - | - | - | - | - | - | | 3,4,5,7,12 |
| | $\overline{Reset}$ | | 2 | - | ↓ | | - | ↓ | | - | - | - | 2 | - | - | - | - | - | - | | 7,9,10,11,12 |
| | Clock | | 12** | - | | | - | | | - | - | - | 12 | - | - | - | - | - | - | ↓ | 2,3,4,5,7,9,10,11,12 |
| | J | $I_{R2}$ | 3 | - | 1.0 | mAdc | - | 1.0 | mAdc | - | - | - | - | 3 | - | - | - | - | - | 14 | 2,4,5,7,12 |
| | K | | 9 | - | | | - | | | - | - | - | - | 9 | - | - | - | - | - | | 7,10,11,12,13 |
| | $\overline{Set}$ | | 13 | - | | | - | | | - | - | - | - | 13 | - | - | - | - | - | | 3,4,5,7,12 |
| | $\overline{Reset}$ | | 2 | - | | | - | | | - | - | - | - | 2 | - | - | - | - | - | | 7,9,10,11,12 |
| | Clock | | 12 | - | ↓ | | - | ↓ | | - | - | - | - | 12 | - | - | - | - | - | ↓ | 2,3,4,5,7,9,10,11,12 |
| **Output** | | | | | | | | | | | | | | | | | | | | | |
| Output Voltage | | $V_{OL}$ | 6 | - | 0.4 | Vdc | - | 0.4 | Vdc | 6 | - | - | - | - | - | 2 | 13 | - | 14 | - | 7 |
| | | | 8 | - | 0.4 | Vdc | - | 0.4 | Vdc | 8 | - | - | - | - | - | 13 | 2 | - | 14 | - | 7 |
| | | $V_{OH}$ | 6 | 2.4 | - | Vdc | 2.4 | - | Vdc | - | 6 | - | - | - | - | 13 | 2 | - | 14 | - | 7 |
| | | | 8 | 2.4 | - | Vdc | 2.4 | - | Vdc | - | 8 | - | - | - | - | 2 | 13 | - | 14 | - | 7 |
| Short-Circuit Current | | $I_{SC}$ | 6 | -20 | -57 | mAdc | -18 | -57 | mAdc | - | - | - | - | - | 3,4,5,9,10,11 | - | - | - | - | 14 | 2,6,7,12 |
| | | | 8 | -20 | -57 | mAdc | -18 | -57 | mAdc | - | - | - | - | - | 3,4,5,9,10,11 | - | - | - | - | 14 | 7,8,12,13 |
| **Power Requirements** | | | | | | | | | | | | | | | | | | | | | |
| Power Supply Drain | | $I_{PD}$ | 14 | - | 12 | mAdc | - | 12 | mAdc | - | - | - | - | - | - | - | - | 14 | - | - | 2,7 |
| | | | 14 | - | 12 | mAdc | - | 12 | mAdc | - | - | - | - | - | - | - | - | 14 | - | - | 7,13 |

*Momentarily ground pin prior to taking measurement.
**Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

## OPERATING CHARACTERISTICS

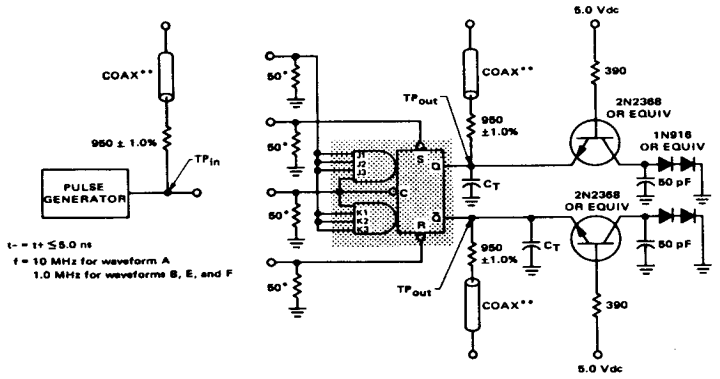
Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{RESET}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{RESET}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors $Q_A$ have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of −2.0 V appear at the clock.

### SWITCHING TIME TEST CIRCUIT




t− = t+ ≤5.0 ns
f = 10 MHz for waveform A
1.0 MHz for waveforms B, E, and F

Two pulse generators are required and must be slaved together for testing $\overline{\text{SET}}$ and $\overline{\text{RESET}}$. Only one pulse generator is required for J, K, and $\overline{\text{CLOCK}}$ tests.

*Resistor used only when that input is under test.

**The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T$ = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

## MC5472L, MC7472P, L (continued)

**OPERATING CHARACTERISTICS** (continued)

**TEST PROCEDURES**

(Letters shown in test columns refer to waveforms.)

| TEST | SYMBOL | INPUT | | | | Q | $\bar{Q}$ | LIMITS | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $\bar{C}$ | J, K | $\bar{R}$ | $\bar{S}$ | | | Min | Max | Unit |
| Toggle Frequency | $f_{Tog}$ | A | A | 2.4 V | 2.4 V | † | † | 10 | – | MHz |
| Turn-On Delay | $t_{pd-}$ | B | B | 2.4 V | 2.4 V | C | C | – | 50 | ns |
| Turn-Off Delay | $t_{pd+}$ | B | B | 2.4 V | 2.4 V | D | D | – | 50 | ns |
| Turn-On Delay | $t_{sd-}$ | 2.4 V | 2.4 V | E | F | G | H | 10 | 50 | ns |
| Turn-Off Delay | $t_{sd+}$ | 2.4 V | 2.4 V | E | F | G | H | 10 | 50 | ns |
| Enable Voltage | $V_{EN}$ | B | 2.0 V | 2.4 V | 2.4 V | † | † | † | – | – |
| Inhibit Voltage | $V_{INH}$ | B | 0.8 V | 2.4 V | 2.4 V | ‡ | ‡ | ‡ | – | – |

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

**VOLTAGE WAVEFORMS AND DEFINITIONS**