PLC810PG
HiperPLC™ Family

Continuous Mode PFC & LLC Controller with Integrated Half-bridge Drivers

Product Highlights

Features

- Highly integrated, eliminates external components
- Frequency and phase synchronized PFC and LLC
  - Reduced noise and EMI
  - Ripple current reduction in PFC output capacitor
  - Edge collision-avoidance simplifies layout
- Comprehensive PFC and LLC fault handling and current limiting
- Proprietary continuous conduction mode PFC for high efficiency with low component cost
- High efficiency Zero Voltage Switching (ZVS) LLC
- Off-time PFC control eliminates AC input sensing components
- Configurable, precise dead time control and frequency limit
  - Prevents hard MOSFET switching
- Tight LLC duty cycle symmetry for balanced O/P diode currents
- Lead and halogen free Green package

Applications

- 32” to 60” LCD TV power supplies
- Off-line 150 W to 600 W efficiency-optimized power supplies
- LED street lighting

Description

The PLC810PG is a combined PFC and LLC off-line controller with integrated high voltage half-bridge drivers. Figure 1 shows a simplified schematic of a PLC810PG based power supply where the LLC resonant inductor is integrated into the transformer. The PFC section of the PLC810PG is a universal input continuous current mode (CCM) design that does not require a sinusoidal input reference, thereby reducing system cost and external components.

The DC-DC controller drives an LLC resonant topology. This variable frequency controller provides high efficiency by switching the power MOSFETs at zero voltage, eliminating most switching losses. The LLC controller is built around a current controlled oscillator with a control range selected to support the traditional frequency of operation found in televisions.

To ensure zero voltage switching, the dead time of the LLC switching in the PLC810PG is tightly toleranced and can be adjusted with an external resistor. The highside/lowside duty cycle is also closely matched to provide balanced output currents reducing output diode cost.

A typical PLC810PG LLC design operates at 100 kHz (under nominal conditions). Depending on the LLC circuit design, the switching frequency can vary from half to three times the nominal operating frequency as a result of line and load changes.

The PFC converter is frequency locked to the LLC to minimize noise and electromagnetic interference. Increasing the PFC frequency in synchronization with the LLC at light loads reduces the current at which the PFC boost converter

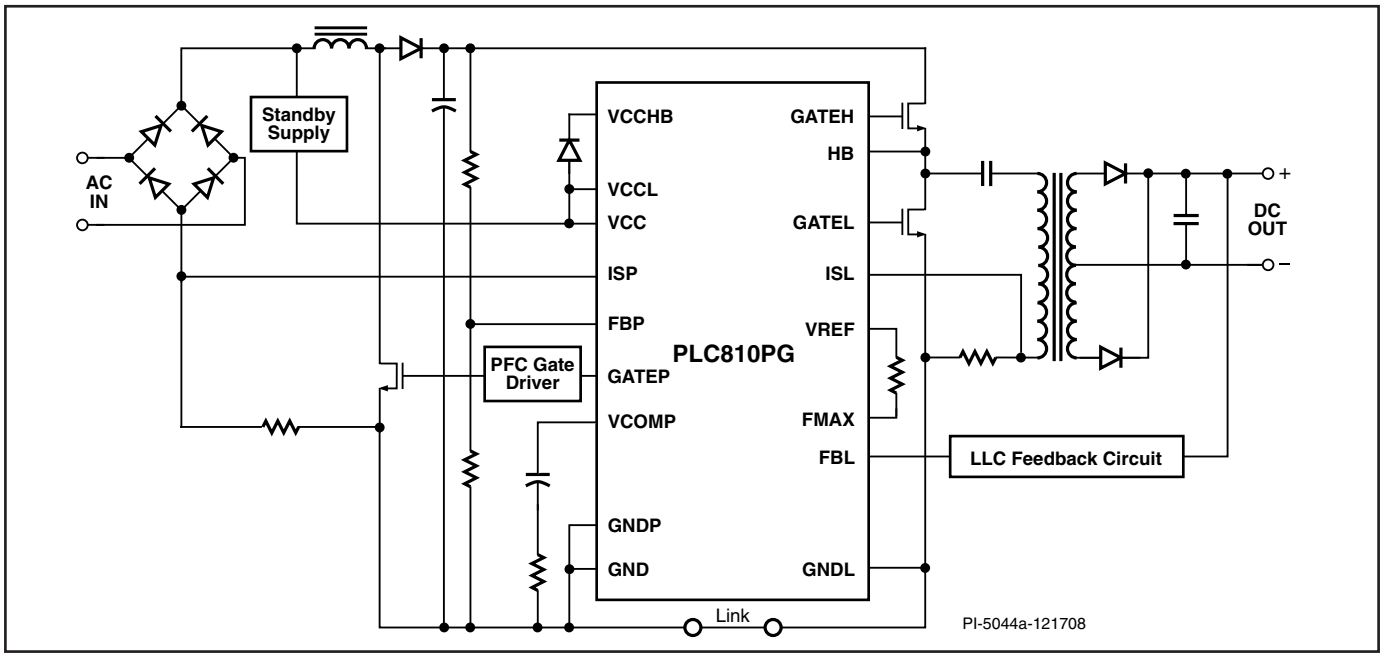


Figure 1. Typical Application Circuit – LCD TV Power Supply.

becomes discontinuous improving light load operation and reducing power line harmonics. PFC and LLC primary side fault management is provided.

The phase of the PFC PWM output is dynamically adjusted relative to the LLC phase such that the switching edges do not coincide with noise sensitive events in the PWM and LLC timing circuits. This edge-collision avoidance technology simplifies power supply layout and improves performance. Phase synchronization reduces EMI spectral components and reduces ripple current in the PFC capacitor.

Pin Description

VCC Pins

VCC
VCC powers the small signal analog circuitry inside the IC. A bypass capacitor must be connected from the VCC pin to the GND pin. This capacitor needs to be a 10 µF ceramic capacitor, or a parallel combination of a 10 µF electrolytic capacitor and a 0.1 µF ceramic capacitor.

VCCL
VCCL is the supply pin for the LLC low side driver. It powers only the LLC low side MOSFET driver and the communications circuitry between the analog circuitry and the LLC drivers. A 1 µF ceramic bypass capacitor must be connected from the VCCL pin to the GNDL pin. This capacitor provides the instantaneous current for turning on the gate of the LLC low-side MOSFET.

VCCHB
VCCHB is the floating supply pin for the LLC high-side driver, which is referenced to the HB pin. The HB pin is in turn connected to the LLC MOSFET half-bridge center point. A 1 µF ceramic bypass capacitor must be connected from the VCCHB pin to the HB pin. This capacitor provides the instantaneous current for turning on the gate of the high side LLC MOSFET.

In a typical application, VCC is connected to the standby supply. VCCL should be connected to the VCC pin through a 5 Ω resistor for noise immunity. VCCHB is connected to the standby supply through a series combination of a high voltage diode and a 5 Ω resistor. This diode plus resistor combination charges the 1 µF decoupling capacitor whenever the LLC low-side MOSFET is on. The resistor limits the peak instantaneous charging current. See R42 and D8 in Figure 4.

GND Pins

GND
GND is the return node for all analog small signals. All small signal pin bypass capacitors must be connected to this pin via short traces. This pin must have a single point connection, via a dedicated trace to the PFC current sense resistor, which in turn must be placed close to the PFC MOSFET. It must not be connected to any other point in the PFC/LLC power train. The VCC bypass capacitor must also be connected to this pin.

GNDP
GNDP is the return for the PFC gate drive signal **only**. This pin must be connected on the PCB directly to the GND pin.

GNDL
GNDL is the return for the LLC low side gate driver only. This pin must be connected to the LLC low side MOSFET Source pin, with a dedicated trace, and a small ferrite bead. This pin must be connected to the GND pin via a 1 Ω resistor for noise immunity. The VCCL bypass capacitor must also be returned to this pin.

Other Pins

HB
Half-bridge pin. This pin is the return of the LLC high side MOSFET driver. It must be connected to the center of the half-bridge formed by the LLC MOSFETs. The VCCHB bypass capacitor must also be returned to this pin.

ISP
Current sense, PFC. It is for sensing the negative voltage on the current sense resistor (which describes PFC inductor current). This sense resistor is connected between PFC MOSFET Source and Bridge '-' terminal. The signal must pass through an RC low-pass filter with a time constant between 100 and 200 ns. The resistor must be no greater than 150 Ω due to internal offset current requirements for the ISP pin. The average inductor current (measured over several switching cycles) is used for the PFC control algorithm. This pin also Implements pulse-by-pulse current limiting.

ISL
Current sense, LLC. This pin is for sensing transformer primary current, to detect LLC overload. It should be connected to the current sense resistor, which is connected between the LLC low side MOSFET Source pin and the bottom side of the transformer primary. The signal must pass through an RC low-pass filter with a time constant between 200 ns and 1 µs. The capacitor in the low-pass filter must be connected to the GND pin. The current limit has 2 levels, a lower, slow current limit for output overload, and a higher, fast current limit for component failure protection. The series resistor in the low-pass filter should be 1 kΩ or greater to limit current into the ISL pin.

GATEP
Gate drive output signal for the PFC MOSFET gate drive circuit.

GATEL
Gate drive for the low side LLC MOSFET.

GATEH
Gate drive for the high side LLC MOSFET.

VREF
3.3 V reference pin for the LLC feedback circuitry. A 1 µF ceramic decoupling capacitor must be connected from the V_{REF} pin to the GND pin.

FBP
The Feedback PFC pin is connected to the external resistor divider that senses PFC output voltage. This is a non-inverting input to a transconductance amplifier. The transconductance amplifier output is connected to the VCOMP pin, to which the feedback compensation is also connected. A 10 nF decoupling capacitor must be connected from the FBP pin to the GND pin.

VCOMP
This pin is the connection point for PFC feedback loop components. The voltage on this pin is used as an input to the PFC controller multiplier. The linear voltage range for this pin is nominally 0.5 V to 2.5 V, where higher voltage signifies less power.

FBL
LLC Feedback pin. Current entering this pin determines LLC switching frequency. It has a Thevenin equivalent circuit of nominally 0.65 V and 3.3 kΩ. FBL must be decoupled to the GND pin with a 1 nF capacitor. Note that this capacitor forms a pole with the input resistance.

FMAX
This pin is for programming maximum LLC frequency with a resistor to VREF. If the frequency commanded by the FBL pin current exceeds 95% of the programmed maximum frequency, the LLC high and low side drivers turn both LLC MOSFETs off. This pin must be decoupled to the GND pin with a 1 nF capacitor.

RSVD1, RSVD2, and RSVD3
RSVD1 must be connected to VREF. RSVD2 and RSVD3 must be connected to the GND pin.

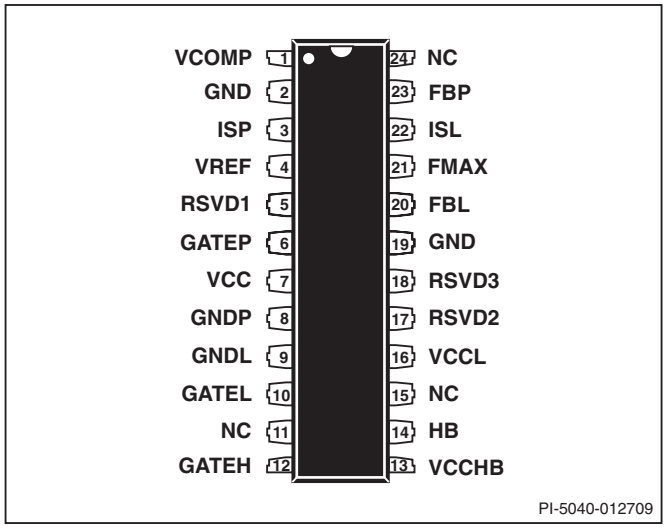


Figure 2. Pin Numbering and Designation (Top View).

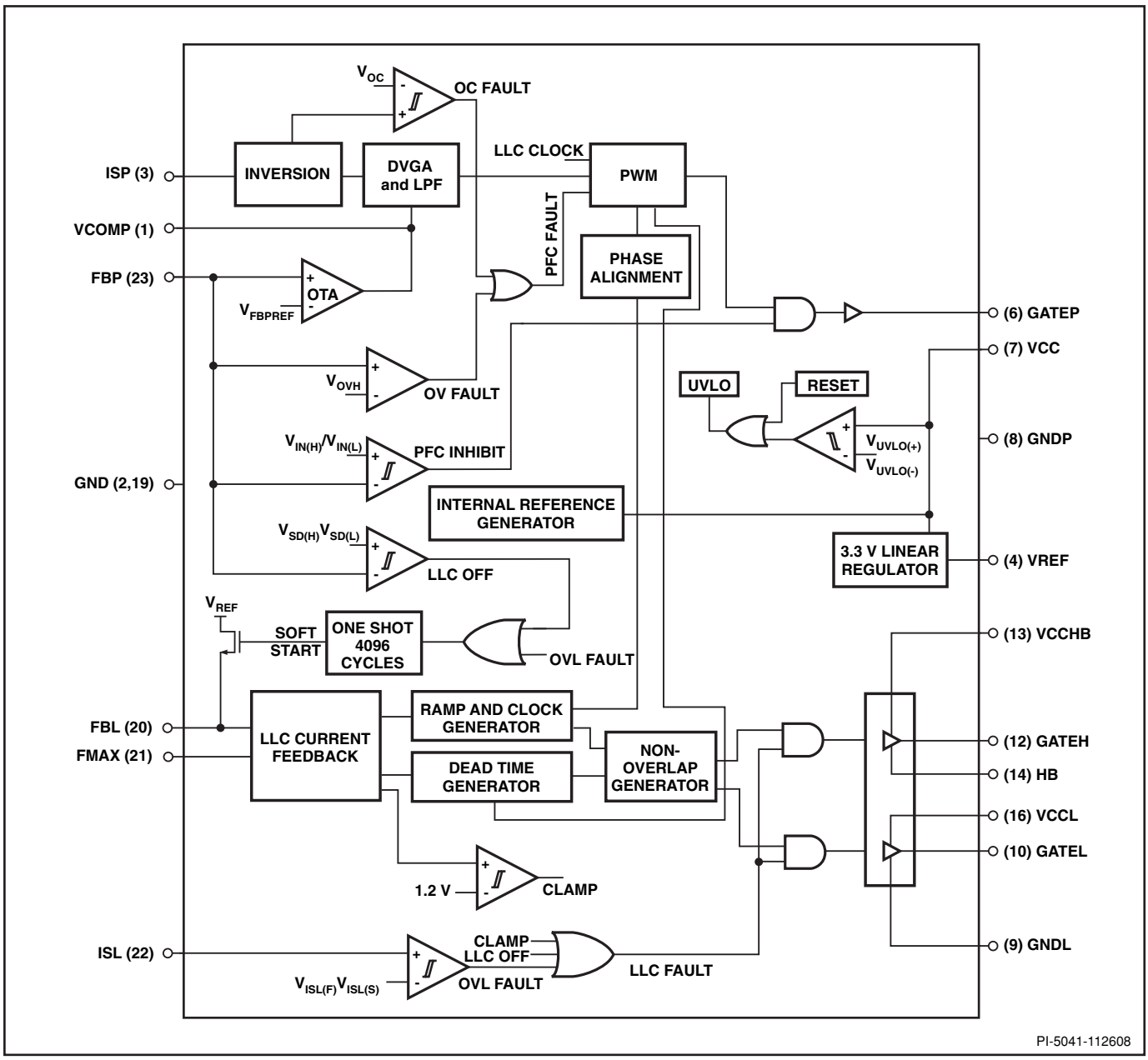


Figure 3. Block Diagram of PLC810PG. Reserved Pins are not Shown.

Block Diagram

Figure 3 shows a block diagram of the functional elements that make up the PLC810PG. The reserved pins are not shown in the diagram. Those pins are reserved for PI use during manufacture and testing. The PLC810PG PFC control blocks and circuits are shown on the upper half of the block diagram, while the LLC control blocks are shown on the lower half. Some of the functional blocks are shared.

PLC810PG Power Block

The PLC810PG is powered through VCC and VCCL pins. The VCCL pin powers the LLC driver while VCC powers the rest of the device. VCC pin must be supplied by a voltage between $V_{UVLO(+)}$ and 15 V. The provided supply is continuously compared against the $V_{UVLO(+)}$ and $V_{UVLO(-)}$ thresholds to start/stop the PLC810PG. When VCC is above the $V_{UVLO(+)}$ threshold the PLC810PG de-asserts the undervoltage lockout (UVLO) signal allowing the device to start. If VCC falls below $V_{UVLO(-)}$, the UVLO signal is asserted, shutting down the PLC810PG.

The VCCL pin powers the LLC driver, and VCCHB provides the charge for the LLC high-side MOSFET for gate drive.

An internal linear regulator is used to generate a 3.3 V rail to power the low voltage circuits inside the PLC810PG. The 3.3 V is brought outside on the VREF pin allowing external low voltage circuits to be powered by the PLC810PG.

PLC810PG PFC Control Block

The PLC810PG PFC is a boost converter which conditions the average input current to make it (typically) sinusoidal and in phase with the input voltage. In normal operation the PFC operates in continuous conduction mode (CCM). Under light load, depending on the PFC inductor value, the converter may enter a discontinuous conduction mode (DCM). The PLC810PG PFC controller does not need to sense the input voltage. The PLC810PG PFC controller exploits the fact that the input voltage (V_{IN}) is effectively constant over a few adjacent switching cycles, because the input is changing at 60 Hz while the switching frequency is 1500 times higher. Using the average input voltage and output voltage values, the off-time for the boost converter is:

$$D_{OFF} = (1 - D) = \frac{V_{IN}}{V_O}$$

The input current is the same as the inductor current (sensed current), thus from the previous equation, it can be deduced that:

$$\frac{V_{IN}}{I_{IN}} = D_{OFF} \times \frac{V_O}{I_{SENSE}}$$

In order to make the input impedance look resistive, the input current must be proportional to the input voltage:

$$\frac{V_{IN}}{I_N} = R_E$$

Thus, D_{off} has to be controlled by:

$$D_{OFF} = \left(\frac{R_E}{V_O}\right) \times I_{SENSE}$$

If (D_{OFF}) changes slowly with the input voltage, the average current will be in-phase with the input voltage. The PLC810PG PFC block controls the PFC off-time (D_{OFF} = (1–D)).

The output voltage needs to be regulated and R_E needs to be adjusted as a function of the load and the input voltage.

The PLC810PG PFC has two inputs:

- The feed-back PFC output voltage is reduced by a resistor divider and sensed and via the FBP pin.
- The instantaneous inductor current, sensed via the ISP pin.

The PFC output voltage is sensed at the FBP pin through an external resistive divider so that the desired DC boost voltage (typically 385 V) is reduced to match the internally generated V_{FBPREF} (2.2 V) reference voltage. The FBP input pin and the V_{FBPREF} voltage are inputs to an operational transconductance amplifier (OTA). The output of the OTA drives the VCOMP pin, allowing external compensation of the low frequency voltage loop.

The purpose of the phase alignment block is to set the edges of the PFC MOSFET gate drive signal to avoid the LLC converter switching edges. This eliminates switching-noise coupling between LLC and PFC circuits.

The compensation components are connected between VCOMP and the analog ground pin (GND). The VCOMP pin is used to apply compensation to the low frequency voltage loop.

The voltage developed across the PFC current sense resistor and applied to the ISP pin is compared against an overcurrent threshold (which has built in hysteresis). This implements a pulse-by-pulse current limit to protect the PFC MOSFET against overcurrent.

The ISP pin voltage is also averaged (over several switching cycles), and used as an input to the PFC multiplier.

The Discrete Variable Gain Amplifier, DVGA/LPF block is responsible for averaging the ISP pin voltage (over several switching cycles) and implementing a multiplier as part of the PFC control loop, under control of the VCOMP signal.

Using the feedback voltage on FBP, PFC and LLC circuit protection is provided:

- **PFC overvoltage protection**: The feedback voltage on the FBP pin is compared against an overvoltage threshold ($V_{OV(H)}$). If the voltage at the FBP pin is greater than $V_{OV(H)}$, the PFC MOSFET gate signal is turned OFF immediately, and held off for at least one cycle. When FBP drops below $V_{OV(H)}$, PFC switching recommences.
- **Minimum boost voltage detection**: The feedback voltage on FBP is compared against a minimum boost voltage threshold ($V_{IN(H)}$/$V_{IN(L)}$). The PFC is inhibited if the FBP voltage is below $V_{IN(L)}$. The gate of the PFC MOSFET is driven via GATEP if the FBP voltage is above $V_{IN(H)}$). This is done to prevent PFC startup in brownout or during AC failure conditions.
- **Minimum boost voltage for LLC startup**: The feedback voltage on FBP is compared against an LLC shutdown voltage threshold ($V_{SD(H)}$/ $V_{SD(L)}$). This inhibits LLC startup until the PFC output voltage is close to regulation. The purpose of $V_{SD(L)}$ is to shutdown the LLC when the PFC output voltage is low (~64% of nominal), which may occur during AC dropout, shutdown, or overload conditions.
- **PFC open-loop protection**: The FBP pin includes a high-impedance (5 MΩ) pull-down resistor to protect against a floating FBP pin resulting in an open-loop condition.

PLC810 LLC Control Block

The PLC810PG LLC controller supports half-bridge topologies. The LLC circuit relies on two switches in a half-bridge topology driving a resonant tank (LLC) and power transformer. The LLC circuit has two resonant frequencies: the series resonant frequency and the parallel resonant frequency. Typically, an LLC converter is designed to operate at a switching frequency which is slightly higher than the series resonant frequency when at nominal input voltage. In this operating region, the MOSFET switching can be performed at zero voltage, reducing the switching losses. In the normal mode of operation, the LLC controller will vary its switching frequency around a narrow range of frequencies to regulate the output voltage.

Feedback and Maximum Frequency Limit

The PLC810PG LLC controller has nominal operating frequency of 100 kHz. For voltage regulation, with input voltage and load variations, the operating frequency will vary and may exceed 250 kHz. The maximum frequency set by the resistor on FMAX pin is typically chosen to be two to three times the nominal operating frequency. The appropriate maximum frequency is set

using a resistor connected between the VREF pin and the FMAX pin using the curve in Figure 15. The resistor on the FMAX pin also sets the LLC dead time interval (see Figure 14).

The FBL pin provides output voltage regulation. As such the current entering this pin modulates the switching frequency. More current forces a higher switching frequency. The FMAX pin sets an upper limit for the switching frequency to ensure zero voltage switching. Minimum switching frequency is determined by the adjusting minimum bias applied to the FBL pin.

If the external feedback circuit attempts to push the LLC controller to a frequency equal to or higher than the maximum frequency limit set by the resistor at FMAX pin, the LLC MOSFET gate driver outputs are turned off until the current into the FBL pin drops below the FMAX pin current. The gate outputs are turned off synchronously with the clock for whole cycles.

LLC Soft Start

The LLC controller implements a soft start to prevent excessive currents during startup, and to prevent overshoot on the output when the feedback loop comes into operation. The soft start time is determined by external components on the FBL pin. In the event of an LLC fault turning off the LLC circuit, the external circuit is allowed to discharge, initiating a new soft start. When the soft start signal is asserted, the FBL pin is pulled up to V_{REF} (3.3 V), keeping the current applied to the FBL pin to maximum. During the soft start cycle, the LLC outputs turn on and the switching frequency slowly decays from its maximum to the nominal operating point.

LLC Overcurrent Detection (ISL Pin)

Overcurrent in the LLC converter is detected via a sense resistor in series with the low side of the transformer's primary winding. When the overcurrent condition is detected, the LLC MOSFETS are turned OFF. The overcurrent detection has two thresholds; fast overcurrent threshold ($V_{ISL(F)}$) and slow overcurrent threshold ($V_{ISL(S)}$). The fast overcurrent threshold is triggered by abnormally high current. The LLC is shutdown immediately if the pulse on the ISL pin exceeds this threshold. The slow overcurrent threshold is lower than the fast overcurrent threshold. The slow overcurrent response is triggered and the LLC is shutdown if the ISL pin voltage exceeds this threshold for eight consecutive clock cycles.

Typically the ($V_{ISL(F)}$) threshold is used to detect catastrophic failures such as shorted components, while the slow $V_{ISL(S)}$ threshold is used to detect overload conditions. This overcurrent detection circuit prevents the LLC converter from operating in the capacitive region of the LLC, thus avoiding failure of the converter components from overheating.

Other LLC Control Blocks

The non-overlap (dead time) generator creates two non-overlapping signals with equal on-times to drive the LLC MOSFETS. The drive signal for the two LLC MOSFETS is symmetrical with a 50% duty cycle. The dead time block is used both by the PFC and LLC to control the dead time of the switching function. The dead time in the PLC810PG is configurable via the FMAX pin. The dead time allows zero voltage switching, reducing the body diode losses in the switching MOSFETs and minimizing the reverse recovery time of the body diodes.

Start-up

Once the VCC voltages reach the startup voltage ($V_{UVLO(+)}$), the PLC810PG starts switching the PFC MOSFET and the PFC output ramps to its nominal value. When the PFC boost voltage (sensed through FBP pin) raises the FBP pin voltage above the LLC start threshold ($V_{SD(H)}$), the LLC circuit is enabled and the LLC soft start begins.

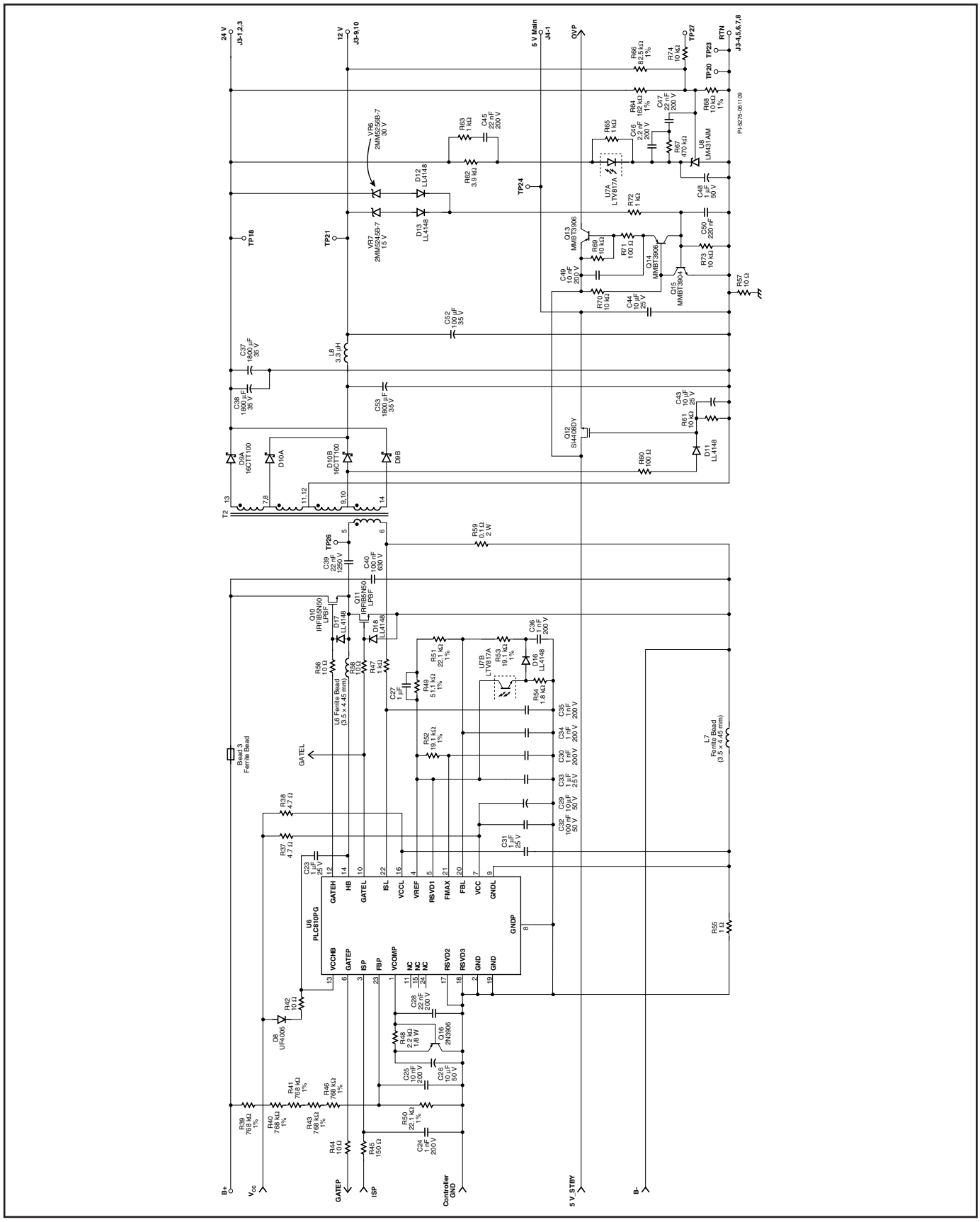


Figure 4. PLC810PG LCD TV Power Supply Application Circuit, PFC Circuit Control Inputs and LLC Stage.

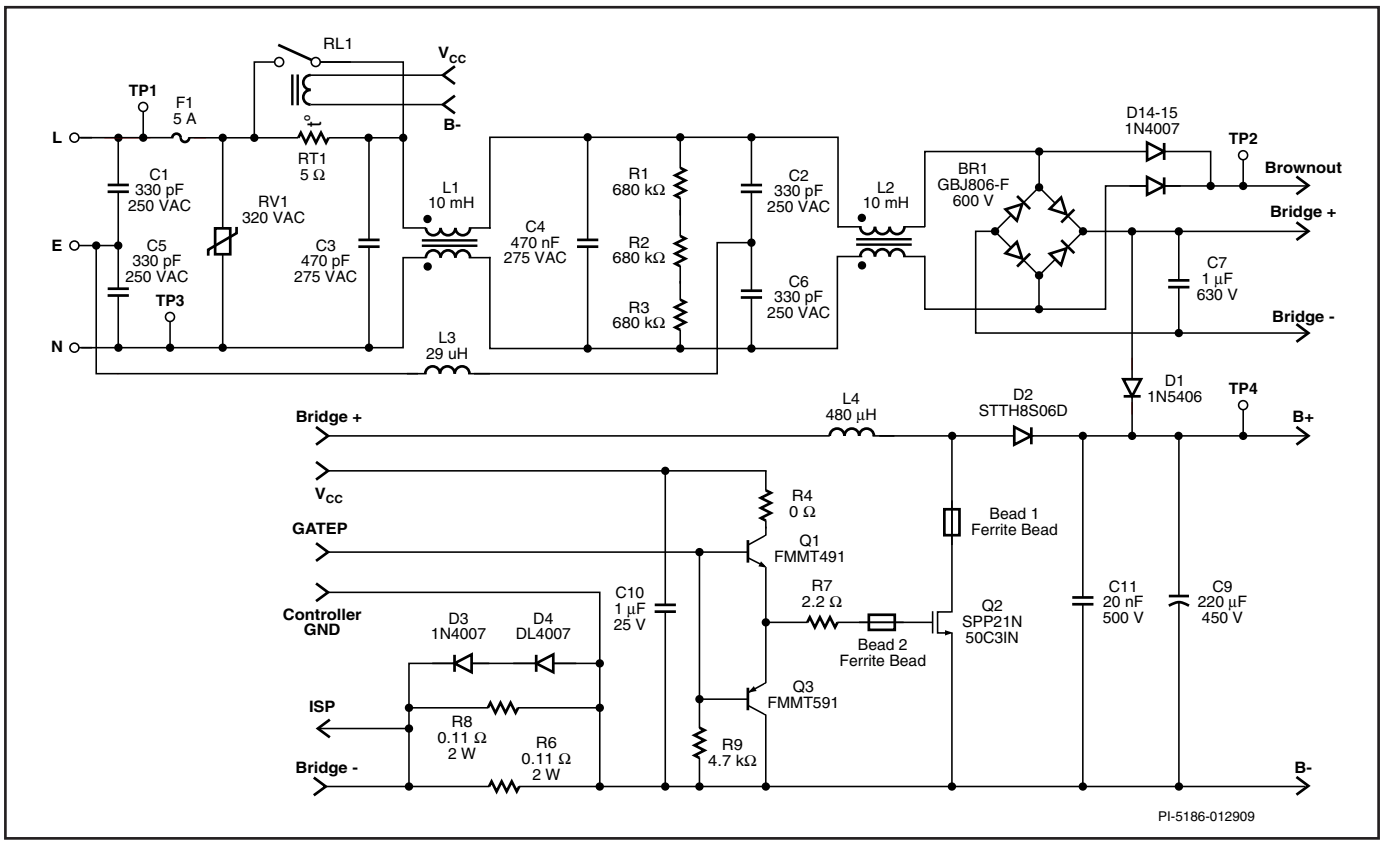


Figure 5. PLC810PG LCD TV Power Supply Application Circuit, Input Circuit and PFC Power Stage.

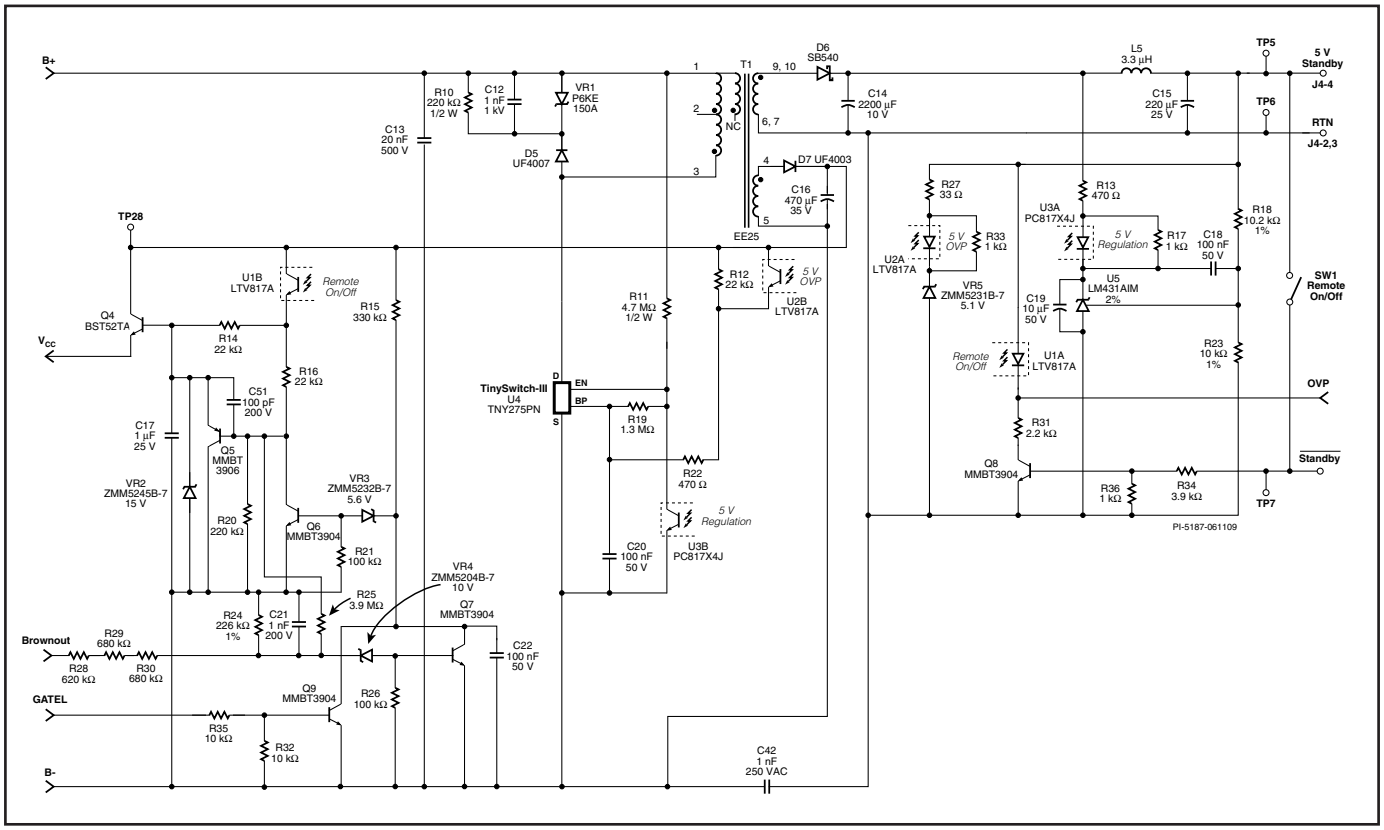


Figure 6. PLC810PG LCD TV Power Supply Application Circuit, Standby Supply.

Applications Example

Circuit Description

Figures 4, 5, and 6 show the schematic of a typical 280 W LCD TV power supply application using HiperPLC and TinySwitch-III. The PSU contains PFC + LLC stage using a PLC810PG which provides the high power outputs, plus a standby power supply using a TNY275PN.

The design has 4 outputs: 12 V and 24 V, 5 V main and 5 V standby. The 5 V main and 5 V standby are provided by the TinySwitch-III flyback circuit. See the Typical Application section of the TinySwitch-III data sheet found on the Power Integrations website for a description of a TinySwitch-III flyback converter.

The PSU has a standby input signal, which enables the main converter (PLC810PG).

EMI Filtering and Rectification
Capacitors C42, C1, C5, C3, C4, C2, C6 and common mode chokes L1 and L2 perform EMI filtering. Diode bridge BR1 rectifies the input AC with D14 and D15 providing a separate full-wave rectified signal for the brownout circuit.

Inrush Limiting
Thermistor RT1 provides inrush limiting. It is bypassed by a relay (RL1) which is driven by the power supply remote-on signal. The use of a relay increases efficiency by approximately 1%. Diode D3 provides an inrush path to the bulk capacitor C9 that bypasses the PFC inductor L4 to prevent it from saturating.

PFC Stage
The main PFC inductor L4, MOSFET Q2, boost diode D2, and bulk cap C9, form a PFC boost converter. Capacitor C8 and R5 damp reverse recovery ringing on D2. Inductor L4 uses a small low cost Sendust core. Two key advantages of this continuous mode PFC design are that the low ripple current allows the use of:

1. High B_{SAT} material (such as low-cost Sendust), allowing fewer turns which saves copper cost and reduces size.
2. Low-cost magnet wire rather than Litz wire.

Diode D2 is a low-cost silicon ultrafast PFC boost diode.

Components Q1, Q3, C10 and R7 form the gate drive circuit. See description under “Recommended PFC Gate Drive Circuit“.

PFC Current sense resistors R6 and R8 are clamped by D3 and D4 to protect the current sense input of the controller IC during inrush. Capacitor C11 is positioned close to the PFC MOSFET and diode to limit the size of the high frequency loop around components Q2, D2 and C9. This reduces EMI. Low-loss film capacitor C7 functions as the input capacitance to the PFC boost converter, and also filters EMI.

LLC Stage

LLC Input Stage
MOSFETs Q10 and Q11 form the LLC half-bridge. They are driven directly by the PLC810 via gate resistors R56 and R58. Capacitor C39 is the primary resonating capacitor, and should be a low-loss type rated to tolerate the highest RMS current seen at maximum load. Transformer T2 has a large built-in leakage inductance which acts with C39 to form the series resonant tank. Capacitor C40 is used for local bypassing, and is located directly adjacent to Q10 and Q11. Resistor R59 provides primary current sensing to the controller for overload protection.

LLC Outputs
The secondary ouputs of transformer T2 are rectified and filtered by D9, D10, C38, C39 and C53 to provide the +12 and +24 V outputs.

Switched +5 V Main Output
MOSFET Q12 is used to switch the output of the +5 V logic supply. The AC signal from one side of the 12 V output rectifier is used to drive Q12 via R60, R61, D11, and C43. Capacitor C44 provides filtering near the output connection.

Bias Regulator / Remote On/Off and Brownout Shutdown Circuit
Components Q4, U1, C17, and associated components constitute the bias regulator and provide the remote on-off function. Darlington transistor Q4, R14, and VR2 form a simple emitter follower voltage regulator that is switched via optocoupler U1. Capacitor C17 limits the rate of rise of the bias voltage. Transistor Q5 and R20 quickly discharge C17 when optocoupler U1 is turned off.

On the secondary, optocoupler U1 is turned on via Q8 when the standby signal is high. This turns on the PFC LLC stages.

A brownout shutdown circuit is provided to actively shutdown the PSU when the output turns off due to a brownout condition.

This circuit operates by sensing the AC input voltage together with the presence of the GATEL signal from the LLC controller. During a brownout condition, the PFC output voltage will drop until the VFB pin voltage drops to INH, turning off the LLC stage. If at this point the AC voltage is below 82 VAC, the brownout circuit will turn off the PLC810 via the bias regulator, preventing the PFC from charging up the bulk capacitor again, restarting the LLC, and repeating the cycle (and creating output voltage glitches).

Resistor R24, R26, R28-30, C21, VR4, and Q7 are used to sense the AC input voltage. The voltage threshold of this circuit is set below the turn-on threshold of the standby/primary bias converter. Sufficient AC voltage turns on Q7, discharging capacitor C22, which is charged via R15. Components R32, R35, and Q9 sense the switching GATEL signal. Transistor Q9 discharges capacitor C22 when the switching signal is present.

When the AC input voltage is low, Q7 and Q9 turn off, allowing C22 to charge. Transistor Q6, R21, and VR3 sense the voltage on C22. When C22 has charged sufficiently, Q6 turns on, turning off the primary bias supply via Q5, shutting down the PLC810 and thus the PFC and LLC stages.

Controller

Figure 4 shows the circuitry around the U13 main controller IC, which provides control functions for the input PFC and output LLC stages.

PFC Control

The PFC boost stage output voltage is fed back to the FBP pin of the PLC810PG via resistors R39-41, R43, R46, and R50. A 10 nF capacitor (C25) filters noise. Capacitor C26, C28 and R48 provide frequency compensation for the PFC. The PFC current sense signal from resistors R6 and R8 is filtered by R45 and C24. The PFC drive signal is routed to the main switching MOSFET via resistor R44, which damps any ringing in the PFC drive signal caused by the trace length from the PLC810PG to the PFC gate drive circuitry.

Bypassing/Ground Isolation

See “GND Pins” and “VCC Pins” under the section “Pin Description”. Capacitors C29 and C32 provide decoupling for the VCC pin. Capacitor C31 provides decoupling for the VCCL pin. Resistor R37 is an optional resistor that provides additional filtering for the VCC pin. This will help reject any noise picked up by long VCC traces from the standby supply.

Capacitors C24, C25, C32, C29, C30, C31, C33, C34, C35 must be connected to the correct ground pins, and be connected with short traces to the PLC810PG. See section “Pin Description”.

Resistor R55 separates the GND and GNDL pins. Together with ferrite bead L7, it provides high frequency isolation between GND and GNDL pins. The GATEL output gate drive for the low-side LLC MOSFET Q11 returns to GNDL through ferrite bead L7. The GATEH output gate drive for the high-side LLC MOSFET Q10 returns to HB through ferrite bead L6. This bead is optional, but provides symmetry with L7.

LLC Control

Feedback from the LLC output sense/error amplifiers circuits is provided by optocoupler U7. Resistor R54 is the optocoupler load. Diode D16 allows the optocoupler to pull up on the LLC feedback pin (FBL) only. See “LLC Controller section” for the description of the functions performed by of R54, C36, R53, R51, R49, and C27. The LLC current sense signal from resistor R59 is filtered by R47 and C35. Capacitor C23, R42, and D8 provide the booststrap supply for the LLC high side MOSFET driver. See “GND Pins” and “VCC Pins” under the section “Pin Description”.

LLC Secondary Control Circuits

Figure 4 shows the secondary control schematic for the LLC stage.

Voltage Feedback

The LLC converter 12 V and 24 V outputs are sensed, weighted, and summed by resistors R64, R66, and R68. Resistor R62 is the main gain-setting resistor. Resistor R63 and C45 form a phase-lead compensator which extends the feedback loop’s crossover frequency and increases the phase margin. Resistor R67, C46 and C47, in conjunction with R68 set the low-frequency compensation. Capacitor C48 is a “soft finish” capacitor that reduces output overshoot at start up, by conducting during the output rise time. It does not affect the main feedback loop characteristics.

OVP

Zener diodes VR6-7 and D12, D13 sense any overvoltage condition in the 12 V or 24 V outputs. An overvoltage signal from either output is used to trigger a bipolar latch (Q14, Q15, R70, R73), which turns on transistor Q13. This transistor is used to deactivate the remote on-circuit which turns off the primary bias, and hence the PLC810PG.

Power Supply Block Functions and Key Design Details

PFC Control Section

The PFC controller uses continuous conduction mode, with an off-duty-cycle control algorithm. This approach removes the requirement for input AC voltage sensing. The off-time is proportional to the product of the average inductor current (averaged over several switching cycles), and the error amp output. This automatically shapes the average input current, to the same shape as the input AC voltage.

The PLC810PG PFC circuit is frequency and phase locked to the LLC circuit. PLC810PG employs collision avoidance technology, where the PFC edges straddle those of the LLC so that simultaneous edge transitions in both the PFC and LLC sections are prevented. This reduces interference between PFC and the LLC circuits.

The PFC section has 2 input pins: a current sense input (ISP pin), and a voltage feedback input (FBP pin). There are 2 output pins. A VCOMP pin for placing the feedback compensation components, and a MOSFET gate signal output designed to work with an external MOSFET driver.

Inductor current is sensed via the ISP pin which monitors the negative voltage developed across the PFC current sense resistor. This resistor is connected to the PFC MOSFET Source pin. The current is averaged over several switching cycles and is used for the PFC control algorithm. This pin also implements a cycle-by-cycle current limit to protect the PFC MOSFET in the event of a short-circuit. The RC filter with 100-200 ns time constant attenuates high frequency switching noise, but must be fast enough to detect a saturating PFC inductor in order to protect the PFC MOSFET.

PFC output voltage is sensed by the FBP pin via a resistor voltage divider network. The FBP pin is connected to the input

of an operational transconductance amplifier (OTA). The output of this OTA is connected to the VCOMP pin. The feedback loop operates to keep the voltage on the FBP pin (and therefore the PFC output voltage) to a fixed value, depending on the resistor divider ratio. When the PFC output voltage is higher than the set point, the transconductance amplifier will source current, raising the voltage on the VCOMP pin. When the PFC output voltage is lower than the set point, the transconductance amplifier will sink current, lowering the voltage on VCOMP pin. The gain of the stage is equal to the product of the OTA gain (G_M), and the impedance of the network connected to the VCOMP pin.

The PFC controller senses the voltage on the VCOMP pin. A higher voltage tends to reduce the PFC MOSFET's duty cycle, while a lower voltage tends to increase it.

The VCOMP pin has a linear operating range of 0.5 V to 2.5 V, and is scaled and multiplied by the average inductor current to set D_{OFF}, the off-duty-cycle of the PFC gate signal. During closed-loop steady state operation, the VCOMP voltage is a function of the line voltage and the PFC load. A low voltage on VCOMP signifies high power, while a high voltage corresponds to low power.

The VCOMP pin is internally connected to an input of a multiplier which is part of the PFC modulator. The linear range of this pin is 0.5 V to 2.5 V. 0.5 V signifies maximum power, and 2.5 V signifies minimum power.

The FBP pin has 3 start-up and shutdown voltage thresholds.

1. INH – Inhibits PFC start-up at low AC input voltage.
2. $V_{SD(H)}$ – inhibits LLC start-up after PFC start-up. LLC start-up is delayed until the PFC output voltage is close to its regulation set point.
3. $V_{SD(L)}$ – shuts down the LLC converter when the bulk cap has discharged to a low voltage – typically at the end of holdup time.

Before PFC start-up, the voltage on the bulk cap is approximately equal to the peak of the input voltage, and INH acts as an AC undervoltage lockout. After the PFC starts, the PFC output voltage no longer tracks the input voltage and there is no low AC voltage shutdown function.

For a typical design with a PFC voltage set point of 385 V, the PFC is inhibited when bulk voltage <100 V (typical), which is equivalent to VAC <71 V (typical). LLC start-up is inhibited until the PFC output voltage reaches 368 V (typical). For the same design, the LLC will shut down when the PFC output voltage drops below 246 V (typical).

LLC Controller Section

The LLC converter is a variable frequency converter (an LLC converter's output power decreases as frequency increases). The designer needs to set the minimum and maximum frequencies of the PLC810PG to suit the power train.

FMAX Pin

The FMAX pin is connected via a programming resistor to the VREF pin. This resistor programs the current into the FMAX pin. This pin has a nominal Thevenin equivalent circuit of 0.65 V and 1.5 kΩ. The programmed current into the FMAX pin controls two parameters:

1. The LLC drive (GATEL and GATEH) dead-time. The smaller the resistor value, the greater the current and the higher the maximum frequency, see Figure 15.
2. The maximum LLC operating frequency. When the FBL pin current increases above the FMAX pin current, the LLC MOSFETs will be shut down. Switching will restart when the FBL pin current drops below the FMAX pin current.

The dead-time should be longer than the actual voltage rise and fall times of the LLC half-bridge center-point (longest times at minimum load). If the programmed dead-time is shorter than the actual rise and fall times, the MOSFETs will no longer operate in the ZVS region, and losses will increase. Dead-times somewhat longer than this required minimum have very little impact on efficiency.

During long dead-times the body diodes of the LLC switching MOSFETs will conduct current just before turn-on; the additional conduction loss is very small compared to other losses. The FMAX pin programming resistor sets both dead-time and maximum frequency. Setting a longer dead-time than that required at no-load is the recommended approach if a lower maximum frequency is desired
.
If the required dead-time is very long, and the resulting F_{MAX} is lower than that required for light load regulation (for the worst case at maximum input voltage), then the solution is to limit F_{MAX} and allow the LLC to enter burst-mode under light load (maximum frequency) in order to keep the output in regulation. Maximum input voltage occurs during a 100-0% load step which causes the PFC output voltage to overshoot to VOV(H) triggering the PFC output overvoltage protection circuit (which is nominally 105% of the PFC nominal voltage set point). For a typical design, an LLC converter requires an F_{MAX} of 1.5x ~ 2x the nominal operating frequency (measured at full load and nominal input voltage).

If burst-mode regulation is required for light load operation, the FBL pin resistors must be chosen such that the maximum current driven by the feedback loop into the FBL pin is greater than the FMAX pin current (set by the FMAX pin resistor). When the FBL pin current is greater than the FMAX pin current, the LLC gate drivers turn off both MOSFETs. During line/load conditions that require higher frequency than F_{MAX} to maintain regulation, the LLC converter will go into hysteretic burst-mode to maintain regulation.

When burst mode is used, care must be taken to ensure that during startup, the peak primary currents do not trigger primary over current (ISL pin). This is because switching frequency cannot be higher than F_{MAX} (even during soft start) and the peak primary currents with a low soft start frequency will therefore be higher.

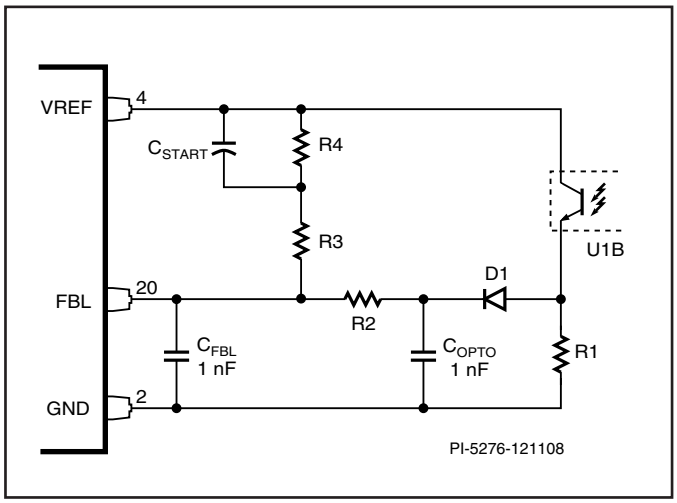


Figure 7. Typical LLC Feedback Network.

FBL pin

The FBL pin is the voltage regulation feedback pin. It sinks current in normal operation. The greater the input current, the higher the LLC switching frequency. The characteristic of frequency versus the size of shunt resistor (connected to VREF) is given in Figure 16. The FBL pin has a Thevenin equivalent circuit of nominally 0.65 V and 3.3 kΩ. It should be noted that the 1 nF decoupling Capacitor, C_{FBL} (see Figure 7), in conjunction with the 3.5 kΩ input resistance presented by the FBL pin, form a pole in the LLC transfer function. This needs to be considered as part of the LLC feedback loop. To insure loop stability the 1 nF capacitor should not be increased.

A typical feedback network uses a TL431 and an optocoupler for output regulation. The optocoupler regulates current provided to the FBL pin. A resistor network between the optocoupler and the FBL pin sets the minimum, maximum, and start-up currents into the FBL pin.

In Figure 7 optocoupler U1B is connected to the FBL pin through a resistor network comprised of resistors R1, R2, R3, R4, and the Capacitor C_{START}. C_{START} is active only during soft start and can be ignored during normal operation. Copto is a filter capacitor that reduces noise from the long optocoupler traces. The value (R3 + R4) sets the minimum FBL pin current and therefore minimum LLC frequency, F_{MIN} (when the optocoupler is turned off). This occurs at the end of holdup time, when the bulk capacitor has discharged down to 64% (nominal) of the regulation set point.

The maximum FBL pin current (and therefore the maximum LLC frequency that the feedback loop can command) is set by R2, R3, and R4. Maximum frequency occurs when the optocoupler is fully saturated, such as when the LLC output moves above the set point during an output load dump. It should be noted that if the maximum FBL pin current is greater than the FMAX pin current, the LLC gate drivers turn both MOSFETs off.

The start-up current (and therefore the starting frequency), is determined by the value of R3. Note that during start-up, C_{START} is a virtual short-circuit, the optocoupler is turned off and all FBL pin current comes from R3.

The procedure for selecting the resistor values is as follows.

Choose R1

This is the main load resistance in series with the optocoupler. A value of 1.8 kΩ will yield good frequency response with an acceptable maximum collector load current of approximately 2 mA. Note that the overall loop gain will be proportional to this resistor value.

Choose F_{START} (the initial frequency at start-up)

F_{START} is typically chosen to be equal to or just less than F_{MAX}. Determine the resistance value that corresponds to the desired F_{START} from Figure 16. Set R3 to this value. R3 will typically have a value close to that of the FMAX resistor.

The next step is to set F_{MIN}. F_{MIN} is the frequency that the LLC needs in order to regulate at full load, F_{MIN} is determined by the sum of (R3 + R4). Look up the resistance value R for the desired F_{MIN} in Figure 16. Set R4 according to the equation below.

$$R4 = R - R3$$

Calculate the Value of R2

$I_{FBL(MAX)}$ is the current that flows into the FBL pin when the optocoupler is saturated. This represents the maximum frequency that the feedback loop can command via the FBL pin. If this current is greater than the FMAX pin current (set by the FMAX pin resistor), the LLC converter may be forced into hysteretic burst-mode in order to regulate the output voltage at zero or light load. If burst-mode is not desired, $I_{FBL(max)}$ must be set less than the FMAX pin current. In this case, ensure that there is sufficient dead-time given by the FMAX pin resistor. If F_{MAX} is less than the frequency needed for regulation at light load, then burst mode operation will be required.

The relationship between I_{FBL} (FBL pin current) and frequency is given in Figure 17. The relationship between $I_{FBL(max)}$ and the resistor values is given below (1):

$$I_{FBL(MAX)} = \frac{V_{REF} - V_{FBL}(I_{FBL(MAX)})}{R3 + R4} + \frac{V_{REF} - V_{CESAT} - V_{FBL}(I_{FBL(MAX)}) - V_D}{R2} \quad (1)$$

V_{R2} (the voltage across R2) can be defined as:

$$V_{R2} = V_{REF} - V_{CESAT} - V_{FBL}(I_{FBL(MAX)}) - V_D \quad (2)$$

We can and then substitute this into (1) and rearrange:

$$R2 = V_{R2} \frac{R3 + R4}{I_{FBL(MAX)} R3 + I_{FBL(MAX)} R4 - V_{REF} + V_{FBL}(I_{FBL(MAX)})} \quad (3)$$

Where V_{FBL} is a function of I_{FBL}

$V_{CESAT} = V_{CE}$ of optocoupler in saturation (typical 0.3 V)

V_D = diode forward voltage drop

V_{REF} = 3.25 V (nominal)

LLC Soft Start

LLC Soft start is implemented by C_{START} (Figure 7). The LLC starts at high frequency and ramps down until output regulation is reached. Soft start is required as this allows the resonant tank to begin to oscillate. It also prevents large LLC primary currents during start-up that may trip the overcurrent threshold on the ISL pin.

When the PLC810PG starts up, the FBL pin is internally pulled up to VREF (3.25 V), and the LLC outputs are disabled. This ensures that the soft start capacitor C_{START} discharged. The FBL pin is then released falling to approximately 0.8 V; the PLC810PG begins sensing the current into the FBL pin and the LLC gate drive outputs begin switching. At start-up, the optocoupler will have no current flowing (because the LLC converter output is low) and the FBL pin current will be equal to $I_{FBLSTART}$. As C_{START} charges, the current into the FBL pin decreases, the LLC switching frequency decreases and the LLC converter output rises. When regulation is reached, the feedback loop closes and the optocoupler regulates the FBL current. During normal operation, C_{START} remains charged and does not have any current flow.

The start-up time constant is:

$$\tau_{START} = C_{START} \times \frac{R3 \times R4}{R3 + R4}$$

LLC Protection and Auto-Restart

The ISL pin senses LLC primary current via a sense resistor in series with the bottom side of the transformer primary. An RC low-pass filter is required, with recommended values of 1 kΩ and 1 nF respectively. The ISL pin has 2 thresholds. The higher threshold, $V_{ISL(F)}$, will immediately shut off and protect the LLC MOSFETs in the event of component failure. The lower threshold, $V_{ISL(S)}$, when exceeded for 8 consecutive cycles, also shuts down the LLC protecting against output overcurrent. Either fault mode will invoke an auto-restart sequence. When either of these fault conditions occur, the FBL pin is pulled-up internally to VREF, discharging the soft start capacitor. The controller counts for 4096 clock cycles, then initiates a new start-up (soft start) sequence. Typically 4096 cycles is sufficient to completely discharge the soft start capacitor ensuring that the LLC will re-start at frequency F_{START}.

Layout Considerations

PFC Powertrain Layout

PFC Layout

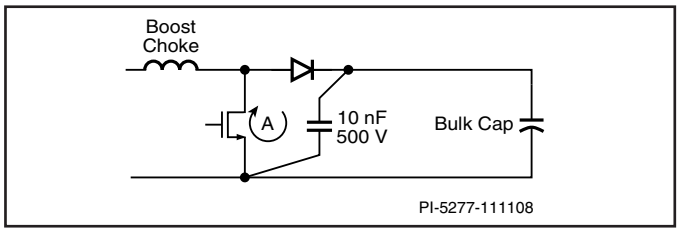


Figure 8. Power Elements in a Boost Converter Stage.

Figure 8 shows a typical PFC boost converter power stage using a single bulk capacitor (some designs may use 2 because of the ripple current requirement). With a single bulk capacitor, the bulk capacitor should be closer to the PFC MOSFET than the LLC MOSFETs. The PFC MOSFET, diode, and bulk capacitor should be mounted close to each other, with short leads connecting them. In addition, a 10 nF-47 nF high frequency bypass capacitor is recommended to reduce EMI. It should be connected close to the PFC MOSFET and diode, in order to minimize loop area (“A” in the diagram). This loop area sees the highest di/dt, and thus must be minimized. In some cases, an optional damping resistor in series with the 10 nF capacitor can reduce turn on Drain current ringing and consequent EMI. The recommended value for this resistor is between 0.2 Ω and 1 Ω.

LLC Powertrain Layout

Locating the Bulk Capacitor

If 2 parallel bulk capacitors are used to meet the ripple current requirement, place 1 near the PFC MOSFET, and the second near the LLC MOSFETs. If only one bulk capacitor is used, it is recommended that a high voltage decoupling capacitor, (10 nF-100 nF), is connected across the HVDC bus and primary return, connected with short traces to the LLC MOSFETs. (See C40 in schematic in Figure 4, and in PCB layout in Figure 9) The LLC converter MOSFETs see high di/dt, and this high voltage decoupling capacitor will reduce EMI.

High Voltage Pins

Three pins on the device have high voltage and high dv/dt because they track the LLC MOSFET half-bridge output. These are HB, VCCHB, and GATEH (pins 12, 13, and 14). These pins must be isolated from the rest of the pins on the PLC810PG (extra package isolation is also provided by omitting pins 11 and 15). Because these pins have high dv/dt, the traces and components connected to them have to be kept away from low voltage pins. Stray capacitance from these nodes to low voltage, (high impedance) pins will cause noise-coupling and erratic operation. Maintain 160 mil (4 mm) spacing between these pins, and surrounding low voltage nodes. See highlighted spacing in Figure 10.

Low Voltage Signal Pins

All pin decoupling capacitors must be mounted close to the IC and with short traces to the pins. All decoupling capacitors should be returned to the GND pin, with the exception of the decoupling capacitors for VCCL, and VCCHB.

Several pins require external RC low-pass filters. There are the ISP, ISL, FBP, and FBL pins. The capacitors and resistors should be mounted close to the IC. This will prevent capacitive coupling with high dv/dt nodes. The ISP pin is the input pin with the smallest signal and the widest bandwidth. It not only senses the average current in the PFC choke, it also senses peak current in order to perform peak-to-peak current limiting (to protect the PFC MOSFET). The current limiting function requires wide bandwidth.

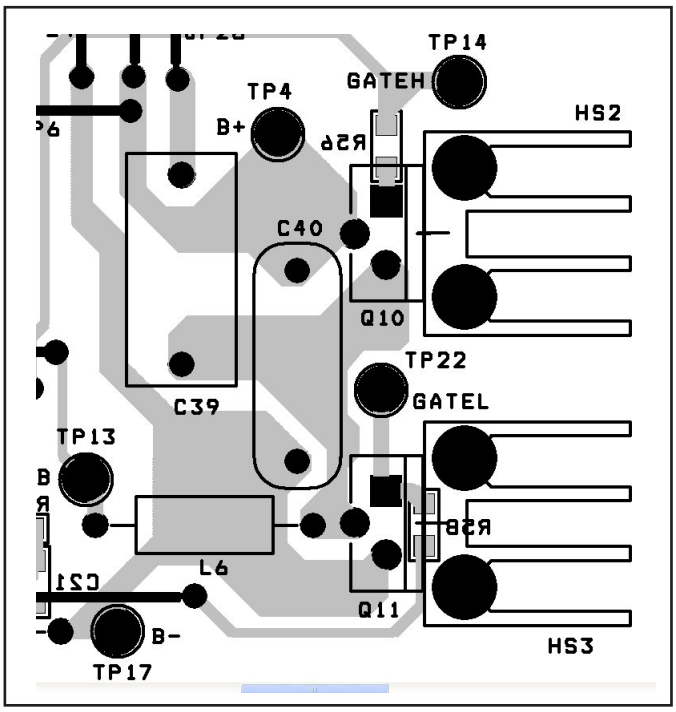


Figure 9. Location of LLC High Voltage Film Decoupling Capacitor, C40.

Use an RC low-pass filter with time constant between 100 ns and 200 ns, mounted near the device. The low-pass filter capacitor should be returned to the GND pin. Mount the PFC sense resistor close to the PFC MOSFET.

Run a dedicated trace from the GND pin to the junction of the PFC MOSFET Source and the PFC sense resistor. There should be no other connections on the trace from the GND pin to the PFC/LLC power components.

Run a dedicated trace from the resistor of the RC low-pass filter on the ISP pin to the PFC sense resistor. To avoid loop pick up from di/dt noise that may effect signal integrity, this trace must run alongside the trace from the GND pin to the PFC MOSFET source.

Layout the PFC driver circuitry near the PFC MOSFET. Run the trace connecting GATEP to the PFC driver circuitry adjacent to the ISP trace to the sense resistor. It is preferable to have the GND trace between the GATEP and ISP signal traces. This will reduce potential noise coupling from the GATEP trace to the ISP trace. See Figure 12.

FBL Pin Circuitry and Optocoupler

See Figure 13. The FBL pin circuitry should be mounted close to the PLC810PG. The feedback optocoupler is typically

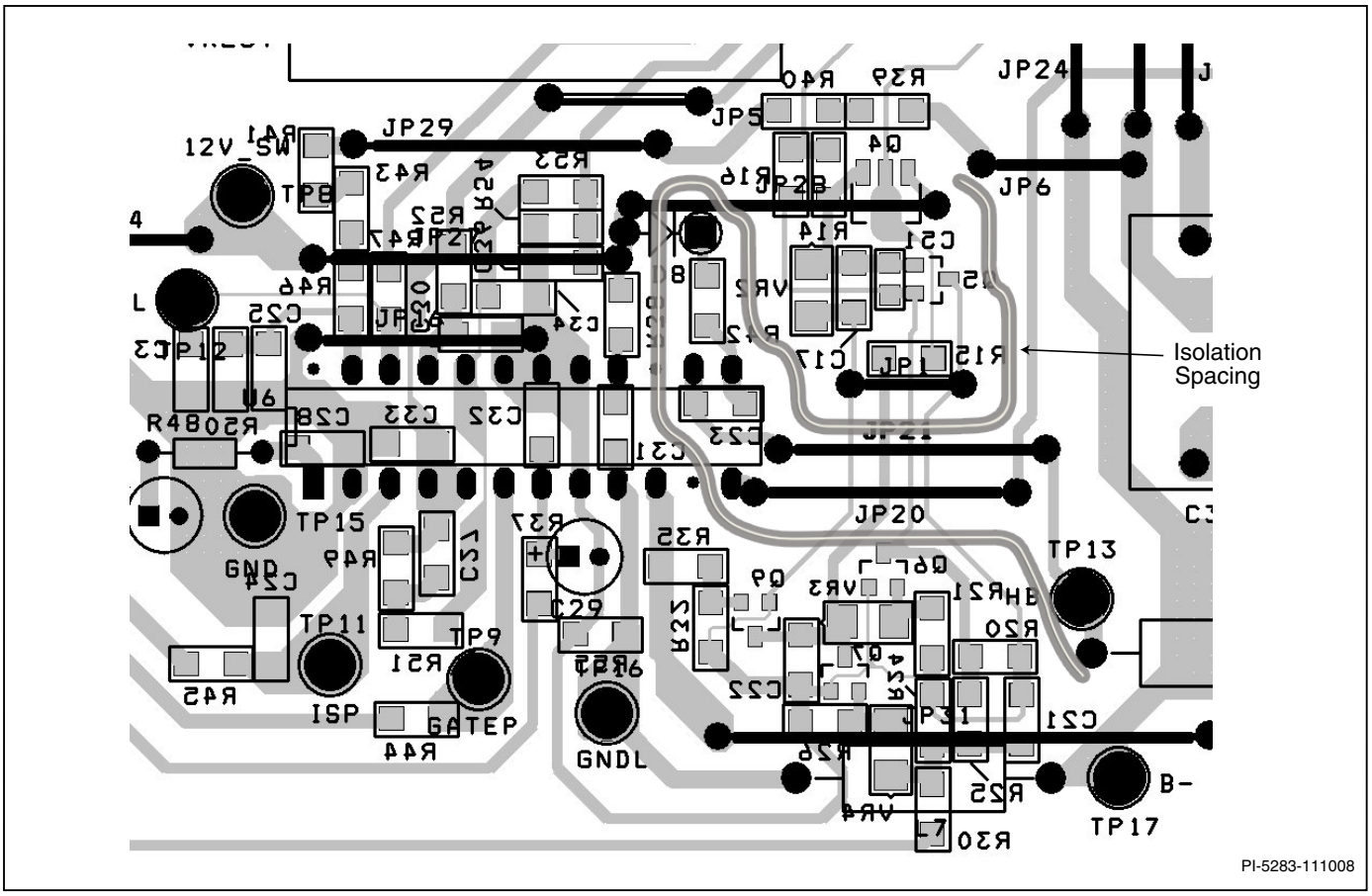


Figure 10. Isolation of High dv/dt Pins From Low Voltage Pins and Traces.

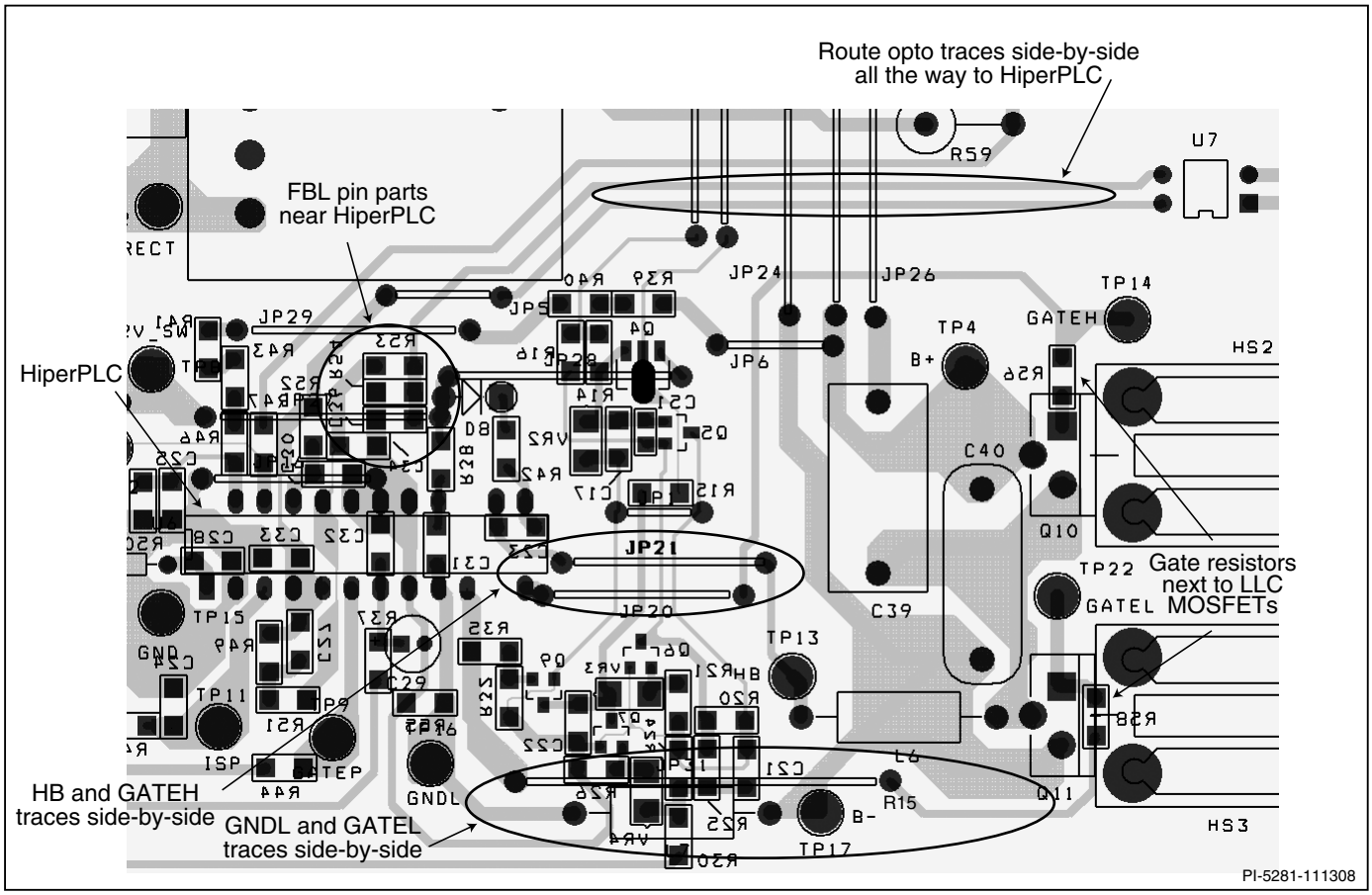


Figure 11. Gate Drive and Feedback PCB Layout Recommendations.

mounted far away from the IC. The 2 traces from the optocoupler (emitter and collector), should be run side by side to the FBL circuitry. This minimizes loop area and limits stray di/dt (inductive) noise coupling.

GATEL and GNDL

See Figure 11. The lines from GATEL pin, and the GNDL pins, which go to the LLC low side MOSFET Gate and Source respectively, should run side by side. The GNDL pin should be connected to the LLC low MOSFET Source pin via a ferrite bead. The gate resistor (R28) should also be mounted close to the MOSFET.

HB and GATEH

Refer to Figure 11. The HB and GATEH lines should run side by side from the LLC high side MOSFET to the PLC810PG. The gate resistor (R26) should be mounted close to the MOSFET.

Recommended PFC Gate Drive Circuit

Figure 13 shows the recommended PFC MOSFET gate drive circuit. This circuit needs to be placed close to the PFC MOSFET. The gate turn-off current is limited by R33, while gate turn-on current is limited by the sum of the values of R33 and R4. Resistor R4 also prevents high shoot-through currents flowing through both BJTs during switching edges. The resistor R4 is placed in series with the collector of Q8 instead of the emitter, as this will prevent negative Vbe voltage in Q8 which can lead to break down of the junction. Resistors R3 and R4 have a strong effect on PFC efficiency, and EMI. The local 1 µF bypass capacitor, C28, needs to be mounted close to the BJTs (Q8 and Q9). Resistor R107 is for keeping the MOSFET off when the PLC810PG is unpowered.

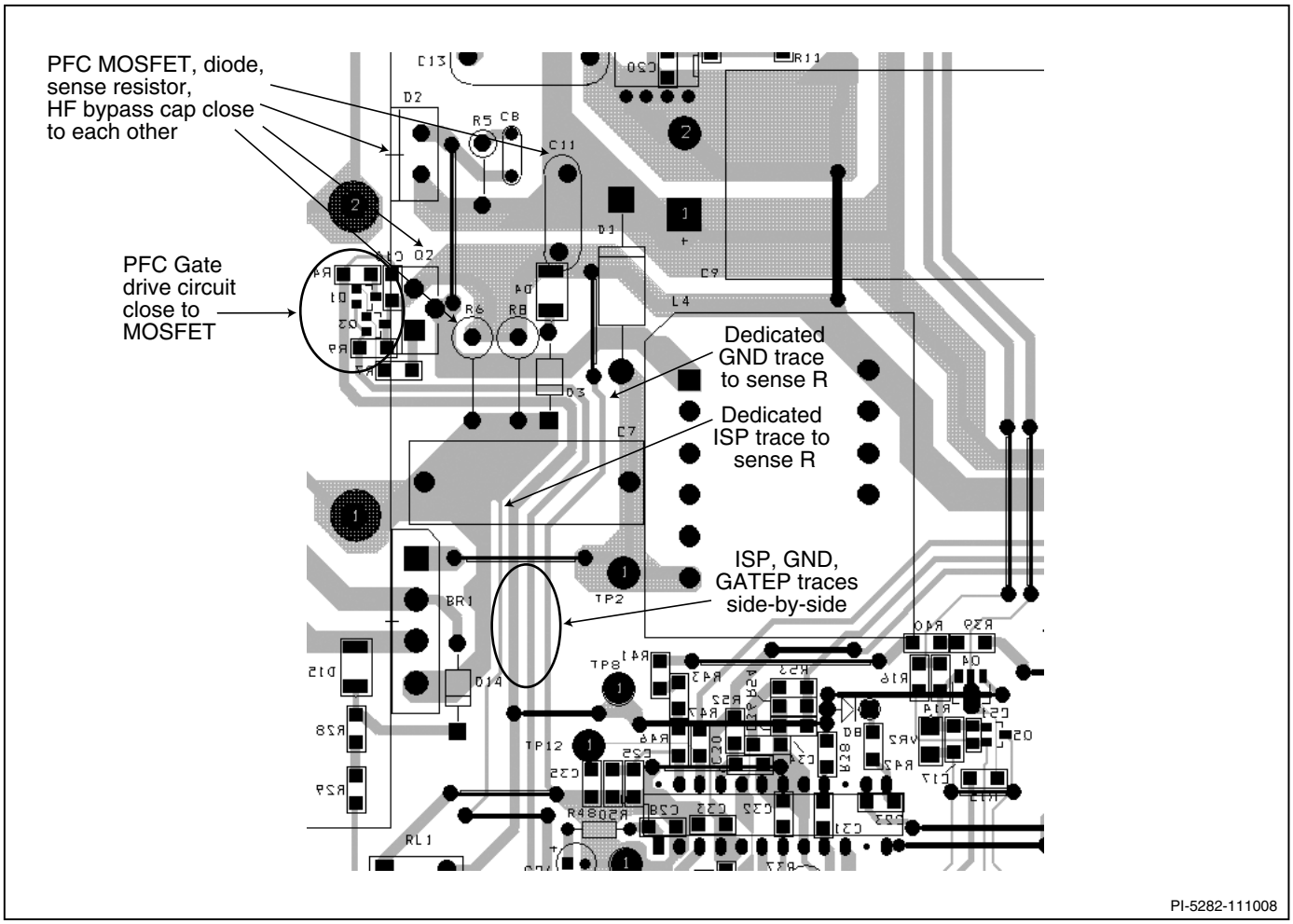


Figure 12. PFC Power and Signal Layout Recommendations.

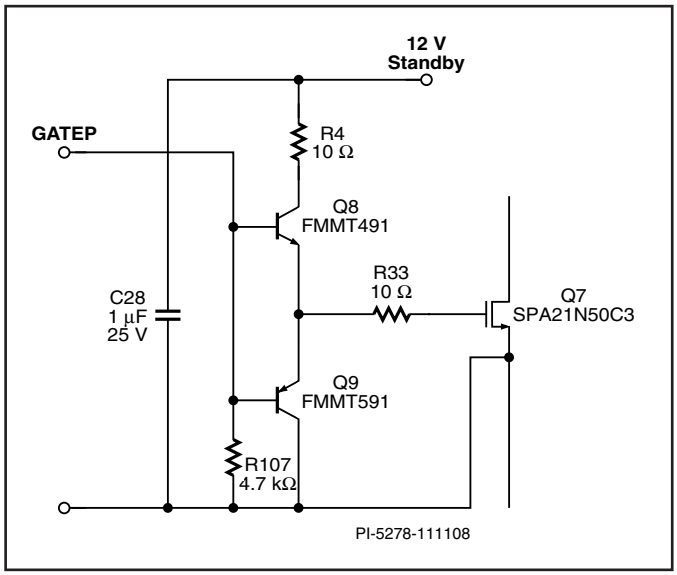


Figure 13. PFC Gate Drive Circuit Recommendation.

Absolute Maximum Ratings

Table 1 lists the absolute maximum ratings. Stress beyond these limits is likely to cause permanent damage to the PLC810PG. Exposure to conditions above recommended operating limits may effect performance and reliability. Normal ESD handling precautions are recommended.

Absolute Maximum Ratings	
Junction temperature ..... -40 °C to +125 °C	LLC high side floating output voltage (GATEH) ..... V_{HB}-0.3 to V_{VCCHB}+0.3
Storage temperature ..... -65 °C to +150 °C	LLC low side output voltage (GATEL) ..... -0.3 V to VCCL+0.3
Theta$_{JA}$ ..... 35 °C/W	GNDP to GND ..... -0.3 V to +0.3
Continuous supply voltage (VCC, VCCL) ..... -0.3 V to 15 V	GND to GNDL ..... -0.3 V to +0.3
LLC voltage (HB pin) ..... -0.3 V to 600 V	Power dissipation ..... 700 mW
LLC high side floating supply voltage (VCCHB pin with respect to HB pin) ..... -0.3 V to V_{CCL}	
Terminal Voltage With Respect To GND	
3.3 V Tolerant pins ..... -0.3 V to V_{REF}+0.3 V	ISL and ISP pins, max current ..... -100 mA
ISL and ISP pins ..... -0.65 V to V_{REF}+0.3 V	I_{FMAX} ..... 120 µA

Table 1. Absolute Maximum Ratings.

DC operating characteristics

Table 2 lists the minimum, typical, and maximum DC operating voltages and currents for all inputs and outputs of PLC810PG. Negative currents flow out of the IC, positive currents flow into the IC. The DC operating characteristics are for a junction temperature of -10 °C to 125 °C and VCC = 12 V, unless otherwise noted. All voltages are relative to GNDP, GNDL or GND (0 V). The pin names that are designated by VCC refer to VCC, VCCL and VCCHB. The voltages on this pins are respectively to GNDP/GND, GNDL and HB.

Parameter	Symbol	Pin	Notes	Min	Typ	Max	Units
Power Supply Current							
Startup Current	I_{CCOFF}	VCC	VCC/VCCL = UVLO - VCCHB = 0		60	120	µA
		VCCL			1.1	2	mA
Inhibit Current	$I_{CCINHIBIT}$	VCC	V(FBP) < INH (inhibit state) VCC/VCCL = 12 V VCCHB = 0		0.7	1.5	mA
		VCCL			1.1	2	
Operating Current	I_{CCON}	VCC	PFC and LLC operating 100 kHz / 50% duty cycle, GATE outputs unloaded, No Load on V_{REF} VCC/VCCL/VCCHB = 12 V		3.0	4.5	mA
		(VCCL + VCCHB)			7	9	
Leakage Current	I_{OZ}	ISP, ISL, FBP, VCOMP, FMAX	0 < V_{IN} < V_{REF}. Device in UVLO state.	-10		10	µA
Leakage Current	I_{OZ}	ISP	V_{IN} = -0.48 V		-10	-800	µA

Parameter	Symbol	Pin	Notes	Min	Typ	Max	Units
Undervoltage Lockout							
VCC Start Threshold Voltage	$V_{UVLO(+)}$	VCC	Device exits UVLO state when VCC exceeds $V_{UVLO(+)}$	8.2	9.1	10	V
		VCCHB - HB			9.2		
VCC Shutdown Threshold Voltage	$V_{UVLO(-)}$	VCC	Device enters UVLO state when VCC falls below $V_{UVLO(-)}$	7.2	8.1	9.0	V
		VCCHB - HB			8.7		
VCC Start-up/ Shutdown Hysteresis	$V_{UVLO(HYST)}$	VCC		0.7	1.0	1.3	V
LLC VCO							
VCO Frequency Range	F_{RANGE}	FBL	LLC/PFC Synchronized	50		300	kHz
Accuracy of VCO Min Frequency Limit	F_{MINACC}	FBL	R(FBL) = 100 kΩ to VREF	-15		+15	%
Accuracy of VCO Max Frequency Limit	F_{MAXACC}	FMAX	R(FMAX) = 17.8 kΩ to VREF	-15		+15	%
LLC Duty Cycle	DVCO	GATEH, GATEL	On-time matching GATEH (GATEH + GATEL)	49	50	51	%
Dead Time Accuracy	$t_{DVCOACC}$	GATEH, GATEL	R(FMAX) = 17.8 kΩ to VREF	-8		+12	%
Maximum FMAX Current	I_{FMAX}	FMAX	Power dissipation limit, I_{FBL} is limited by the current into FMAX			135	µA
FBL Current Upper Limit	I_{FBL}	FBL	Operating range of FBL controlled VCO		95		% I_{FMAX}
FBL Equivalent Input Circuit	$V_{IN(FBL)}$	FBL	FBL input behaves as $R_{IN(FBL)}$ in series with $V_{IN(FBL)}$. $I_{(FBL)}$ from 50 to 130 µA		0.65		V
	$R_{IN(FBL)}$				3.3		kΩ
FBL Pin Voltage	V_{FBL}	FBL	F_{VCO} = 100 kHz		0.83		V
FBL Soft Start Pull-up Resistance	$R_{PU(SS)}$	FBL	Internal pull-up to V_{REF} during soft start reset (4096 F_{MAX} cycles instantaneous)		900	1500	Ω
Fast LLC Overcurrent Fault Voltage Threshold	$V_{ISL(F)}$	ISL		1.33	1.4	1.47	V
Slow LLC Overcurrent Fault Voltage Threshold	$V_{ISL(S)}$	ISL	8 Cycle de-bounce	0.385	0.5	0.525	V
LLC Overcurrent Fault Pulse Width	T_{OVL}	ISL	Minimum time VISL exceeds $V_{ISL(F)}$/$V_{ISL(S)}$ per cycle to trigger fault		75		ns

Parameter	Symbol	Pin	Notes	Min	Typ	Max	Units
PFC							
PFC Overcurrent Limit Threshold	V_{OC}	ISP	Static Measurement	-440	-480	-520	mV
PFC Output Continuous Duty Cycle Range	DC_{PFC}	GATEP		0		100	%
PFC Error Amplifier Reference	V_{FBPREF}	FBP			2.2		V
PFC Error Amplifier Reference Accuracy	FBPREF	FBP		-2		2	%
PFC Overvoltage Threshold	$V_{OV(H)}$	FBP	See Note 1	103	105	107	$\%V_{FBPREF}$
PFC Inhibit Upper Threshold	INH	FBP	See Note 1	25	26	27	$\%V_{FBPREF}$
PFC Inhibit Lower Threshold	INL	FBP	See Note 1	22	23	24	$\%V_{FBPREF}$
Transconductance	G_M	FBP	$V_{FBP} = V_{FBPREF}$ ±85 mV	55	85	115	µA/V
LLC							
LLC Shutdown Upper Threshold	$V_{SD(H)}$	FBP	See Note 1	94.5	95.5	96.5	$\%V_{FBPREF}$
LLC Shutdown Lower Threshold	$V_{SD(L)}$	FBP	See Note 1	63	64	65	$\%V_{FBPREF}$
Reference							
Reference Voltage	V_{REF}	VREF	Loaded with I_{REF}	3.09	3.25	3.41	V
Current Source Capability of V_{REF} Pin	I_{REF}	VREF				5	mA
V_{REF} Capacitance	C_{REF}	VREF	Required external decoupling capacitance on VREF pin	1			µF
PFC GATE Output							
PFC GATE Output Voltage	$V_{GATE(P)}$	GATEP		GND		VCC	
Output Short-circuit Current Driving High	$I_{SC(H)}$	GATEP			25		mA
Output Short-circuit Current Driving Low	$I_{SC(L)}$	GATEP			60		mA
Output High Voltage	$V_{O(H)}$	GATEP	VCC = 12 V I_{OH} = 1.25 mA	11.5	11.8		V
Output Low Voltage	$V_{O(L)}$	GATEP	VCC = 12 V I_{OL} = 5 mA		0.5	0.75	V

Parameter	Symbol	Pin	Notes	Min	Typ	Max	Units
LLC GATE Driver							
LLC High Side Output Voltage	$V_{GATE(H)}$	GATEH		VHB		VCCHB	
LLC Low Side Output Voltage	$V_{GATE(L)}$	GATEL		VCOM		VCCL	
Output High Voltage	$V_{O(H)}$	GATEH, GATEL	VCCL/VCCHB = 12 V I_{OH} = -65 mA	11	11.4		V
Output Low Voltage	$V_{O(L)}$	GATEH, GATEL	VCCL/VCCHB = 12 V I_{OL} = 130 mA		0.5	1	V
Output Short-circuit Current Driving High	$I_{SC(H)}$	GATEH/ GATEL	VCCL/VCCHB = 12 V PW <10 µS		-0.8	-0.5	A
Output Short-circuit Current Driving Low	$I_{SC(L)}$	GATEH/ GATEL	VCCL/VCCHB = 12 V PW <10 µS	0.9	1.4		A
Maximum Allowed Slew Rate on HB Pin	$dV_{HB/dt}$	HB			10		V/nsec
Turn On Rise Time (10% - 90%)	T_R	GATEH, GATEL	VCCL/VCCHB = 12 V 1000 pF load capacitance		50		nsec
Turn Off Fall Time (90% - 10%)	T_F	GATEH, GATEL	VCCL/VCCHB = 12 V 1000 pF load capacitance		25		nsec

Table 2. DC Operating Characterisitics.

Notes:

1. This parameter tracks V_{FBPREF}.

Typical Performance Characteristics

Figure 14. FMAX Pin Pull-up Resistor to VREF Pin vs. Dead-time Requirement.

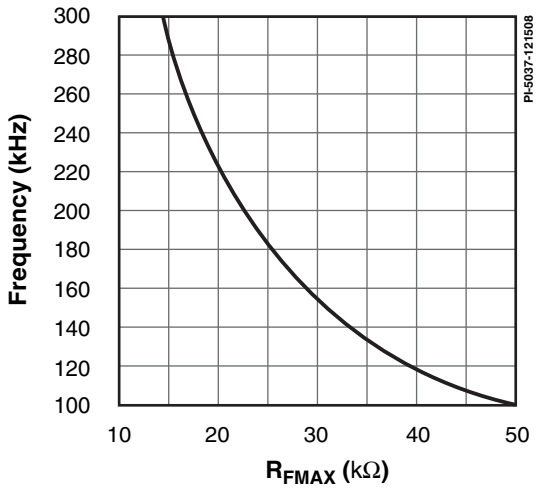


Figure 15. Maximum Frequency Limit vs. Pull-up Resistor from FMAX Pin to VREF Pin.

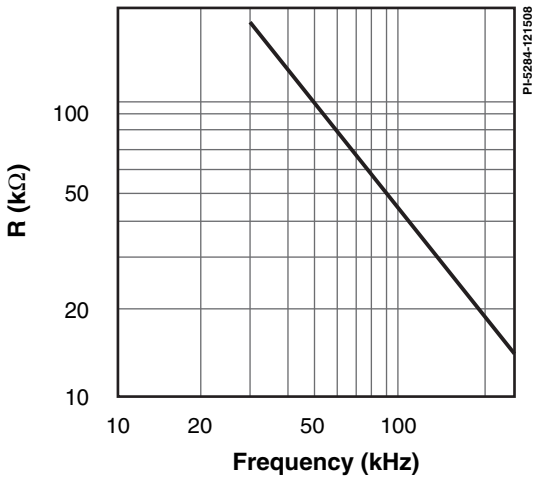


Figure 16. Pull-up Resistance from FBL Pin to VREF Pin vs. Switching Frequency

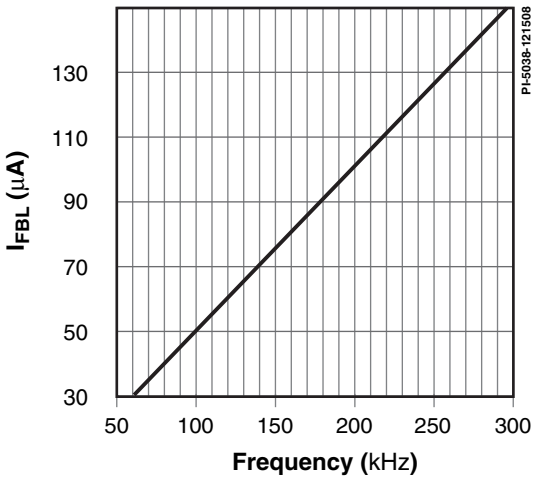
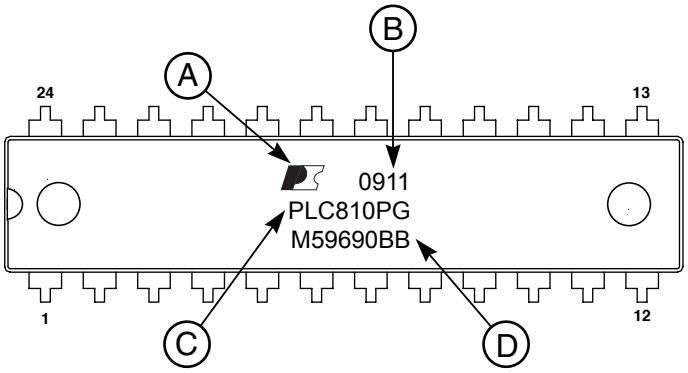


Figure 17. FBL Pin Current vs. Switching Frequency.

Package Information and Part Marking

The PLC810PG is packaged in a 24 lead 0.300 PDIP package (Figure 18 shows the PLC810PG part marking). Figure 19 shows the package outline and dimensions.

HiperPLC MARKING



A. Power Integrations Registered Trademark
B. Encapsulation Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-5163-081309

Figure 18. PLC810PG Part Marking.

PDIP-24 (0.300”)

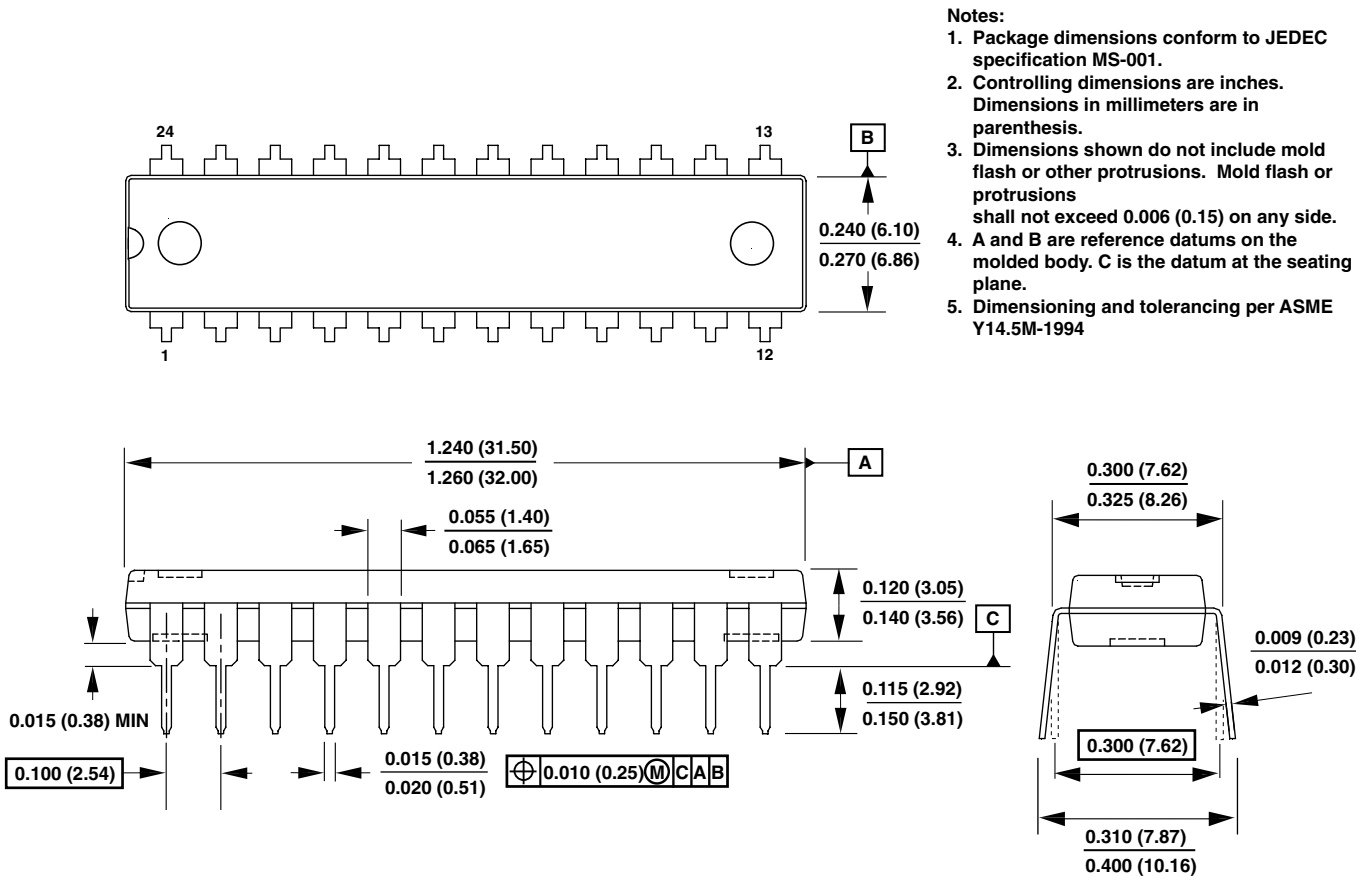


Figure 19. PDIP-24 Package Marking.

Revision	Notes	Date
A	Initial Release	11/08
B	Revised figures and text	11/08
C	Text, schematic updates	12/08
D	Schematic updates	02/09
E	Fixed schematic Figure 4 error and removed Note 2 from Parameter Table	05/09
F	Updated Figures 4, 6, 14 and 18	08/09

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