8-Channel CMOS Logic to High Voltage Level Translator

ADG3123

FEATURES

- 2.3 V to 5.5 V input voltage range
- Output voltage levels (V_{DDA} and V_{DDB} to $V_{SS} \leq 35$ V)
  - Low output voltage levels: down to −24.4 V
  - High output voltage levels: up to +35 V
- Rise/fall time: 12 ns/19.5 ns typical
- Propagation delay: 80 ns typical
- Operating frequency: 100 kHz typical
- Ultralow quiescent current: 65 µA typical
- 20-lead, Pb-free, TSSOP package

APPLICATIONS

- Low voltage to high voltage translation
- TFT-LCD panels
- Piezoelectric motor drivers

FUNCTIONAL BLOCK DIAGRAM

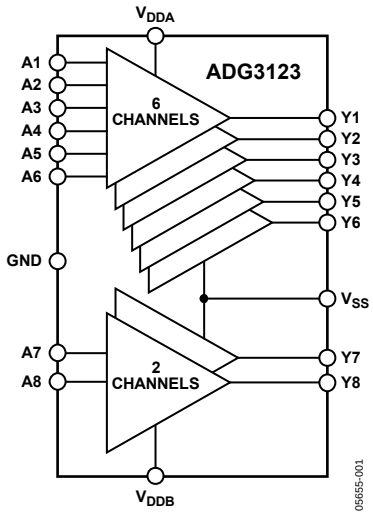

Figure 1.

GENERAL DESCRIPTION

The ADG3123 is an 8-channel, noninverting CMOS to high voltage level translator. Fabricated on an enhanced LC^{2}MOS process, the device is capable of operating at high supply voltages while maintaining ultralow power consumption.

The internal architecture of the device ensures compatibility with logic circuits running from supply voltages within the 2.3 V to 5.5 V range. The voltages applied to Pin V_{DDA}, Pin V_{DDB}, and Pin V_{SS} set the logic levels available at the outputs on the Y side of the device. Pin V_{DDA} and Pin V_{DDB} set the high output level for Pin Y1 to Pin Y6 and for Pin Y7 to Pin Y8, respectively. The V_{SS} pin sets the low output level for all channels. The ADG3123 can provide output voltages levels down to −10 V for a low input level and up to +30 V for a high input logic level. For proper operation, V_{DDB} must always be greater than or equal to V_{DDA} and the voltage between the Pin V_{DDB} and Pin V_{SS} should not exceed 35 V.

The low output impedance of the channels guarantees fast rise and fall times even for significant capacitive loads. This feature, combined with low propagation delay and low power consumption, makes the ADG3123 an ideal driver for TFT-LCD panel applications.

The ADG3123 is guaranteed to operate over the −40°C to +85°C temperature range and is available in a compact, 20-lead TSSOP, Pb-free package.

PRODUCT HIGHLIGHTS

1. Compatible with a wide range of CMOS logic levels.
2. High output voltage levels.
3. Fast rise and fall times coupled with low propagation delay.
4. Ultralow power consumption.
5. Compact, 20-lead TSSOP, Pb-free package.

Rev. A

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REVISION HISTORY

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9/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DDA} = V_{DDB} = 27 V, V_{SS} = −7 V, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Min	Typ[2]	Max	Unit	Conditions
DIGITAL INPUTS (Pin A1 to Pin A8)						V_{AX} = 0 V to 5.5 V
Input High Voltage	V_{IH}	1.7			V	
Input Low Voltage	V_{IL}			0.8	V	
Leakage Current	I_{IL}		±0.03	±1	µA	
Capacitance[3]	C_I		1		pF	
ANALOG INPUTS (Pin V_{DDA})						
Input Voltage Range	V_{DDA}	0		V_{DDB}	V	
DIGITAL OUTPUTS (Pin Y1 to Pin Y8)						V_{DDA} = V_{DDB} = 25 V to 30 V, V_{SS} = −5 V to −7 V, V_{DDA} and V_{DDB} to V_{SS} ≤ 35V
Output High Voltage (Pin Y1 to Pin Y6)	V_{OH}	V_{DDA} − 1			V	I_{OH} = −10 mA
Output High Voltage (Pin Y7 to Pin Y8)	V_{OH}	V_{DDB} − 1			V	I_{OH} = −10 mA
Output Low Voltage	V_{OL}			V_{SS} + 1	V	I_{OL} = +10 mA
Output Impedance	R_0		30		Ω	V_{DDA} = V_{DDB} = +27 V, V_{SS} = −7 V
SWITCHING CHARACTERISTICS[3]						See Figure 2
Propagation Delay						
Low to High Transition	t_{PLH}		76	125	ns	
High to Low Transition	t_{PHL}		80	125	ns	
Rise Time	t_R		12	20	ns	
Fall Time	t_F		19.5	32	ns	
Maximum Operating Frequency	F_0	50	100		kHz	100 pF load, all channels, see Figure 2
POWER REQUIREMENTS						
Quiescent Power Supply Current	I_{DDA}		0.03	1	µA	V_{AX} = 0 V or 5.5 V, no load, V_{DDA} ≤ V_{DDB}
	I_{DDB}		65	150	µA	
	I_{SS}		0.03	1	µA	
Power Supply Voltages						
V_{DDB} to V_{SS}		10.8		35	V	
V_{DDB} to GND	V_{DDB}	10.8		35	V	V_{DDB} to V_{SS} ≤ 35 V
V_{SS} to GND	V_{SS}	−24.2		0	V	V_{DDB} to V_{SS} ≤ 35 V

[1] Temperature range for B version is −40°C to +85°C.
[2] Typical values are specified at 25°C.
[3] Guaranteed by design; not subject to production testing.

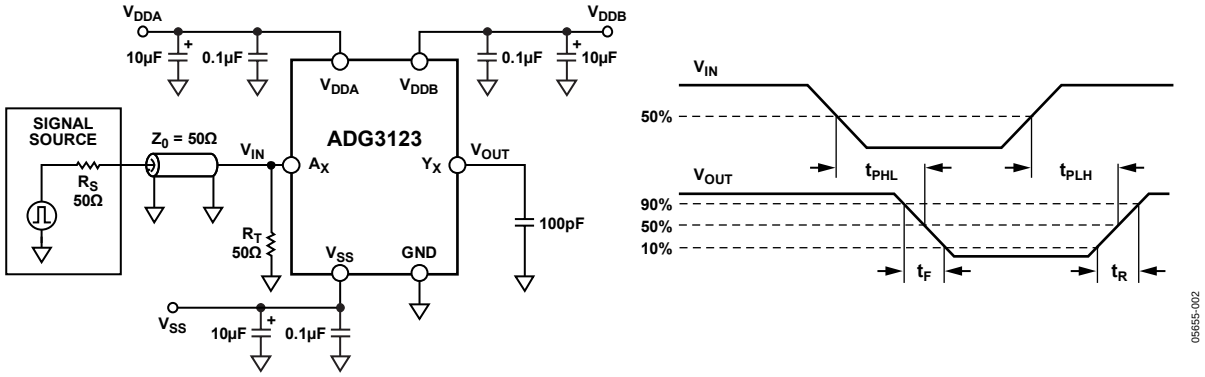


Figure 2. Switching Characteristics Test Circuit

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DDA}/V_{DDB} to V_{SS}	44 V
V_{DDB} to GND	−0.3 V to +32 V
V_{DDA} to GND	−0.3 V to V_{DDB}
V_{SS} to GND	+0.3 V to −32 V
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DDB} + 0.3 V or 20 mA, whichever occurs first
Load Current Per Device	
Average	15 mA at 25°C
	8 mA at 85°C
Peak Current[2]	150 mA at 25°C
	80 mA at 85°C
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	78°C/W[3]
Reflow Soldering (Pb-Free)	
Peak Temperature	260 (+0/−5)°C
Time at Peak Temperature	10 seconds to 40 seconds

[1] Overvoltage at Pin A1 to Pin A8 is clamped by internal diodes. Limit the current to the maximum ratings given.
[2] Pulsed at 100 kHz; 10% duty cycle maximum with the load shown in Figure 2.
[3] Guaranteed when the device is soldered on a 4-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

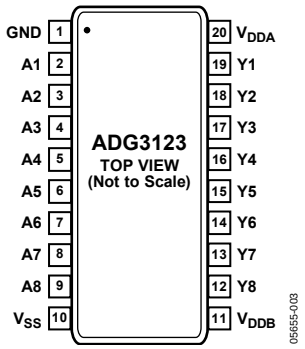


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Reference (0 V).
2 to 9	A1 to A8	Level Translator CMOS Inputs.
10	V_{SS}	Most Negative Power Supply. Use the V_{SS} pin to generate the output low level for Output Y1 to Output Y8.
11	V_{DDB}	Positive Power Supply. Use the V_{DDB} pin to generate the output high level for Output Y7 and Output Y8.
12 to 19	Y8 to Y1	Level Translator High Voltage Outputs.
20	V_{DDA}	Analog Input. Use the V_{DDA} pin to generate the output high level for Output Y1 to Output Y6 ($V_{DDA} \leq V_{DDB}$).

TYPICAL PERFORMANCE CHARACTERISTICS

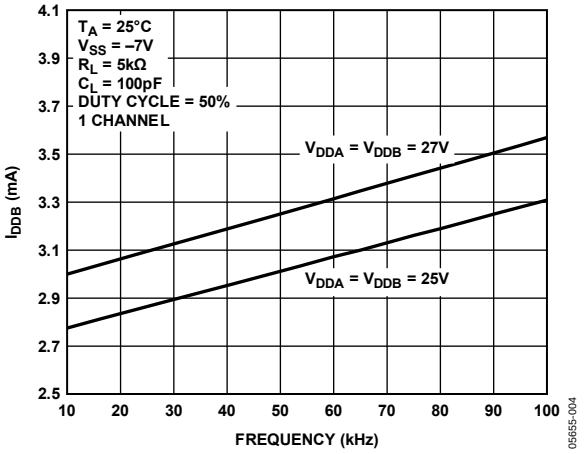


Figure 4. Supply Current (I_{DDB}) vs. Frequency

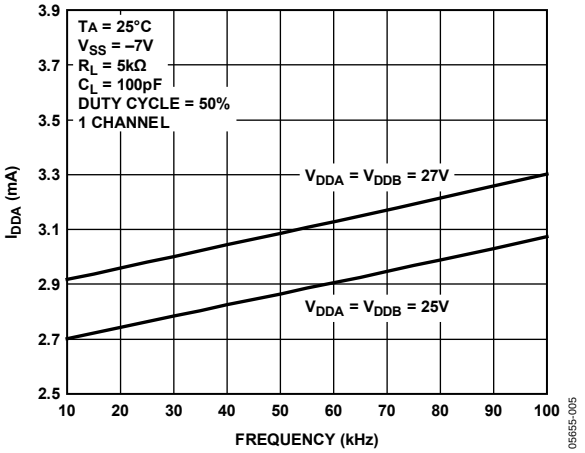


Figure 5. Supply Current (I_{DDA}) vs. Frequency

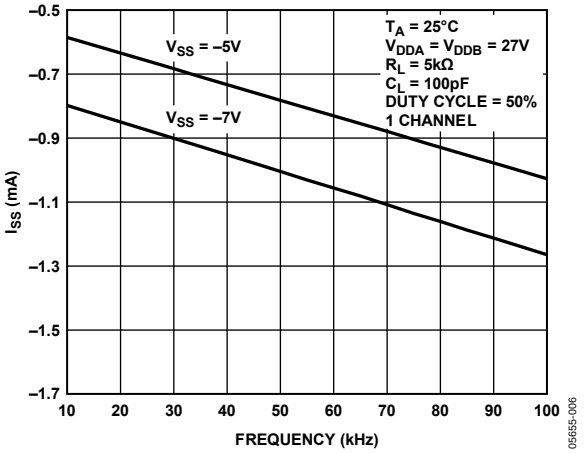


Figure 6. Supply Current (I_{SS}) vs. Frequency

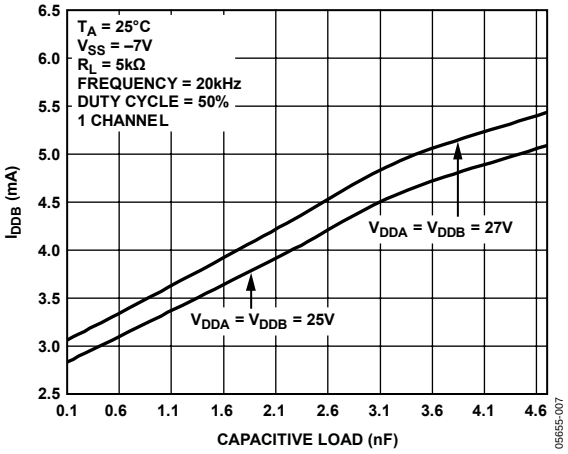


Figure 7. Supply Current (I_{DDB}) vs. Capacitive Load

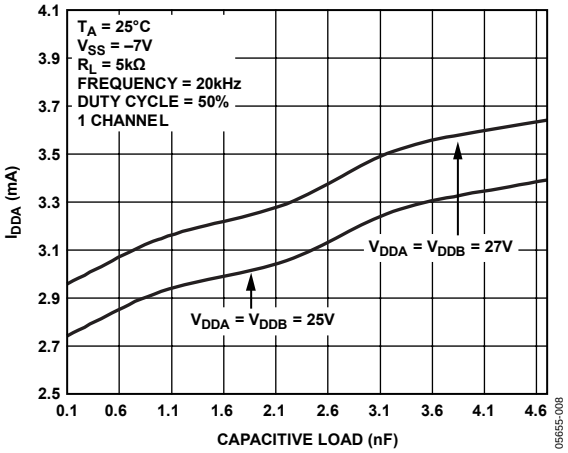


Figure 8. Supply Current (I_{DDA}) vs. Capacitive Load

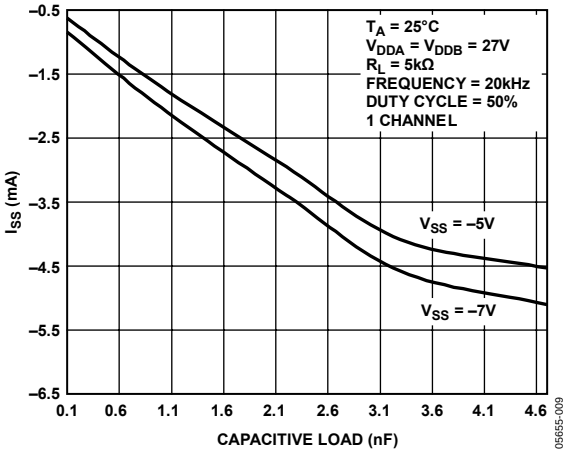


Figure 9. Supply Current (I_{SS}) vs. Capacitive Load

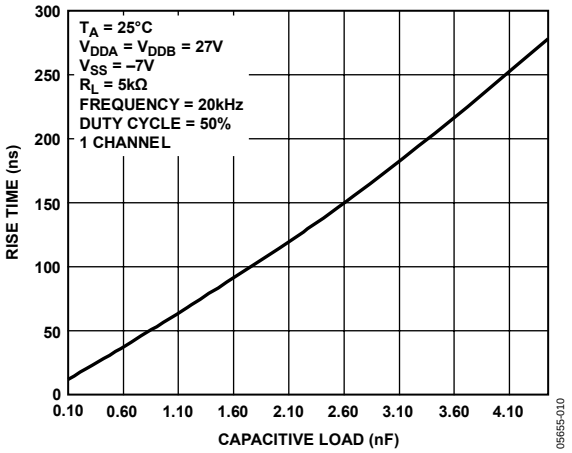


Figure 10. Rise Time vs. Capacitive Load

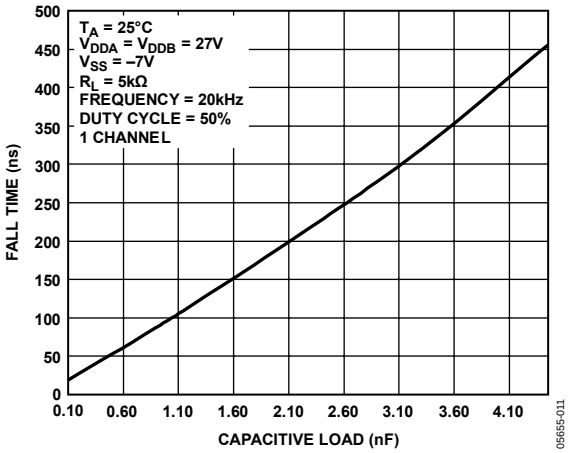


Figure 11. Fall Time vs. Capacitive Load

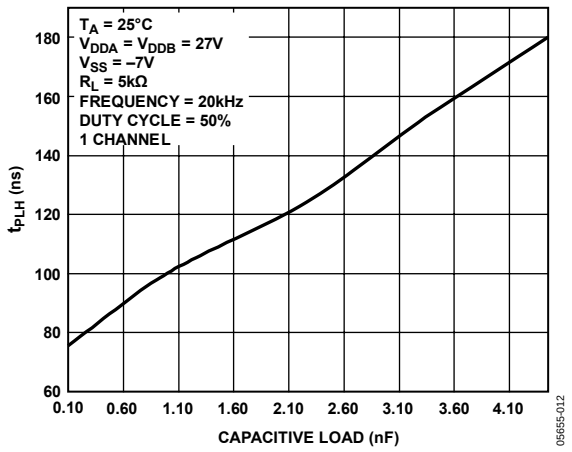


Figure 12. Propagation Delay (t_{PLH}) vs. Capacitive Load

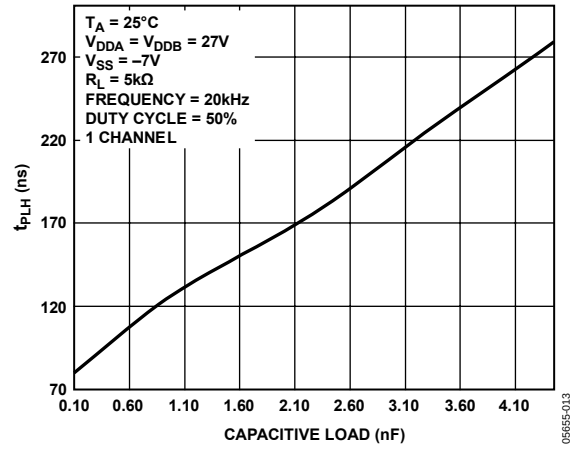


Figure 13. Propagation Delay (t_{PHL}) vs. Capacitive Load

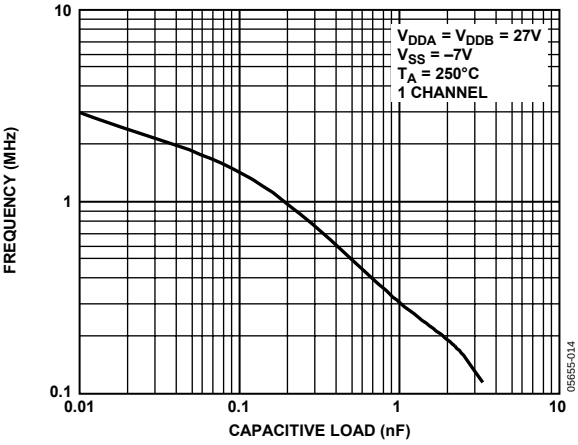


Figure 14. Maximum Operating Frequency vs. Capacitive Load (One Channel)

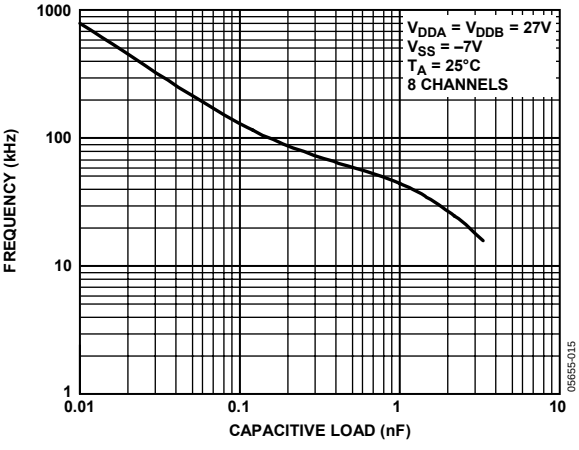


Figure 15. Maximum Operating Frequency vs. Capacitive Load (Eight Channels)

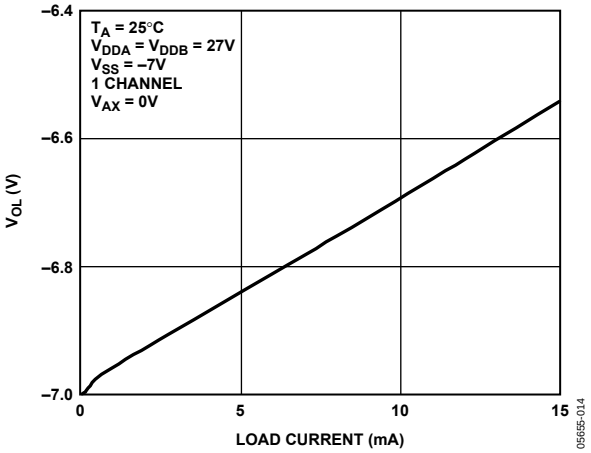


Figure 16. Output Voltage (V_{OL}) vs. Load Current

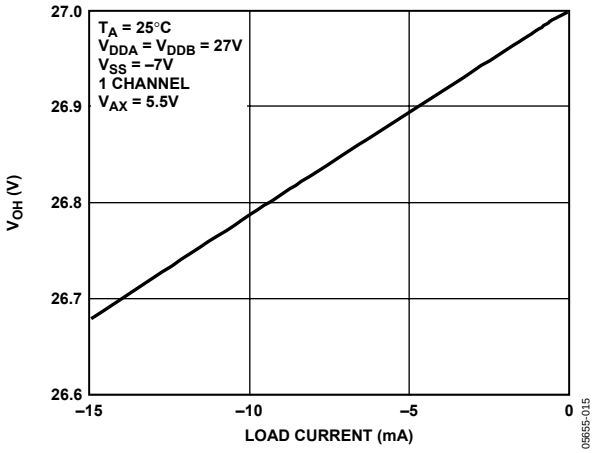


Figure 17. Output Voltage (V_{OH}) vs. Load Current

TERMINOLOGY

V_{IH}
Logic input high voltage at Pin A1 to Pin A8.

V_{IL}
Logic input low voltage at Pin A1 to Pin A8.

I_{IL}
Leakage current at Pin A1 to Pin A8.

C_I
Capacitance measured at Pin A1 to Pin A8.

V_{OH}

Logic output high voltage at Pin Y1 to Pin Y8.

V_{OL}
Logic output low voltage at Pin Y1 to Pin Y8.

Ro
Output impedance.

t_{PLH}
Propagation delay through the part measured between the input signal applied to any one channel and its corresponding output for a low-to-high transition (see Figure 2).

t_{PHL}
Propagation delay through the part measured between the input signal applied to any one channel and its corresponding output for a high-to-low transition (see Figure 2).

t_R
Rise time of the output signal at Pin Y1 to Pin Y8 (see Figure 2).

t_F
Fall time of the output signal at the Pin Y1 to Pin Y8 (see Figure 2).

F_O
Frequency of the signal applied to the A1 to A8 input pins.

V_{DDA}
Input voltage used to generate the high logic levels for Y1 to Y6 outputs.

V_{DDB}
Positive power supply voltage. Also used to generate the high logic levels for Y7 to Y8 outputs.

V_{SS}
Negative power supply voltage. It is used to generate the low logic level for Y1 to Y8 outputs.

GND
Ground (0 V) reference.

I_{DDA}
Supply current at the V_{DDA} pin.

I_{DDB}
Supply current at the V_{DDB} pin.

I_{SS}
Supply current at the V_{SS} pin.

THEORY OF OPERATION

The ADG3123 is an 8-channel, noninverting CMOS to high voltage level translator. Fabricated on an enhanced LC²MOS process, the device is capable of operating at high supply voltages while maintaining ultralow power consumption.

The device requires a dual-supply voltage, V_{DDB} and V_{SS}, which sets the low logic levels for all outputs and the high logic levels for the Y7 and Y8 outputs. The V_{DDA} pin acts as an analog input. The voltage applied to the V_{DDA} pin sets the output high logic level for the Y1 to Y6 outputs.

The device translates the CMOS logic levels applied to the A1 to A8 inputs into high voltage bipolar levels available on the Y side of the device at Pin Y1 to Pin Y8.

To ensure proper operation, V_{DDB} must always be greater than or equal to V_{DDA} and the voltage between the Pin V_{DDB} and Pin V_{SS} should not exceed 35 V.

INPUT DRIVING REQUIREMENTS

The ADG3123 design ensures low input capacitance and leakage current thereby reducing the loading of the circuit that drives the input pins (Pin A1 to Pin A8) to a minimum. Its input threshold levels are compliant with JEDEC standards for drivers operated from supply voltages between 2.3 V and 5.5 V. It is recommended that the inputs of any unused channel be tied to a stable logic level (low or high).

OUTPUT LOAD REQUIREMENTS

The low output impedance of the ADG3123 allows each channel to drive both resistive and capacitive loads. The maximum load current is limited by the current carrying capability of any given channel. If more channels are used, the maximum load current per channel is reduced accordingly. Note that the sum of the load currents on all channels should never exceed the absolute maximum ratings specifications.

The average load current on each channel, $I_{CHANNEL}$, can be determined using the formulas shown in the Capacitive Loads and the Resistive Loads sections.

Capacitive Loads

$$I_{CHANNEL}(A) = F_O \times C_L \times (V_{DDX} + |V_{SS}|)$$

where:

F_O is the frequency of the signal applied to the channel in Hz.
C_L is the load capacitance in farads.
V_{SS} is the voltage applied to the V_{SS} pin.
V_{DDX} is V_{DDA} for Y1 to Y6 outputs, and V_{DDB} for Y7 to Y8 outputs.

Resistive Loads

$$I_{CHANNEL}(A) = \frac{D \times V_{DDX} + (1 - D) \times |V_{SS}|}{R_L}$$

where:

D is the duty cycle of the input signal. D is defined as the ratio between the high state duration of the signal and its period.
R_L is the load resistor in Ω.
V_{SS} is the voltage applied to the V_{SS} pin.
V_{DDX} is V_{DDA} for Y1 to Y6 outputs, and V_{DDB} for Y7 to Y8 outputs.

POWER SUPPLIES

The ADG3123 operates from a dual-supply voltage. As good design practice for all CMOS devices dictates, power up the ADG3123 first (V_{DDB} and V_{SS}) before applying the signals to its inputs (A1 to A8 and V_{DDA}). To ensure correct operation of the ADG3123, the voltage applied to the V_{DDB} pin must always be greater than or equal to V_{DDA} and the voltage between the Pin V_{DDB} and Pin V_{SS} should not exceed 35 V.

To ensure optimum performance, use decoupling capacitors on all power supply pins. Furthermore, good engineering and layout practice suggests placing these capacitors as close as possible to the package supply pins.

APPLICATIONS

The high voltage operation coupled with high current driving capability and the wide range of CMOS levels accepted by the ADG3123, make the device ideal for LCD-TFT panel applications. In this type of application, the controllers that generate the timing signals required to control the pixel scanning process inside the panel are usually low voltage CMOS devices.

Most LCD-TFT panels operate at high supply voltages; therefore, the timing signals generated by the controller require level translation to drive the panel. Figure 18 shows a typical application circuit where the ADG3123 translates eight timing signals provided by the timing controller into high voltage logic levels required to drive the panel.

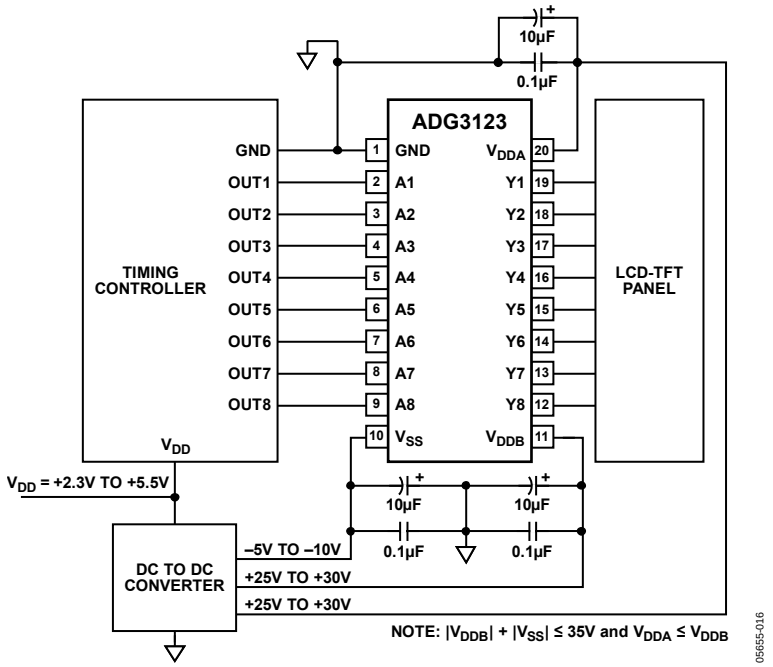
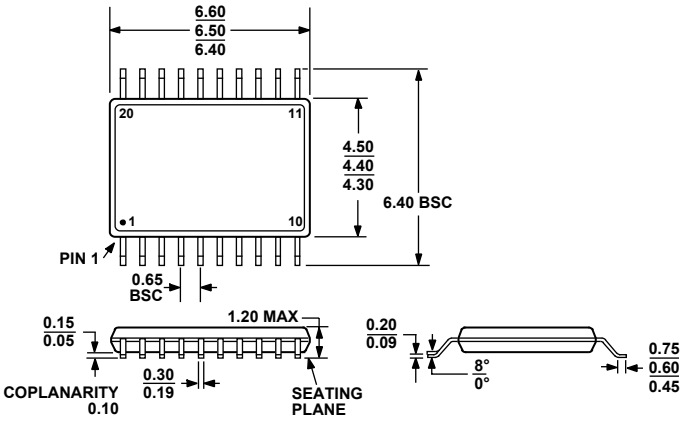


Figure 18. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 19. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG3123BRUZ[1]	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20
ADG3123BRUZ-REEL[1]	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20
ADG3123BRUZ-REEL7[1]	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20

[1] Z = Pb-free part.