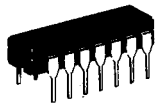
MPQ6001 (SILICON)
MPQ6002
MPQ6501
MPQ6502

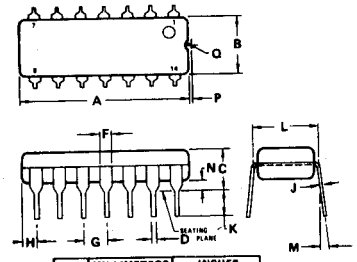
QUAD DUAL-IN-LINE SILICON ANNULAR COMPLEMENTARY PAIR TRANSISTORS

. . . designed for high-speed switching circuits, DC to VHF amplifier applications and complementary circuitry.

- DC Current Gain Specified – 1.0 to 300 mAdc
- High Current-Gain–Bandwidth Product
  f_T = 400 MHz (Typ) @ I_C = 50 mAdc
- NPN Transistor Similar to 2N2218 or 2N2219
- PNP Transistor Similar to 2N2904 or 2N2905
- TO-116 Package – Compact Size Compatible with IC Automatic Insertion Equipment
- MPQ6501, MPQ6502 Matching Characteristics Available as Specials on Q1-Q4 and Q2-Q3.

QUAD DUAL-IN-LINE SILICON COMPLEMENTARY PAIR TRANSISTORS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	30		Vdc
Collector-Base Voltage	V_{CB}	60		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	500		mAdc
		Each Transistor	Four Transistors Equal Power	
Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	650 5.18	1250 10	mW mW/°C
Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 8.0	3.0 24	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

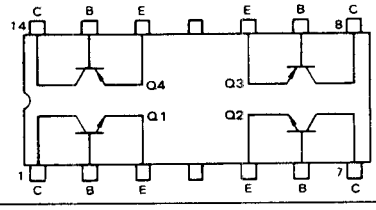
(1) Second Breakdown occurs at power levels greater than 3 times the power dissipation rating.

THERMAL CHARACTERISTICS

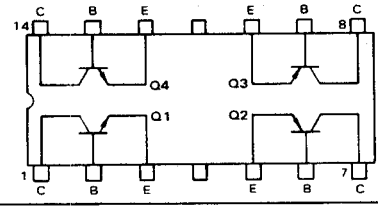
Characteristic		Junction to Case	Junction to Ambient	Unit
Thermal Resistance	Each Die	125	193	°C/W
	Effective, 4 Die	41.6	100	°C/W
Coupling Factors	Q1-Q4 or Q2-Q3	30	60	%
	Q1-Q2 or Q3-Q4	2.0	24	%

CONNECTION DIAGRAM

MPQ6001, MPQ6002



MPQ6501, MPQ6502



THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

Where ΔT_{J1} is the change in junction temperature of die 1
$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4
P_{D1} thru 4 is the power dissipated in die 1 through 4
$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4 P_D$ equation (3) can be further simplified and by substituting into equation (2) results in

(4) $R_{\theta(EFF)} = R_{\theta 1}(1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		BV_{CBO}	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	5.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)		I_{CBO}	–	–	30	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	–	30	nAdc
ON CHARACTERISTICS						
DC Current Gain(1)		h_{FE}				–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc	MPQ6001,6501		25	35	–	
	MPQ6002,6502		50	65	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	MPQ6001,6501		35	50	–	
	MPQ6002,6502		75	90	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)	MPQ6001,6501		40	65	–	
	MPQ6002,6502		100	120	–	
(I_C = 300 mAdc, V_{CE} = 10 Vdc)	MPQ6001,6501		20	25	–	
	MPQ6002,6502		30	35	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$				Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)			–	0.2	0.4	
(I_C = 300 mAdc, I_B = 30 mAdc)			–	0.35	1.4	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$				Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)			–	0.9	1.3	
(I_C = 300 mAdc, I_B = 30 mAdc)			–	1.0	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product (1) (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)		f_T	200	350	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	PNP	C_{ob}	–	6.0	8.0	pF
	NPN		–	4.5	8.0	
Input Capacitance (V_{EB} = 2.0 Vdc, I_C = 0, f = 100 kHz)	PNP	C_{ib}	–	20	30	pF
	NPN		–	17	30	
SWITCHING CHARACTERISTICS						
Turn-On Time (V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc, Figure 1)		t_{on}	–	30	–	ns
Turn-Off Time (V_{CC} = 30 Vdc, I_C = 150 mAdc, $I_{B1} = I_{B2}$ = 15 mAdc, Figure 2)		t_{off}	–	225	–	ns

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

NPN SATURATED SWITCHING TIME TEST CIRCUITS

For PNP Switching Tests, reverse the diodes, voltage polarities, and input pulses.

FIGURE 1 – NPN TURN-ON TIME

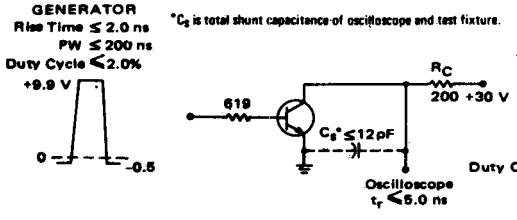


FIGURE 2 – NPN TURN-OFF TIME