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FAIRCHILD

August 2016

FAN3850A
Microphone Pre-Amplifier with Digital Output

Features

- Optimized for Mobile Handset and Notebook PC Microphone Applications
- Accepts Input from Electret Condenser Microphones (ECM)
- Pulse Density Modulation (PDM) Output
- Standard 5-Wire Digital Interface
- 16dB Gain
- Low Input Capacitance, High PSR, 20 kHz Pre-Amplifier
- Low-Power 1.5 µA Sleep Mode
- Typical 470 µA Supply Current
- SNR of 62 dB(A) for 16 dB Gain Respectively
- Total Harmonic Distortion 0.02%
- Input Clock Frequency Range of 1-4 MHz
- Integrated Low Drop-Out Regulator (LDO)
- Small 1.26 mm x 0.86 mm 6-Ball WLCSP Package

Description

The FAN3850A integrates a pre-amplifier, LDO, and ADC that converts Electret Condenser Microphone (ECM) outputs to digital Pulse Density Modulation (PDM) data streams. The pre-amplifier accepts analog signals from the ECM and drives an over-sampled sigma delta Analog-to-Digital Converter (ADC) and outputs PDM data. The PDM digital audio has the advantage of noise rejection and easy interface to mobile handset processors.

The FAN3850A features an integrated LDO and is powered from the system supply rails up to 3.63 V, with low power consumption of only 0.85 mW and less than 20 µW in Power-Down Mode.

Applications

- Electret Condenser Microphones with Digital Output
- Mobile Handset
- Headset Accessories
- Personal Computer (PC)

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Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN3850AUC16X	-30°C to +85°C	6 Ball, Wafer-Level Chip-Scale Package (WLCSP)	3000 Units on Tape & Reel

Block Diagram

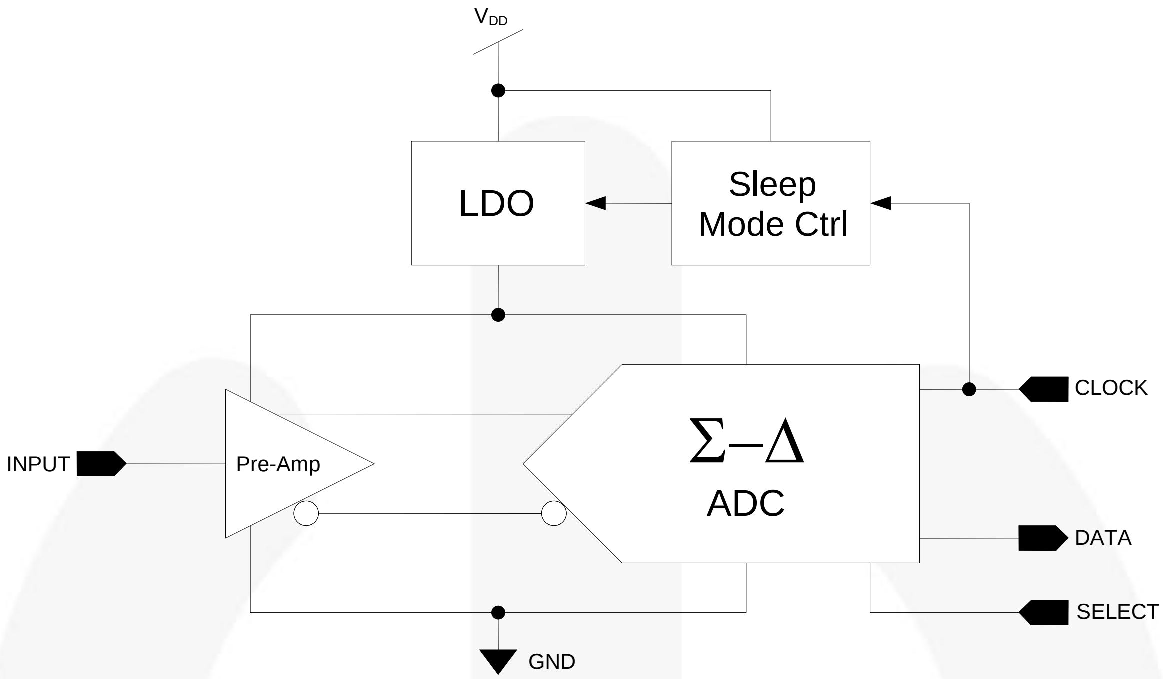


Figure 1. Block Diagram

Pin Configuration

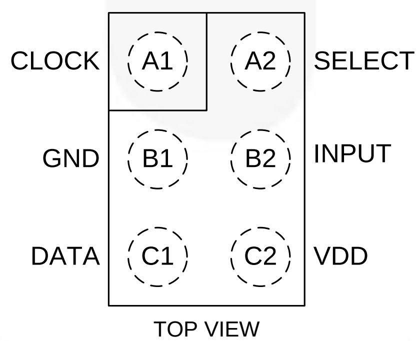


Figure 2. Pin Assignments

Pin Definitions

Pin#	Name	Type	Description
A1	CLOCK	Input	Clock Input
B1	GND	Input	Ground Pin
C1	DATA	Output	PDM Output – 1 Bit ADC
A2	SELECT	Input	Rising or Falling Clock Edge Select
B2	INPUT	Input	Microphone Input
C2	VDD	Input	Device Power Pin

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	-0.3	4.0	V
V_{IO}	Digital I/O	-0.3	V_{DD}+0.3	V
	Microphone Input	-0.3	2.2	
ESD	Human Body Model, JESD22-A114, All Pins Except Microphone Input	±7		kV
	Human Body Model, JESD22-A114 – Microphone Input	±300		V

Note:
1. This device is fabricated using CMOS technology and is therefore susceptible to damage from electrostatic discharges. Appropriate precautions must be taken during handling and storage of this device to prevent exposure to ESD.

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+125	°C
T_{RFLW}	Peak Reflow Temperature			+260	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		90		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-30		+85	°C
V_{DD}	Supply Voltage Range	1.64	1.80	3.63	V
t_{RF-CLK}	Clock Rise and Fall Time			10	ns

Device Specific Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8 V, V_{IN}=94 dB (SPL), and f_{CLK}=2.4 MHz. Duty Cycle=50% and C_{MIC}=15 pF.

Symbol	Parameter	FAN3850AUC16X			Unit
		Min.	Typ.	Max.	
SNR	Signal-to-Noise Ratio f_{IN}=1kHz (1Pa), A-Weighted		62		dB(A)
e_N	Total Input RMS Noise(3) 20Hz to 20kHz, A-Weighted		5.74	6.80	μV_{RMS}
V_{IN}	Maximum Input Signal f_{IN}=1kHz, THD+N < 10%, Level=0V			448	mV_{PP}

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8 V, V_{IN}=94 dB (SPL), and f_{CLK}=2.4 MHz. Duty Cycle=50% and C_{MIC}=15 pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Range		1.64	1.80	3.63	V
I_{DD}	Supply Current	INPUT=AC Coupled to GND, CLOCK=On, No Load		470		µA
I_{SLEEP}	Sleep Mode Current	f_{CLK}=GND		1.5	8.0	µA
PSR	Power Supply Rejection(3)	INPUT=AC Coupled to GND, Test Signal on V_{DD}=217 Hz Square Wave and Broadband Noise(2), Both 100mV_{P-P}		-74		dBFS
IN_{NOM}	Nominal Sensitivity(4)	INPUT=94 dBSPL (1Pa)		-26		dBFS
THD	Total Harmonic Distortion(6)	f_{IN}=1 kHz, INPUT=-26 dBFS		0.02	0.20	%
THD+N	THD and Noise(3)	50Hz ≤ f_{IN} ≤ 1 kHz, INPUT=-20 dBFS		0.2	1.0	%
		f_{IN}=1 kHz, INPUT=-5 dBFS		1.0	5.0	
		f_{IN}=1kHz, INPUT=0 dBFS		5.0	10.0	
C_{IN}	Input Capacitance(7)	INPUT		0.2		pF
R_{IN}	Input Resistance(7)	INPUT	>100			GΩ
V_{IL}	CLOCK & SELECT Input Logic LOW Level				0.3	V
V_{IH}	CLOCK & SELECT Input Logic HIGH Level		1.5		V_{DD}+0.3	V
V_{OL}	Data Output Logic LOW Level				0.35*V_{DD}	V
V_{OH}	Data Output Logic HIGH Level		0.65*V_{DD}			V
V_{OUT}	Acoustic Overload Point(7)	THD < 10%	120			dBSPL

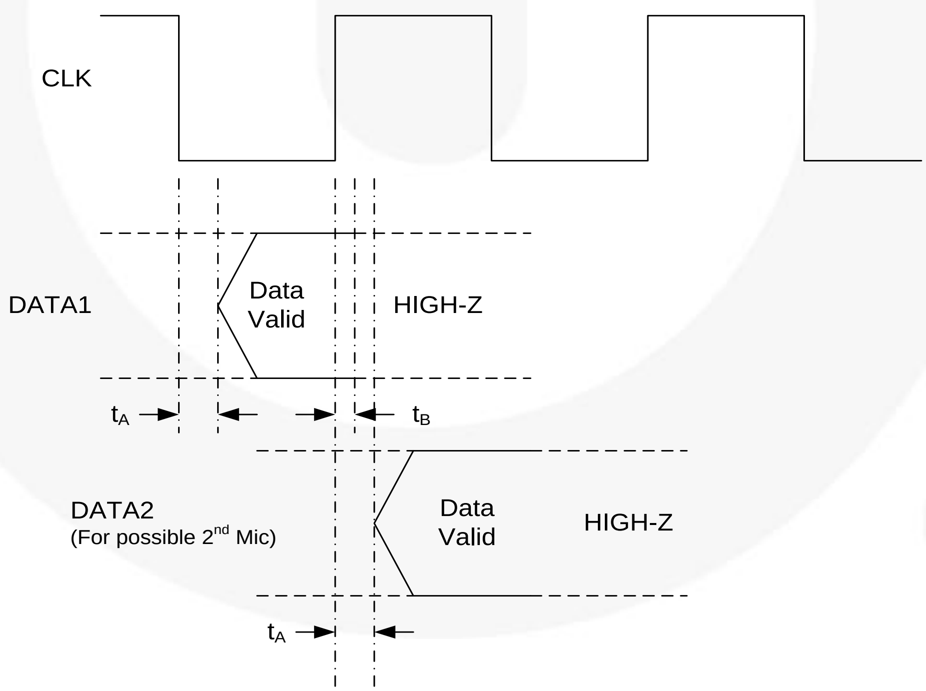
Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8 V, V_{IN}=94 dB(SPL), and f_{CLK}=2.4 MHz. Duty Cycle=50% and C_{MIC}=15 pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_A	Time from CLOCK Transition to Data becoming Valid	On Falling Edge of CLOCK, SELECT=GND, C_{LOAD}=15 pF	18	43		ns
t_B	Time from CLOCK Transition to Data becoming HIGH-Z	On Rising Edge of CLOCK, SELECT=GND, C_{LOAD}=15 pF	0	5	16	ns
t_A	Time from CLOCK Transition to Data becoming Valid	On Rising Edge of CLOCK, SELECT=V_{DD}, C_{LOAD}=15 pF	18	56		ns
t_B	Time from CLOCK Transition to Data becoming HIGH-Z	On Falling Edge of CLOCK, SELECT=V_{DD}, C_{LOAD}=15 pF	0	5	16	ns
f_{CLK}	Input CLOCK Frequency(8)	Active Mode	1.0	2.4	4.0	MHz
CLK_{dc}	CLOCK Duty Cycle(3)		40	50	60	%
t_{WAKEUP}	Wake-Up Time(9)	f_{CLK}=2.4MHz		0.35	2.00	ms
$t_{FALLASLEEP}$	Fall-Asleep Time(10)	f_{CLK}=2.4MHz	0	0.01	1.00	ms
C_{LOAD}	Load Capacitance on Data				100	pF

Notes:
2. Pseudo-random noise with triangular probability density function. Bandwidth up to 10 MHz.
3. Guaranteed by characterization.
4. Assuming that 120 dB(SPL) is mapped to 0 dBFS.
5. Assuming an input of -45 dBV.
6. Guaranteed by design.
7. All parameters are tested at 2.4 MHz. Frequency range guaranteed by characterization.
8. Device wakes up when $f_{CLK} \geq$ 300 kHz.
9. Device falls asleep when $f_{CLK} \leq$ 70 kHz.



t_A – Microphone delay from clock edge to data assertion.
t_B – Microphone delay from clock edge to high-impedance state.
$t_A > t_B$ to have interim HIGH-Z state in both signals.

Figure 3. Interface Timing

Typical Performance Characteristics

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8 V, V_{IN}=94 dB(SPL), f_{CLK}=2.4 MHz, and duty cycle=50%.

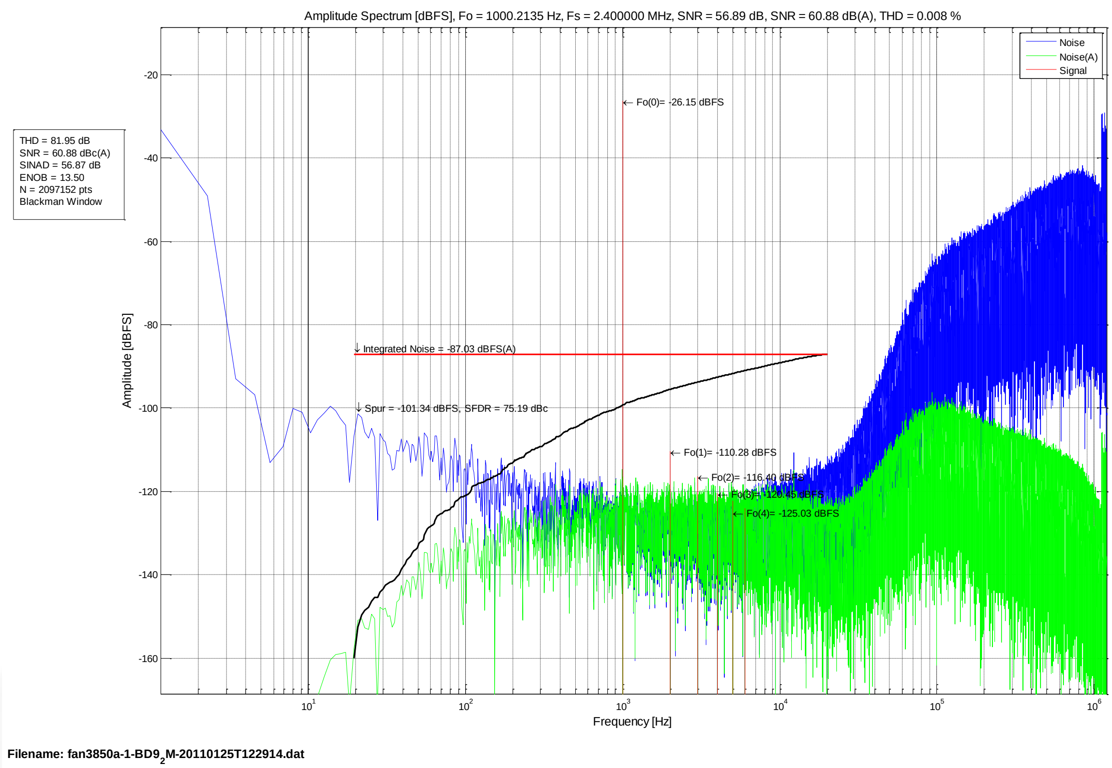


Figure 4. Noise vs. Frequency

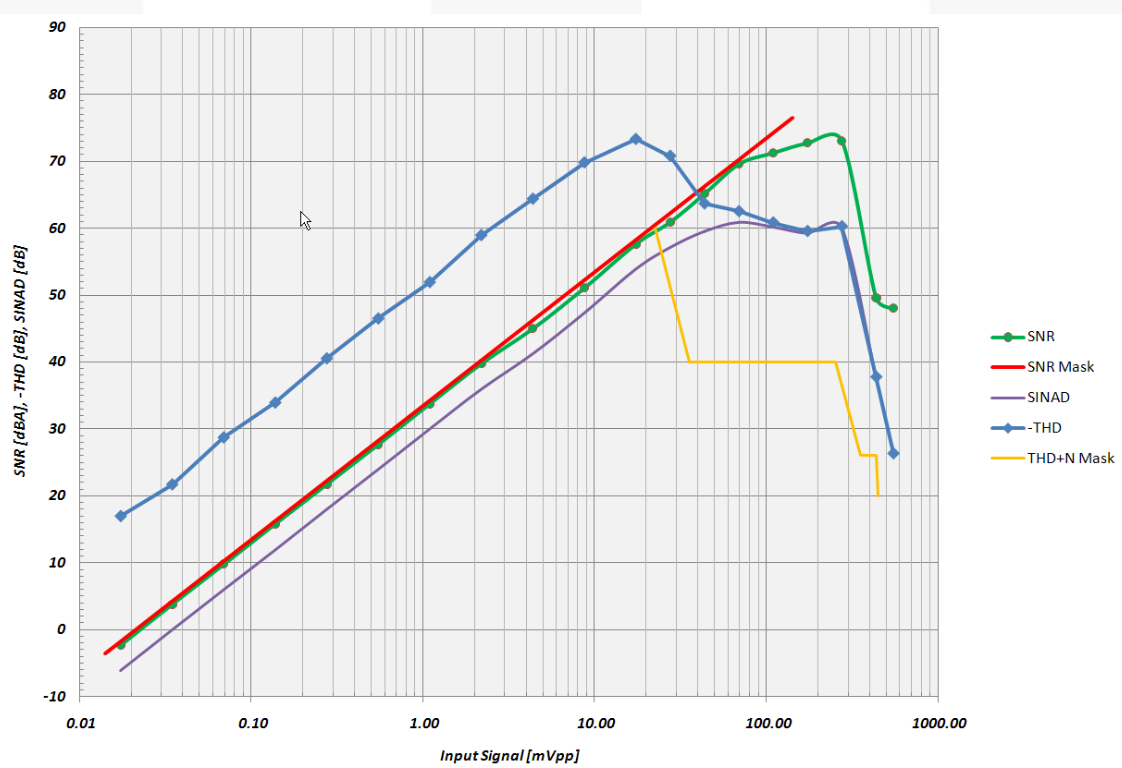


Figure 5. THD, SINDA, and SNR vs. Input Amplitude

Typical Performance Characteristics (Continued)

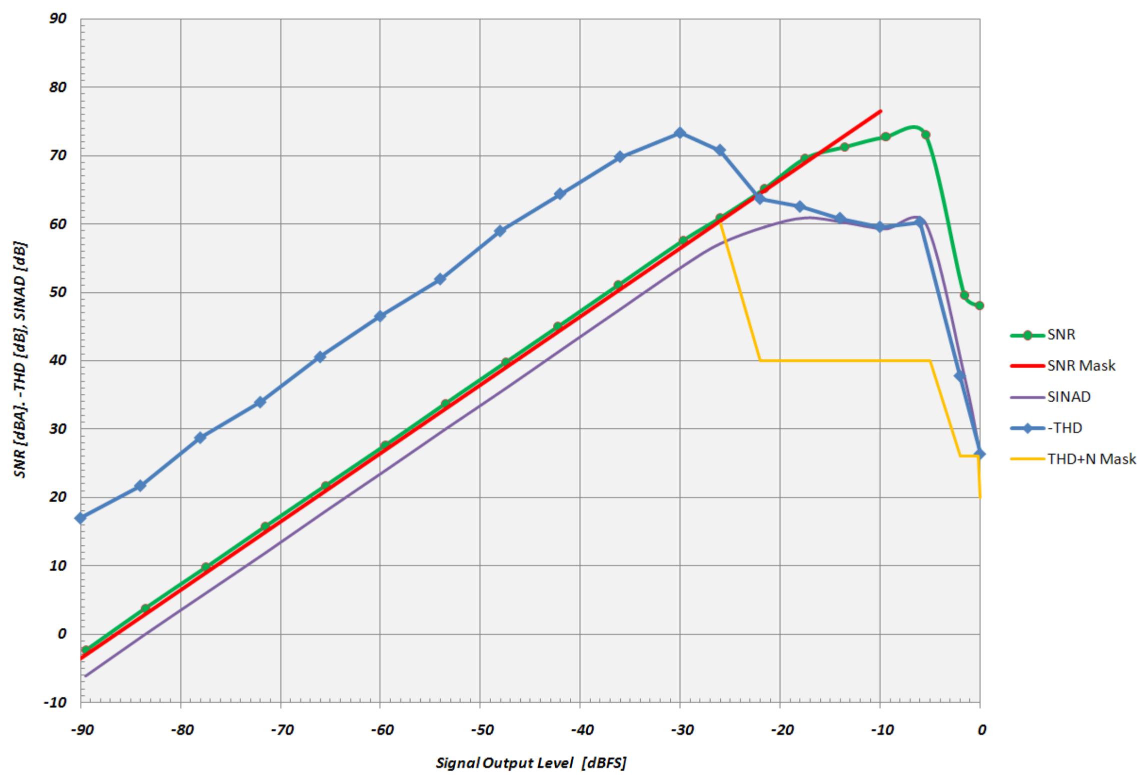


Figure 6. THD, SINAD, and SNR vs. Output Level

Temp (˚C)	Delta(dB)
-40	0.1971
-30	0.1644
-20	0.1260
-10	0.0954
0	0.0657
10	0.0359
20	0.0139
25	0.0000
30	-0.0097
40	-0.0344
50	-0.0514
60	-0.0739
70	-0.0998
80	-0.1183
85	-0.1271

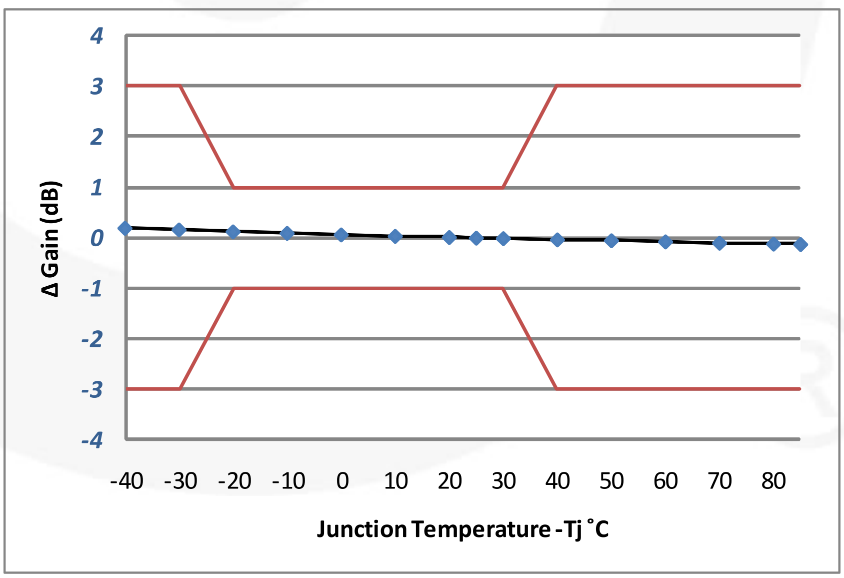


Figure 7. Δ Gain vs. Temperature (Nominal Temperature= 25°C)

Applications Information

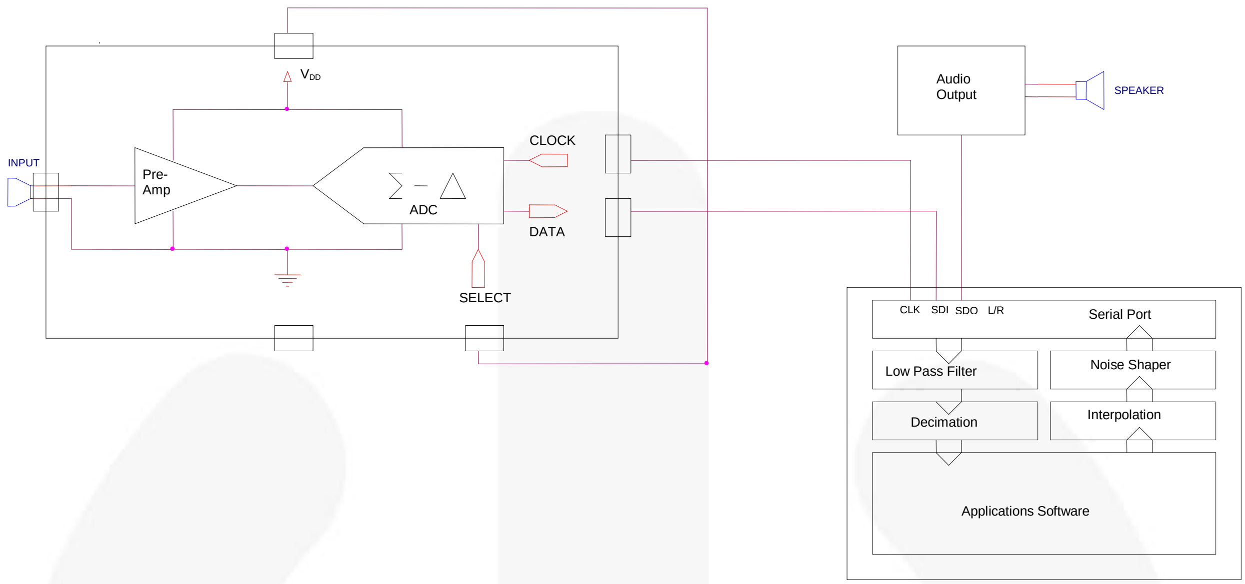


Figure 8. Mono Microphone Application Circuit

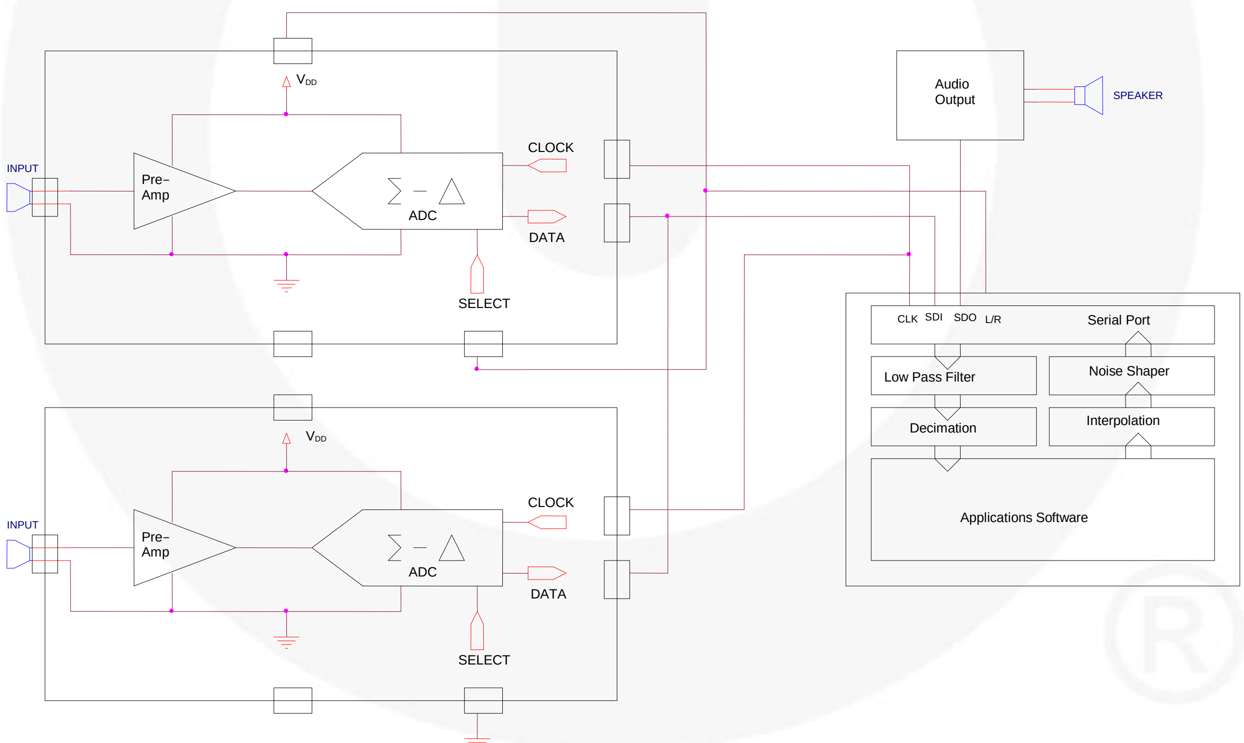


Figure 9. Stereo Microphone Application Circuit

Applications Information (Continued)

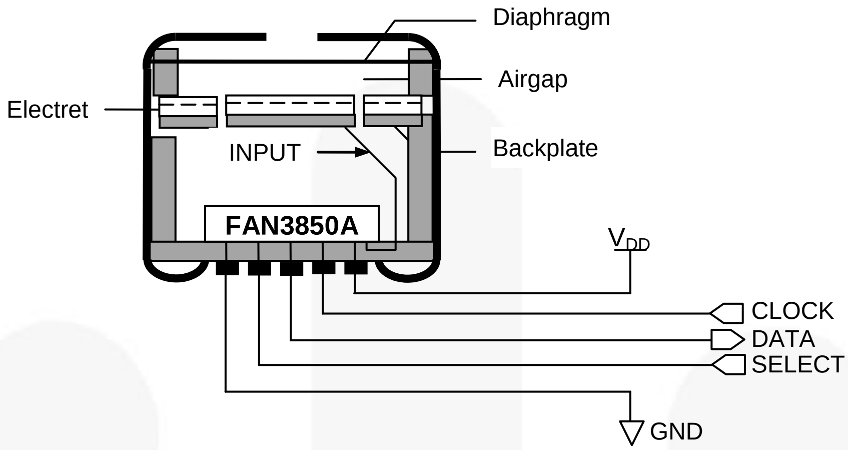


Figure 10. MIC Element Drawing

A 0.1 µF decoupling capacitor is required for V_{DD}. It can be located inside the microphone or on the PCB very close to the VDD pin.

Due to high input impedance, care should be taken to remove all flux used during the reflow soldering process.

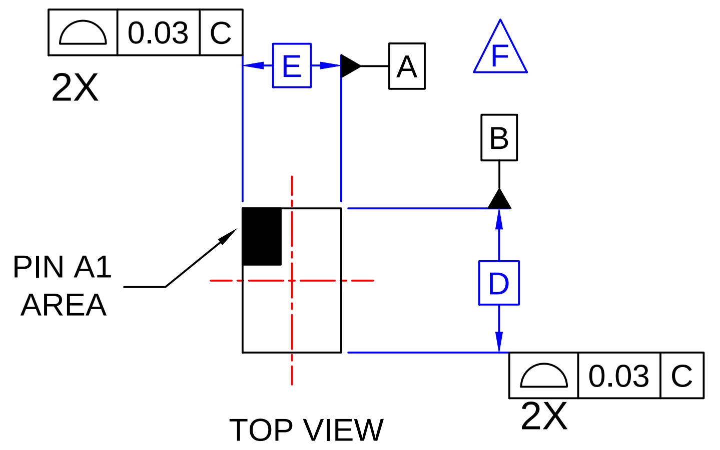
A 100 Ω resistance is recommended on the clock output of the device driving the FAN3850A to minimize ringing and improve signal integrity.

For optimal PSR, route a trace to the VDD pin. Do not place a VDD plane under the device.

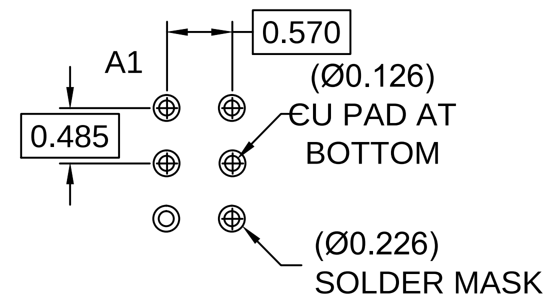
The table below pertains to the Marketing Outline drawing on the following page.

FAN3850A External Product Dimensions

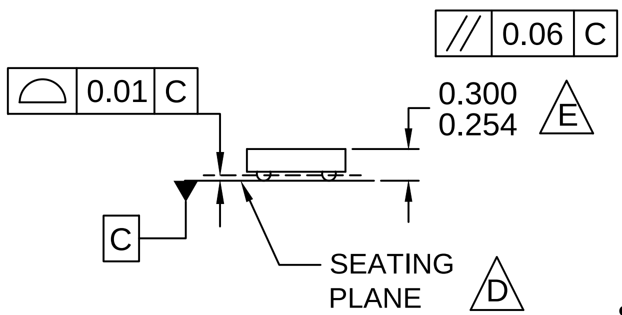
Product ID	D	E	X	Y
All options	1.260mm	0.860mm	0.145mm	0.145mm

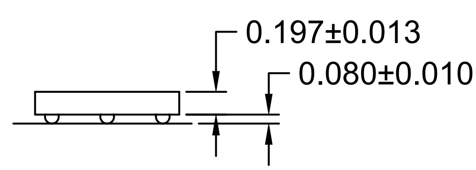


TOP VIEW

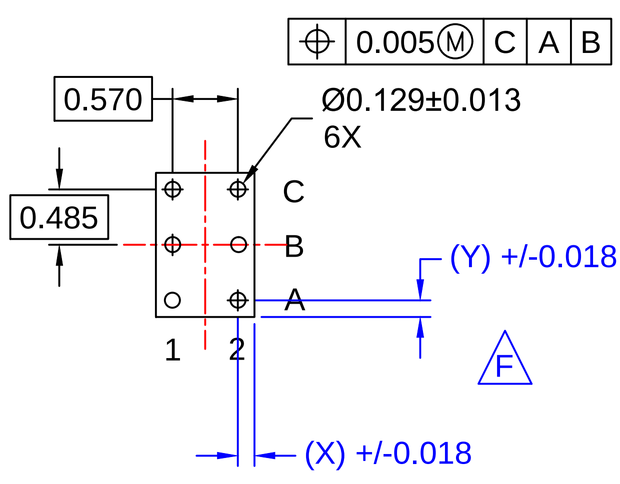


RECOMMENDED LAND
PATTERN (NSMD)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 273 MICRONS ±23 MICRONS (254-300 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: UC006AHrev4.

PUBLICATION ORDERING INFORMATION

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