

# BLA6G1011-200R; BLA6G1011L(S)-200RG

Power LDMOS transistor

Rev. 6 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

200 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

**Table 1. Test information**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$ .

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)	t <sub>r</sub> (ns)	t <sub>f</sub> (ns)
Typical RF performance in a class-AB production test circuit for SOT502A							
pulsed RF	1030 to 1090	28	200	20	65	10	6
Typical RF performance in a Gullwing application for SOT502C and SOT502D							
pulsed RF	1030 to 1090	28	200	20	65	15	6

### 1.2 Features and benefits

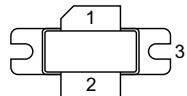
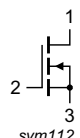
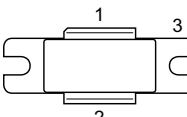
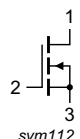
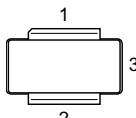
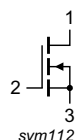
- Typical pulsed RF performance at frequencies from 1030 MHz to 1090 MHz, a supply voltage of 28 V and an  $I_{DQ}$  of 100 mA:
  - ◆ Output power = 200 W
  - ◆ Power gain = 20 dB
  - ◆ Efficiency = 65 %
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range.

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA6G1011-200R (SOT502A)			
1	drain		
2	gate		
3	source <sup>[1]</sup>		
BLA6G1011L-200RG (SOT502D)			
1	drain		
2	gate		
3	source <sup>[1]</sup>		
BLA6G1011LS-200RG (SOT502C)			
1	drain		
2	gate		
3	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA6G1011-200R	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA6G1011L-200RG	-	eared flanged ceramic package; 2 mounting holes; 2 leads	SOT502D
BLA6G1011LS-200RG	-	earless flanged ceramic package; 2 leads	SOT502C

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$I_D$	drain current		-	49	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Type	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 50\text{ }\mu\text{s}$ ; $\delta = 2\%$	BLA6G1011-200R	0.085	K/W
			BLA6G1011L-200RG	0.065	K/W
			BLA6G1011LS-200RG	0.065	K/W

## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 270\text{ mA}$	1.4	2.0	2.4	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$ ; $I_D = 1620\text{ mA}$	1.7	2.2	2.7	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$	-	-	4.2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	40	48	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	420	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 9.45\text{ A}$	11	18	26	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 9.45\text{ A}$	0.012	0.07	0.093	$\Omega$
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$ ; $f = 1\text{ MHz}$	-	3	-	pF

Table 7. RF characteristics

Test signal: Pulsed RF;  $t_p = 50\text{ }\mu\text{s}$ ;  $\delta = 2\%$ ;  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 100\text{ mA}$ ;  $T_{case} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified; in a class-AB production test circuit for straight leads.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_L$	output power		200	-	-	W
$G_p$	power gain	$P_L = 200\text{ W}$	18	20	-	dB
$RL_{in}$	input return loss	$P_L = 200\text{ W}$	-	-10	-8	dB
$\eta_D$	drain efficiency	$P_L = 200\text{ W}$	58	65	-	%
$t_r$	rise time	$P_L = 200\text{ W}$	-	10	20	ns
$t_f$	fall time	$P_L = 200\text{ W}$	-	6	20	ns

### 6.1 Ruggedness in class-AB operation

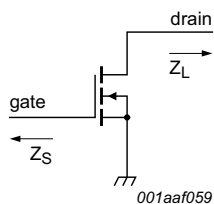
The BLA6G1011-200R, BLA6G1011L-200RG and BLA6G1011LS-200RG are enhanced rugged devices and are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:  $t_p = 50\text{ }\mu\text{s}$ ;  $\delta = 2\%$ ;  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 100\text{ mA}$ ;  $P_L = 200\text{ W}$ ;  $f = 1030\text{ MHz}$  to  $1090\text{ MHz}$ .

## 7. Application information

### 7.1 Impedance information

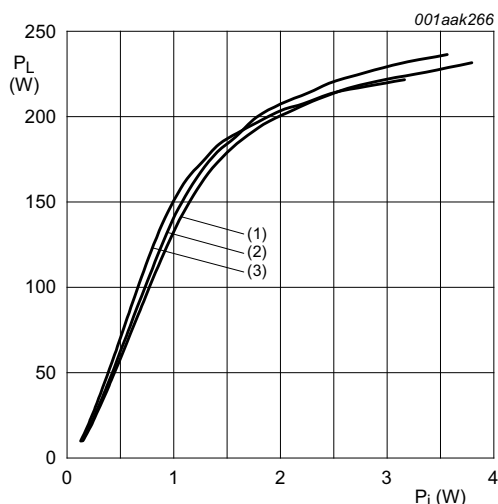
**Table 8. Typical impedance**  
Typical values unless otherwise specified.

<b>f</b>	<b>Z<sub>S</sub></b>	<b>Z<sub>L</sub></b>
<b>(MHz)</b>	<b>(Ω)</b>	<b>(Ω)</b>
<b>BLA6G1011-200R</b>		
1030	0.57 – j0.94	0.80 – j0.68
1060	0.70 – j1.13	0.84 – j0.52
1090	0.80 – j1.53	0.86 – j0.35
<b>BLA6G1011L-200RG and BLA6G1011LS-200RG</b>		
1030	0.69 – j2.18	0.84 – j0.59
1060	0.86 – j2.36	0.85 – j0.73
1090	1.12 – j2.54	0.86 – j0.87



**Fig 1. Definition of transistor impedance**

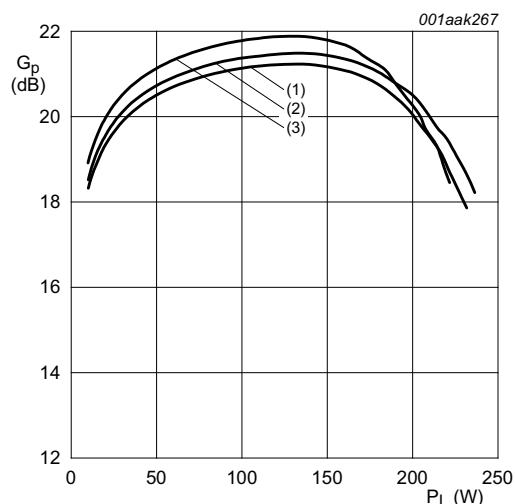
## 7.2 RF performance



$V_{DS} = 28 \text{ V}$ ;  $t_p = 50 \text{ } \mu\text{s}$ ;  $\delta = 2 \%$ ;  $I_{Dq} = 100 \text{ mA}$ .

- (1)  $f = 1030 \text{ MHz}$
- (2)  $f = 1060 \text{ MHz}$
- (3)  $f = 1090 \text{ MHz}$

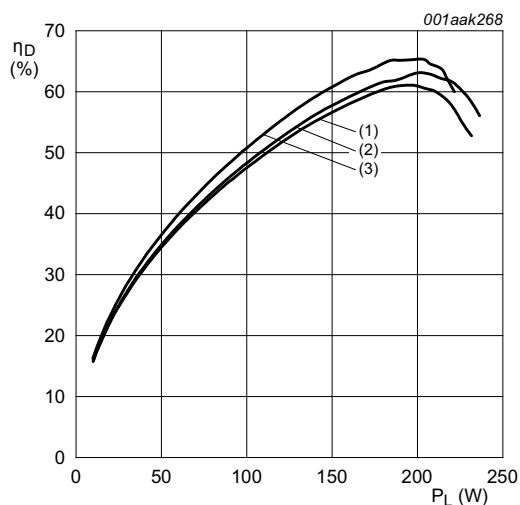
**Fig 2. Output power as a function of input power; typical values**



$V_{DS} = 28 \text{ V}$ ;  $t_p = 50 \text{ } \mu\text{s}$ ;  $\delta = 2 \%$ ;  $I_{Dq} = 100 \text{ mA}$ .

- (1)  $f = 1030 \text{ MHz}$
- (2)  $f = 1060 \text{ MHz}$
- (3)  $f = 1090 \text{ MHz}$

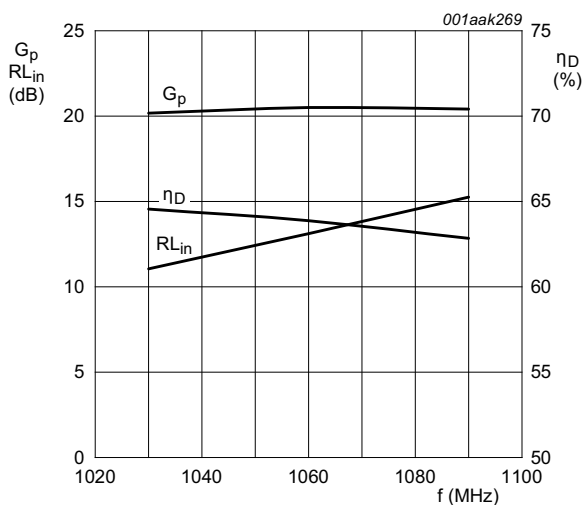
**Fig 3. Power gain as a function of output power; typical values**



$V_{DS} = 28 \text{ V}$ ;  $t_p = 50 \text{ } \mu\text{s}$ ;  $\delta = 2 \%$ ;  $I_{Dq} = 100 \text{ mA}$ .

- (1)  $f = 1030 \text{ MHz}$
- (2)  $f = 1060 \text{ MHz}$
- (3)  $f = 1090 \text{ MHz}$

**Fig 4. Drain efficiency as a function of output power; typical values**

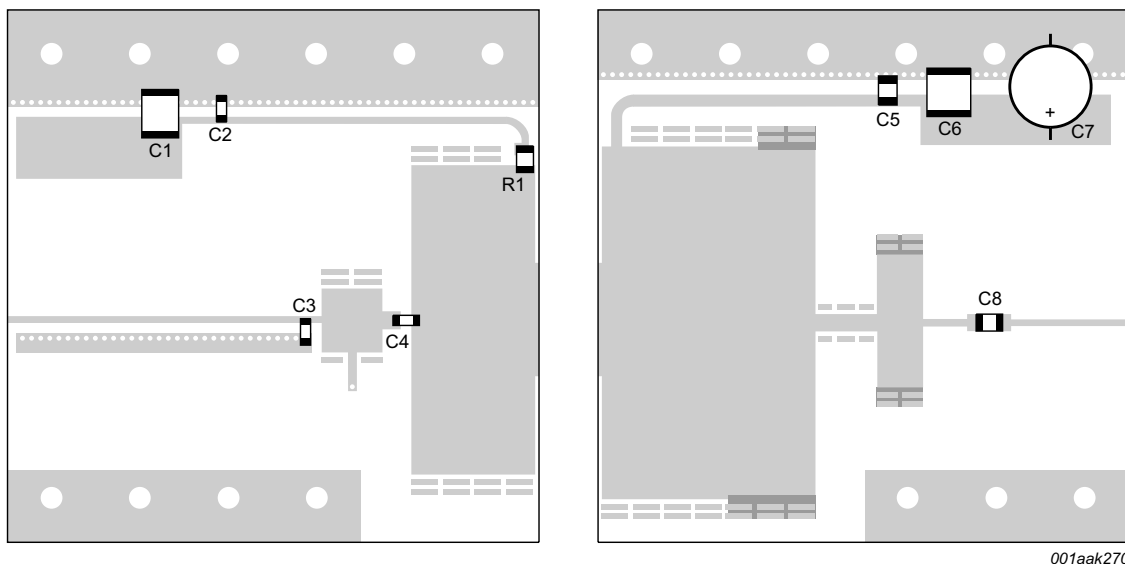


$P_L = 200 \text{ W}$ ;  $V_{DS} = 28 \text{ V}$ ;  $t_p = 50 \text{ } \mu\text{s}$ ;  $\delta = 2 \%$ ;  $I_{Dq} = 100 \text{ mA}$ .

**Fig 5. Power gain, input return loss and drain efficiency as function of frequency; typical values**

### 7.3 Application circuit

**Remark:** For BLA6G1011-200R with straight leads



See [Table 9](#) for list of components.

**Fig 6. Component layout for class-AB application circuit**

**Table 9. List of components**

See [Figure 6](#).

Striplines are on a Rogers Duroid 6006 Printed-Circuit Board (PCB);  $\epsilon_r = 6.15$  F/m; thickness = 0.64 mm

Component	Description	Value	Remarks
C1, C6	multilayer ceramic chip capacitor	10 $\mu$ F	TDK
C2	multilayer ceramic chip capacitor	68 pF <sup>[1]</sup>	
C3	multilayer ceramic chip capacitor	1.5 pF <sup>[1]</sup>	
C4	multilayer ceramic chip capacitor	3.9 pF <sup>[1]</sup>	
C5, C8	multilayer ceramic chip capacitor	30 pF <sup>[2]</sup>	
C7	electrolytic capacitor	470 $\mu$ F; 63 V	
R1	SMD resistor	12 $\Omega$	SMD 1206

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

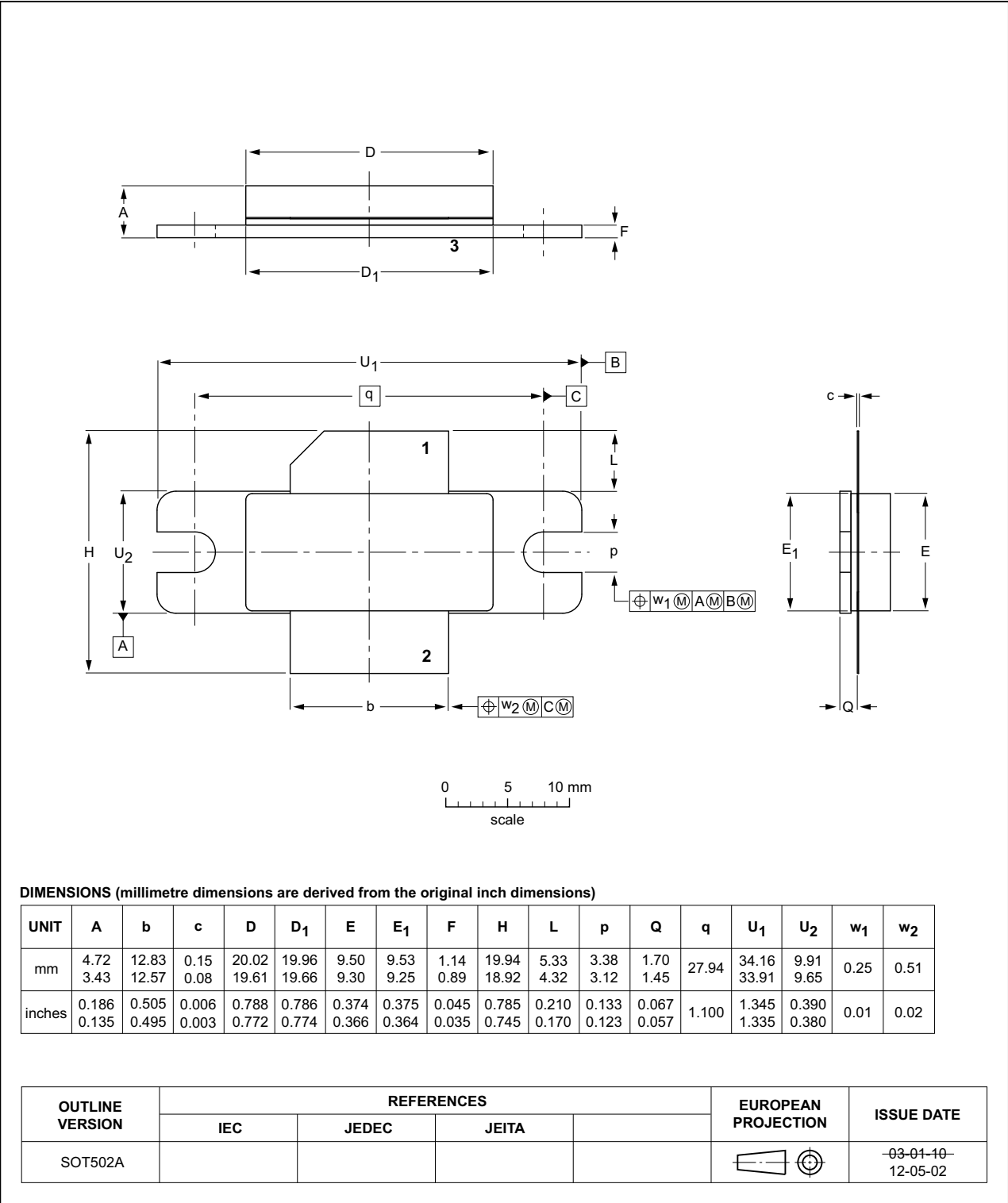
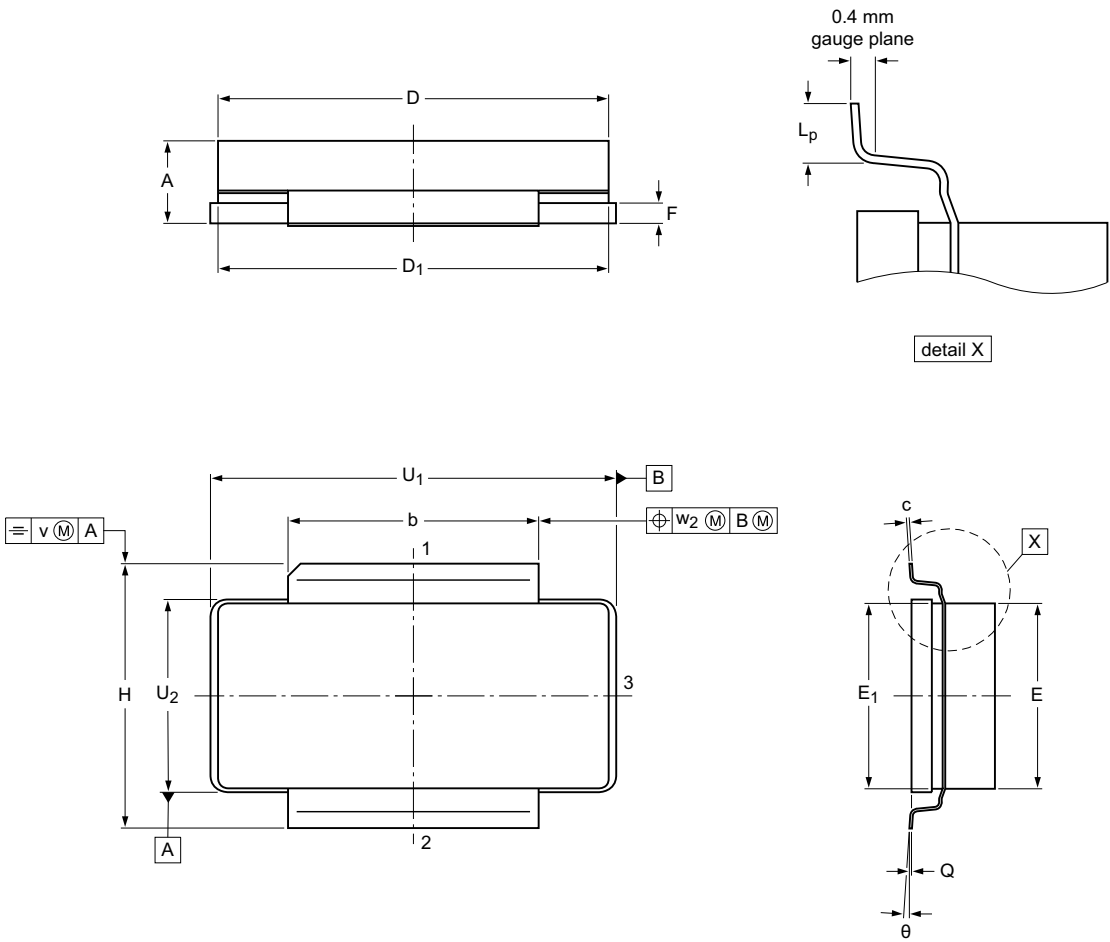


Fig 7. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502C



Dimensions

Unit <sup>(1)</sup>		A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L <sub>p</sub>	Q	U <sub>1</sub>	U <sub>2</sub>	v	w <sub>2</sub>	θ
mm	max	4.72	12.83	0.16	20.02	19.96	9.53	9.53	1.14	13.6	1.2	0.195	20.70	9.91	0.25	0.25	7°
	nom min	3.43	12.57	0.10	19.61	19.66	9.27	9.27	0.89	13.2	0.8	0.055	20.45	9.65			0°
inches	max	0.185	0.505	0.006	0.788	0.786	0.375	0.375	0.045	0.536	0.048	0.008	0.815	0.39	0.01	0.01	7°
	nom min	0.135	0.495	0.004	0.772	0.774	0.365	0.365	0.035	0.519	0.031	0.002	0.805	0.38			0°

Note  
1. Millimeter dimensions are derived from the original inch dimensions.

sot502c\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502C						11-05-02 12-05-02

Fig 8. Package outline SOT502C

Eared flanged ceramic package; 2 leads; 2 mounting holes

SOT502D

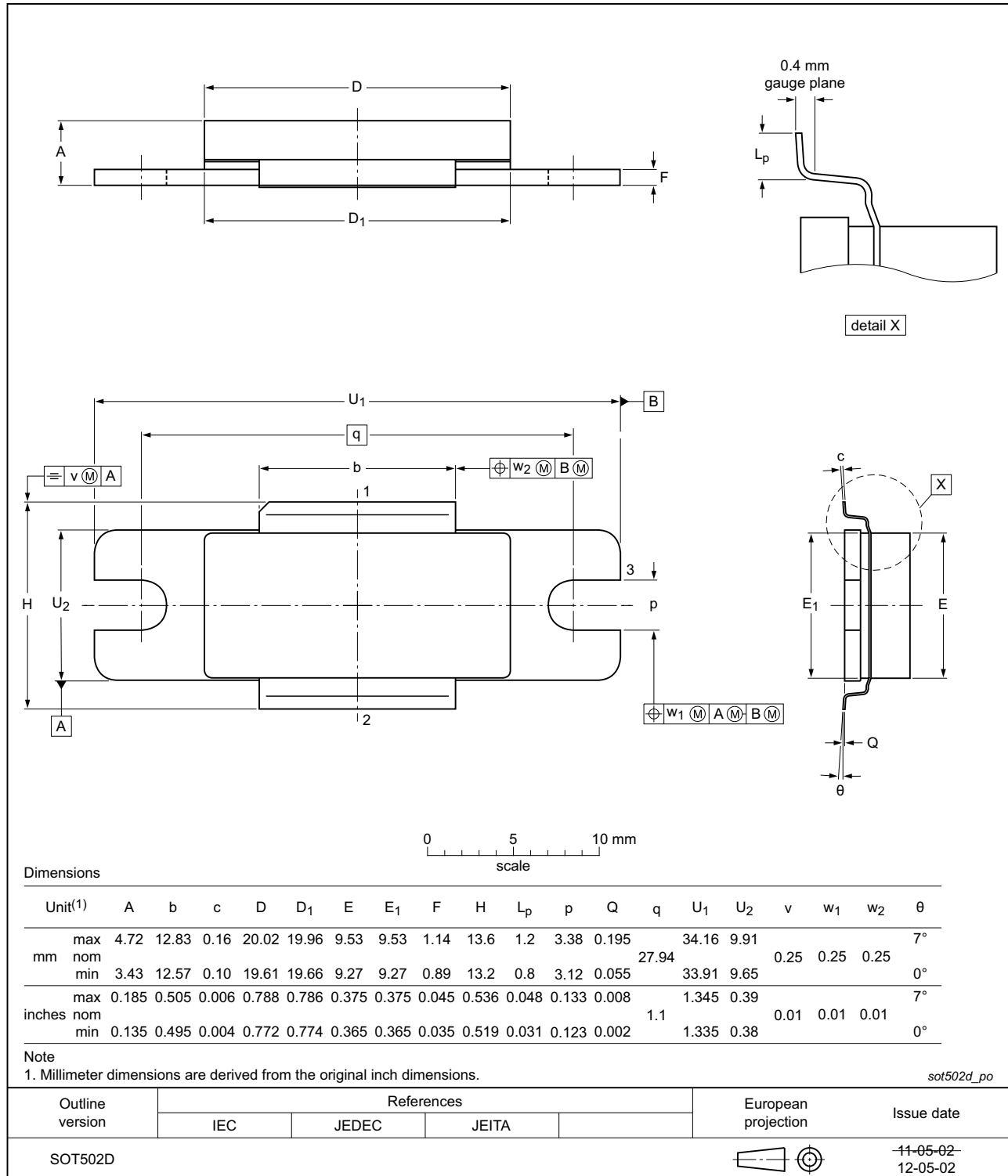


Fig 9. Package outline SOT502D

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA6G1011-200R_L-200RG_LS-200RG#6	20150901	Product data sheet		BLA6G1011-200R v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLA6G1011-200R_L-200RG_LS-200RG v.5	20150317	Product data sheet		BLA6G1011-200R v.4
BLA6G1011-200R_L-200RG_LS-200RG v.4	20111109	Product data sheet		BLA6G1011-200R v.3
BLA6G1011-200R v.3	20100714	Product data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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