

**16 Gb, 4-Bit ECC, x8 I/O, and 1.8 V V_{CC}
NAND Flash for Embedded****Distinctive Characteristics**

- Density
 - 16 Gb (4 Gb × 4)
- Architecture (For each 4 Gb device)
 - Input / Output Bus Width: 8-bits
 - Page Size: (2048 + 128) bytes; 128-byte spare area
 - Block Size: 64 Pages or (128k + 8k) bytes
 - Plane Size
 - 2048 Blocks per Plane or (256M + 16M) bytes
 - Device Size
 - 2 Planes per Device or 512 Mbyte
- NAND Flash Interface
 - Open NAND Flash Interface (ONFI) 1.0 compliant
 - Address, Data and Commands multiplexed
- Supply Voltage
 - 1.8V device: $V_{CC} = 1.7V \sim 1.95V$
- Security
 - One Time Programmable (OTP) area
 - Serial number (unique ID)
 - Hardware program/erase disabled during power transition
- Additional Features
 - Supports Multiplane Program and Erase commands
 - Supports Copy Back Program
 - Supports Multiplane Copy Back Program
 - Supports Read Cache
- Electronic Signature
 - Manufacturer ID: 01h
- Operating Temperature
 - Industrial: $-40^{\circ}C$ to $85^{\circ}C$

Performance

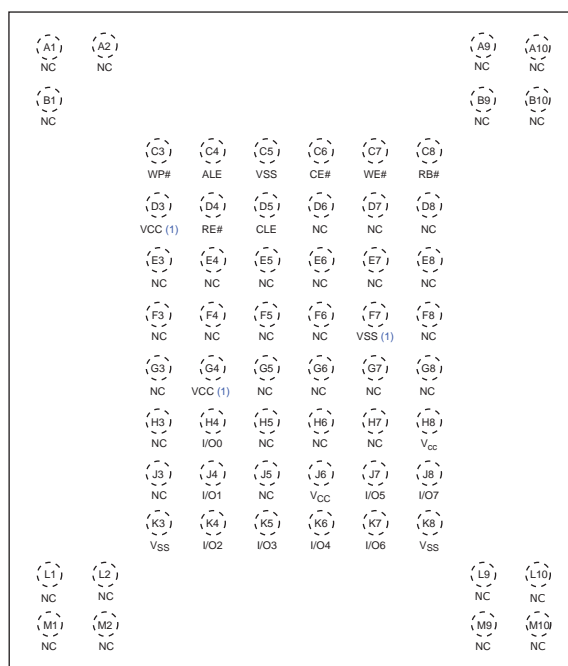
- Page Read / Program
 - Random access: 30 μs (Max)
 - Sequential access: 45 ns (Min)
 - Program time / Multiplane Program time: 300 μs (Typ)
- Block Erase / Multiplane Erase
 - Block Erase time: 3.5 ms (Typ)
- Reliability
 - 100,000 Program / Erase cycles (Typ) (with 4-bit ECC per 528 bytes)
 - 10 Year Data retention (Typ)
 - Blocks zero and one are valid and will be valid for at least 1000 program-erase cycles with ECC
- Package Options
 - Lead Free and Low Halogen
 - 63-Ball BGA $9 \times 11 \times 1.2$ mm

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The Cypress® S34MS16G2 16-Gb NAND is offered in 1.8V V_{CC} with x8 I/O interface. This document contains information for the S34MS16G2 device, which is a quad-die stack of four S34MS04G2 die. For detailed specifications, please refer to the discrete die data sheet: [S34MS01G2 04G2](#).

Figure 2.1 63-BGA Contact, x8 Device (Balls Down, Top View)



3. Pin Description

Table 3.1 Pin Description

| Pin Name | Description |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O0 - I/O7 | Inputs/Outputs. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled. |
| CLE | Command Latch Enable. This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#). |
| ALE | Address Latch Enable. This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#). |
| CE# | Chip Enable. This input controls the selection of the device. When the device is not busy CE# low selects the memory. |
| WE# | Write Enable. This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#. |
| RE# | Read Enable. The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one. |
| WP# | Write Protect. The WP# pin, when low, provides hardware protection against undesired data modification (program / erase). |
| R/B# | Ready Busy. The Ready/Busy output is an Open Drain pin that signals the state of the memory. |
| V _{CC} | Supply Voltage. The V _{CC} supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when V _{CC} is less than V _{LKO} . |
| V _{SS} | Ground. |
| NC | Not Connected. |

Notes:

1. A 0.1 μ F capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever V_{CC} is below 1.8V to protect the device from any involuntary program/erase during power transitions.

4. Block Diagrams

Figure 4.1 Functional Block Diagram

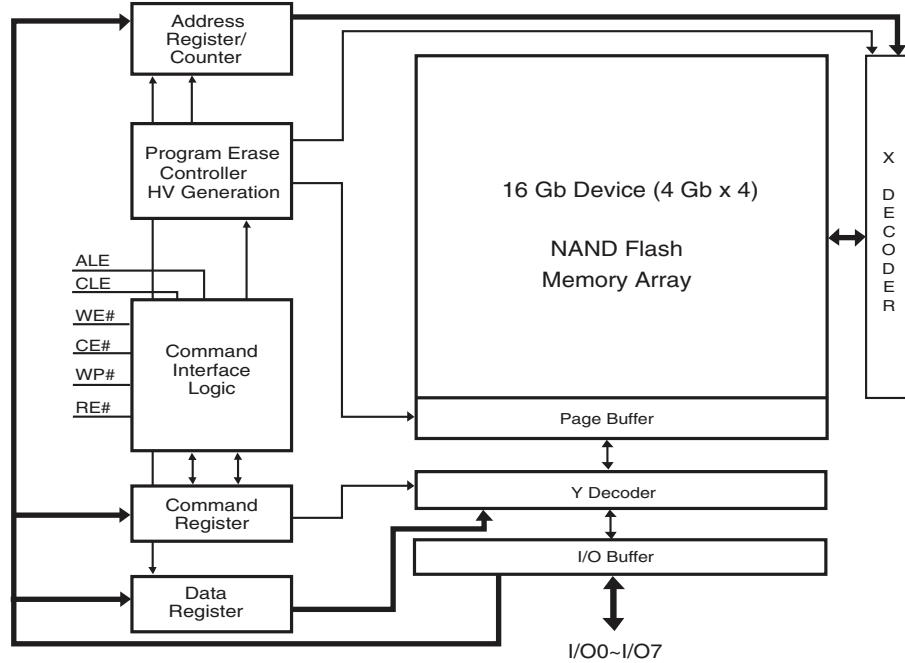
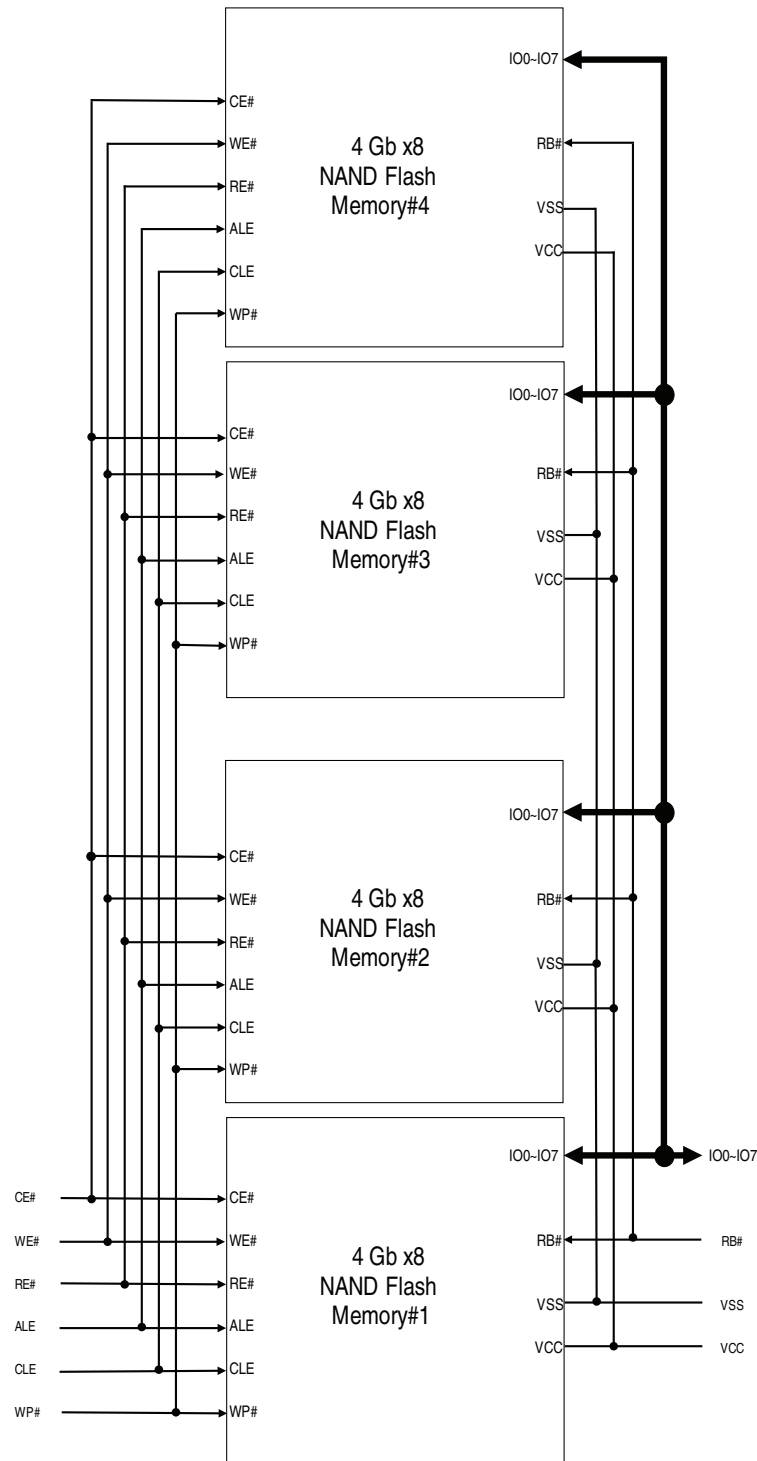


Figure 4.2 Block Diagram — 16 Gb (4 Gb x 4) 63-Ball BGA with 1 CE# (One Chip Enable Signal)



5. Addressing

Table 5.1 Address Cycle Map

| Bus Cycle | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 |
|----------------------|-----------|------------|------------|------------|-----------|-----------|------------|-----------|
| 1st / Col. Add. 1 | A0 (CA0) | A1 (CA1) | A2 (CA2) | A3 (CA3) | A4 (CA4) | A5 (CA5) | A6 (CA6) | A7 (CA7) |
| 2nd / Col. Add. 2 | A8 (CA8) | A9 (CA9) | A10 (CA10) | A11 (CA11) | Low | Low | Low | Low |
| 3rd / Row Add. 1 | A12 (PA0) | A13 (PA1) | A14 (PA2) | A15 (PA3) | A16 (PA4) | A17 (PA5) | A18 (PLA0) | A19 (BA0) |
| 4th / Row Add. 2 | A20 (BA1) | A21 (BA2) | A22 (BA3) | A23 (BA4) | A24 (BA5) | A25 (BA6) | A26 (BA7) | A27 (BA8) |
| 5th / Row Add. 3 (6) | A28 (BA9) | A29 (BA10) | A30 (BA11) | A31 (BA12) | Low | Low | Low | Low |

Notes:

1. CAx = Column Address bit.
2. PAx = Page Address bit.
3. PLA0 = Plane Address bit zero.
4. BAx = Block Address bit.
5. Block address concatenated with page address and plane address = actual page address, also known as the row address.
6. A31 for 16 Gb (4 Gb x 4 – QDP).

For the address bits, the following rules apply:

- A0–A11: column address in the page
- A12–A17: page address in the block
- A18: plane address (for multiplane operations) / block address (for normal operations)
- A19–A31: block address

6. Read Status Enhanced

Read Status Enhanced is used to retrieve the status value for a previous operation in the following cases:

- In the case of concurrent operations on a multi-die stack.

When four dies are stacked to form a quad-die package (QDP), it is possible to run one operation on the first die, then activate a different operation on the second die, for example: Erase while Read, Read while Program, etc.

- In the case of multiplane operations in the same die.

7. Read ID

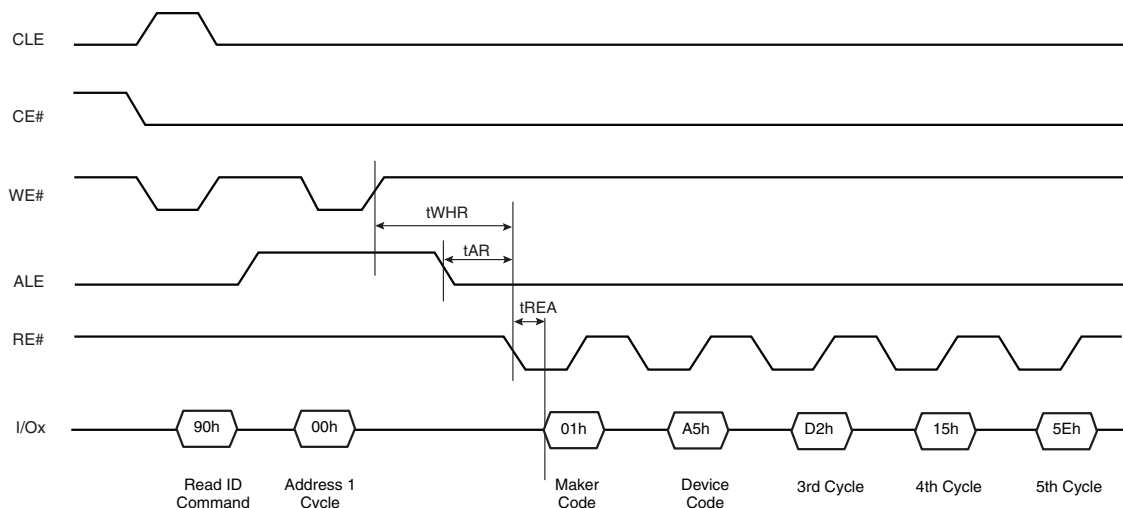
The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

Note: If you want to execute Read Status command (0x70) after Read ID sequence, you should input dummy command (0x00) before Read Status command (0x70).

For the S34MS16G2 device, five read cycles sequentially output the manufacturer code (01h), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it.

Table 7.1 Read ID for Supported Configurations

| Density | Org | V _{CC} | 1st | 2nd | 3rd | 4th | 5th |
|-------------------------------------|-----|-----------------|-----|-----|-----|-----|-----|
| 4 Gb | x8 | 1.8V | 01h | ACh | 90h | 15h | 56h |
| 16 Gb (4 Gb x 4 – QDP with one CE#) | x8 | 1.8V | 01h | A5h | D2h | 15h | 5Eh |

Figure 7.1 Read ID Operation Timing


5th ID Data

Table 7.2 Read ID Byte 5 Description

| | Description | I/O7 | I/O6 I/O5 I/O4 | I/O3 I/O2 | I/O1 I/O0 |
|------------------------------------|-------------------|------|----------------|-----------|-----------|
| ECC Level | 1 bit / 512 bytes | | | | 0 0 |
| | 2 bit / 512 bytes | | | | 0 1 |
| | 4 bit / 512 bytes | | | | 1 0 |
| | 8 bit / 512 bytes | | | | 1 1 |
| Plane Number | 1 | | | 0 0 | |
| | 2 | | | 0 1 | |
| | 4 | | | 1 0 | |
| | 8 | | | 1 1 | |
| Plane Size (without spare area) | 64 Mb | | 0 0 0 | | |
| | 128 Mb | | 0 0 1 | | |
| | 256 Mb | | 0 1 0 | | |
| | 512 Mb | | 0 1 1 | | |
| | 1 Gb | | 1 0 0 | | |
| | 2 Gb | | 1 0 1 | | |
| | 4 Gb | | 1 1 0 | | |
| Reserved | | 0 | | | |

7.1 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the command register, followed by an address input of 00h. The command register remains in Parameter Page mode until further commands are issued to it. [Table 7.3](#) explains the parameter fields.

Note: For 32nm Cypress NAND, for a particular condition, the Read Parameter Page command does not give the correct values. To overcome this issue, the host must issue a Reset command before the Read Parameter Page command. Issuance of Reset before the Read Parameter Page command will provide the correct values and will not output 00h values.

Table 7.3 Parameter Page Description

| Byte | O/M | Description | Values |
|------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| Revision Information and Features Block | | | |
| 0-3 | M | Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I" | 4Fh, 4Eh, 46h, 49h |
| 4-5 | M | Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0) | 02h, 00h |
| 6-7 | M | Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width | 1Eh, 00h |
| 8-9 | M | Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command | 3Bh, 00h |
| 10-31 | | Reserved (0) | 00h |
| Manufacturer Information Block | | | |
| 32-43 | M | Device manufacturer (12 ASCII characters) | 53h, 50h, 41h, 4Eh, 53h, 49h, 4Fh, 4Eh, 20h, 20h, 20h, 20h |
| 44-63 | M | Device model (20 ASCII characters) | 53h, 33h, 34h, 4Dh, 53h, 31h, 36h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| 64 | M | JEDEC manufacturer ID | 01h |
| 65-66 | O | Date code | 00h |
| 67-79 | | Reserved (0) | 00h |
| Memory Organization Block | | | |
| 80-83 | M | Number of data bytes per page | 00h, 08h, 00h, 00h |
| 84-85 | M | Number of spare bytes per page | 80h, 00h |
| 86-89 | M | Number of data bytes per partial page | 00h, 00h, 00h, 00h |
| 90-91 | M | Number of spare bytes per partial page | 00h, 00h |

Table 7.3 Parameter Page Description (Continued)

| Byte | O/M | Description | Values |
|------------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|
| 92-95 | M | Number of pages per block | 40h, 00h, 00h, 00h |
| 96-99 | M | Number of blocks per logical unit (LUN) | 00h, 40h, 00h, 00h (1 CE#) |
| 100 | M | Number of logical units (LUNs) | 01h (1 CE#) |
| 101 | M | Number of address cycles 4-7 Column address cycles 0-3 Row address cycles | 23h |
| 102 | M | Number of bits per cell | 01h |
| 103-104 | M | Bad blocks maximum per LUN | 47h, 01h (1 CE#) |
| 105-106 | M | Block endurance | 01h, 05h |
| 107 | M | Guaranteed valid blocks at beginning of target | 01h |
| 108-109 | M | Block endurance for guaranteed valid blocks | 01h, 03h |
| 110 | M | Number of programs per page | 04h |
| 111 | M | Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints | 00h |
| 112 | M | Number of bits ECC correctability | 04h |
| 113 | M | Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits | 01h |
| 114 | O | Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support | 04h |
| 115-127 | | Reserved (0) | 00h |
| Electrical Parameters Block | | | |
| 128 | M | I/O pin capacitance | 0Ah |
| 129-130 | M | Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1 | 03h, 00h |
| 131-132 | O | Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0 | 03h, 00h |
| 133-134 | M | t _{PROG} Maximum page program time (μs) | BCh, 02h |

Table 7.3 Parameter Page Description (Continued)

| Byte | O/M | Description | Values |
|----------------------------------|-----|--------------------------------------------------------|-----------------------------|
| 135-136 | M | t _{BERS} Maximum block erase time (μs) | 10h, 27h |
| 137-138 | M | t _R Maximum page read time (μs) | 1Eh, 00h |
| 139-140 | M | t _{CCS} Minimum Change Column setup time (ns) | C8h, 00h |
| 141-163 | | Reserved (0) | 00h |
| Vendor Block | | | |
| 164-165 | M | Vendor specific Revision number | 00h |
| 166-253 | | Vendor specific | 00h |
| 254-255 | M | Integrity CRC | 11h, F5h (1CE#) |
| Redundant Parameter Pages | | | |
| 256-511 | M | Value of bytes 0-255 | Repeat Value of bytes 0-255 |
| 512-767 | M | Value of bytes 0-255 | Repeat Value of bytes 0-255 |
| 768+ | O | Additional redundant parameter pages | FFh |

Note:

1. "O" Stands for Optional, "M" for Mandatory.

8. Electrical Characteristics

8.1 Valid Blocks

Table 8.1 Valid Blocks

| Device | Symbol | Min | Typ | Max | Unit |
|-----------|----------|-----------|-----|-------|--------|
| S34MS04G2 | N_{VB} | 4016 | — | 4096 | Blocks |
| S34MS16G2 | N_{VB} | 16057 (1) | — | 16384 | Blocks |

Note:

1. Each 4 Gb can have a maximum 80 bad blocks.

8.2 DC Characteristics

Table 8.2 DC Characteristics and Operating Conditions

(Values listed are for each 4 Gb NAND, 16 Gb (4 Gb x 4) will differ accordingly)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Units |
|-----------------------------------|-----------------|-----------------|--------------------------------------------------------------------------------|---------------------|-----|---------------------|---------------|
| Power On Current | | I_{CC0} | FFh command input after power on | — | — | 50 per device | mA |
| Operating Current | Sequential Read | I_{CC1} | $t_{RC} = t_{RC}(\text{min})$ $CE\# = V_{IL}$, $I_{out} = 0 \text{ mA}$ | — | 15 | 30 | mA |
| | Program | I_{CC2} | Normal | — | 15 | 30 | mA |
| | | | Cache | — | 15 | 30 | mA |
| | Erase | I_{CC3} | — | — | 15 | 30 | mA |
| Standby Current, (TTL) | | I_{CC4} | $CE\# = V_{IH}$, $WP\# = 0V/V_{CC}$ | — | — | 1 | mA |
| Standby Current, (CMOS) | | I_{CC5} | $CE\# = V_{CC}-0.2$, $WP\# = 0/V_{CC}$ | — | 10 | 50 | μA |
| Input Leakage Current | | I_{LI} | $V_{IN} = 0 \text{ to } V_{CC}(\text{max})$ | — | — | ± 10 | μA |
| Output Leakage Current | | I_{LO} | $V_{OUT} = 0 \text{ to } V_{CC}(\text{max})$ | — | — | ± 10 | μA |
| Input High Voltage | | V_{IH} | — | $V_{CC} \times 0.8$ | — | $V_{CC} + 0.3$ | V |
| Input Low Voltage | | V_{IL} | — | -0.3 | — | $V_{CC} \times 0.2$ | V |
| Output High Voltage | | V_{OH} | $I_{OH} = -100 \mu\text{A}$ | $V_{CC} - 0.1$ | — | — | V |
| Output Low Voltage | | V_{OL} | $I_{OL} = 100 \mu\text{A}$ | — | — | 0.1 | V |
| Output Low Current (R/B#) | | $I_{OL(R/B\#)}$ | $V_{OL} = 0.1\text{V}$ | 3 | 4 | — | mA |
| Erase and Program Lockout Voltage | | V_{LKO} | — | — | 1.1 | — | V |

Notes:

1. All V_{CC} pins, and V_{SS} pins respectively, are shorted together.
2. Values listed in this table refer to the complete voltage range for V_{CC} and to a single device in case of device stacking.
3. All current measurements are performed with a 0.1 μF capacitor connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin.
4. Standby current measurement can be performed after the device has completed the initialization process at power up.

8.3 Pin Capacitance

Table 8.3 Pin Capacitance (TA = 25°C, f=1.0 MHz)

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|----------------|-----------------|----------------------|-----|-----|------|
| Input | C _{IN} | V _{IN} = 0V | — | 10 | pF |
| Input / Output | C _{IO} | V _{IL} = 0V | — | 10 | pF |

Note:

1. For the stacked devices version the Input is 10 pF x [number of stacked chips] and the Input/Output is 10 pF x [number of stacked chips].

8.4 Power Consumptions and Pin Capacitance for Allowed Stacking Configurations

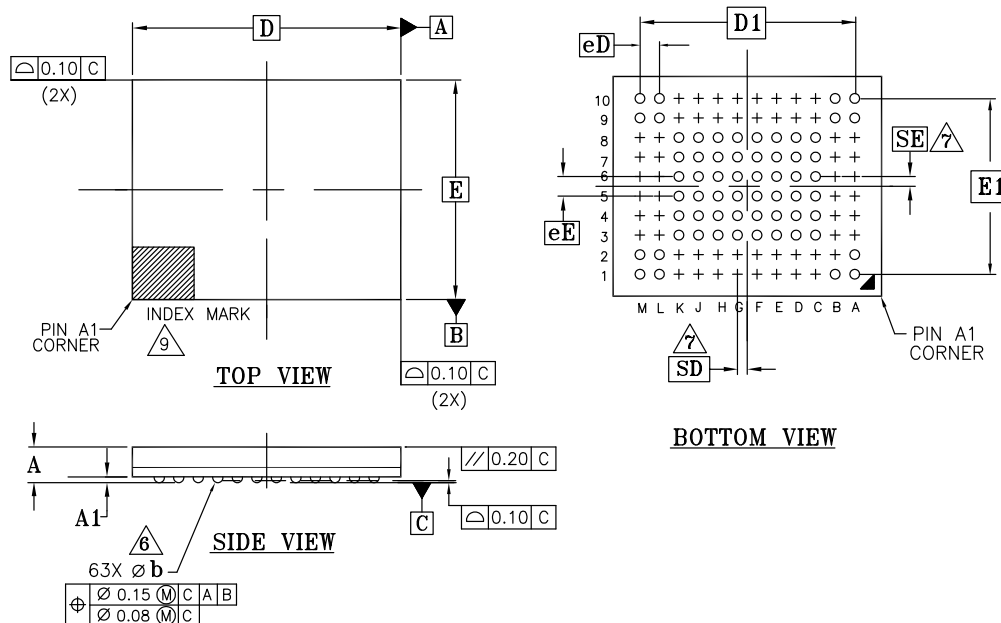
When multiple dies are stacked in the same package, the power consumption of the stack will increase according to the number of chips. As an example, the standby current is the sum of the standby currents of all the chips, while the active power consumption depends on the number of chips concurrently executing different operations.

When multiple dies are stacked in the same package the pin/ball capacitance for the single input and the single input/output of the combo package must be calculated based on the number of chips sharing that input or that pin/ball.

9. Physical Interface

9.1 63-Ball BGA Package

Figure 9.1 63-Ball BGA 9 x 11 x 1.2 mm



NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP 95, SECTION 3, SPP-020.
- eE** REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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10. Ordering Information

The ordering part number is formed by a valid combination of the following:

| S34MS | 16G | 2 | 02 | B | H | I | 00 | 0 | |
|-------|-----|---|----|---|---|---|----|---|----------------------------------------------|
| | | | | | | | | | Packing Type |
| | | | | | | | | | 0 = Tray |
| | | | | | | | | | 3 = 13" Tape and Reel |
| | | | | | | | | | Model Number |
| | | | | | | | | | 00 = Standard Interface / ONFI (x8) |
| | | | | | | | | | 20 = Two Chip Enable with Standard ONFI (x8) |
| | | | | | | | | | Temperature Range |
| | | | | | | | | | I = Industrial (–40°C to + 85°C) |
| | | | | | | | | | Materials Set |
| | | | | | | | | | F = Lead (Pb)-free |
| | | | | | | | | | H = Lead (Pb)-free and Low Halogen |
| | | | | | | | | | Package |
| | | | | | | | | | B = BGA |
| | | | | | | | | | T = TSOP |
| | | | | | | | | | Bus Width |
| | | | | | | | | | 00 = x8 NAND, single die |
| | | | | | | | | | 04 = x16 NAND, single die |
| | | | | | | | | | 01 = x8 NAND, dual die |
| | | | | | | | | | 02 = x8 NAND, quad die |
| | | | | | | | | | 05 = x16 NAND, dual die |
| | | | | | | | | | Technology |
| | | | | | | | | | 2 = Cypress NAND Revision 2 (32 nm) |
| | | | | | | | | | Density |
| | | | | | | | | | 01G = 1 Gb |
| | | | | | | | | | 02G = 2 Gb |
| | | | | | | | | | 04G = 4 Gb |
| | | | | | | | | | 08G = 8 Gb |
| | | | | | | | | | 16G = 16 Gb |
| | | | | | | | | | Device Family |
| | | | | | | | | | S34MS |
| | | | | | | | | | Cypress SLC NAND Flash Memory for Embedded |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Valid Combinations | | | | | | | | |
|--------------------|---------|------------|-----------|--------------|-------------------|-----------------------------|--------------|---------------------|
| Device Family | Density | Technology | Bus Width | Package Type | Temperature Range | Additional Ordering Options | Packing Type | Package Description |
| S34MS | 16G | 2 | 02 | BH | I | BH – 00 | 0, 3 | BGA |

11. Revision History

Document History Page

| Document Title: S34MS16G2, 16 Gb, 4-Bit ECC, x8 I/O, and 1.8V V _{CC} NAND Flash for Embedded Document Number: 002-00464 | | | | |
|-------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | — | XILA | 12/12/2014 | Initial release |
| *A | — | XILA | 04/24/2015 | Performance: Corrected Package Options for 63-Ball BGA to 9 x 11 x 1.2 mm Physical Interface: Corrected figure title to '63-Ball BGA 9 x 11 x 1.2 mm' Ordering Information: Ordering Information table: corrected Model Number and Materials Set |
| *B | 4962771 | XILA | 10/14/2015 | Updated to Cypress template. |
| *C | 5244672 | XILA | 04/28/2016 | Changed status from Advance to Final. Updated Read ID : Updated Read Parameter Page : Updated description. Updated to new template. |
| *D | 5497766 | XILA | 10/27/2016 | Updated Table 8.2 . Updated Notes 1 and 2 in DC Characteristics . Updated Copyright and Disclaimer. |
| *E | 5962114 | AESATMP8 | 11/09/2017 | Updated logo and Copyright. |

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