SC2672
Dual Synchronous Voltage Mode Controller

Description

The SC2672 is a versatile 2 phase, synchronous, voltage mode PWM controller that may be used in two distinct ways. First, the SC2672 is ideal for dual voltage independent applications. Alternatively, the SC2672 will generate a dual tracking voltage for DDR memories.. The SC2672 features a temperature compensated voltage reference, an undervoltage lockout over current protection and internal level-shifted, high-side drive circuitry.

In dual switcher configuration, two feedback paths are provided for independent control of the separate outputs. The device will provide a regulated output from flexibly configured inputs (3.3V, 5V, 12V), provided 5V is present for V_{CC}. The two switchers are 180° out of phase to minimize input and output ripple.

For DDR applications, the second channel uses the output of the first one as a reference for better tracking of the second channel voltage.

Features

- 300kHz operating frequency
- Soft Start
- Power Good output provided
- Undervoltage current limit
- Phase-shifted switchers minimize ripple
- High efficiency operation, >90%
- Programmable output(s) as low as .9V
- Industrial temperature range
- SOIC-16 pin package
- Bias voltage as low as 4.5V

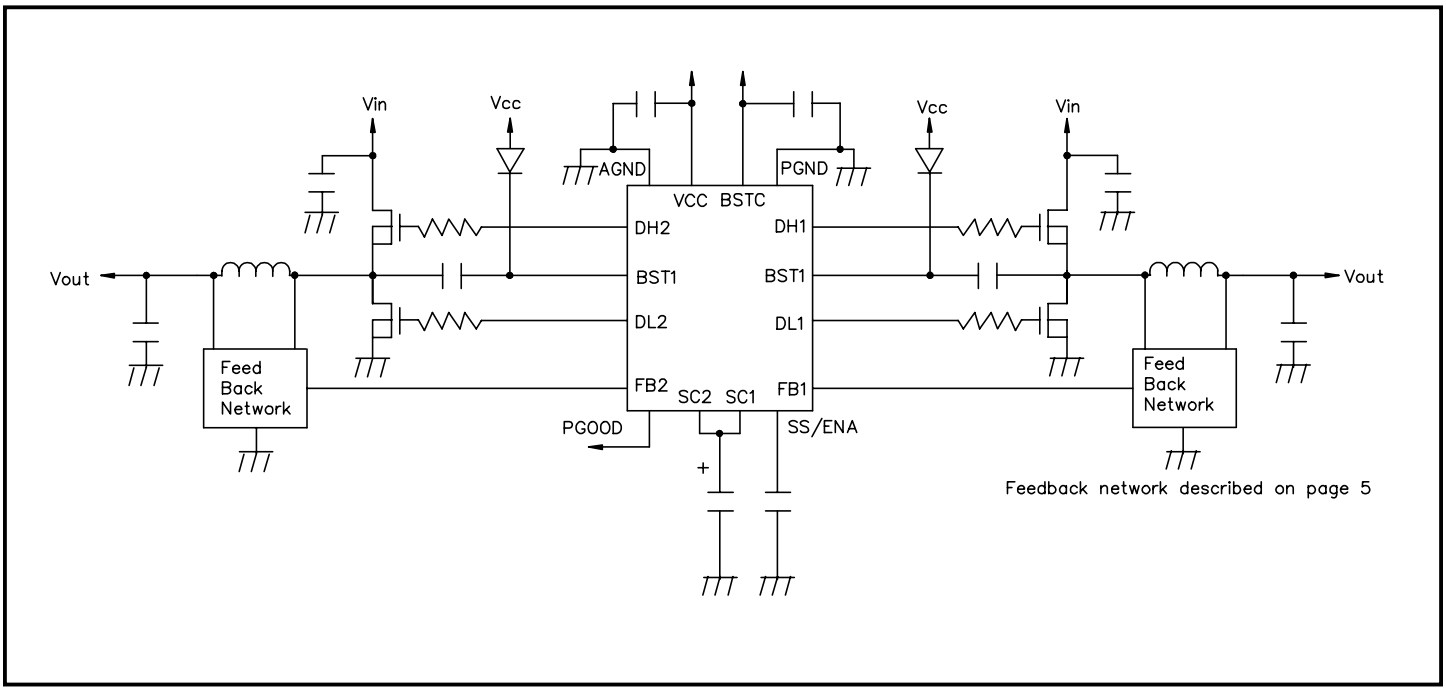
Two Independent PWM Controllers

- Flexible, same or separate V_{IN}
- Independent control for each channel
- Independent and separate output UVLO
- 2 phases operating opposed for ripple reduction (if same V_{IN} used)

Applications

- Graphics cards
- DDR Memory
- Peripheral add-in card
- SSTL Termination
- Power supplies requiring two outputs

Typical Application Schematic



Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Limits	Units
V_{CC} to GND	V_{IN}	-0.3 to 15	V
PGND to GND		± 1	V
BST to GND		-0.3 to 26	V
Thermal Resistance Junction to Case	θ_{JC}	40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	120	°C/W
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature Range	T_J	0 to 125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, 0mV < (CS(+) - (CS(-)) < 60mV , T_J = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	I_O = 2A(1), V_{OUT} set to 2.75V	2.65	2.75	2.85	V
Supply Voltage	V_{CC}	3		15	V
Supply Current	V_{CC} = 5.0		10		mA
Reference		.89	.9	.91	V
Load Regulation	I_O = 0.3A to 15A (1)		1		%
Reference Line Regulation	5V < V_{CC} < 15V			.5	%
Output Line Regulation	5V < V_{IN} < 15V			.5	%
Gain (A_{OL})	V_{OSENSE} to V_O		35		dB
Short Circuit Protection	Output undervoltage lockout		70		%
Oscillator Frequency		285	300	315	kHz
Oscillator Max Duty Cycle		90	95		%
DH Sink Current	DH - PGND = 2.5V	1.7			A
DH Sink Current	DH - PGND = 1.75V	.85			A
DH Source Current	BSTH - DH = 3V	1.7			A
DH Source Current	BSTH - DH = 2.5V	.85			A

Electrical Characteristics (Cont.)

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, 0mV < (CS(+) - (CS(-)) < 60mV , T_J = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DL Sink Current	DL - PGNG = 2.5V	1.7			A
DL Sink Current	DL - PGND = 1.75V	.85			A
DL Source Current	BSTL - DL = 3V	1.7			A
DL Source Current	BSTL - DL = 2.5V	.85			A
Dead Time		30	50		ns
Soft Start Charge Current (2)			25		µA
Soft Start Enable	0% duty cycle		1		V
Soft Start End	100% duty cycle		1.5		V
Soft Start Transition(2)	Synchronous mode		2		V
Output Undervoltage Lockout	Both channels		66%		V_{OUT}
Input Bias Current	-IN1, -IN2			1	µA

NOTES:

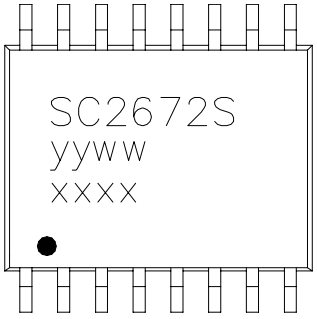
(1) Specification refers to application circuit.

(2) The soft start pin sources 25µA to an external capacitor. The converter operates in synchronous mode above the soft start transition threshold and in asynchronous mode below it.

(3) Power good is an open collector pulled low when the output voltage is under 75%.

Marking Information

(SOIC-16)

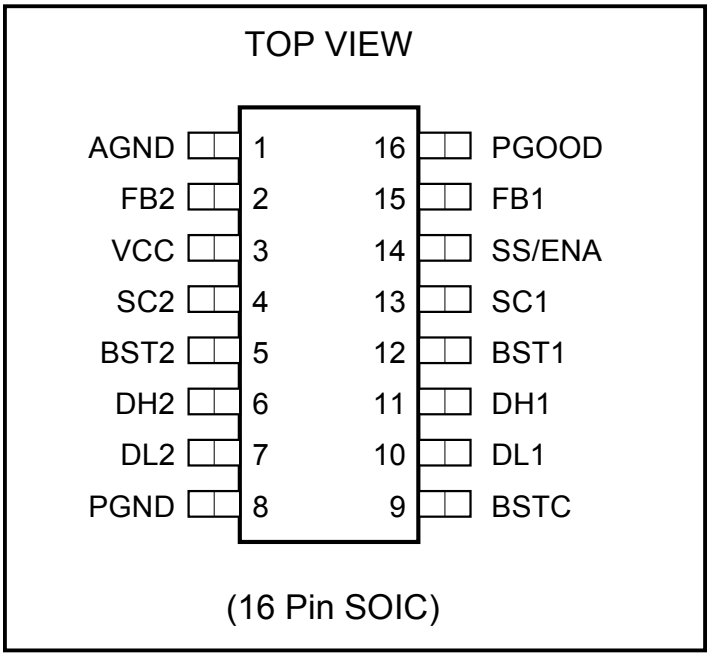


TOP

yyww = Datecode (Example: 9908)

xxxx = Semtech Lot # (Example: 90101)

Pin Configuration



Ordering Information

Device(1)	Package
SC2672STR	SOIC-16

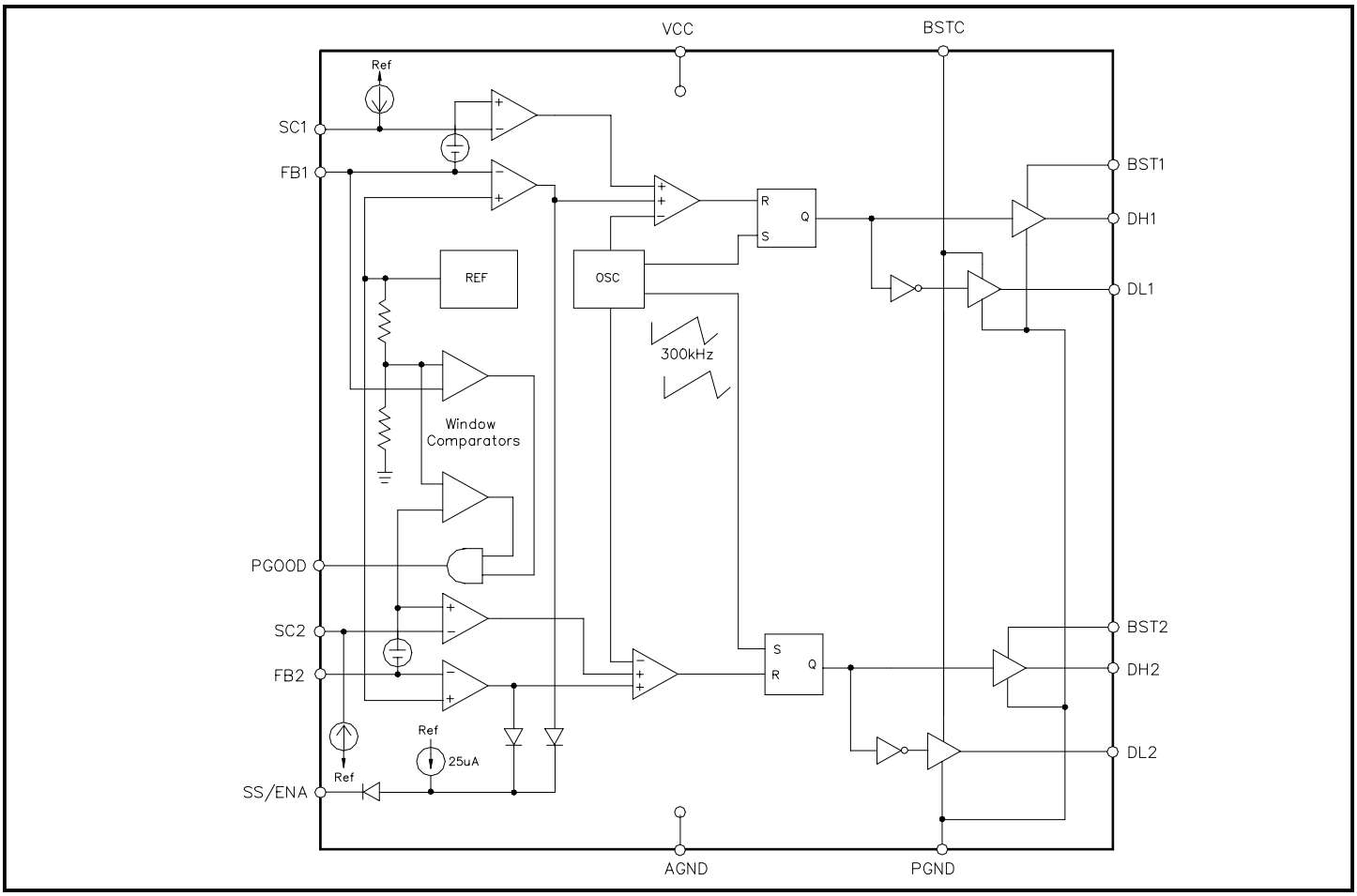
Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

EXPANDED PIN DESCRIPTION

Pin 1: (AGND)
Analog GND.
Return of analog signals and bias of chip
Pin 3: (VCC)
Bias for chip 3V to 15V.
Pin 2, 15: (FB2, FB1)
"-" inputs of error amplifiers.
Pin 4, 13: (SC2, SC1)
Output UVLO programmation.
Pin 5, 12: (BST2, BST1)
BST signal. Supply for high side driver.
Can be connected to a high enough voltage source.
Usually connected to bootstrap circuit.
Pin 6, 11: (DH2, DH1)
DH signal (Drive High).
Gate drive for top MOSFETs.
Requires a small serie resistor.
Pin 7, 10: (DL2, DL1)
DL signal (Drive Low).
Gate drive for bottom MOSFETs.
Requires a small serie resistor.
Pin 8: (PGND)
Power GND. Return of gate drive currents.
Pin 9: (BSTC)
Supply for bottom MOSFETs gate drive.
Pin 14: (SS/ENA)
Soft start pin. Internal current source connected to external capacitor.
Inhibits he chip if pulled down.
Pin 16: (PGOOD)
Power good signal.
Open collector signal .
Turns to 0 if output voltage is outside the power good window.

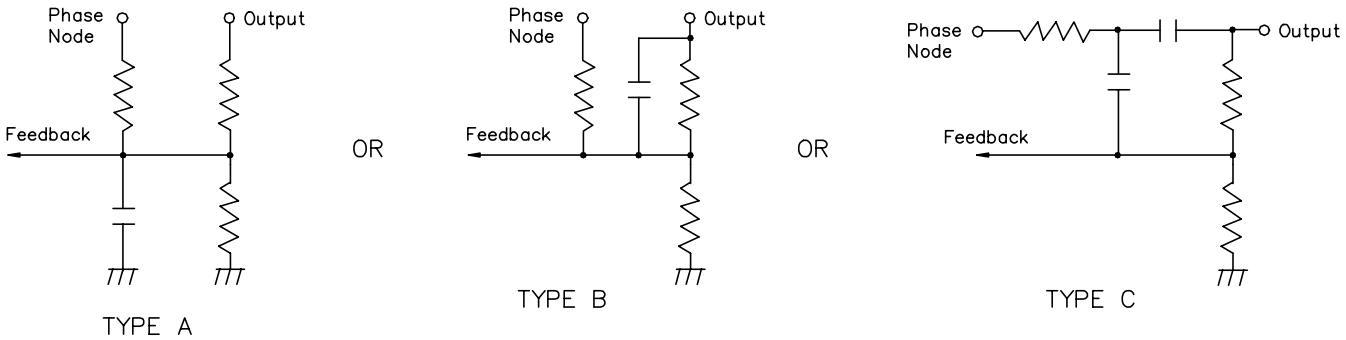
Block Diagram



Feedback Network

For simple applications with electrolytic output capacitors, the feedback network can be a simple divider from output to feedback pin without phase node injection.

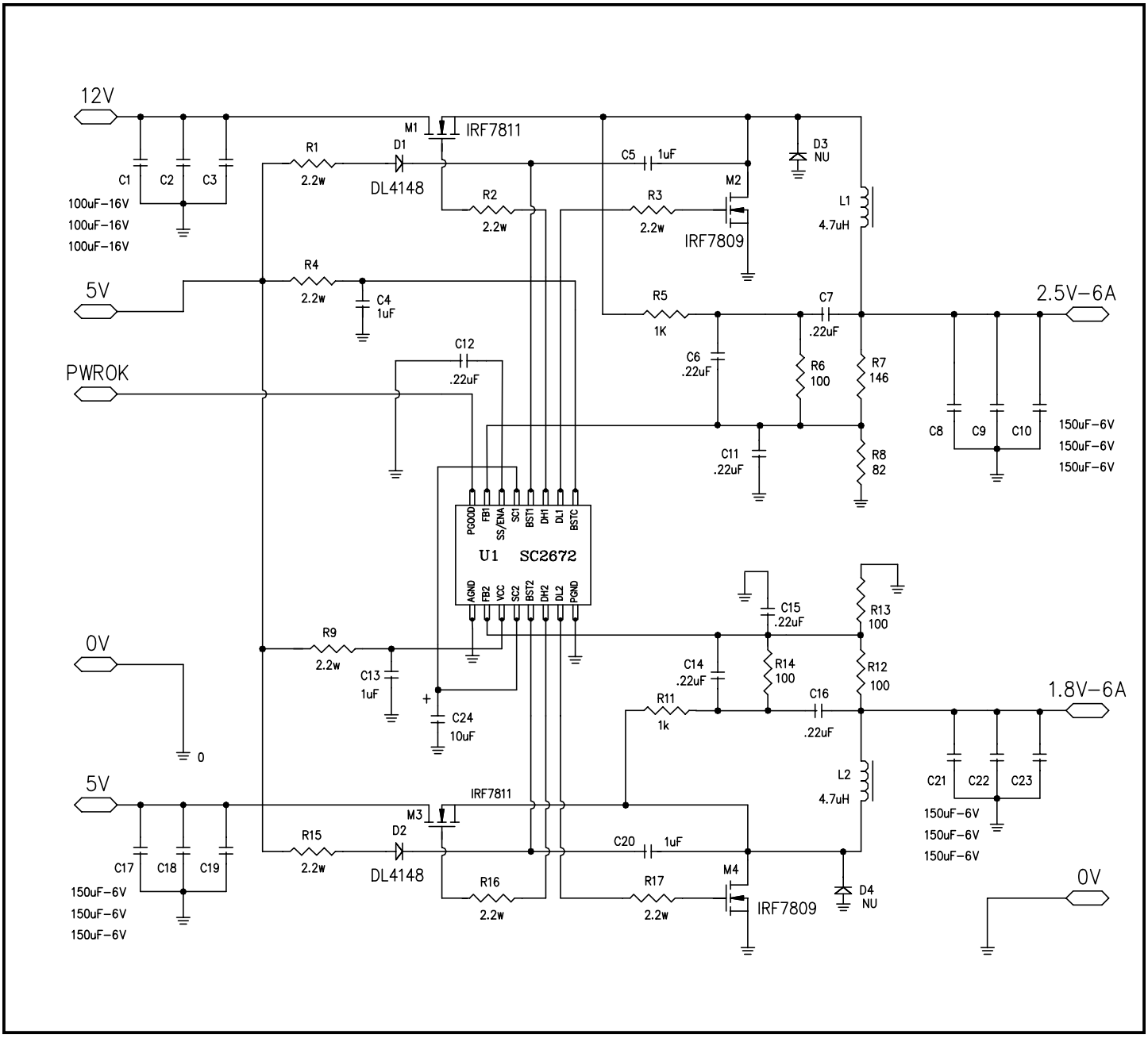
For ceramic output capacitors and/or droop control, the network can be:



The phase injection improves stability and can provide droop response.

Evaluation Board Schematic

Two Independent Channels



Main Loop(s)

The SC2672 is a dual, voltage mode synchronous Buck controller, the two separate channels are identical and share only IC supply pins (Vcc and GND), output driver ground (PGND) and pre-driver supply voltage (BSTC).

They also share a common oscillator generating a sawtooth waveform for channel 1 and an dephased sawtooth for channel 2. Channel 2 has both inputs of the error amplifier uncommitted and available externally.

a) Two independent channels with either common or different input voltages and different output voltages. The two channels each have their own voltage feedback path from their own output. In this mode, positive inputs of error amplifier 2 are connected externally to Vref. If the application uses a common input voltage, the sawtooth phase shift between the channels provides some measure of input ripple current cancellation.

It is possible to sequence the start up of the channel with an RC delay between the reference and +IN2. The capacitor will be internally reset during UVLO and soft start.

Power Good

The controller provides a power good signal. This is an open collector output, which is pulled low if the output voltage is outside of the power good window.

Soft Start/Enable

The Soft Start/Enable (SS/ENA) pin serves several functions. If held below the Soft Start Enable threshold, both channels are inhibited. DH1 and DH2 will be low, turning off the top FETs. Between the Soft Start Enable threshold and the Soft Start End threshold, the duty cycle is allowed to increase. At the Soft Start End threshold, maximum duty cycle is reached. In practical applications the error amplifier will be controlling the duty cycle before the Soft Start End threshold is reached. To avoid boost problems during startup in current share mode, both channels start up in asynchronous mode, and the bottom FET body diode is used for recirculating current during the FET off time. When the SS/ENA pin reaches the Soft Start Transition threshold, the channels begin operating in synchronous mode for improved efficiency. The soft start pin sources approximately 25uA and soft start timing can be set by selection of an appropriate soft start capacitor value.

Layout Guidelines

Power and signal traces must be kept separated for noise considerations. Feedback, current sense traces and analog ground should not cross any traces or planes carrying high switching currents, such as the input loop or the phase node.

The input loop, consisting of the input capacitors and both MOSFETs must be kept as small as possible. All of the high switching currents occur in this loop. The enclosed loop area must be kept small to minimize inductance and radiated and conducted emissions. Designing for minimum trace length is not always the best approach, often a more optimum layout can be achieved by keeping loop area constraints in mind.

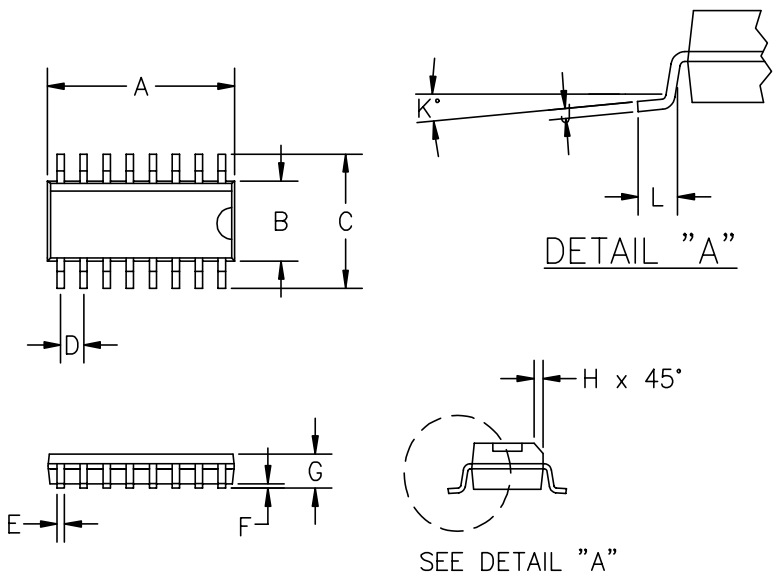
It is important to keep gate lengths short, the IC must be close to the power switches. This is more difficult in a dual channel device than a single and requires that the two power paths run on either side of a centrally located controller.

Grounding requirements are always conflicting in a buck converter, especially at high power, and the trick is to achieve the best compromise. Power ground (PGND) should be returned to the bottom MOSFET source to provide the best gate current return path. Analog ground (GND) should be returned to the ground side of the output capacitors so that the analog circuitry in the controller has an electrically quiet reference and to provide the greatest feedback accuracy. The problem is that the differential voltage capability of the two IC grounds is limited to about 1V for proper operation and so the physical separation between the two grounds must also be minimized. If the grounds are too far apart, fast current transitions in the connection can generate voltage spikes exceeding the 1V capability, resulting in unstable and erratic behavior.

The feedback divider must be close to the IC and be returned to analog ground. Current sense traces must be run parallel and close to each other and to analog ground.

The IC must have a ceramic decoupling capacitor across its supply pins, mounted as close to the device as possible. The small ceramic, noise-filtering capacitors on the current sense lines should also be placed as close to the IC as possible.

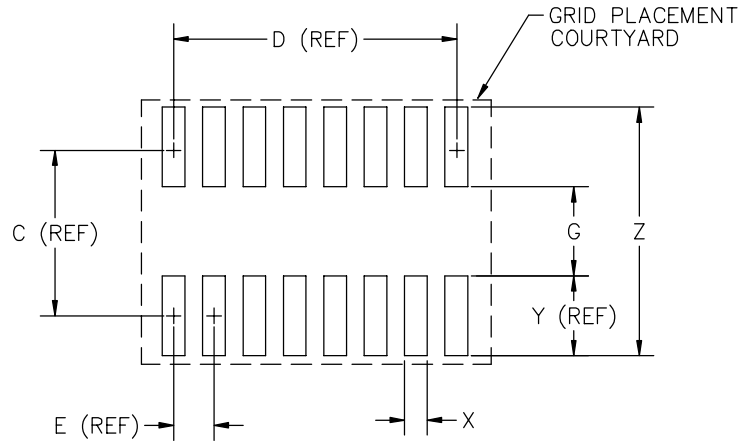
Outline Drawing - SO-16



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.386	.393	9.80	10.0	[2]
B	.150	.158	3.80	4.00	[2]
C	.228	.244	5.80	6.20	–
D	.050	BSC	1.27	BSC	–
E	.013	.020	0.33	0.51	–
F	.004	.010	.10	.25	–
G	.053	.069	1.35	1.75	–
H	.010	.020	.25	.50	–
J	.007	.010	.19	.25	–
K	0°	8°	0°	8°	–
L	.016	.050	.40	1.27	–

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS

Land Pattern - SO-16



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.197	–	5.00	–
D	–	.35	–	8.89	–
E	–	.05	–	1.27	–
G	.102	.110	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.095	–	2.40	–
Z	.28	.29	7.20	7.40	–

[1] GRID PLACEMENT COURTYARD IS 22 X 16 ELEMENTS (11mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

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