

HD74LS03

Quadruple 2-Input Positive NAND Gates
(with Open Collector Outputs)

REJ03D0390-0200

Rev.2.00

Feb.18.2005

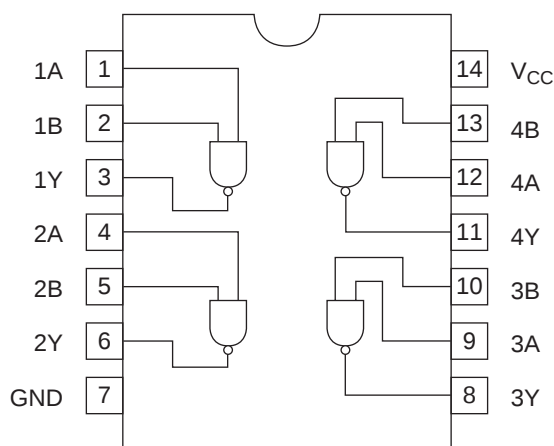
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS03P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS03FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

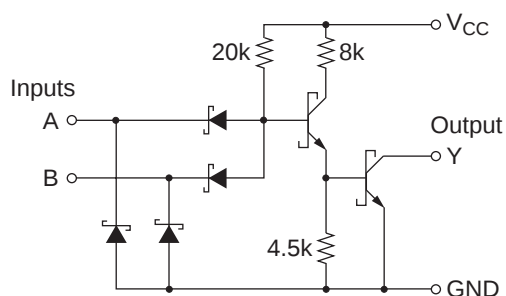
Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Circuit Schematic (1/4)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC} ^{Note}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output voltage	V_{OH}	—	—	5.5	V
Output current	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OL}	—	—	0.5	V	$I_{OL} = 8\text{ mA}$ $I_{OL} = 4\text{ mA}$ $V_{CC} = 4.75\text{ V}, V_{IH} = 2\text{ V}$
		—	—	0.4		
Input current	I_{IH}	—	—	20	μA	$V_{CC} = 5.25\text{ V}, V_I = 2.7\text{ V}$
	I_{IL}	—	—	–0.4	mA	$V_{CC} = 5.25\text{ V}, V_I = 0.4\text{ V}$
	I_I	—	—	0.1	mA	$V_{CC} = 5.25\text{ V}, V_I = 7\text{ V}$
Output current	I_{OH}	—	—	100	μA	$V_{CC} = 4.75\text{ V}, V_{IH} = 0.8\text{ V}, V_{OH} = 5.5\text{ V}$
Supply current	I_{CCH}	—	0.8	1.6	mA	$V_{CC} = 5.25\text{ V}$
	I_{CCL}	—	2.4	4.4	mA	$V_{CC} = 5.25\text{ V}$
Input clamp voltage	V_{IK}	—	—	–1.5	V	$V_{CC} = 4.75\text{ V}, I_{IN} = -18\text{ mA}$

Note: * $V_{CC} = 5\text{ V}$, Ta = 25°C

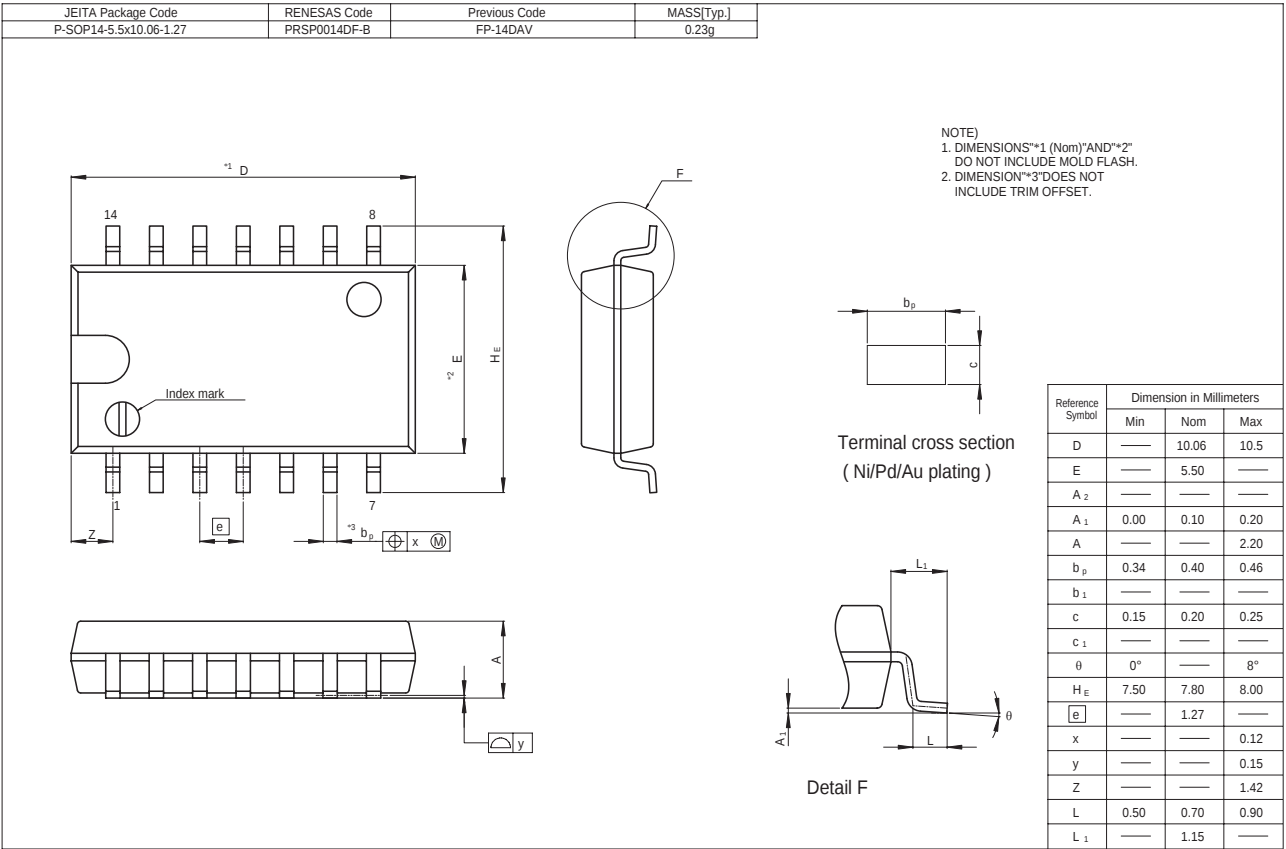
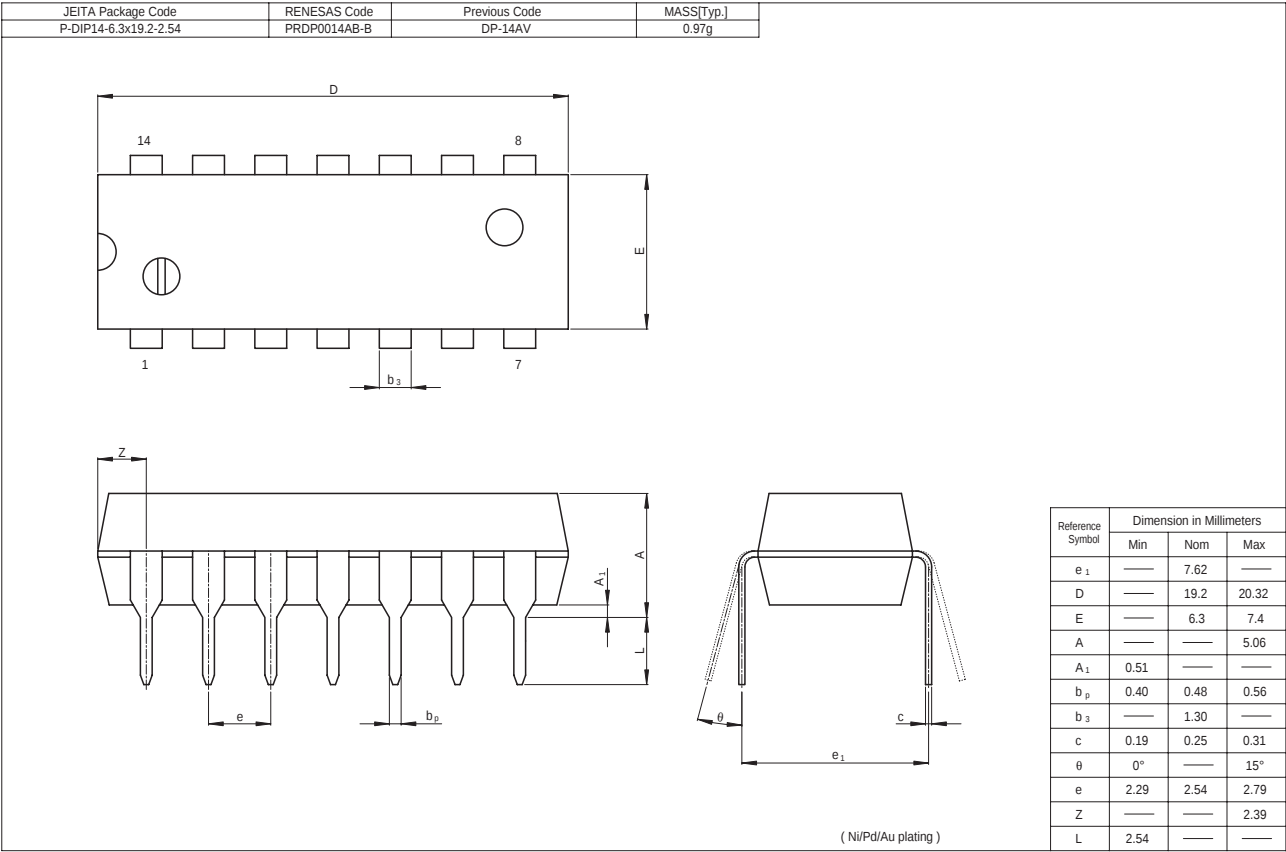
Switching Characteristics

($V_{CC} = 5\text{ V}$, Ta = 25°C)

Item	Symbol	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	—	17	32	ns	$C_L = 15\text{ pF}, R_L = 2\text{ k}\Omega$
	t_{PHL}	—	25	28	ns	

Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

Package Dimensions



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