General Description

The MAX690 family of supervisory circuits reduces the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include µP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX690 family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

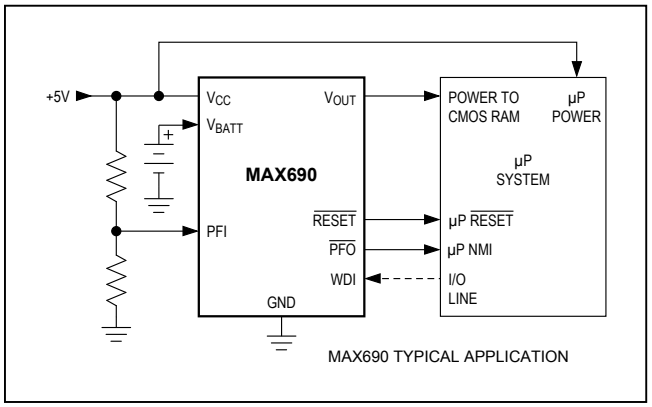
The MAX690, MAX692, and MAX694 are supplied in 8-pin packages and provide four functions:

- A reset output during power-up, power-down, and brownout conditions.
- Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
- A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
- A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MAX691, MAX693, and MAX695 are supplied in 16-pin packages and perform all MAX690, MAX692, MAX694 functions, plus:

- Write protection of CMOS RAM or EEPROM.
- Adjustable reset and watchdog timeout periods.
- Separate outputs for indicating a watchdog timeout, backup-battery switchover, and low V_{CC}.

Typical Operating Circuit



MAX690 TYPICAL APPLICATION

Benefits and Features

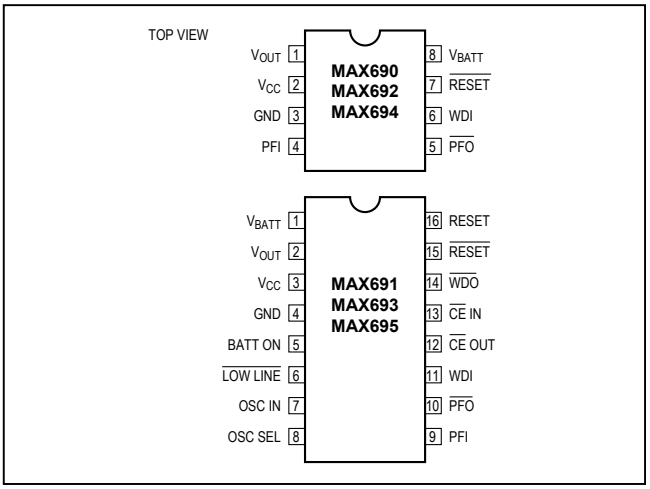
- Supervisory Function Integration Saves Board Space while Fully Protecting Microprocessor-Based Systems
  - Precision Voltage Monitor
    - 4.65V (MAX690, MAX691, MAX694, MAX695)
    - 4.40V (MAX692, MAX693)
  - Power OK/Reset Time Delay
    - 50ms, 200ms, or Adjustable
  - Watchdog Timer
    - 100ms, 1.6s, or Adjustable
  - Battery Backup Power Switching
  - Voltage Monitor for Power Fail or Low Battery Warning
  - Minimum External Component Count
- Low Power Consumption in Battery Backup Mode Extends Battery Life
  - 1µA Standby Current
- Onboard Gating of Chip Enable Signals Protects Against Erroneous Data Written to RAM During Low V_{CC} Events

Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

Ordering information appears at end of data sheet.

Pin Configurations



maxim integrated™

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6.0V
- V_{BATT} ..... -0.3V to +6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{OUT} + 0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/µs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... -40°C to +85°C
- M suffix ..... -55°C to +125°C

Power Dissipation
- 8-Pin Plastic DIP (derate 5mW/°C above +70°C) 400mV
- 8-Pin CERDIP (derate 8mW/°C above +85°C) 500mV
- 16-Pin Plastic DIP (derate 7mW/°C above +70°C) 600mV
- 16-Pin Small Outline (derate 7mW/°C above +70°C) 600mV
- 16-Pin CERDIP (derate 10mW/°C above +85°C) 600mV

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (Soldering, 10s) ..... 300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATTERY BACKUP SWITCHING						
Operating Voltage Range (MAX690, MAX691, MAX694, MAX695 V_{CC})			4.75		5.5	V
Operating Voltage Range (MAX690, MAX691, MAX694, MAX695 V_{BATT})			2.0		4.25	
Operating Voltage Range (MAX692, MAX693 V_{CC})			4.5		5.5	
Operating Voltage Range (MAX692, MAX693 V_{BATT})			2.0		4.0	
V_{OUT} Output Voltage	I_{OUT} = 1mA		V_{CC} - 0.3	V_{CC} - 0.1		V
	I_{OUT} = 50mA		V_{CC} - 0.5	V_{CC} - 0.25		
V_{OUT} in Battery Backup Mode	I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Supply Current (Excluded I_{OUT})	I_{OUT} = 1mA			2	5	mA
	I_{OUT} = 50mA			3.5	10	
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V			0.6	1	µA
Battery Standby Current (+ = Discharge, - = Charge)	5.5V > V_{CC} > V_{BATT} + 1V	T_A = +25°C	-0.1		+0.02	µA
		T_A = full operating range	-1.0		+0.02	
Battery Switchover Threshold (V_{CC} - V_{BATT})	Power-up			70		mV
	Power-down			50		

Electrical Characteristics (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short-Circuit Current	BATT ON = V_{OUT} = 4.5V sink current			25		mA
	BATT ON = 0V source current		0.5	1	25	µA
RESET AND WATCHDOG TIMER						
Reset Voltage Threshold	T_A = full operating range	MAX690, MAX691, MAX694, MAX695	4.5	4.65	4.75	V
		MAX692, MAX693	4.25	4.4	4.5	
Reset Threshold Hysteresis				40		mV
Reset Timeout Delay (MAX690/MAX691/ MAX692/MAX693)	Figure 6, OSC SEL HIGH, V_{CC} = 5V		35	50	70	ms
Reset Timeout Delay (MAX694/MAX695)	Figure 6, OSC SEL HIGH, V_{CC} = 5V		140	200	280	ms
Watchdog Timeout Period, Internal Oscillator	Long period, V_{CC} = 5V		1.0	1.6	2.25	s
	Short period, V_{CC} = 5V		70	100	140	ms
Watchdog Timeout Period, External Clock	Long period		3840		4097	Clock Cycles
	Short period		768		1025	
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 0.8V_{CC}		200			ns
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage	I_{SINK} = 1.6mA, V_{CC} = 4.25V				0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V		3.5			
RESET and $\overline{WDO}$ Output Voltage	I_{SINK} = 1.6mA				0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V		3.5			
Output Short-Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$		1	3	25	µA
WDI Input Threshold Logic-Low	V_{CC} = 5V (Note 2)				0.8	V
WDI Input Threshold Logic-High	V_{CC} = 5V (Note 2)		3.5			
WDI Input Current	WDI = V_{OUT}			20	50	µA
	WDI = 0V		-50	-15		
POWER-FAIL DETECTOR						
PFI Threshold	V_{CC} = 5V, T_A = full		1.2	1.3	1.4	V
PFI Current				±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA				0.4	V
	I_{SOURCE} = 1µA		3.5			V
$\overline{PFO}$ Short Circuit Source Current	PFI = V_{IH}, $\overline{PFO}$ = 0V		1	3	25	µA

Electrical Characteristics (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP ENABLE GATING					
$\overline{CE}$ IN Thresholds	V_{IL}			0.8	V
	V_{IH}	3.0			
$\overline{CE}$ IN Pullup Current			3		µA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 3.0mA	V_{OUT} - 1.5			
	I_{SOURCE} = 1µA, V_{CC} = 0V	V_{OUT} - 0.05			
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		50	200	ns
OSCILLATOR					
OSC IN Input Current			±2		µA
OSC SEL Input Pullup Current			5		µA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125kΩ.

Pin Description

PIN		NAME	FUNCTION
MAX690/ MAX692/ MAX694	MAX691/ MAX693/ MAX695		
2	3	V_{CC}	The +5V Input
8	1	V_{BATT}	Backup Battery Input. Connect to Ground if a backup battery is not used.
1	2	V_{OUT}	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used. Connect a 0.1µF or larger bypass capacitor to V_{OUT}.
3	4	GND	0V Ground Reference for All Signals
7	15	$\overline{RESET}$	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MAX690/691/694/695, and 4.4V for the MAX692 and MAX693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V, (except 200ms in MAX694/695). $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
6	11	WDI	Watchdog Input (WDI). WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer input.
4	9	PFI	Noninverting Input to the Power-Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX690/ MAX692/ MAX694	MAX691/ MAX693/ MAX695		
5	10	$\overline{PFO}$	Output of the Power-Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
—	13	$\overline{CE}$ IN	$\overline{CE}$ Gating Circuit Input. Connect to GND or V_{OUT} if not used.
—	12	$\overline{CE}$ OUT	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MAX691 and MAX695, 4.4V for MAX693). See Figure 6.
—	5	BATT ON	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 25mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
—	6	$\overline{LOW\ LINE}$	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
—	16	RESET	Active-High Output. It is the inverse of $\overline{RESET}$.
—	8	OSC SEL	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3µA internal pullup. See Table 1.
—	7	OSC IN	When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting and external oscillator to this pin. See Figure 8. When OSC SEL is high or floating, OSC IN selects between fast and slow Watchdog timeout periods.
—	14	$\overline{WDO}$	The Watchdog Output ($\overline{WDO}$). $\overline{WDO}$ goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

Typical Applications

MAX691, MAX693, and MAX695

A typical connection for the MAX691/693/695 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 25mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1µA maximum when V_{CC} is between 0V and V_{BATT}–700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's Reset line low when V_{CC} is below 4.65V (4.4V for MAX693). An internal monostable holds $\overline{RESET}$ low for 50ms* after V_{CC} rises above 4.65V (4.4V for MAX693). This prevents repeated toggling of $\overline{RESET}$ even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{RESET}$ must be held low until the microprocessor clock oscillator has started. The MAX690 family power-up $\overline{RESET}$ pulse lasts 50ms* to allow for this oscillator start-up time. The manual reset switch and the 0.1µF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

*200ms for MAX695

Power-Fail Detector

The MAX691/93/95 issues a nonmaskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the power-fail input (PFI). When the voltage at PFI falls below 1.3V, the power-fail output ($\overline{PFO}$) drives the processor's NMI input low. If a power-fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} fails from 4.8V to 4.65V to save data into RAM. An earlier power-fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MAX691/MAX693/MAX695 $\overline{CE}$ OUT line drives the $\overline{Chip}$ $\overline{Select}$ inputs of the CMOS RAM. $\overline{CE}$ OUT follows $\overline{CE}$ IN as long as V_{CC} is above the 4.65V (4.4V for MAX693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{CE}$ OUT goes high, independent of the logic level at $\overline{CE}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The $\overline{LOW}$ $\overline{LINE}$ output goes low when V_{CC} falls below 4.65V (4.4V for MAX693).

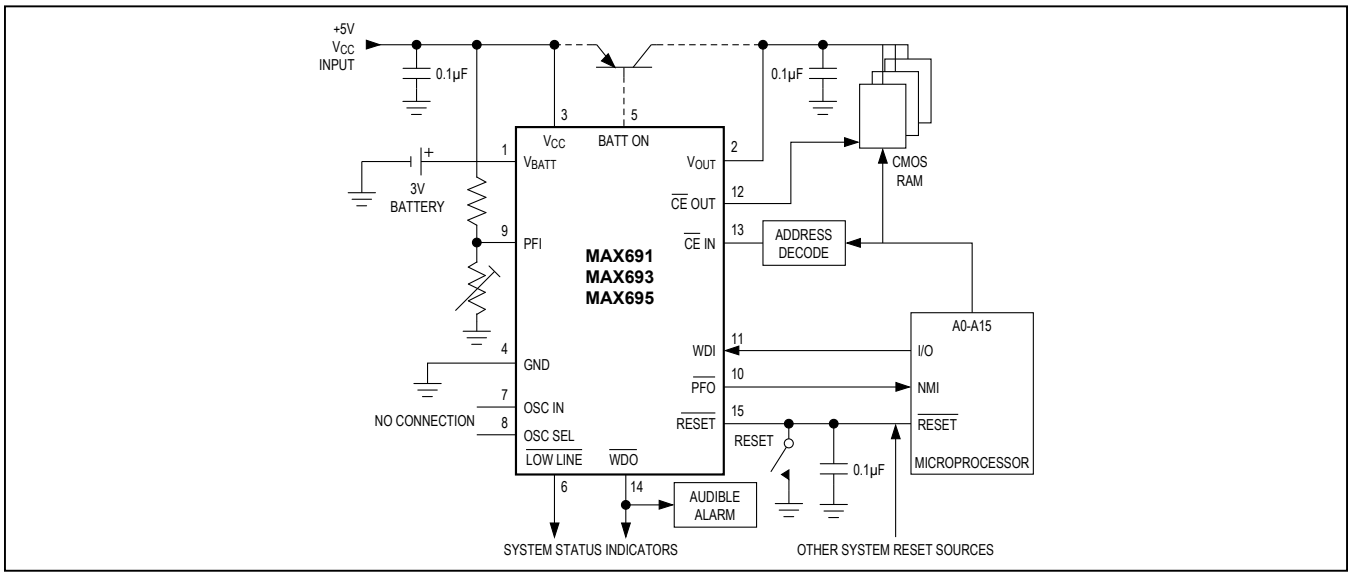


Figure 1. MAX691/693/695 Typical Application

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6s to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled the MAX691/MAX693 will issue a 50ms* $\overline{\text{RESET}}$ pulse after 1.6s. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6s until the WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MAX690, MAX692, and MAX694

The 8 pin MAX690, MAX692, and MAX694 have most of the features of the MAX691, MAX693, and MAX695. Figure 2 shows the MAX690/MAX692/MAX694 in a typical application. Operation is much the same as with the MAX691/MAX693/MAX695 (Figure 1), but in this case, the power- fail input (PFI) monitors the unregulated input to the 7805 regulator. The MAX690/MAX694 $\overline{\text{RESET}}$ output goes low when V_{CC} falls below 4.65V. The $\overline{\text{RESET}}$ output of the MAX692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 50mA. The MAX690/MAX692/MAX694 does not have a BATT ON output to drive an external transistor. The MAX690/MAX692/MAX694 also does not include chip enable gating circuitry that is available on the MAX690/MAX692/MAX694. In many systems though, $\overline{\text{CE}}$ gating is not needed since a low input to the microprocessor $\overline{\text{RESET}}$ line prevents the processor from writing to RAM during power-up and power-down transients.

The MAX690/MAX692/MAX694 watchdog timer has a fixed 1.6s timeout period. If WDI remains either low or high for more than 1.6s, a $\overline{\text{RESET}}$ pulse is sent to the microprocessor. The watchdog timer is disabled if WDI is left unconnected.

**200ms for MAX695*

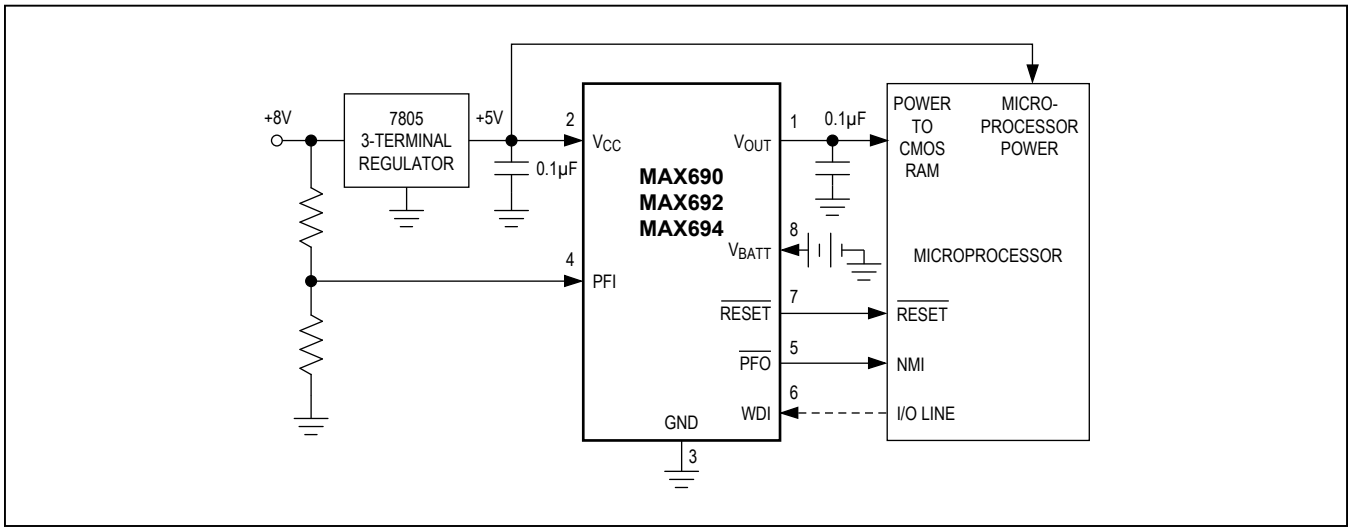


Figure 2. MAX690/692/694 Typical Application

Detailed Description

Battery-Switchover and V_{OUT}

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MAX691/MAX693/MAX695 only) can directly drive the base of the external transistor.

It should be noted that the MAX690–MAX695 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} - 700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX690/MAX691/MAX694/MAX695 operate with battery voltages from 2.0V to 4.25V while MAX692/MAX693 operate with battery voltages from 2.0V to 4.0V. High value capacitors can also be used for short-term memory backup. External circuitry is required to ensure that the capacitor voltage does not rise above the reset threshold, and that the charging resistor does not discharge the capacitor when in backup mode. The MAX691A and the MAX791 provide solutions requiring fewer external components.

A small charging current of typically 10nA (0.1µA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

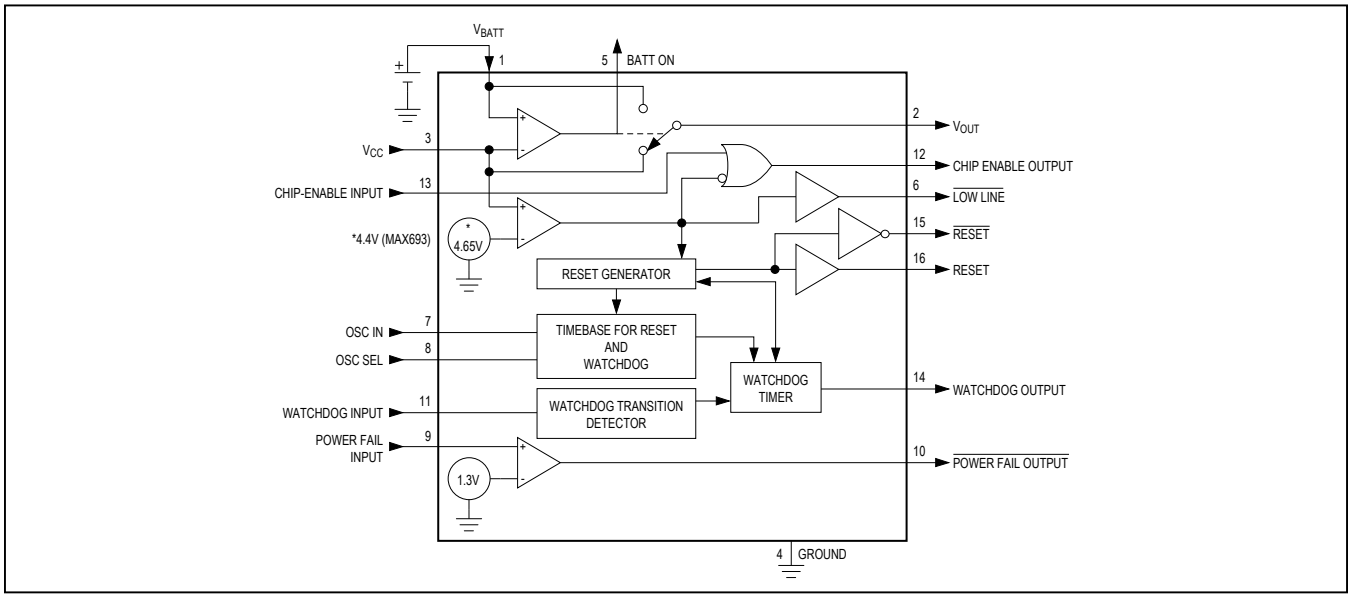


Figure 3. MAX691/MAX693/MAX695 Block Diagram

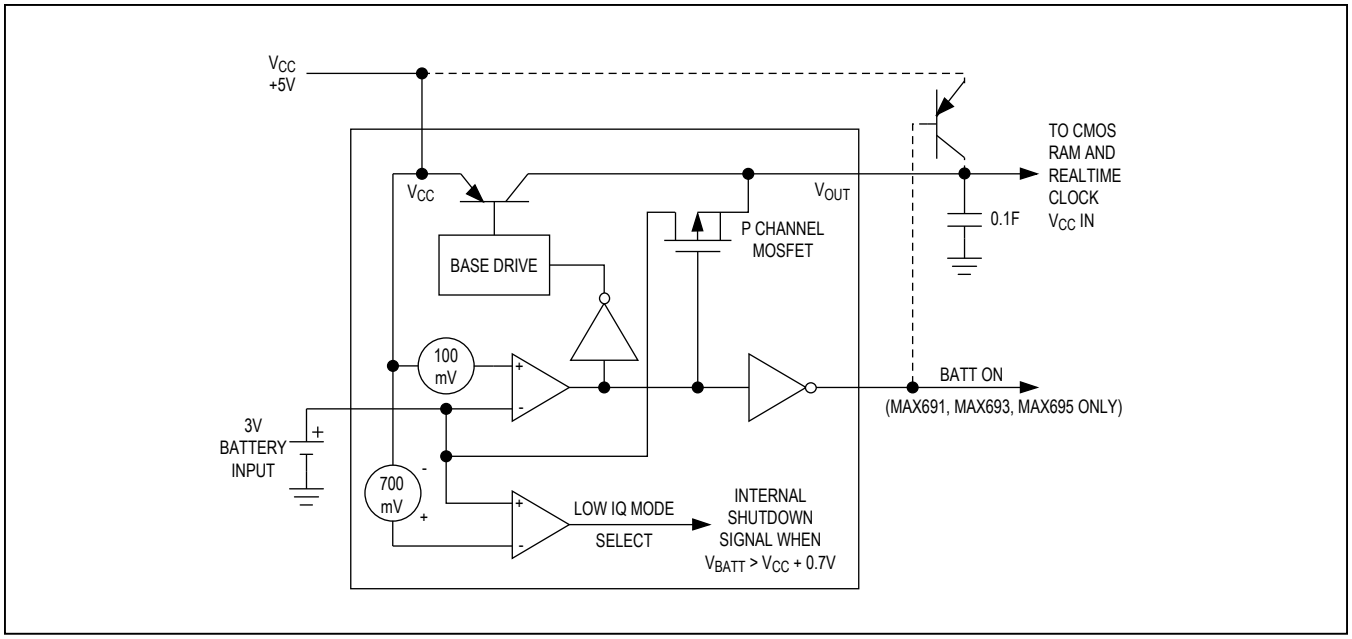


Figure 4. Battery-Switchover Block Diagram

Reset Output

$\overline{RESET}$ is an active-low output which goes low whenever V_{CC} falls below 4.5V (MAX690/MAX691/MAX694/MAX695) or 4.25V (MAX692/MAX693). It will remain low until V_{CC} rises above 4.75V (MAX690/691/694/695) or 4.5V (MAX692/MAX693) for milliseconds*. See Figures 5 and 6.

The guaranteed minimum and maximum thresholds of MAX690/MAX691/MAX694/MAX695 are 4.5V and 4.75V, while the guaranteed thresholds of the MAX692/MAX693 are 4.25V and 4.5V. The MAX690/MAX691/MAX694/MAX695 is compatible with 5V supplies with a +10%, -5% tolerance while the MAX692/MAX693 is compatible with 5V ±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MAX690/MAX691/MAX694/MAX695, and 4.4V in the MAX692/MAX693.

The response time of the reset voltage comparator is about 100µs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{RESET}$ output.

$\overline{RESET}$ also goes low if the watchdog timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{RESET}$ has an internal 3µA pullup, and can either connect to and open collector Reset bus or directly drive a CMOS gate without and external pullup resistor.

**200ms for MAX694 and MAX695*

$\overline{CE}$ Gating and RAM Write Protection

The MAX691/MAX693/MAX695 use two pins to control the $\overline{Chip\ Enable}$ or $\overline{Write}$ inputs of CMOS RAMs. When V_{CC} is +5V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The MAX693 $\overline{CE}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{CE}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{CE}$ OUT typically drives the $\overline{CE}$, $\overline{CS}$, or $\overline{Write}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at and invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}$ OUT to drive the $\overline{Store}$ or $\overline{Write}$ inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{CE}$ OUT is too long, connect $\overline{CE}$ IN to GND and use the resulting $\overline{CE}$ OUT to control a high speed external logic gate. A second alternative is to AND the $\overline{LOW\ LINE}$ output with the $\overline{CE}$ or $\overline{WR}$ signal. An external logic gate and the $\overline{RESET}$ output of the MAX690/MAX692/MAX694 can also be used for CMOS RAM write protection.

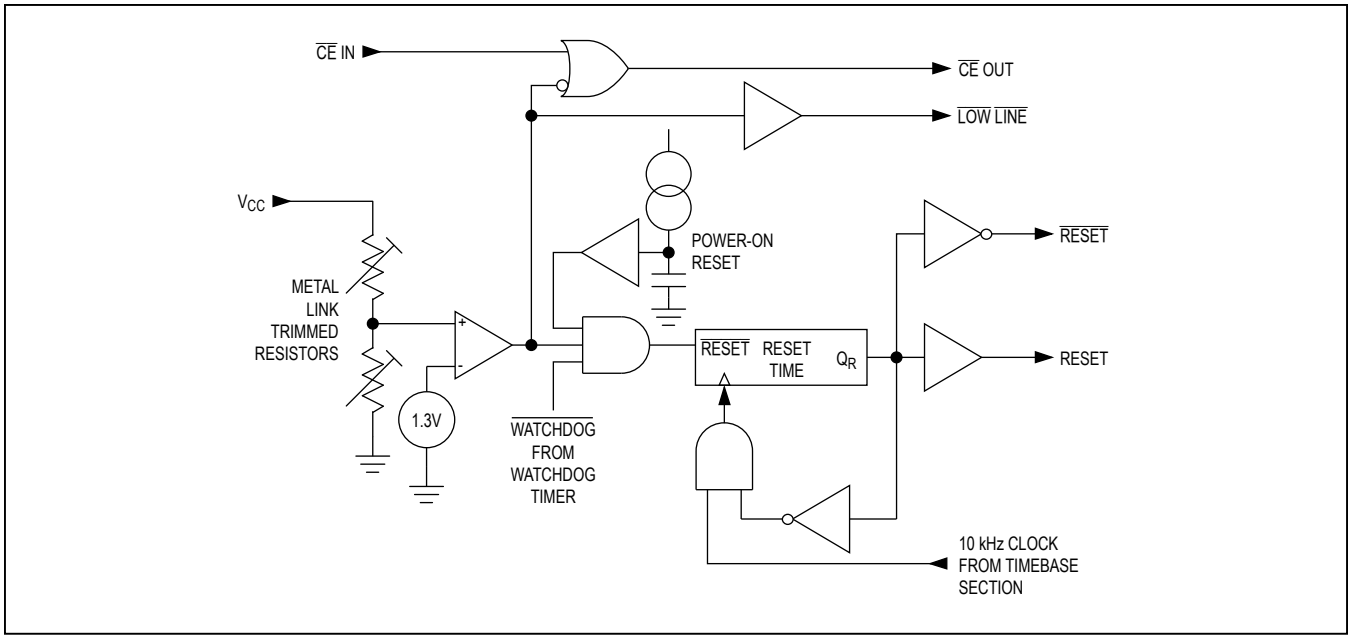


Figure 5. Reset Block Diagram

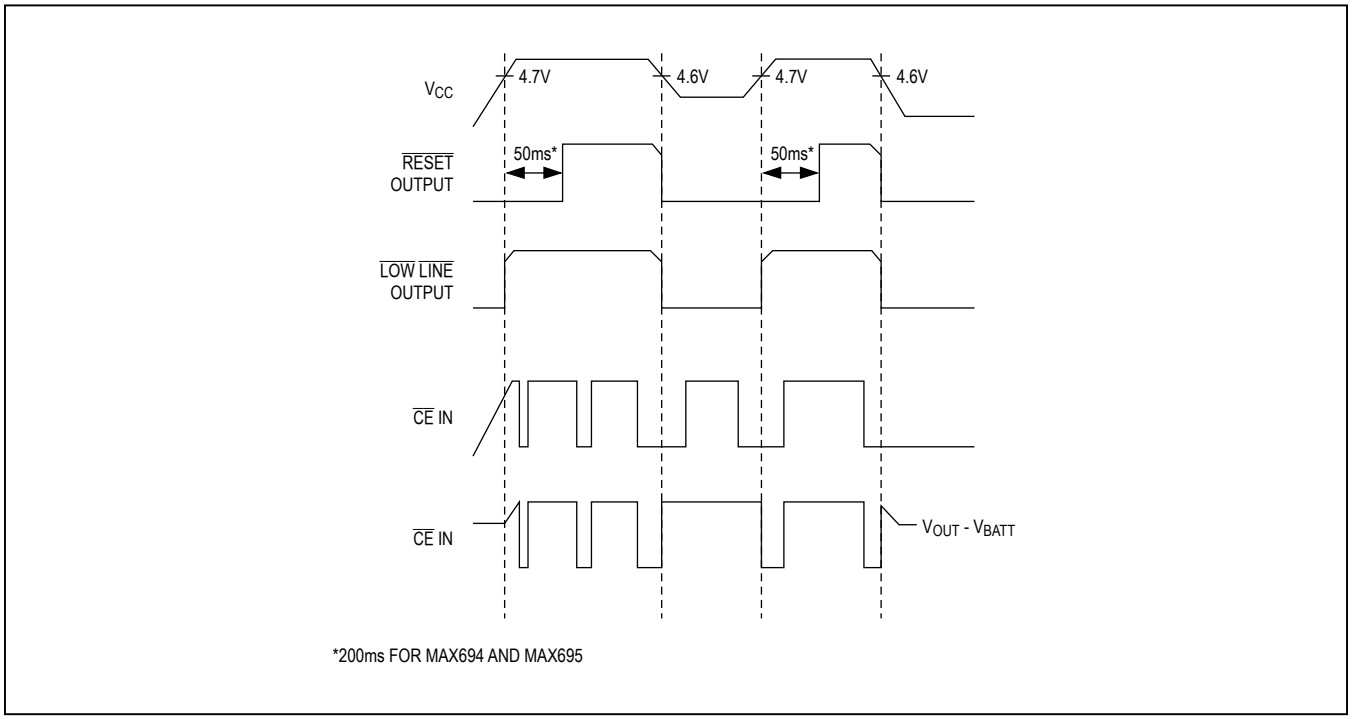


Figure 6. Reset Timing

1.3V Comparator and Power-Fail Warning

The power-fail input (PFI) is compared to an internal 1.3V reference. The power-fail output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3V. Typically, PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the +5V supply falls below 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the $\overline{RESET}$ output goes low (4.5V for MAX692/MAX693).

The power-fail detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced when V_{CC} is lower than V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50ms* $\overline{RESET}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX691/MAX693/MAX695 has a longer timeout period after reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{RESET}$ has gone high. The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6s. The watchdog monitor can be deactivated by floating the watchdog input (WDI).

The watchdog output ($\overline{WDO}$, MAX691/MAX693/MAX695 only) goes low if the watchdog timer times out and remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6s and the reset pulse width is fixed at 50ms* on the 8-pin MAX690/MAX692/MAX694. The MAX691/MAX693/MAX695 allow these times to be adjusted per Table 1. Figures 8 shows various oscillator configurations.

The internal oscillator is enabled when OSC SEL is floating. In this mode, OSC IN selects between the 1.6s and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period 1.6s. This gives the microprocessors time to reintialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

**200ms for MAX694*

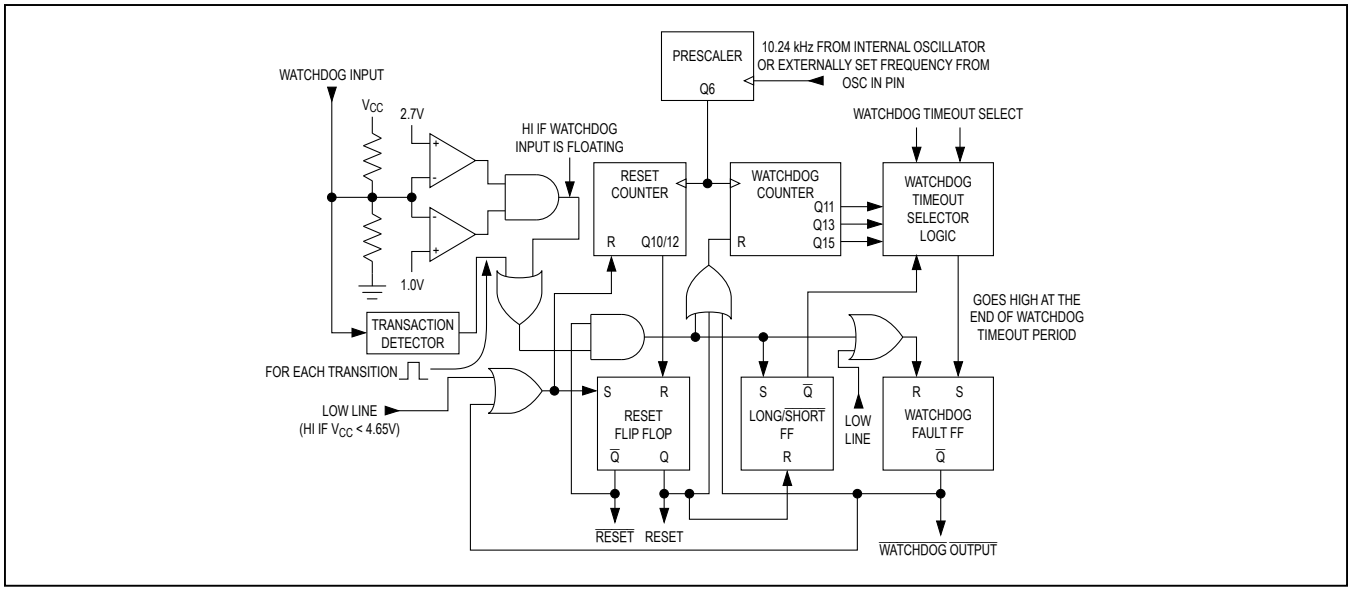


Figure 7. Watchdog Timer Block Diagram

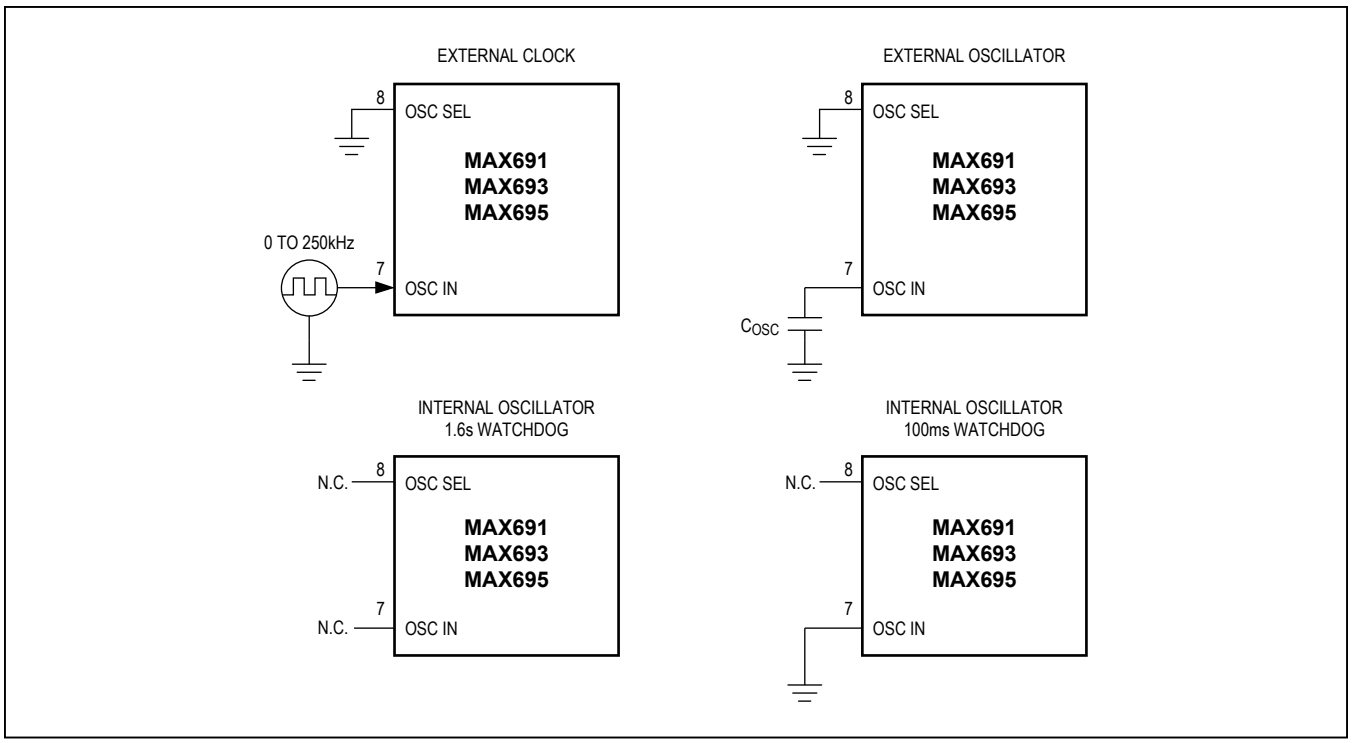


Figure 8. Oscillator Circuits

Table 1. MAX691/MAX693/MAX695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	WATCHDOG TIMEOUT PERIOD		RESET TIMEOUT PERIOD	
		NORMAL	IMMEDIATELY AFTER REST	MAX691/MAX693	MAX695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor	400ms/47pF x C	1.6s/47pF x C	200ms/47pF x C	800ms/47pF x C
Floating	Low	100ms	1.6s	50ms	200ms
Floating	Floating	1.6s	1.6s	50ms	200ms

Note 1: The MAX690/MAX692/MAX694 watchdog timeout period is fixed at 1.6s nominal, the MAX690/692 reset pulse width is fixed at 50ms nominal and the MAX694 is 200ms nominal.

Note 2: When the MAX691 OSC SEL pin is low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 6.55kHz. The nominal oscillator frequency with capacitor is:

$$f_{OSC}(Hz) = \frac{120{,}000}{C(pF)}$$

Note 3: See *Electrical Characteristics* table for minimum and maximum timing values.

Application Hints

Other Uses of the Power-Fail Detector

In Figure 9, the power-fail detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the power-fail detector is not as accurate as the onboard reset-voltage detector, a trimpot must be used to adjust the voltage detection threshold. Both the $\overline{PFO}$ and $\overline{RESET}$ outputs have high sink current capability and only 10µA of source current drive. This allows the two outputs to be connected directly to each other in a wired OR fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is noninverting, hysteresis can be added by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 12. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a three-state buffer (Figure 13). The drawback to this circuit is that a software fault may be erroneously three-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01µF capacitor sets a watchdog timeout delay of 100s. When the control input is low the OSC SEL pin is high, selecting the internal oscillator. The 100ms or the 1.6s period is chosen, depending on which diode in Figure 14 is used.

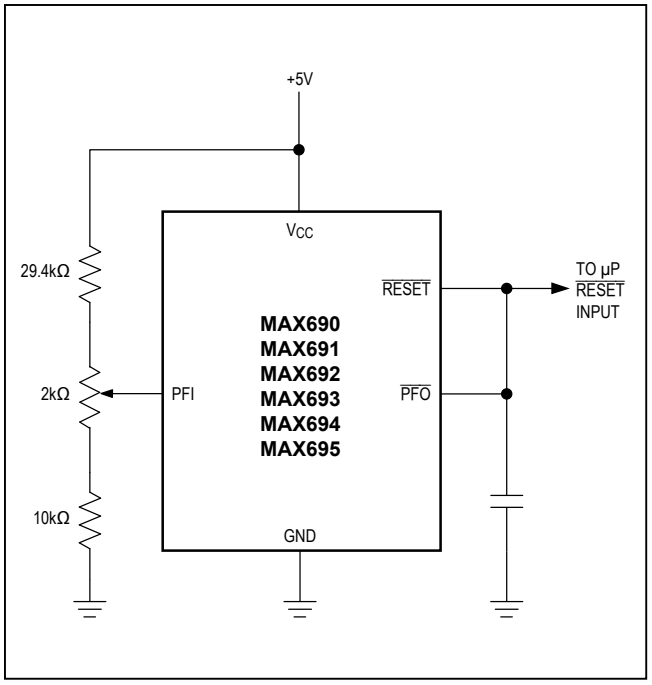


Figure 9. Externally Adjustable V_{CC} Reset Threshold

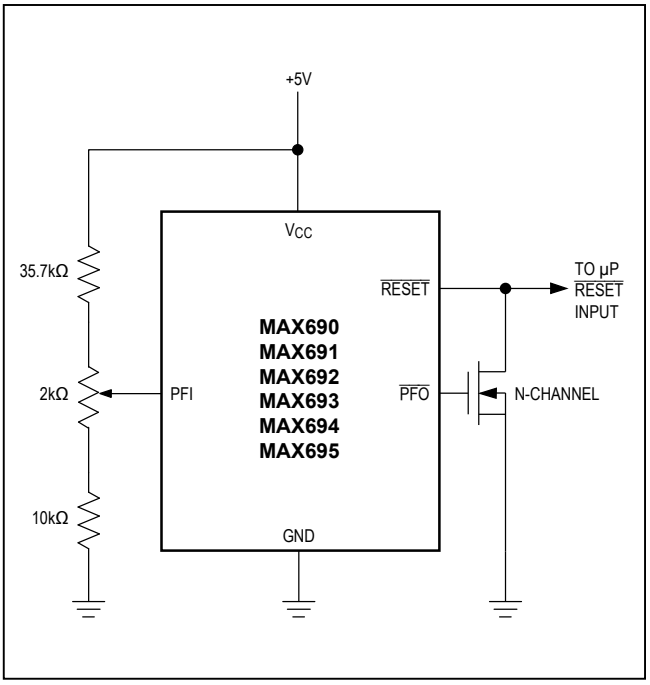


Figure 10. Reset on Overvoltage or Undervoltage

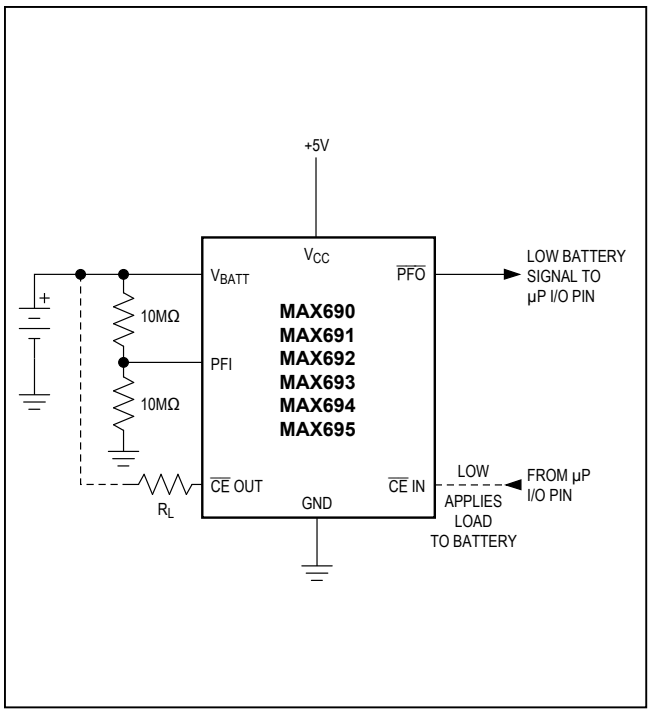


Figure 11. Backup VBattery Monitor with Optional Test Load

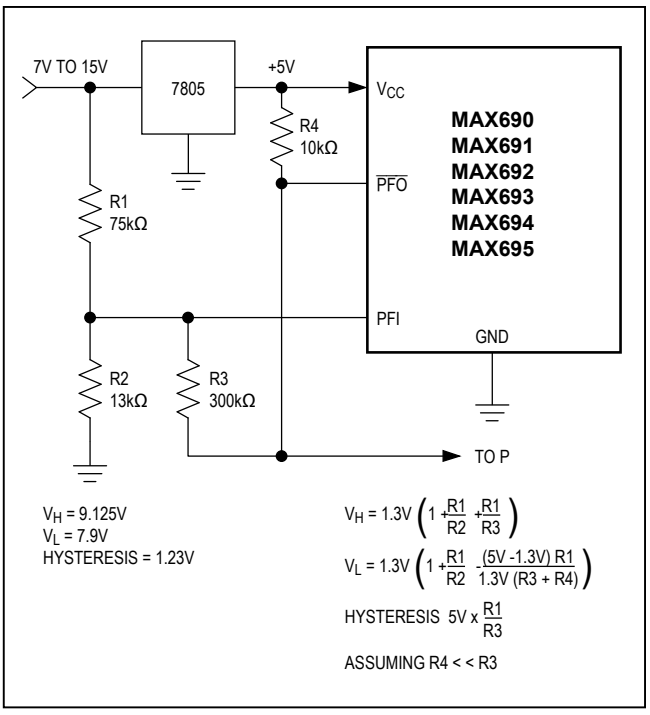


Figure 12. Adding Hysteresis to the Power-Fail Voltage Comparator

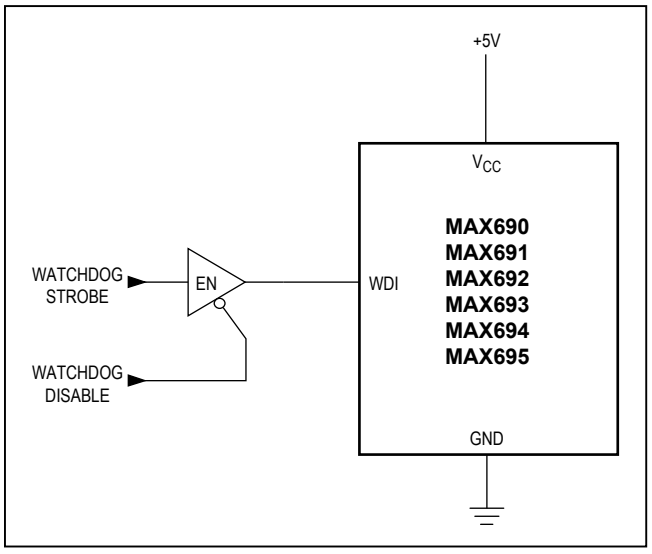


Figure 13. Disabling the Watchdog Under Program Control

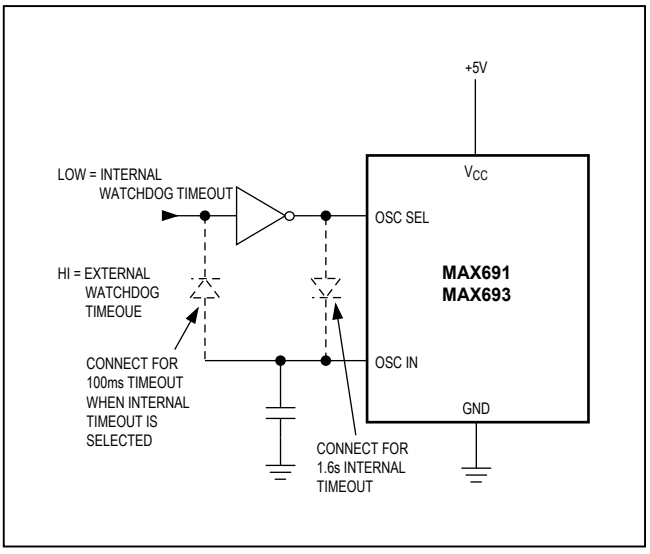


Figure 14. Selecting Internal or External Watchdog Timeout

Table 2. Input and Output Status In Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic-low
RESET	Logic-high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic-low
BATT ON	Logic-high
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect the source current.
$\overline{WDO}$	Logic-high
PFI	The power-fail comparator is turned off and the power-fail input voltage has no effect on the power-fail output.
$\overline{PFO}$	Logic-low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect the source current.
$\overline{CE}$ OUT	Logic-high
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12µA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} +100mV and V_{BATT} - 700mV. The supply current is 1µA maximum when V_{CC} is less than V_{BATT} - 700mV.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX690CPA	0°C to +70°C	8 Lead Plastic DIP
MAX690C/D	0°C to +70°C	Dice*
MAX690EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX690EJA	-40°C to +85°C	8 Lead CERDIP
MAX690MJA	-55°C to +125°C	8 Lead CERDIP
MAX691CPE	0°C to +70°C	16 Lead Plastic DIP
MAX691CWE	0°C to +70°C	16 Lead Wide SO
MAX691C/D	0°C to +70°C	Dice*
MAX691EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX691EWE	-40°C to +85°C	16 Lead Wide SO
MAX691EJE	-40°C to +85°C	16 Lead CERDIP
MAX691MJE	-55°C to +125°C	16 Lead CERDIP
MAX692C/D	0°C to +70°C	Dice
MAX692CPA	0°C to +70°C	8 Lead Plastic DIP
MAX692EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX692EJA	-40°C to +85°C	8 Lead CERDIP
MAX692MJA	-55°C to +125°C	8 Lead CERDIP
MAX693C/D	0°C to +70°C	Dice

PART	TEMP RANGE	PIN-PACKAGE
MAX693CPE	0°C to +70°C	16 Lead Plastic DIP
MAX693CWE	0°C to +70°C	16 Lead Wide SO
MAX693EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX693EJE	-40°C to +85°C	16 Lead CERDIP
MAX693EWE	-40°C to +85°C	16 Lead Wide SO
MAX693MJE	-55°C to +125°C	16 Lead CERDIP
MAX694C/D	0°C to +70°C	Dice
MAX694CPA	0°C to +70°C	8 Lead Plastic DIP
MAX694EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX694EJA	-40°C to +85°C	8 Lead CERDIP
MAX694MJA	-55°C to +125°C	8 Lead CERDIP
MAX695C/D	0°C to +70°C	Dice
MAX695CPE	0°C to +70°C	16 Lead Plastic DIP
MAX695CWE	0°C to +70°C	16 Lead Wide SO
MAX695EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX695EJE	-40°C to +85°C	16 Lead CERDIP
MAX695EWE	-40°C to +85°C	16 Lead Wide SO
MAX695MJE	-55°C to +125°C	16 Lead CERDIP

**Contact factory for dice specifications.*

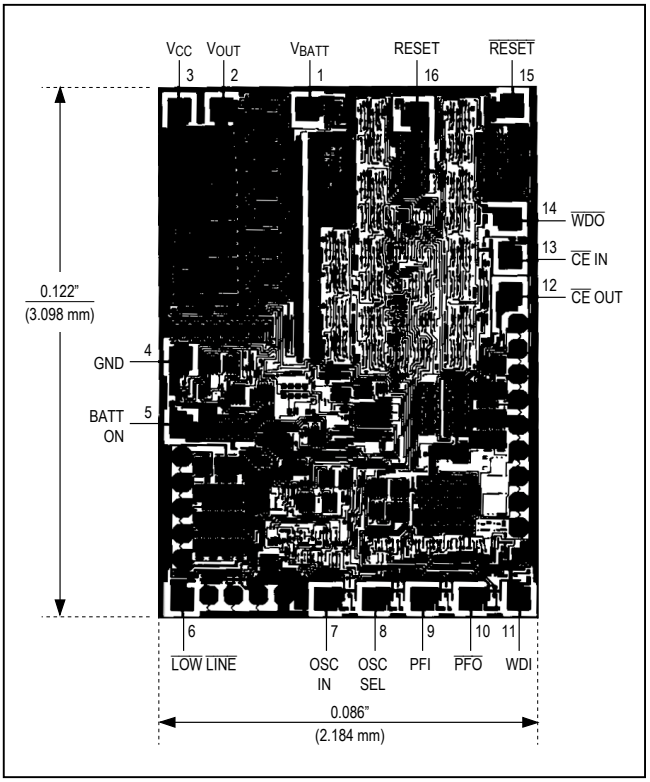
Devices in PDIP and SO packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP	P8-2	21-0043	—
8 CEDIP	J8-2	21-0045	—
16 PDIP	P16-1	21-0043	—
16 Wide SO	W16-1	21-0042	—
16 CERDIP	P16-1	21-0043	—

Chip Topography



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	4/15	Revised *Benefits and Features* section	1

