

CMOS Logic MN4000B Series

MN4015B/MN4015BS

6932852 PANASONIC INDL,ELECTRONIC

66C 04945

D T-46-09-05

MN4015B / MN4015BS

Dual 4-Stage Static Shift Registers

■ Description

The MN4015B/S are dual 4-bit static shift registers.

Each register of D type flip-flop has a common reset input and can be cleared asynchronously, and triggered on the positive going edge of the clock.

A High on the reset input clears all registers and forces the outputs ($O_0 \sim O_3$) Low, independent of the clock and data inputs.

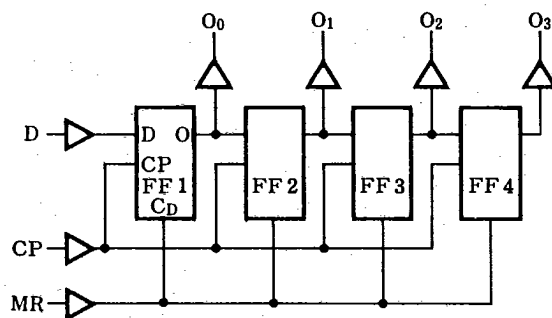
The MN4015B/S are equivalent to MOTOROLA MC14015B and RCA CD4015B.

■ Truth Table

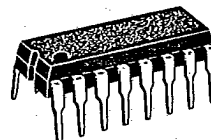
Input				Output			
n	CP	D	MR	O_0	O_1	O_2	O_3
1		D_1	L	D_1	×	×	×
2		D_2	L	D_2	D_1	×	×
3		D_3	L	D_3	D_2	D_1	×
4		D_4	L	D_4	D_3	D_2	D_1
		×	L	no change			
	×	×	H	L	L	L	L

Note) X : don't care
 D_n : High or Low
 n : Clock pulse count

■ Logic Diagram (1/2)



P-3



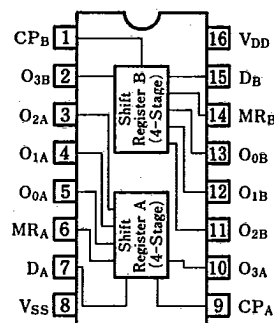
16-Pin • Plastic DIL Package

P-4



16-Pin • Panafat Package (SO-16D)

Pin Configuration



Pin Explanation

D : Data input
 CP : Clock input ()
 MR : Reset input
 $O_0 \sim O_3$: Output (4 Bits)

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■ Maximum Ratings ($T_a=25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	$-0.5 \sim +18$	V
Input Voltage	V_i	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage	V_o	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input · Output Current	$\pm I_i$	max. 10	mA
Power Dissipation (per package)	P_D	max. 400	mW
		Decrease up to 200mW rating at $8\text{mW}/^\circ\text{C}$	
Power Dissipation (per output terminal)	P_D	max. 100	mW
Operating Ambient Temperature	T_{opr}	$-40 \sim +85$	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-65 \sim +150$	$^\circ\text{C}$

* $V_{DD} + 0.5\text{V}$ should be under 18V■ DC Characteristics ($V_{SS}=0\text{V}$)

Item	V_{DD} (V)	Sym- bol	Conditions	$T_a = -40^\circ\text{C}$		$T_a = 25^\circ\text{C}$		$T_a = 85^\circ\text{C}$		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_i = V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_i = V_{SS}$ or V_{DD} $ I_o < 1\mu\text{A}$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_i = V_{SS}$ or V_{DD} $ I_o < 1\mu\text{A}$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_o < 1\mu\text{A}$ $V_o = 0.5\text{V}$ or 4.5V $V_o = 1\text{V}$ or 9V $V_o = 1.5\text{V}$ or 13.5V	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_o < 1\mu\text{A}$ $V_o = 0.5\text{V}$ or 4.5V $V_o = 1\text{V}$ or 9V $V_o = 1.5\text{V}$ or 13.5V	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_o = 0.4\text{V}, V_i = 0\text{V}$ or 5V	0.52	—	0.44	—	0.36	—	mA
	10		$V_o = 0.5\text{V}, V_i = 0\text{V}$ or 10V	1.3	—	1.1	—	0.9	—	
	15		$V_o = 1.5\text{V}, V_i = 0\text{V}$ or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_o = 4.6\text{V}, V_i = 0\text{V}$ or 5V	0.52	—	0.44	—	0.36	—	mA
	10		$V_o = 9.5\text{V}, V_i = 0\text{V}$ or 10V	1.3	—	1.1	—	0.9	—	
	15		$V_o = 13.5\text{V}, V_i = 0\text{V}$ or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_o = 2.5\text{V}, V_i = 0\text{V}$ or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_i$	$V_i = 0\text{V}$ or 15V	—	0.3	—	0.3	—	1	μA

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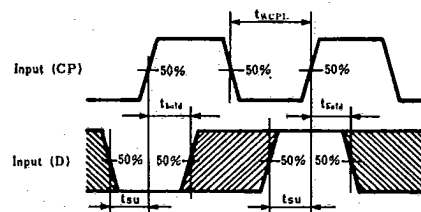
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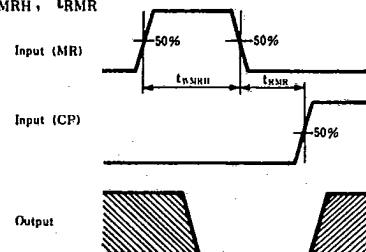
Switching Characteristics ($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$, $C_L = 50\text{pF}$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On(H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time CP→On(L→H)	5	t_{PLH}	—	120	360	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time MR→On(H→L)	5	t_{PHL}	—	185	555	ns
	10		—	70	210	
	15		—	40	120	
Set-up Time (Fig. 1) D→CP	5	t_{su}	—	55	166	ns
	10		—	15	45	
	15		—	10	30	
Hold Time (Fig. 1) D→CP	5	t_{hold}	—	20	60	ns
	10		—	10	30	
	15		—	8	24	
(Fig. 1) Minimum Clock Pulse Width	5	t_{WCPI}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
(Fig. 2) Minimum Reset Pulse Width	5	t_{WMRH}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time (Fig. 2)	5	t_{RMR}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Maximum Clock Frequency	5	f_{max}	4	9	—	MHz
	10		12	23	—	
	15		17	34	—	
Input Capacitance		C_i	—	—	7.5	pF

• Dynamic Signal Waveforms

(Fig. 1) t_{su} , t_{hold} , t_{WCPI} .

Waveforms showing set-up times, hold times and minimum clock pulse width

(Fig. 2) t_{WMRH} , t_{RMR} 

Waveforms showing recovery time for MR and minimum MR pulse width