V61C31161024
64K x 16 HIGH SPEED STATIC RAM

PRELIMINARY INFORMATION

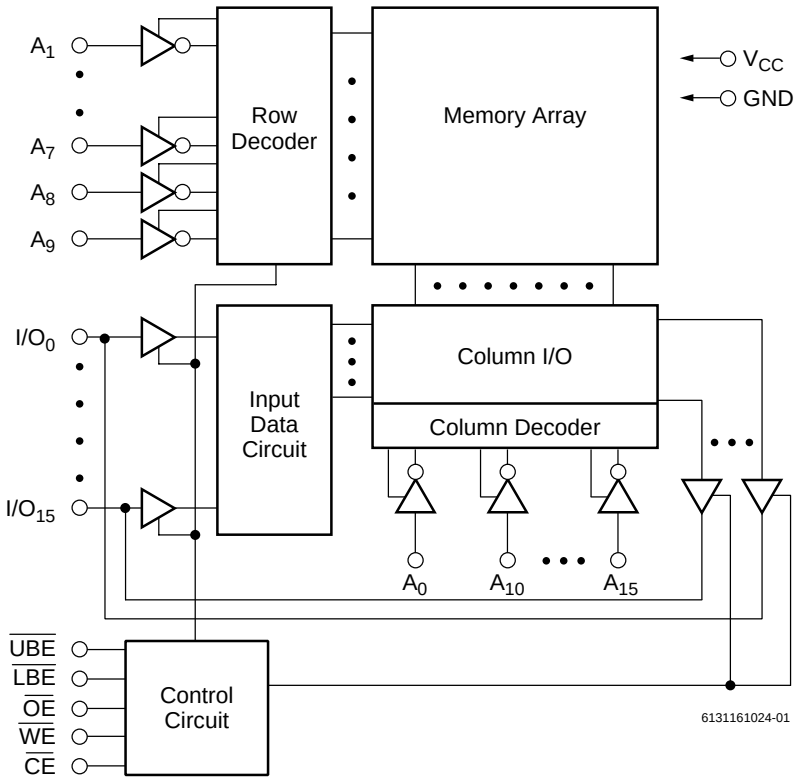
Features

- High-speed: 10, 12, 15 ns
- All inputs and outputs directly TTL compatible
- Three state outputs
- Single 3.3V ± 10% Power Supply
- Packages
  - 44-pin TSOP (Standard)
  - 44-pin 400 mil SOJ
- Low Power Consumption
  - Active: 140mA
  - Standby: 2mA (CMOS)

Description

The V61C31161024 is a 1,048,576-bit static random-access memory organized as 65,536 words by 16 bits. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Temperature Mark
	T	K	10	12	15	
0°C to 70 °C	•	•	•	•	•	Blank

Pin Descriptions

A_0–A_{15} Address Inputs
These 16 address inputs select one of the 64K x 16 bit segments in the RAM.

$\overline{CE}$ Chip Enable Input
$\overline{CE}$ is active LOW. It must be active to read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when deselected.

$\overline{OE}$ Output Enable Input
The output enable input is active LOW. When $\overline{OE}$ is Low with $\overline{CE}$ Low and $\overline{WE}$ High, data will be presented on the I/O pins. The I/O pins will be in the high impedance state when $\overline{OE}$ is High.

$\overline{UBE}$, $\overline{LEB}$ Byte Enable
Active low inputs. These inputs are used to enable the upper or lower data byte.

$\overline{WE}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present at the I/O pins; when $\overline{WE}$ is LOW and $\overline{OE}$ is HIGH, the data present on the I/O pins will be written into the selected memory locations.

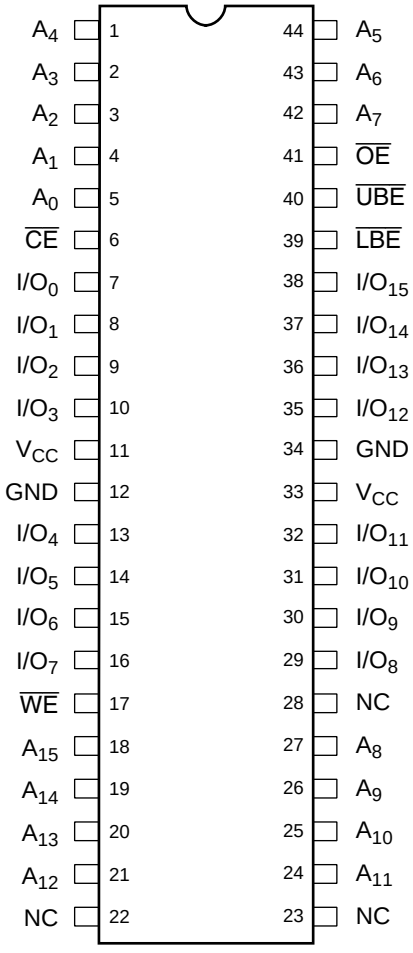
I/O_0–I/O_{15} Data Input and Data Output Ports
These 16 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

GND Ground

Pin Configurations (Top View)

44-Pin SOJ



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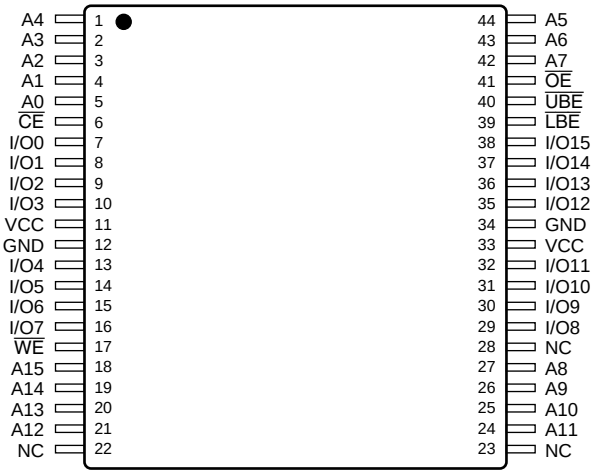
44-Pin TSOP-II (Standard)



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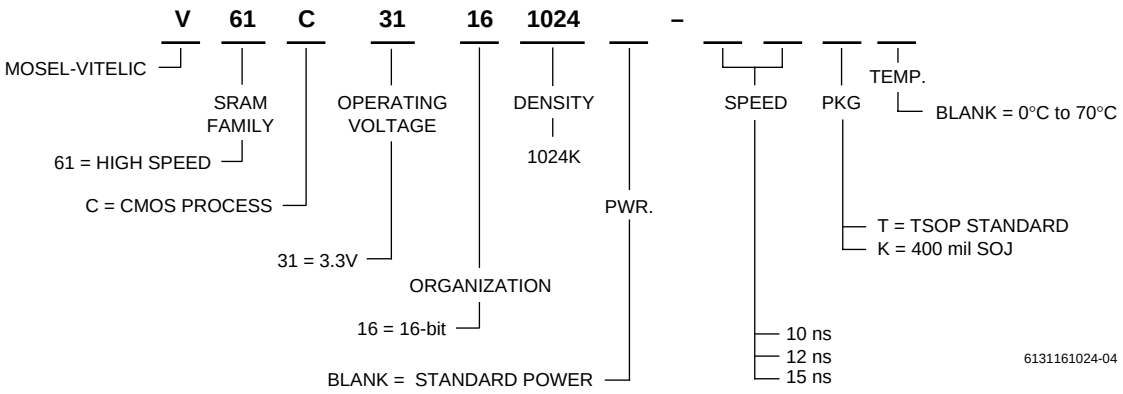
Part Number Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Units
V_{IN}	Input Voltage	-0.5 to V_{CC}+0.5	V
P_T	Power Dissipation	1.0	W
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-65 to +150	°C

NOTE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance* T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:
1. This parameter is guaranteed and not tested.

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{UBE}$	$\overline{LBE}$	I/O_{8-15} Operation	I/O_{0-7} Operation
Standby	H	X	X	X	X	High Z	High Z
Output Disable	L	X	X	H	H	High Z	High Z
Output Disable	L	H	H	X	X	High Z	High Z
Read	L	L	H	L	L	D_{OUT}	D_{OUT}
Read	L	L	H	L	H	D_{OUT}	High Z
Read	L	L	H	H	L	High Z	D_{OUT}
Write	L	X	L	L	L	D_{IN}	D_{IN}
Write	L	X	L	L	H	D_{IN}	High Z
Write	L	X	L	H	L	High Z	D_{IN}

NOTE:
X = Don't Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, V_{CC} = 3.3V ± 10%)

Symbol	Parameter	Test Conditions	-10		-12		-15		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current	V_{CC} = MAX, V_{IN} = GND to V_{CC}	—	5	—	5	—	5	µA
I_{OL}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}	—	5	—	5	—	5	µA
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0, f = f_{max}	—	140	—	130	—	120	mA
ISB	Standby Power Supply Current (TTL Level)	$\overline{CE}$ = V_{IH}, f = f_{max}	—	25	—	20	—	20	mA
I_{SB1}	Standby Power Supply Current (CMOS Level)	$\overline{CE}$ ≥ V_{CC} – 0.2V, f = 0, V_{IN} ≤ 0.2V or V_{IN} > V_{CC} – 0.2V	—	2	—	2	—	2	mA
V_{IL}	Input Low Voltage(1,2)		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}	Input High Voltage(1)		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	2.4	—	2.4	—	2.4	—	V

NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -3.0V for pulse width < 20ns.
3. $f_{MAX} = 1/t_{RC}$.
4. Maximum values.

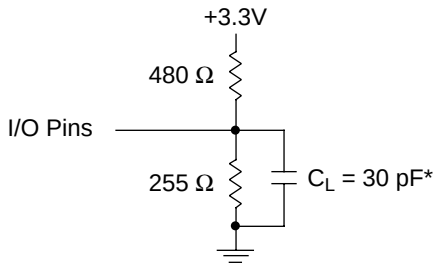
AC Test Conditions

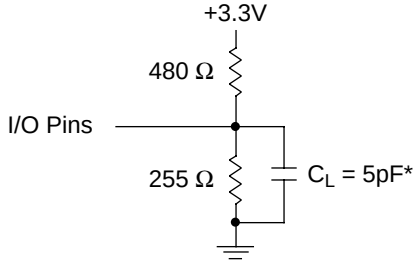
Input Pulse Levels	0 to 3V
Input Rise and Fall Times	3 ns
Timing Reference Levels	1.5V
Output Load	see below

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms





for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{WHZ}, t_{OW}, and t_{OHZ}

* Includes scope and jig capacitance

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AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

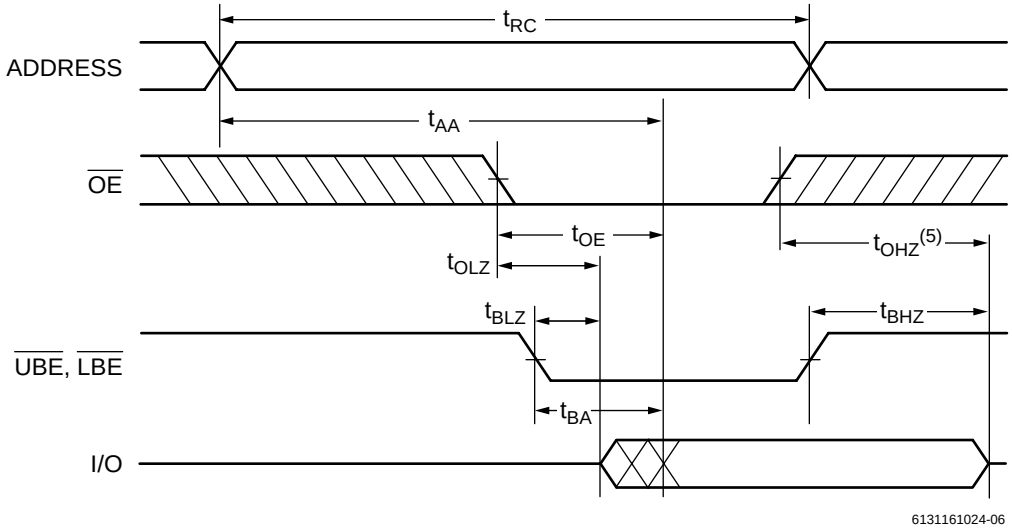
Parameter Name	Parameter	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Enable Access Time	—	10	—	12	—	15	ns
t_{BA}	$\overline{UBE}$, $\overline{LBE}$ Access Time	—	5	—	6	—	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{CLZ}	Chip Enable to Output in Low Z	2	—	3	—	3	—	ns
t_{BLZ}	$\overline{UBE}$, $\overline{LBE}$ to Output in Low Z	0	—	0	—	0	—	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}	Chip Disable to Output in High Z	0	5	0	6	0	7	ns
t_{OHZ}	Output Disable to Output in High Z	0	5	0	6	0	7	ns
t_{BHZ}	$\overline{UBE}$, $\overline{LBE}$ to Output in High Z	0	5	0	6	0	7	ns
t_{OH}	Output Hold from Address Change	2	—	3	—	3	—	ns

Write Cycle

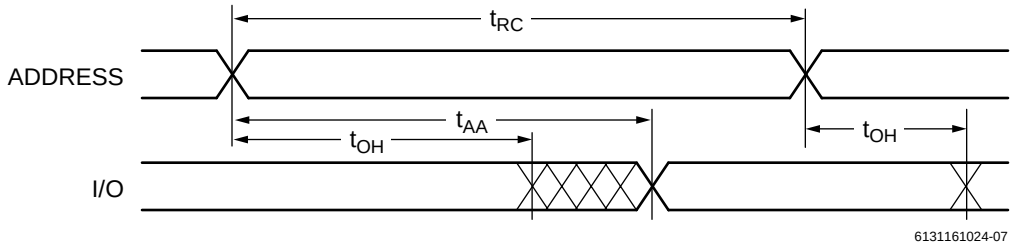
Parameter Name	Parameter	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{CW}	Chip Enable to End of Write	7	—	8	—	10	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	10	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	10	—	ns
t_{AH}	Address Hold from End of Write	0	—	0	—	0	—	ns
t_{WHZ}	Write to Output High-Z	0	5	0	6	0	7	ns
t_{WLZ}	Write to Output Low Z	3	—	3	—	5	—	ns
t_{DW}	Data Setup to End of Write	5	—	6	—	7	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	0	—	ns
t_{BW}	$\overline{UBE}$, $\overline{LBE}$ to End of Write	7	—	8	—	10	—	ns

Switching Waveforms (Read Cycle)

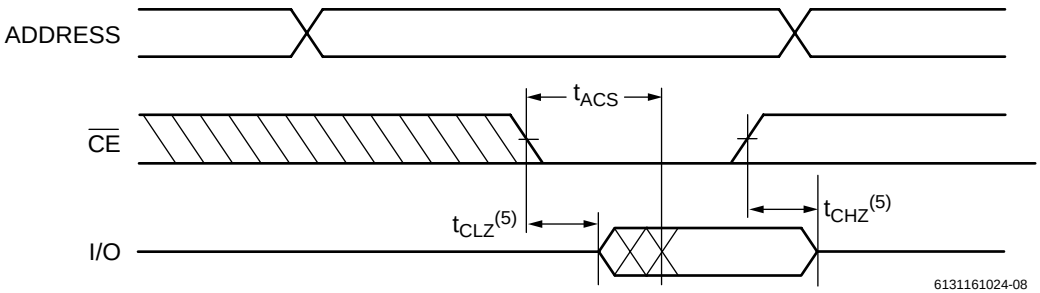
Read Cycle 1(1, 2)



Read Cycle 2(1, 2, 4)



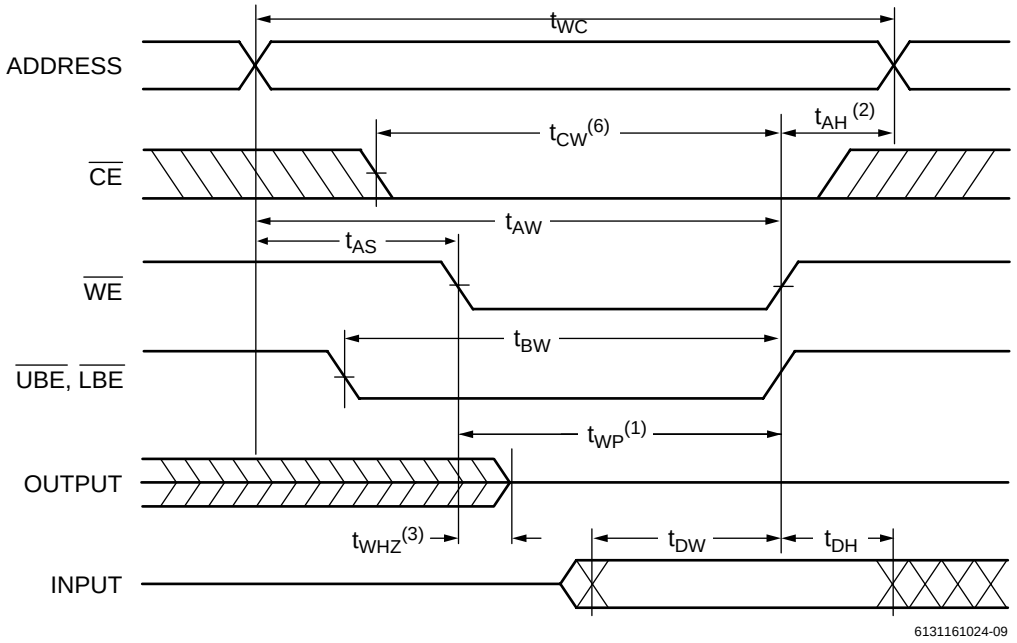
Read Cycle 3(1, 3, 4)



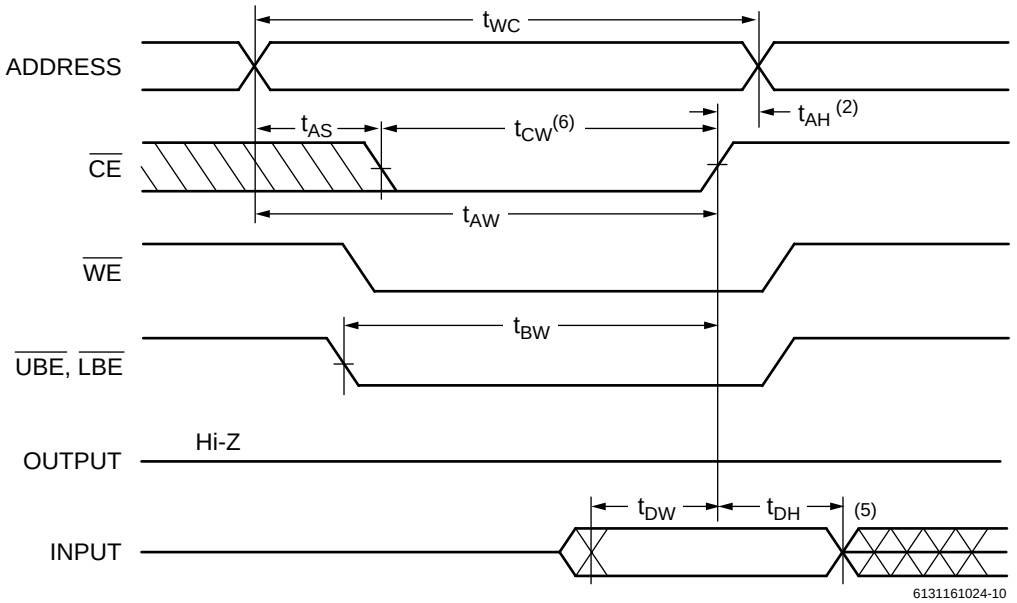
NOTES:
1. $\overline{WE} = V_{IH}$.
2. $\overline{CE}_1 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.
6. $\overline{UBE} = V_{IL}$, $\overline{LBE} = V_{IL}$.

Switching Waveforms (Write Cycle)

Write Cycle 1 ($\overline{WE}$ Controlled)[4]



Write Cycle 2 ($\overline{CE}$ Controlled)[4]

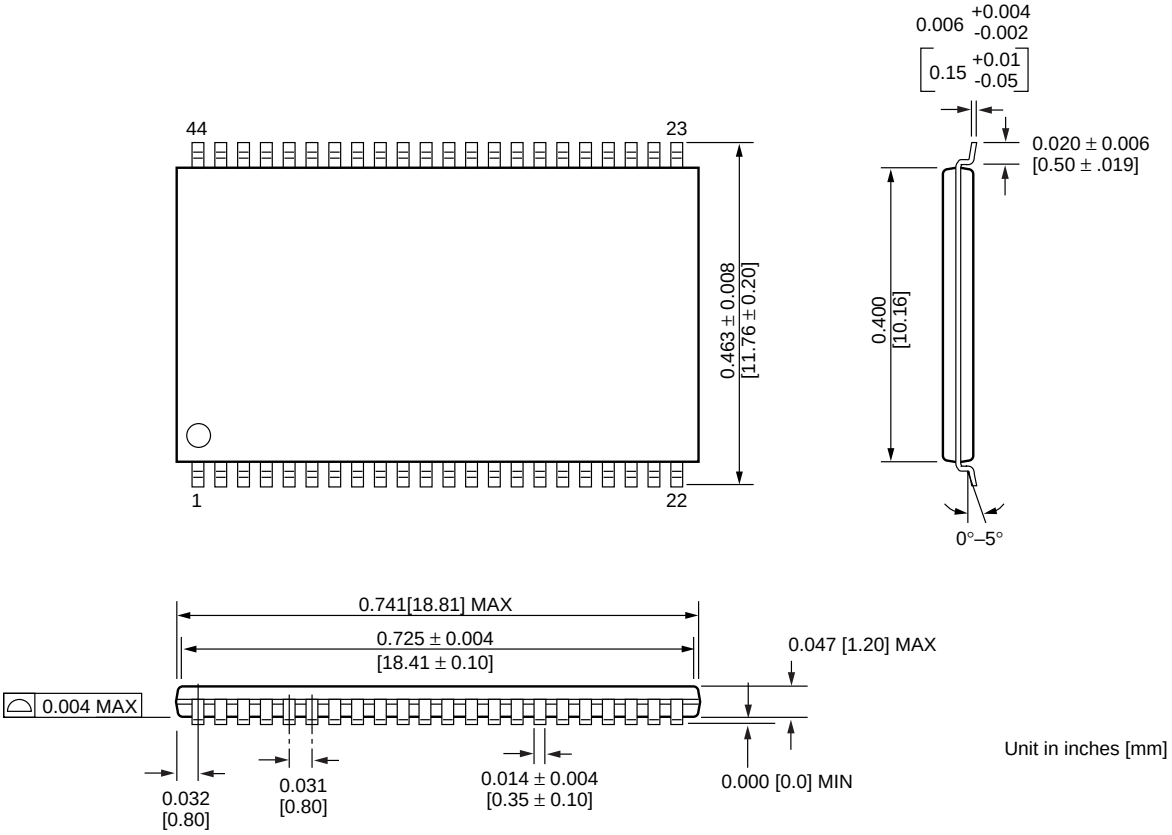


NOTES:

1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{AH} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE}$ = V_{IL} or V_{IH}. However it is recommended to keep $\overline{OE}$ at V_{IH} during write cycle to avoid bus contention.
5. If $\overline{CE}$ is LOW during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from $\overline{CE}$ going low to the end of write.

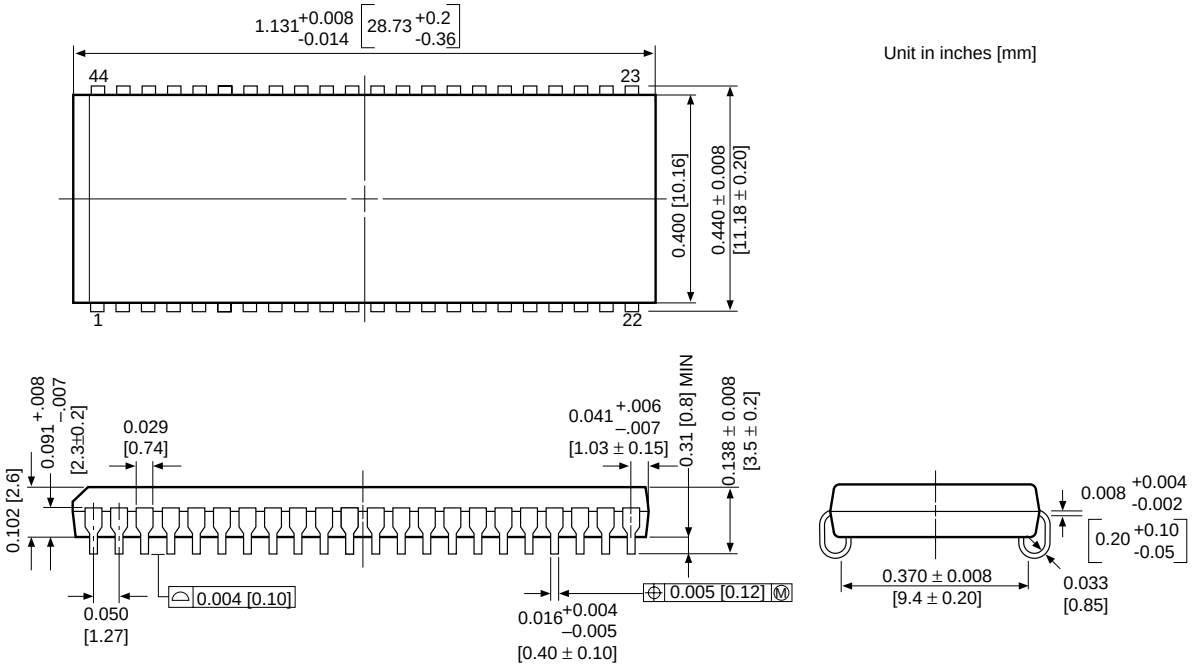
Package Diagrams

44-pin 400 mil TSOP-II



Package Diagrams

44-pin 400 mil SOJ (450 mil pin-to-pin)



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