M66014FP

16-bit Serial Bus Controller

REJ03F0265-0200
Rev.2.00
Mar 18, 2008

Description

M66014 semiconductor integrated circuit is a serial bus controller. It converts 2-byte parallel data that arrives from microcomputer into serial and outputs it to serial bus. It also converts serial data input from serial bus into parallel and outputs it to microcomputer.

The M66014 is used for the extension of microcomputer I/O ports and two-way communication with peripheral equipment connected with serial buses.

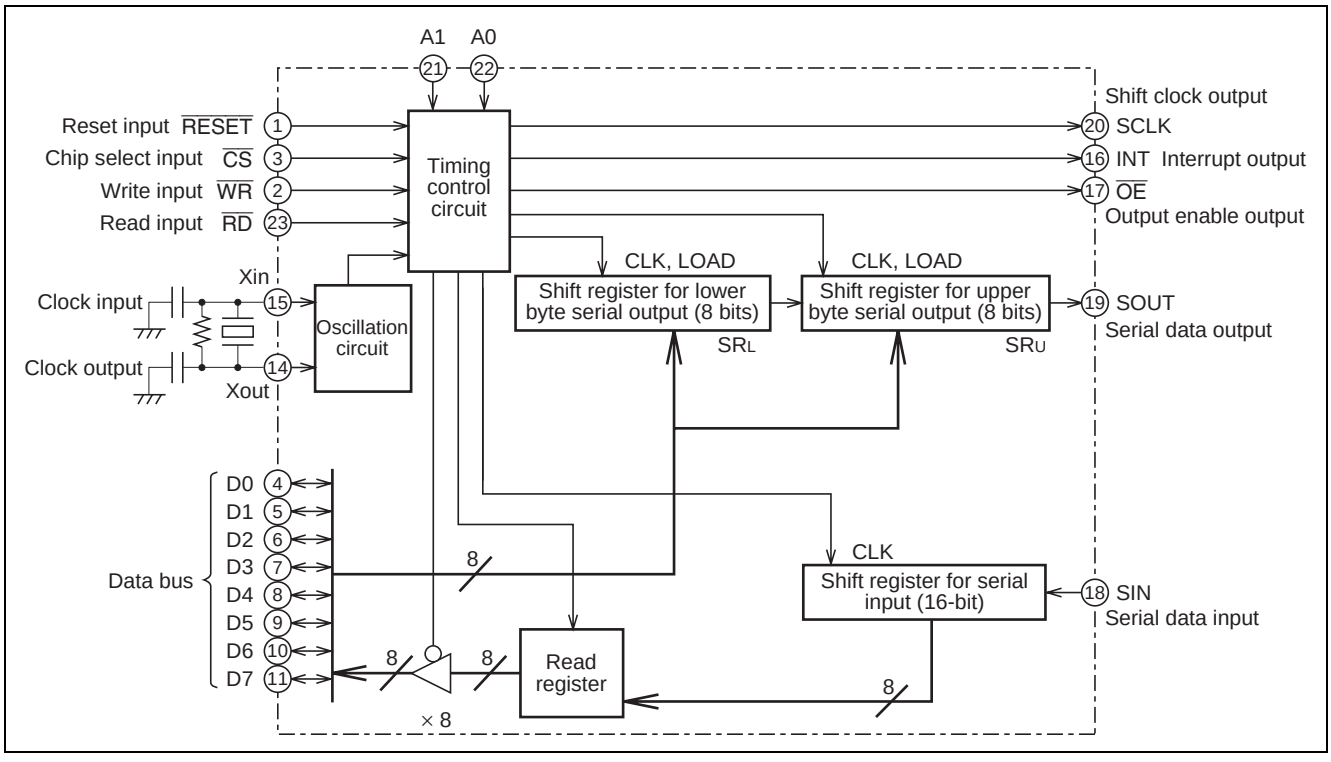
Features

- Compatible with general-purpose 8-bit microprocessor busses
- TTL level input (one microcomputer side)
- Interrupt output
- Schmitt input ($\overline{\text{RESET}}$, $\overline{\text{CS}}$, SIN)
- Pin arrangement is fully compatible with M66011FP
- Low power dissipation
- Wide operating temperature range (Ta = –20 to 75°C)

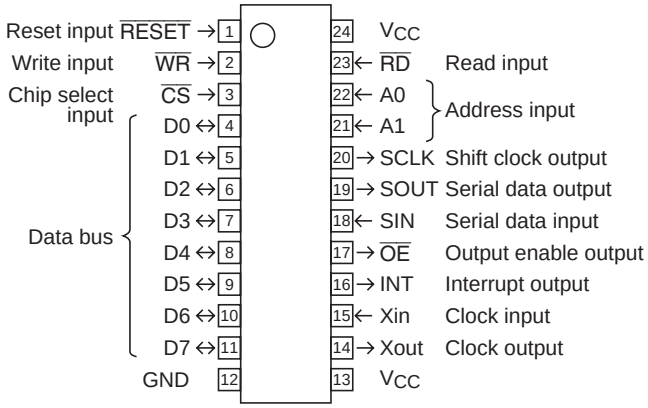
Application

Microcomputer I/O port extension, etc.

Block Diagram



Pin Arrangement



(Top view)

Outline: 24P2N-B

Serial Data Input/Output Operation

A cycle of 16-bit serial output data setting and serial data communication starts with a write access given by microcomputer to transmission shift registers in M66014.

M66014 has two 8-bit shift registers, on for upper byte (SR_U), the other for lower byte (SR_L). If the $\overline{CS}$ status rises from "L" to "H" after a write access is given to SR_L, serial data communication is started. SR_U 8-bit data and SR_L 8-bit data are output in series in this order. Output of each data starts from its most significant bit.

At the $\overline{CS}$ rise edge, busy flag in M66014 is set, and $\overline{OE}$ output shifts from "H" to "L". Shift clock SCLK and serial data SOUT are then output.

At SCLK fall edges, serial output shift register executes shifting operation, and data on shift register is output in series from pin SOUT. Serial input data from pin SIN is taken into input shift register at SCLK rise edges.

After the SCLK 16T rise edge, the status of SOUT and $\overline{OE}$ shifts to "H" after one bit's delay of SCLK, and busy flag is reset. When interrupt output is being set to enable, INT output is set.

Remarks

(1) If $\overline{CS}$ rises after write operation is executed on SR_L only and not on SR_U, SR_U data is unstable.
(2) When write operations executed on SR_L, M66014 becomes ready for start of serial communication and stands by for detection of $\overline{CS}$ rise. However, if a read access is given after data is written on SR_L while $\overline{CS}$ is maintained on "L" level, this standby status is canceled. To resume serial communication in this case, rewrite data on SR_L and raise $\overline{CS}$.

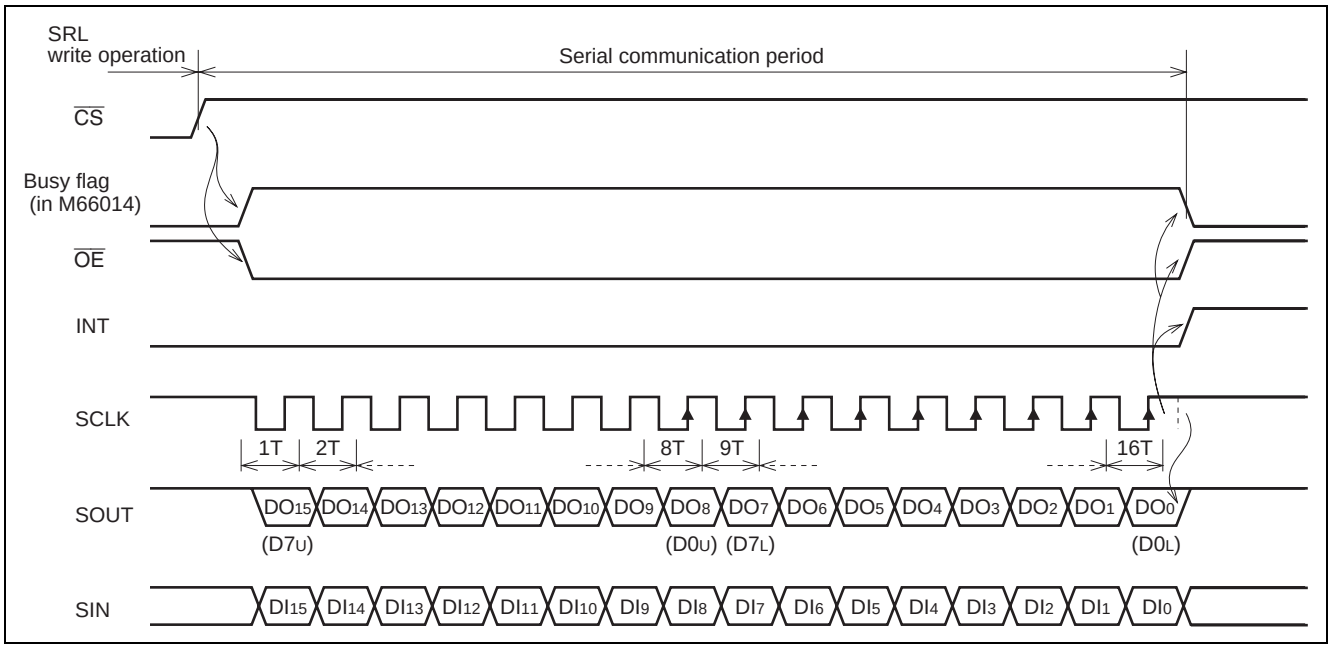


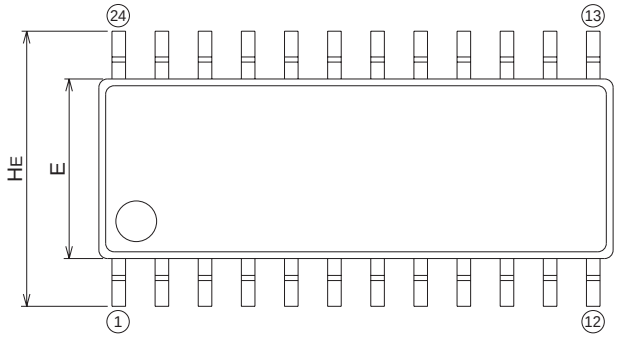
Figure 1 Serial Communication Timing Chart

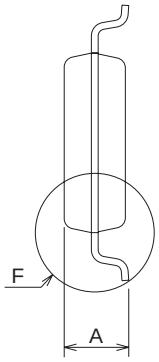
Package Dimensions

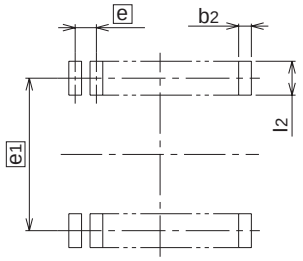
24P2N-B

Plastic 24pin 300mil SOP

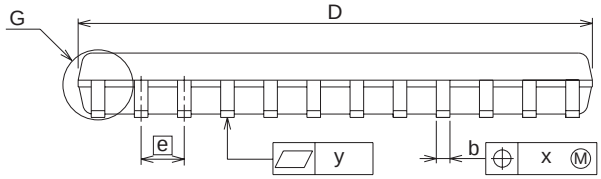
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP24-P-300-1.27	—		Cu Alloy

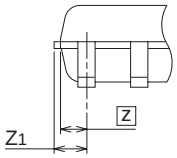




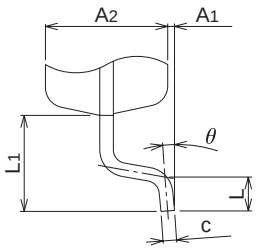


Recommended Mount Pad





Detail G



Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A_1	0	0.1	0.2
A_2	—	1.8	—
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	14.92	15.02	15.12
E	5.2	5.3	5.4
e	—	1.27	—
H_E	7.82	8.12	8.42
L	0.3	0.5	0.7
L_1	—	1.41	—
z	—	0.525	—
Z_1	—	—	0.675
x	—	—	0.25
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.76	—
e_1	—	7.62	—
l_2	1.27	—	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
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Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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