- **Outstanding Combination of DC Precision and AC Performance:**
  Unity-Gain Bandwidth . . . 15 MHz Typ
  V_n . . . 3.3 nV/$\sqrt{Hz}$ at f = 10 Hz Typ,
  2.5 nV/$\sqrt{Hz}$ at f = 1 kHz Typ
  V_{IO} . . . 100 µV Typ
  A_{VD} . . . 45 V/µV Typ With R_L = 2 kΩ,
  38 V/µV Typ With R_L = 1 kΩ
- **Available in 16-Pin Small-Outline Wide-Body Package**
- **Macromodels and Statistical Information Included**
- **Output Features Saturation Recovery Circuitry**

description

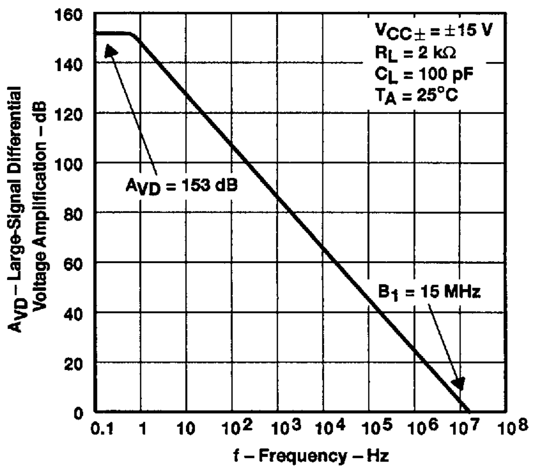
The TLE2227C combines innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in dual operational amplifiers. This device allows upgrades to systems that use lower-precision devices and is manufactured using Texas Instruments state-of-the-art Excalibur process.

In the area of dc precision, the TLE2227C offers a typical offset voltage of 100 µV, a common-mode rejection ratio of 115 dB (typ), a supply voltage rejection ratio of 120 dB (typ), and a dc gain of 45 V/µV (typ).

The ac performance is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{Hz}$ and 2.5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz and 1 kHz, respectively.

The TLE2227C is available in a wide variety of packages, including the industry standard 16-pin small-outline wide-body version for high-density system applications. This device is characterized for operation from 0°C to 70°C.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

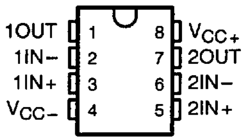


AVAILABLE OPTIONS

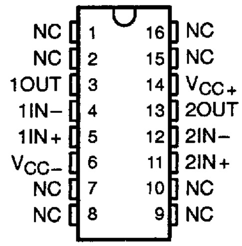
T_A	V_{IO}typ AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (DW)	PLASTIC DIP (P)	
0°C to 70°C	100 µV	TLE2227CDW	TLE2227CP	TLE2227Y

The DW package is available taped and reeled. Add R suffix to device type (e.g., TLE2227CDWR).

P PACKAGE
(TOP VIEW)

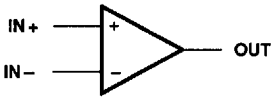


DW PACKAGE
(TOP VIEW)



NC – No internal connection

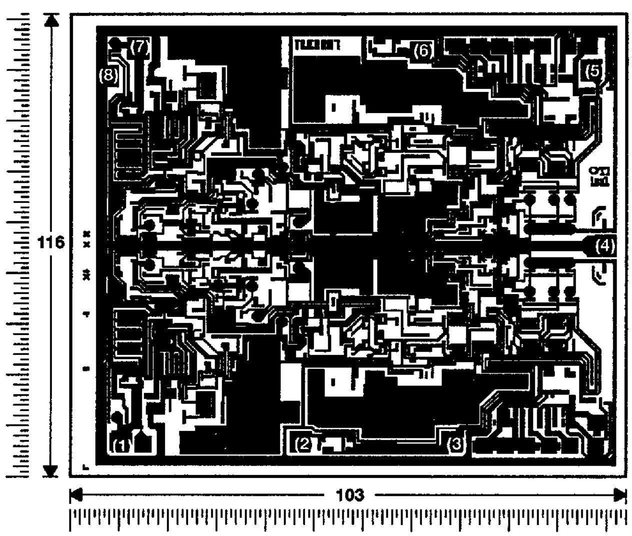
symbol (each amplifier)

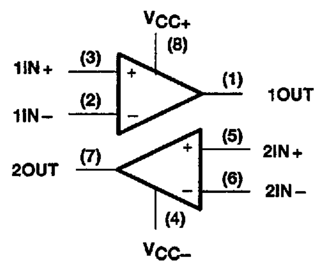


TLE2227Y chip information

This chip, properly assembled, displays characteristics similar to the TLE2227C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips my be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

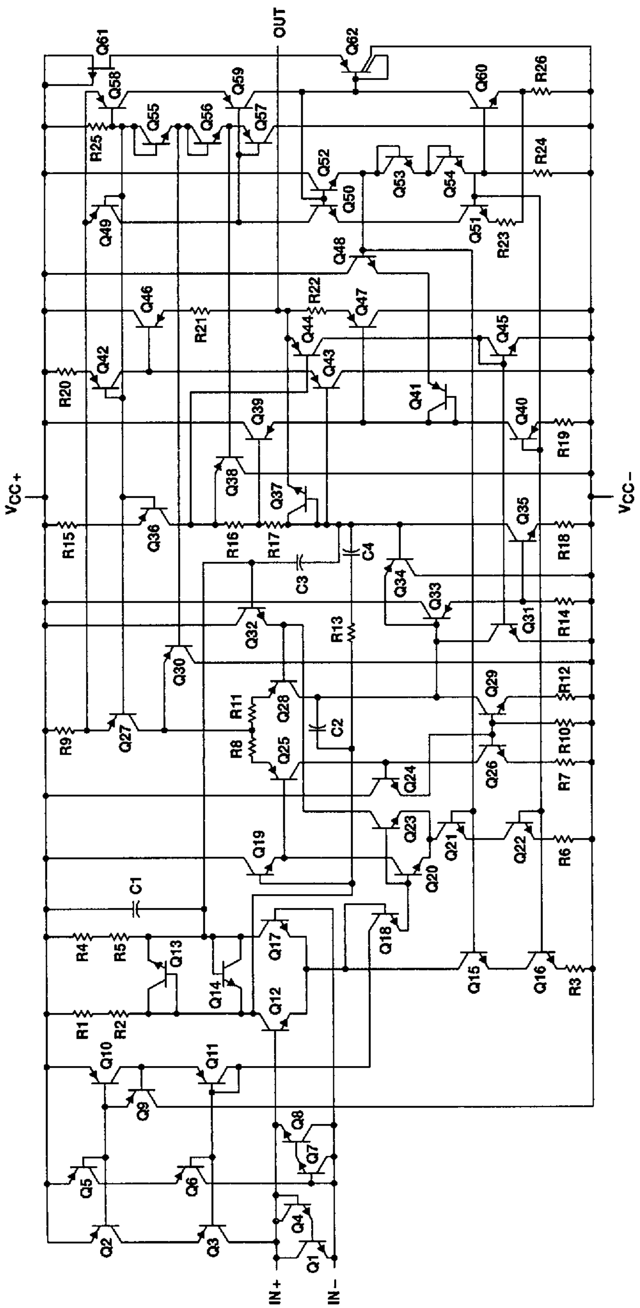
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	62
Diodes	0
Resistors	24
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) .... 19 V
Supply voltage, V_{CC-} .... −19 V
Differential input voltage, V_{ID} (see Note 2) .... ±1.2 V
Input voltage range, V_I (any input) .... $V_{CC\pm}$
Input current, I_I (each input) .... ±1 mA
Output current, I_O .... ±50 mA
Total current into V_{CC+} .... 50 mA
Total current out of V_{CC-} .... 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A .... 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4	±19	V
Common-mode input voltage, V_{IC}	$T_A = 25°C$		±11	V
	T_A = Full range†		±10.5	
Operating free-air temperature, T_A		0	70	°C

† Full range is 0°C to 70°C.

8961724 0094379 802

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2227C MIN	TLE2227C TYP	TLE2227C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		25°C		100	350	µV
				Full range			500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		0.4	1	µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.006	1	µV/mo
I_{IO}	Input offset current			25°C		7.5	90	nA
				Full range			150	
I_{IB}	Input bias current			25°C		15	90	nA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C	−11 to 11	−13 to 13		V
				Full range	−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 1\ k\Omega$		25°C	10.5			V
				Full range	10			
		$R_L = 2\ k\Omega$		25°C	12			
				Full range	11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 1\ k\Omega$		25°C	−10.5	−13		V
				Full range	−10			
		$R_L = 2\ k\Omega$		25°C	−12	−13.5		
				Full range	−11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V,	$R_L = 2\ k\Omega$	25°C	2.5	45		V/µV
		$V_O = \pm10$ V,	$R_L = 2\ k\Omega$	Full range	2			
		$V_O = \pm10$ V,	$R_L = 1\ k\Omega$	25°C	3.5	38		
				Full range	1			
c_i	Input capacitance			25°C		8		pF
z_o	Open-loop output impedance	$I_O = 0$		25°C		50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min,	$R_S = 50\ \Omega$	25°C	98	115		dB
				Full range	95			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V,	$R_S = 50\ \Omega$	25°C	94	120		dB
		$V_{CC\pm} = \pm4$ V to ±18 V,	$R_S = 50\ \Omega$	Full range	92			
I_{CC}	Supply current	$V_O = 0$,	No load	25°C		7.3	10.6	mA
				Full range			11.2	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2227C MIN	TLE2227C TYP	TLE2227C MAX	UNIT
SR	Slew rate	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C	1.7	2.5		V/μs
			Full range	1.2			
V_n	Equivalent input noise voltage	$R_S = 20$ Ω, f = 10 Hz	25°C		3.3	8	nV/√HZ
		$R_S = 20$ Ω, f = 1 kHz			2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4	pA/√HZ
		f = 1 kHz			0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm10$ V, $A_{VD} = 1$, See Note 5	25°C		<0.002%		
B_1	Unity-gain bandwidth	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C	7	13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	25°C		30		kHz
ϕ_m	Phase margin	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C		40°		

† Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis is 0.002%.

electrical characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise noted)

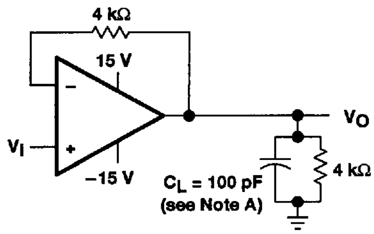
PARAMETER		TEST CONDITIONS		TLE2227Y MIN	TLE2227Y TYP	TLE2227Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		100	350	µV
	Input offset voltage long-term drift (see Note 4)				0.006	1	µV/mo
I_{IO}	Input offset current				7.5	90	nA
I_{IB}	Input bias current				15	90	nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		−11 to 11	−13 to 13		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 1\ k\Omega$		10.5			V
		$R_L = 2\ k\Omega$		12			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 1\ k\Omega$		−10.5	−13		V
		$R_L = 2\ k\Omega$		−12	−13.5		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V,	$R_L = 2\ k\Omega$	2.5	45		V/µV
		$V_O = \pm10$ V,	$R_L = 1\ k\Omega$	3.5	38		
c_i	Input capacitance				8		pF
z_o	Open-loop output impedance	$I_O = 0$			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$,	$R_S = 50\ \Omega$	98	115		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V,	$R_S = 50\ \Omega$	94	120		dB
I_{CC}	Supply current	$V_O = 0$,	No load		7.3	10.6	mA

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TLE2227Y MIN	TLE2227Y TYP	TLE2227Y MAX	UNIT
SR	Slew rate	$R_L = 2\ k\Omega$,	$C_L = 100$ pF	1.7	2.5		V/µs
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$,	f = 10 Hz		3.3	8	nV/√HZ
		$R_S = 20\ \Omega$,	f = 1 kHz		2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			50	250	nV
I_n	Equivalent input noise current	f = 10 Hz			1.5	4	pA/√HZ
		f = 1 kHz			0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm10$ V, $A_{VD} = 1$,	See Note 5		<0.002%		
B_1	Unity-gain bandwidth	$R_L = 2\ k\Omega$,	$C_L = 100$ pF	7	13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\ k\Omega$			30		kHz
ϕ_m	Phase margin	$R_L = 2\ k\Omega$,	$C_L = 100$ pF		40°		

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5 Measured distortion of the source used in the analysis is 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

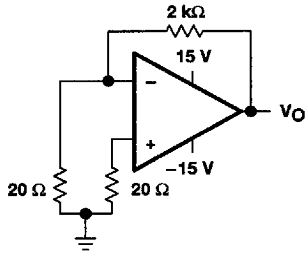
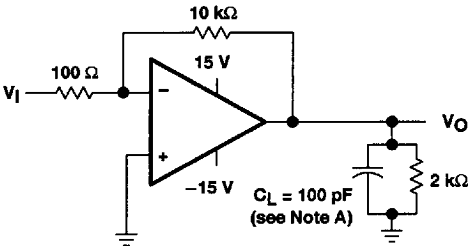
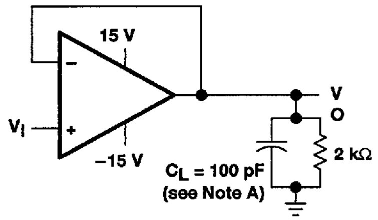


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
ΔV_{IO}	Input offset voltage change	vs Time after power on	6, 7
I_{IO}	Input offset current	vs Free-air temperature	8
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	9 10
I_I	Input current	vs Differential input voltage	11
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	12
V_{OM}	Maximum peak output voltage	vs Load resistance vs Free-air temperature	13, 14 15, 16
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	17 19 18, 20 21
z_o	Output impedance	vs Frequency	22
CMRR	Common-mode rejection ratio	vs Frequency	23
k_{SVR}	Supply voltage rejection ratio	vs Frequency	24
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	25, 26 27, 28 29, 30
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	31 32
	Pulse response	Small signal Large signal	33 34
V_n	Equivalent input noise voltage	vs Frequency	35
	Noise voltage (referred to input)	vs Time	36
B_1	Unity-gain bandwidth	vs Supply voltage vs Load capacitance	37 38
SR	Slew rate	vs Free-air temperature	39
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance	40 41
	Phase shift	vs Frequency	18, 20

TYPICAL CHARACTERISTICS†

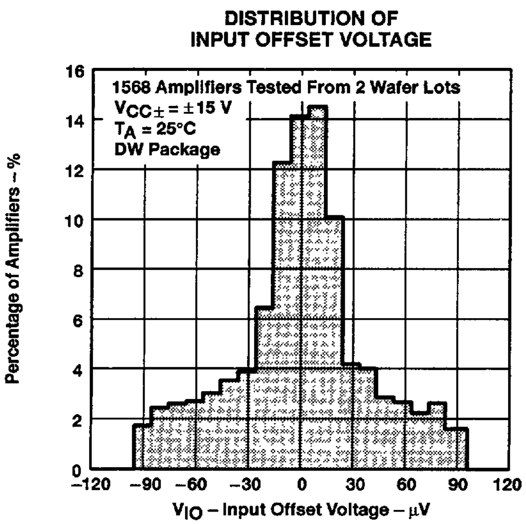


Figure 5

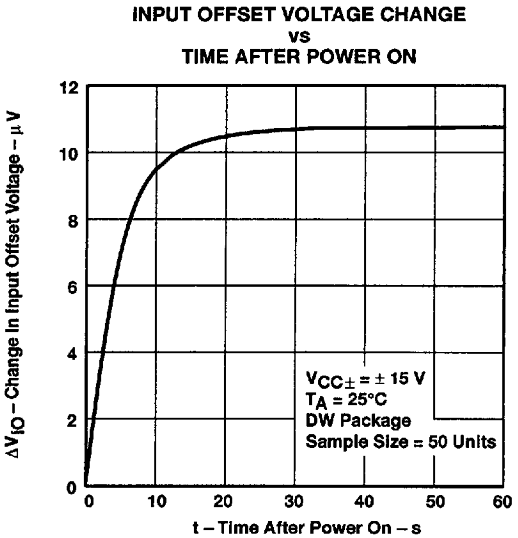


Figure 6

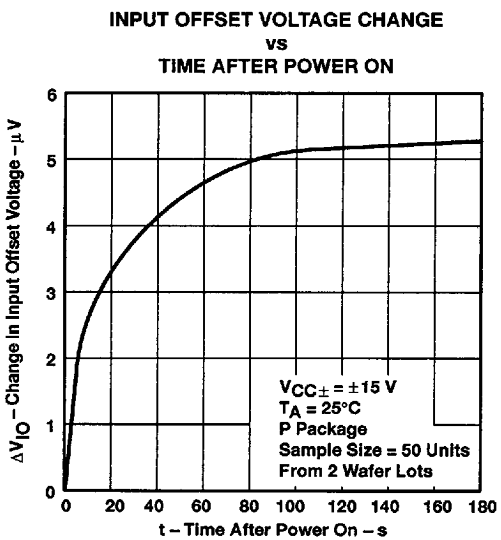


Figure 7

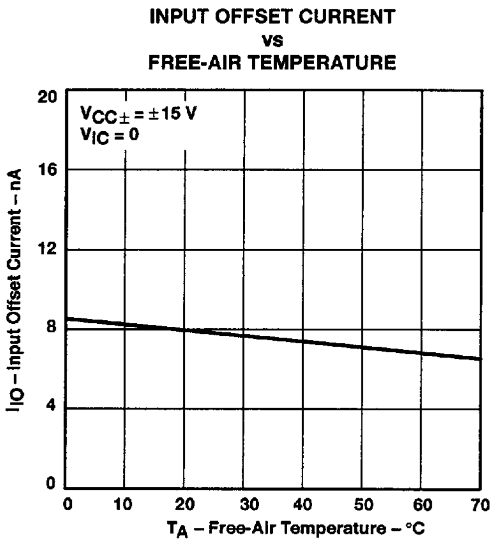


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

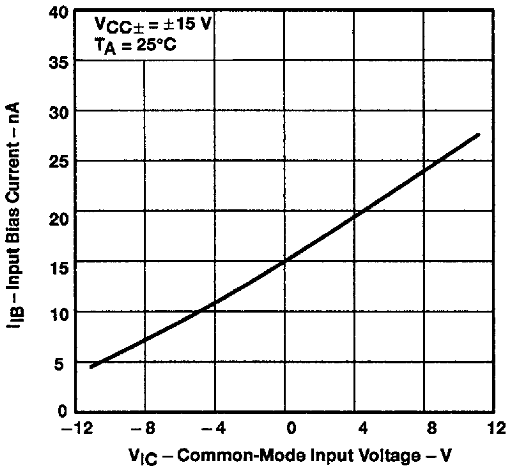


Figure 9

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

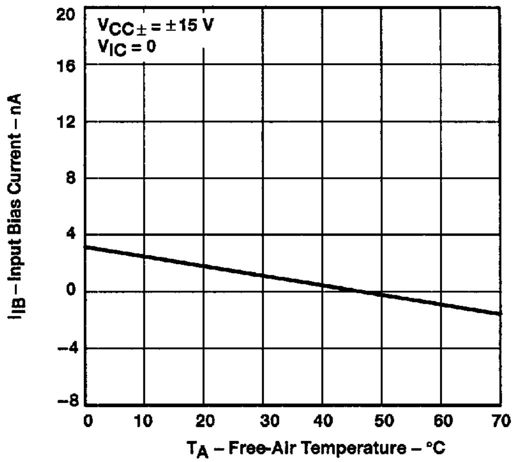


Figure 10

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

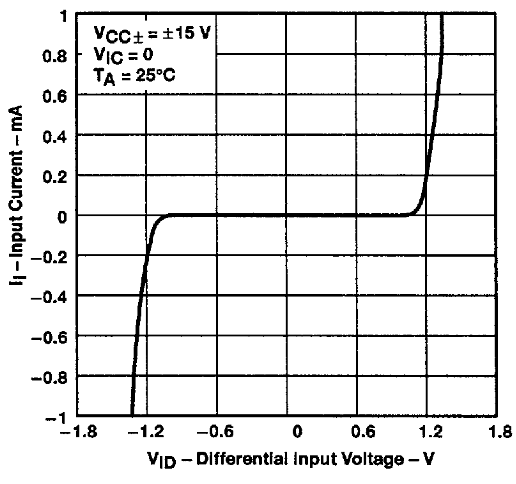


Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

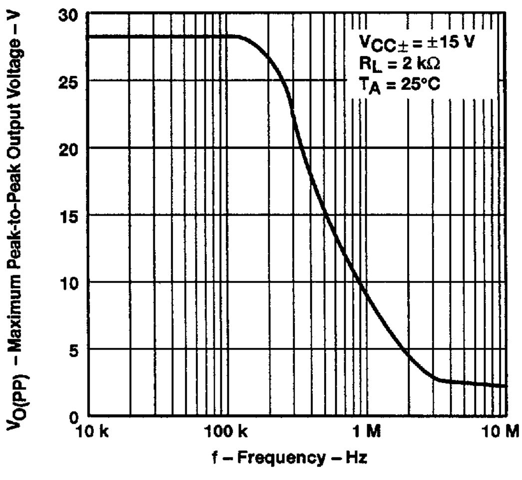


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

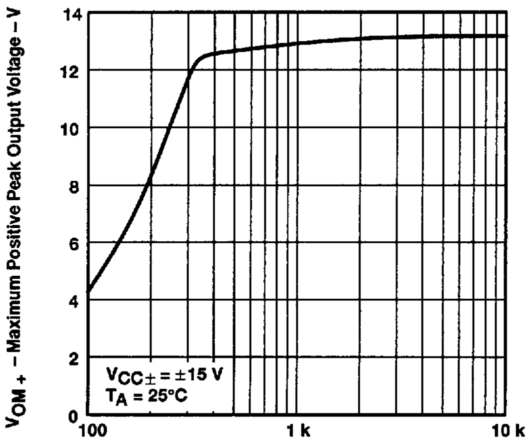


Figure 13

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

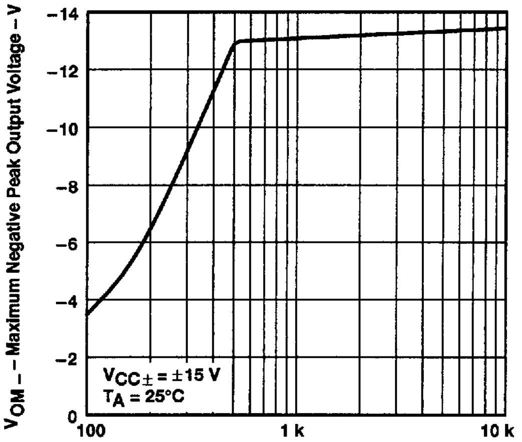


Figure 14

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

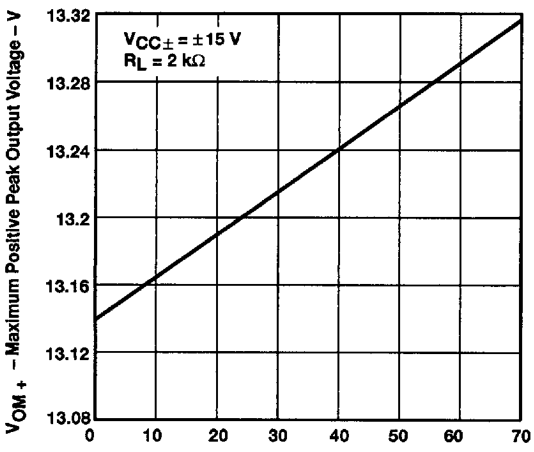


Figure 15

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

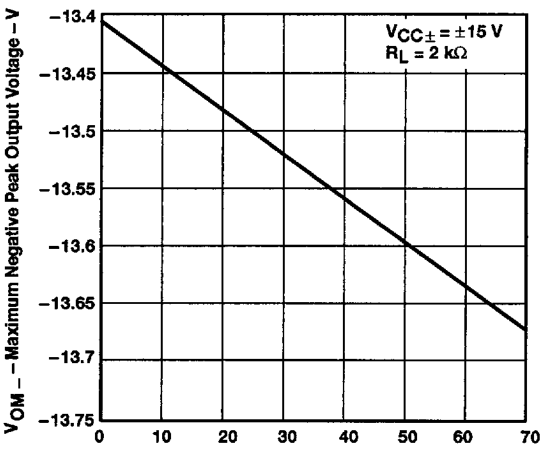


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

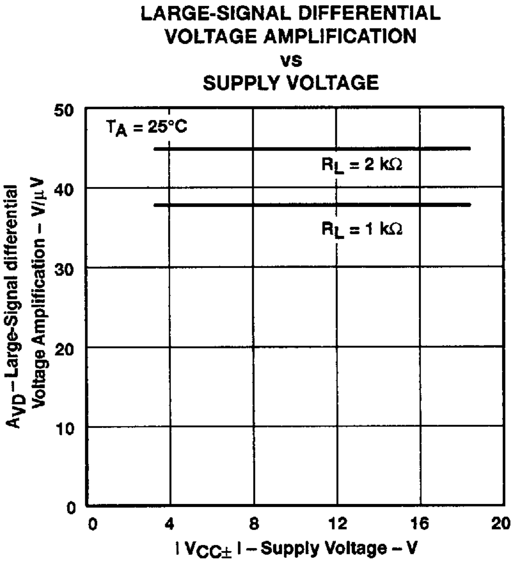


Figure 17

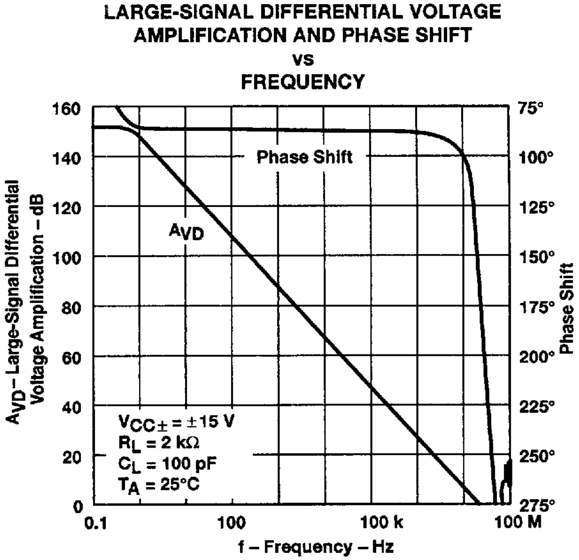


Figure 18

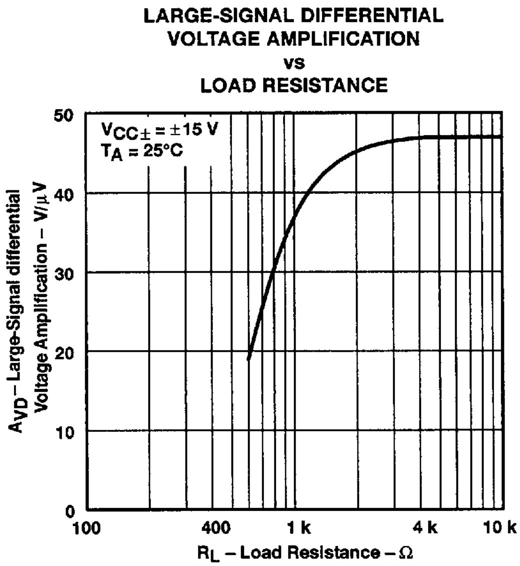


Figure 19

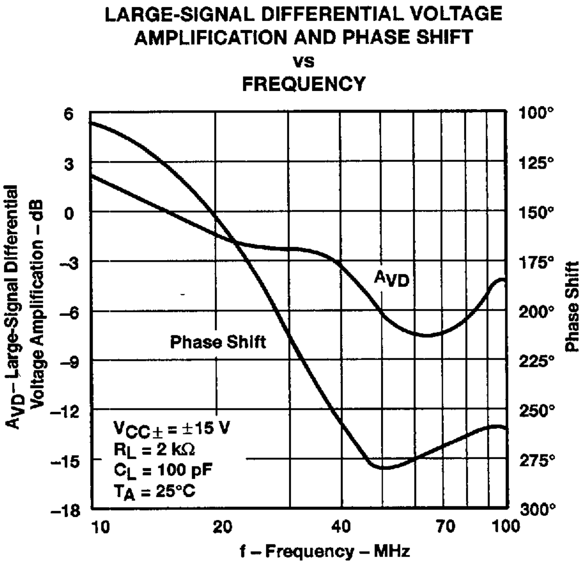


Figure 20

TYPICAL CHARACTERISTICS†

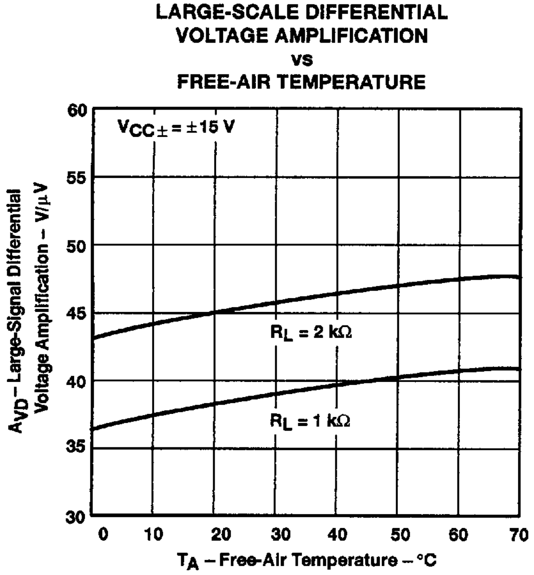


Figure 21

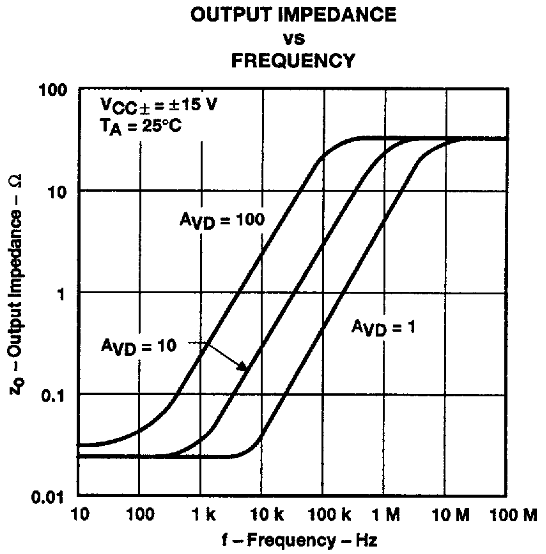


Figure 22

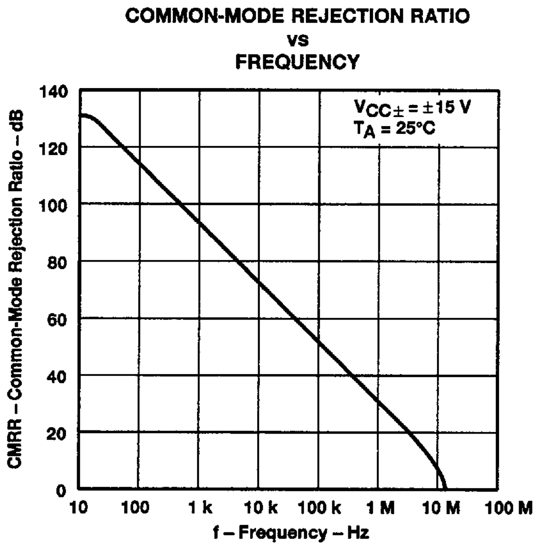


Figure 23

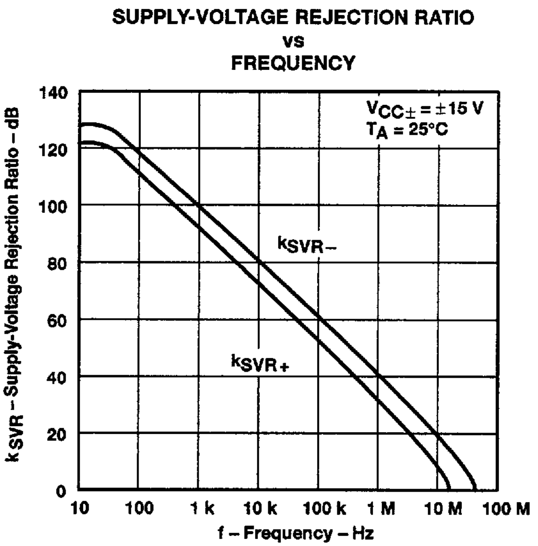


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

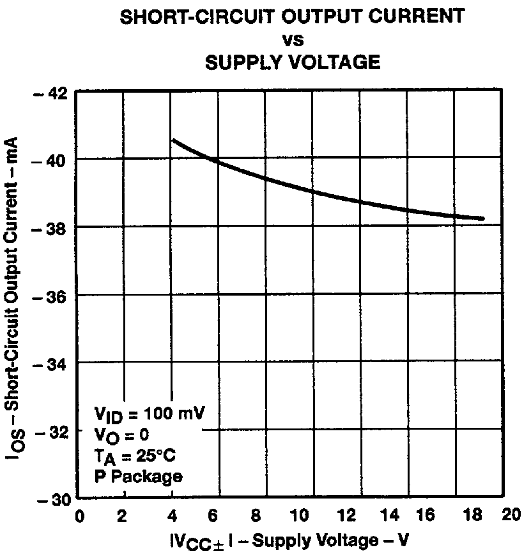


Figure 25

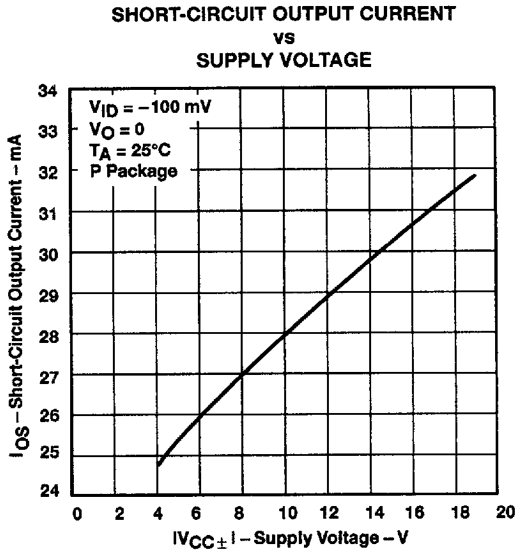


Figure 26

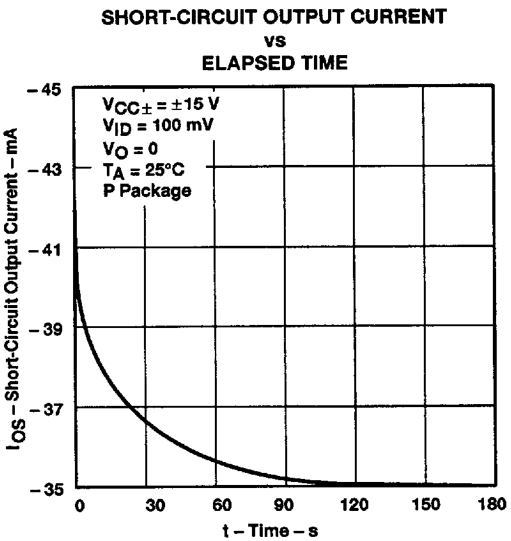


Figure 27

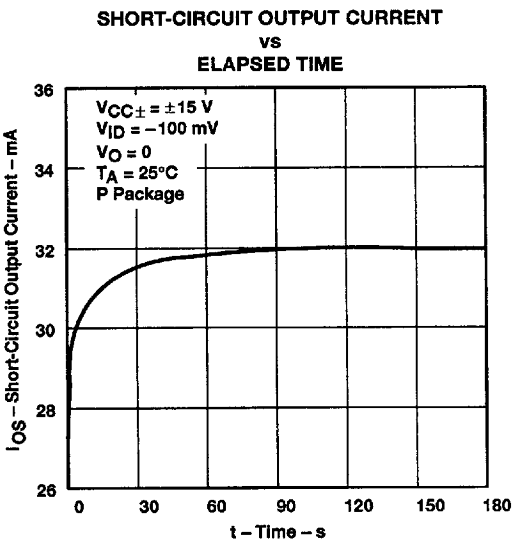


Figure 28

TYPICAL CHARACTERISTICS†

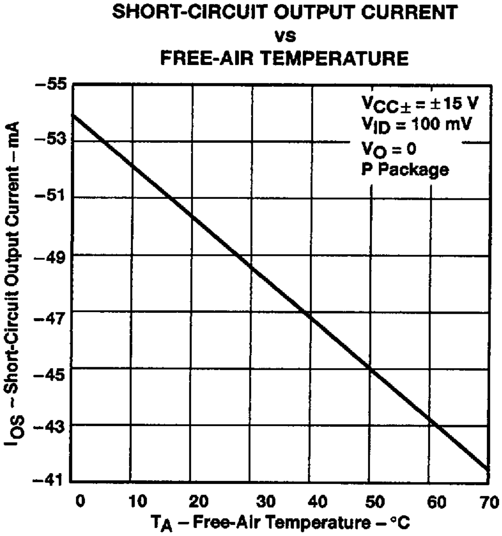


Figure 29

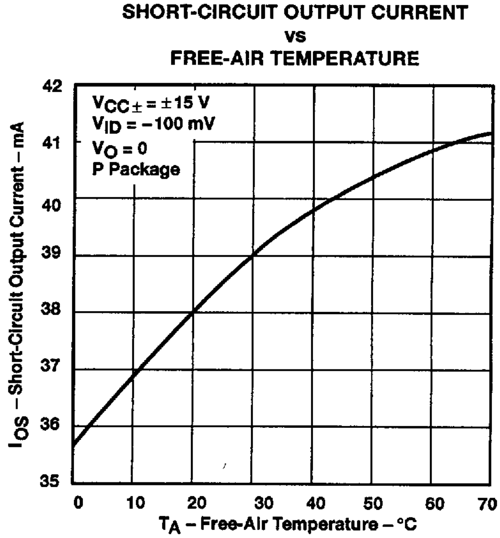


Figure 30

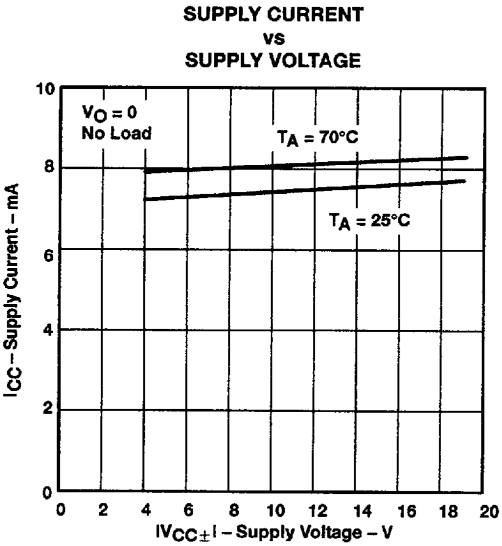


Figure 31

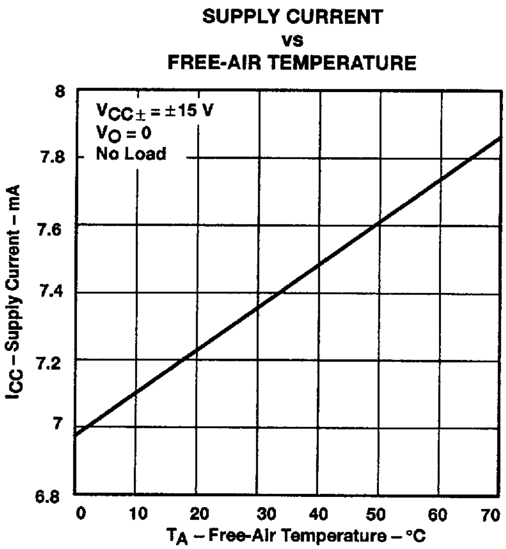


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

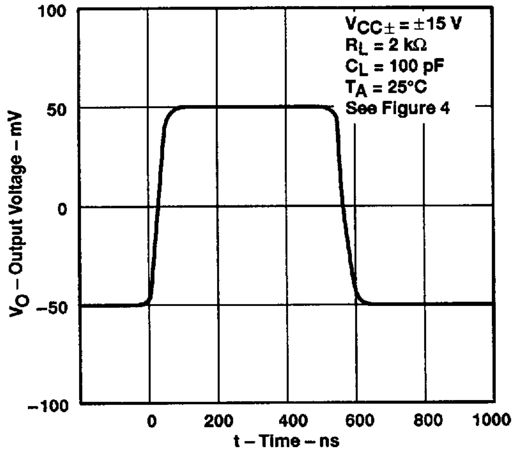


Figure 33

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

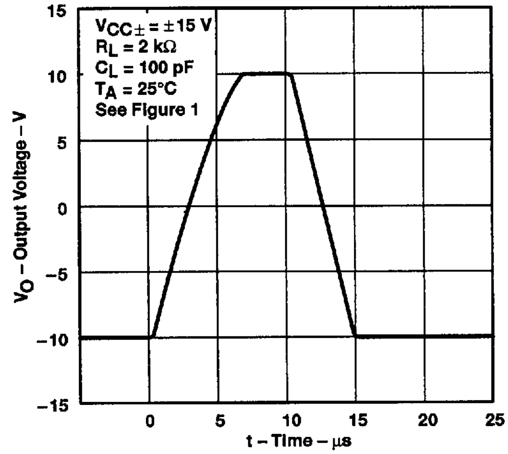


Figure 34

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

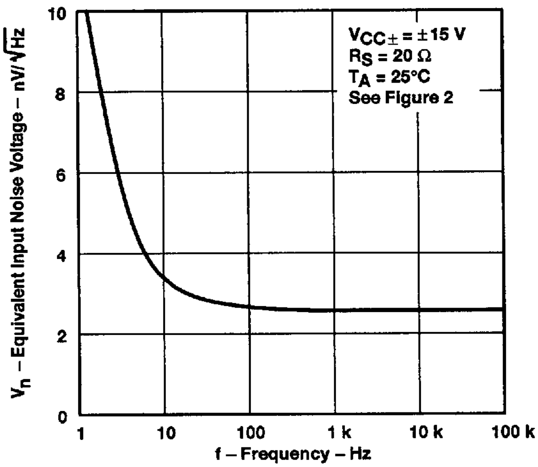


Figure 35

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

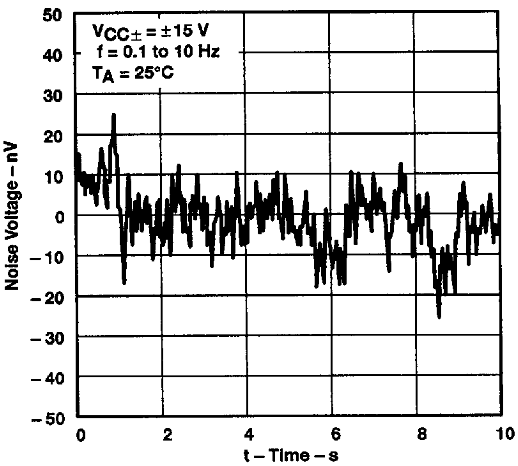


Figure 36

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

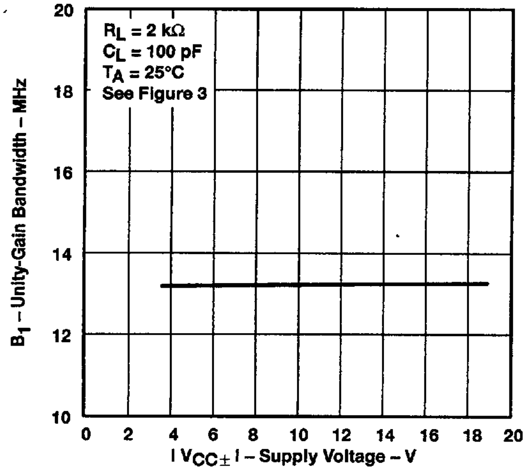


Figure 37

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

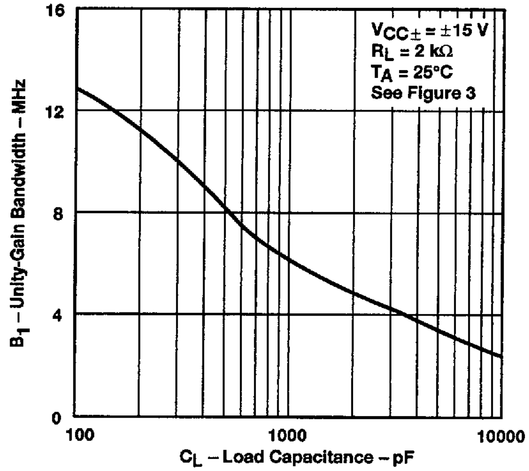


Figure 38

SLEW RATE vs FREE-AIR TEMPERATURE

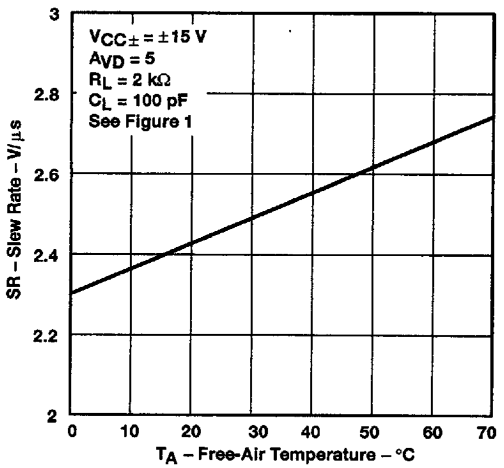


Figure 39

PHASE MARGIN vs SUPPLY VOLTAGE

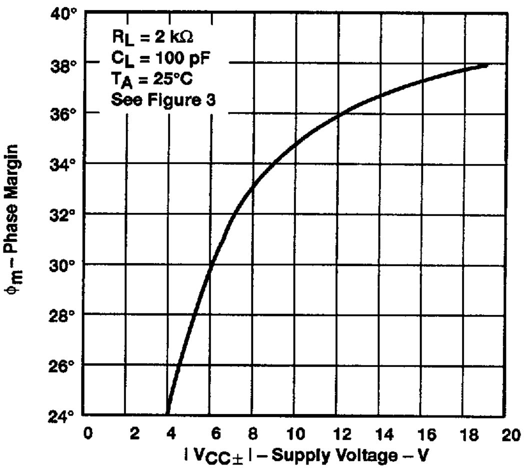


Figure 40

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

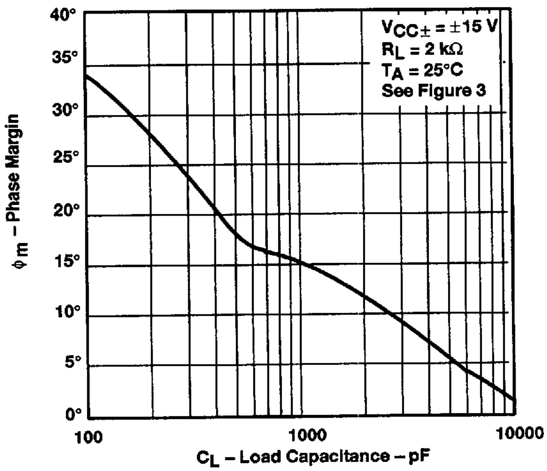


Figure 41

APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 42 and 43 are generated using the TLE2227C typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain bandwidth
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

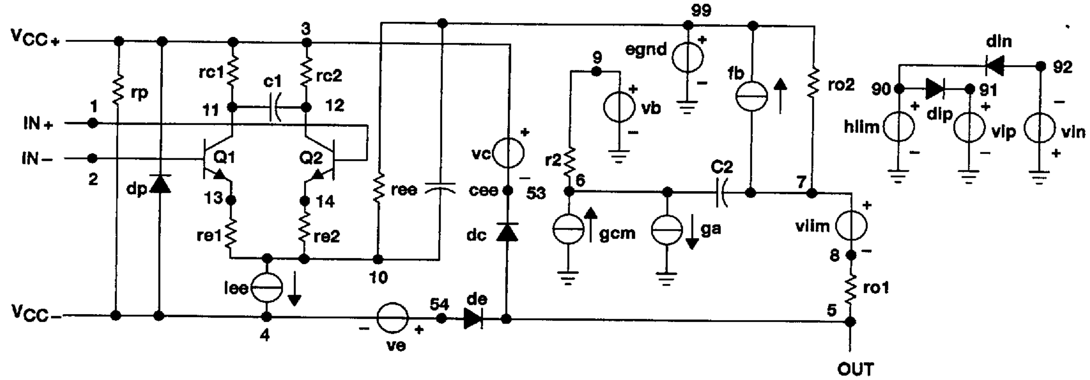


Figure 42. Boyle Macromodel

```
.subckt TLE2227  1   2   3   4   5
*
  c1      11     12  4.003E-12
  c2       6      7  20.00E-12
  dc       5     53  dx
  de      54      5  dx
  dlp     90     91  dx
  dln     92     90  dx
  dp       4      3  dx
  egnd    99      0  poly(2)   (3,0)  (4,0)  0   .5  .5
  fb       7     99  poly(5)   vb  vc  ve  vlp   vln   0   954.8E6   -1E9   1E9   1E9-1E9
  ga       6      0  11  12  2.062E-3
  gcm      0      6  10  99  531.3E-12
  iee     10      4  dc  56.01E-6
  hlim    90      0  vlim   1K
  q1      11      2  13  qx
  q2      12      1  14  qx
  r2       6      9  100.0E3
  rc1      3     11  530.5
  rc2      3     12  530.5
  re1     13     10  -393.2
  re2     14     10  -393.2
  ree     10     99  3.571E6
  ro1      8      5  25
  ro2      7     99  25
  rp       3      4  8.013E3
  vb       9      0  dc  0
  vc       3     53  dc  2.400
  ve      54      4  dc  2.100
  vlim     7      8  dc  0
  vlp     91      0  dc  40
  vln      0     92  dc  40
.model   dx D(Is=800.0E-18)
.model   qx NPN(Is=800.0E-18   Bf=7.000E3)
.ends
```

Figure 43. Macromodel Subcircuit

APPLICATION INFORMATION

voltage-follower applications

The TLE2227C circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. A feedback resistor is recommended to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 44).

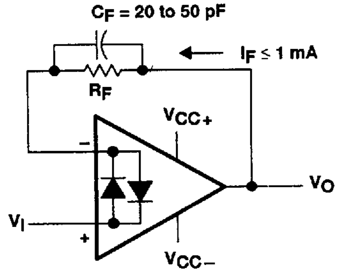
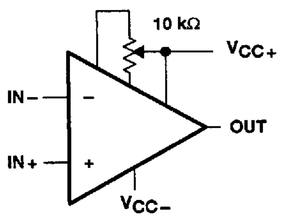


Figure 44. Voltage-Follower Circuit

input offset voltage nulling

The TLE2227C offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 45 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins can be left disconnected.



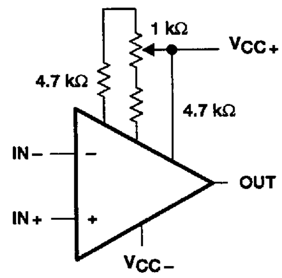


Figure 45. Input Offset Voltage Nulling Circuits

8961724 0094396 991