Hitachi LCD Controller/Driver LSI Data Book

HITACHI

INDEX

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General Information

Quick Reference Guide

Type	**Extension Driver**			
Type Number	**HD44100R**	**HD66100F**	**HD61100A**	**HD61200**
Power supply for internal circuits (V)	2.7 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5
Power supply for LCD driver circuits (V)	3 to 13	3 to 6	5.5 to 17	8 to 17
Power dissipation (mW)	5	5	5	5
Operating temperature (°C)	–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75
Memory ROM (bit)	—	—	—	—
Memory RAM (bit)	—	—	—	—
LCD driver Common	20	—	—	—
LCD driver Column	40 (20)	80	80	80
Instruction set	—	—	—	—
Operation frequency (MHz)	0.4	1	2.5	2.5
Recommend duty	Static–1/53	Static–1/16	Static–1/128	1/32–1/128
Package	FP-60A Chip	FP-100	FP-100	FP-100

Type	**Column Driver**					
Type Number	**HD66204**	**HD66214T**	**HD66224T**	**HD66107T**	**HD66110ST**	**HD66120T**
Power supply for internal circuits (V)	2.7 to 5.5	2.7 to 5.5	2.5 to 5.5	4.5 to 5.5	2.7 to 5.5	2.7 to 5.5
Power supply for LCD driver circuits (V)	10 to 28	10 to 28	10 to 28	14 to 37	14 to 40	14 to 40
Power dissipation (mW)	15	15	15	25	40	50
Operating temperature (°C)	–20 to +75*1	–20 to +75	–20 to +75	–20 to +75	–20 to +75	–20 to +75
Memory ROM (bit)	—	—	—	—	—	—
Memory RAM (bit)	—	—	—	—	—	—
LCD driver Common	—	—	—	160	—	—
LCD driver Column	80	80	80	160	160	240
Instruction set	—	—	—	—	—	—
Operation frequency (MHz)	8 MHz at 5 V 4 MHz at 4 V	8	8 MHz at 5 V 6.5 MHz at 3 V	8	20 MHz at 5 V 13 MHz at 3 V	20 MHz at 5 V 10 MHz at 3 V
Recommend duty	1/64–1/240	1/64–1/240	1/64–1/240	1/100–1/480	1/100–1/480	1/100–1/480
Package	FP-100 TFP100 Chip	TCP	SLIM-TCP	TCP	SLIM-TCP	SLIM-TCP

*1 –40 to +80°C (special request). Please contact Hitachi agents.
*2 Under development

Quick Reference Guide

Type		Column Drive (within RAM)					TFT Column Driver		
Type Number		**HD44102CH**	**HD61102**	**HD61202**	**HD66108T**	**HD66520T**	**HD66300T**	**HD66310T**	**HD66330T**
Power supply for internal circuits (V)		4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	2.7 to 5.5	3.0 to 3.6	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5
Power supply for LCD driver circuits (V)		4.5 to 11	4.5 to 15.5	8 to 17	6 to 15	8 to 28	16 to 20 15 V_{PP}	15 to 23	4.5 to 5.5
Power dissipation (mW)		5	5	5	5	1	160	100	100
Operating temperature (°C)		–20 to +75*1	–20 to +75	–20 to +75*1	–20 to +75	–20 to +75	–20 to +75	–20 to +75*2 (–20 to +60)	–20 to +75
Memory	ROM (bit)	—	—	—	—	—	—	—	—
	RAM (bit)	200 × 8	512 × 8	512 × 8	165 × 65	160 × 240 × 2	—	—	—
LCD driver	Common	—	—	—	0–65	—	—	—	—
	Column	50	64	64	100–165	160	120	160	192
Instruction set		6	7	7	7	—	—	—	—
Operation frequency (MHz)		0.28	0.4	0.4	4	3.3	4.8	12/15	35
Recommend duty		Static–1/32	Static–1/64	1/32–1/128	1/32, 1/34, 1/36, 1/48, 1/50, 1/64, 1/66	1/64–1/240	—	—	—
Package		FP-80 Chip	FP-100	FP-100 TFP-100 Chip	TCP	TCP	TCP	TCP	SLIM-TCP

Type		Segment Display			
Type Number		**HD61602**	**HD61603**	**HD61604**	**HD61605**
Power supply for internal circuits (V)		2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Power supply for LCD driver circuits (V)		2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Power dissipation (mW)		0.5	0.5	0.5	0.5
Operating temperature (°C)		–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75*1
Memory	ROM (bit)	—	—	—	—
	RAM (bit)	204	64	204	64
LCD driver	Common	4	1	4	1
	Column	51	64	51	64
Instruction set		4	4	4	4
Operation frequency (MHz)		0.52	0.52	0.52	0.52
Recommend duty		Static, 1/2, 1/3, 1/4	Static	Static, 1/2, 1/3, 1/4	Static
Package		FP-80 FP-80A	FP-80	FP-80	FP-80

*1 –40 to +80°C (special request). Please contact Hitachi agents.
*2 –20 to +75°C in 12 MHz version, –20 to +65°C in 15 MHz version

Type		Common Driver							
Type Number		**HD44103CH**	**HD44105H**	**HD61103A**	**HD61203**	**HD66205**	**HD66215T**	**HD66113T**	**HD66115T**
Power supply for internal circuits (V)		4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	2.7 to 5.5	2.5 to 5.5	2.5 to 5.5	2.5 to 5.5
Power supply for LCD driver circuits (V)		4.5 to 11	4.5 to 11	4.5 to 17	8 to 17	10 to 28	10 to 28	14 to 40	14 to 40
Power dissipation (mW)		4.4	4.4	5	5	5	5	5	5
Operating temperature (°C)		–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75	–20 to +75	–20 to +75
Memory	ROM (bit)	—	—	—	—	—	—	—	—
	RAM (bit)	—	—	—	—	—	—	—	—
LCD driver	Common	20	32	64	64	80	100/101	120 (60 + 60)	160 (80 + 80)
	Column	—	—	—	—	—	—	—	—
Instruction set		—	—	—	—	—	—	—	—
Operation frequency (MHz)		1	1	2.5	2.5	0.1	0.1	2.5	2.5
Recommend duty		1/8, 1/12, 1/16, 1/24, 1/32	1/8, 1/12, 1/32, 1/48	1/48, 1/64, 1/96, 1/128	1/48, 1/64, 1/96, 1/128	1/64–1/240	1/64–1/240	1/100–1/480	1/100–1/480
Package		FP-60	FP-60 Chip	FP-100	FP-100 TFP-100 Chip	FP-100 TFP-100 Chip	SLIM-TCP	SLIM-TCP	SLIM-TCP

Type		Character Display Controller					
Type Number		**HD44780U (LCD-II)**	**HD66702R (LCD-II/E20)**	**HD66710 (LCD-II/F8)**	**HD66712 (LCD-II/F12)**	**HD66720 (LCD-II/K8)**	**HD66730 (LCD-II/J6)**
Power supply for internal circuits (V)		2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Power supply for LCD driver circuits (V)		3 to 11	3 to 8	3 to 13	3 to 13	3 to 11	3 to 13
Power dissipation (mW)		2	2	2	2	2	2
Operating temperature (°C)		–20 to +75*1	–20 to +75*1	–20 to +75*1	–20 to +75	–20 to +75*1	–20 to +75*1
Memory	ROM (bit)	9920	7200	9600	9600	9600	510 k
	RAM (bit)	80 × 8, 64 × 8	80 × 8, 64 × 8	80 × 8, 64 × 8, 8 × 8	80 × 8, 64 × 8, 16 × 8	40 × 8, 64 × 8, 16 × 8	40 × 2 × 8, 8 × 26 × 8, 16 × 8
LCD driver	Common	16	16	33	33	9 (16)	26
	Column	40	100	40	60	50 (42)	71
Instruction set		11	11	11	11	11	13
Operation frequency (MHz)		0.25	0.25	0.25	0.25	0.1 to 0.4	0.08 to 0.7
Recommend duty		1/8, 1/11, 1/16	1/8, 1/11, 1/16	1/17, 1/33	1/17, 1/33	1/9, 1/17	1/14, 1/27, 1/40, 1/53
Package		FP-80B TFP-80 Chip	FP-144A Chip	FP-100A TFP-100 Chip	TCP FP-128 Chip	FP-100A TFP-100 Chip	FP-128 Chip

*1 –40 to +80°C (special request). Please contact Hitachi agents.

Quick Reference Guide

Type		Graphic Display Controller				
Type Number		**HD61830 LCDC**	**HD61830B LCDC**	**HD63645F HD64645F HD64646FS LCTC**	**HD66840F HD66841F LVIC**	**HD66850 CLINE**
Power supply for internal circuits (V)		4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5
Power supply for LCD driver circuits (V)		—	—	—	—	—
Power dissipation (mW)		30	50	50	250	500
Operating temperature (°C)		–20 to +75	–20 to +75*1	–20 to +75	–20 to +75	–20 to +75
Memory	ROM (bit)	7360	7360	—	—	—
	RAM (bit)	—	—	—	—	9762
LCD driver	Common	—	—	—	—	—
	Column	—	—	—	—	—
Instruction set		12	12	15	16/24	63
Operation frequency (MHz)		1.1	2.4	10	25 MHz (840) 30 MHz (841)	32
Recommend duty		Static–1/128	Static–1/128	Static–1/512	Static–1/1024	Static–1/512
Package		FP-60	FP-60	FP-80 FP-80B	FP-100A	FP-136

*1 –40 to +80°C (special request). Please contact Hitachi agents.

Type Number Order

Sorted by Type Name

Type	Function	Reference Page
HD44100RFS	40-channel LCD driver	151
HD44102CH	50-channel column driver within RAM	669
HD44103CH	20-channel common driver	694
HD44105H	32-channel common driver	704
HD44780UA00FS/00TF/01FS/ 02FS/UB**FS/UB**TF LCD-II	LCD controller/driver (8 × 2 character)	206
HD61100A	80-channel column driver	179
HD61102RH	64-channel column driver within RAM	714
HD61103A	64-channel common driver	741
HD61200	80-channel column driver	192
HD61202/TFIA	64-channel column driver within RAM	766
HD61203/TFIA	64-channel common driver	796
HD61602R/RH	Segment display type LCD driver	1172
HD61603R	Segment display type LCD driver	1172
HD61604R	Segment display type LCD driver	1205
HD61605R	Segment display type LCD driver	1205
HD61830A00H LCDC	LCD controller	1234
HD61830B00H LCDC	LCD controller	1234
HD63645F LCTC	LCD timing controller (68 family)	1271
HD64645F LCTC	LCD timing controller (80 family)	1271
HD64646FS LCTC	LCD timing controller (80 family)	1271
HD66100F/FH	80-channel LCD driver	164
HD66107T00/01/11/12/24/25	160-channel column/common driver	1084
HD66108T00	165-channel graphic LCD controller/driver	885
HD66110TB0/TB2	160-channel column driver	1105
HD66113TA0	120-channel common driver	1122
HD66115TA0/1	160-channel common driver	1139
HD66120T	240-channel segment driver	1156
HD66204F/FL/TF/TFL	80-channel column driver	983
HD66205F/FL/TF/TFL/TA1/TA2/ TA3/TA6/TA7/TA9L	80-channel common driver	999
HD66214TA1/2/3/6/9L	80-channel column driver	1015
HD66215TA0/1/2	100-channel common driver	1046
HD66224TA1/TA2/TB0	80-channel column driver	1030
HD66300T00	120-channel TFT analog column driver	1448
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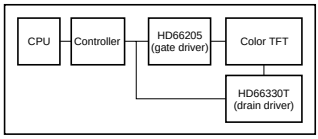
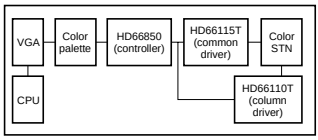
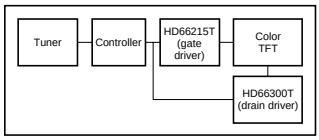
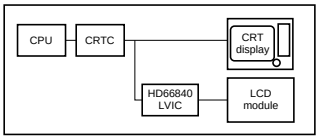
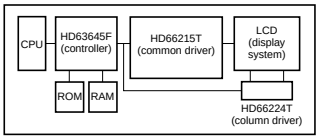
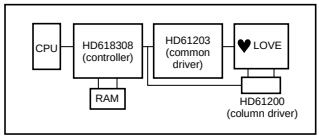
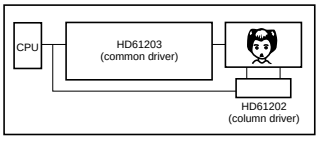
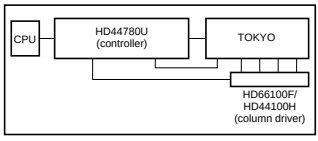
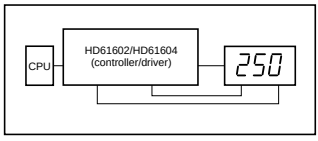
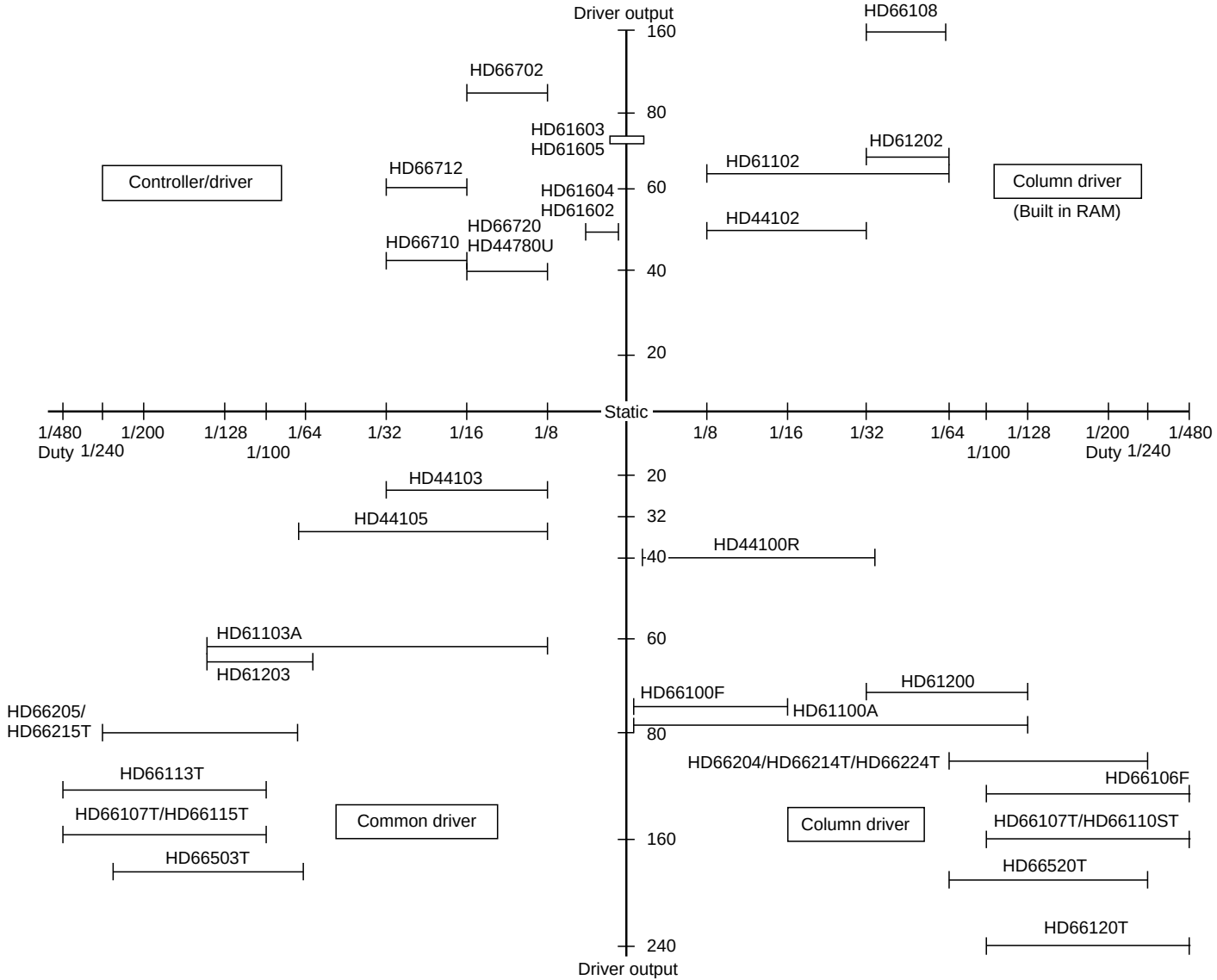
HD66330TA0	192-channel TFT digital column driver (64 gray scale)	1531
HD66410Txx	RAM-provided 128-channel driver	823
HD66503	240-channel common driver	858
HD66520T	160-channel grayscale display column driver	942
HD66702RA00F/00FL/01F/02F/ RB**F/RB**FL LCD-II/E20	LCD controller/driver (20 × 2 character)	268
HD66710A00FS/00TF/01TF/02TF/ B**FS/B**TF LCD-II/F8	LCD controller/driver (8 × 4 character)	332
HD66712A00FS/00TA0/00TB0/02FS/ B**FS LCD-II/F12	LCD controller/driver (12 × 4 character)	416
HD66720A03FS/TF	Panel controller/driver	502
HD66730A00FS	LCD controller/driver	583
HD66840FS LVIC	LCD video interface controller (8 gray scale control)	1318
HD66841FS LVIC-II	LCD video interface controller (8 gray scale control)	1318
HD66850F CLINE	Color LCD interface engine (16 gray scale control)	1379

Selection Guide

Hitachi LCD Driver System

Type	Reference Figure	Screen Size (Max)	Lineup	Application
TFT full color system		(800 × 3) × 520 dots	HD66310T (drain) HD66330T (drain) HD66205 (gate) HD66215T (gate)	Personal computer Terminal workstation Navigation system
STN full color system		(720 × 3) × 480 dots	HD66850F (controller) HD66107T (column, common) HD66110T (column) HD66115T (common) HD66120T (column) HD66113T (common)	Personal computer Terminal workstation
Color LCD-TV system		720 × 480 dots	HD66300T (drain) HD66205 (gate) HD66215T (gate)	LCD-TV Portable video
Video to LCD converter		720 × 512 dots	HD66840F, HD66841F HD66106F (driver) HD66107T (driver) HD66204 (column)/ 66205 (common) HD66224T (column)/ HD66215T (common)	Personal computer Terminal OHP
Display system for CRT compatible		640 × 400 dots	HD63645/64645/ 64646 (controller) HD66204 (column)/ 66205 (common) HD66224T (column)/ HD66215T (common)	Personal computer Wordprocessor Terminal
Graphic display system		Character 80 × 16 Graphic 480 × 128 dots	HD61100A (column) HD61830B (controller) HD61200 (column) HD61103A (common) HD61203 (common)	Laptop computer Facsimile Telex Copy machine
Graphic display system (bitmap)		480 × 128 dots	HD44102 (column)/ 61102 (column) HD44103 (common) HD61202 (column) HD44105 (common)/ 61103A (common) HD61203 (common) HD66108 (column/common)	Laptop computer Handy wordprocessor Toy
Character display system		40 characters × 2 columns 80 characters × 1 column	HD44780U (LCD-II) (controller/driver) HD44100R (column) HD66100F (column) HD66702 (LCD-II/E20) HD66710 (LCD-II/F8) HD66712 (LCD-II/F12)	Electrical typewriter, Multifunction telephone, Handy terminal
Segment display system		25 digits × 1 column	HD61602 (controller/driver) HD61604 (controller/driver) HD61603 (controller/driver) HD61605 (controller/driver)	ECR, Measurement system, Telephone industrial measurement system


Driver output
160
80
60
40
20
Static
20
32
40
60
80
160
240
Driver output
1/480
1/200
1/128
1/64
1/32
1/16
1/8
Duty 1/240
1/100
1/8
1/16
1/32
1/64
1/128
1/200
1/480
1/100
Duty 1/240
HD66108
HD66702
HD61603
HD61605
HD61202
HD61102
HD66712
Controller/driver
HD61604
HD61602
HD66720
HD44780U
HD66710
HD44102
Column driver
(Built in RAM)
HD44103
HD44105
HD44100R
HD61103A
HD61203
HD66205/
HD66215T
HD66100F
HD61100A
HD61200
HD66204/HD66214T/HD66224T
HD66106F
HD66113T
HD66107T/HD66115T
HD66503T
Common driver
Column driver
HD66107T/HD66110ST
HD66520T
HD66120T

Selection Guide

Application

Character and Graphic Display

1 character = 7 × 8 dot (15 × 7 dot + cursor)

<table>
<tr><th>Character
Line</th><th>8</th><th>16</th><th>20</th><th>24</th><th>32</th><th>40</th><th>Over 80</th></tr>
<tr><td>1</td><td rowspan="5"></td><td colspan="5" rowspan="2">HD66100F</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td><td colspan="4" rowspan="2">HD44100R</td></tr>
<tr><td>4</td></tr>
<tr><td>6 to 8</td><td colspan="5"></td></tr>
<tr><td>12 to 15</td><td colspan="7">HD61200 (column) + HD61203 (common)</td></tr>
<tr><td>16 to 25</td><td colspan="7" rowspan="2">HD66204 (column) + HD66205 (common)
HD66214T/HD66224T (column) + HD66215T (common)
HD66107T
HD66110T (column) + HD66115T (common)
HD66120T (column) + HD66113T (common)</td></tr>
<tr><td>26 to 50</td></tr>
</table>

Graphic Display

<table>
<tr><th>Horizontal
Vertical</th><th>48</th><th>96</th><th>120</th><th>180</th><th>240</th><th>480</th><th>Over 640</th></tr>
<tr><td>16</td><td colspan="5" rowspan="4">HD61202 (column) + HD61203 (common)</td><td rowspan="4"></td></tr>
<tr><td>32</td></tr>
<tr><td>48</td></tr>
<tr><td>64</td></tr>
<tr><td>128</td><td colspan="6" rowspan="3">HD66204 (column) + HD66205 (common)
HD66214T/HD66224T (column) + HD66215T (common)
HD66107T
HD66110T (column) + HD66115T (common)
HD66120T (column) + HD66113T (common)</td></tr>
<tr><td>400</td></tr>
<tr><td>Over 400</td></tr>
</table>

Note: Applications on this page are only examples, and this combination of devices is not the best.

Differences Between Products

1. HD66100F and HD44100R

	HD66100F	HD44100H
LCD driver circuits	80	20 × 2
Power supply for internal logic (V)	3 to 6	3 to 13
Display duty	Static to 1/16	Static to 1/33
Package	100 pin plastic QFP	60 pin plastic QFP

2. HD61100A and HD61200

		HD61100A	HD61200
LCD drive circuits	Common	—	—
	Column	80	80
Display duty		Static to 1/128	1/32 to 1/128
Power supply for LCD drive circuits (V)		0 to 17	8 to 17
Power supply limits of LCD driver circuit voltage		V_{CC} to V_{EE} (no limit)	Shown in figures below

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y_1 to Y_{80} is specified under the following conditions:

$V_{CC} - V_{EE} = 17$ V

V1L = V1R, V3L = V3R = $V_{CC} - 2/7\ (V_{CC} - V_{EE})$

V2L = V2R, V4L = V4R = $V_{EE} + 2/7\ (V_{CC} - V_{EE})$

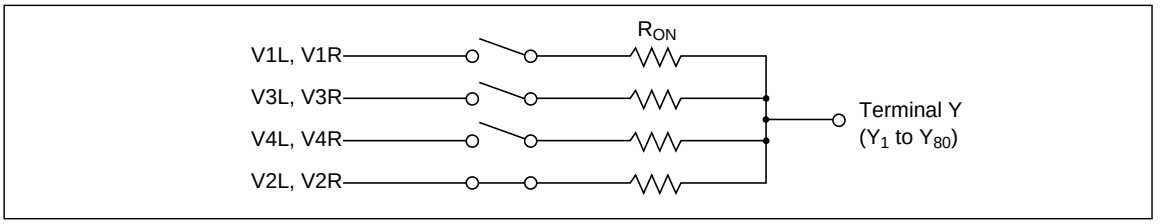


Figure 1 Resistance between Y and V Terminals

The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice the ΔV depends on power supply voltage $V_{CC} - V_{EE}$.

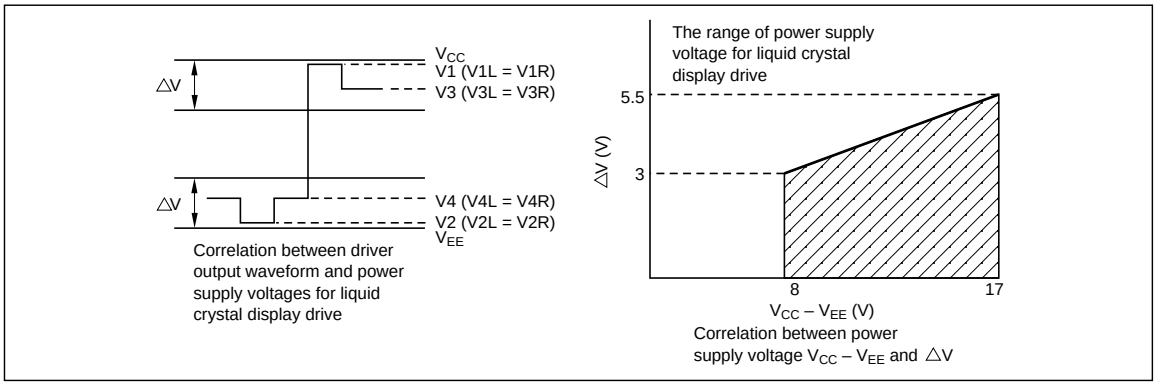


Figure 2 Power Supply Voltage Range

3. HD66100F and HD61100A

		HD66100F	HD61100A
LCD drive circuits	Common	—	—
	Column	80	80
Power supply for LCD drive circuits (V)		3 to 6	5.5 to 17.0
Display duty		Static to 1/16	Static to 1/128
Operating frequency (MHz)		1.0 MHz (max)	2.5 MHz (max)
Data fetch method		Shift	Latch
Package		100 pin plastic QFP (FP-100)	100 pin plastic QFP (FP-100)

4. HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal	External
Operating frequency (MHz)	1.1 MHz	2.4 MHz
Display duty	Static to 1/128	Static to 1/128
Programmable screen size (max)	64 × 240 dots (1/64 duty)	128 × 480 dots (1/64 duty)
Other	Pin 6: C Pin 7: R Pin 9: CPO	Pin 6: $\overline{CE}$ Pin 7: $\overline{OE}$ Pin 9: NC
Package marking	Ⓐ	Ⓑ

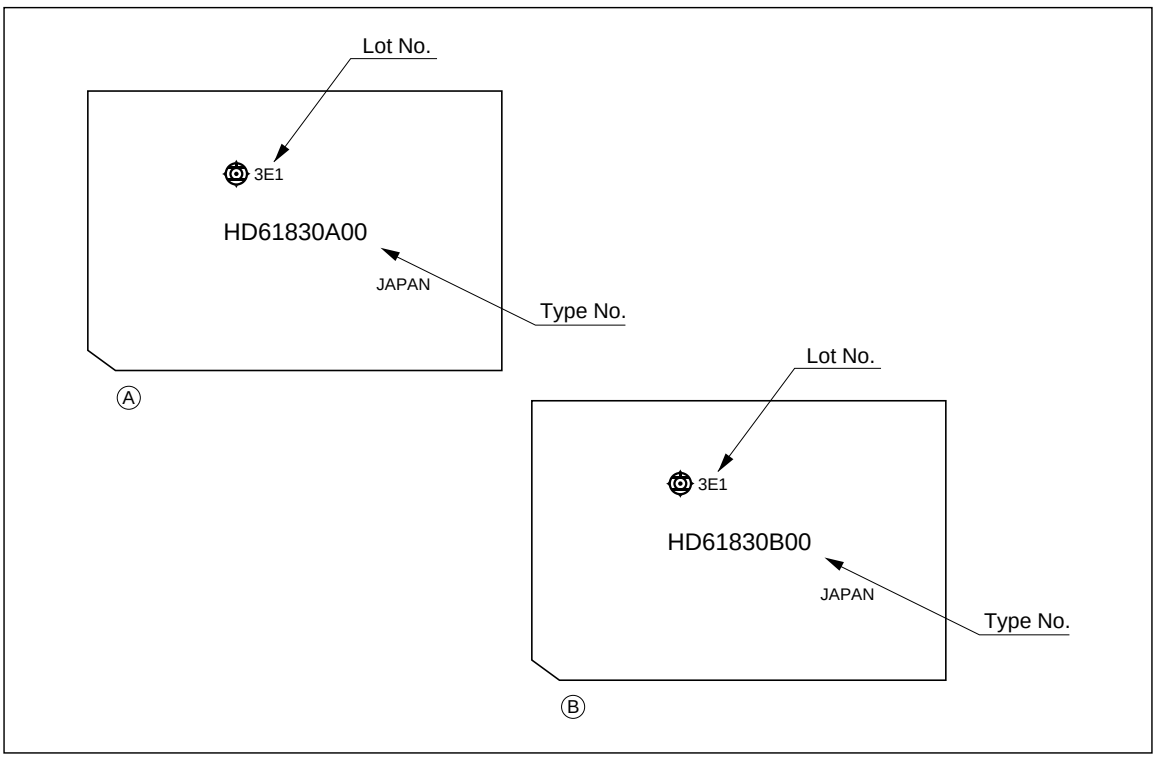


Figure 3 Package Marking

5. HD61102 and HD61202

	HD61102	HD61202
Display duty	Static to 1/64	1/32 to 1/64
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 15.5	8 to 17
Power supply limits of LCD driver circuits voltage	V_{CC} to V_{EE} (no limit)	Shown in following figures
Pin 88	DY (output)	NC (no connection)
Absolute maximum rating of V_{EE} (V)	V_{CC} – 17.0 to V_{CC} + 0.3	V_{CC} – 19.0 to V_{CC} + 0.3

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y_1 to Y_{64} is specified under the following conditions:

$V_{CC} – V_{EE} = 15$ V

V1L = V1R, V3L = V3R = $V_{CC} – 2/7 (V_{CC} – V_{EE})$

V2L = V2R, V4L = V4R = $V_{EE} + 2/7 (V_{CC} – V_{EE})$

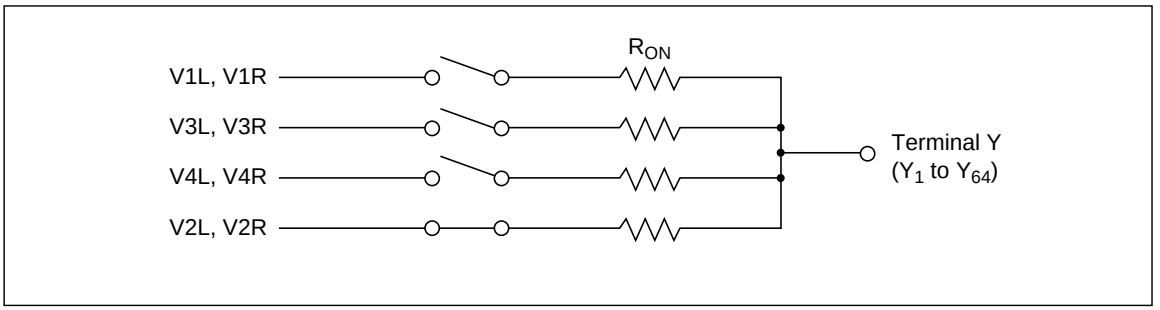


Figure 4 Resistance between Y and V Terminals

The following is a description of the range of power supply voltage for liquid crystal display drives. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} – V_{EE}$.

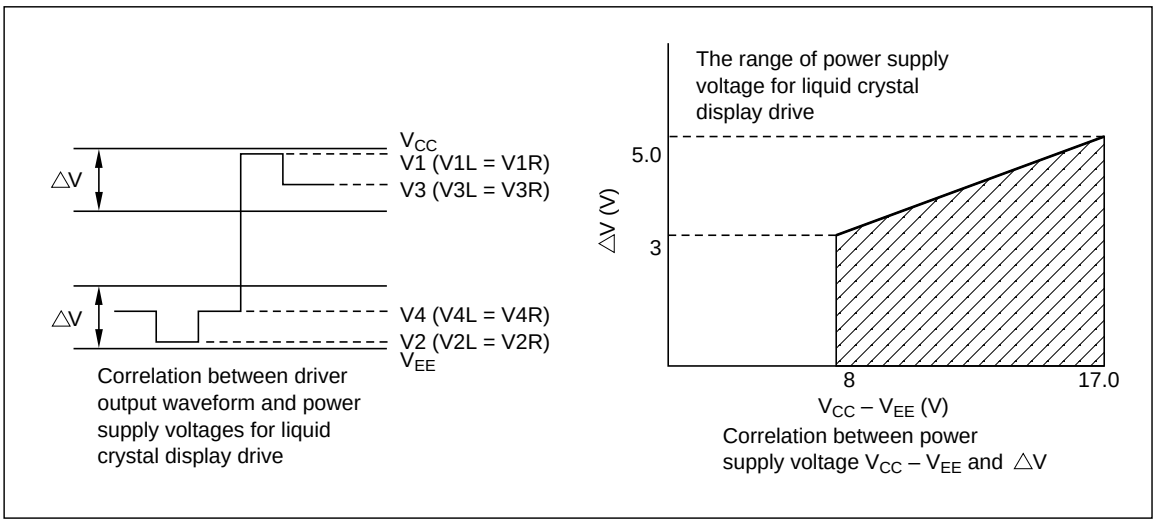


Figure 5 Power Supply Voltage Range

6. HD61103A and HD61203

	HD61103A	HD61203
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 17	8 to 17
Power supply limits of LCD drive circuits voltage	V_{CC} to V_{EE} (no limit)	Shown in figures below
Output terminal	Shown in following figure 4	Shown in following figure 5

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:
$V_{CC} - V_{EE} = 17$ V
V1L = V1R, V6L = V6R = $V_{CC} - 1/7\ (V_{CC} - V_{EE})$
V2L = V2R, V5L = V5R = $V_{EE} + 1/7\ (V_{CC} - V_{EE})$

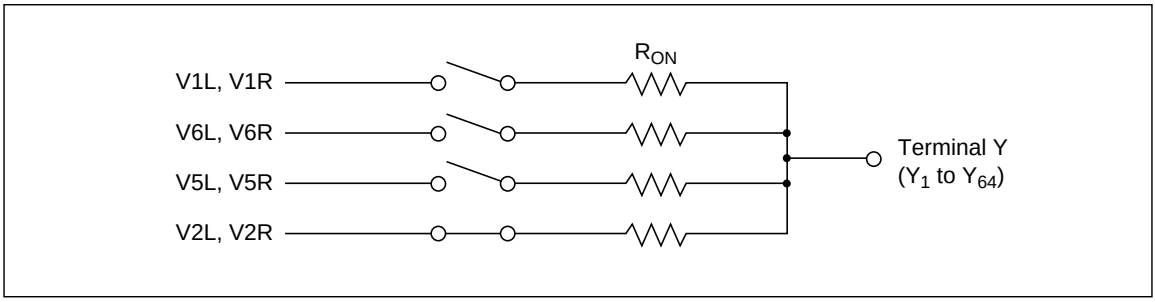


Figure 6 Resistance between Y and V Terminals

Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V6L = V6R and negative voltage to V2L = V2R and V5L = V5R within the ΔV range.
This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.

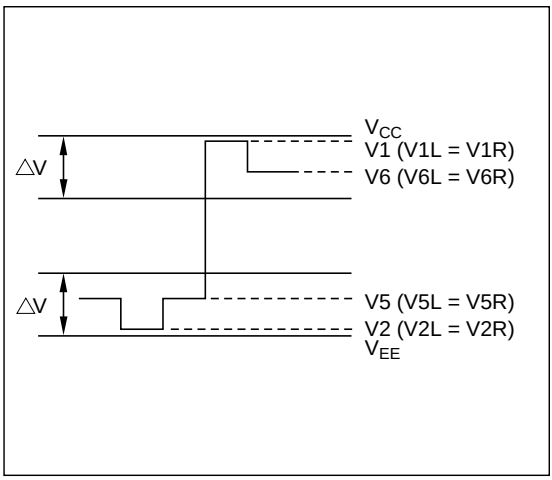


Figure 7 Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

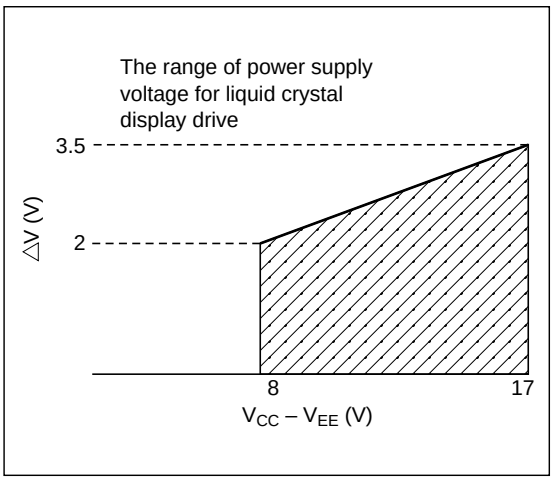


Figure 8 Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

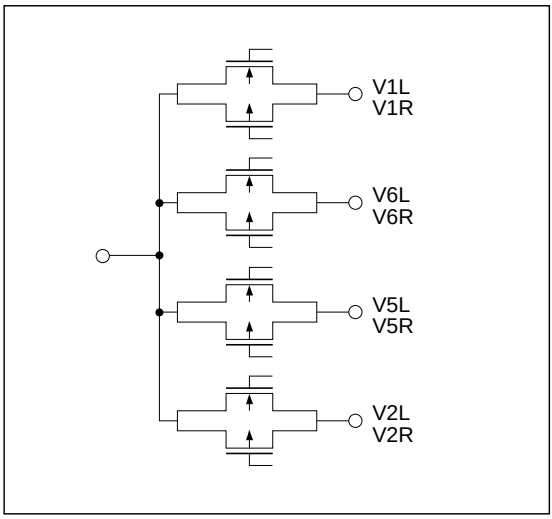


Figure 9 HD61103A Output Terminal

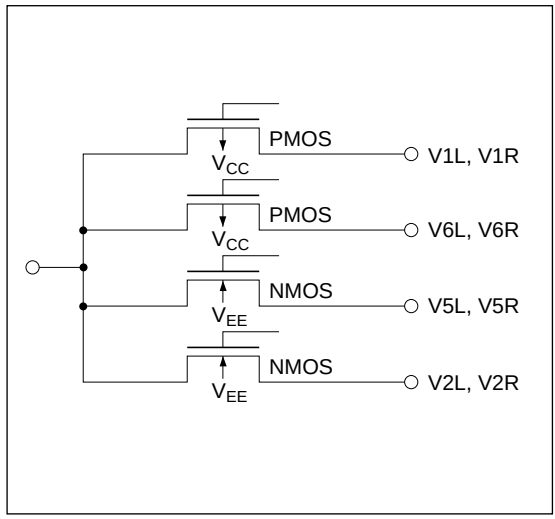


Figure 10 HD61203 Output Terminal

7. HD61602, HD61603, HD61604, and HD61605

		HD61602	HD61603	HD61604	HD61605
Power supply (V_{DD})		2.2 to 5.5 V	2.2 to 5.5 V	4.5 to 5.5 V	4.5 to 5.5 V
Instruction word		8 bits × 2	4 bits × 4	8 bits × 2	4 bits × 4
LCD power supply circuit		Yes	—	—	—
Segment terminals		51	64	51	64
Display size frame frequency (fosc = 100 kHz)	Static	6 digits + 3 marks 33 Hz	8 digits 33 Hz	6 digits + 3 marks 98 Hz	8 digits 98 Hz
	1/2 duty	12 digits + 6 marks 65 Hz	—	12 digits + 6 marks 195 Hz	—
	1/3 duty	17 digits 208 Hz	—	17 digits 521 Hz	—
	1/4 duty	25 digits + 4 marks 223 Hz	—	25 digits + 4 marks 781 Hz	—

8. LCD-II Family (HD44780U, HD66702R and HD66710)

Item	LCD-II (HD44780U)	LCD-II/20 (HD66702)	LCD-II/F8 (HD66710)
Power supply voltage	2.7 V to 5.5 V	5 V ± 10% (standard) 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V
Liquid crystal drive voltage V_{LCD}	3.0 V to 11 V	3.0 V to 7.0 V	3.0 V to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines
Segment display	None	None	40 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33
CGROM	9,920 bits (208: 5 × 8 dot characters and 32: 5 × 10 dot characters)	7,200 bits (160: 5 × 7 dot characters and 32: 5 × 10 dot characters)	9,600 bits (240: 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes
Segment signals	40	100	40
Common signals	16	16	33
Liquid crystal drive waveform	A	B	B
Number of displayed lines	1 or 2	1 or 2	1, 2 or 4
Low power mode	None	None	Available
Horizontal scroll	Character unit	Character unit	Dot unit
CPU bus timing	2 MHz (5-V operation) 1 MHz (3-V operation)	1 MHz	2 MHz (5-V operation) 1 MHz (3-V operation)
Package	QFP1420-80 80-pin bare chip	LQFP2020-144 144-pin bare chip	QFP1420-100 100-pin bare chip

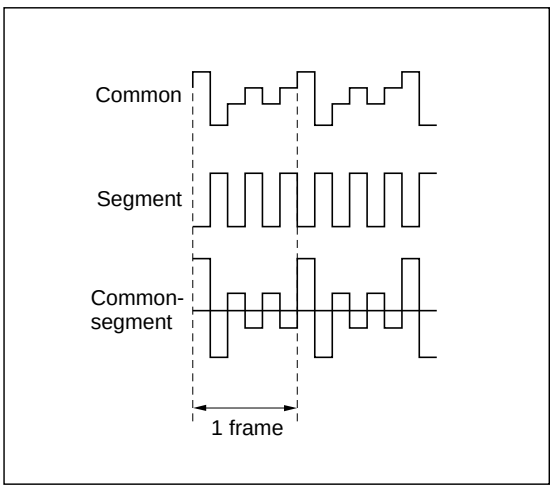


Figure 11 Waveform A (1/3 Duty, 1/3 Bias)

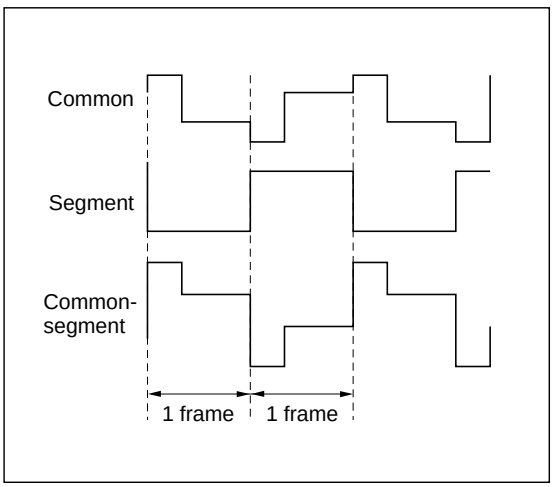


Figure 12 Waveform B (1/3 Duty, 1/3 Bias)

9. HD66204, HD66214T and HD66224T

	HD66204	HD66214T	HD66224T
Data input (bit)	4	4	4/8
Package	100-pin plastic QFP FP-100, TFP-100 Die	TCP	TCP (8 mm)

10. HD66205, HD66215T and HD66115T

	HD666205	HD66215T	HD66115T
LCD drive circuits	80	100/101	160
Power supply for LCD drive circuits (V)	–10 to –28 (V_{CC}–V_{EE})	–10 to –28 (V_{CC}–V_{EE})	+14 to +40 (V_{LCD}–GND)

11. HD66107T and HD66110RT

	HD66107T	HD66110ST
LCD drive circuits	160	160
Data transfer	4/8-bits	4-bits/8-bits
Operating frequency (MHz)	8	20
Power supply for LCD drive circuits	14 to 37	14 to 40
Package	TCP	TCP (9 mm)

12. HD63645, HD64645 and HD64646

	HD63645F	HD64645F	HD64646FS
CPU interface	68 family	80 family	80 family
Package	80-pin plastic QFP (FP-80)	80-pin plastic QFP (FP-80)	80-pin plastic QFP (FP-80A)
Other	—	—	HD64646 has another LCD drive interface in HD64645

13. HD66840F and HD66841F

	HD66840F	HD66841F
Frame-based thinning control	Each line	Each dot and each line
Display mode 16	Signal screen Both sides X/Y driver Horizontal stripe	Dual screen One sides X/Y driver Vertical stripe
Gray-scale palette	No	8 registers

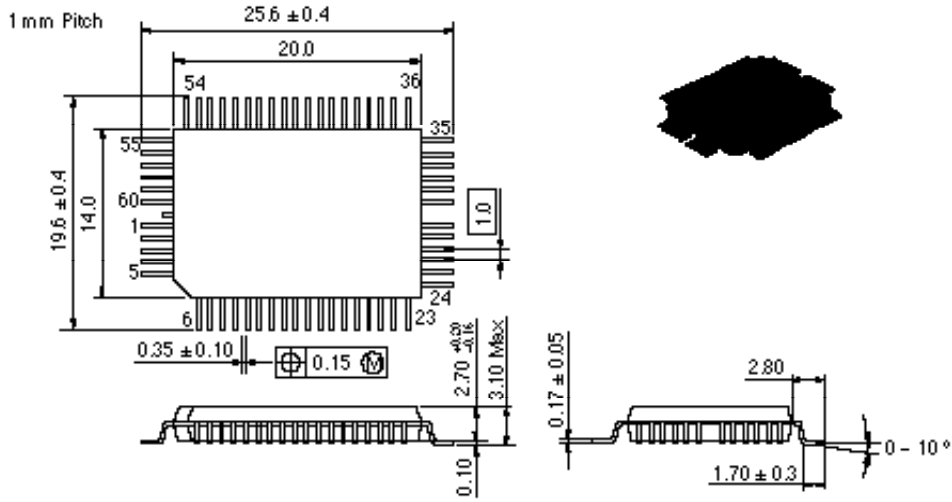
Package Information

The Hitachi LCD driver devices use plastic flat packages to reduce the size of the equipment in which they are incorporated and provide higher density mounting by utilizing the features of thin liquid crystal display elements.

Package Dimensions

Scale: 3/2

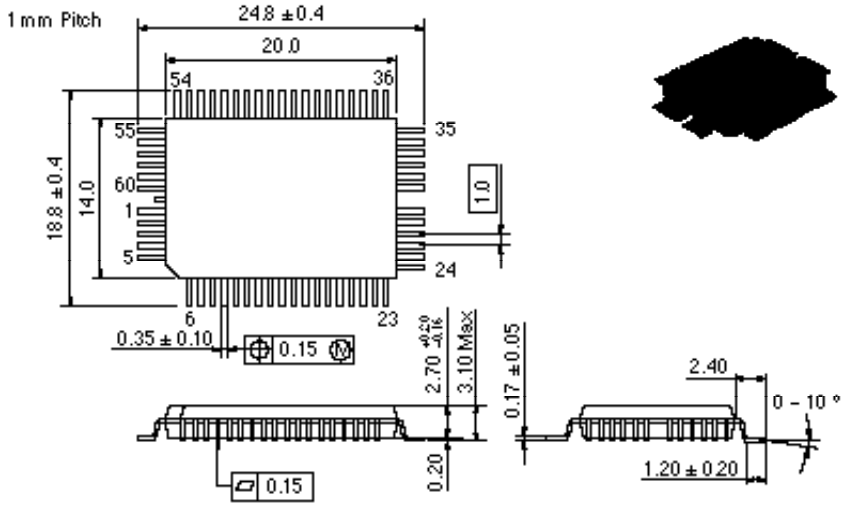
FP-60



Code	FP-60
EIAJ	—
JEDEC	—

Applicable LSI	HD44103, HD44105, HD61830, HD61830B

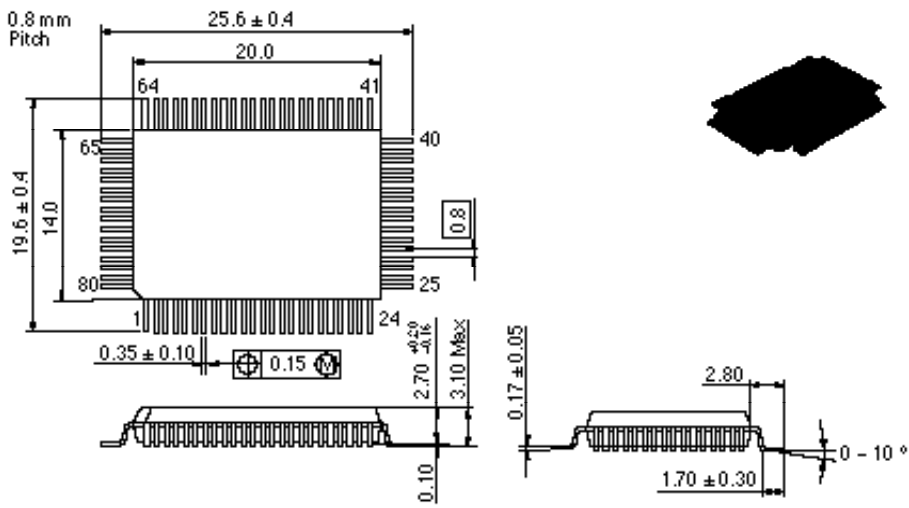
FP-60A



Code	FP-60A
EIAJ	SC-582-F
JEDEC	—

Applicable LSI	HD44100R

FP-80

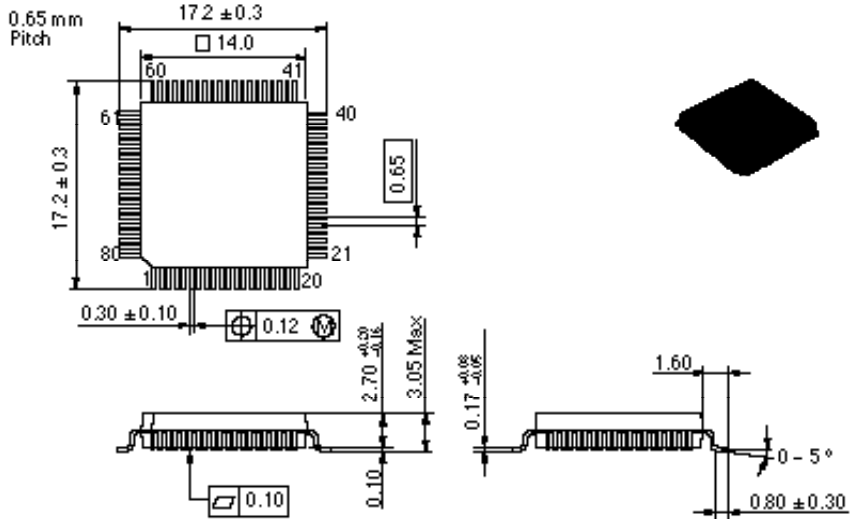


Code	FP-80
EIAJ	—
JEDEC	—

Applicable LSI	HD61602, HD61603, HD61604, HD61605, HD63645, HD64645, HD44102

Package Information

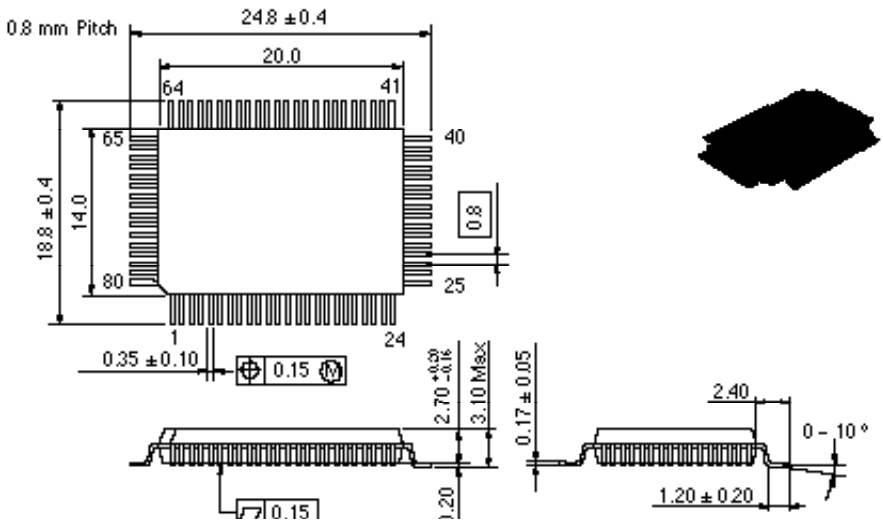
FP-80A



Code	FP-80A
EIAJ	—
JEDEC	—

Applicable LSI	HD61602

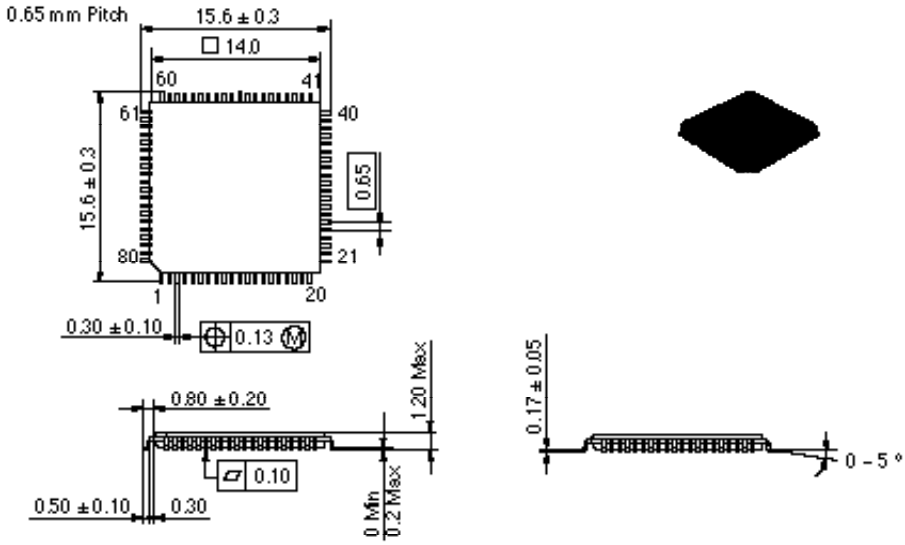
FP-80B



Code	FP-80B
EIAJ	—
JEDEC	—

Applicable LSI	HD64646, HD44780U

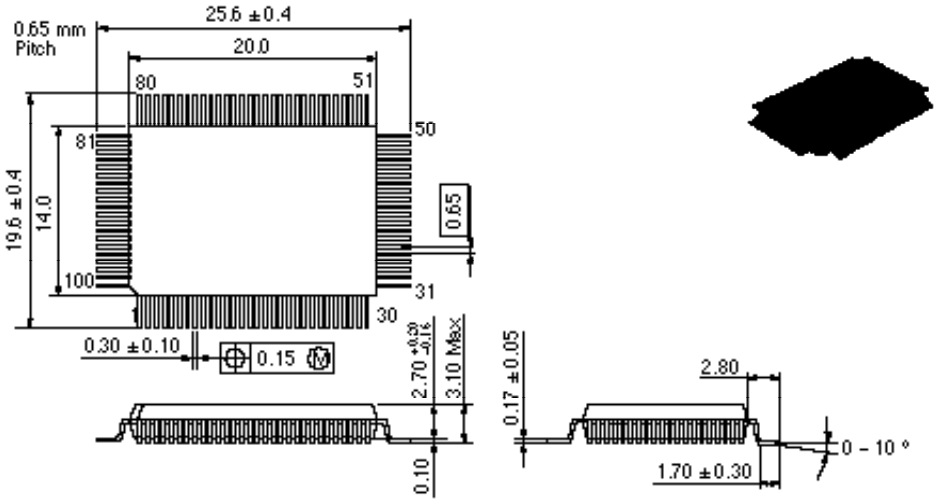
TFP-80



Code	TFP-80
EIAJ	—
JEDEC	—

Applicable LSI	HD44780U

FP-100

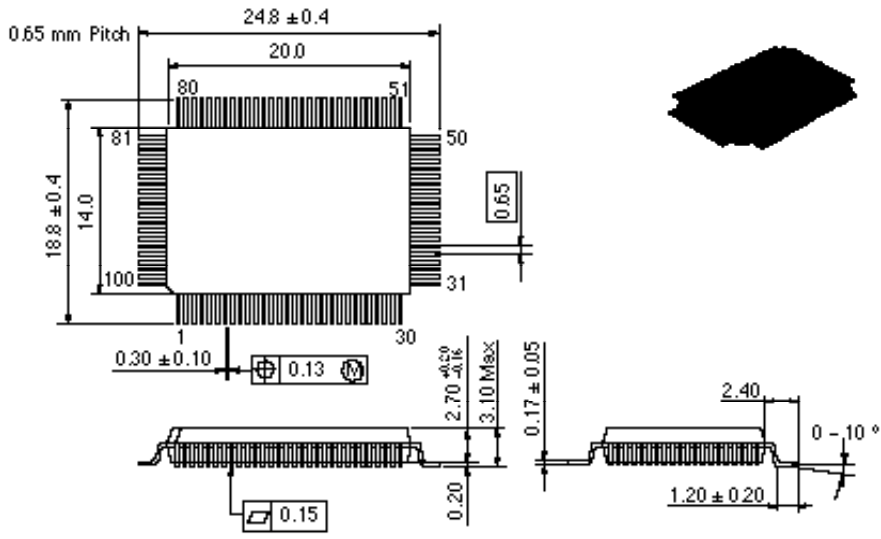


Code	FP-100
EIAJ	—
JEDEC	—

Applicable LSI	HD61100A, HD61102, HD61103A, HD66204, HD66205, HD61200, HD61202, HD61203, HD66100F

Package Information

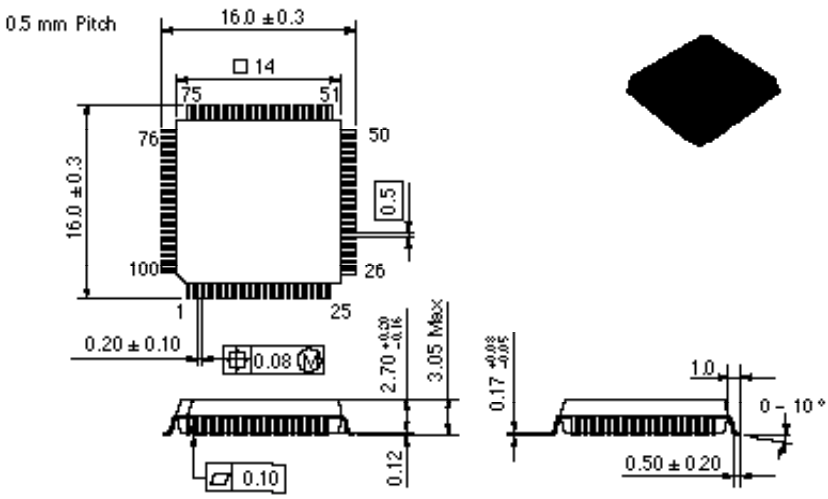
FP-100A



Code	FP-100A
EIAJ	—
JEDEC	—

Applicable LSI	HD66840F, HD66841F, HD66710

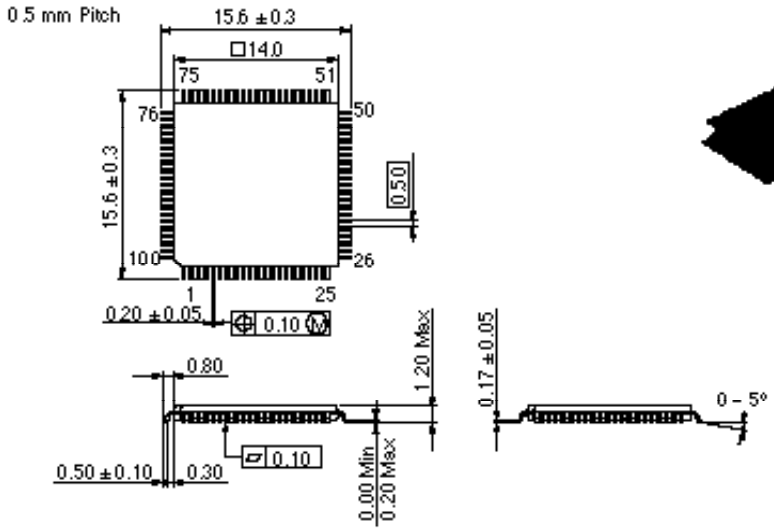
FP-100B



Code	FP-100B
EIAJ	—
JEDEC	—

Applicable LSI	HD66100F

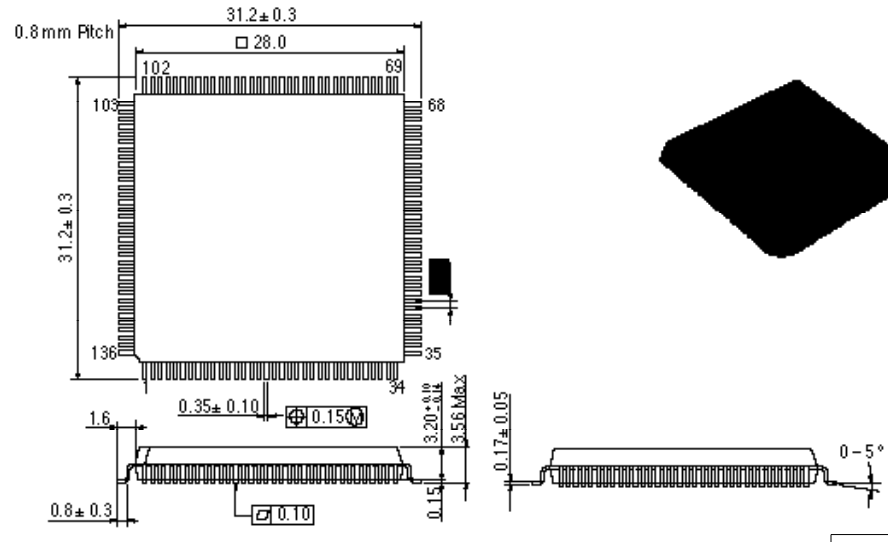
TFP-100



Code	TFP-100
EIAJ	—
JEDEC	—

Applicable LSI	HD66204, HD66205, HD61202, HD61203

FP-136

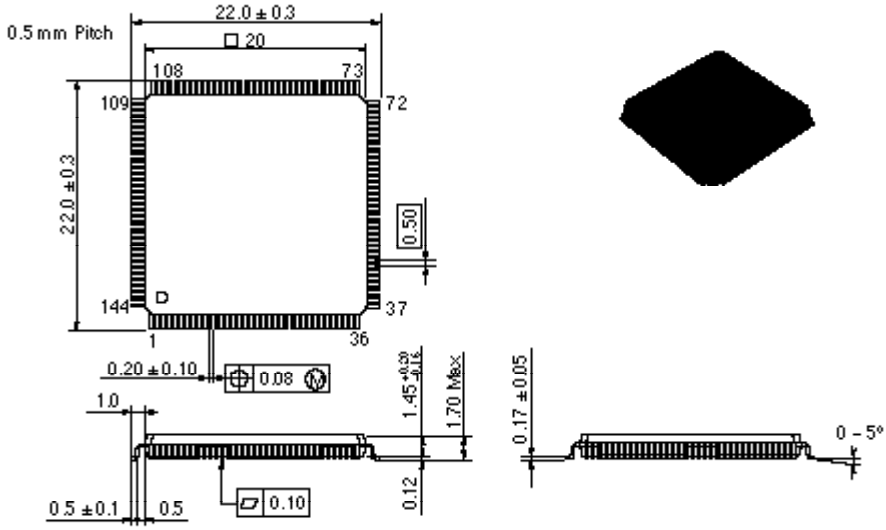


Code	FP-136
EIAJ	—
JEDEC	—

Applicable LSI	HD66850F

Package Information

FP-144A



Code	FP-144A
EIAJ	SC-596-A
JEDEC	—

Applicable LSI	HD66702

1. Damage from Static Electricity

Semiconductor devices are easily damaged by static discharges, so they should be handled and mounted with the utmost care. Precautions are discussed below.

1.1 Work Environment

Low relative humidity facilitates the accumulation of static charge. Although surface mounting package devices must be stored in a dry atmosphere to prevent moisture absorption, they should be handled and mounted in a work environment with a relative humidity of 50% or greater to prevent static buildup.

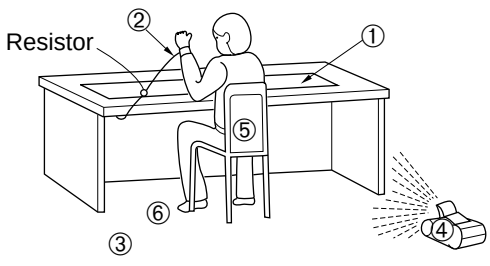
1.2 Preventing Static Buildup in Handling

1. Avoid the use of insulating materials that easily accumulate a static charge in workplaces where mounting operations are performed. In particular, charged objects can induce charges in semiconductors and finished PC boards even without direct contact. Recommended measures include the use of anti-static work garments, conductive carrier boxes, and ionized air blowers.

2. Ground all instruments, conveyors, work benches, floor mats, tools, and soldering irons to prevent the accumulation of static charges. Lay conductive mats (with a resistance on the order of 10^9 Ω to 10^{11} Ω) on workbenches and floors and ground them. (See figure 1.)

3. Personnel should wear grounding bracelets on their arms or legs. To prevent electric shocks, insert a resistor of 1 MΩ or greater in series as shown in figure 2.

4. If soldering irons are used, use low voltage (12 V to 24 V) soldering irons designed for use with semiconductors. Ground soldering iron tips



① High resistance conductive mat (grounded)
② Personal ground (bracelet)
③ High resistance conductive mat (grounded)
④ Humidifier
⑤ Anti-static work clothes
⑥ Anti-static shoes

Figure 1 Static Electricity Countermeasures for Semiconductor Handling

as shown in figure 3.

1.3 Preventing Semiconductor Discharges

Semiconductors are not damaged by static charges on the package or chip itself. However, damage will occur if the lead frame contacts a metal object and the charge dissipates. Grounding the metal object does not help in this situation.

The following measures should be taken.

1. Avoid contact or friction between semiconductors and easily charged insulators.

2. Avoid handling or working with semiconductors on metal surfaces. Semiconductors should be handled on grounded high resistance mats.

3. If a semiconductor may be charged, do not allow that device to contact any metal objects.

1.4 Precautions during Mounting

1. Grounded high resistance mats must be used when mounting semiconductors on PC boards. Ground mats before handling semiconductors. Particular caution is required following conductivity testing, since capacitors on the PC board may retain a charge.

2. PC boards can also acquire a static charge by contact, friction, or induction. Take precautions to prevent discharge through contact with transport boxes or other metal objects during transportation. Such precautions include the use of anti-static bags or other techniques for isolating the PC boards.

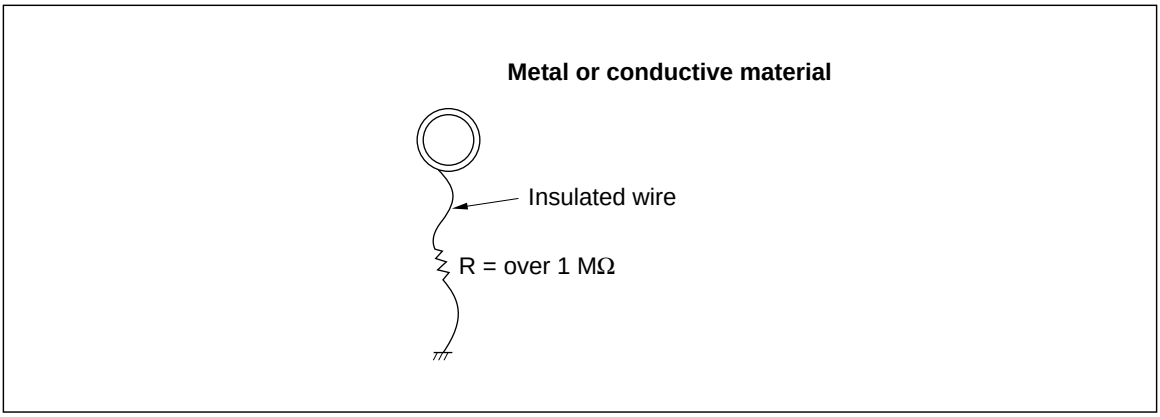


Figure 2 Personal Ground

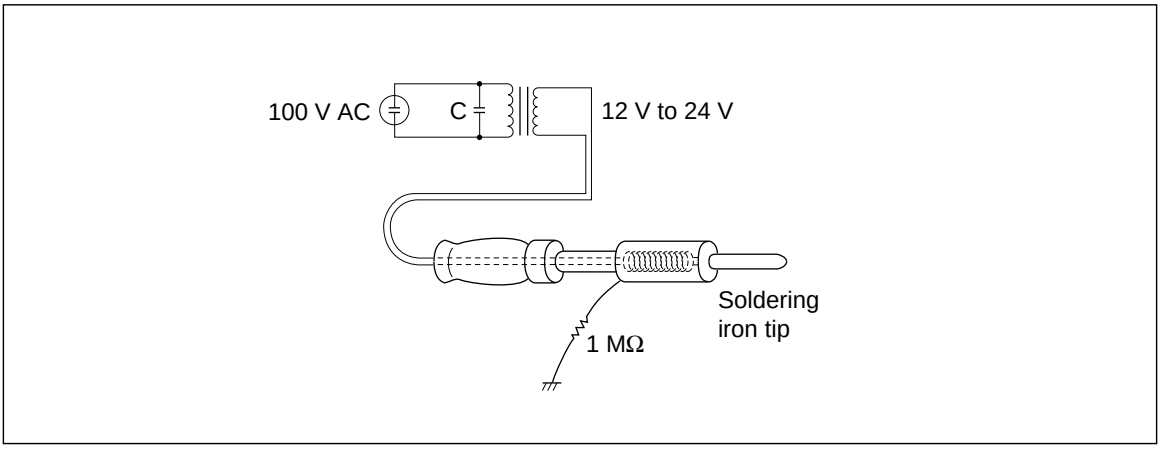


Figure 3 Soldering Iron Grounding Example

———— = D (t) ————

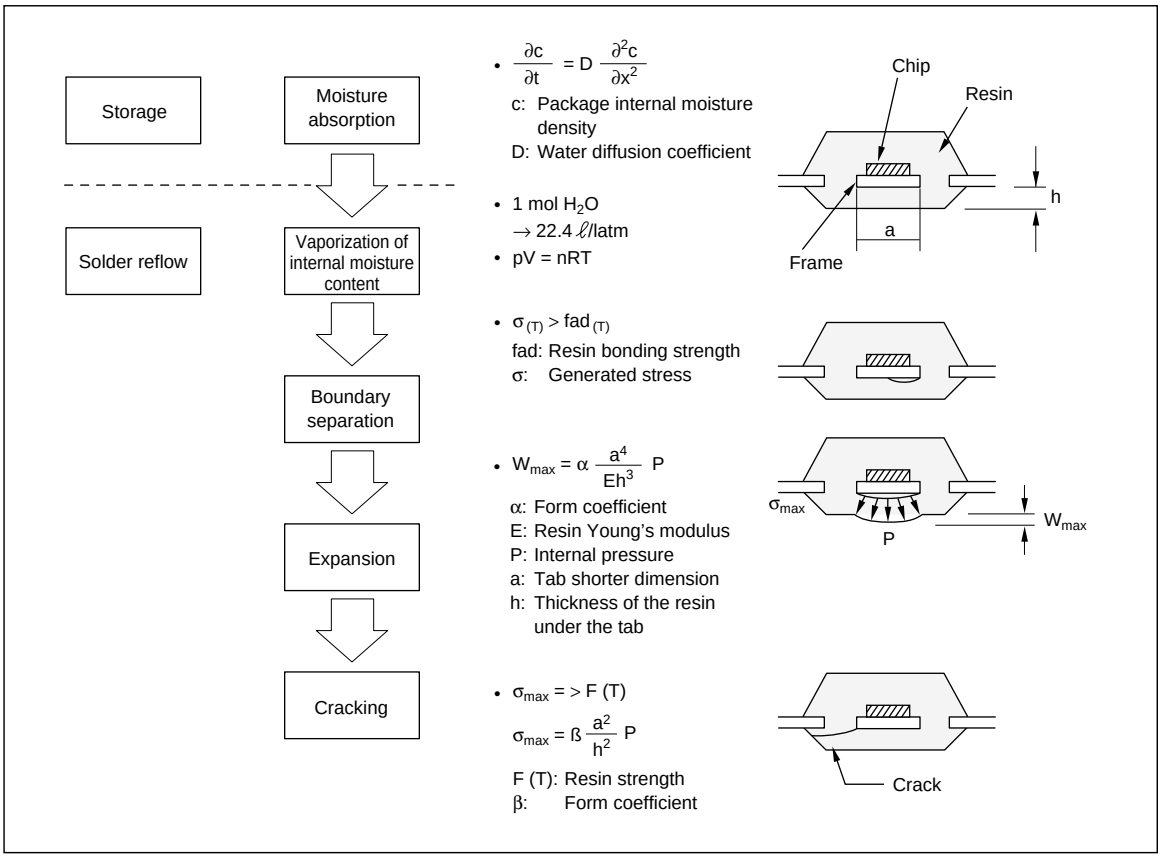


Figure 4 Package Crack Generation Mechanism

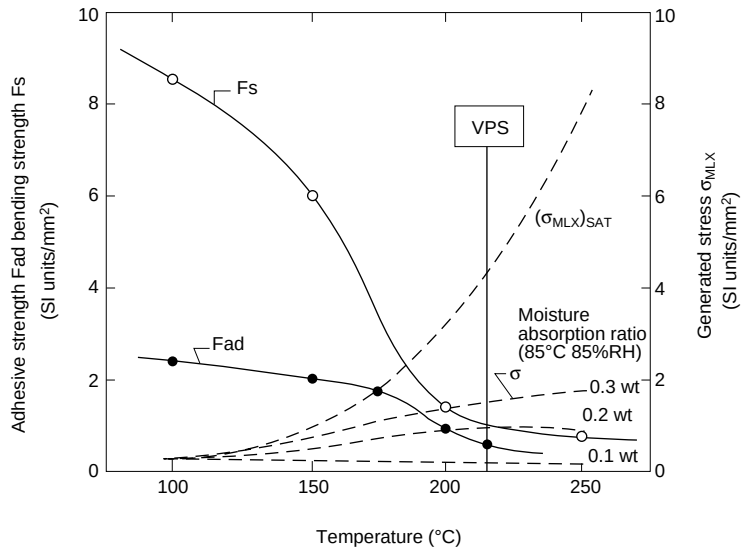


Figure 5 Temperature Dependence of Resin Adhesive Strength, Mechanical Strength, and Generated Stress

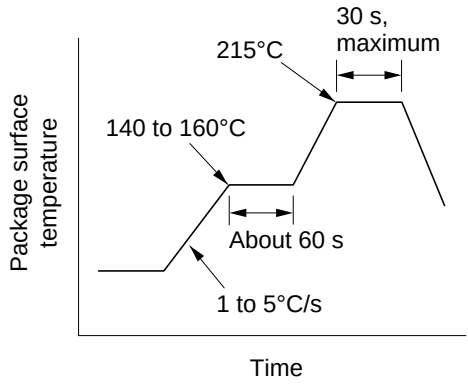
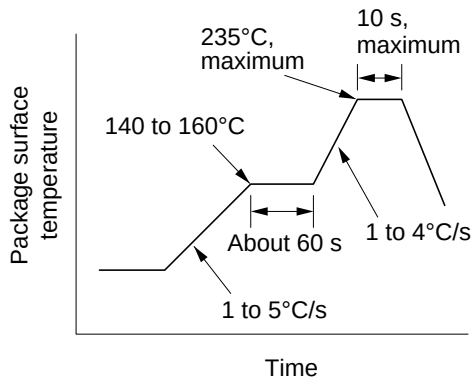
3. Recommended Soldering Conditions

Soldering temperature stipulations must be followed and the moisture absorption states of plastic packages must be carefully monitored to prevent degradation of the reliability of surface mount packages due to thermal shock. This section presents Hitachi's recommended soldering conditions.

3.1 Recommended Soldering Temperatures

See table 1.

Table 1 Recommended IC Soldering Temperatures

Method	Recommended Conditions	Notes
Vapor-phase reflow		
Infrared reflow Hot-air reflow		Since TSOP, TQFP, and packages whose body thickness is less than 1.5 mm are especially vulnerable to thermal shock, we recommend limiting the soldering conditions to a maximum temperature of 230°C for a maximum time of 10 seconds for these packages.

2. Precautions Prior to Reflow Soldering

Surface mount packages that hold large chips are weaker than insertion mount packages. Since the whole package is heated during the reflow operation, the characteristics described below should be considered when determining the handling used prior to reflow soldering and the conditions used in the reflow operation.

2.1 Package Cracking Mechanism in Reflow Soldering

Packages that have absorbed moisture are thought to crack due to the mechanism shown in figure 4. Moisture absorbed during storage diffuses through the interior of the package. When a package in this state is passed through the reflow furnace, that moisture rediffuses. Some of it escapes along the boundary between the resin and the frame. This can lead to boundary separation. As the pressure in this space increases the resin warps, finally resulting in a crack.

The Fick diffusion model can be used to calculate the diffusion of moisture in resin:

$$\frac{\partial C(x,t)}{\partial_t} \qquad \frac{\partial^2 C(x,t)}{\partial^2 x^2}$$

The volume of moisture absorbed by the package can be expressed as follows:

$$Q(t) = \int C(x,t)\,dx$$

The increase in internal pressure can be calculated from the moisture diffusion during reflow heating by using the C (x, t) function.

Figure 5 shows the relationships between the maximum stresses when packages of various moisture absorption states are heated, the adhesion strength between the resin and frame at various temperatures, and the strength of the resin itself. While this model indicates that cracks will result in this example when the moisture absorption ratio exceeds 0.2 wt% in a VPS (vapor phase soldering at 215°C) process, actual tests show that cracks result in packages with a moisture absorption ratio of 0.25 wt%. This indicates that the model is valid.

Therefore moisture management should focus on the moisture content in the vicinity of the frame.

Surface Mounting Package Handling Precautions

1. Package Temperature Distribution

The most common method used for mounting a surface mounting device is infrared reflow. Since the package is made of a black epoxy resin, the portion of the package directly exposed to the infrared heat source will absorb heat faster and thus rise in temperature more quickly than other parts of the package unless precautions are taken. As shown in the example in figure 6, the surface directly facing the infrared heat source is 20° to 30°C higher than the leads being soldered and 40°C to 50°C higher than the bottom of the package. If soldering is performed under these conditions, package cracks may occur.

To avoid this type of problem, it is recommended that an aluminum infrared heat shield be placed over the resin surface of the package. By using a 2-mm thick aluminum heat shield, the top and bottom surfaces of the resin can be held to 175°C when the peak temperature of the leads is 240°C.

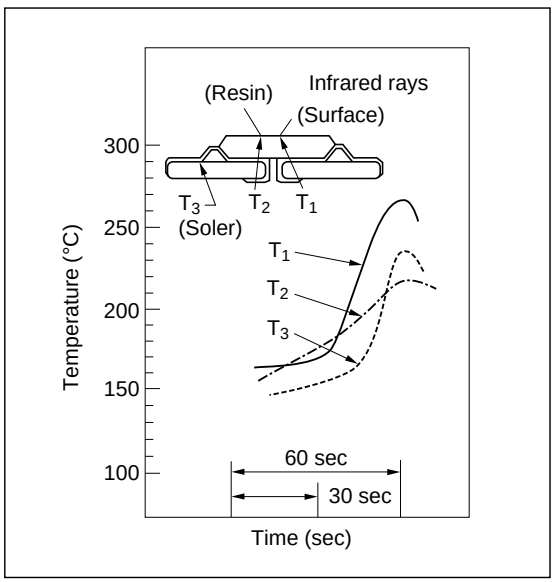


Figure 6 Temperature Profile During Infrared Heat Soldering (Example)

2. Package Moisture Absorption

The epoxy resin used in plastic packages will absorb moisture if stored in a high-humidity environment. If this moisture absorption becomes excessive, there will be sudden vaporization during soldering, causing the interface of the resin and lead frame to spread apart. In extreme cases, package cracks will occur. Therefore, especially for thin packages, it is important that moisture-proof storage be used.

To remove any moisture absorbed during transportation, storage, or handling, it is recommended that the package be baked at 125°C for 16 to 24 hours before soldering.

3. Heating and Cooling

One method of soldering electrical parts is the solder dip method, but compared to the reflow method, the rate of heat transmission is an order of magnitude higher. When this method is used with plastic items, there is thermal shock resulting in package cracks and a deterioration of moisture-resistant characteristics. Thus, it is recommended that the solder dip method not be used.

Even with the reflow method, an excessive rate of heating or cooling is undesirable. A rate in temperature change of less than 4°C/sec is recommended.

4. Package Contaminants

It is recommended that a resin-based flux be used during soldering. Acid-based fluxes have a tendency of leaving an acid residue which adversely affects product reliability. Thus, acid-based fluxes should not be used.

With resin-based fluxes as well, if a residue is left behind, the leads and other package parts will begin to corrode. Thus, the flux must be thoroughly washed away. If cleansing solvents used to wash away the flux are left on the package for an extended period of time, package markings may fade, so care must be taken.

The precautions mentioned above are general points to be observed for reflow. However, specific reflow conditions will depend on such factors as the package shape, printed circuit board type, reflow method, and device type.

For details on surface mounting small thin packages, please consult the separate manual available on mounting. If there are any additional

Features of TCP (TAB Technology)

The structure and materials used by Tape Carrier Package (TCP) give it the following features as compared with conventional packages:

Thin, Lightweight, and Fine Pitch

With thickness less than 1 mm and fine-pitch leads, a reduced pad pitch on the device enables more functionality in a package of equivalent size. Specifically, these features enable:

- Thin and high definition LCM (Liquid Crystal display Module)
- Lightweight and ultra-high pin count systems

Flexible Design

The following can be tailored to the design of the system (e.g. mother board design):

- Pattern layout
- TCP design

TCP Applications

Thinness, ultra-high pin count, and fine pitch open up new possibilities of TCP applications for compact and highly functional systems. Figure 1 shows some applications of TCP-packaged chips.

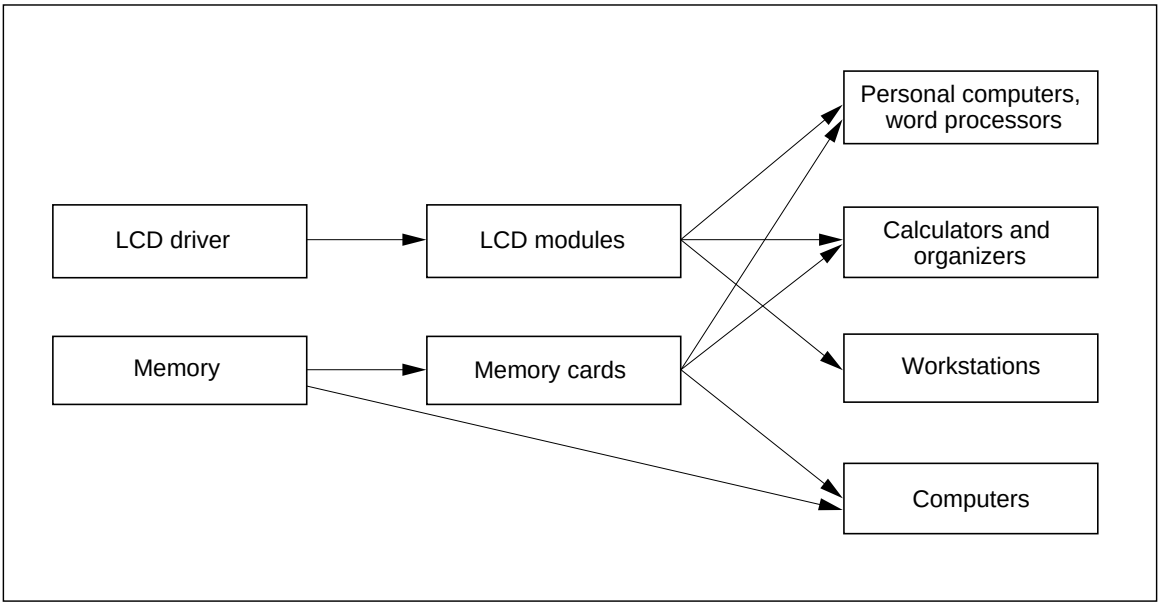


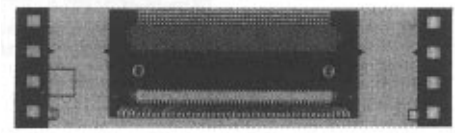
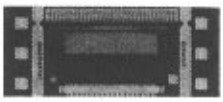
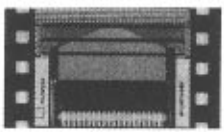
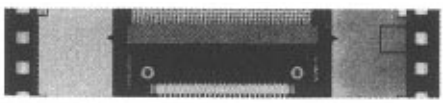
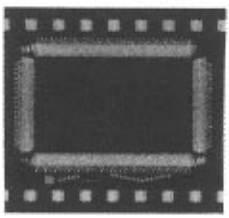
Figure 1 Examples of TCP-Packaged Chip Applications

Hitachi TCP Products

TCP for Hitachi LCD Driver

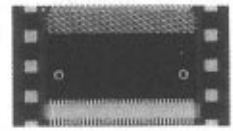
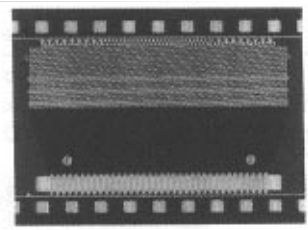
Hitachi offers tape-carrier-packaged LCD drivers for LCD modules ranging from miniature to large sizes. Table 1 shows some examples of standard tape carrier packages for LCD drivers. Hitachi LCD drivers combine a device that can withstand high voltages and provide high definition with a tape carrier package that promises excellent reliability, making possible applications that would not be feasible with a conventional QFP. For material specifications of the products in table 1, s e e table 3.

Table 1 TCPs for Hitachi LCD Drivers

	Function		Appearance			
Application	Drive	Signal Output	Product Code	Total Pin Count (Output)	Outer Lead Pitch	Remarks
TFT*1	Column only	Analog				
			HD66330TA0	236 (192)	0.16 mm	
Color STN*2 liquid crystal	Column only	Digital				
			HD66110STB2	191 (160)	0.092 mm	
Color STN*2 liquid crystal	Column only	Digital				Outer lead pitch: 0.074 mm products are also available
			HD66120TA0	269 (240)	0.07 mm	
Color STN*2 liquid crystal	Common only	Digital				Outer lead pitch: 0.250 mm products are also available
			HD66115TA0	181 (160)	0.18 mm	
Small liquid crystal	Column and common	Digital				Built-in controller (on-chip RAM)
			HD66108T00	208 (165)	0.4 mm	

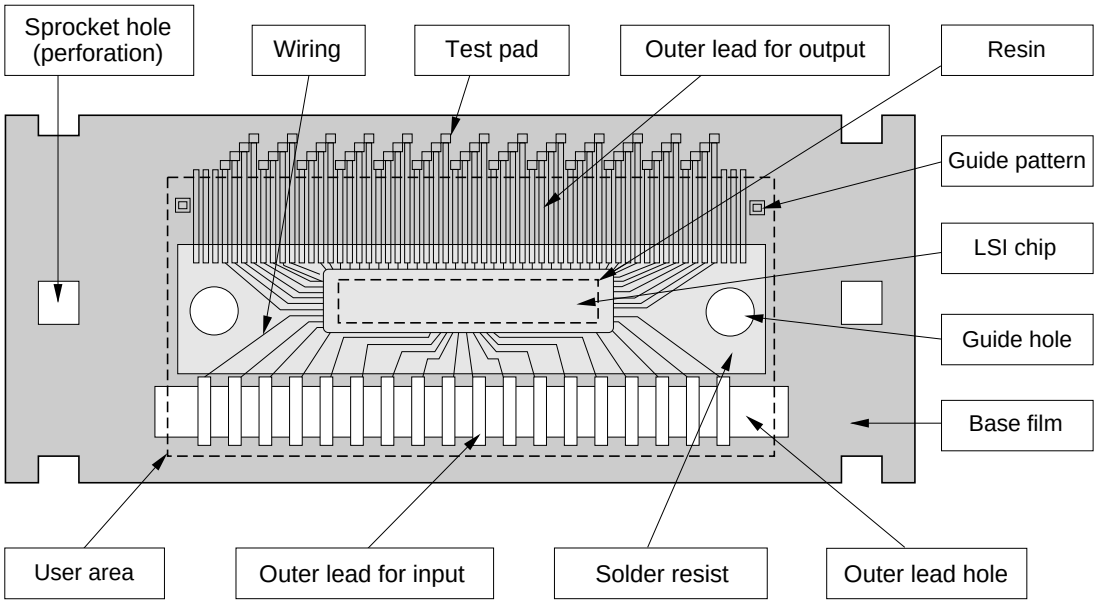
Notes: 1. TFT: Thin Film Transistor
2. STN: Super Twist Nematic

Table 1 TCPs for Hitachi LCD Drivers (cont)

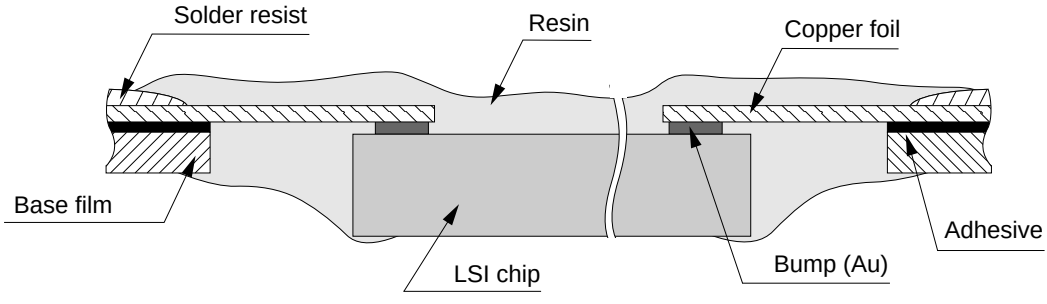
Function			Appearance			
Application	Drive	Signal Output	Product Code	Total Pin Count (Output)	Outer Lead Pitch	Remarks
Small liquid crystal	Column and common	Digital				
			HD66712TA0	128 (94)	0.24 mm	
						Folding TCP
			HD66712TB0	128 (94)	0.3 mm	

TCP External View and Cross-Sectional Structure

TCP Components



Cross-Sectional Structure



TCP Materials and Features

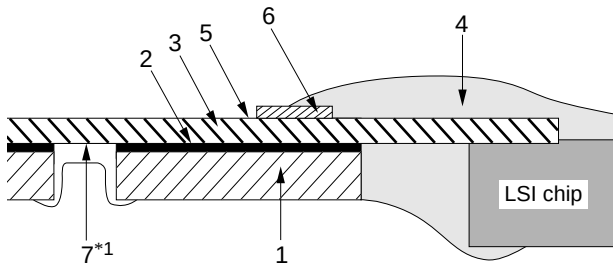
TCP Material Specifications: Table 2 lists Hitachi TCP material specifications. Ask us if you require other materials. In this case, use TCP ordering manual [ADE-801-001 (O)].

Table 3 lists current material specifications for various Hitachi products.

Table 2 Hitachi TCP Material Specifications

No.	Item	Specifications
1	Base film	UPILEX® S-type: thickness 75 µm ±5 µm KAPTON® V-type: thickness 125 or 75 µm ±5 µm
2	Adhesive	Toray #5900
		TOMOEGAWA E-type
3	Copper foil	Rolled copper: thickness 35 or 25 µm ±5 µm
		Electro-deposited copper: thickness 35 or 25 µm ±5 µm
4	Resin	Epoxy resin
5	Outer lead plating	Tin
6	Solder resist	Epoxy solder resist
7	Solder resist on rear surface of folding TCP slit	Polyimide solder resist

Cross-sectional view



*1: Folding TCP only

Table 3 Material Specifications for Hitachi Products

Product Code	Application	Base Film	Adhesive	Copper Foil	Outer Lead Plating
HD66330TA0	TFT	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin
HD66110STB2	Color STN	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin
HD66120TA0	Color STN	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin
HD66115TA0	Color STN	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin
HD66108T00	Small liquid crystal	KAPTON® V	Toray #5900	Rolled copper	Tin
HD66712TA0	Small liquid crystal	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin
HD66712TB0	Small liquid crystal	UPILEX® S	TOMOEGAWA E-type	Electro-deposited copper	Tin

Properties of Materials: Properties of Hitachi TCP materials are as follows.

1. Base film

   The properties of base film are shown in table 4. Hitachi currently adopts UPILEX® S, which exhibits high rigidity and super dimensional stability with respect to temperature changes compared with conventional KAPTON® V.

2. Copper foil (copper wiring)

   The properties of rolled foil and electro-deposited foil are shown in table 5. Hitachi plans to adopt electro-deposited foil due to its excellent elongation properties at room temperature (RT) compared with conventional rolled foil.

Table 4 Properties of Base Film (See references 1 and 2, page 28)

Property		UPILEX® S (Ube Industries, Ltd.)	KAPTON® V (Du Pont-Toray Co., Ltd.)
Coefficient of linear expansion $\times 10^{-5}$/°C	To 100°C	0.8	—
	To 200°C	1.0	2.6
Tensile modules (MPa)		8826.0	3481.4

Table 5 Properties of Copper Foil (See reference 3, page 28)

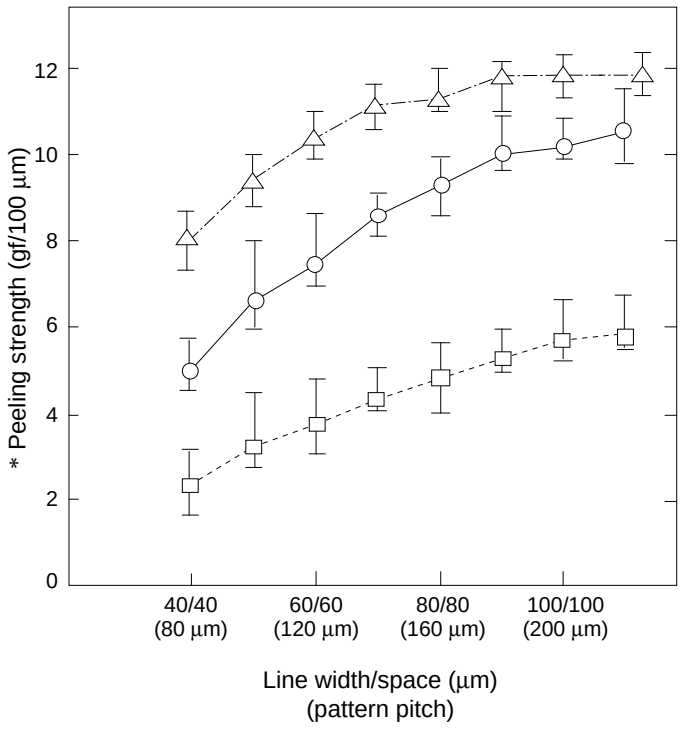
Property	Sampling Condition	Rolled Foil (Hitachi Cable, Ltd.) CF-W5-1S-LP	Electro-Deposited Foil (Mitsui Mining & Smelting Co., Ltd.) 3EC-VLP
Tensile strength at RT (MPa)	Raw foil	421.7	538.4
Elongation at RT (%)	Raw foil	1.0	10.1
Tensile strength at 180°C (kgf/mm^2)	Raw foil	229.5	249.1
Elongation at 180°C (%)	Raw foil	7.7	7.0

Note: Data from film suppliers.
Number of measured samples: 2 pieces each
1 MPa = 1.01972×10^{-1} kgf/mm^2

3. Adhesive

The relationship between peeling strength (adhesive/electro-deposited foil) and lead width is shown in figure 2. Hitachi adopts the following two combinations because of their higher peeling strength.

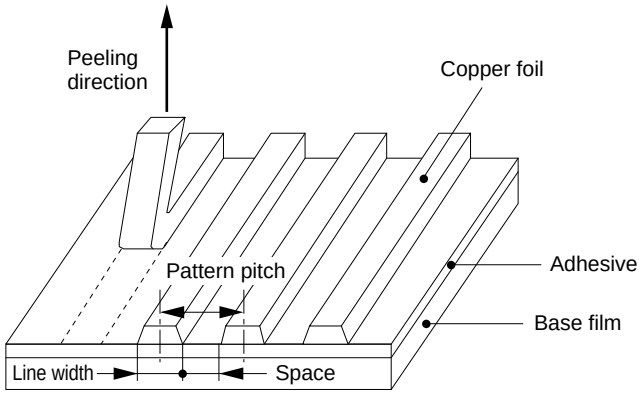
— Adhesive TOMOEGAWA E-type/electro-deposited foil
— Adhesive Toray #5900/rolled foil



	Adhesive	Copper foil
△	TOMOEGAWA E-type	Electro-deposited foil
○	Toray #5900	Rolled foil
□	TOMOEGAWA E-type	Rolled foil

* Peeling strength

— How to measure —



Measuring method: 90° peel

Measuring condition: 25°C

Number of measured samples:
Five pieces are measured for each specification, and two leads are measured for each piece.

Figure 2 Relationship between Peeling Strength and Lead Width

Fine-Pitch Bump Formation

Bumps are essential in TCP products; they are the foundation of TAB technology and have excellent corrosion resistance in their structure. When the current trend toward high-performance chips with ultra-large pin-out began driving pad counts upward (and reducing pad pitch), Hitachi was quick to develop a volume production process for forming fine-pitch bumps.

Figure 3 shows the Hitachi TCP bump structure. Figure 4 shows a flowchart of the bump formation process.

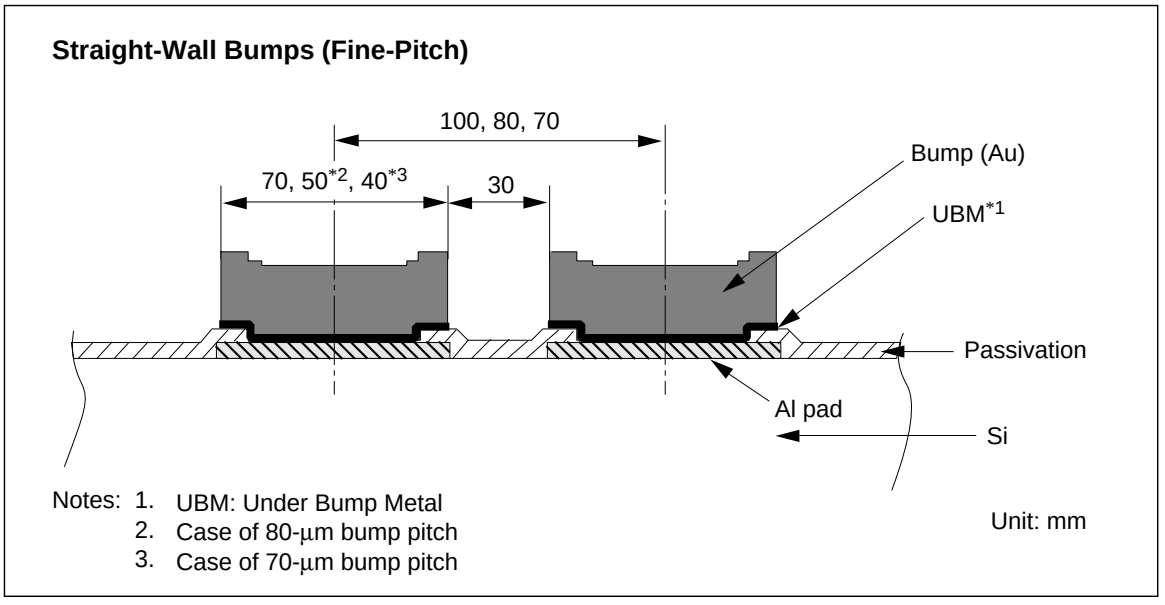


Figure 3 Hitachi TCP Bump Structure

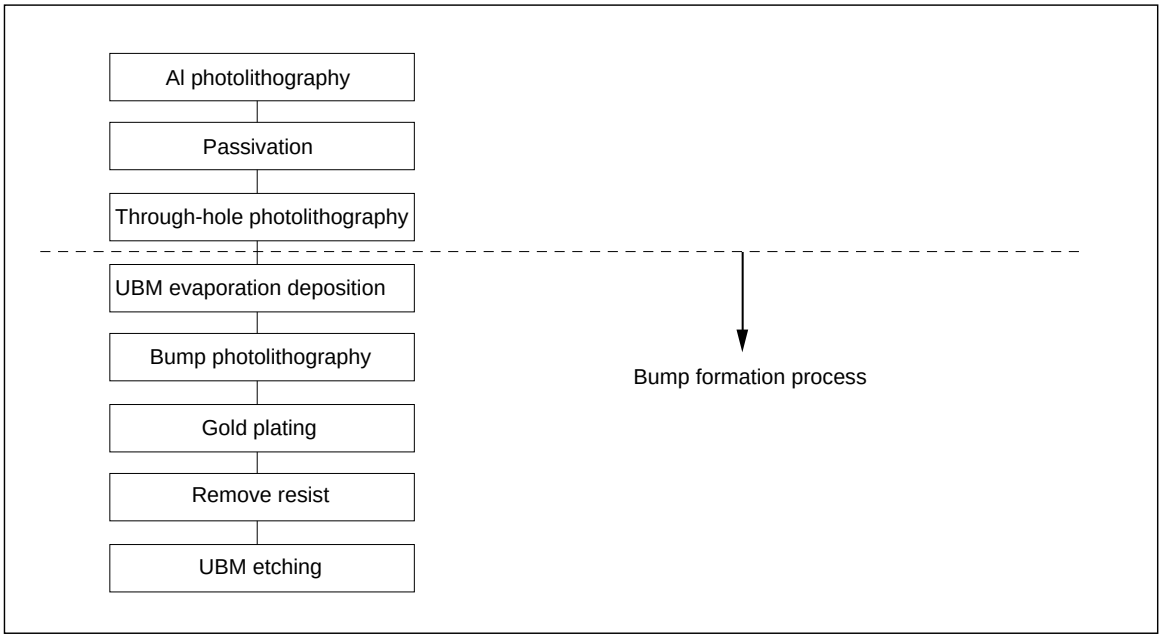


Figure 4 Bump Formation Flowchart

TCP Fabrication Flow

TCP Tape: TCP tapes are purchased from tape manufacturers. In many cases, the quality of TCP products depends critically on the quality of the tape, so in addition to evaluating constituent materials, Hitachi strictly controls the stability of the tape fabrication process.

TCP Fabrication Process: The TCP fabrication process starts from wafers (or chips) with bumps, and a patterned tape. After being bonded by a high-precision inner lead bonder, the chips are sealed in resin. Figure 5 shows the standard fabrication process for TCPs used in Hitachi LCDs.

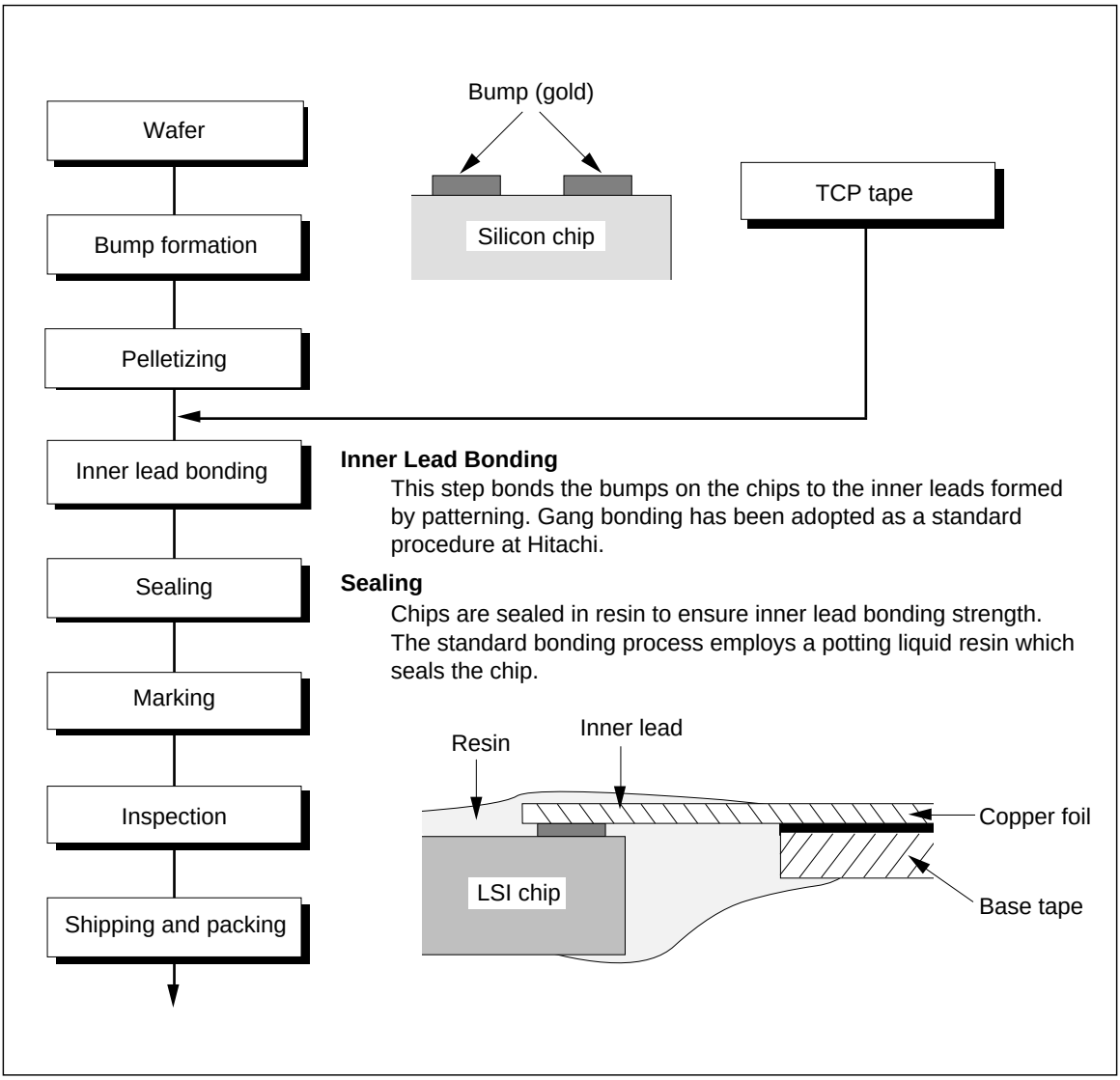


Figure 5 Standard Fabrication Process for TCPs Used in Hitachi LCDs

Packing

Packing Format: TCP products are packed in moisture-proof packages. A reel wound with TCP tape is sealed in an opaque antistatic sheet with N_2 to protect the product from mechanical shock and then packed into a carton before delivery to ensure the solderability of lead plating.

Labels which indicate the product name, quantity, and so on are placed on the reel, antistatic sheet, and carton. Figure 6 shows the TCP packing format.

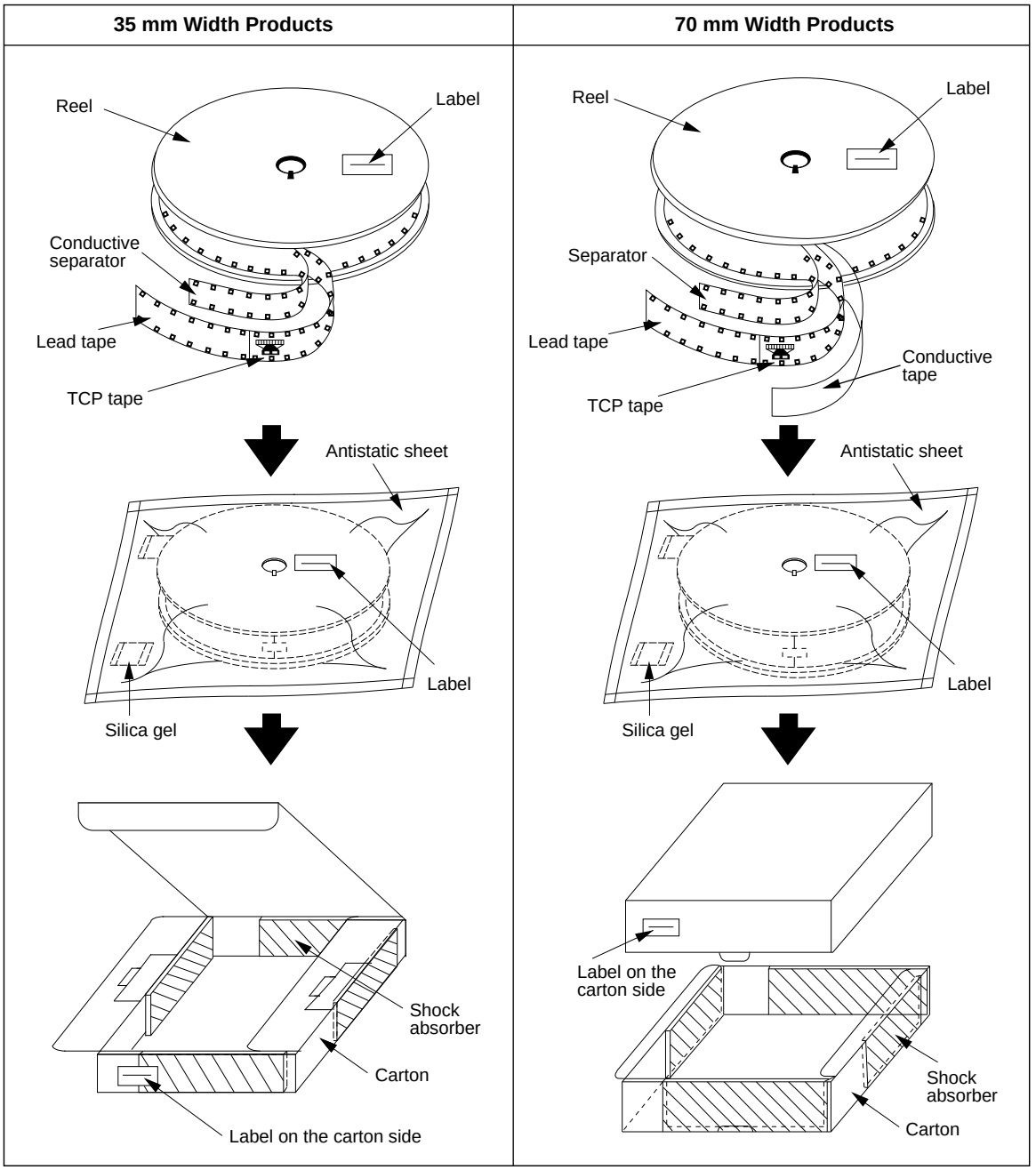


Figure 6 Packing Format

Tape Specification:

	Width of Tape	
	35 mm	**70 mm**
TCP tape	40 m	40 m
Lead tape	2 +1/–0.5 m added to both ends of the TCP	2 +1/–0.5 m added to both ends of the TCP
Conductive tape	—	40 m
Separator	—	40 m
Conductive separator	40 m	—

Note: The lengths of the TCP tape, conductive tape, and separator may vary slightly depending on the quantity of the product on the tape.

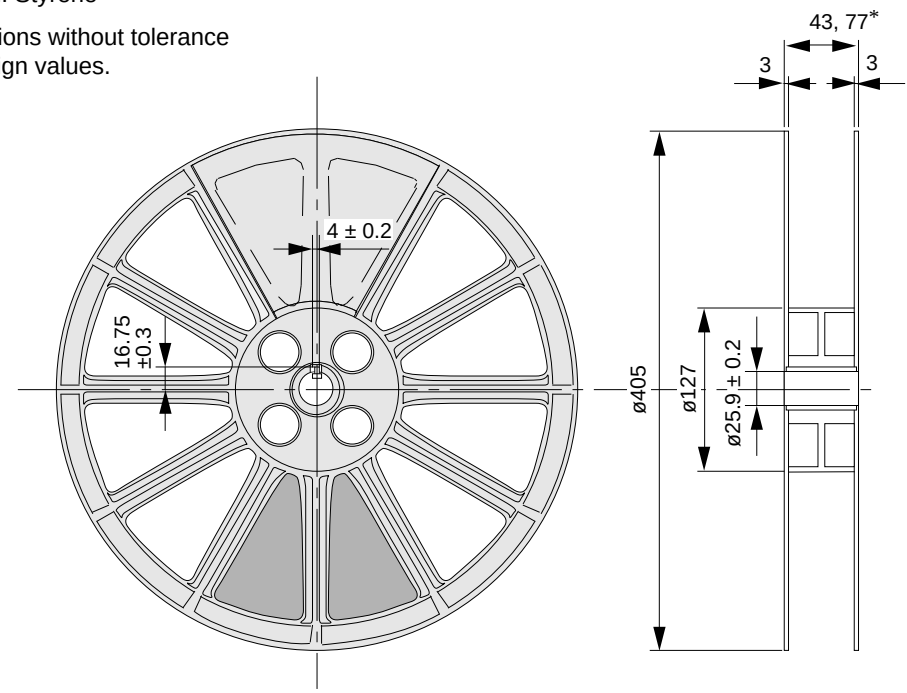
Reel Specification: Figure 7 shows reel dimensions.

For recycling purpose, we would appreciate it if you return the reel and separator to us after use.

Units: mm

Material: Styrene

Dimensions without tolerance are design values.



Note: * For 70 mm width tape.

Figure 7 Reel Dimensions

TCP Winding Direction: Figure 8 shows one way of winding TCPs. The combination of two product directions when pulling it out from the reel and placement of the patterned face on either the front or back of the tape makes for four types of TCP winding directions.

The winding direction is an essential specification which affects the chip punching machine and assembly equipment during the packaging process. As the wind direction differs according to the product, please check the delivery specification before using TCP.

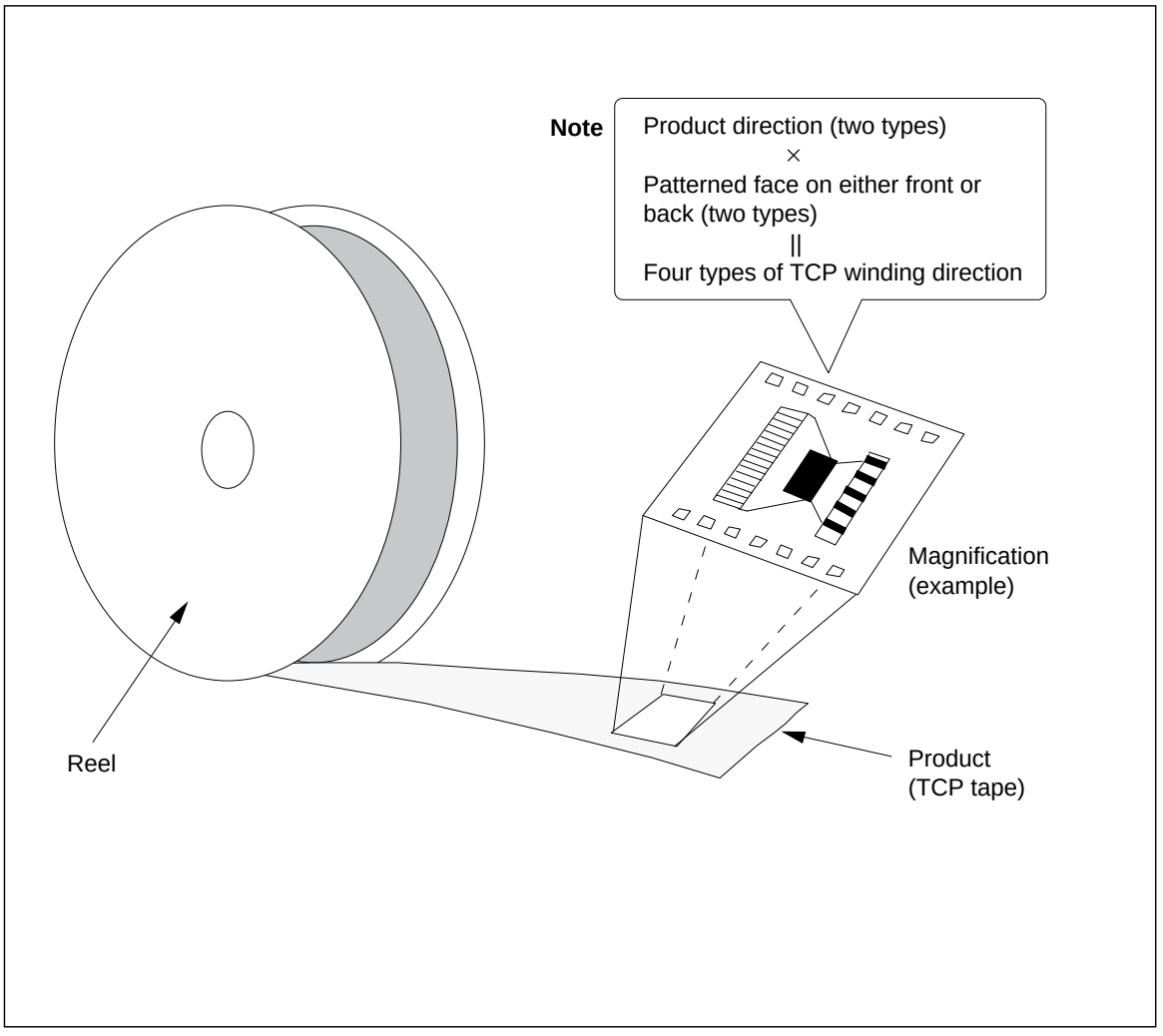


Figure 8 Example of TCP Winding Direction

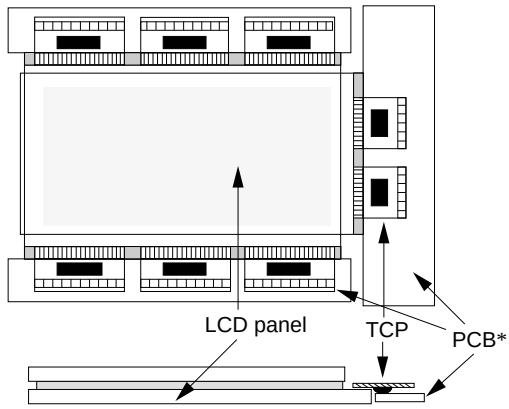
TCP Mounting Methods

TCP Mounting Structure

Typical example of an LCM structure using TCPs is illustrated in figure 9.

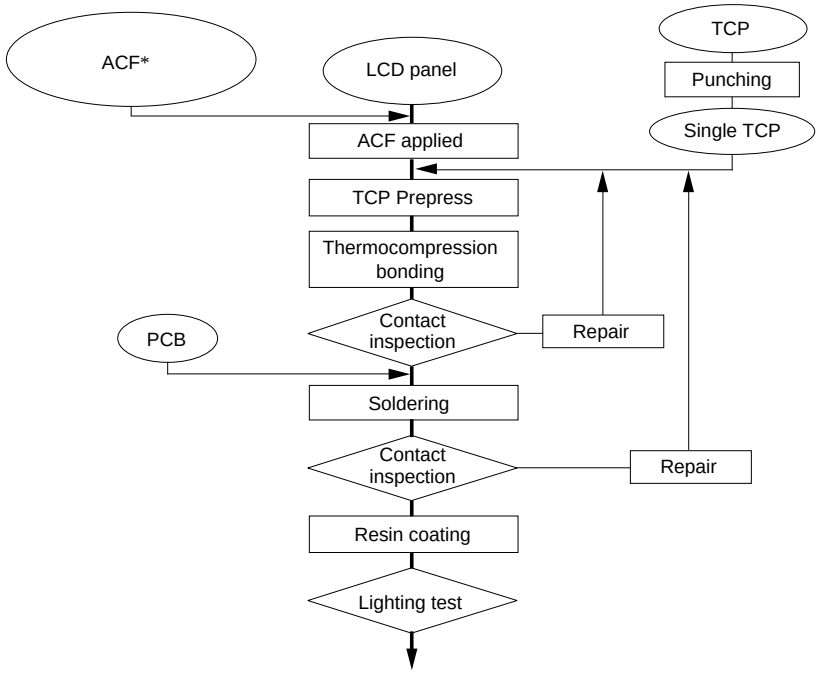
Basic Mounting Process

See figure 10.



Note: * PCB: Printed circuit board

Figure 9 LCM Structure



Note: * ACF: Anisotropic conductive film

Figure 10 TCP OLB (Outer Lead Bonding) Basic Flowchart

Process Outline

An outline of LCM assembly process using TCPs is given in figure 11.

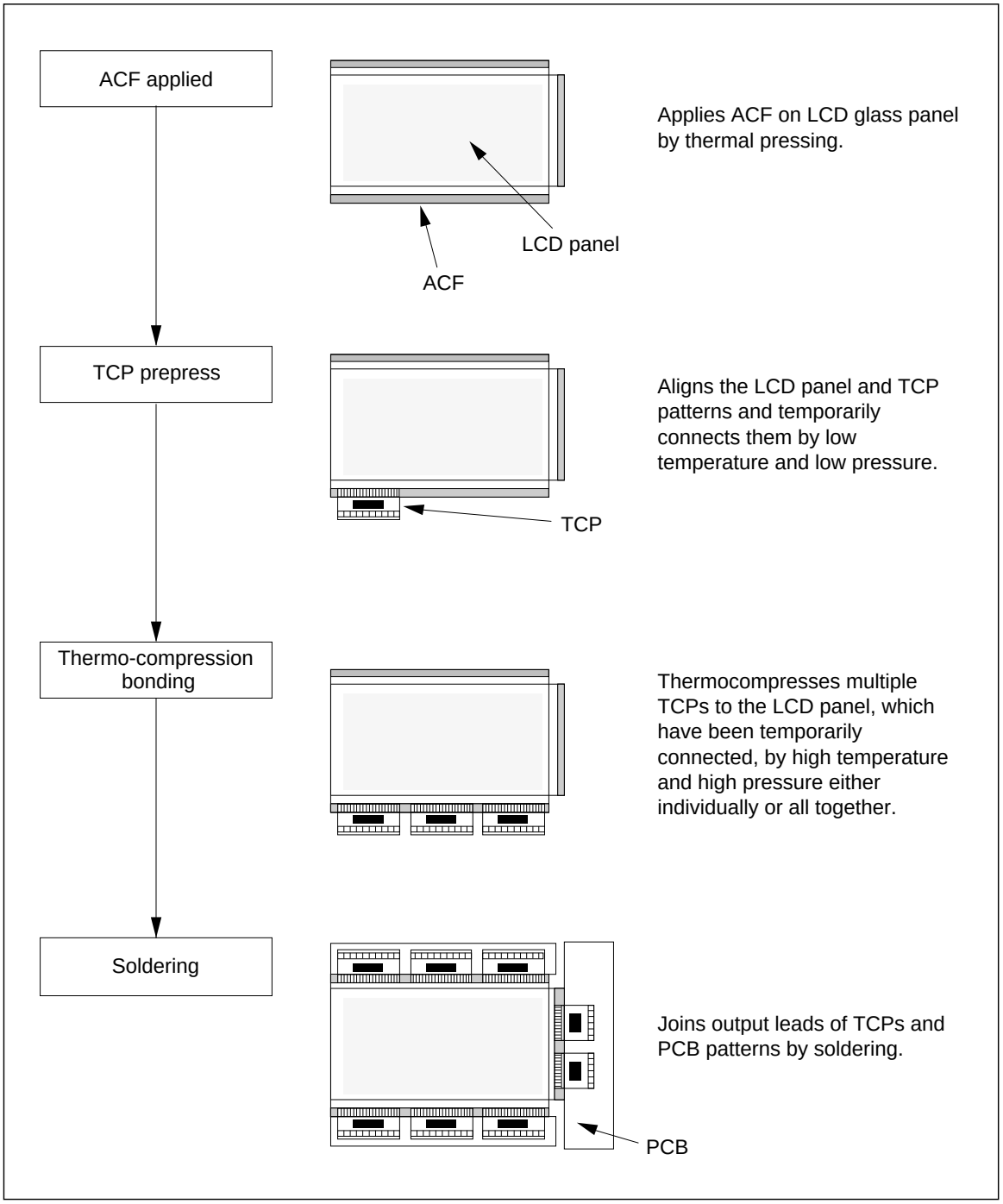


Figure 11 Outline of LCM Assembly Process

TCP Mounting Conditions

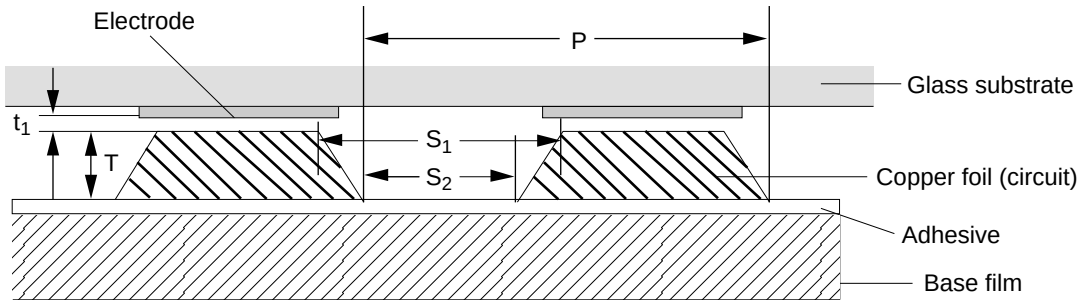
Mounting TCPs on LCD Panels (See reference 4, page 28): ACF is an adhesive film that can connect electrodes on an LCD glass panel with output leads of TCPs. There are two types of ACFs:

- One whose thermosetting and thermoplastic properties make handling easier (such as in repair) and reduces the stresses caused by temperature changes.
- One whose thermosetting properties provide low connection resistance and high thermostability.

Please select ACF depending on the type of application.

1. Selection of ACF thickness

   An appropriate ACF thickness must be selected depending on the height, line width and space width of the circuit to be connected; a rough calculation formula for obtaining a proper ACF thickness is shown below.



$$\text{ACF thickness before connection } t_0 = \frac{\frac{S_1 + S_2}{2}}{P} \times T + t_1 + \alpha$$

t_1: ACF thickness after connection (2 µm)
T: Circuit height
P: Pitch
S_1: Space width (top)
S_2: Space width (bottom)
α: Correction value
AC-6073, AC-6103 — 0.15T
AC-7104, AC-7144 — 0.25T

Incomplete filling can occur in the space if ACF thickness is too thin, while if too thick, connection reliability becomes poor since conductive particles are not flattened out. It is necessary to select an appropriate ACF thickness. Some adjustment of ACF thickness can be controlled by bonding conditions (especially pressure).

2. Laminating and bonding conditions

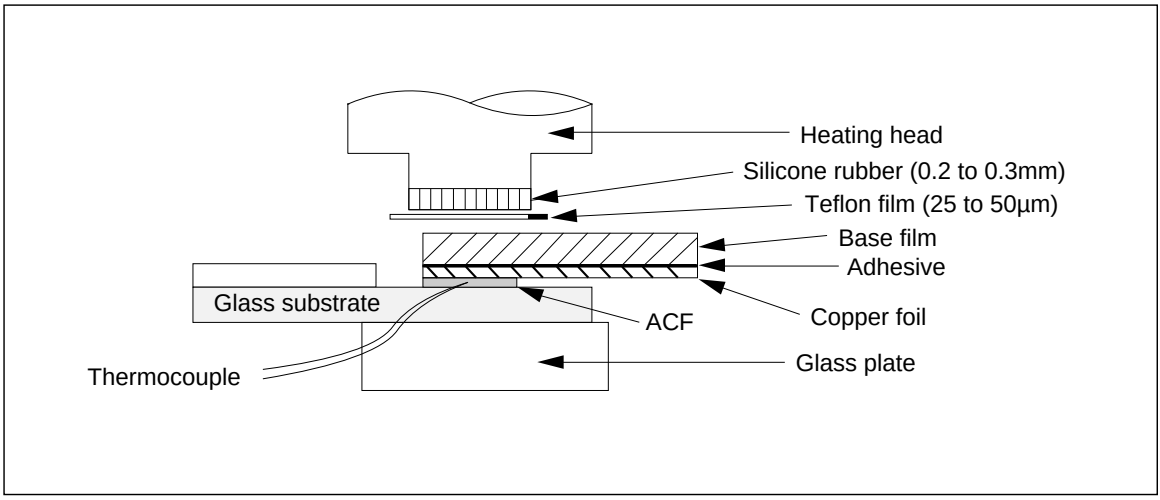
It is necessary to optimize bonding conditions according to ACF, TCP and glass panel specifications. The bonding conditions adopted by ANISOLM® (Hitachi Chemical Co., Ltd.) are shown in table 6 for reference. Please determine your optimum bonding conditions based on the following.

Table 6 Bonding Conditions of ANISOLM®

Item				Unit		Mixture of Thermosetting and Thermoplastic				Thermosetting				Remarks
						AC-6073		AC-6103		AC-7104		AC-7144		
Standard specifications	Min. pitch	Line	Resolution	μm	Line/mm	70	7	50	10	50	10	35	14	
		Space		μm		70		50		50		35		
	Thickness			μm		22		22, 18		25		16		
	Width			mm		3, 2.5, 2				3, 2.5, 2				
	Length			m		50				50				
	Color					Transparent (gray)				Transparent (gray)				
	Core diameter			mm		18.5				18.5				
Bonding conditions	Laminating	Temperature		°C		80 to 100				70 to 90				Temperature on ANISOLM®
		Pressure		MPa		1				1				
		Time		s		5				5				
	Bonding	Temperature		°C		170 to 190				160 to 180				Temperature on ANISOLM®
		Pressure		MPa*		2				2		3		
		Time		s		20				20				

Note: * 1 MPa = 1.01972×10^{-1} kgf/mm^2

Measuring Method of ACF Temperature Profile (example)



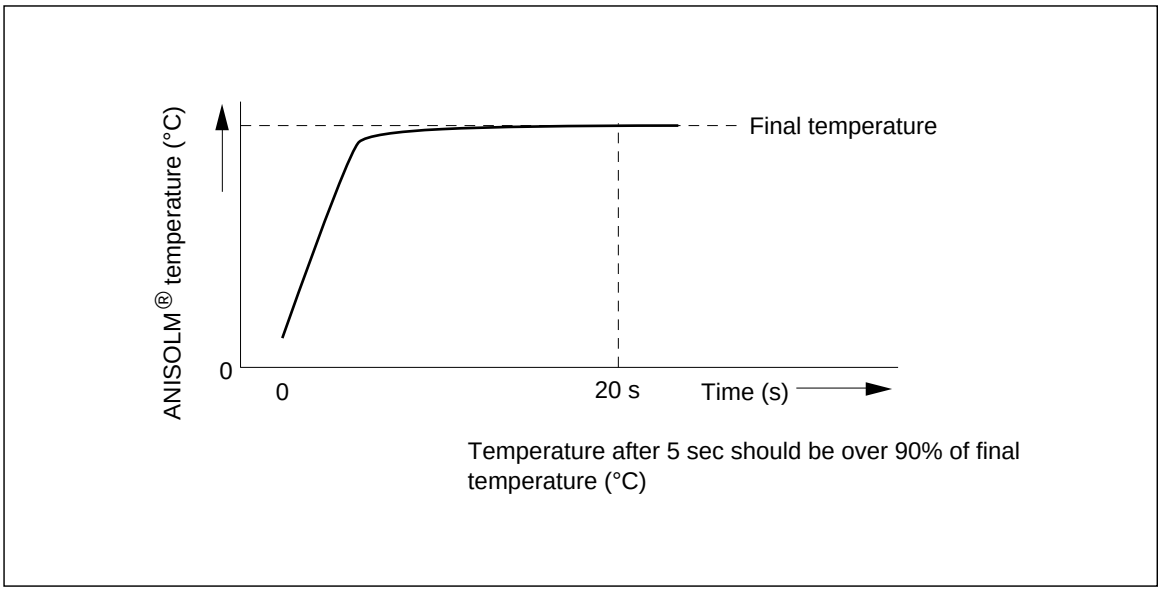
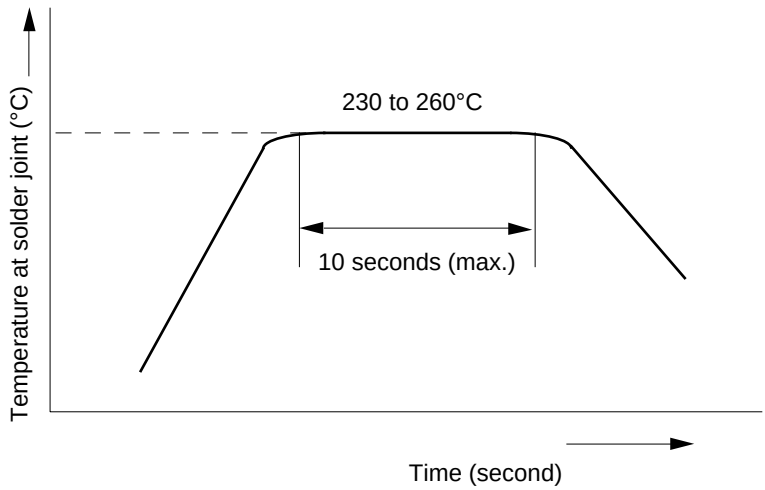


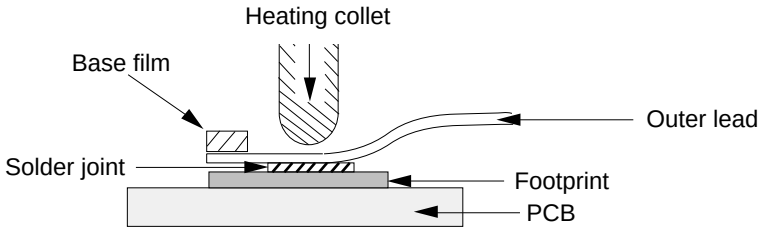
Figure 12 Bonding Temperature Profile

Soldering Conditions: Solder TCPs on the PCB under the following conditions. If soldering temperature is low, solder may not melt. However, if soldering temperature is too high, solder may not adequately spread over the leads owing to their oxidized surfaces, and/or the leads plating may become attached to the heating collet. In the latter case, copper foil of leads may become exposed. Please determine adequate soldering conditions for mass production carefully.

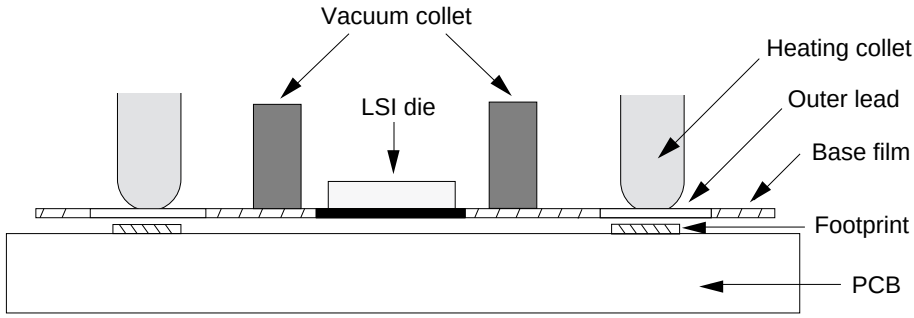
- Soldering temperature (at solder joint): 230 to 260°C
- Soldering time: 10 seconds max.

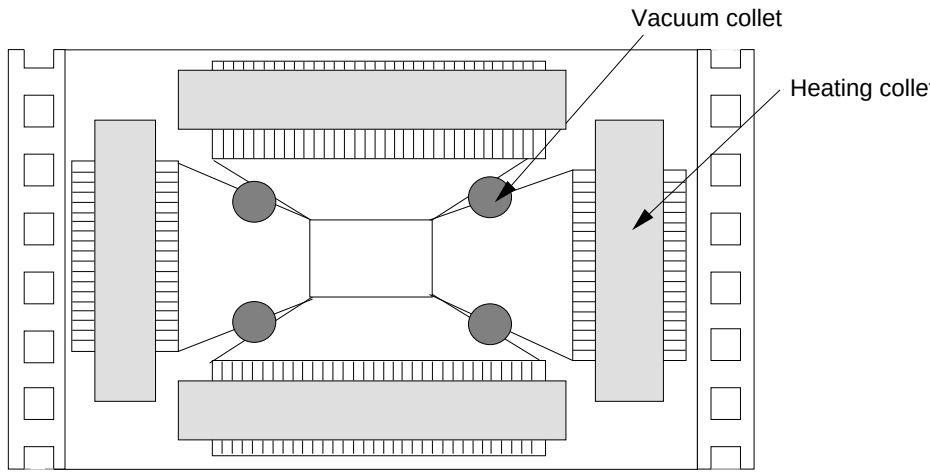


Note 1: Temperature at solder joint is normally 30 to 50°C lower than the heating collet temperature. Soldering temperature has a great impact on the quality of the products. Operating conditions should therefore be specified after examining the temperature relationship between the tip of the heating collet and solder joint.



Note 2: In case of soldering quad type TCPs, please fix the TCPs using vacuum collets or equivalent to prevent base film warpage and circuit position misalignment.





Storage Restrictions

1. Packed TCP products should be used within six months.

2. TCP products removed from the antistatic sheet should be stored in N_2 having a dew point of –30°C or lower. However, they should be used as soon as possible after removal, because solderability of leads plated with Sn or solder decreases with time.

Handling Precautions

Electrical Handling

1. Anti-electrostatic discharge measures

   TCP products require the following care beyond what is required for non-TCP products.

   - Give special attention to ion-blow and grounding especially when removing TCP products from the reel, since they easily collect static electricity because of the base film. If TCP products become charged, discharge the electricity little by little using the ion-blow; rapid discharge may damage the devices.

   - Handle the product so that static electricity is not applied to outer leads. Depending on the equipment used, this may require taking proper anti-electrostatic discharge measures, such as not allowing the tapeguide to contact the outer leads.

2. Outer lead coating

   Outer leads should be coated with resin or other appropriate materials to prevent short-circuits and disconnections due to corrosion. Conductive foreign particles can easily cause short-circuits since lead spacing for TCP products is much narrower than that for non-TCP products. Disconnections from corrosion can also easily occur due to solder flux or similar materials adhering to leads while mounting the products on a board. This is because TCP product leads are formed by bonding very thin copper foil to the base film in order to attain high-density mounting.

3. To prevent electric breakdown when mounting TCP products on a board, do not allow any electrical contact with the die's bottom surface. These types of failures easily occur since TCP products have a bare Si monocrystal on the die's bottom surface in order to make the product as thin as possible.

   To prevent degradation of electrical characteristics, do not expose TCP products to sunlight.

Mechanical Handling

1. To prevent die cracks when mounting TCP products on a board, do not allow any physical contact with the die's bottom surface. These types of failures easily occur since TCP products have a bare Si monocrystal on the die's bottom surface in order to make the product as thin as possible.

2. Handle TCP products carefully to avoid bending the leads from base film transformation.

3. Do not bend TCP products since this may cause

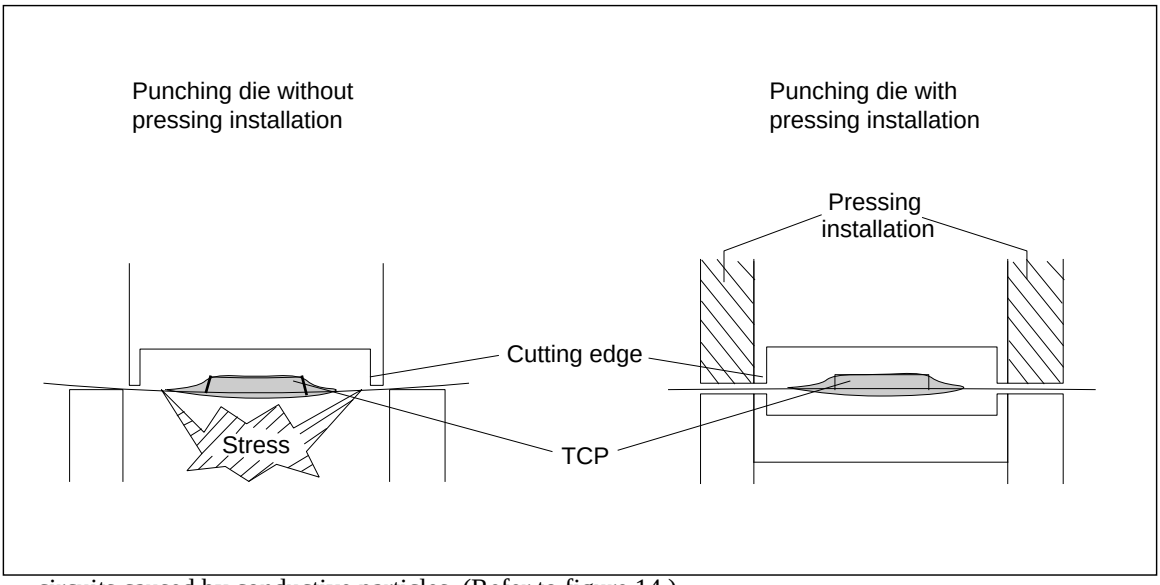
cracks in the solder resist.

4. Punching

Punching the continuous base film to extract single TCP products requires the following care.

- Align each product correctly according to tape perforations (sprocket holes).
- Use a metal punching die with pressing installation to prevent resin cracks and reduce cutting stresses in the outer leads. (Refer to figure 13.)
- Determine the punching position so that the cutting edge does not touch the molding area based on the relationship between maximum molding area (specified in the design drawing) and the punching die accuracy.

Punch TCP products in the section where outer leads are straight (not slanted) to prevent short-circuits caused by conductive particles. (Refer to figure 14.)



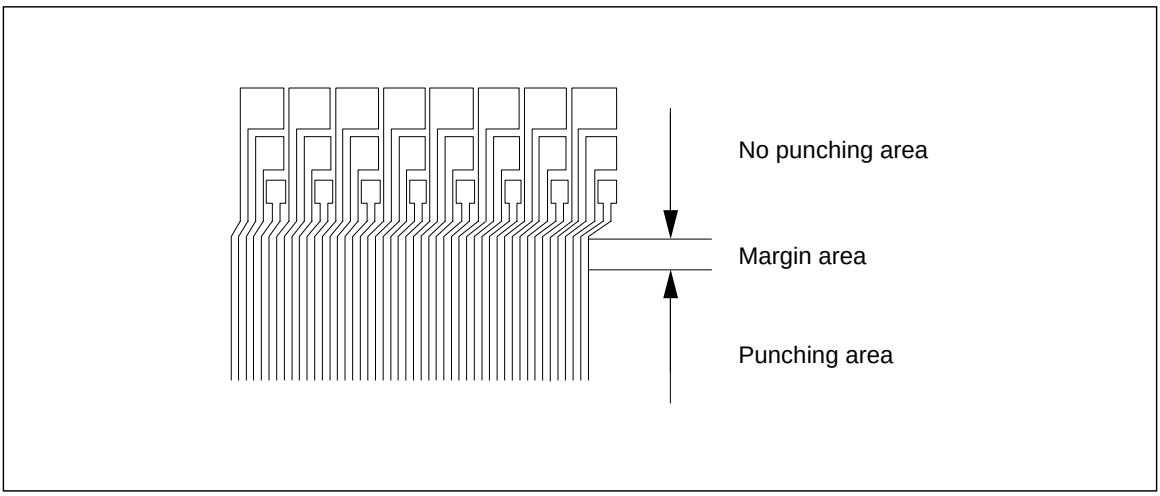


Figure 13 Punching Die

Figure 14 Punching Position

5. Mounting structure

   Copper foil can easily break even from a small physical stress because of its thinness needed to accommodate fine patterns. Large stresses should therefore not be applied to the copper foil when mounting TCP products on a board.

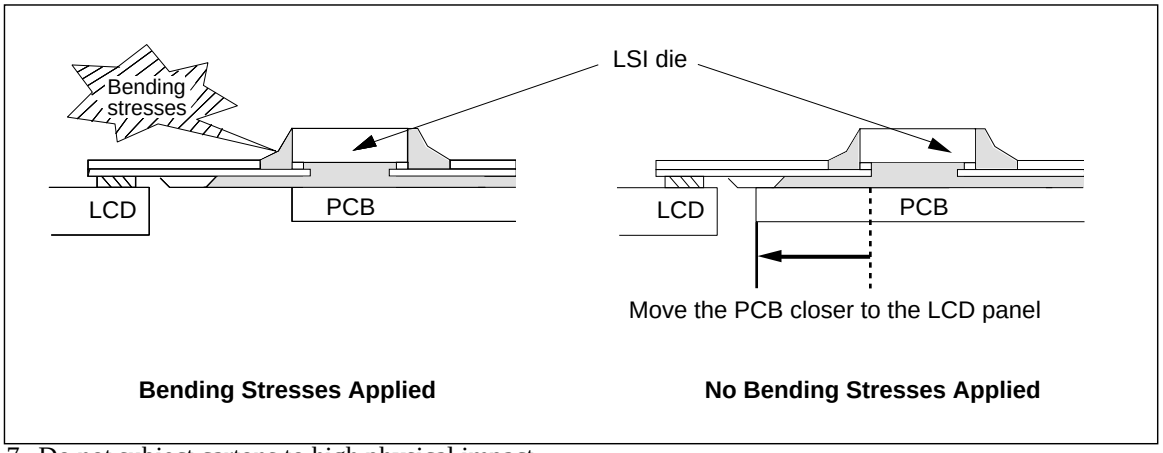
   • Bending stresses

     When the edges of a die and a PCB are aligned, resin cracks may occur due to bending stresses. To avoid this problem, locate the board closer to the LCD panel so that it can support the molded part of the package. (Refer to figure 15)

   • Thermal stresses

     LCM consists of glass, TCPs and a glass-epoxy substrate having their respective coefficients of thermal expansion (CTE). This difference in expansion effects may cause “thermal stresses” that especially concentrate in TCPs. The joining structure of LCMs is roughly shown in figure 16. Before beginning mass production, investigate and determine a joining structure that reduces thermal stresses so as to prevent contact and other defects from occurring.

6. Do not stack more than ten cartons of products.



7. Do not subject cartons to high physical impact.

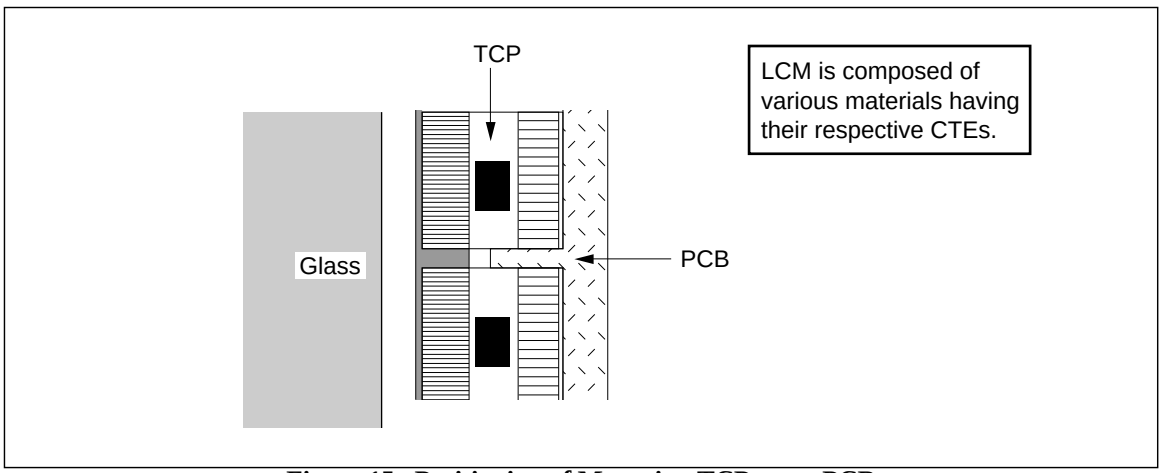


Figure 15 Positioning of Mounting TCPs on a PCB

Figure 16 Joining Structure of LCM

Correction of ITO (Indium Tin Oxide) Electrode Pitch: TCP products expand by absorbing moisture or heat during storage and assembly. Pitch correction for the ITO electrode should be performed based on the TCP dimensions after it is mounted on a conductive film. However, if ITO pitch correction is performed based on TCP dimensions before mounting, it must be based on data measured after removing TCP products from the package and storing at a temperature of 20 to 25°C and a humidity of 50 to 70% RH for 48 hours.

Correct the ITO electrode pitch depending on the bonding equipment and conditions used.

Miscellaneous

1. Do not heat the lead tape and separator; they have poor heat-resistivity and will expand.

2. Do not subject TCPs to high temperature for a long period of time while cleaning or other operations; copper foil may peel off due to the rapid deterioration of adhesion between the copper foil and base film.

3. Carrier tapes have some waviness that may cause problems in tape transport. Use a tapeguide or equivalent to secure the tape.

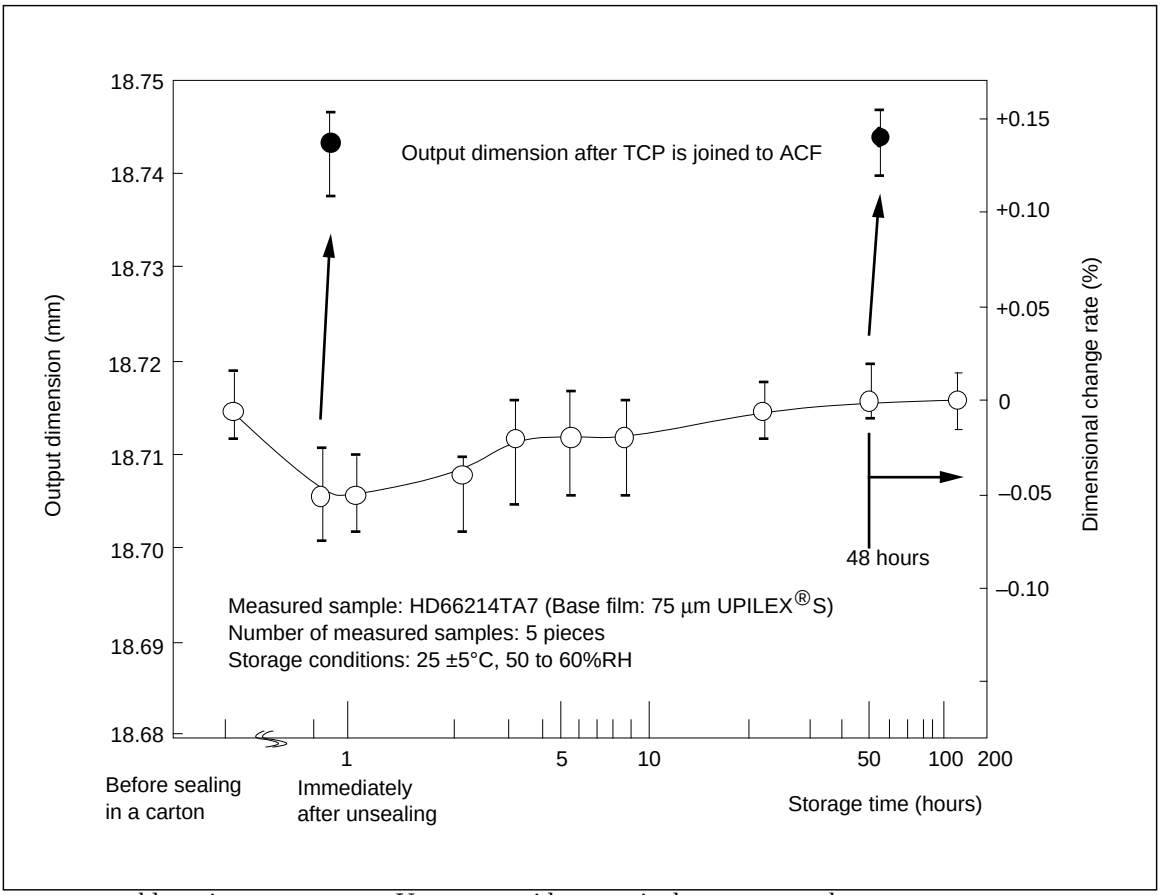
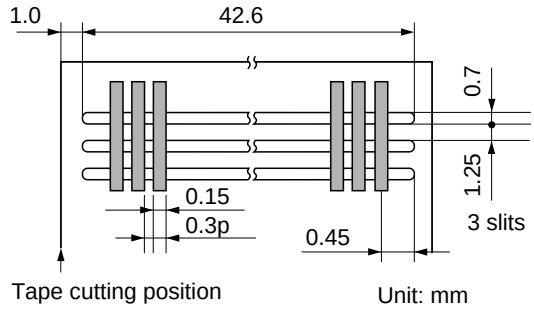
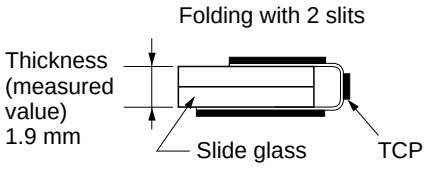


Figure 17 Dimensional Change of Output

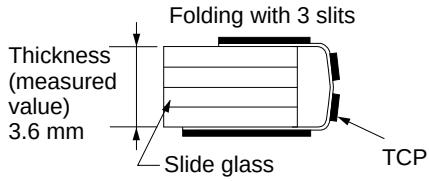
4. The number of folding TCP bending operations that can be performed before the lead breaks is shown in figure 18. The greater the bending angle, the sooner the lead will break. The TCP should be mounted in such a way that the bending angle of each slit does not exceed 90°.



Folding slit shape



Double-bend (90 degrees per slit)



Triple-bend (90 degrees or less per slit)

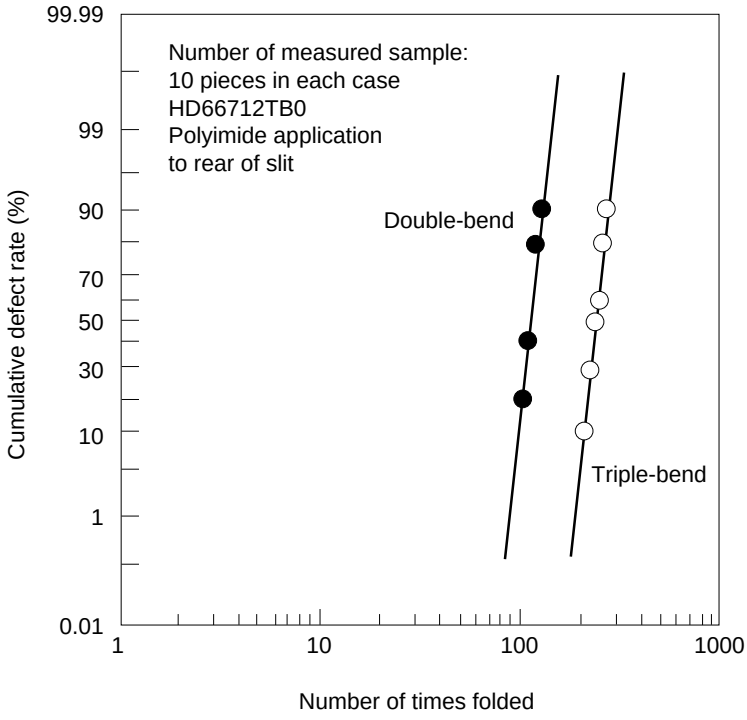


Figure 18 Example of Number of Times Folded vs Cumulative Defect Rate

TCP Standardization

At present, standardization of LCD drive TCPs is difficult because of differences in mounting methods and customer specifications. However, standardization of TCPs (QTP and DTP) that correspond in shape to TQFP and TSOP packages has been discussed by the Tape Carrier Package Working Group in the Semiconductor External Standards Committee (EE-13) of the EIAJ (Electronics Industries Association of Japan). This working group, which is composed of various semiconductor manufacturers including Hitachi, tape manufacturers, and socket manufacturers, is taking a comprehensive approach.

The EIAJ has adopted metric control standards against JEDEC*'s inch control standards, and has determined standards based on the following two items:

- Fixed test pad layout, variable package size
- Fixed test pad layout, variable terminal pitch

Accordingly, users can share the socket by deciding the width of tape and the test pad pitch. As JEDEC has already agreed to the metric-control TCP, Hitachi is now making efforts to produce metric-control TCPs.

General rules covering TCP outlines that have already been formulated and published by the EE-13 committee are shown below.

EIAJ ED-7431 Quad Tape Carrier Package (QTP)

EIAJ ED-7432 Dual Tape Carrier Package (Type I) (DTP(I))

EIAJ ED-7433 Dual Tape Carrier Package (Type II) (DTP(II))

A summary of these general rules is given below.

Note that these standards do not necessarily apply to LCD drive TCPS.

Note: * JEDEC:
Joint Electronic Device Engineering Council.

Quad Tape Carrier Package (QTP) EIAJ ED-7431

1. Tape width: 35, 48, 70 mm
2. Package size: 35 mm 14×14, 16×16, 18×18, 20×20
   48 mm 16×16, 20×20, 24×24, 26×26, 28×28
   70 mm 24×24, 28×28, 32×32, 36×36, 40×40
3. Test pad pitch: 0.5, 0.4, 0.3, 0.25 mm
4. Outer lead pitch: 0.5, 0.4, 0.3, 0.25, 0.2, 0.15 mm
5. Sprocket-hole type: 35 mm Super
   48 mm Wide, Super
   70 mm Wide, Super
6. Number of test pads: Fixed maximum number of test pads, regardless of the outer lead count.
   For 35-mm tape: 196 for 0.5 pitch; 244 for 0.4 pitch.

Dual Tape Carrier Package (Type I) (DTP(I)) EIAJ ED-7432

1. Tape width: 35 mm
2. Package size: 6×14, 6×16, 6×18, 6×20
   ($E \times (D + 1)$) 8×14, 8×16, 8×18, 8×20
   10×14, 10×16, 10×18, 10×20
   12×14, 12×16, 12×18, 12×20
3. Test pad pitch: 0.5 mm
4. Outer lead pitch: 0.5, 0.4, 0.3 mm
5. Sprocket-hole type: 35 mm Super
6. Number of test pads: N = 50 (E = 6, 8, 10)
   66 (E = 12)

Dual Tape Carrier Package (Type II) (DTP(II)) EIAJ ED-7433

1. Tape width: 35 mm
2. Package size: 300 mil, 350 mil, 400 mil, 450 mil, 500 mil, 550 mil,
   (E_{nom}) 600 mil
3. Test pad pitch: 1.27 mm (outer lead pitch: 1.27, 1.0)
   0.8 mm (outer lead pitch: 0.8, 0.65)
4. Outer lead pitch: 1.27, 1.0, 0.8, 0.65 mm
5. Sprocket-hole type: Super
6. Number of test pads: N = 42 (test pad pitch: 1.27 mm)
   70 (test pad pitch: 0.8 mm)

Reference Materials

TCP Mounting Equipment Manufacturer

Manufacturer: Hitachi Chemical Co., Ltd.

Area	Address	Tel No.	Fax No.
USA	Hitachi Chemical Co., America, Ltd. 4 International Drive, Rye Brook, NY 10573, U.S.A.	(914) 934-2424	(914) 934-8991
Europe	Hitachi Chemical Europe Gm bH. Immermmstr. 43, D-4000 Düsseldorf 1, F. R. Germany	(211) 35-0366 to 9	(211) 16-1634
S.E. Asia	Hitachi Chemical Asia-Pacific Pte, Ltd. 51 Bras Basah Road, #08-04 Plaza By The Park, Singapore 0718	337-2408	337-7132
Taiwan	Hitachi Chemical Taipei Office Room No. 1406, Chia Hsim Bldg., No. 96, Sec. 2, Chung Shang Road N, Taipei, Taiwan	(2) 581-3632, (2) 561-3810	(2) 521-7509
Beijing	Hitachi Chemical Beijing Office Room No. 1207, Beijing Fortune Building, 5 Dong, San Huan Bei-Lu, Chao Yang District, Beijing, China	(1) 501-4331 to 2	(1) 501-4333
Hong Kong	Hitachi Chemical Co., (Hong Kong) Ltd. Room 912, Houston Centre, 63 Mady Road, Tsimshatsui East, Kowloon, Hong Kong	(3) 66-9304 to 7	(3) 723-3549

Manufacturer: Matsushita Electric Industrial Co., Ltd.

Area	Address	Tel No.	Fax No.
USA (Illinois)	Panasonic Factory Automation Company	(708) 452-2500	
Deutschland	Panasonic Factory Automation Deutchland	(040) 8549-2628	
Asia (Japan)	Matsushita Manufacturing Equipment D.	(0552) 75-6222	

Manufacturer: Shinkawa Co., Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	MARUBENI INTERNATIONAL ELECTRONICS CORP. U.S.A. 3285 Scott Blvd, Santa Clara, CA. 95054	408-727-8447	408-727-8370
Singapore, Malaysia, Thailand	MARUBENI INTERNATIONAL ELECTRONICS CORP. SINGAPORE 18 Tannery Lane #06-01/02, Lian Teng Building, SGB 1334	741-2300	741-4870
Korea, Hong Kong, China, Taiwan, Philippine, Brazil	MARUBENI HYTECH CORP. Japan 20-22, Koishikawa 4-chome, Bunkyo-ku, Tokyo 112, Japan	(03)-3817-4952	(03)-3817-4959
Europe	MARUBENI INTERNATIONAL ELECTRONICS EUROPE GMBH Niederrhein STR, 42 4000 Düsseldorf 30 Federal Republic of Germany	0211-4376-00	0211-4332-85

TCP

Manufacturer: Kyushu Matsushita Electric Co., Ltd.

Area	Address	Tel No.	Fax No.
CHICAGO	1240 Landmeier Rd. Elk Grove Village, IL 60007	(708) 822-7262	(708) 952-8079
ATLANTA	1080 Holcomb Bridge Rd. Building 100, Suite 300 Roswell, Georgia 30076	(404) 906-1515	(404) 998-9830
SAN JOSE	177 Bovet Road, Suite 600 San Mateo, CA 99402	(415) 608-0317	(415) 341-1395
LONDON	238/246 King Street, London W6 ORF United Kingdom	(081) 748-2447	(081) 846-9580
SINGAPORE	1 Scotts Road, #21-10/13 Shaw Centre Singapore 0922	7387681	7325238
SEOUL	2ND Floor, Donghwa Bldg. 454-5, Dokok-1 Dong, Kangnam-Ku, Seoul, Korea	(02) 571-2911	(02) 571-2910
TAIWAN	6TH, FL., 360, FU HSING 1ST ROAD, KWEISHAN, TAOYUAN HSIEN, TAIWAN	(03) 328-7070	(03) 328-7080 (03) 328-7090
MALAYSIA	KUALALUMPUR BRANCH 8TH FLOOR, WISMA LEE RUBBER, JAPAN MELAKA, 50100 KUALALUMPUR	(03) 291-0066	(03) 291-8002
BANGKOK	20TH FL., Thaniya Plaza Bldg, 52 Silom Road, Bangrak, BANGKOK, 10500 THAILAND	(02) 231-2345	(02) 231-2342

Manufacturer: Japan Abionis Co., Ltd.

Area	Address	Tel No.	Fax No.
Worldwide	Overseas Department Contact: Mr. K. Asami, or Mr. K. Ito	81-3-3501-7358	81-3-3504-2829

TCP Tape Manufacturers

Manufacturer: Hitachi Cable Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	HITACHI CABLE AMERICA INC.	1-914-993-0991	001-1-914-993-0997
Europe	HITACHI CABLE INTERNATIONAL, LTD. (LONDON)	001-44-71-439-7223	001-44-71-494-1956
Sigapore	HITACHI CABLE INTERNATIONAL, LTD (SINGAPORE)	001-65-2681146	001-65-2680461
Hong Kong	HITACHI CABLE INTERNATIONAL, LTD (HONG KONG)	001-852-721-2077	001-852-369-3472

Manufacturer: Mitsui Mining and Smelting Co., Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	MITSUI MINING AND SMELTING CO., (USA) INC.	212-679-9300 to 2	212-679-9303
Europe	MITSUI MINING AND SMELTING CO., LTD. London Office	71-405-7717 to 8	71-405-0227
Asia	MITSUI MINING AND SMELTING CO., LTD. MICROCIRCUIT DIVISION	03-3246-8079	03-3246-8063

Manufacturer: Shindo Company Ltd.

Area	Address	Tel No.	Fax No.
U.S.A.	SHINDO COMPANY LTD., U.S. BRANCH OFFICE 2635 NORTH FIRST ST., STE. 124 SAN JOSE, CA 95134 U.S.A.	408-435-0808	408-435-0809

Aeolotropy Conductive Film Manufacturers

Manufacturer: Hitachi Chemical Co., Ltd.

Area	Address	Tel No.	Fax No.
USA	Hitachi Chemical Co., America, Ltd. 4 International Drive, Rye Brook, NY 10573, U.S.A.	(914) 934-2424	(914) 934-8991
Europe	Hitachi Chemical Europe GmbH. Immermannstr. 43, D-4000 Düsseldorf 1, F. R. Germany	(211) 35-0366 to 9	(211) 16-1634
S.E. Asia	Hitachi Chemical Asia-Pacific Pte, Ltd. 51 Bras Basah Road, #08-04 Plaza By The Park, Singapore 0718	337-2408	337-7132
Taiwan	Hitachi Chemical Taipei Office Room No. 1406, Chia Hsin Bldg., No. 96, Sec. 2, Chung Shang Road N, Taipei, Taiwan	(2) 581-3632, (2) 561-3810	(2) 521-7509
Beijing	Hitachi Chemical Beijing Office Room No. 1207, Beijing Fortune Building, 5 Dong, San Huan Bei-Lu, Chao Yang District, Beijing, China	(1) 501-4331 to 2	(1) 501-4333
Hong Kong	Hitachi Chemical Co., (Hong Kong) Ltd. Room 912, Houston Centre, 63 Mady Road, Tsimshatsui East, Kowloon, Hong Kong	(3) 66-9304 to 7	(3) 723-3549

Manufacturer: Sony Chemicals

Area	Address	Tel No.	Fax No.
U.S.A.	SONY CHEMICALS CORPORATION OF AMERICA	1-(708) 616-0070	1-(708) 616-0073
Europe	SONY CHEMICALS EUROPE B.V.	31-20-658-1850	31-20-659-8481
Southeast Asia	SONY CHEMICALS SINGAPORE PTE LTD.	65-382-1500	65-382-1750

References

1. KAPTON® V Catalog — Du Pont-Toray Co., Ltd.
2. UPILEX® S Catalog — Ube Industries, Ltd.
3. Electro-deposited Foil Comparison List — Mitsui Mining Smelting Co., Ltd. Electronic Devices Group
4. Hitachi Anisotropic Discharge Film — Hitachi Chemical Co., Ltd.

1992.7.21

Hitach Standard TCP Product Structure

Hitachi can provide the standard TCP products listed in table 7 immediately. Figures 18 to 44 show the structure of each TCP product.

Table 7 Hitachi Standard TCP Product Specifications

No.	Product	Function	No. of Outputs	Output Lead Pitch (µm)	Output Lead Length (mm)	Input Lead Pitch (µm)	Input Lead Length (mm)	Input Lead Arrange*1	User Pattern Area Width X (mm)	User Pattern Area Width Y (mm)	Solder Resist Width (mm)	Product Length*2	Tape Material*3	Plating
1	HD66107T00	LCD driver	160	280	2.5	800	2.0	A	50.20	20.25	46.80	12	K	Sn
2	HD66107T01	LCD driver	80	280	2.5	800	2.0	A	32.00	20.25	28.00	12	K	Sn
3	HD66107T11	LCD driver	160	180	3.3	800	2.5	A	32.42	20.00	31.60	8	K	Sn
4	HD66107T12	LCD driver	160	250	3.3	800	2.5	A	43.50	20.00	42.40	10	K	Sn
5	HD66107T24	LCD driver	160	180	3.3	800	2.5	A	32.52	20.00	31.60	8	U	Sn
6	HD66107T25	LCD driver	80	280	2.5	800	2.0	A	32.00	20.25	28.00	8	K	Sn
7	HD66108T00	LCD driver	165	400	2.0	400	2.0	B	—	—	—	8	K	Sn
8	HD66108TA0	Common/column	165	280	5.34	800	2.7	A	51.0	23.3	48.34	12	U	Sn
9	HD66108TB0	Common/column	165	250	4.5	650	2.0	A	46.0	23.6	44.0	11	U	Sn
10	HD66110STB2	Column	160	92	2.4	500	1.2	A	15.60	9.00	15.10	3	U	Sn
11	HD66110STB3	Column	160	92	1.95	500	1.2	A	15.81	11.0	16.38	4	U	Sn
12	HD66110STB4	Column	160	80	2.14	450	1.0	A	16.6	7.3	15.2	3	U	Sn
13	HD66113TA0	Common	120	190	3.3	800	1.5	A	24.5	10.5	23.5	3	U	Sn
14	HD66115TA0	Common LCD driver	160	180	3.0	800	2.0	A	32.40	11.00	31	3	U	Sn
15	HD66115TA3	Common	160	250	2.6	800	1.5	A	44.0	11.6	42.9	3	U	Sn
16	HD66120TA0	Column	240	70	2.54	500	1.2	A	18.68	9.44	18.68	4	U	Sn
17	HD66120TA2	Column	240	74	3.15	500	1.2	A	18.8	10.5	18.8	4	U	Sn
18	HD66120TA3	Column	240	70	2.1	600	1.0	A	20.08	7.3	18.9	4	U	Sn
19	HD66300T00	TFT analog driver	120	300	2.9	800	3.0	A	46.00	21.50	46.20	10	K	Sn
20	HD66310T00	TFT 8 level gray scale	160	180	3.0	650	2.5	A	33.40	21.00	31.95	8	K	Sn
21	HD66330TA0	TFT 64 level gray scale	192	160	3.5	650	1.5	A	35.30	11.70	33.60	4	U	Sn
22	HD66503TA0	Common	240	200	3.0	800	2.5	A	52.0	15.4	49.7	4	U	Sn
23	HD66503TB0	Common	240	200	3.0	800	2.5	A	56.2	19.55	54.8	5	U	Sn
24	HD66520TA0	Column	160	200	3.0	700	2.5	A	36.0	17.8	33.7	5	U	Sn
25	HD66520TB0	Column	160	200	3.0	700	2.5	A	38.2	21.3	36.7	5	U	Sn
26	HD66712TA0	Common/column	94	300	3.3	650	2.5	A	24.80	17.40	23.80	4	U	Sn
27	HD66712TB0	Common/column	94	300	4.5	1000	2.5	A	46.2	23.65	43.2	10	U	Sn

Notes: 1. Input lead arrange: A = Straight, B = Directions
2. Number of perforations
3. Tape material: K = Kapton, U = Upilex
"Kapton" is a trademark of Dupont, Ltd.
"Upilex" is a trademark of Ube Industries, Ltd.

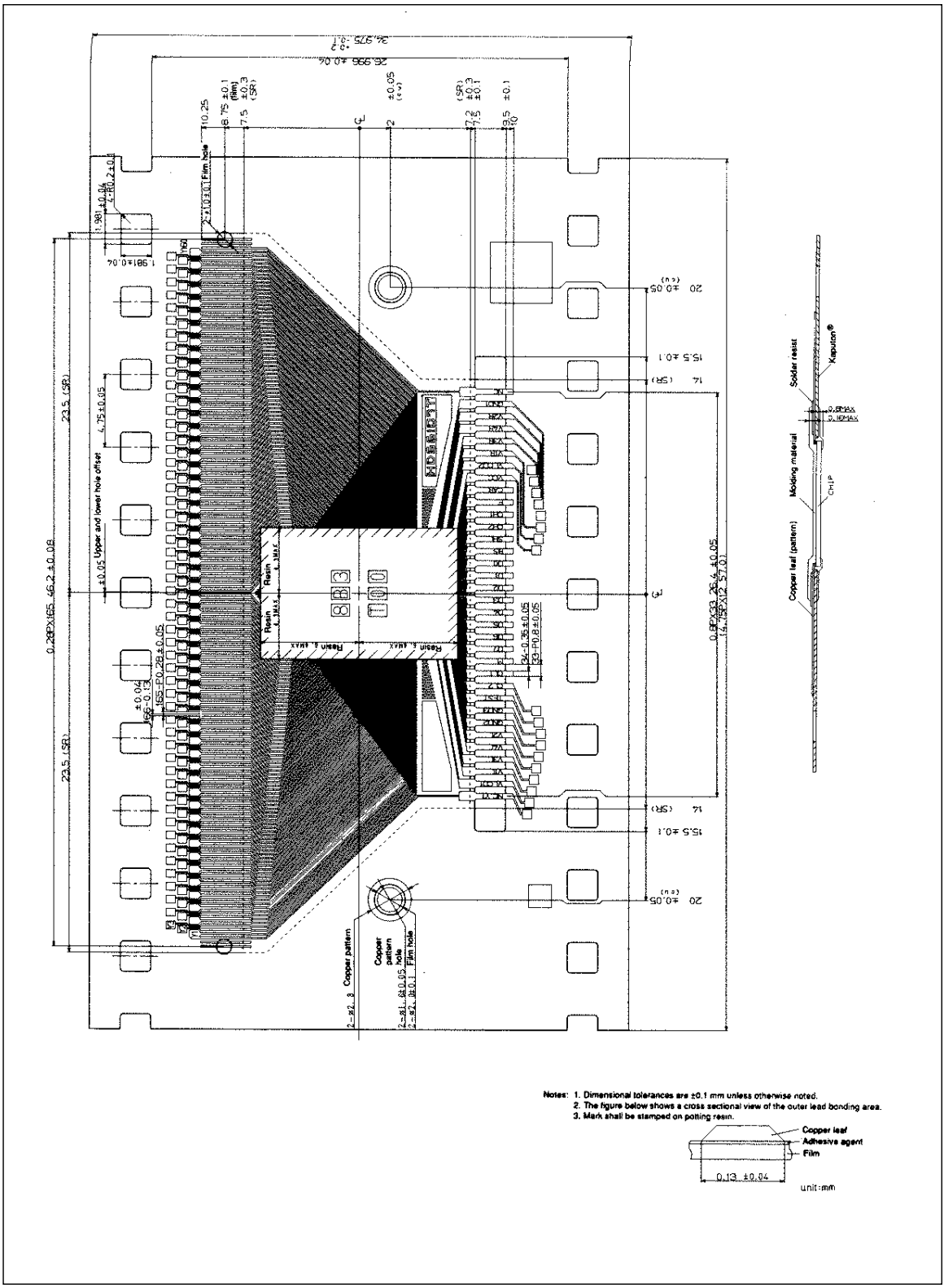


Figure 18 Hitachi Standard TCP 1 — HD66107T00 —

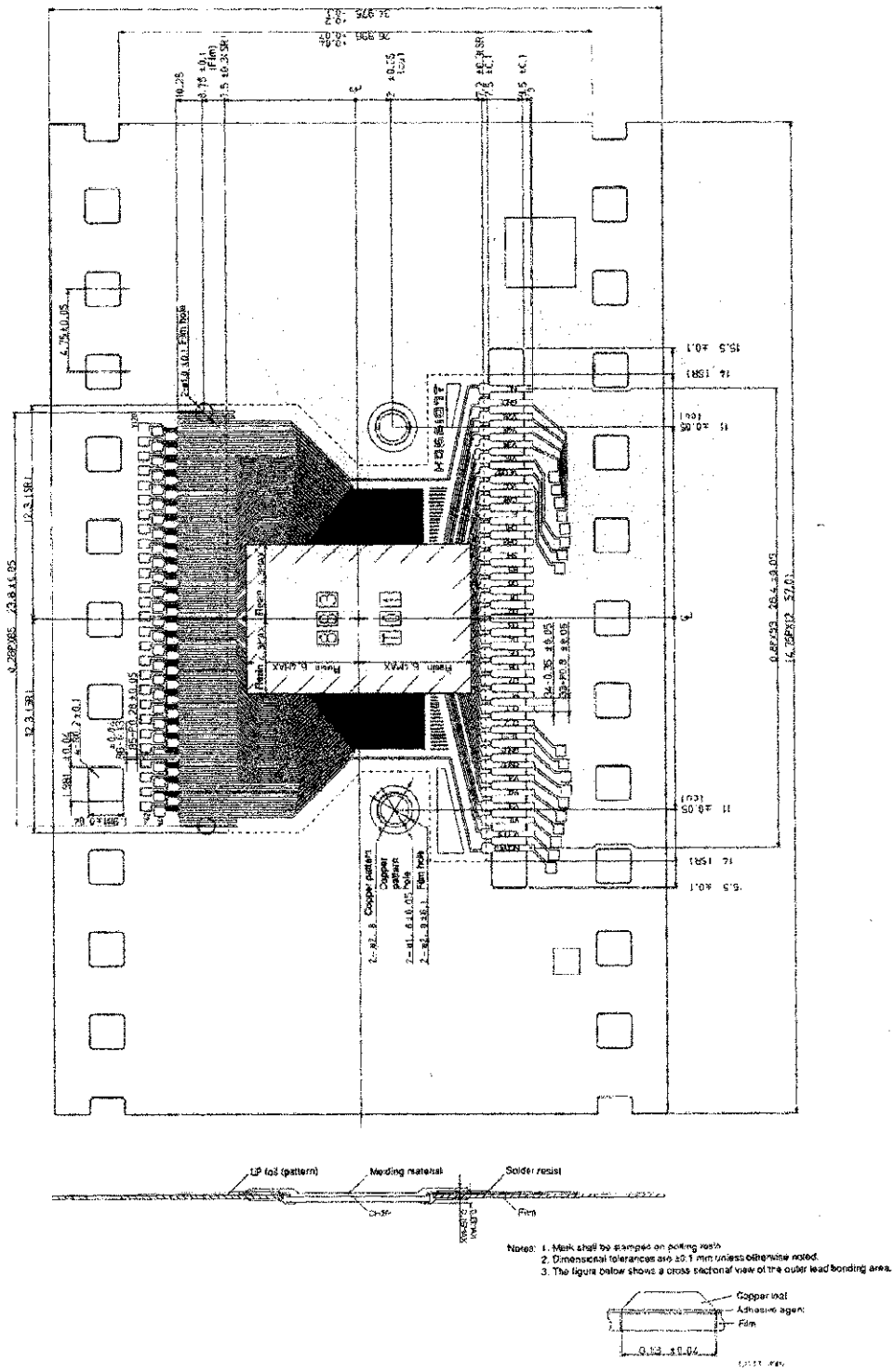


Figure 19 Hitachi Standard TCP 2 — HD66107T01 —

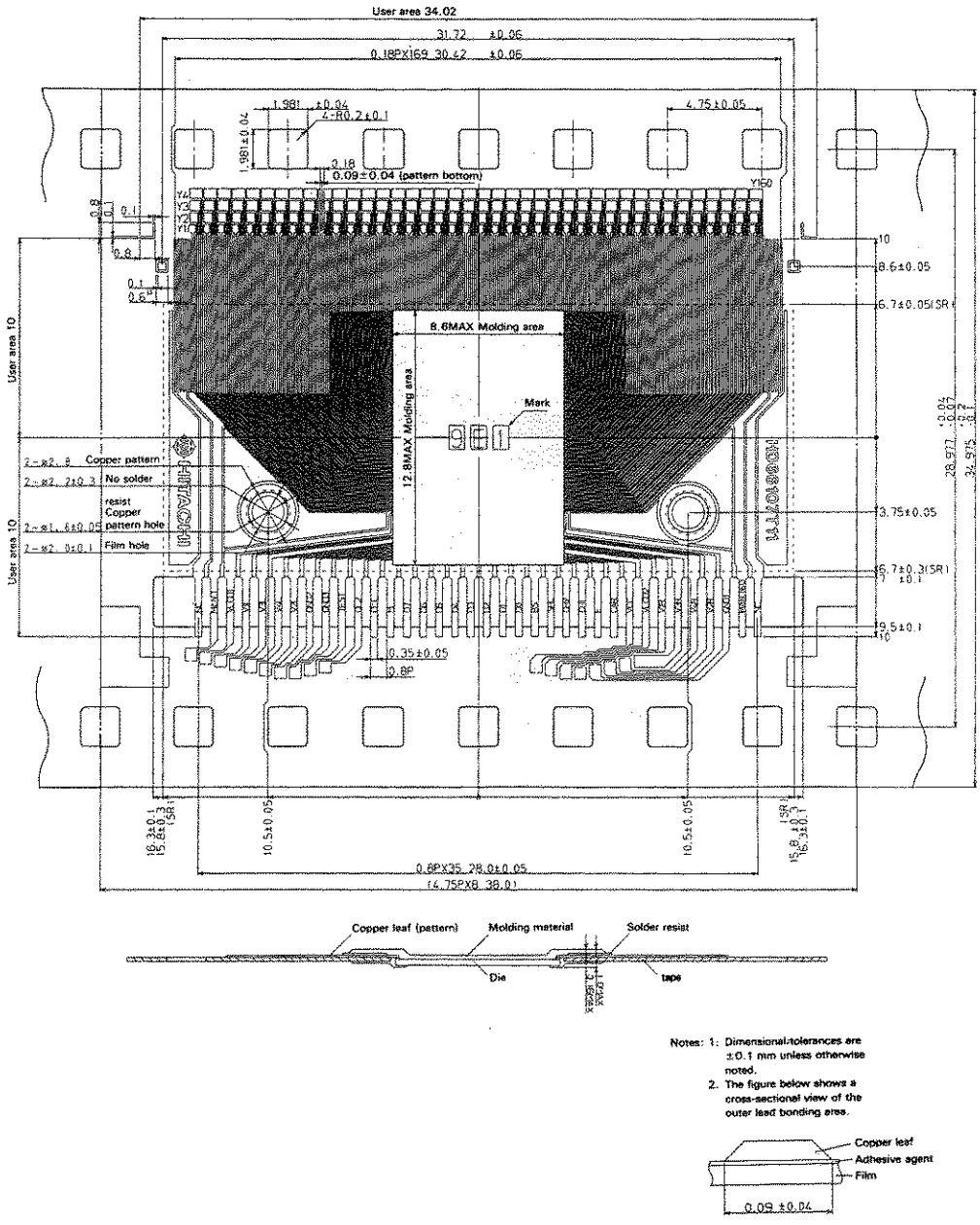


Figure 20 Hitachi Standard TCP 3 — HD66107T11 —

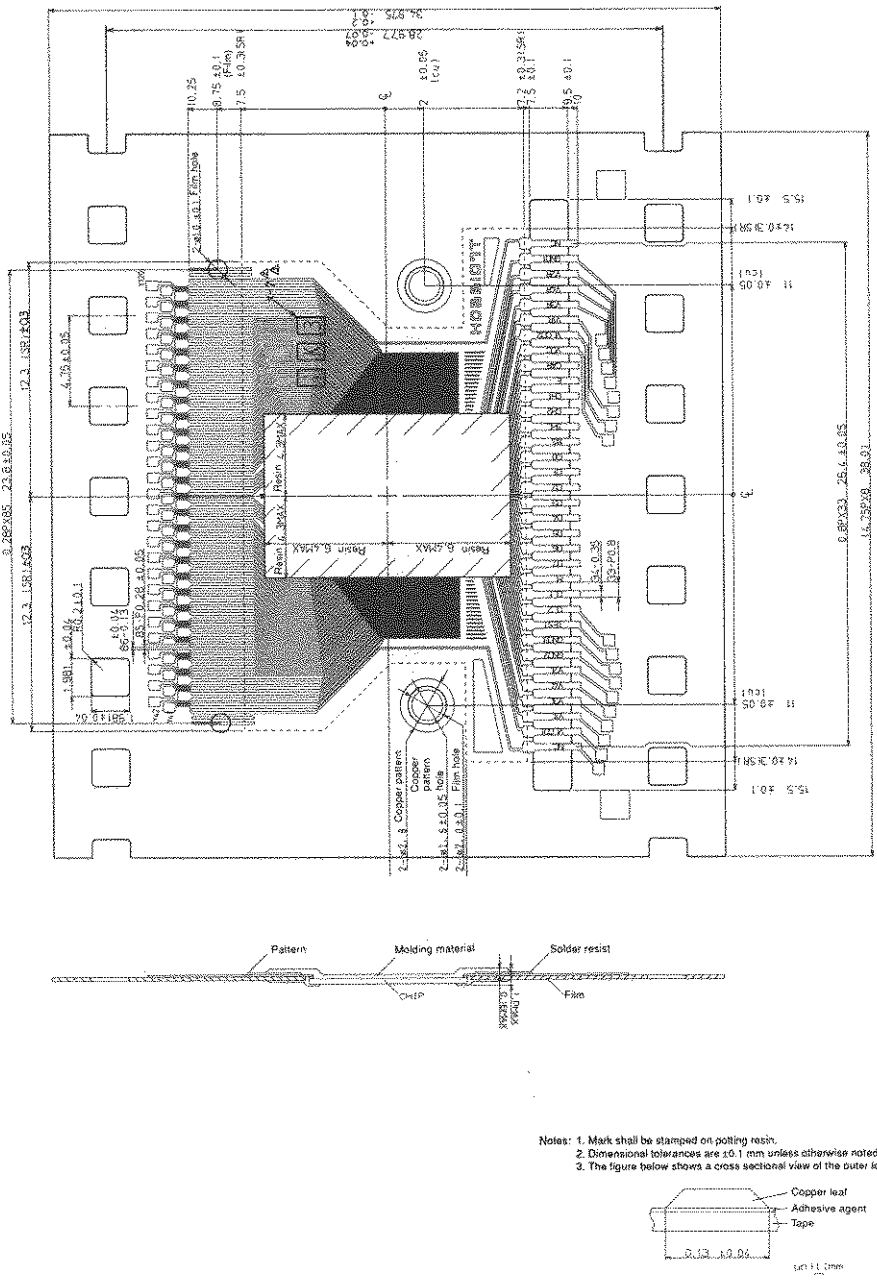
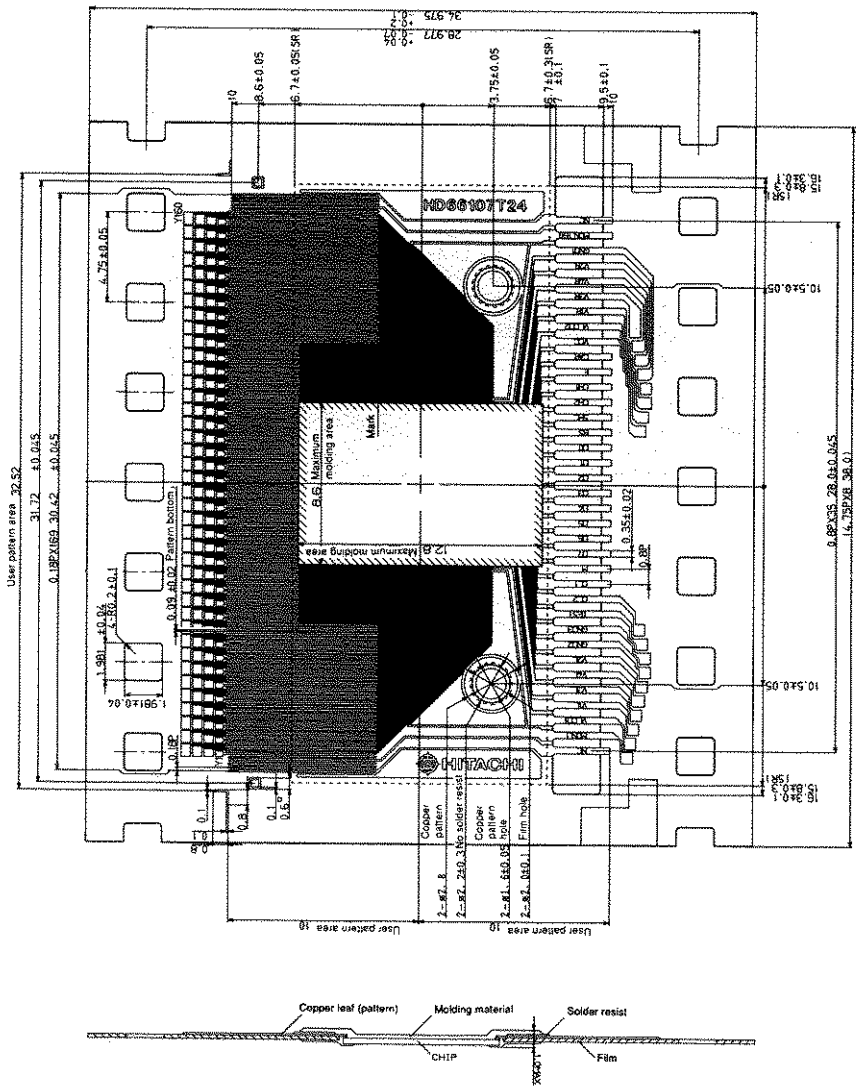


Figure 21 Hitachi Standard TCP 4 — HD66107T12 —



Notes: 1. Dimensional tolerances are ±0.1 mm unless otherwise noted.
2. The figure below shows a cross sectional view of the outer lead bonding area.

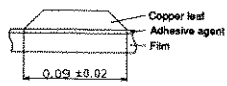


Figure 22 Hitachi Standard TCP 5 — HD66107T24 —

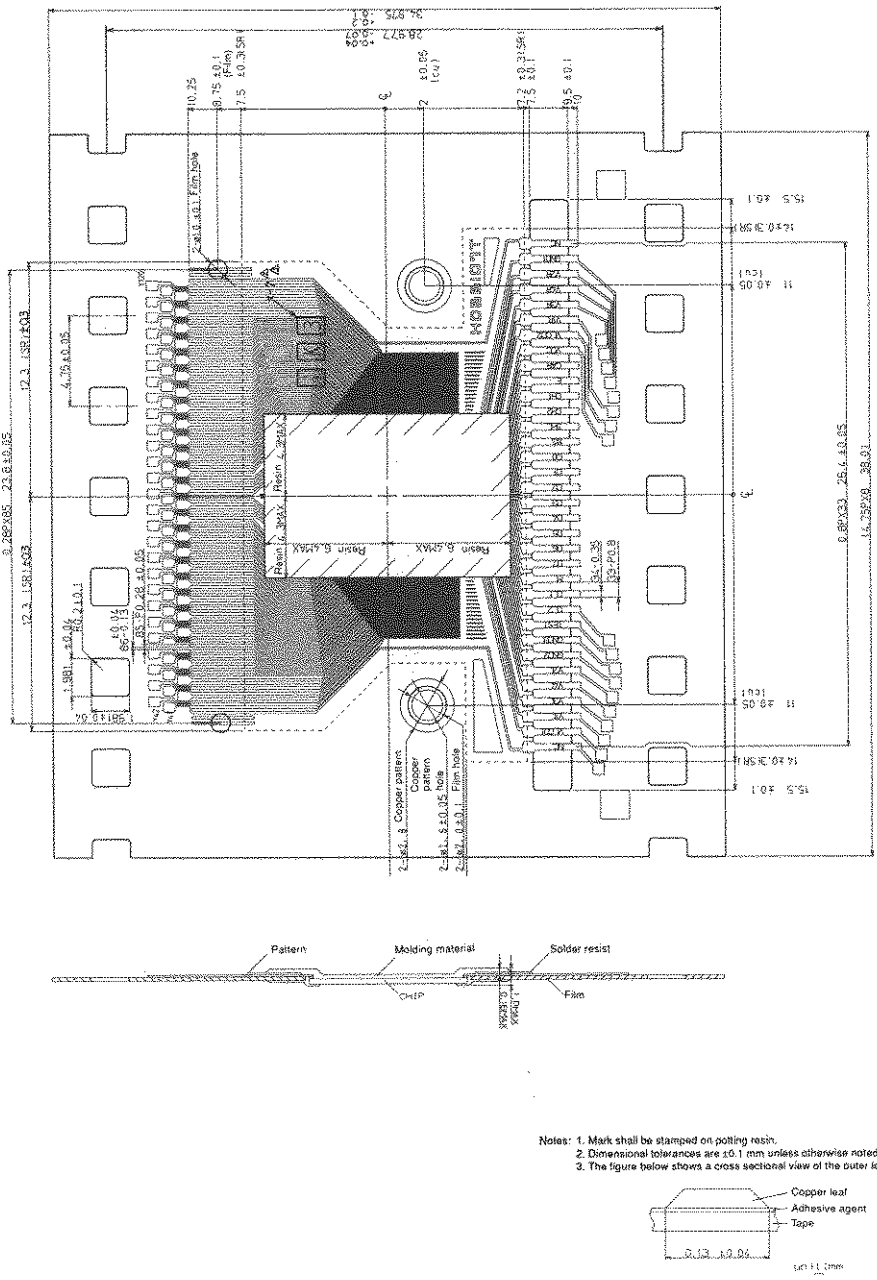
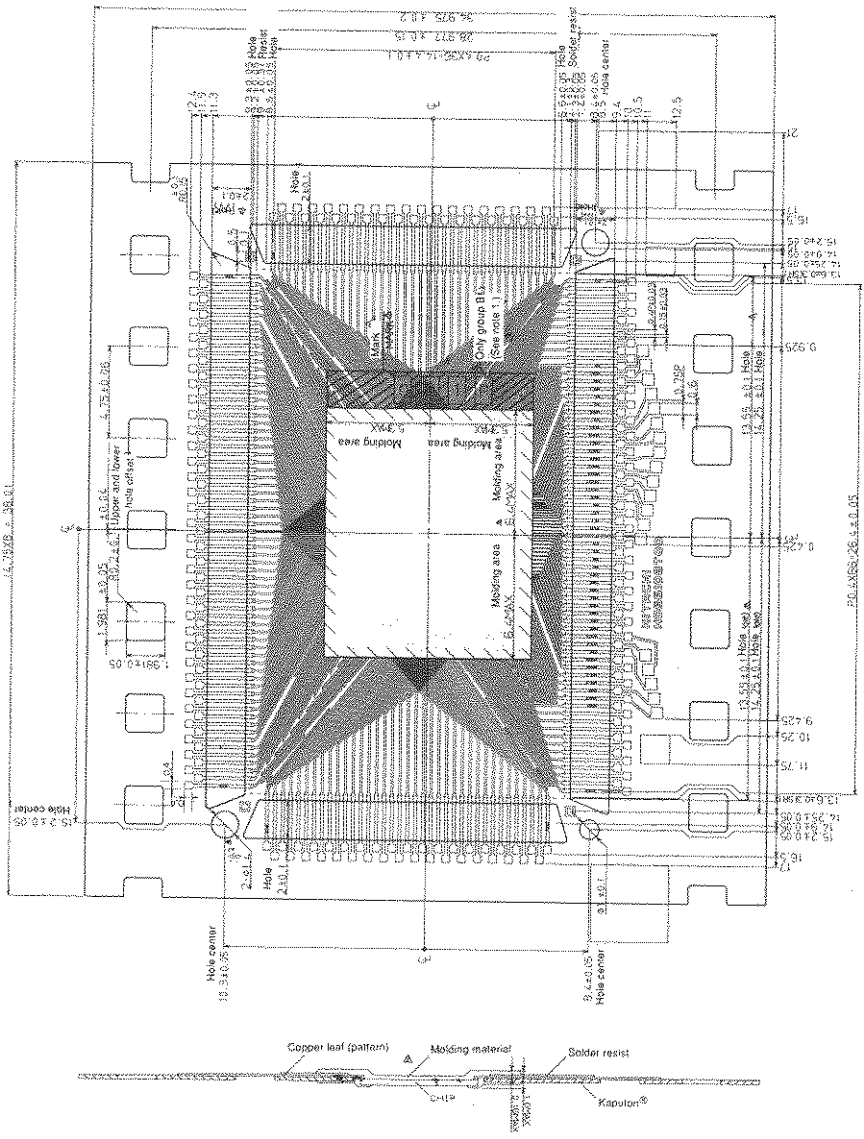


Figure 23 Hitachi Standard TCP 6 — HD66107T25 —



Note 1: Mark specifications

Group	Code
A	Only the year, month, and week code
B	The year, month, week code, and "P"

- Intersection dimensions are to be read from the figure unless otherwise noted.
- Dimensional tolerances are ±0.1 mm unless otherwise noted.
- Tolerance for deviation between pattern and hole centers is ±0.05 mm.
- A mark is stamped on the shaded area, which is to the right of the molded area within the solder resist.

Figure 24 Hitachi Standard TCP 7 — HD66108T00 —

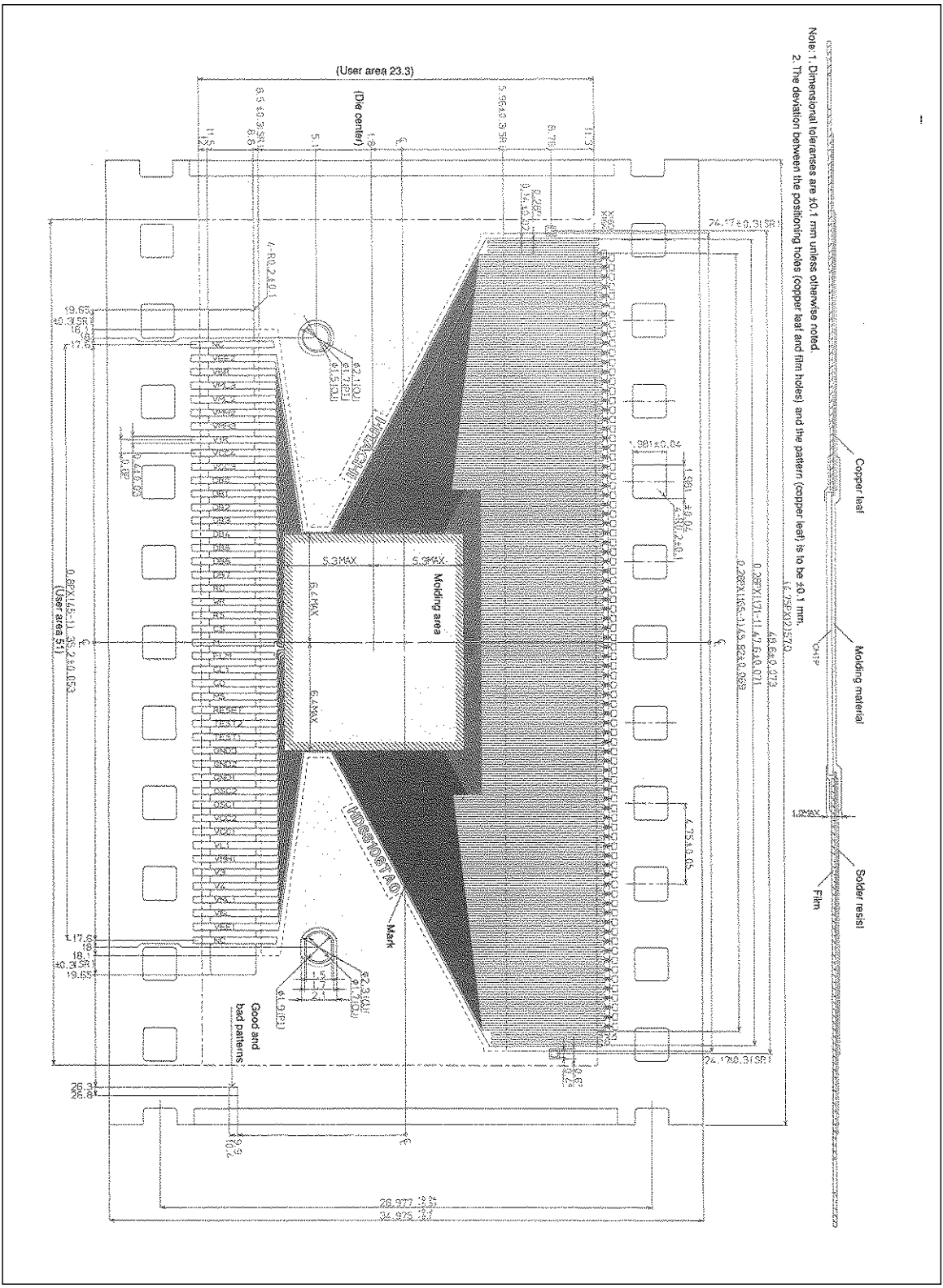


Figure 25 Hitachi Standard TCP 8 — HD66108TA0 —

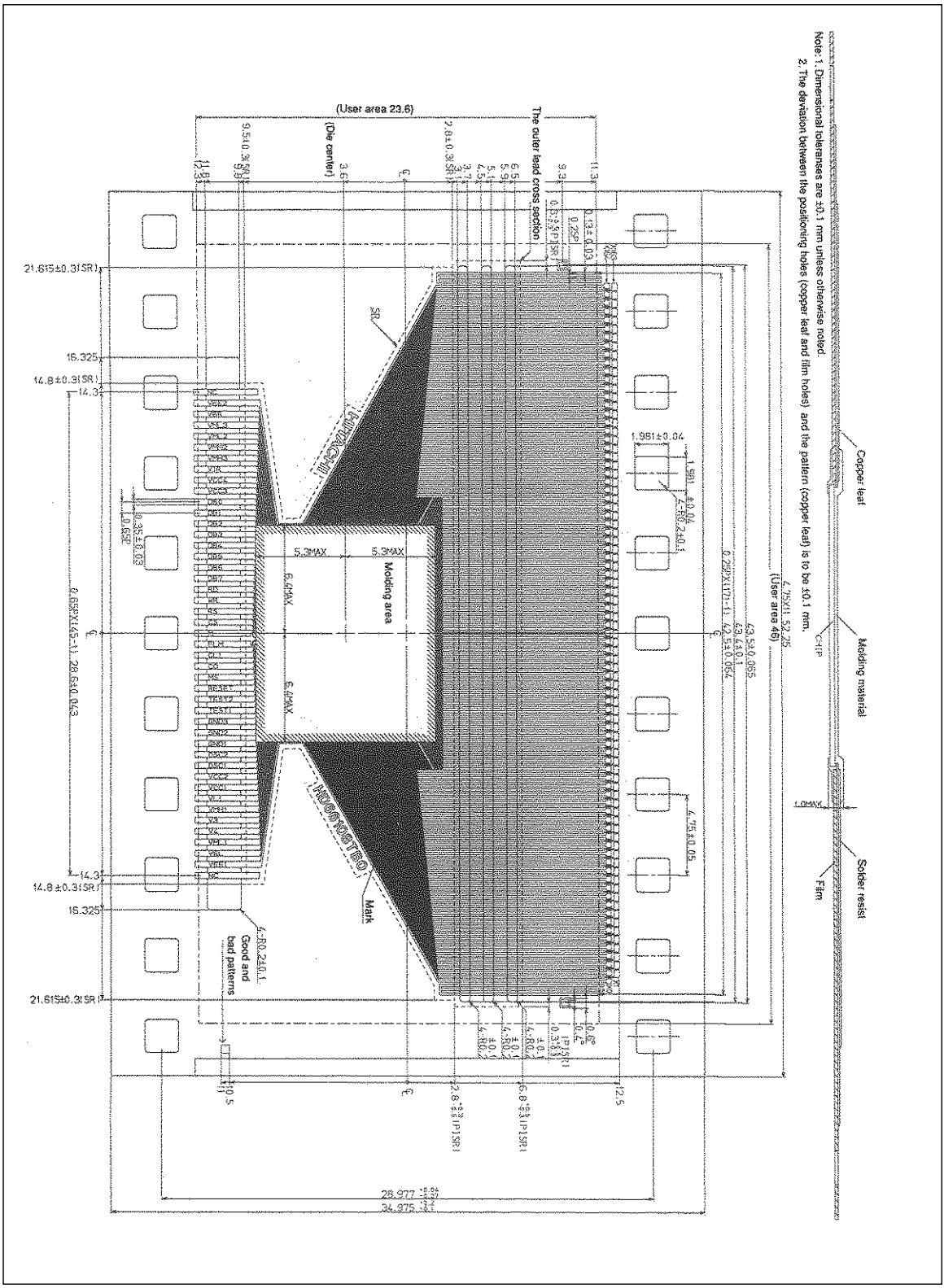
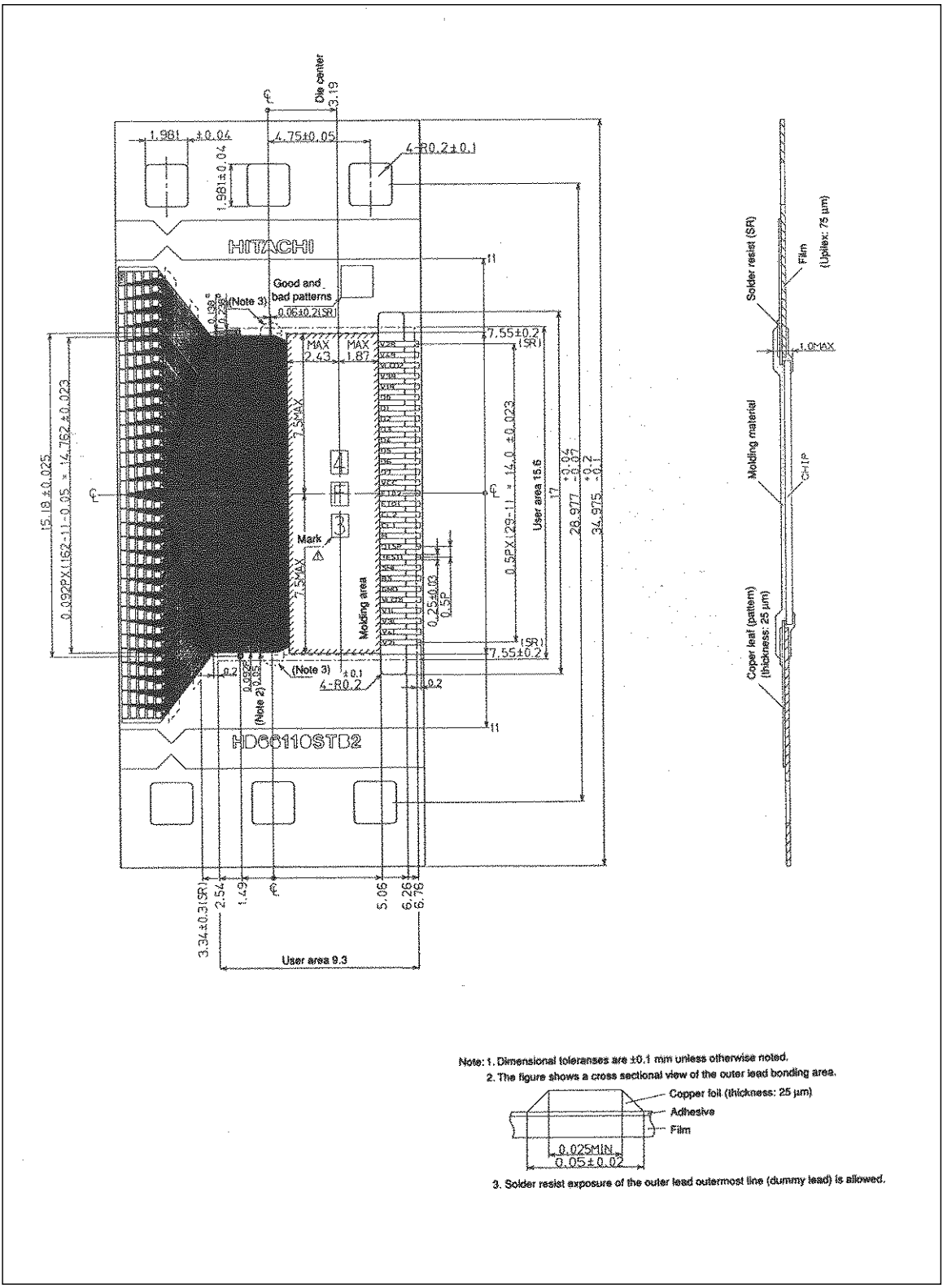


Figure 26 Hitachi Standard TCP 9 — HD66108TB0 —



Note: 1. Dimensional toleranses are ±0.1 mm unless otherwise noted.

2. The figure shows a cross sectional view of the outer lead bonding area.

3. Solder resist exposure of the outer lead outermost line (dummy lead) is allowed.

Figure 27 Hitachi Standard TCP 10 — HD66110STB2 —

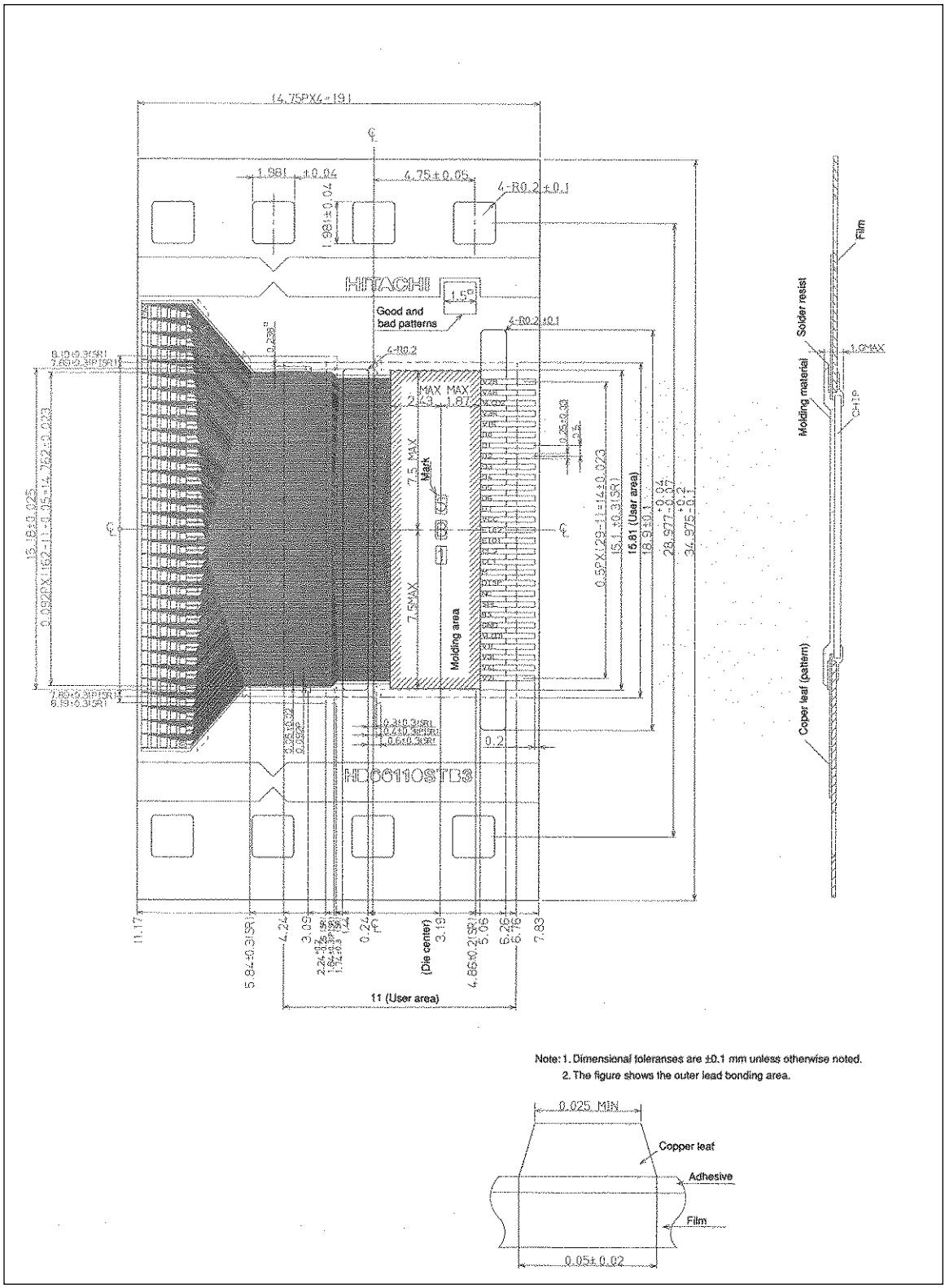


Figure 28 Hitachi Standard TCP 11 — HD66110STB3 —

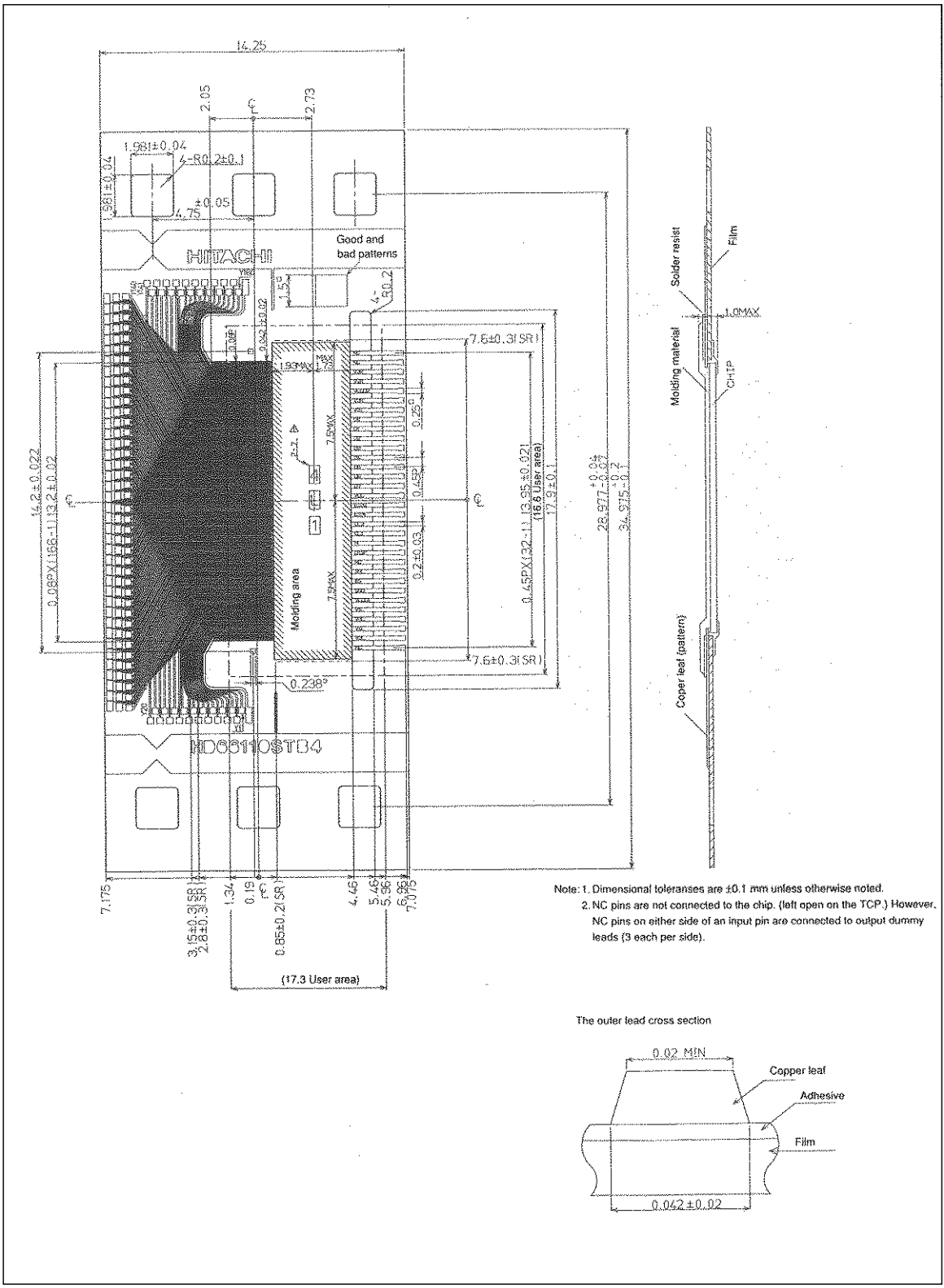
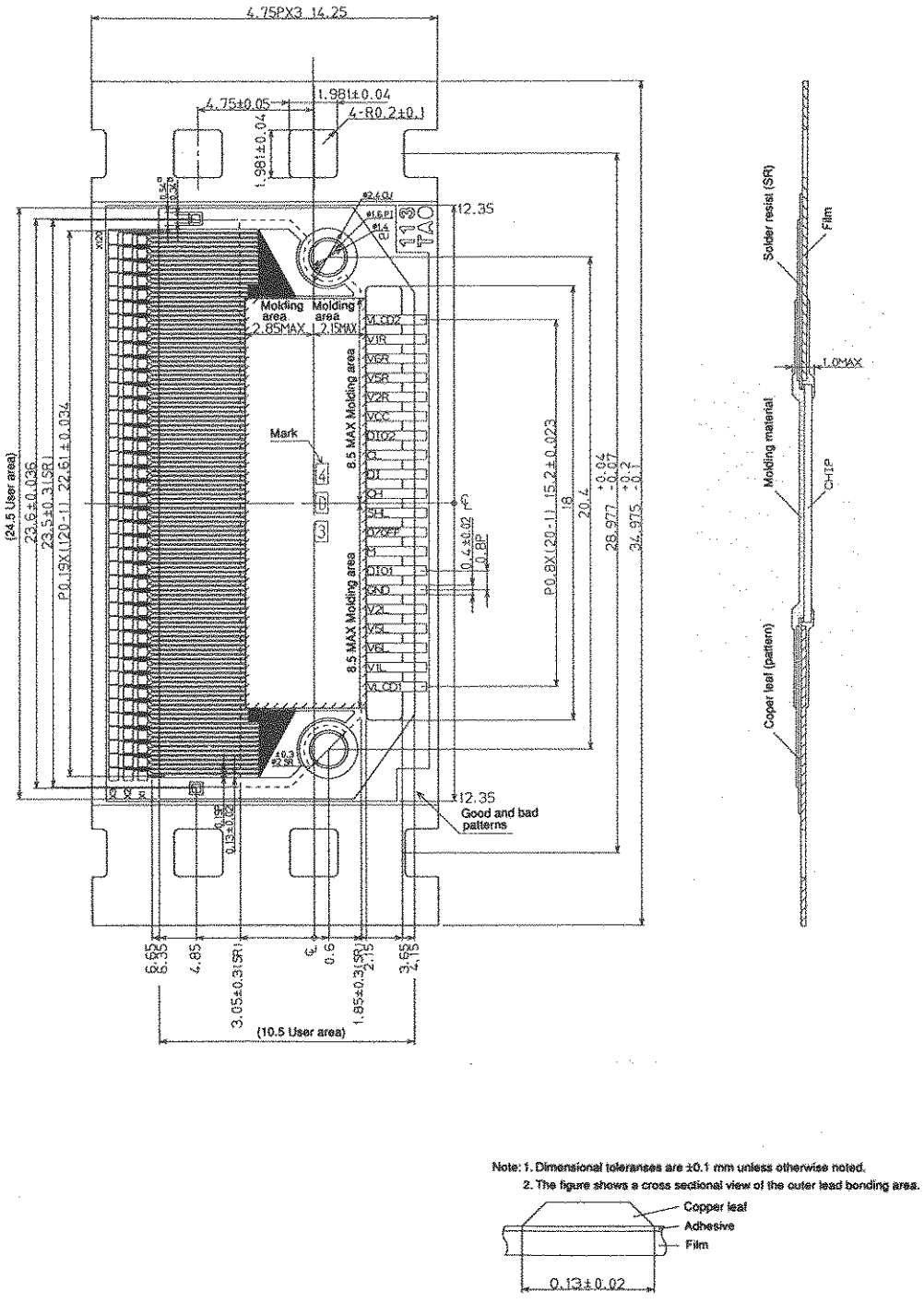


Figure 29 Hitachi Standard TCP 12 — HD66110STB4 —



Note: 1. Dimensional toleranses are ±0.1 mm unless otherwise noted.
2. The figure shows a cross sectional view of the outer lead bonding area.

Figure 30 Hitachi Standard TCP 13 — HD66113TA0 —

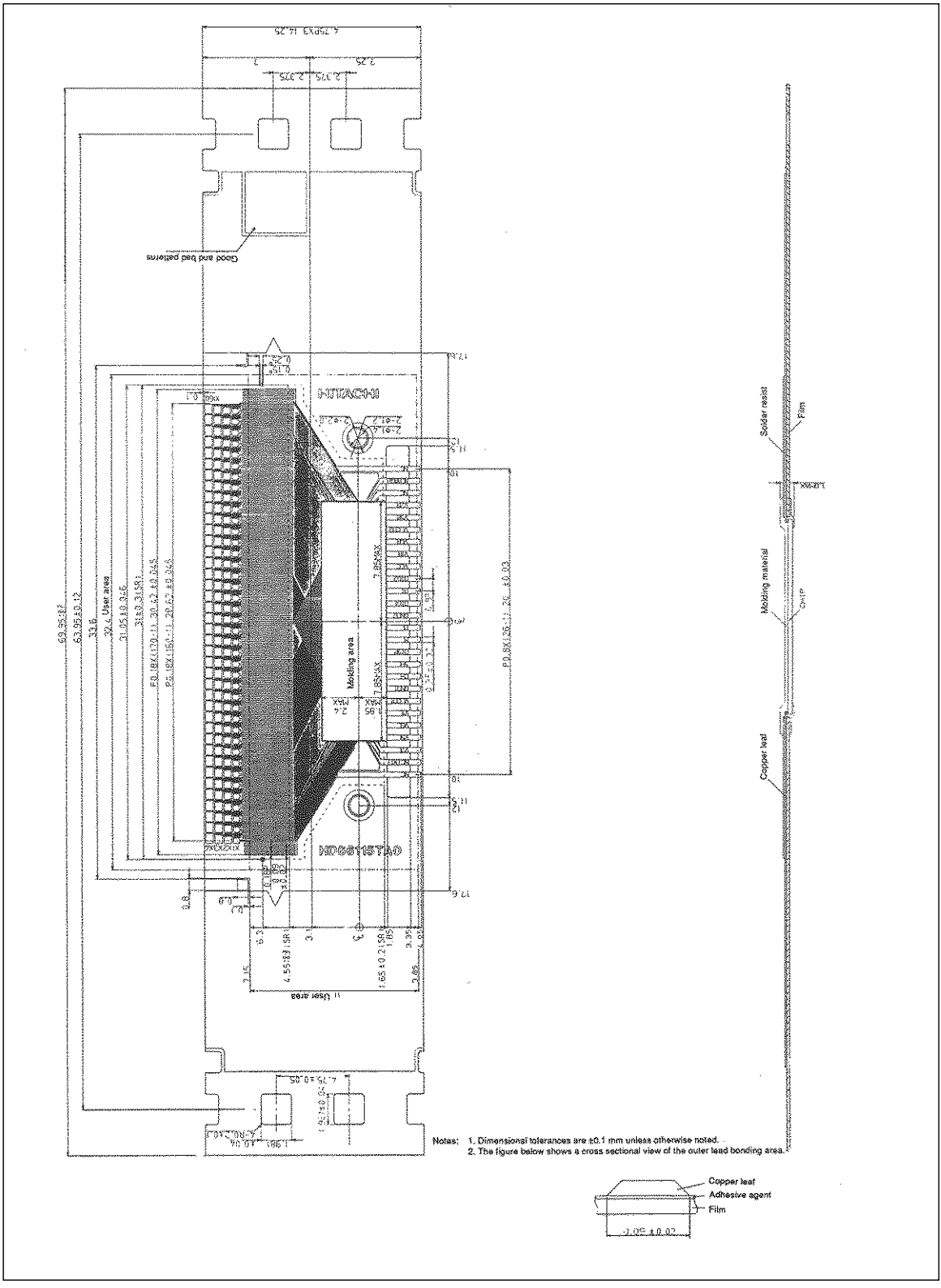


Figure 31 Hitachi Standard TCP 14 — HD66115TA0 —

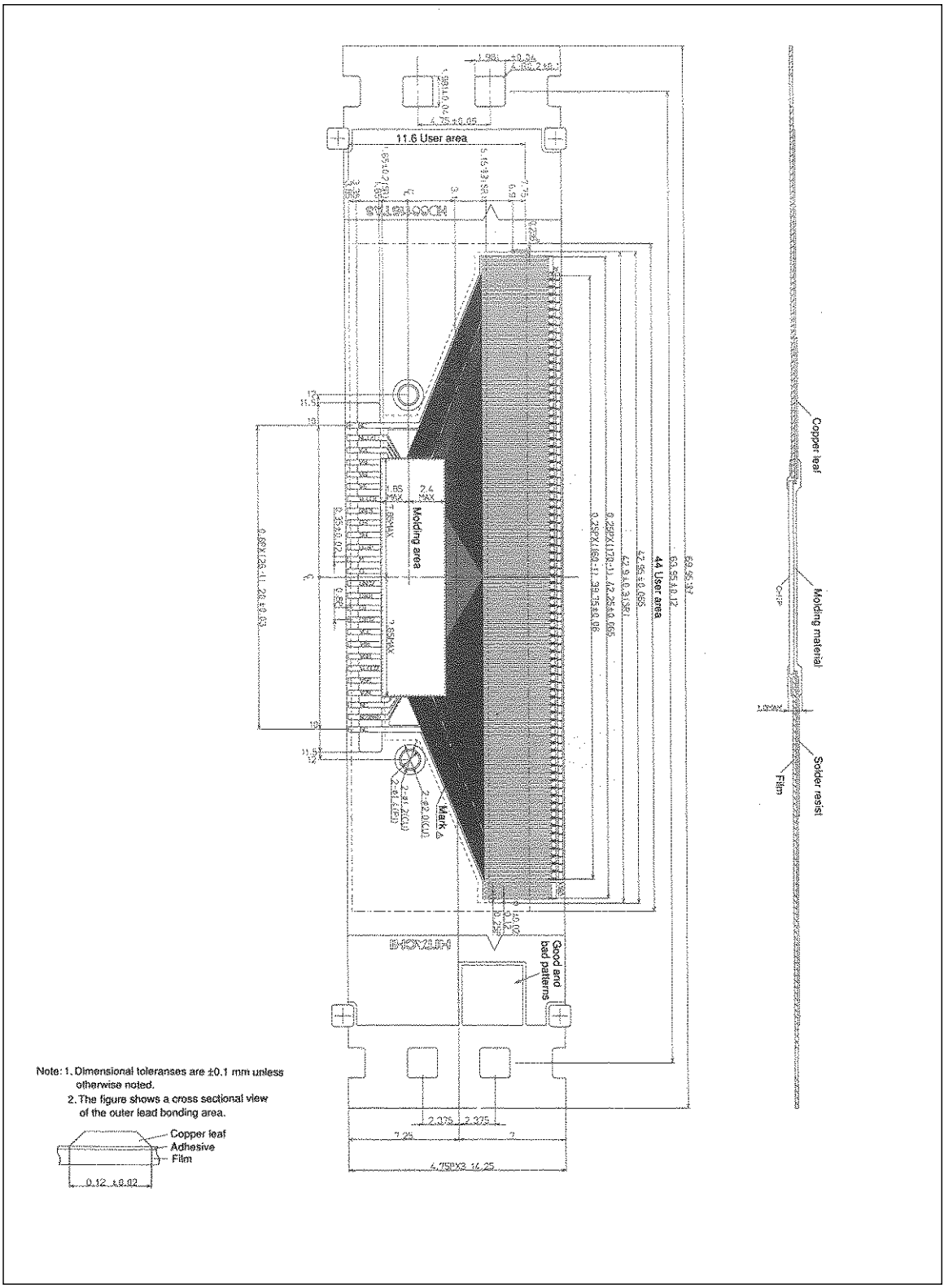


Figure 32 Hitachi Standard TCP 15 — HD66115TA3 —

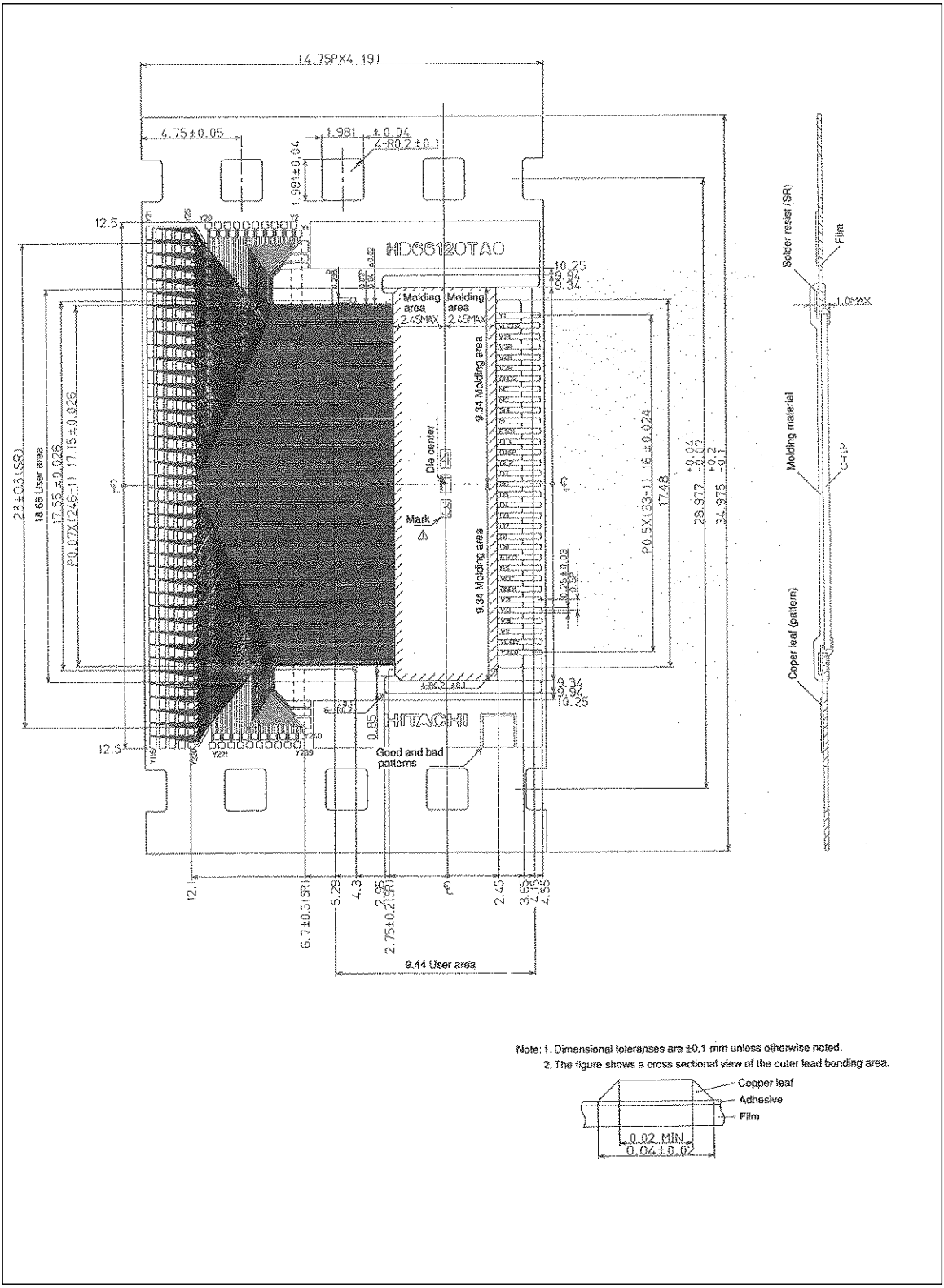


Figure 33 Hitachi Standard TCP 16 — HD66120TA0 —

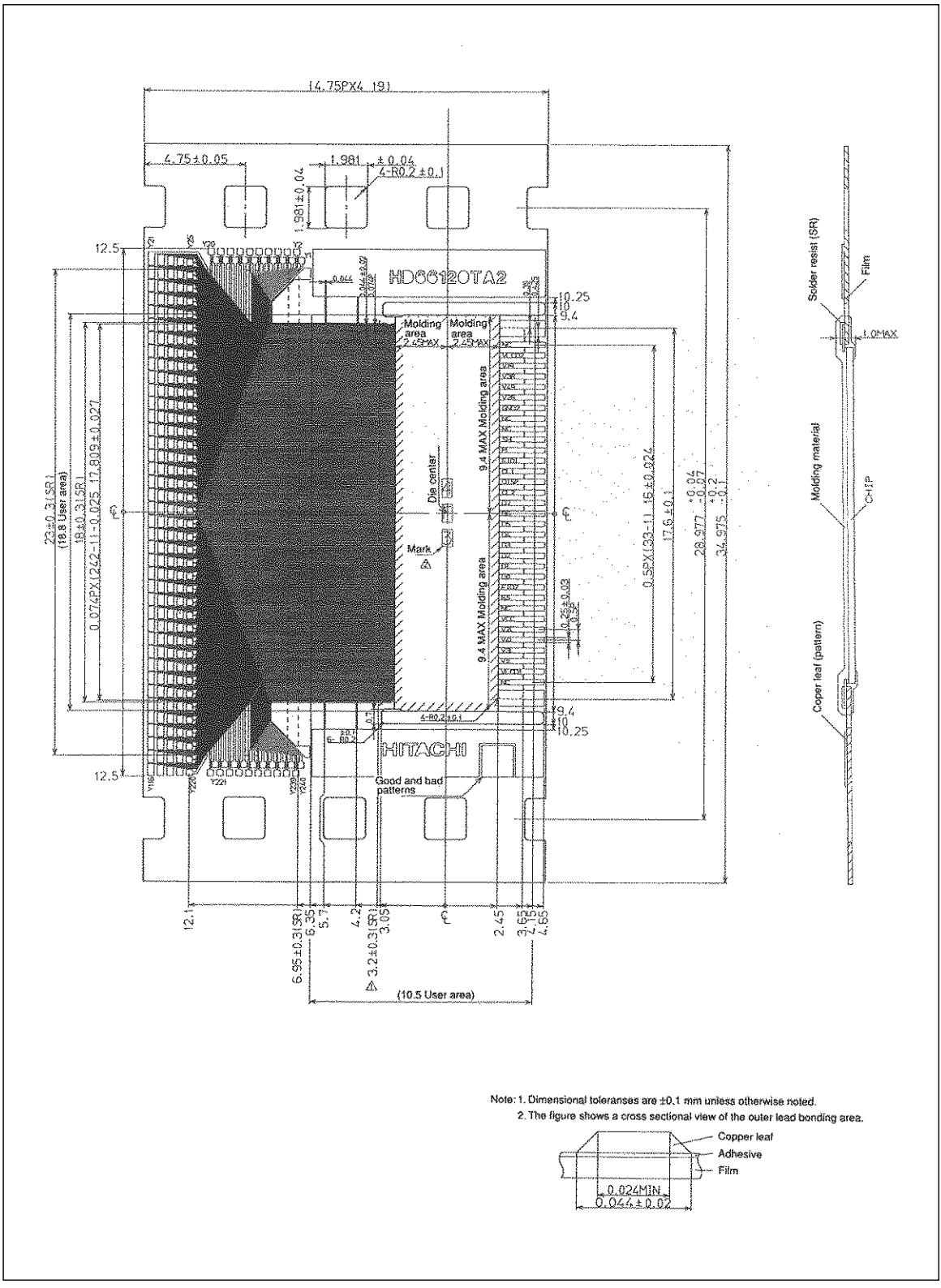
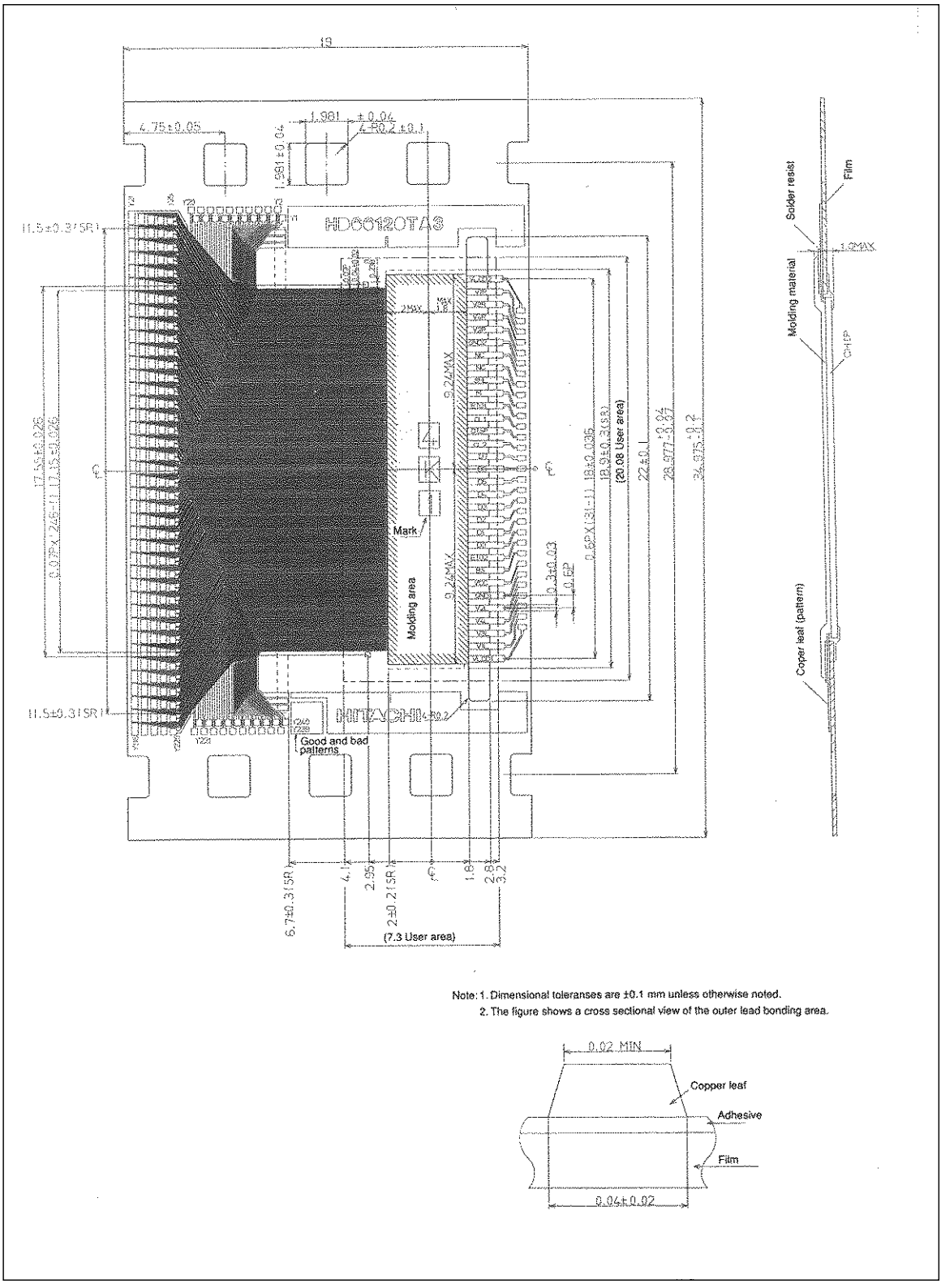


Figure 34 Hitachi Standard TCP 17 — HD66120TA2 —



Note: 1. Dimensional toleranses are ±0.1 mm unless otherwise noted.
2. The figure shows a cross sectional view of the outer lead bonding area.

Figure 35 Hitachi Standard TCP 18 — HD66120TA3 —

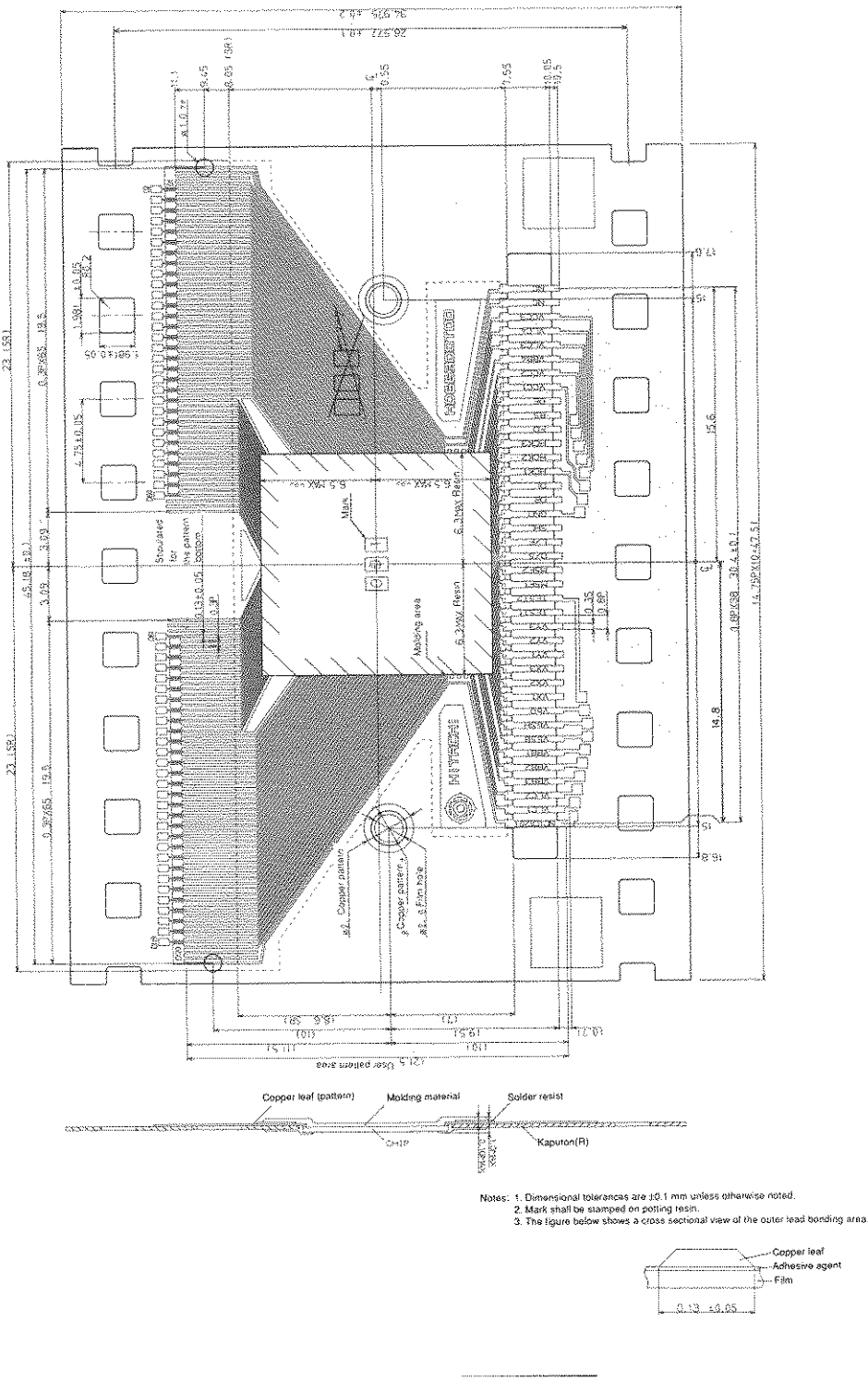


Figure 36 Hitachi Standard TCP 19 — HD66300T00 —

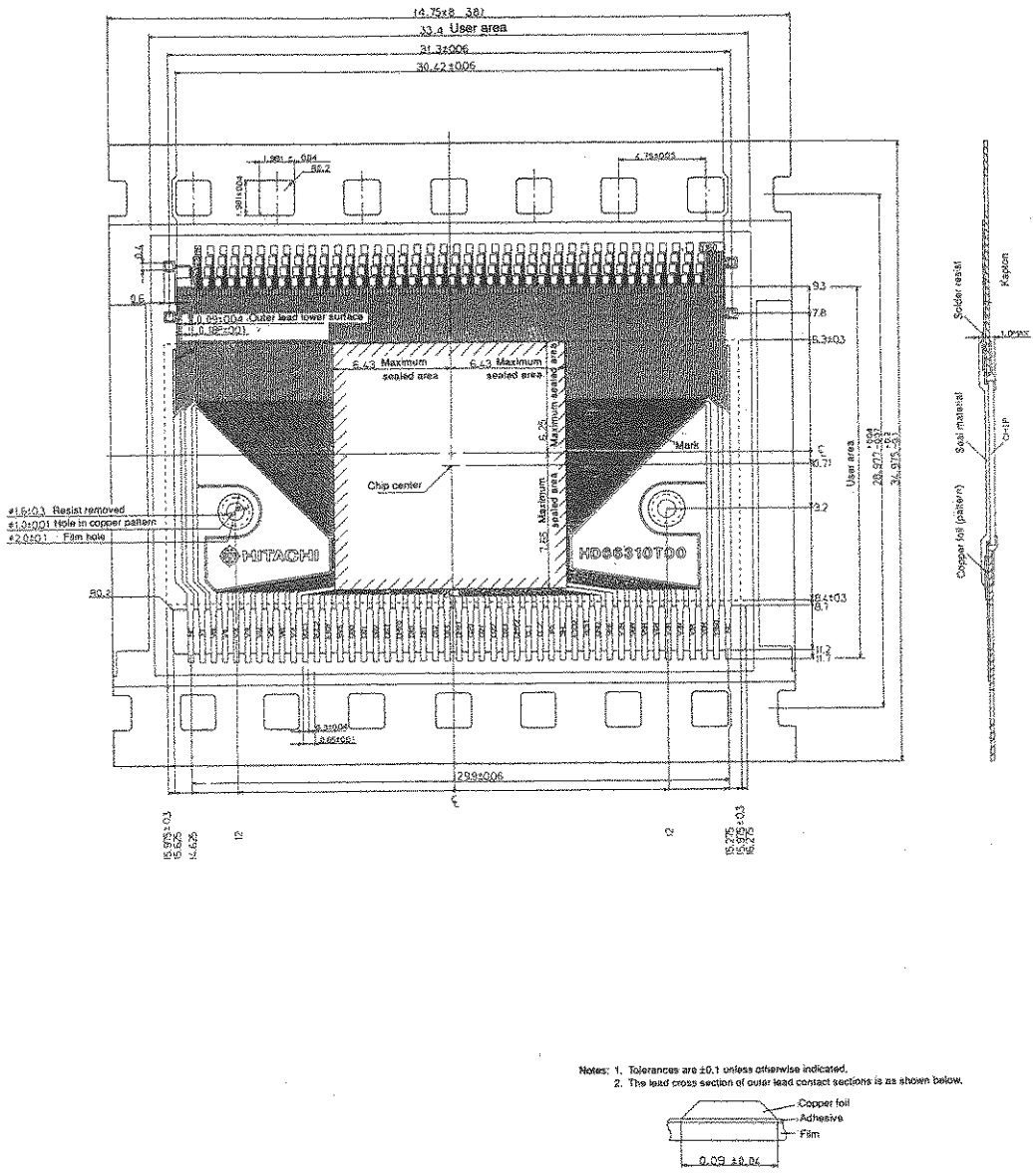


Figure 37 Hitachi Standard TCP 20 — HD66310T00 —

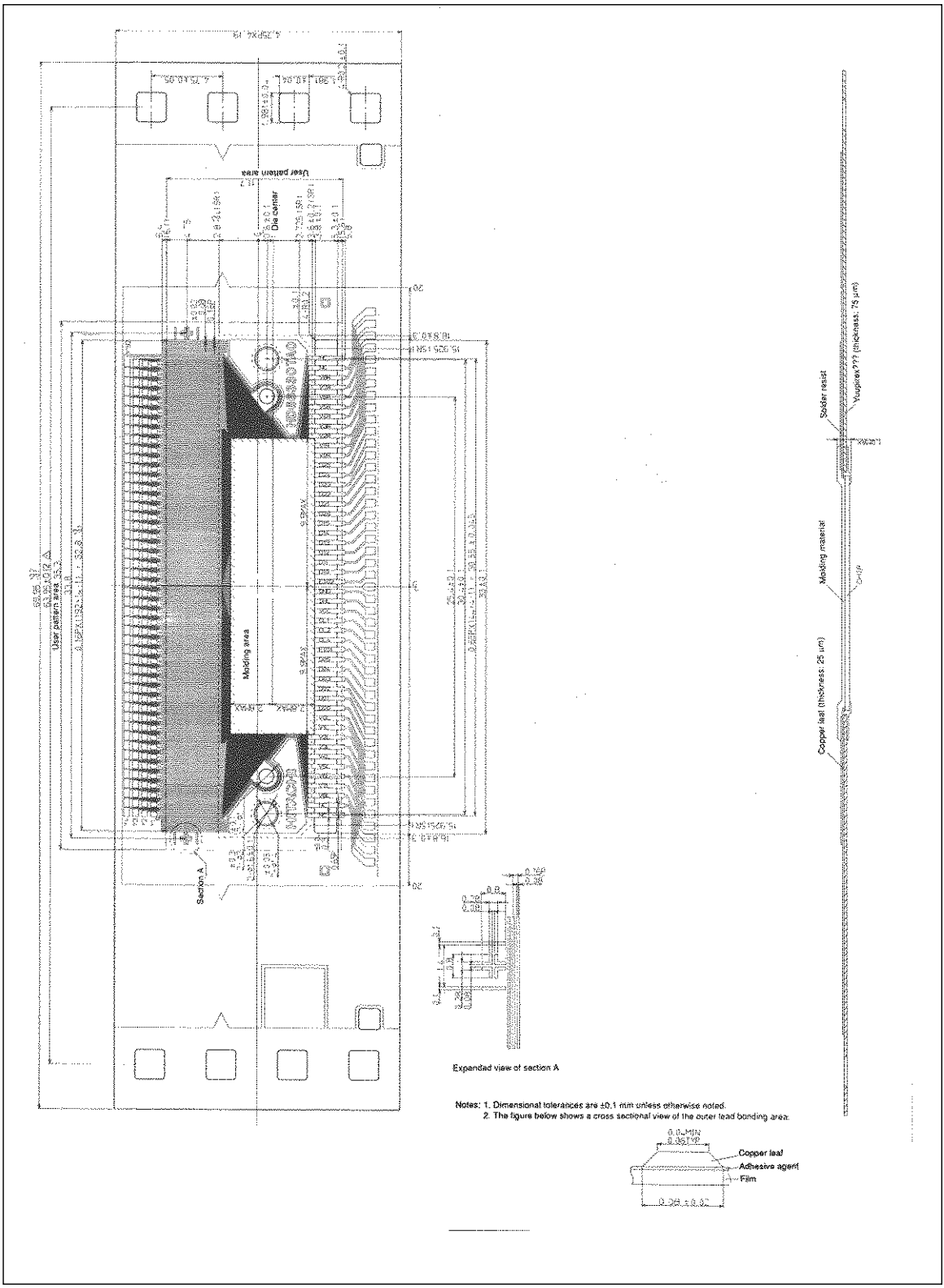


Figure 38 Hitachi Standard TCP 21 — HD66330TA0 —

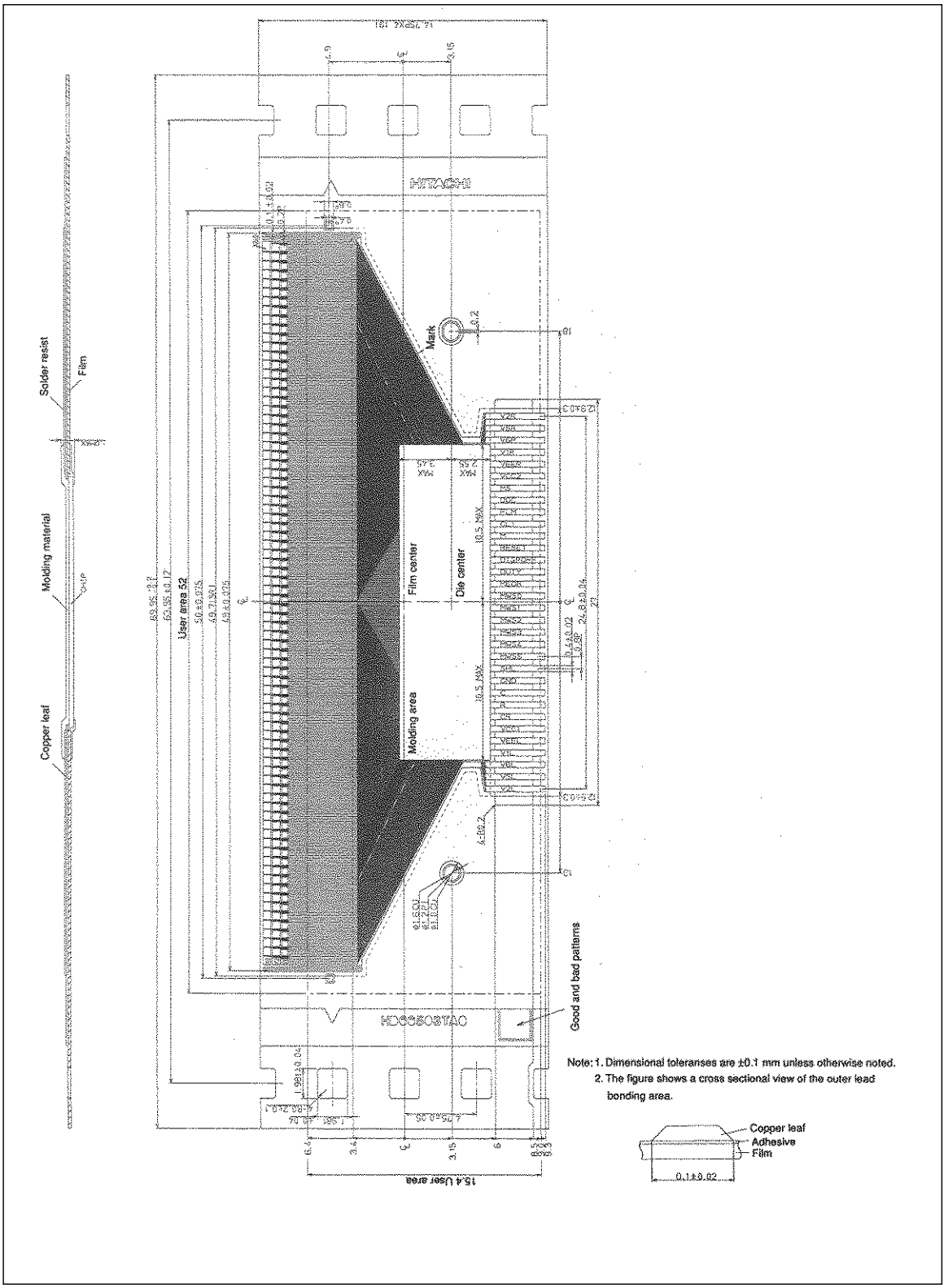


Figure 39 Hitachi Standard TCP 22 — HD66503TA0 —

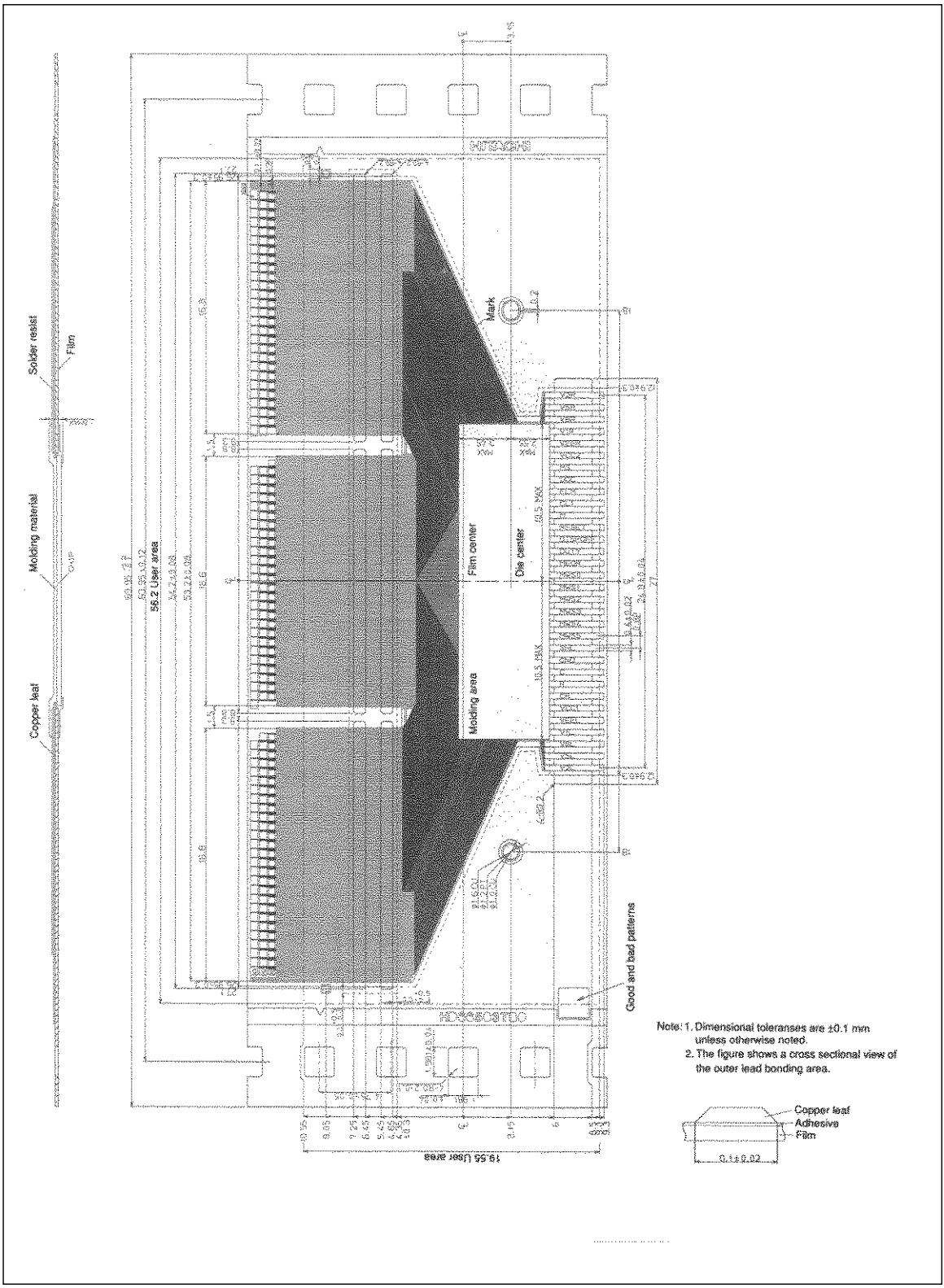


Figure 40 Hitachi Standard TCP 23 — HD66503TB0 —

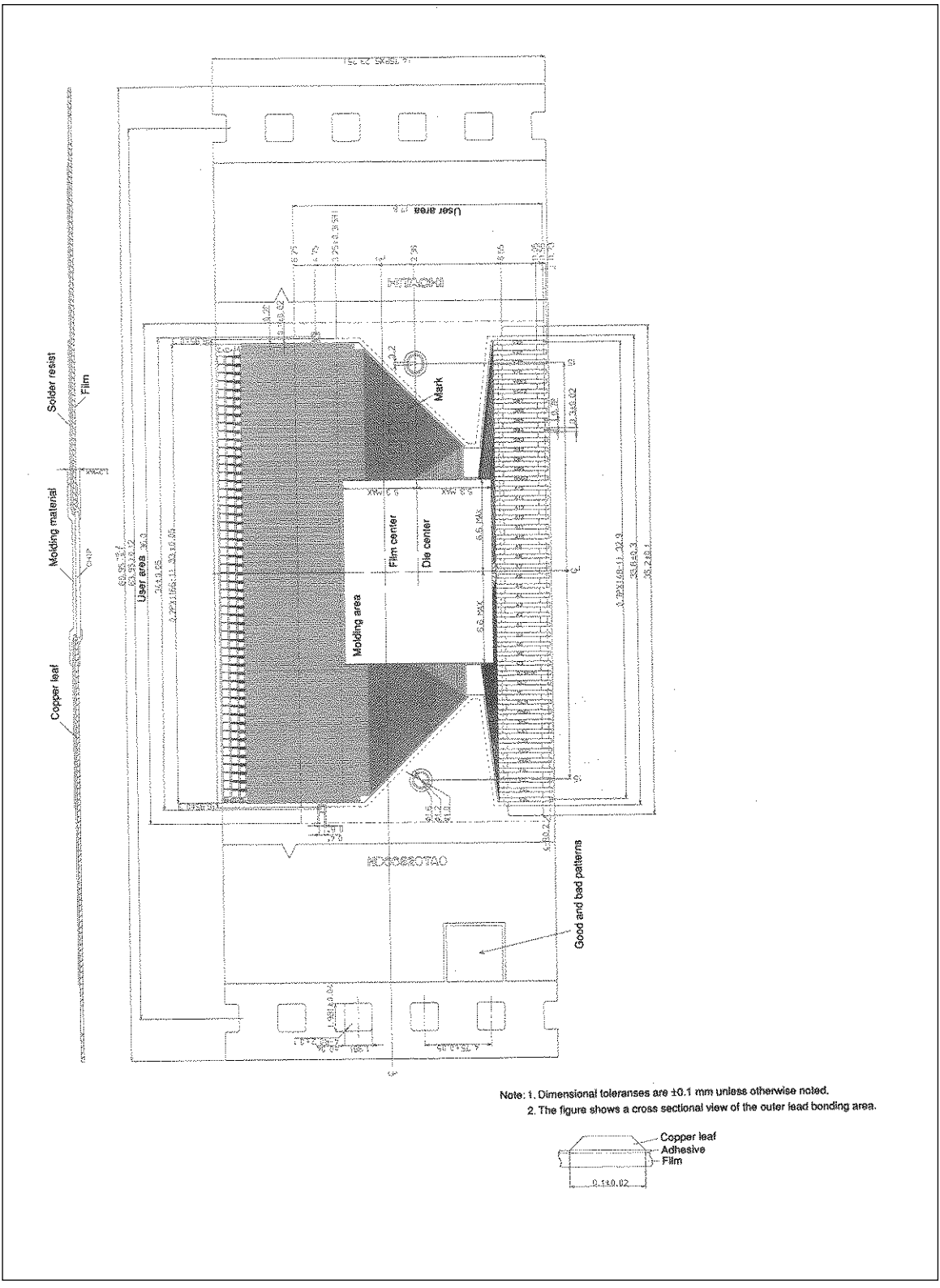


Figure 41 Hitachi Standard TCP 24 — HD66520TA0 —

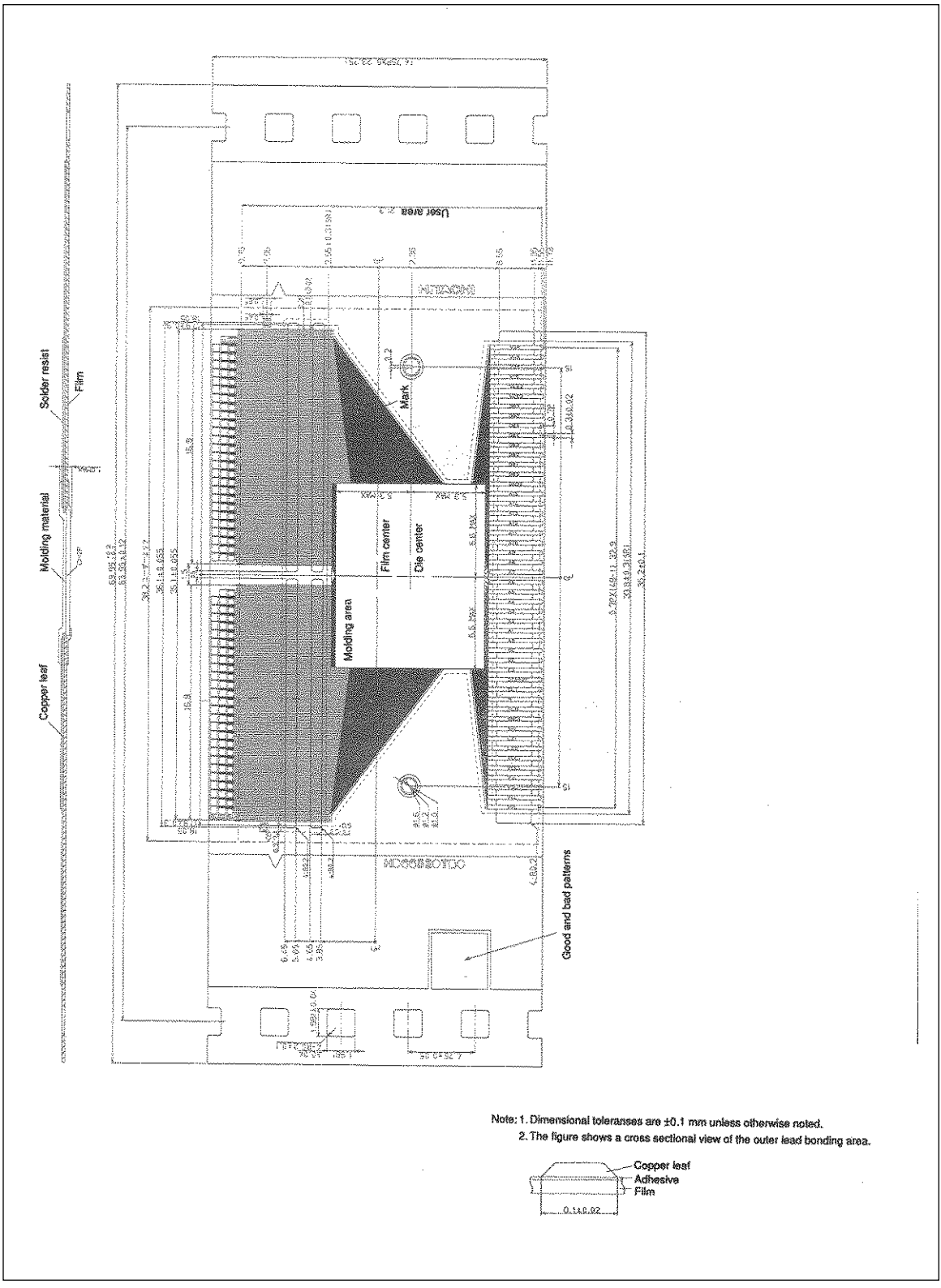
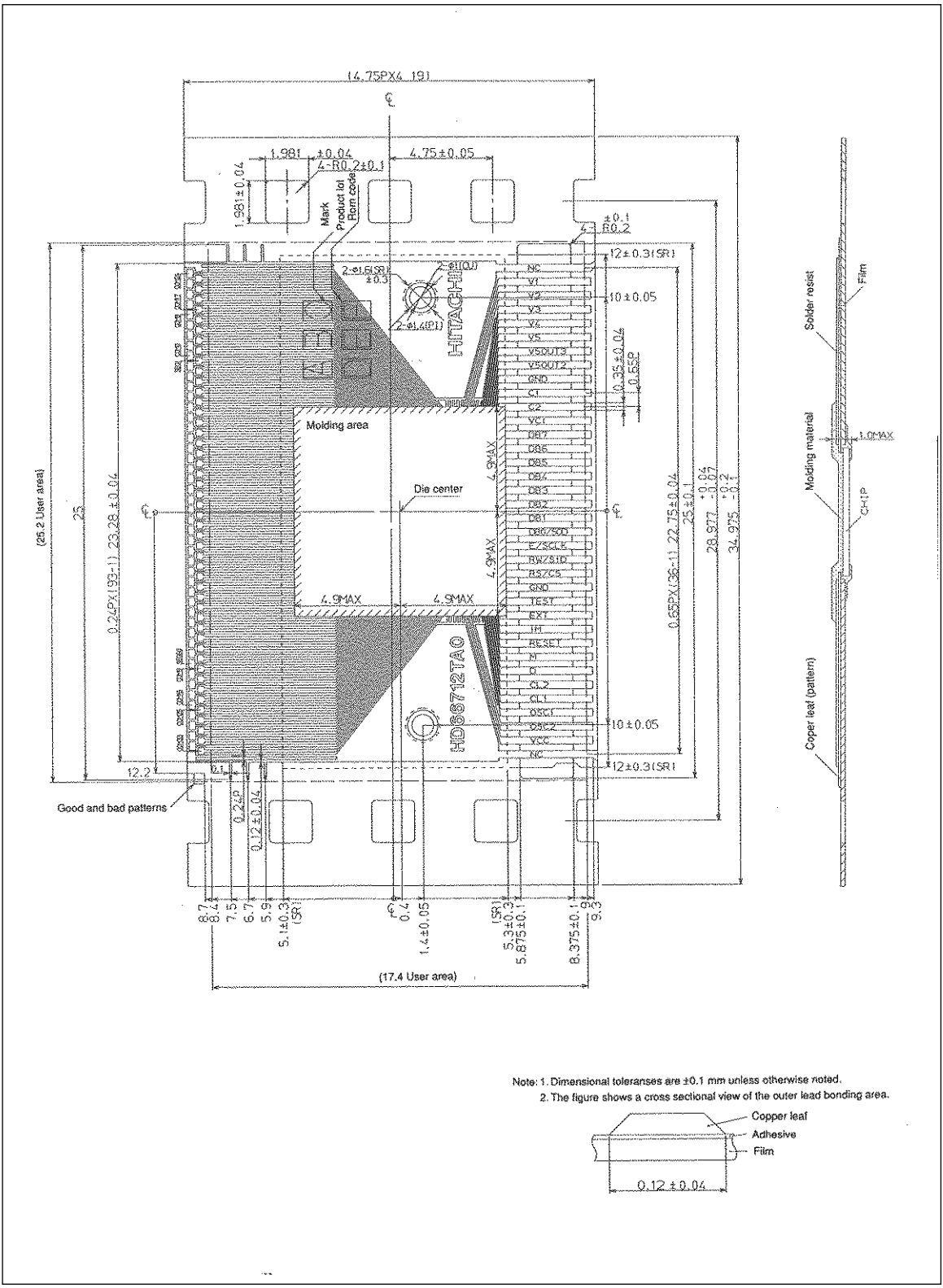
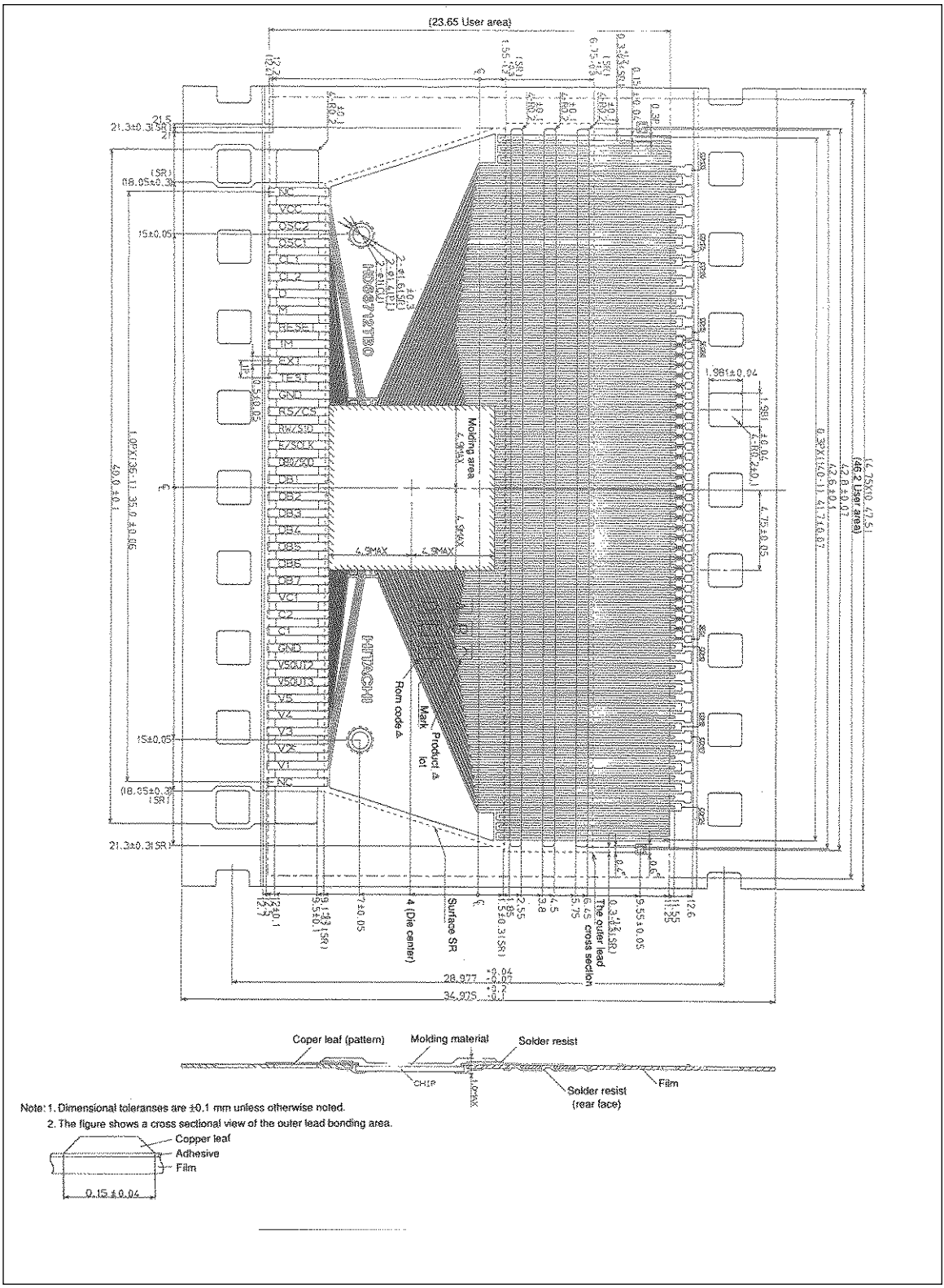


Figure 42 Hitachi Standard TCP 25 — HD66520TB0 —



Note: 1. Dimensional toleranses are ±0.1 mm unless otherwise noted.
2. The figure shows a cross sectional view of the outer lead bonding area.

Figure 43 Hitachi Standard TCP 26 — HD66712TA0 —



Note: 1. Dimensional toleranses are ±0.1 mm unless otherwise noted.
2. The figure shows a cross sectional view of the outer lead bonding area.

Figure 44 Hitachi Standard TCP 27 — HD66712TB0 —

Chip Shipment Products

COB (chip on board) and COG (chip on glass) products form only a small percentage of the thin form and miniature mounting products shipped. However, these products, which are referred to here as “chip shipment products”, involve shipping unmounted chips from the factory.

Since chip shipment products are treated as semi-finished products, there will be differences between their quality guarantee ranges and electrical characteristics items and those published for the packaged (i.e., complete) products. The differences in the quality guarantee ranges, electrical characteristics items, and visual inspection are described in the CAS (customer approval specifications). Product functionality and operation is completely identical to the complete (packaged) product.

This section describes the standard shipment specifications for chip shipment products. The actual shipment stipulations will be those mentioned or stipulated in the CAS for the individual products.

1. Electrical Characteristics and Quality Level

As mentioned above, the quality guarantee ranges and electrical characteristics for chip shipment products differ from those for standard products. Refer to the CAS for the individual products for specific details.

The basic differences are as follows.

1.1 Electrical Characteristics

The electrical characteristics for chip shipment products are guaranteed at the single point T_a = 75°C.

1.2 Quality Level

Electrical characteristics: AQL 4.0%
Visual inspection: AQL 4.0%

(The specific details for visual inspection and other items are contained in the CAS.)

2. Chip Packing Specifications

2.1 Delivery Units

Delivery unit counts (lot size) range from a minimum of 100 units to 10,000 units.

2.2 Packing Specifications

Trays are vacuum packed and sealed with up to 24 trays in a single pack. All the chip products in a given pack will be from the same production lot. Figure 1 shows the chip shipment product packing. Chip products are stored in the trays protected by a sheet of protective paper.

2.3 Markings

The following items will be marked on each tray.

1. Product number
2. Lot number
3. Count
4. Inspection certification seal

The following items will be marked on each pack.

1. Product number
2. Disbursement lot number
3. Count
4. Inspection certification seal

The following items will be marked on the outer packing.

1. Product number
2. Disbursement lot number
3. Count
4. Inspection certification seal

If possible, please return empty trays to your Hitachi sales representative.

3. Storage Specifications

After delivery and after opening the transport packaging, chip shipment products must be stored in a manner that does not cause their electrical, physical, or mechanical properties to degrade due to humidity or reactive gas contamination.

We recommend the following storage conditions for these products.

Chip Shipment Products

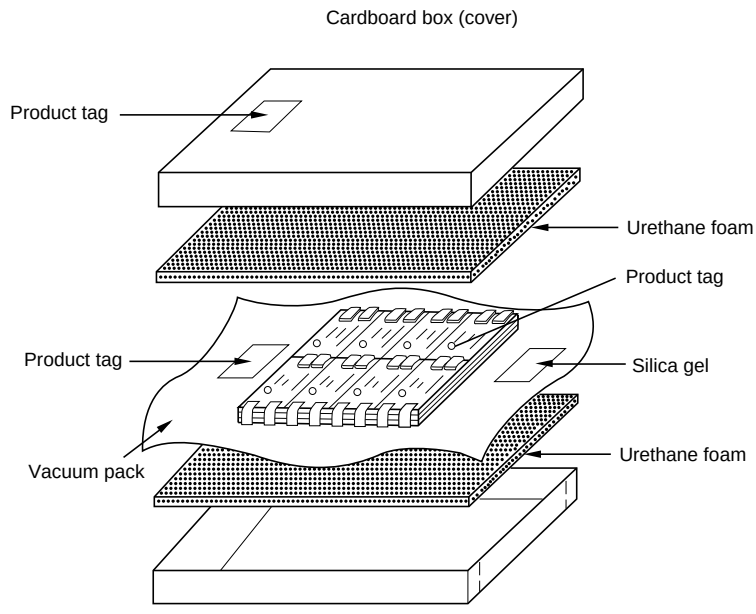
3.1 When Stored in the Packed State

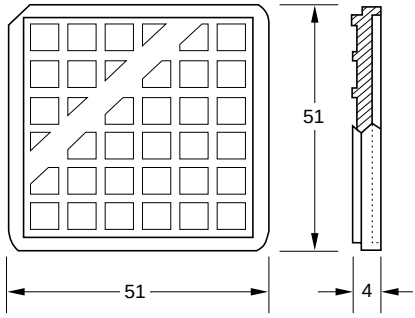
Storage conditions: In dry Nitrogen, at –30°C (30 degrees below zero, Celsius)
Storage period: Six months

The date of the inspection certification seal shall be used as the start of the storage period.

3.2 When Stored after Die Bonding or Wire Bonding

Storage condition 1: Temperature: under 30°C, Humidity: under 70%, Airborne particles: less than 5000 per cubic foot
Storage period 1: Seven days
Storage conditions 2: In dry Nitrogen, at –30°C
Storage period 2: 20 days





36 pcs./ tray	HD44780SA00D, HCD66702, HD44102D, HD44105D, HD61202D, HD61203D, HD61104AD, HD61105AD, HD66106D
49 pcs./ tray	
64 pcs./ tray	HD44100D, HD66100D, HCD66204, HCD66205

Figure 1 Chip Packing

4. Chip Shape Specifications

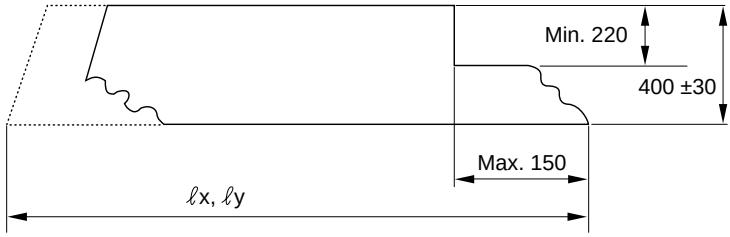
See figure 2.

5. Products Available as Chip Shipment Products

Hitachi, Ltd. currently provides the products listed in table 1 as chip shipment products. Figures 3 to 19 show their respective chip sizes and bonding pad layouts.

Table 1 Chip Shipment Product Table

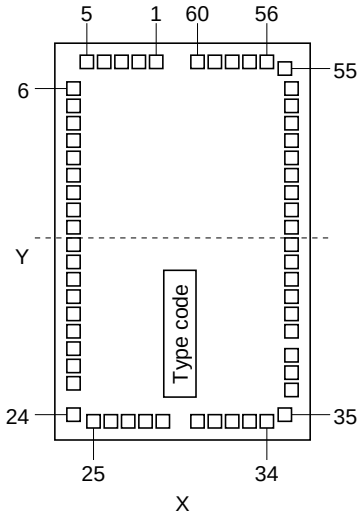
Figure No.	Product No.	Base Product No.	Page
3	HCD44100R	HD44100RFS	101
4	HD44102D	HD44102CH	102
5	HD44105D	HD44105H	103
6	HCD44780U***	HD44780U***FS	104
7	HCD66702R***	HD66702R***F	105
7	HCD66702R***L	HD66702R***FL	105
8	HCD66710***	HD66710***FS	107
9	HD61202D	HD61202	108
10	HCD66712***	HD66712***FS	109
11	HCD66720***	HD66720***FS	111
12	HCD66730***	HD66730***FS	112
13	HD61203D	HD61203	114
14	HD66100D	HD66100F	115
15	HD66106D	HD66106FS	116
16	HCD66204	HD66204F	117
17	HCD66205	HD66205F	118
18	HCD66204L	HD66204FL	119
19	HCD66205L	HD66205FL	120



Surface shape maximum values
X direction: ℓx + 250
Y direction: ℓy + 250
(ℓx and ℓy are the chip dimensions)
(unit: µm)

Figure 2 Chip Cross-Section

- HCD44100R



Chip size (X × Y): 2.40 mm × 3.94 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 90 µm × 90 µm (SiL)

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y30	–280	1815
2	Y31	–460	1815
3	Y32	–640	1815
4	Y33	–820	1815
5	Y34	–1000	1815
6	Y29	–1045	1600
7	Y28	–1045	1420
8	Y27	–1045	1240
9	Y26	–1045	1060
10	Y25	–1045	880
11	Y24	–1045	700
12	Y23	–1045	520
13	Y22	–1045	340
14	Y21	–1045	160
15	Y20	–1045	–20
16	Y19	–1045	–200
17	Y18	–1045	–380
18	Y17	–1045	–560
19	Y16	–1045	–740
20	Y15	–1045	–920

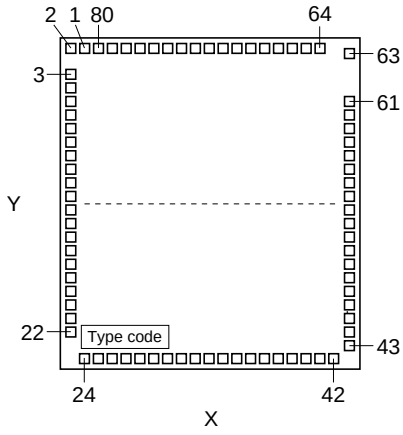
Pad No.	Pad Name	Coordinate X	Coordinate Y
21	Y14	–1045	–1100
22	Y13	–1045	–1300
23	Y12	–1045	–1500
24	Y9	–1045	–1740
25	Y10	–850	–1815
26	Y11	–670	–1815
27	Y8	–490	–1815
28	Y7	–310	–1815
29	V_{CC}	–130	–1815
30	Y6	130	–1815
31	Y5	310	–1815
32	Y4	490	–1815
33	Y3	670	–1815
34	Y2	870	–1815
35	Y1	1030	–1780
36	V_{EE}	1075	–1600
37	CL1	1075	–1410
38	CL2	1075	–1235
39	GND	1075	–990
40	DL1	1075	–810

Pad No.	Pad Name	Coordinate X	Coordinate Y
41	DR1	1075	–630
42	DL2	1075	–450
43	DR2	1075	–270
44			
45	M	1075	–90
46	SHL1	1075	90
47	SHL2	1075	270
48	FCS	1075	450
49	V1	1075	630
50	V2	1075	810
51	V3	1075	990
52	V4	1075	1170
53	V5	1075	1350
54	V6	1075	1550
55	Y40	1045	1800
56	Y39	850	1815
57	Y38	670	1815
58	Y37	490	1815
59	Y36	310	1815
60	Y35	130	1815

Figure 3 HCD44100R

Chip Shipment Products

- HD44102D



Chip size (X × Y): 5.40 mm × 6.16 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 120 µm × 120 µm

(Unit: µm)

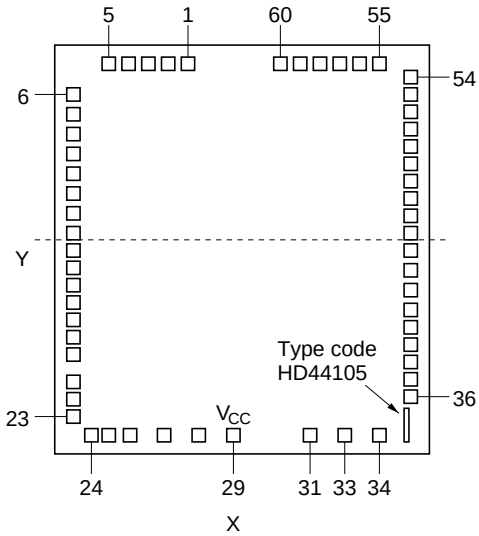
Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y39	–2130	2890
2	Y38	–2465	2890
3	Y37	–2515	2465
4	Y36	–2515	2215
5	Y35	–2515	1965
6	Y34	–2515	1715
7	Y33	–2515	1465
8	Y32	–2515	1215
9	Y31	–2515	965
10	Y30	–2515	715
11	Y29	–2515	465
12	Y28	–2515	215
13	Y27	–2515	–35
14	Y26	–2515	–285
15	Y25	–2515	–535
16	Y24	–2515	–785
17	Y23	–2515	–1035
18	Y22	–2515	–1285
19	Y21	–2515	–1535
20	Y20	–2515	–1785
21	Y19	–2515	–2035
22	Y18	–2515	–2285
23			
24	Y17	–2155	–2890
25	Y16	–1865	–2890
26	Y15	–1635	–2890
27	Y14	–1405	–2890

Pad No.	Pad Name	Coordinate X	Coordinate Y
28	Y13	–1175	–2890
29	Y12	–945	–2890
30	Y11	–715	–2890
31	Y10	–480	–2890
32	Y9	–255	–2890
33	Y8	–25	–2890
34	Y7	205	–2890
35	Y6	435	–2890
36	Y5	665	–2890
37	Y4	915	–2890
38	Y3	1160	–2890
39	Y2	1410	–2890
40	Y1	1640	–2890
41	V_{CC}	1930	–2890
42	BS	2245	–2890
43	RST	2515	–2605
44	CS1	2515	–2365
45	CS2	2515	–2125
46	CS3	2515	–1885
47	E	2515	–1645
48	RW	2515	–1405
49	D1	2515	–1165
50	DB0	2515	–880
51	DB1	2515	–600
52	DB2	2515	–330
53	DB3	2515	–50
54	DB4	2515	220

Pad No.	Pad Name	Coordinate X	Coordinate Y
55	DB5	2515	500
56	DB6	2515	770
57	DB7	2515	1050
58	FRM	2515	1320
59	CL	2515	1560
60	P1 (ø1)	2515	1800
61	P2 (ø2)	2515	2040
62			
63	M	2515	2815
64	GND	2070	2890
65	V_{EE}	1835	2890
66	V1	1600	2890
67	V2	1365	2890
68	V3	1135	2890
69	V4	890	2890
70	Y50	640	2890
71	Y49	410	2890
72	Y48	180	2890
73	Y47	–50	2890
74	Y46	–340	2890
75	Y45	–605	2890
76	Y44	–850	2890
77	Y43	–1100	2890
78	Y42	–1350	2890
79	Y41	–1600	2890
80	Y40	–1845	2890

Figure 4 HD44102D

- HD44105D



Chip size (X × Y): 4.56 mm × 6.00 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 120 µm × 120 µm

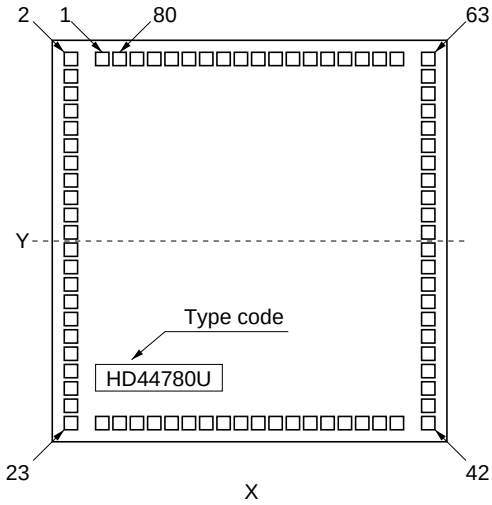
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	X12	–575	2822
2	X11	–875	2822
3	X10	–1175	2822
4	X9	–1475	2822
5	X8	–1775	2822
6	X7	–2105	2372
7	X6	–2105	2047
8	X5	–2105	1732
9	X4	–2105	1417
10	X3	–2105	1102
11	X2	–2105	787
12	X1	–2105	472
13	DL	–2105	117
14	GND	–2105	–208
15	FS1	–2105	–438
16	FS2	–2105	–668
17	DS1	–2105	–898
18	DS2	–2105	–1128
19	DS3	–2105	–1358
20	C	–2105	–1628
21	R	–2105	–2053
22	CR	–2105	–2363
23	$\overline{STB}$	–2105	–2593
24	SHL	–2005	–2822
25	M/S	–1770	–2822
26	ø2	–1460	–2822
27	ø1	–1010	–2822
28	FRM	–605	–2822
29	V_{CC}	–265	–2822
31	M	770	–2822
33	CL	1290	–2822
34	DR	1730	–2822
36	V_{EE}	2105	–2308
37	V1	2105	–2078
38	V2	2105	–1848
39	V5	2105	–1610
40	V6	2105	–1388
41	X32	2105	–1138
42	X31	2105	–833
43	X30	2105	–528
44	X29	2105	–223
45	X28	2105	82
46	X27	2105	387
47	X26	2105	697
48	X25	2105	1002
49	X24	2105	1307
50	X23	2105	1587
51	X22	2105	1867
52	X21	2105	2147
53	X20	2105	2427
54	X19	2105	2707
55	X18	1855	2822
56	X17	1555	2822
57	X16	1255	2822
58	X15	955	2822
59	X14	655	2822
60	X13	355	2822

Figure 5 HD44105D

Chip Shipment Products

- HCD44780U***



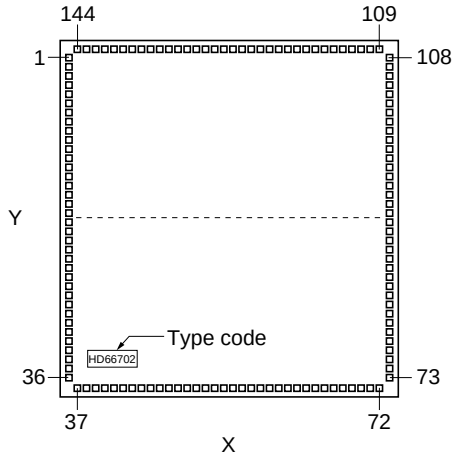
Chip size (X × Y): 4.90 mm × 4.90 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 114 ± 10 µm × 114 ± 10 µm
The aperture area of a bonding pad

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG22	–2100	2313
2	SEG21	–2280	2313
3	SEG20	–2313	2089
4	SEG19	–2313	1833
5	SEG18	–2313	1617
6	SEG17	–2313	1401
7	SEG16	–2313	1186
8	SEG15	–2313	970
9	SEG14	–2313	755
10	SEG13	–2313	539
11	SEG12	–2313	323
12	SEG11	–2313	108
13	SEG10	–2313	–108
14	SEG9	–2313	–323
15	SEG8	–2313	–539
16	SEG7	–2313	–755
17	SEG6	–2313	–970
18	SEG5	–2313	–1186
19	SEG4	–2313	–1401
20	SEG3	–2313	–1617
21	SEG2	–2313	–1833
22	SEG1	–2313	–2073
23	GND	–2280	–2290
24	OSC1	–2080	–2290
25	OSC2	–1749	–2290
26	V1	–1550	–2290
27	V2	–1268	–2290
28	V3	–941	–2290
29	V4	–623	–2290
30	V5	–304	–2290
31	CL1	–48	–2290
32	CL2	142	–2290
33	V_{CC}	309	–2290
34	M	475	–2290
35	D	665	–2290
36	RS	832	–2290
37	R/$\overline{W}$	1022	–2290
38	E	1204	–2290
39	DB0	1454	–2290
40	DB1	1684	–2290
41	DB2	2070	–2290
42	DB3	2260	–2290
43	DB4	2290	–2099
44	DB5	2290	–1883
45	DB6	2290	–1667
46	DB7	2290	–1452
47	COM1	2313	–1186
48	COM2	2313	–970
49	COM3	2313	–755
50	COM4	2313	–539
51	COM5	2313	–323
52	COM6	2313	–108
53	COM7	2313	108
54	COM8	2313	323
55	COM9	2313	539
56	COM10	2313	755
57	COM11	2313	970
58	COM12	2313	1186
59	COM13	2313	1401
60	COM14	2313	1617
61	COM15	2313	1833
62	COM16	2313	2095
63	SEG40	2296	2313
64	SEG39	2100	2313
65	SEG38	1617	2313
66	SEG37	1401	2313
67	SEG36	1186	2313
68	SEG35	970	2313
69	SEG34	755	2313
70	SEG33	539	2313
71	SEG32	323	2313
72	SEG31	108	2313
73	SEG30	–108	2313
74	SEG29	–323	2313
75	SEG28	–539	2313
76	SEG27	–755	2313
77	SEG26	–970	2313
78	SEG25	–1186	2313
79	SEG24	–1401	2313
80	SEG23	–1617	2313

Figure 6 HCD44780U*

- HCD66702R***, HCD66702R***L



Chip size (X × Y): 5.20 mm × 5.20 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 90 µm × 90 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG34	–2475	2350
2	SEG33	–2475	2205
3	SEG32	–2475	2065
4	SEG31	–2475	1925
5	SEG30	–2475	1790
6	SEG29	–2475	1655
7	SEG28	–2475	1525
8	SEG27	–2475	1395
9	SEG26	–2475	1265
10	SEG25	–2475	1135
11	SEG24	–2475	1005
12	SEG23	–2475	875
13	SEG22	–2475	745
14	SEG21	–2475	615
15	SEG20	–2475	485
16	SEG19	–2475	355
17	SEG18	–2475	225
18	SEG17	–2475	95
19	SEG16	–2475	–35
20	SEG15	–2475	–165
21	SEG14	–2475	–295
22	SEG13	–2475	–425
23	SEG12	–2475	–555
24	SEG11	–2475	–685
25	SEG10	–2475	–815
26	SEG9	–2475	–945
27	SEG8	–2475	–1075
28	SEG7	–2475	–1205
29	SEG6	–2475	–1335
30	SEG5	–2475	–1465
31	SEG4	–2475	–1600
32	SEG3	–2475	–1735
33	SEG2	–2475	–1870
34	SEG1	–2475	–2010
35	GND	–2475	–2180
36	OSC2	–2475	–2325
37	OSC1	–2445	–2475
38	V_{CC}	–2305	–2475
39	V_{CC}	–2165	–2475
40	V1	–2025	–2475
41	V2	–1875	–2475
42	V3	–1745	–2475
43	V4	–1595	–2475
44	V5	–1465	–2475
45	CL1	–1335	–2475
46	CL2	–1185	–2475
47	M	–1055	–2475
48	D	–905	–2475
49	EXT	–775	–2475
50	TEST	–625	–2475
51	GND	–495	–2475
52	RS	–345	–2475
53	R/W	–195	–2475
54	E	–45	–2475
55	DB0	85	–2475
56	DB1	235	–2475
57	DB2	365	–2475
58	DB3	515	–2475
59	DB4	645	–2475
60	DB5	795	–2475
61	DB6	925	–2475
62	DB7	1075	–2475
63	COM1	1205	–2475
64	COM2	1335	–2475
65	COM3	1465	–2475
66	COM4	1595	–2475
67	COM5	1725	–2475
68	COM6	1855	–2475
69	COM7	1990	–2475
70	COM8	2125	–2475
71	COM9	2265	–2475
72	COM10	2410	–2475
73	COM11	2475	–2290
74	COM12	2475	–2145
75	COM13	2475	–2005
76	COM14	2475	–1865
77	COM15	2475	–1730
78	COM16	2475	–1595
79	SEG100	2475	–1465
80	SEG99	2475	–1335
81	SEG98	2475	–1205
82	SEG97	2475	–1075
83	SEG96	2475	–945
84	SEG95	2475	–815

Figure 7 HCD66702R*, HCD66702R***L (1)**

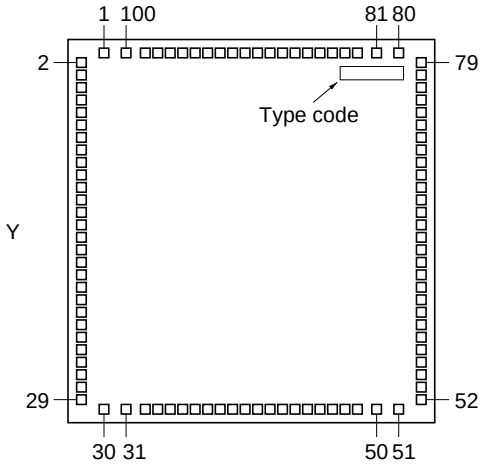
- HCD66702R***, HCD66702R***L

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
85	SEG94	2475	–685	105	SEG74	2475	1925	125	SEG54	195	2475
86	SEG93	2475	–555	106	SEG73	2475	2065	126	SEG53	65	2475
87	SEG92	2475	–425	107	SEG72	2475	2205	127	SEG52	–65	2475
88	SEG91	2475	–295	108	SEG71	2475	2350	128	SEG51	–195	2475
89	SEG90	2475	–165	109	SEG70	2320	2475	129	SEG50	–325	2475
90	SEG89	2475	–35	110	SEG69	2175	2475	130	SEG49	–455	2475
91	SEG88	2475	95	111	SEG68	2035	2475	131	SEG48	–585	2475
92	SEG87	2475	225	112	SEG67	1895	2475	132	SEG47	–715	2475
93	SEG86	2475	355	113	SEG66	1760	2475	133	SEG46	–845	2475
94	SEG85	2475	485	114	SEG65	1625	2475	134	SEG45	–975	2475
95	SEG84	2475	615	115	SEG64	1495	2475	135	SEG44	–1105	2475
96	SEG83	2475	745	116	SEG63	1365	2475	136	SEG43	–1235	2475
97	SEG82	2475	875	117	SEG62	1235	2475	137	SEG42	–1365	2475
98	SEG81	2475	1005	118	SEG61	1105	2475	138	SEG41	–1495	2475
99	SEG80	2475	1135	119	SEG60	975	2475	139	SEG40	–1625	2475
100	SEG79	2475	1265	120	SEG59	845	2475	140	SEG39	–1760	2475
101	SEG78	2475	1395	121	SEG58	715	2475	141	SEG38	–1895	2475
102	SEG77	2475	1525	122	SEG57	585	2475	142	SEG37	–2035	2475
103	SEG76	2475	1655	123	SEG56	455	2475	143	SEG36	–2175	2475
104	SEG75	2475	1790	124	SEG55	325	2475	144	SEG35	–2320	2475

Figure 7 HCD66702R*, HCD66702R***L (2)**

- HCD66710***



Chip size (X × Y): 5.36 mm × 6.06 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

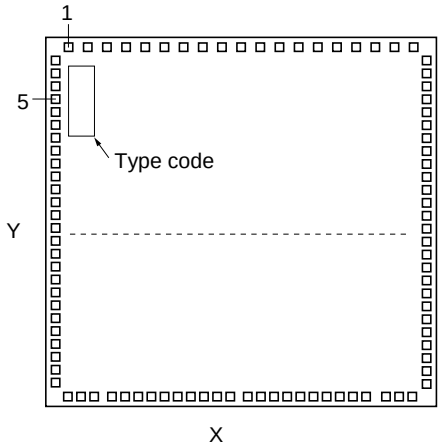
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG27	–2495	2910
2	SEG28	–2695	2730
3	SEG29	–2695	2499
4	SEG30	–2695	2300
5	SEG31	–2695	2100
6	SEG32	–2695	1901
7	SEG33	–2695	1698
8	SEG34	–2695	1498
9	SEG35	–2695	1295
10	SEG36	–2695	1099
11	SEG37	–2695	900
12	SEG38	–2695	700
13	SEG39	–2695	501
14	SEG40	–2695	301
15	COM9	–2695	98
16	COM10	–2695	–113
17	COM11	–2695	–302
18	COM12	–2695	–501
19	COM13	–2695	–701
20	COM14	–2695	–900
21	COM15	–2695	–1100
22	COM16	–2695	–1303
23	COM25	–2695	–1502
24	COM26	–2695	–1702
25	COM27	–2695	–1901
26	COM28	–2695	–2101
27	COM29	–2695	–2300
28	COM30	–2695	–2500
29	COM31	–2695	–2731
30	COM32	–2495	–2910
31	COM24	–2051	–2910
32	COM23	–1701	–2910
33	COM22	–1498	–2910
34	COM21	–1302	–2910
35	COM20	–1102	–2910
36	COM19	–899	–2910
37	COM18	–700	–2910
38	COM17	–500	–2910
39	COM8	–301	–2910
40	COM7	–101	–2910
41	COM6	99	–2910
42	COM5	302	–2910
43	COM4	502	–2910
44	COM3	698	–2910
45	COM2	887	–2910
46	COM1	1077	–2910
47	COM33	1266	–2910
48	V1	1488	–2910
49	V2	1710	–2910
50	V3	2063	–2910
51	V4	2458	–2910
52	V5	2660	–2731
53	V5OUT3	2660	–2500
54	V5OUT2	2660	–2300
55	GND	2640	–2090
56	C1	2650	–1887
57	C2	2675	–1702
58	VCI	2675	–1502
59	OSC1	2675	–1303
60	OSC2	2675	–1103
61	RS	2675	–900
62	R/W	2675	–701
63	E	2675	–501
64	DB0	2675	–302
65	DB1	2675	–99
66	DB2	2675	98
67	DB3	2675	301
68	DB4	2675	501
69	DB5	2675	700
70	DB6	2675	900
71	DB7	2675	1099
72	EXT	2675	1299
73	TEST	2675	1502
74	V_{CC}	2695	1698
75	SEG1	2695	1901
76	SEG2	2695	2104
77	SEG3	2695	2300
78	SEG4	2695	2503
79	SEG5	2695	2730
80	SEG6	2495	2910
81	SEG7	2049	2910
82	SEG8	1699	2910
83	SEG9	1499	2910
84	SEG10	1300	2910
85	SEG11	1100	2910
86	SEG12	901	2910
87	SEG13	701	2910
88	SEG14	502	2910
89	SEG15	299	2910
90	SEG16	99	2910
91	SEG17	–101	2910
92	SEG18	–301	2910
93	SEG19	–500	2910
94	SEG20	–700	2910
95	SEG21	–899	2910
96	SEG22	–1099	2910
97	SEG23	–1302	2910
98	SEG24	–1501	2910
99	SEG25	–1701	2910
100	SEG26	–2051	2910

Figure 8 HCD66710*

Chip Shipment Products

- HD61202D



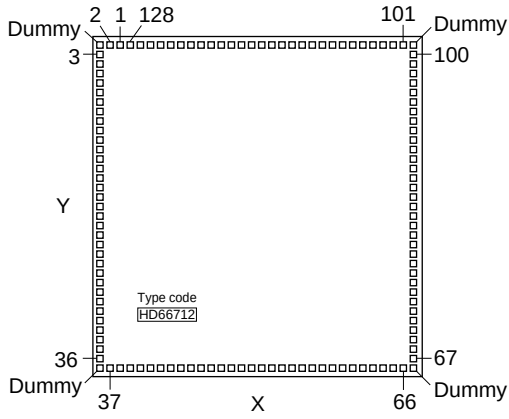
Chip size (X × Y): 6.08 mm × 5.92 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	ADC	–2674	2806
2	M	–2882	2612
3	V_{CC}	–2882	2400
4	V4R	–2882	2213
5	V3R	–2882	2030
6	V2R	–2882	1838
7	V1R	–2882	1655
8	VEE2	–2882	1478
9	Y64	–2882	1258
10	Y63	–2882	1042
11	Y62	–2882	826
12	Y61	–2882	610
13	Y60	–2882	394
14	Y59	–2882	178
15	Y58	–2882	–38
16	Y57	–2882	–254
17	Y56	–2882	–470
18	Y55	–2882	–686
19	Y54	–2882	–902
20	Y53	–2882	–1118
21	Y52	–2882	–1334
22	Y51	–2882	–1550
23	Y50	–2882	–1766
24	Y49	–2882	–1982
25	Y48	–2882	–2198
26	Y47	–2882	–2414
27	Y46	–2882	–2630
28	Y45	–2802	–2806
29	Y44	–2586	–2806
30	Y43	–2370	–2806
31	Y42	–2034	–2806
32	Y41	–1818	–2806
33	Y40	–1602	–2806
34	Y39	–1386	–2806
35	Y38	–1174	–2806
36	Y37	–962	–2806
37	Y36	–750	–2806
38	Y35	–538	–2806
39	Y34	–326	–2806
40	Y33	–114	–2806
41	Y32	98	–2806
42	Y31	314	–2806
43	Y30	530	–2806
44	Y29	746	–2806
45	Y28	962	–2806
46	Y27	1178	–2806
47	Y26	1394	–2806
48	Y25	1610	–2806
49	Y24	1826	–2806
50	Y23	2042	–2806
51	Y22	2378	–2806
52	Y21	2590	–2806
53	Y20	2802	–2806
54	Y19	2882	–2630
55	Y18	2882	–2414
56	Y17	2882	–2198
57	Y16	2882	–1982
58	Y15	2882	–1766
59	Y14	2882	–1550
60	Y13	2882	–1334
61	Y12	2882	–1118
62	Y11	2882	–902
63	Y10	2882	–686
64	Y9	2882	–470
65	Y8	2882	–254
66	Y7	2882	–38
67	Y6	2882	178
68	Y5	2882	394
69	Y4	2882	610
70	Y3	2882	826
71	Y2	2882	1042
72	Y1	2882	1258
73	VEE1	2882	1490
74	V1L	2882	1670
75	V2L	2882	1847
76	V3L	2882	2030
77	V4L	2882	2213
78	GND	2882	2400
79	DB0	2882	2618
80	DB1	2514	2806
81	DB2	2262	2806
82	DB3	1922	2806
83	DB4	1670	2806
84	DB5	1330	2806
85	DB6	1078	2806
86	DB7	738	2806
87			
88			
89			
90	CS3	426	2806
91	CS2	126	2806
92	CS1	–134	2806
93	RST	–434	2806
94	RW	–694	2806
95	DI	–994	2806
96	CL	–1254	2806
97	C2	–1554	2806
98	C1	–1814	2806
99	E	–2114	2806
100	FRM	–2374	2806

Figure 9 HD61202D

- HCD66712***



Chip size (X × Y): 6.00 mm × 6.40 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 μm × 100 μm

(Unit: μm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG44	–2450	3046
2	SEG45	–2650	3046
3	SEG46	–2846	2866
4	SEG47	–2846	2886
5	SEG48	–2846	2340
6	SEG49	–2846	2160
7	SEG50	–2846	2000
8	SEG51	–2846	1840
9	SEG52	–2846	1680
10	SEG53	–2846	1520
11	SEG54	–2846	1360
12	SEG55	–2846	1200
13	SEG56	–2846	1040
14	SEG57	–2846	880
15	SEG58	–2846	720
16	SEG59	–2846	560
17	SEG60	–2846	400
18	COM9	–2846	240
19	COM10	–2846	80
20	COM11	–2846	–80
21	COM12	–2846	–240
22	COM13	–2846	–400
23	COM14	–2846	–560
24	COM15	–2846	–720
25	COM16	–2846	–880
26	COM25	–2846	–1040
27	COM26	–2846	–1200
28	COM27	–2846	–1360
29	COM28	–2846	–1520
30	COM29	–2846	–1680
31	COM30	–2846	–1840
32	COM31	–2846	–2000
33	COM32	–2846	–2160
34	COM33	–2846	–2320
35	V_{CC}	–2857	–2697
36	OSC2	–2857	–2877
37	OSC1	–2650	–3057
38	CL1	–2460	–3057
39	CL2	–2290	–3057
40	D	–2130	–3057
41	M	–1970	–3057
42	RESET	–1810	–3057
43	IM	–1650	–3057
44	EXT	–1490	–3057
45	TEST	–1330	–3057
46	GND	–1170	–3057
47	RS/CS	–990	–3057
48	RW/SiD	–820	–3057
49	E/SCLK	–650	–3057
50	DB0/SOD	–480	–3057
51	DB1	–310	–3057
52	DB2	–140	–3057
53	DB3	30	–3057
54	DB4	200	–3057
55	DB5	370	–3057
56	DB6	540	–3057
57	DB7	710	–3057
58	Vci	880	–3057
59	C2	1063	–3057
60	C1	1251	–3035
61	GND	1426	–3002
62	V5OUT2	1720	–3057
63	V5OUT3	2050	–3057
64	V5	2250	–3057
65	V4	2450	–3057
66	V3	2650	–3057
67	V2	2877	–2880
68	V1	2877	–2703
69	COM24	2846	–2320
70	COM23	2846	–2160
71	COM22	2846	–2000
72	COM21	2846	–1840
73	COM20	2846	–1680
74	COM19	2846	–1520
75	COM18	2846	–1360
76	COM17	2846	–1200
77	COM8	2846	–1040
78	COM7	2846	–880
79	COM6	2846	–720
80	COM5	2846	–560
81	COM4	2846	–400
82	COM3	2846	–240
83	COM2	2846	–80
84	COM1	2846	80
85	COM0	2846	240
86	SEG1	2846	400
87	SEG2	2846	560
88	SEG3	2846	720
89	SEG4	2846	880
90	SEG5	2846	1040
91	SEG6	2846	1200
92	SEG7	2846	1360
93	SEG8	2846	1520
94	SEG9	2846	1680
95	SEG10	2846	1840
96	SEG11	2846	2000
97	SEG12	2846	2160
98	SEG13	2846	2340
99	SEG14	2846	2686
100	SEG15	2846	2866
101	SEG16	2650	3046
102	SEG17	2450	3046

Figure 10 HCD66712* (1)**

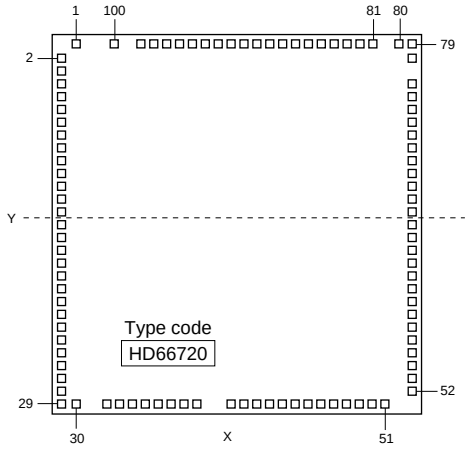
- HCD66712***

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
103	SEG18	2250	3046
104	SEG19	2070	3046
105	SEG20	1890	3046
106	SEG21	1710	3046
107	SEG22	1530	3046
108	SEG23	1350	3046
109	SEG24	1170	3046
110	SEG25	990	3046
111	SEG26	810	3046
112	SEG27	630	3046
113	SEG28	450	3046
114	SEG29	270	3046
115	SEG30	90	3046
116	SEG31	–90	3046
117	SEG32	–270	3046
118	SEG33	–450	3046
119	SEG34	–630	3046
120	SEG35	–810	3046
121	SEG36	–990	3046
122	SEG37	–1170	3046
123	SEG38	–1350	3046
124	SEG39	–1530	3046
125	SEG40	–1710	3046
126	SEG41	–1890	3046
127	SEG42	–2070	3046
128	SEG43	–2250	3046
—	Dummy	–2846	3046
—	Dummy	–2857	–3057
—	Dummy	2877	–3057
—	Dummy	2846	3046

Figure 10 HCD66712* (2)**

- HCD66720***



Chip size (X × Y): 5.60 mm × 6.0 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

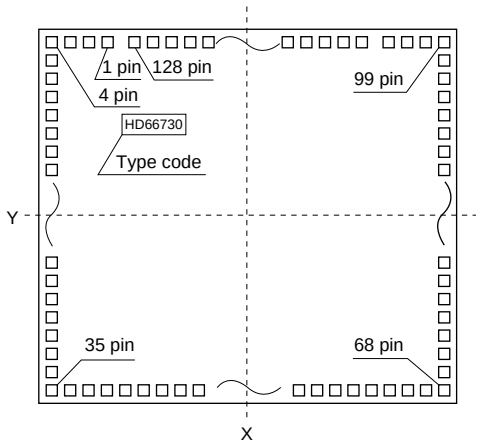
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG22	–2400	2877
2	SEG23	–2677	2700
3	SEG24	–2677	2500
4	SEG25	–2677	2300
5	SEG26	–2677	2100
6	SEG27	–2677	1900
7	SEG28	–2677	1700
8	SEG29	–2677	1500
9	SEG30	–2677	1300
10	SEG31	–2677	1100
11	SEG32	–2677	900
12	SEG33	–2677	700
13	SEG34	–2677	500
14	SEG35	–2677	300
15	SEG36	–2677	100
16	SEG37	–2677	–100
17	SEG38	–2677	–300
18	SEG39	–2677	–500
19	SEG40	–2677	–700
20	SEG41	–2677	–900
21	SEG42	–2677	–1100
22	SEG43/COM1	–2677	–1300
23	SEG44/COM2	–2677	–1500
24	SEG45/COM3	–2677	–1700
25	SEG46/COM4	–2677	–1900
26	SEG47/COM5	–2677	–2100
27	SEG48/COM6	–2677	–2300
28	SEG49/COM7	–2677	–2677
29	SEG50/COM8	–2677	–2877
30	COM1/COM9	–2400	–2877
31	COM2/COM10	–1900	–2877
32	COM3/COM11	–1700	–2877
33	COM4/COM12	–1500	–2877
34	COM5/COM13	–1300	–2877
35	COM6/COM14	–1100	–2877
36	COM7/COM15	–900	–2877
37	COM8/COM16	–700	–2877
38	COMS	–500	–2877
39	V1	–150	–2853
40	V2	100	–2853
41	V3	300	–2853
42	V4	500	–2853
43	V5	800	–2853
44	V5OUT3	1020	–2809
45	V5OUT2	1200	–2809
46	GND	1400	–2790
47	C1	1600	–2853
48	C2	1800	–2809
49	Vci	2000	–2809
50	V_{CC}	2200	–2853
51	OSC1	2400	–2853
52	OSC2	2653	–2700
53	CL1	2653	–2500
54	CL2	2653	–2300
55	D	2653	–2100
56	M	2653	–1900
57	CS*	2653	–1700
58	SCLK	2653	–1500
59	SiD	2653	–1300
60	SOD	2653	–1100
61	NL	2653	–900
62	RESET*	2653	–700
63	TEST2	2653	–500
64	TEST1	2653	–300
65	GND	2653	–30
66	LED0	2653	174
67	LED1	2653	350
68	iRQ*	2653	540
69	KST0	2653	730
70	KST1	2653	920
71	KST2	2653	1110
72	KST3	2653	1300
73	KST4	2653	1500
74	KST5	2653	1700
75	KiN0	2653	1900
76	KiN1	2653	2100
77	KiN2	2653	2300
78	KiN3	2653	2653
79	KiN4	2653	2853
80	SEG1	2400	2877
81	SEG2	1900	2877
82	SEG3	1700	2877
83	SEG4	1500	2877
84	SEG5	1300	2877
85	SEG6	1100	2877
86	SEG7	900	2877
87	SEG8	700	2877
88	SEG9	500	2877
89	SEG10	300	2877
90	SEG11	100	2877
91	SEG12	–100	2877
92	SEG13	–300	2877
93	SEG14	–500	2877
94	SEG15	–700	2877
95	SEG16	–900	2877
96	SEG17	–1100	2877
97	SEG18	–1300	2877
98	SEG19	–1500	2877
99	SEG20	–1700	2877
100	SEG21	–1900	2877

Figure 11 HCD66720*

Chip Shipment Products

- HCD66730***



Chip size (X × Y): 7.48 mm × 6.46 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	SEG34	–2602	3012
2	SEG35	–2984	3012
3	SEG36	–3263	3012
4	SEG37	–3522	3012
5	SEG38	–3522	2782
6	SEG39	–3522	2582
7	SEG40	–3522	2341
8	SEG41	–3522	2161
9	SEG42	–3522	1981
10	SEG43	–3522	1801
11	SEG44	–3522	1621
12	SEG45	–3522	1440
13	SEG46	–3522	1260
14	SEG47	–3522	1030
15	SEG48	–3522	800
16	SEG49	–3522	620
17	SEG50	–3522	439
18	SEG51	–3522	259
19	SEG52	–3522	79
20	SEG53	–3522	–101
21	SEG54	–3522	–281
22	SEG55	–3522	–462
23	SEG56	–3522	–642
24	SEG57	–3522	–822
25	SEG58	–3522	–1002
26	SEG59	–3522	–1182
27	SEG60	–3522	–1363
28	SEG61	–3522	–1543
29	SEG62	–3522	–1723
30	SEG63	–3522	–1939
31	SEG64	–3522	–2183
32	SEG65	–3522	–2364
33	SEG66	–3522	–2544
34	SEG67	–3522	–2774
35	SEG68	–3522	–2984
36	SEG69	–3160	–2984
37	SEG70	–2860	–2984
38	SEG71	–2660	–2984
39	V_{CC}	–2435	–2984
40	RESET*	–2233	–2984
41	OSC2	–2063	–2984
42	OSC1	–1859	–2984
43	CL1	–1689	–2984
44	CL2	–1519	–2984
45	SEGD	–1349	–2984
46	M	–1179	–2984
47	RW/SID	–975	–2984
48	RS/CS*	–771	–2984
49	E/SCLK	–567	–2984
50	IM	–363	–2984
51	DB0/SOD	–146	–2984
52	DB1	71	–2984
53	DB2	287	–2984
54	DB3	504	–2984
55	DB4	721	–2984
56	DB5	938	–2984
57	DB6	1154	–2984
58	DB7	1371	–2984
59	GND	1533	–2984
60	Vci	1730	–2959
61	C2	1896	–2959
62	C1	2057	–2959
63	V5OUT2	2219	–2959
64	V5OUT3	2478	–2959
65	V5	2782	–2984
66	V4	3016	–2984
67	V3	3253	–2984
68	V2	3522	–2984
69	V1	3522	–2806
70	COM25/D	3522	–2626
71	COM24	3522	–2445
72	COM23	3522	–2265
73	COM22	3522	–2085
74	COM21	3522	–1855
75	COM20	3522	–1625
76	COM19	3522	–1444
77	COM18	3522	–1264
78	COM17	3522	–1084
79	COM16	3522	–854
80	COM15	3522	–624
81	COM14	3522	–443
82	COM13	3522	–263
83	COM12	3522	–83
84	COM11	3522	97
85	COM10	3522	277
86	COM9	3522	458
87	COM8	3522	638
88	COM7	3522	818
89	COM6	3522	998
90	COM5	3522	1178
91	COM4	3522	1409
92	COM3	3522	1639
93	COM2	3522	1819
94	COM1	3522	1999
95	COMS	3522	2179
96	SEG1	3522	2410
97	SEG2	3522	2590
98	SEG3	3522	2819
99	SEG4	3522	3012
100	SEG5	3222	3012
101	SEG6	2942	3012
102	SEG7	2662	3012

Figure 12 HCD66730* (1)**

- HCD66730***

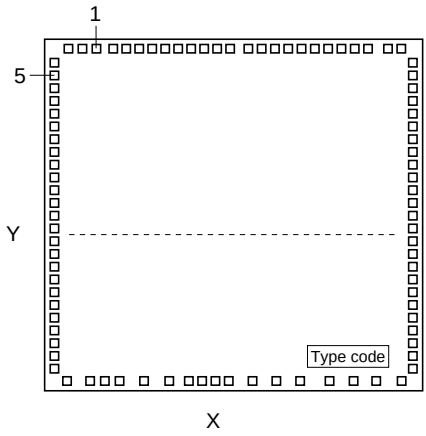
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
103	SEG8	2332	3012
104	SEG9	2152	3012
105	SEG10	1972	3012
106	SEG11	1791	3012
107	SEG12	1611	3012
108	SEG13	1431	3012
109	SEG14	1251	3012
110	SEG15	1071	3012
111	SEG16	890	3012
112	SEG17	710	3012
113	SEG18	530	3012
114	SEG19	350	3012
115	SEG20	170	3012
116	SEG21	–11	3012
117	SEG22	–191	3012
118	SEG23	–371	3012
119	SEG24	–551	3012
120	SEG25	–731	3012
121	SEG26	–912	3012
122	SEG27	–1092	3012
123	SEG28	–1272	3012
124	SEG29	–1452	3012
125	SEG30	–1632	3012
126	SEG31	–1813	3012
127	SEG32	–1993	3012
128	SEG33	–2173	3012

Figure 12 HCD66730* (2)**

Chip Shipment Products

- HD61203D



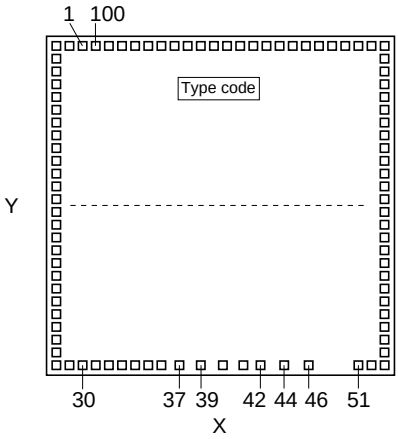
Chip size (X × Y): 5.18 mm × 5.18 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	X22	–1928	2440
2	X21	–2103	2440
3	X20	–2278	2440
4	X19	–2440	2224
5	X18	–2440	2049
6	X17	–2440	1874
7	X16	–2440	1699
8	X15	–2440	1524
9	X14	–2440	1349
10	X13	–2440	1174
11	X12	–2440	999
12	X11	–2440	824
13	X10	–2440	649
14	X9	–2440	474
15	X8	–2440	299
16	X7	–2440	124
17	X6	–2440	–59
18	X5	–2440	–234
19	X4	–2440	–409
20	X3	–2440	–587
21	X2	–2440	–762
22	X1	–2440	–937
23	VEE1	–2440	–1112
24	V6L	–2440	–1287
25	V5L	–2440	–1462
26	V2L	–2440	–1701
27	V1L	–2440	–1876
28	V_{CC}	–2440	–2052
29	DL	–2248	–2440
30	FS	–1944	–2440
31	DS1	–1736	–2440
32	DS2	–1520	–2440
33	C	–1192	–2440
34			
35	R	–904	–2440
36			
37	CR	–572	–2440
38			
39	SHL	–372	–2440
40	GND	–172	–2440
41			
42	MS	16	–2440
43	CK2	344	–2440
44	CK1	644	–2440
45			
46	FRM	908	–2440
47	M	1232	–2440
48			
49	FCS	1568	–2440
50	DR	1868	–2440
51			
52	CL2	2268	–2440
53			
54	V1R	2440	–1980
55	V2R	2440	–1804
56	V5R	2440	–1549
57	V6R	2440	–1374
58	VEE2	2440	–1199
59	X64	2440	–1024
60	X63	2440	–849
61	X62	2440	–674
62	X61	2440	–499
63	X60	2440	–324
64	X59	2440	–149
65	X58	2440	26
66	X57	2440	212
67	X56	2440	387
68	X55	2440	562
69	X54	2440	737
70	X53	2440	912
71	X52	2440	1087
72	X51	2440	1262
73	X50	2440	1437
74	X49	2440	1612
75	X48	2440	1787
76	X47	2440	1962
77	X46	2440	2137
78	X45	2440	2312
79	X44	2265	2440
80	X43	2090	2440
81	X42	1809	2440
82	X41	1634	2440
83	X40	1459	2440
84	X39	1284	2440
85	X38	1102	2440
86	X37	922	2440
87	X36	742	2440
88	X35	562	2440
89	X34	387	2440
90	X33	212	2440
91	X32	–55	2440
92	X31	–230	2440
93	X30	–405	2440
94	X29	–580	2440
95	X28	–767	2440
96	X27	–942	2440
97	X26	–1117	2440
98	X25	–1292	2440
99	X24	–1483	2440
100	X23	–1658	2440

Figure 13 HD61203D

- HD66100D



Chip size (X × Y): 4.50 mm × 4.50 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

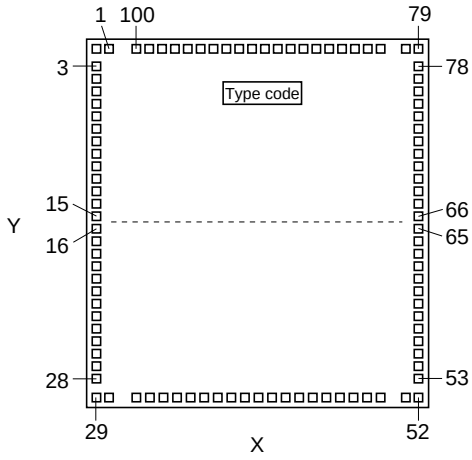
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y30	–1725	2100
2	Y29	–1925	2100
3	Y28	–2100	2060
4	Y27	–2100	1865
5	Y26	–2100	1690
6	Y25	–2100	1520
7	Y24	–2100	1360
8	Y23	–2100	1200
9	Y22	–2100	1040
10	Y21	–2100	880
11	Y20	–2100	720
12	Y19	–2100	560
13	Y18	–2100	400
14	Y17	–2100	240
15	Y16	–2100	80
16	Y15	–2100	–80
17	Y14	–2100	–240
18	Y13	–2100	–400
19	Y12	–2100	–560
20	Y11	–2100	–720
21	Y10	–2100	–880
22	Y9	–2100	–1040
23	Y8	–2100	–1200
24	Y7	–2100	–1360
25	Y6	–2100	–1520
26	Y5	–2100	–1690
27	Y4	–2100	–1865
28	Y3	–2100	–2060
29	Y2	–1925	–2100
30	Y1	–1725	–2100
31	V_{EE}	–1520	–2100
32	V1	–1360	–2100
33	V2	–1200	–2100
34	V3	–1040	–2100
35	V4	–880	–2100
36	GND	–720	–2100
37	CL1	–470	–2100
38			
39	SHL	–270	–2100
40	CL2	–70	–2100
41	DI	130	–2100
42	DO	350	–2100
43			
44	M	620	–2100
45			
46	V_{CC}	980	–2100
47			
48			
49			
50			
51	Y80	1725	–2100
52	Y79	1925	–2100
53	Y78	2100	–2060
54	Y77	2100	–1865
55	Y76	2100	–1690
56	Y75	2100	–1520
57	Y74	2100	–1360
58	Y73	2100	–1200
59	Y72	2100	–1040
60	Y71	2100	–880
61	Y70	2100	–720
62	Y69	2100	–560
63	Y68	2100	–400
64	Y67	2100	–240
65	Y66	2100	–80
66	Y65	2100	80
67	Y64	2100	240
68	Y63	2100	400
69	Y62	2100	560
70	Y61	2100	720
71	Y60	2100	880
72	Y59	2100	1040
73	Y58	2100	1200
74	Y57	2100	1360
75	Y56	2100	1520
76	Y55	2100	1690
77	Y54	2100	1865
78	Y53	2100	2060
79	Y52	1925	2100
80	Y51	1725	2100
81	Y50	1520	2100
82	Y49	1360	2100
83	Y48	1200	2100
84	Y47	1040	2100
85	Y46	880	2100
86	Y45	720	2100
87	Y44	560	2100
88	Y43	400	2100
89	Y42	240	2100
90	Y41	80	2100
91	Y40	–80	2100
92	Y39	–240	2100
93	Y38	–400	2100
94	Y37	–560	2100
95	Y36	–720	2100
96	Y35	–880	2100
97	Y34	–1040	2100
98	Y33	–1200	2100
99	Y32	–1360	2100
100	Y31	–1520	2100

Figure 14 HD66100D

Chip Shipment Products

- HD66106D



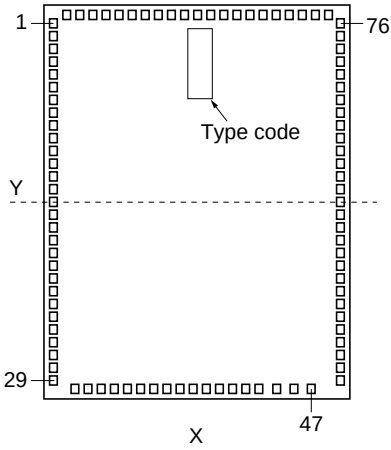
Chip size (X × Y): 4.84 mm × 5.16 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y30	–2025	2430
2	Y29	–2210	2430
3	Y28	–2270	2188
4	Y27	–2270	2013
5	Y26	–2270	1838
6	Y25	–2270	1663
7	Y24	–2270	1488
8	Y23	–2270	1313
9	Y22	–2270	1138
10	Y21	–2270	963
11	Y20	–2270	788
12	Y19	–2270	613
13	Y18	–2270	438
14	Y17	–2270	263
15	Y16	–2270	88
16	Y15	–2270	–88
17	Y14	–2270	–263
18	Y13	–2270	–438
19	Y12	–2270	–613
20	Y11	–2270	–788
21	Y10	–2270	–963
22	Y9	–2270	–1138
23	Y8	–2270	–1313
24	Y7	–2270	–1488
25	Y6	–2270	–1663
26	Y5	–2270	–1838
27	Y4	–2270	–2013
28	Y3	–2270	–2188
29	Y2	–2210	–2430
30	Y1	–2025	–2430
31	VLCD1	–1663	–2430
32	V1	–1488	–2430
33	V2	–1313	–2430
34	V3	–1138	–2430
35	V4	–963	–2430
36	VLCD2	–780	–2430
37	GND	–604	–2430
38	CL1	–428	–2430
39	SHL	–235	–2430
40	CL2	–44	–2430
41	CH1	148	–2430
42	M	341	–2430
43	D3	532	–2430
44	D2	725	–2430
45	D1	916	–2430
46	D0	1109	–2430
47	E	1300	–2430
48	CAR	1484	–2430
49	V_{CC}	1668	–2430
51	Y80	2025	–2430
52	Y79	2210	–2430
53	Y78	2270	–2188
54	Y77	2270	–2013
55	Y76	2270	–1838
56	Y75	2270	–1663
57	Y74	2270	–1488
58	Y73	2270	–1313
59	Y72	2270	–1138
60	Y71	2270	–963
61	Y70	2270	–788
62	Y69	2270	–613
63	Y68	2270	–438
64	Y67	2270	–263
65	Y66	2270	–88
66	Y65	2270	88
67	Y64	2270	263
68	Y63	2270	438
69	Y62	2270	613
70	Y61	2270	788
71	Y60	2270	963
72	Y59	2270	1138
73	Y58	2270	1313
74	Y57	2270	1488
75	Y56	2270	1663
76	Y55	2270	1838
77	Y54	2270	2013
78	Y53	2270	2188
79	Y52	2210	2430
80	Y51	2025	2430
81	Y50	1663	2430
82	Y49	1488	2430
83	Y48	1313	2430
84	Y47	1138	2430
85	Y46	963	2430
86	Y45	788	2430
87	Y44	613	2430
88	Y43	438	2430
89	Y42	263	2430
90	Y41	88	2430
91	Y40	–88	2430
92	Y39	–263	2430
93	Y38	–438	2430
94	Y37	–613	2430
95	Y36	–788	2430
96	Y35	–963	2430
97	Y34	–1138	2430
98	Y33	–1313	2430
99	Y32	–1488	2430
100	Y31	–1663	2430

Figure 15 HD66106D

- HCD66204



Chip size (X × Y): 3.80 mm × 4.60 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

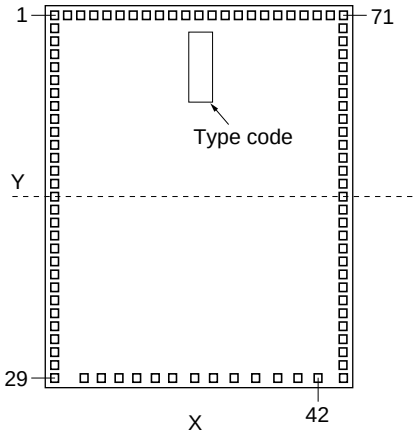
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y51	–1748	2150
2	Y52	–1750	1940
3	Y53	–1750	1770
4	Y54	–1750	1615
5	Y55	–1750	1470
6	Y56	–1750	1325
7	Y57	–1750	1180
8	Y58	–1750	1035
9	Y59	–1750	890
10	Y60	–1750	745
11	Y61	–1750	600
12	Y62	–1750	455
13	Y63	–1750	310
14	Y64	–1750	165
15	Y65	–1750	20
16	Y66	–1750	–125
17	Y67	–1750	–270
18	Y68	–1750	–415
19	Y69	–1750	–560
20	Y70	–1750	–705
21	Y71	–1750	–850
22	Y72	–1750	–995
23	Y73	–1750	–1140
24	Y74	–1750	–1285
25	Y75	–1750	–1430
26	Y76	–1750	–1575
27	Y77	–1750	–1720
28	Y78	–1750	–1865
29	Y79	–1750	–2110
30	Y80	–1610	–2150
31	E	–1434	–2150
32	V1	–1232	–2150
33	V3	–1092	–2150
34	V4	–952	–2150
35	V_{EE}	–812	–2150
36	M	–652	–2150
37	CL1	–438	–2150
38	GND	–250	–2150
39	DISPOFF	–82	–2150
40	V_{CC}	98	–2150
41	SHL	278	–2150
42	D3	426	–2150
43	D2	640	–2150
44	D1	788	–2150
45	D0	1002	–2150
46	CL2	1150	–2150
47	CAR	1458	–2150
48	Y1	1750	–2150
49	Y2	1750	–1930
50	Y3	1750	–1760
51	Y4	1750	–1605
52	Y5	1750	–1460
53	Y6	1750	–1315
54	Y7	1750	–1170
55	Y8	1750	–1025
56	Y9	1750	–860
57	Y10	1750	–715
58	Y11	1750	–570
59	Y12	1750	–425
60	Y13	1750	–280
61	Y14	1750	–135
62	Y15	1750	10
63	Y16	1750	155
64	Y17	1750	300
65	Y18	1750	445
66	Y19	1750	590
67	Y20	1750	735
68	Y21	1750	880
69	Y22	1750	1025
70	Y23	1750	1170
71	Y24	1750	1315
72	Y25	1750	1460
73	Y26	1750	1605
74	Y27	1750	1750
75	Y28	1750	1900
76	Y29	1750	2120
77	Y30	1610	2150
78	Y31	1432	2150
79	Y32	1273	2150
80	Y33	1114	2150
81	Y34	955	2150
82	Y35	796	2150
83	Y36	637	2150
84	Y37	478	2150
85	Y38	319	2150
86	Y39	160	2150
87	Y40	1	2150
88	Y41	–158	2150
89	Y42	–317	2150
90	Y43	–476	2150
91	Y44	–635	2150
92	Y45	–794	2150
93	Y46	–953	2150
94	Y47	–1112	2150
95	Y48	–1271	2150
96	Y49	–1430	2150
97	Y50	–1589	2150

Figure 16 HCD66204

Chip Shipment Products

- HCD66205



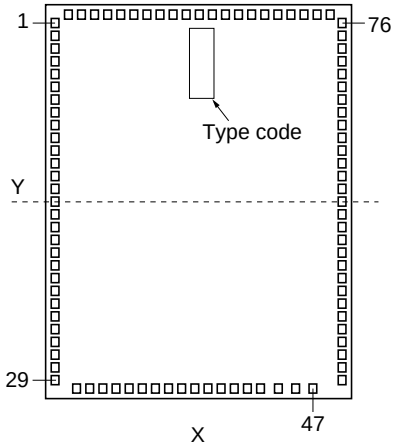
Chip size (X × Y): 3.80 mm × 4.60 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	X51	–1748	2150
2	X52	–1750	1940
3	X53	–1750	1770
4	X54	–1750	1615
5	X55	–1750	1470
6	X56	–1750	1325
7	X57	–1750	1180
8	X58	–1750	1035
9	X59	–1750	890
10	X60	–1750	745
11	X61	–1750	600
12	X62	–1750	455
13	X63	–1750	310
14	X64	–1750	165
15	X65	–1750	20
16	X66	–1750	–125
17	X67	–1750	–270
18	X68	–1750	–415
19	X69	–1750	–560
20	X70	–1750	–705
21	X71	–1750	–850
22	X72	–1750	–995
23	X73	–1750	–1140
24	X74	–1750	–1285
25	X75	–1750	–1430
26	X76	–1750	–1575
27	X77	–1750	–1720
28	X78	–1750	–1865
29	X79	–1750	–2110
30	X80	–1610	–2150
31	D0	–1294	–2150
32	V_{EE}	–1042	–2150
33	V5	–842	–2150
34	V6	–644	–2150
35	V1	–444	–2150
36	DISPOFF	–222	–2150
37	V_{CC}	–16	–2150
38	SHL	206	–2150
39	GND	474	–2150
40	M	746	–2150
41	CL	1010	–2150
42	D1	1274	–2150
43	X1	1750	–2150
44	X2	1750	–1930
45	X3	1750	–1760
46	X4	1750	–1605
47	X5	1750	–1460
48	X6	1750	–1315
49	X7	1750	–1170
50	X8	1750	–1025
51	X9	1750	–860
52	X10	1750	–715
53	X11	1750	–570
54	X12	1750	–425
55	X13	1750	–280
56	X14	1750	–135
57	X15	1750	10
58	X16	1750	155
59	X17	1750	300
60	X18	1750	445
61	X19	1750	590
62	X20	1750	735
63	X21	1750	880
64	X22	1750	1025
65	X23	1750	1170
66	X24	1750	1315
67	X25	1750	1460
68	X26	1750	1605
69	X27	1750	1750
70	X28	1750	1900
71	X29	1750	2120
72	X30	1610	2150
73	X31	1432	2150
74	X32	1273	2150
75	X33	1114	2150
76	X34	955	2150
77	X35	796	2150
78	X36	637	2150
79	X37	478	2150
80	X38	319	2150
81	X39	160	2150
82	X40	1	2150
83	X41	–158	2150
84	X42	–317	2150
85	X43	–476	2150
86	X44	–635	2150
87	X45	–794	2150
88	X46	–953	2150
89	X47	–1112	2150
90	X48	–1271	2150
91	X49	–1430	2150
92	X50	–1589	2150

Figure 17 HCD66205

- HCD66204L



Chip size (X × Y): 3.80 mm × 4.60 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

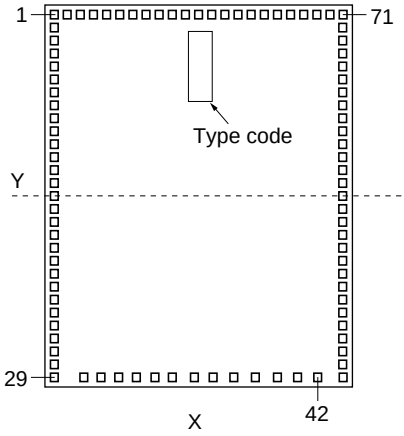
(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	Y51	–1748	2150
2	Y52	–1750	1940
3	Y53	–1750	1770
4	Y54	–1750	1615
5	Y55	–1750	1470
6	Y56	–1750	1325
7	Y57	–1750	1180
8	Y58	–1750	1035
9	Y59	–1750	890
10	Y60	–1750	745
11	Y61	–1750	600
12	Y62	–1750	455
13	Y63	–1750	310
14	Y64	–1750	165
15	Y65	–1750	20
16	Y66	–1750	–125
17	Y67	–1750	–270
18	Y68	–1750	–415
19	Y69	–1750	–560
20	Y70	–1750	–705
21	Y71	–1750	–850
22	Y72	–1750	–995
23	Y73	–1750	–1140
24	Y74	–1750	–1285
25	Y75	–1750	–1430
26	Y76	–1750	–1575
27	Y77	–1750	–1720
28	Y78	–1750	–1865
29	Y79	–1750	–2110
30	Y80	–1610	–2150
31	E	–1434	–2150
32	V1	–1232	–2150
33	V3	–1092	–2150
34	V4	–952	–2150
35	V_{EE}	–812	–2150
36	M	–652	–2150
37	CL1	–438	–2150
38	GND	–250	–2150
39	DISPOFF	–82	–2150
40	V_{CC}	98	–2150
41	SHL	278	–2150
42	D3	426	–2150
43	D2	640	–2150
44	D1	788	–2150
45	D0	1002	–2150
46	CL2	1150	–2150
47	CAR	1458	–2150
48	Y1	1750	–2150
49	Y2	1750	–1930
50	Y3	1750	–1760
51	Y4	1750	–1605
52	Y5	1750	–1460
53	Y6	1750	–1315
54	Y7	1750	–1170
55	Y8	1750	–1025
56	Y9	1750	–860
57	Y10	1750	–715
58	Y11	1750	–570
59	Y12	1750	–425
60	Y13	1750	–280
61	Y14	1750	–135
62	Y15	1750	10
63	Y16	1750	155
64	Y17	1750	300
65	Y18	1750	445
66	Y19	1750	590
67	Y20	1750	735
68	Y21	1750	880
69	Y22	1750	1025
70	Y23	1750	1170
71	Y24	1750	1315
72	Y25	1750	1460
73	Y26	1750	1605
74	Y27	1750	1750
75	Y28	1750	1900
76	Y29	1750	2120
77	Y30	1610	2150
78	Y31	1432	2150
79	Y32	1273	2150
80	Y33	1114	2150
81	Y34	955	2150
82	Y35	796	2150
83	Y36	637	2150
84	Y37	478	2150
85	Y38	319	2150
86	Y39	160	2150
87	Y40	1	2150
88	Y41	–158	2150
89	Y42	–317	2150
90	Y43	–476	2150
91	Y44	–635	2150
92	Y45	–794	2150
93	Y46	–953	2150
94	Y47	–1112	2150
95	Y48	–1271	2150
96	Y49	–1430	2150
97	Y50	–1589	2150

Figure 18 HCD66204L

Chip Shipment Products

- HCD66205L



Chip size (X × Y): 3.80 mm × 4.60 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 µm × 100 µm

(Unit: µm)

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	X51	–1748	2150
2	X52	–1750	1940
3	X53	–1750	1770
4	X54	–1750	1615
5	X55	–1750	1470
6	X56	–1750	1325
7	X57	–1750	1180
8	X58	–1750	1035
9	X59	–1750	890
10	X60	–1750	745
11	X61	–1750	600
12	X62	–1750	455
13	X63	–1750	310
14	X64	–1750	165
15	X65	–1750	20
16	X66	–1750	–125
17	X67	–1750	–270
18	X68	–1750	–415
19	X69	–1750	–560
20	X70	–1750	–705
21	X71	–1750	–850
22	X72	–1750	–995
23	X73	–1750	–1140
24	X74	–1750	–1285
25	X75	–1750	–1430
26	X76	–1750	–1575
27	X77	–1750	–1720
28	X78	–1750	–1865
29	X79	–1750	–2110
30	X80	–1610	–2150
31	D0	–1294	–2150
32	V_{EE}	–1042	–2150
33	V5	–842	–2150
34	V6	–644	–2150
35	V1	–444	–2150
36	DISPOFF	–222	–2150
37	V_{CC}	–16	–2150
38	SHL	206	–2150
39	GND	474	–2150
40	M	746	–2150
41	CL	1010	–2150
42	D1	1274	–2150
43	X1	1750	–2150
44	X2	1750	–1930
45	X3	1750	–1760
46	X4	1750	–1605
47	X5	1750	–1460
48	X6	1750	–1315
49	X7	1750	–1170
50	X8	1750	–1025
51	X9	1750	–860
52	X10	1750	–715
53	X11	1750	–570
54	X12	1750	–425
55	X13	1750	–280
56	X14	1750	–135
57	X15	1750	10
58	X16	1750	155
59	X17	1750	300
60	X18	1750	445
61	X19	1750	590
62	X20	1750	735
63	X21	1750	880
64	X22	1750	1025
65	X23	1750	1170
66	X24	1750	1315
67	X25	1750	1460
68	X26	1750	1605
69	X27	1750	1750
70	X28	1750	1900
71	X29	1750	2120
72	X30	1610	2150
73	X31	1432	2150
74	X32	1273	2150
75	X33	1114	2150
76	X34	955	2150
77	X35	796	2150
78	X36	637	2150
79	X37	478	2150
80	X38	319	2150
81	X39	160	2150
82	X40	1	2150
83	X41	–158	2150
84	X42	–317	2150
85	X43	–476	2150
86	X44	–635	2150
87	X45	–794	2150
88	X46	–953	2150
89	X47	–1112	2150
90	X48	–1271	2150
91	X49	–1430	2150
92	X50	–1589	2150

Figure 19 HCD66205L

1. Views on Quality and Reliability

Hitachi's basic quality aims are to meet individual user's purchase purpose and quality required, and to be at a satisfactory quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, Hitachi tries to assure reliability so that semiconductor devices delivered can perform their function in actual operating circumstances. To realize this quality in the manufacturing process, the key points should be to establish a quality control system in the process and to enhance the quality ethic.

In addition, quality required by users of semiconductor devices is going toward higher levels as performance of electronic system in the market is increasing and expanding in size and application fields. To cover the situation, Hitachi is performing the following:

1. Building in reliability in design at the stage of new product development.
2. Building in quality at the sources of the manufacturing process.
3. Executing stricter inspection and reliability confirmation of final products.
4. Making quality levels higher with field data feedback.
5. Cooperating with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet users' requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

The reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability targets with failure rates under certain common test conditions. The reliability target is determined corresponding to the character of equipment taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering the operating circumstances of equipment the semiconductor device is used in, reliability target of the system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

2.2.1 Design Standardization

Establishment of design rules, and standardization of parts, material and process are necessary. To establish design rules, critical quality and reliability items are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in newly developed devices, except in cases where special functions are needed.

2.2.2 Device Design

It is important in device design to consider the total balance of process design, structure design, circuit and layout design. Especially when new processes and new materials are employed, careful technical study is executed prior to device development.

2.2.3 Reliability Evaluation by Test Site

Test site is sometimes called test pattern. It is a useful method for design and process reliability evaluation of ICs and LSIs which have complicated functions.

Purposes of test site are:

- Marking fundamental failure mode clear
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing

Evaluation by test site is effective because:

- Common fundamental failure mode and failure mechanism in devices can be evaluated.
- Factors dominating failure mode can be picked up, and comparison can be made with processes that have been experienced in field.
- Relation between failure causes and manufacturing factors can be analyzed.
- Easy to run tests.
- Etc.

2.3 Design Review

Design review is an organized method to confirm that a design satisfies the required performance (including users') and that design work follows the specified methods, and whether or not improved technical items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of the competitive power of products, the major purpose of the design review is to ensure quality and reliability of the products. In Hitachi, design reviews are preformed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows:

1. Description of the products based on specified design documents.
2. From the standpoint of the specialties of individual participants, design documents are studied, and if unclear matter is found, calculation, experiments, investigation, etc. will be carried out.
3. Determine contents of reliability and methods, etc. based on design documents and drawings.
4. Check process ability of manufacturing line to achieve design goal.
5. Discussion about preparation for production.
6. Planning and execution of subprograms for design changes proposed by individual specialists, and for tests, experiments and calculation to confirm the design changes.
7. Reference of past failure experiences with similar devices, confirmation of methods to prevent them, and planning and execution of test programs for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are:

1. Problems in an individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
2. Feedback of information should be used to ensure satisfactory level of process capability.
3. To assure required reliability as a result of the items mentioned above is the purpose of quality assurance.

The following discusses device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure required quality and reliability, quality approval is carried out at the trial production stage of device design and the mass production stage based on reliability design as described in section 2.

Hitachi's views on quality approval are:

1. A third party must perform approval objectively from the standpoint of customers.
2. Fully consider past failure experiences and information from the field.
3. Approval is needed for design change or work change.
4. Intensive approval is executed on parts material and process.
5. Study process capability and variation factor, and set up control points at mass production stage.

Considering the views mentioned above, figure 1 shows how quality approval is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control execution is divided organically by function between manufacturing

department and quality assurance department, and other related departments. The total function flow is shown in figure 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices improve, the importance of quality control of material and parts (crystal, lead frame, fine wire for wire bonding, package) to build products, and materials needed in manufacturing process (mask pattern and chemicals) increases. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is also key in quality control of parts and materials. The incoming inspection is performed based on an incoming inspection specification, following purchase specification and drawings, and sampling inspection is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

1. Outside vendor technical information meeting
2. Approval on outside vendors, and guidance of outside vendors
3. Physical chemical analysis and test

The typical check points of parts and materials are shown in table 1.

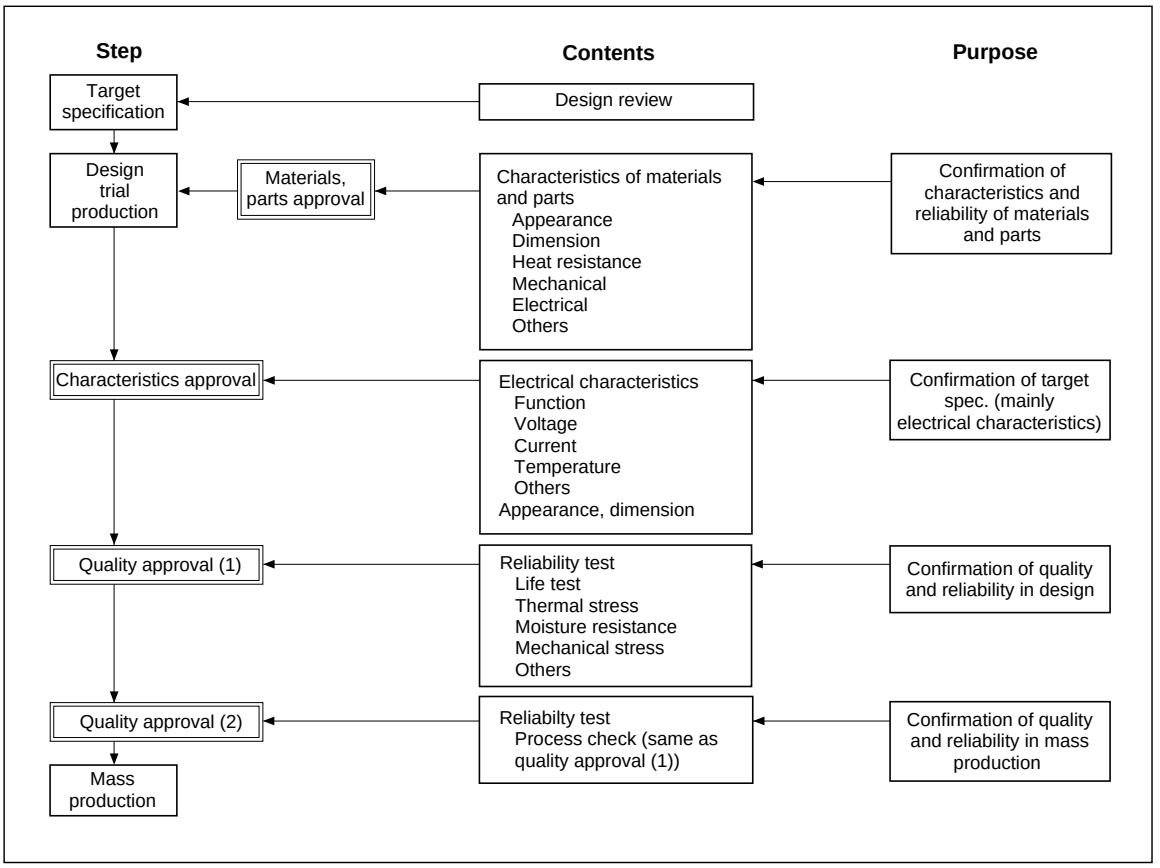


Figure 1 Quality Approval Flowchart

3.3.2 Inner Process Quality Control

Inner process quality control performs a very important function in quality assurance of a semiconductor devices. The following is a description of control of semifinal products, final products, manufacturing facilities, measuring equipments, circumstances and submaterials. The quality control in the manufacturing process is shown in figure 3 corresponding to the manufacturing process.

1. Quality control of semifinal products and final production products

   Potential failure factors of semiconductor devices should be removed in manufacturing process. To achieve this, check points are setup in each process, and products that have potential failure factors are not transferred to the next

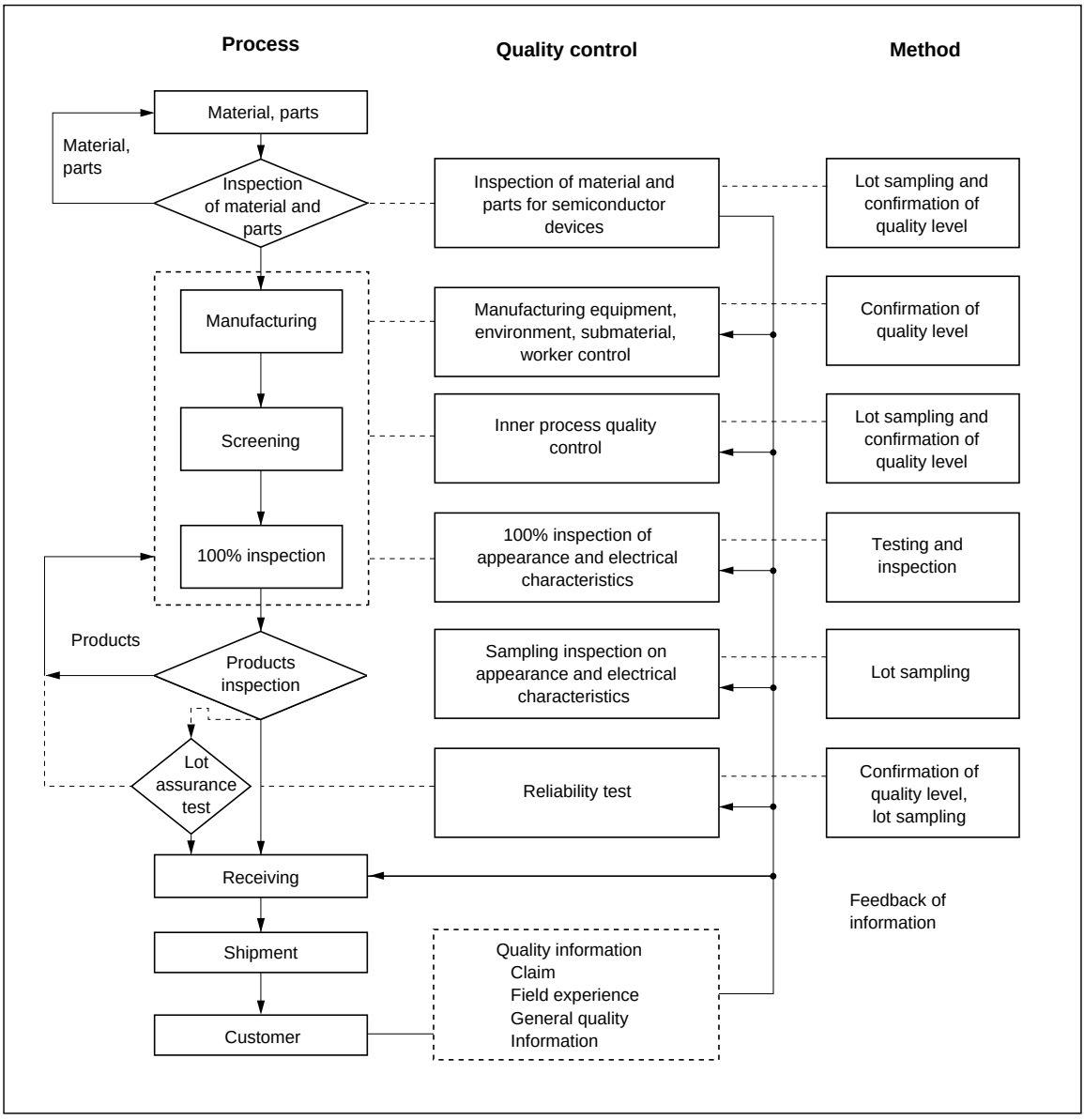


Figure 2 Flowchart of Quality Control in Manufacturing Process

process. For high reliability semiconductor devices, especially manufacturing line is carefully selected, and the quality control in the manufacturing process is tightly executed: Strict check on each process and each lot, 100% inspection to remove failure factor caused by manufacturing variation, and necessary screening, such as high temperature aging and temperature cycling. Contents of inner process quality control are:

- Condition control on individual equipment and workers, and sampling check of semifinal products
- Proposal and carrying-out of work improvement
- Education of workers
- Maintenance and improvement of yield
- Detection of quality problems, and execution of countermeasures
- Transmission of information about quality

2. Quality control of manufacturing facilities and measuring equipment

   Equipment for manufacturing semiconductor devices have been developing extraordinarily, with required high performance devices and production improvements. They are important factors to determine quality and reliability. In Hitachi, automation of manufacturing equipment is promoted to improve manufacturing variation, and controls maintain proper operation and function of high performance equipment. Maintenance inspection for quality control is performed daily based on related specifications, and also periodical inspections. At the inspection, inspection points listed in the specification are checked one by one to avoid any omissions. During adjustment and maintenance of measuring equipment, maintenance number and specifications are checked one by one to maintain and improve quality.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Points to Check
Wafer	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratch
	Dimension	Dimension level
	Registration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratch, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratch
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratch
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

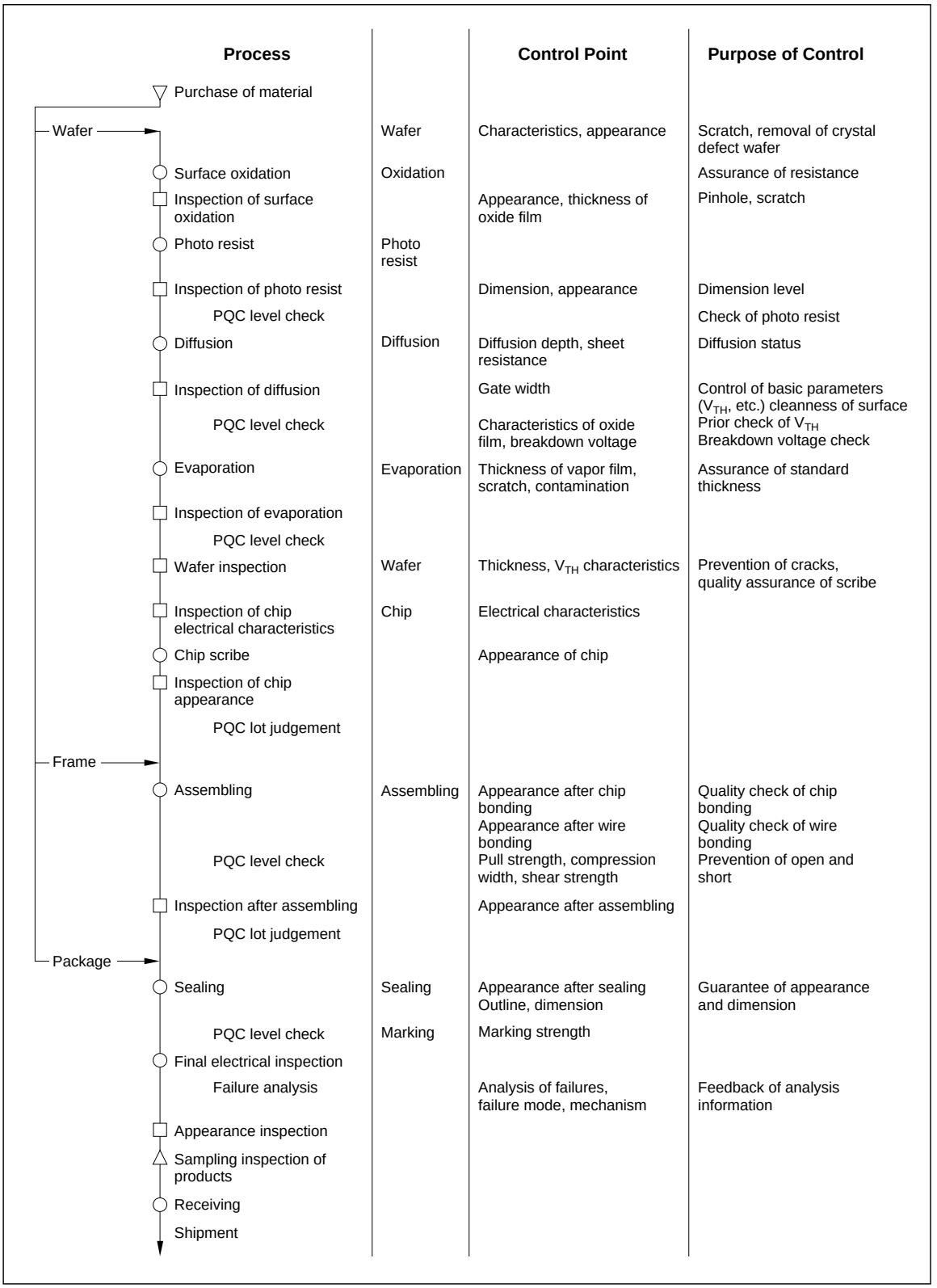


Figure 3 Example of Inner Process Quality Control

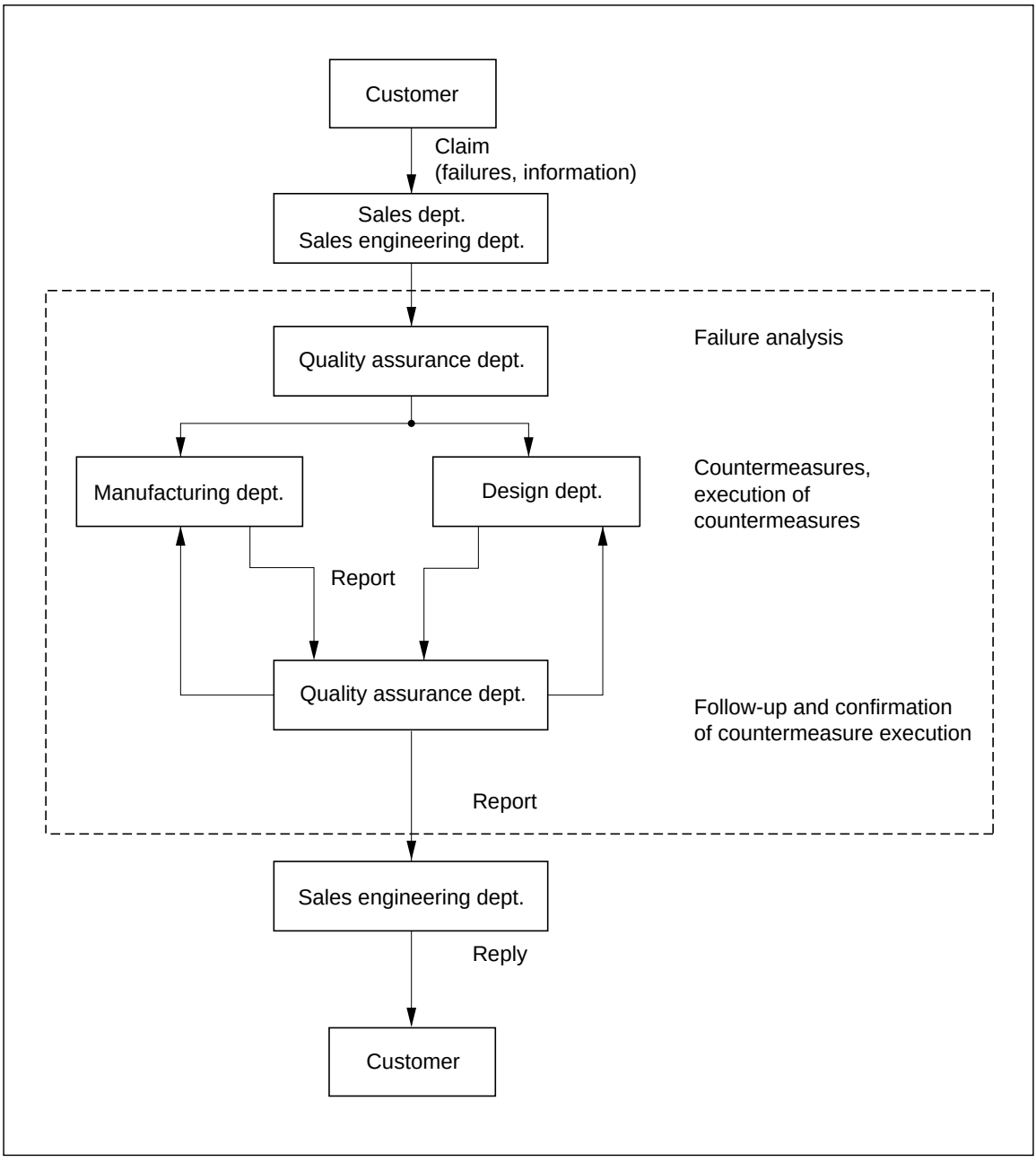


Figure 4 Process Flowchart of Field Failure

Reliability Test Data of LCD Drivers

1. Introduction

The use of liquid crystal displays with micro-computer application systems has been increasing, because of their low power consumption, freedom in display pattern design, and thin shape. Low power consumption and high density packaging have been achieved through the use of the CMOS process and the flat plastic packages, respectively.

This chapter describes reliability and quality assurance data for Hitachi LCD driver LSIs based on test data and failure analysis results.

2. Chip and Package Structure

The Hitachi LCD driver LSI family uses low power CMOS technology and flat plastic package. The Si-gate process is used for high reliability and high density. Chip structure and basic circuit are shown in figure 1, and package structure is shown in figure 2.

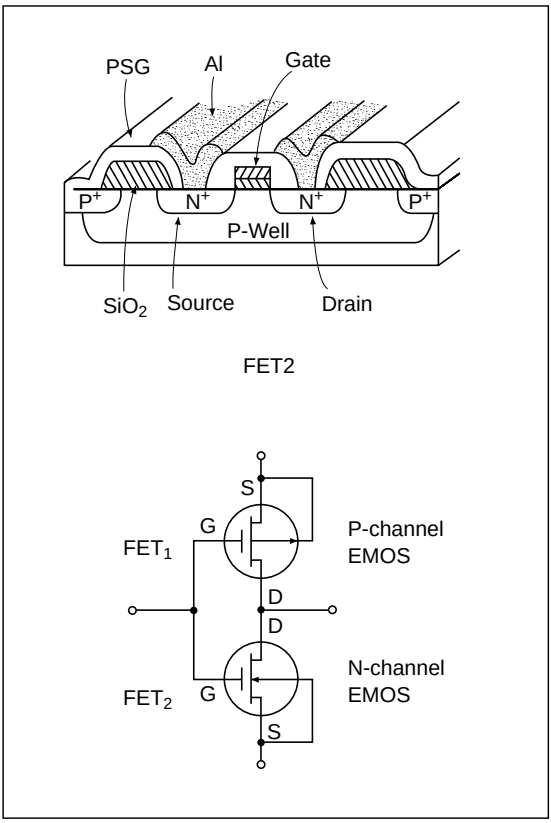


Figure 1 Chip Structure and Basic Circuit

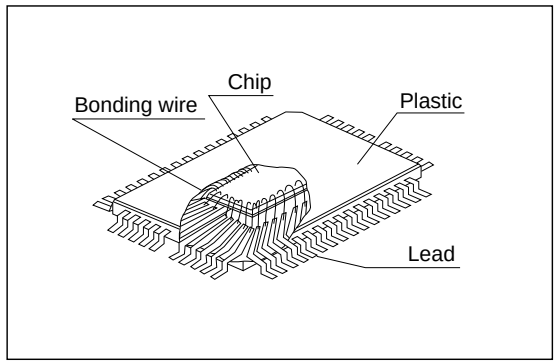


Figure 2 Package Structure

3. Reliability Test Results

The test results of LCD driver LSI family are shown in tables 1, 2, and 3.

Table 1 Test Result 1, High Temperature Operation (T_a = 125°C, V_{CC} = 5.5 V)

Device	Sample Size	Component Hour	Failure
HD44100H	40	40,000	0
HD44102H	40	40,000	0
HD44103H	40	40,000	0
HD44780U	90	90,000	0
HD66100F	45	45,000	0
HD61100A	80	80,000	0
HD61102	50	50,000	0
HD61103A	50	50,000	0
HD61200	40	40,000	0
HD61202	50	50,000	0
HD61203	40	40,000	0
HD61830	40	40,000	0
HD61830B	40	40,000	0
HD63645	32	32,000	0
HD64645	32	32,000	0
HD61602	38	38,000	0
HD61603	32	32,000	0
HD61604	32	32,000	0
HD61605	32	32,000	0
HD66840	45	45,000	0

Table 2 Test Result 2

Test Item	Test Condition	Sample Size	Component Hour	Failure
High temp, storage	T_a = 150°C, 1000 h	180	180,000	0
Low temp, storage	T_a = –55°C, 1000 h	140	140,000	0
Steady state humidity	65°C, 95% RH, 1000 h	860	860,000	1*
Steady state humidity, biased	85°C, 90% RH, 1000 h	165	170,000	2*
Pressure cooker	121°C, 2 atm. 100 h	200	20,000	0

Note: * Aluminum corrosion

Table 3 Test Results 3

Test Items	Test Condition	Sample Size	Failure
Thermal shock	0 to 100°C 10 cycles	108	0
Temperature cycling	–55°C to 150°C 10 cycles	678	0
Soldering heat	260°C, 10 seconds	283	0
Resistance to VPS	215°C, 30 seconds	88	0
Solderability	230°C, 5 seconds	140	0

4. Quality Data from Field Use

Field failure rate is estimated in advance through production process evaluation and reliability tests. Past field data on similar devices provides the basis for this estimation. Quality information from the users is indispensable to the improvement of product quality. Therefore, field data on products delivered to the users is followed up carefully. On the basis of information furnished by the user, failure analysis is conducted and the results are quickly fed back to the design and production divisions.

Failure analysis results on MOS LSIs returned to Hitachi is shown in figure 3.

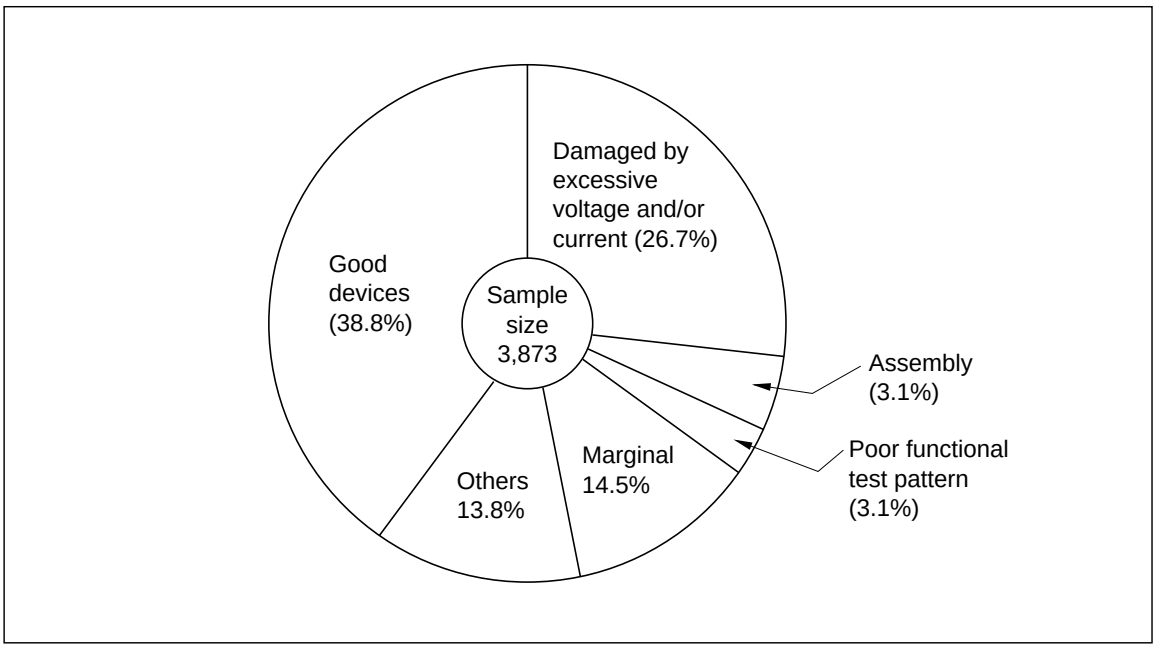


Figure 3 Failure Analysis Result

5. Precautions

5.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent deterioration in their electrical characteristics, solderability, and appearance, or breakage.

1. Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.
2. Store in a clean air environment, free from dust and reactive gas.
3. Store in a container that does not induce static electricity.
4. Store without any physical load.
5. If semiconductor devices are stored for a long time, store them in unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.
6. If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at –30°C or lower. Unpackaged devices must not be stored for over 3 months.
7. Take care not to allow condensation during storage due to rapid temperature changes.

5.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be taken, too:

1. Use containers or jugs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.
2. Prevent device breakage from clothes-induced static electricity.
3. When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a conveyor belt is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.
4. When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

5.3 Handling for Measurement

Avoid static electricity, noise, and surge voltage when measuring semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open providing the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, conveyor belt, etc. The device will fail if it touches something that leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units, etc. to leak current through their terminals or housings.

Especially, while testing the devices, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source. During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that there is no soldering bridge or foreign matter before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further

Flat Plastic Package (QFP) Mounting Methods

Surface Mounting Package Handling Precautions

1. Package Temperature Distribution

The most common method used for mounting a surface mounting device is infrared reflow. Since the package is made of a black epoxy resin, the portion of the package directly exposed to the infrared heat source will absorb heat faster and thus rise in temperature more quickly than other parts of the package unless precautions are taken. As shown in the example in figure 1, the surface directly facing the infrared heat source is 20° to 30°C higher than the leads being soldered and 40° to 50°C higher than the bottom of the package. If soldering is performed under these conditions, package cracks may occur.

To avoid this type of problem, it is recommended that an aluminum infrared heat shield be placed over the resin surface of the package. By using a 2-mm thick aluminum heat shield, the top and bottom surfaces of the resin can be held to 175°C when the peak temperature of the leads is 240°C.

2. Package Moisture Absorption

The epoxy resin used in plastic packages will absorb moisture if stored in a high-humidity environment. If this moisture absorption becomes excessive, there will be sudden vaporization during soldering, causing the interface of the resin and lead frame to spread apart. In extreme cases, package cracks will occur. Therefore, especially for thin packages, it is important that moisture-proof storage be used.

To remove any moisture absorbed during transportation, storage, or handling, it is recommended that the package be baked at 125°C for 16 to 24 hours before soldering.

3. Heating and Cooling

One method of soldering electrical parts is the solder dip method, but compared to the reflow method, the rate of heat transmission is an order of magnitude higher. When this method is used with plastic items, there is thermal shock resulting in package cracks and a deterioration of moisture-resistant characteristics. Thus, it is recommended that the solder dip method not be used.

Even with the reflow method, an excessive rate of heating or cooling is undesirable. A rate in temperature change of less than 4°C/sec is recommended.

4. Package Contaminants

It is recommended that a resin-based flux be used during soldering. Acid-based fluxes have a tendency of leaving an acid residue which adversely affects product reliability. Thus, acid-based fluxes should not be used.

With resin-based fluxes as well, if a residue is left behind, the leads and other package parts will begin to corrode. Thus, the flux must be thoroughly washed away. If cleansing solvents used to wash away the flux are left on the package for an extended period of time, package markings may fade, so care must be taken.

The precautions mentioned above are general points to be observed for reflow. However, specific reflow conditions will depend on such factors as the package shape, printed circuit board type, reflow method, and device type. For reference purposes, an example of reflow conditions for a QFP infrared reflow furnace is given in figure 2. The values given in the figure refer to the temperature of the package resin, but the leads must also be limited to a maximum of 260°C for 10 seconds or less.

Of the reflow methods, infrared reflow is the most common. In addition, there is also the paper phase reflow method. The recommended conditions for a paper phase reflow furnace are given in figure 3.

For details on surface mounting small thin packages, please consult the separate manual available on mounting. If there are any additional

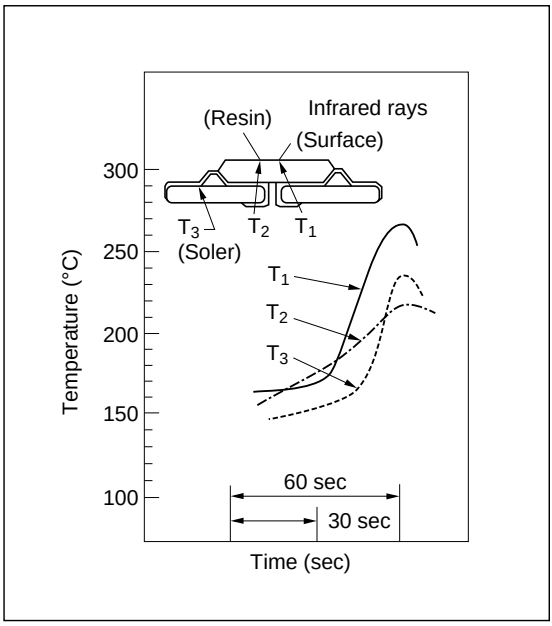


Figure 1 Temperature Profile During Infrared Heat Soldering (Example)

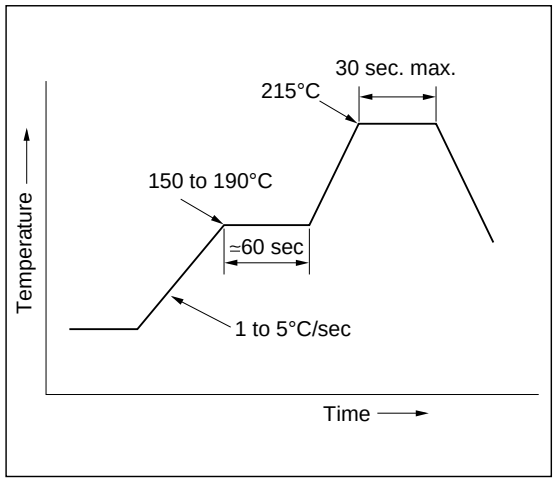


Figure 3 Example Vapor-Phase Reflow Conditions

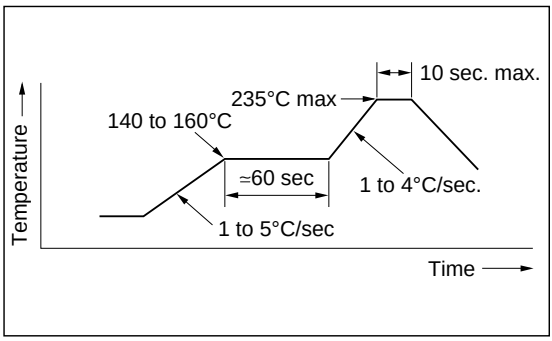


Figure 2 Recommended Reflow Conditions for QFP

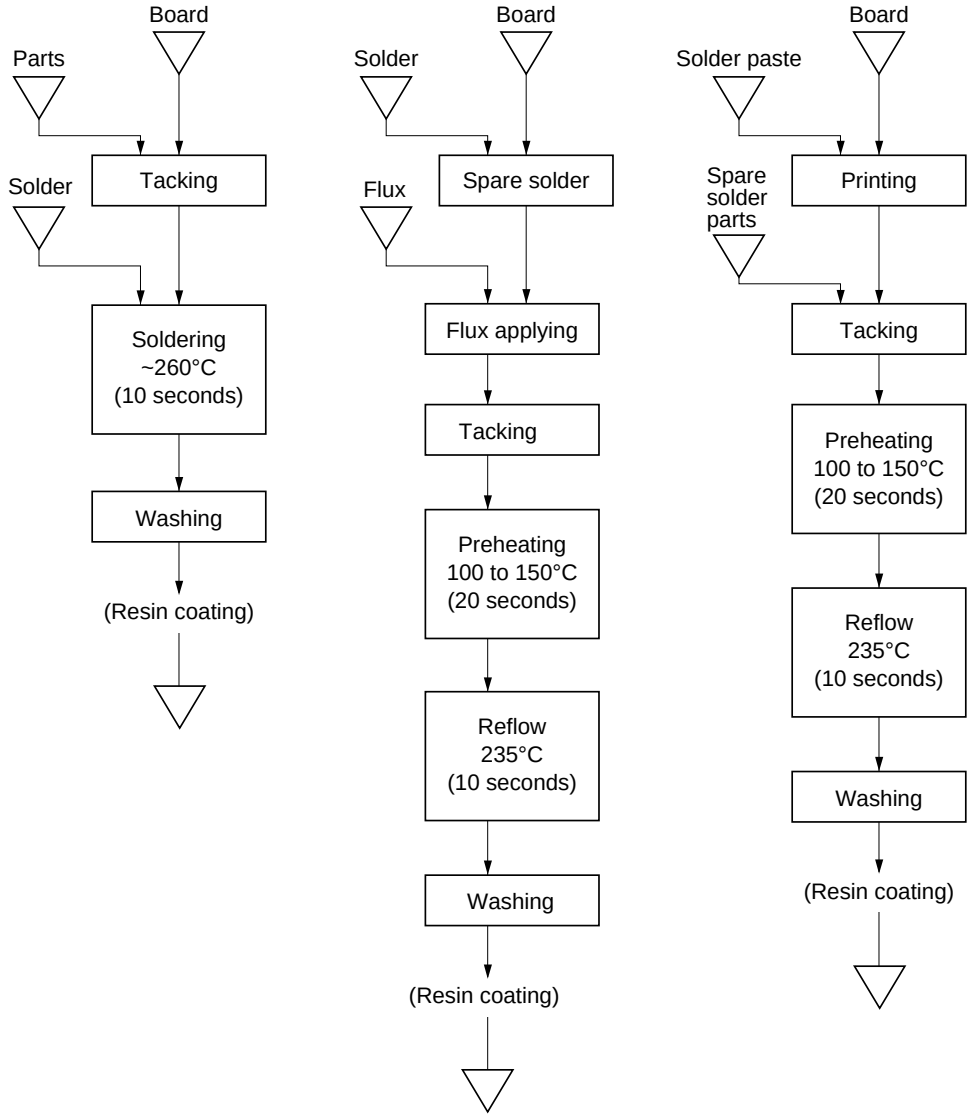


Figure 4 Recommended Paper Phase Reflow Conditions

Liquid Crystal Driving Methods

Driving a liquid crystal at direct current triggers an electrode reaction inside the liquid cell, degrading display quality rapidly. The liquid crystal must be driven by alternating current. The AC driving method includes the static driving method and the multiplex driving method, each of which has features for different applications. Hitachi has developed different LCD driver devices corresponding to the static driving method and the multiplex driving method. The following sections describe the features of each driving method, the driving waveforms, and how to apply bias.

1. Static Driving Method

Figure 1 shows the driving waveforms of the static driving method and an example in which "4" is displayed by the segment method. The static driving method is the most basic method by which good display quality can be obtained. However, it is not suitable for liquid displays with many segments because one liquid crystal driver circuit is required per segment.

The static driving method uses the frame frequency ($1/t_f$) of several tens to several hundreds Hz.

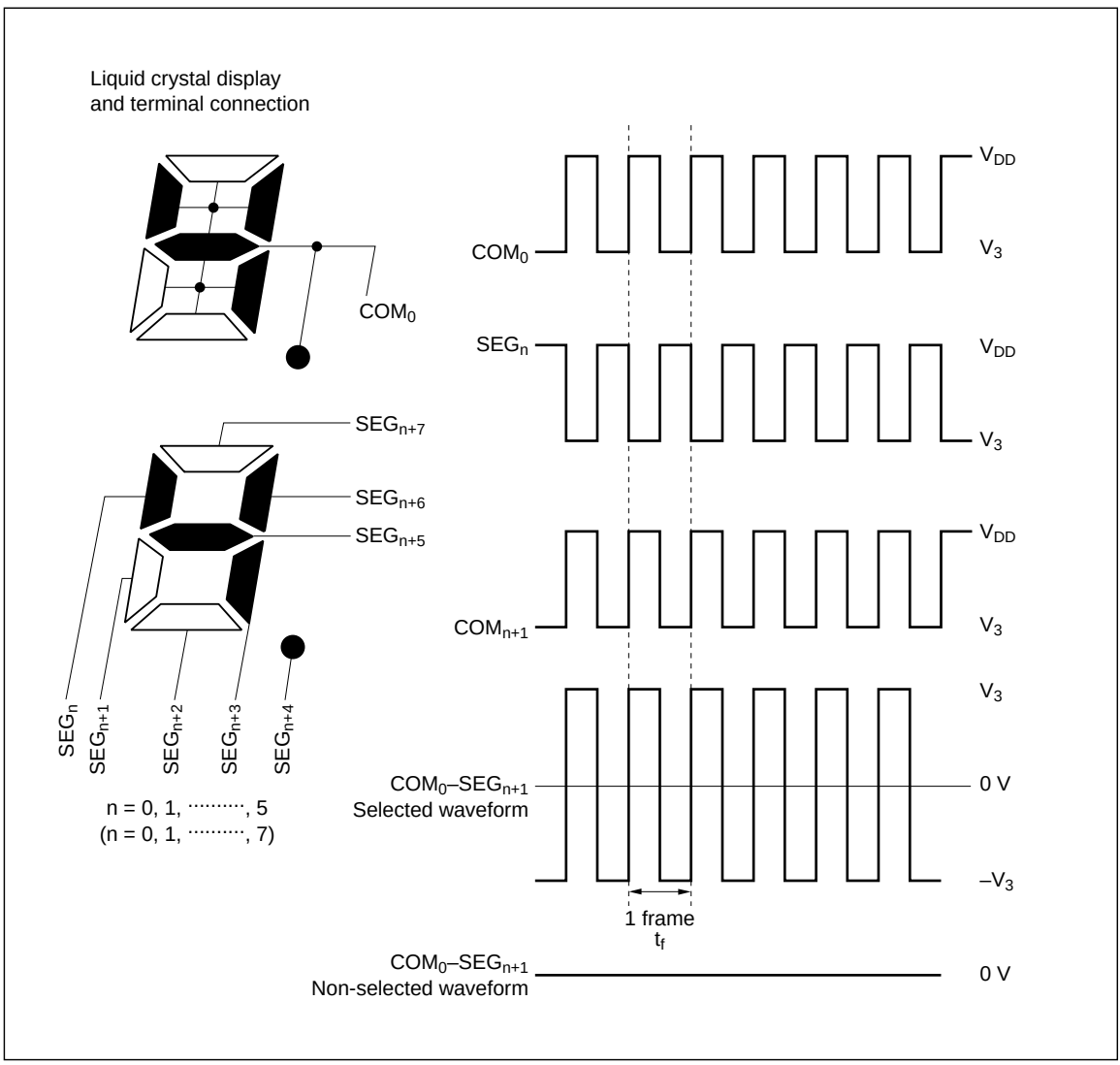


Figure 1 Example of Static Drive Waveforms (Example of HD61602/HD61603)

2. Multiplex Driving Method

The multiplex driving method is effective in reducing the number of driver circuits, the number of connections between the circuit and the display cell, and the cost when driving many display picture elements. Figure 2 shows a comparison of the static drive with the multiplex drive (1/3 duty cycle) in an 8-digit numeric display. The number of liquid crystal driver circuits required is 65 for the former and 27 for the latter. The multiplex drive reduces the number of driver circuits. However, greater multiplexing reduces the driving voltage tolerance. Thus, there are limits to the extent of multiplexing.

There are two types of multiplex drive waveforms: A type and B type. A type, shown in figure 3, is used for alternation in 1 frame. B type is used for alternation in between 2 frames (figure 4). B type has better display quality than A type in high multiplex drive.

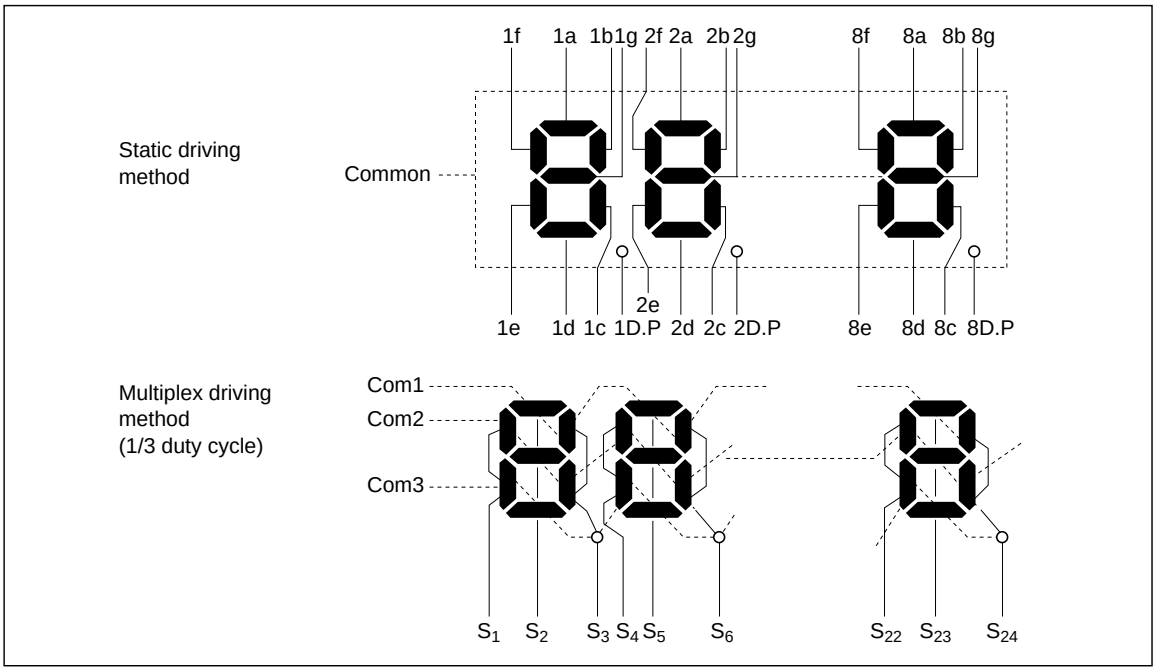


Figure 2 Example of Comparison of Static Drive with Multiples Drive

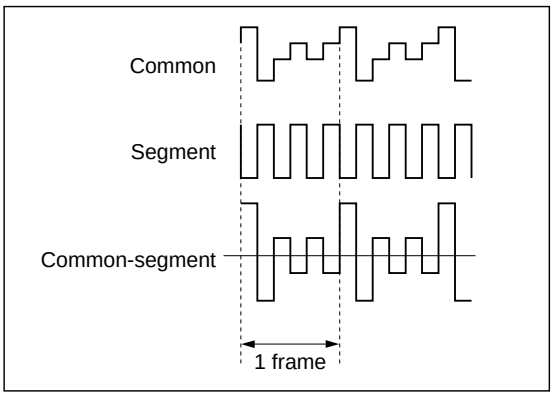


Figure 3 A Type Waveforms (1/3 Duty Cycle, 1/3 Bias)

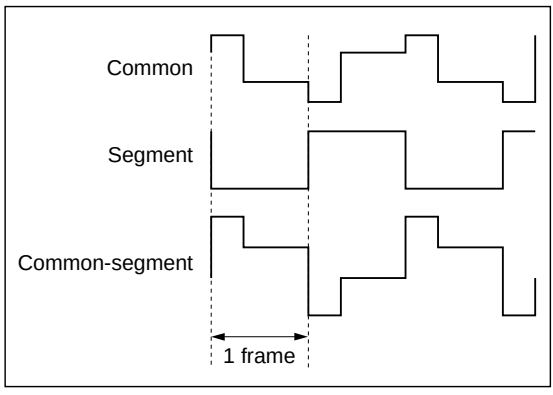


Figure 4 B Type Waveforms (1/3 Duty Cycle, 1/3 Bias)

2.1 1/2 Bias, 1/2 Duty Drive

In the 1/2 duty drive method, 1 driver circuit drives 2 segments. Figure 5 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

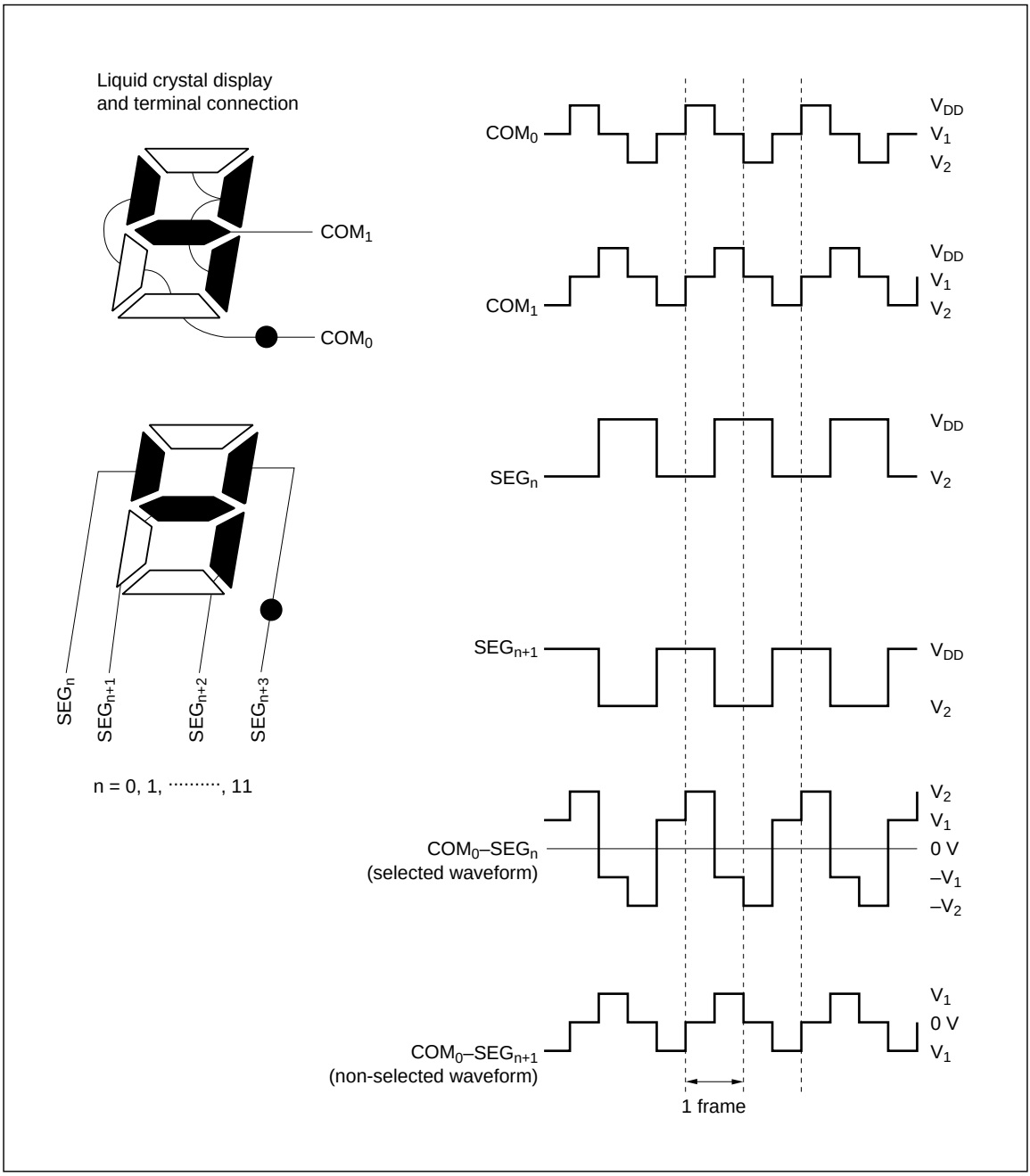


Figure 5 Example of Waveforms in 1/2 Duty Cycle Drive (B Type) (Example of HD61602)

2.2 1/3 Bias, 1/3 Duty Cycle Drive

In the 1/3 duty cycle drive, 3 segments are driven by 1 segment output driver. Figure 6 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

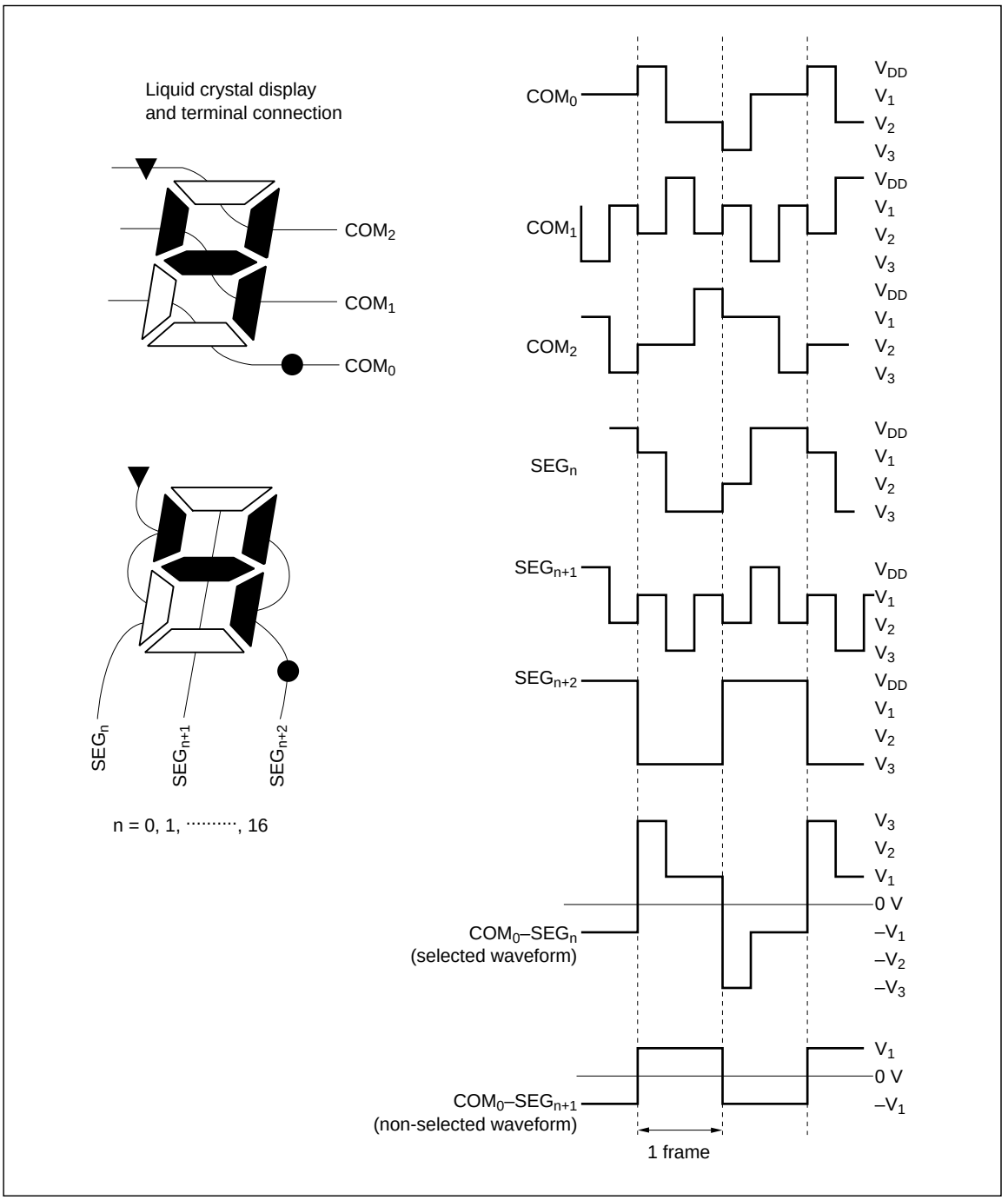


Figure 6 Example of Waveforms in 1/3 Duty Cycle Drive (B Type) (Example of HD61602)

2.3 1/3 Bias, 1/4 Duty Cycle Drive

In the 1/4 duty cycle drive, 4 segments are driven by 1 segment output driver. Figure 7 shows an example of the connection to display '4' on a liquid crystal display of 7-segment type, and the output waveforms.

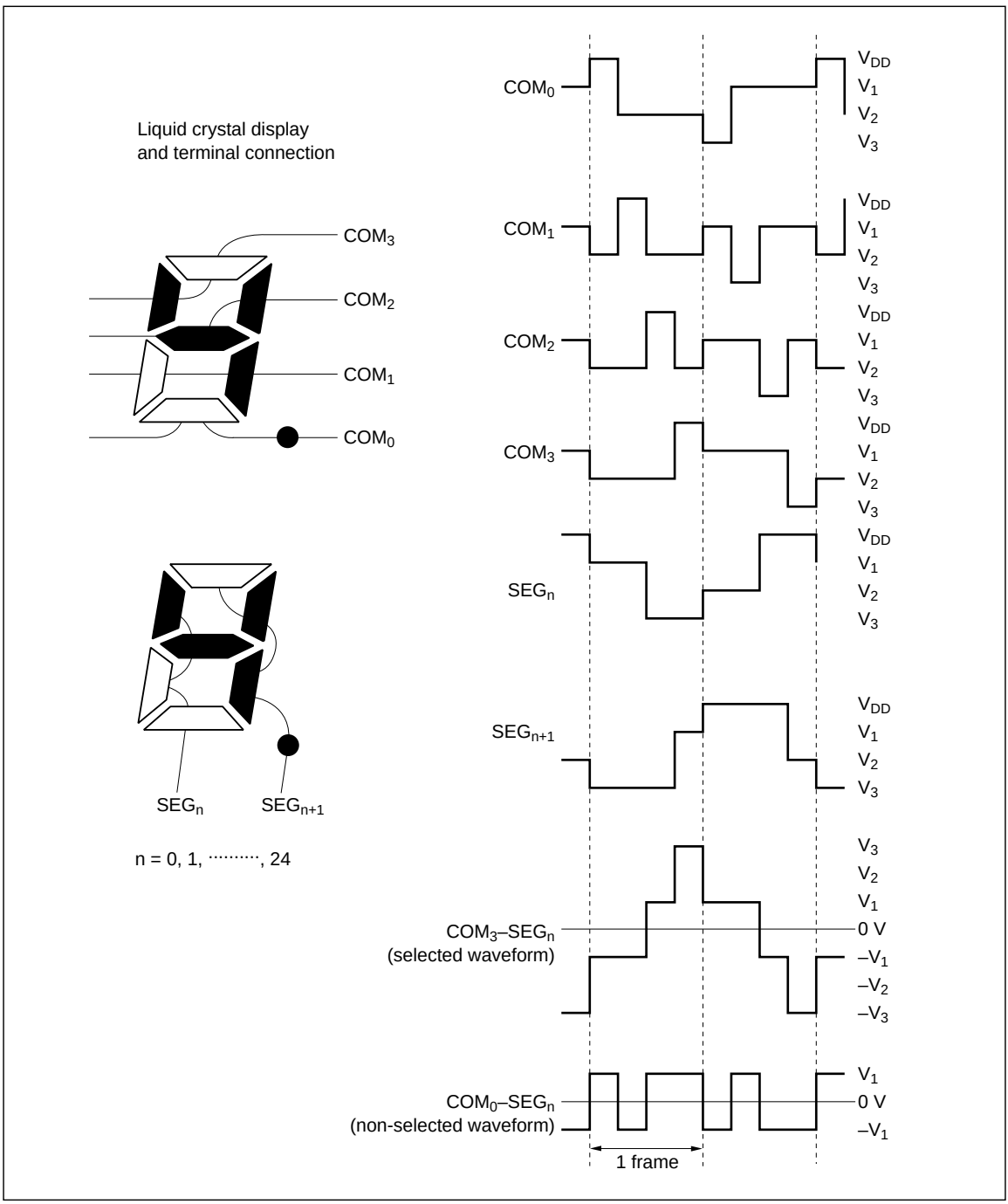


Figure 7 Example of Waveforms in 1/4 Duty Cycle Drive (B Type) (Example of HD61602)

2.4 1/4 Bias, 1/8 Duty Cycle Drive

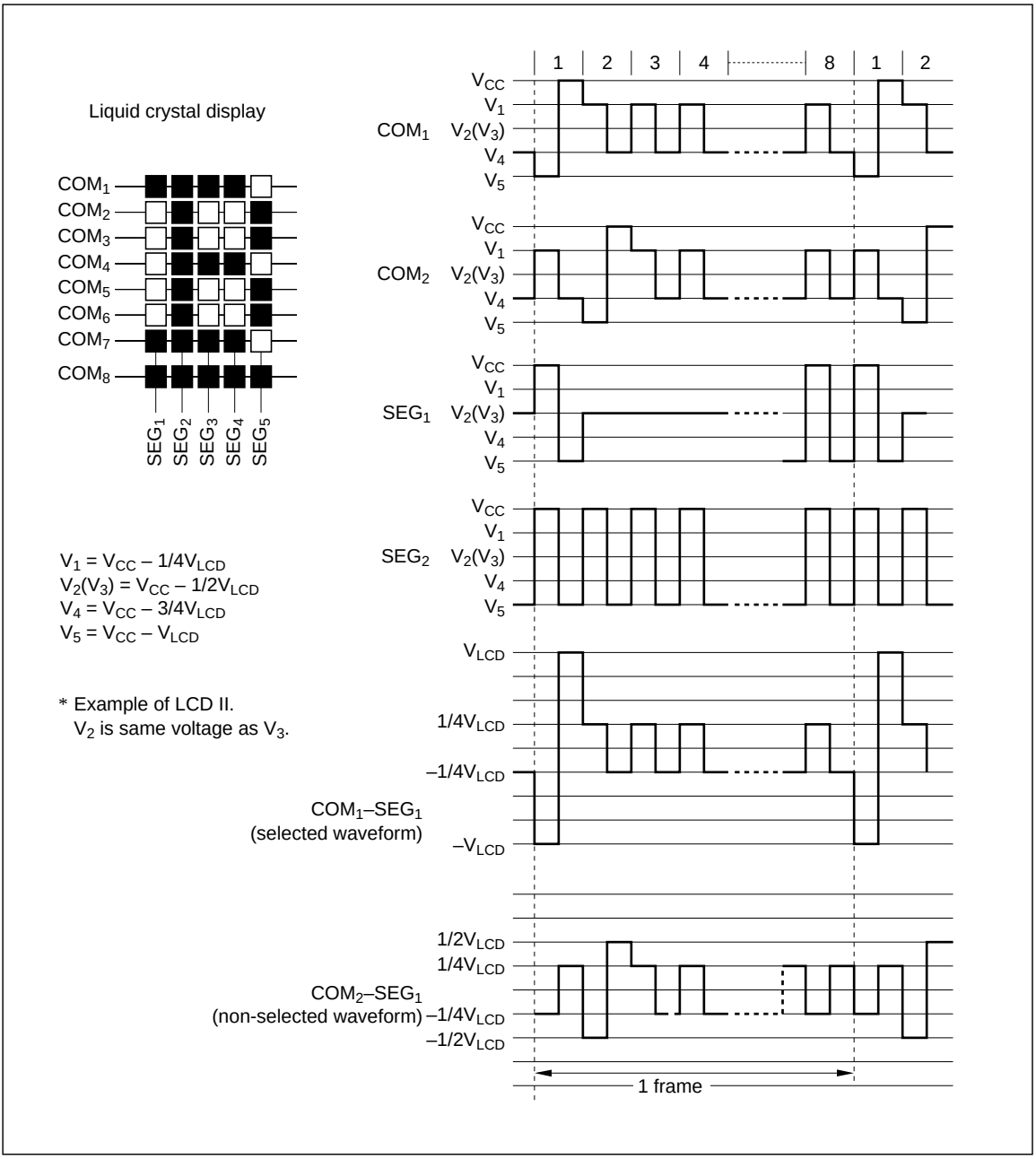


Figure 8 Example of Waveforms in 1/8 Duty Cycle Drive (A Type)
(Example of LCD-II)

2.5 1/5 Bias, 1/8 Duty Cycle Drive

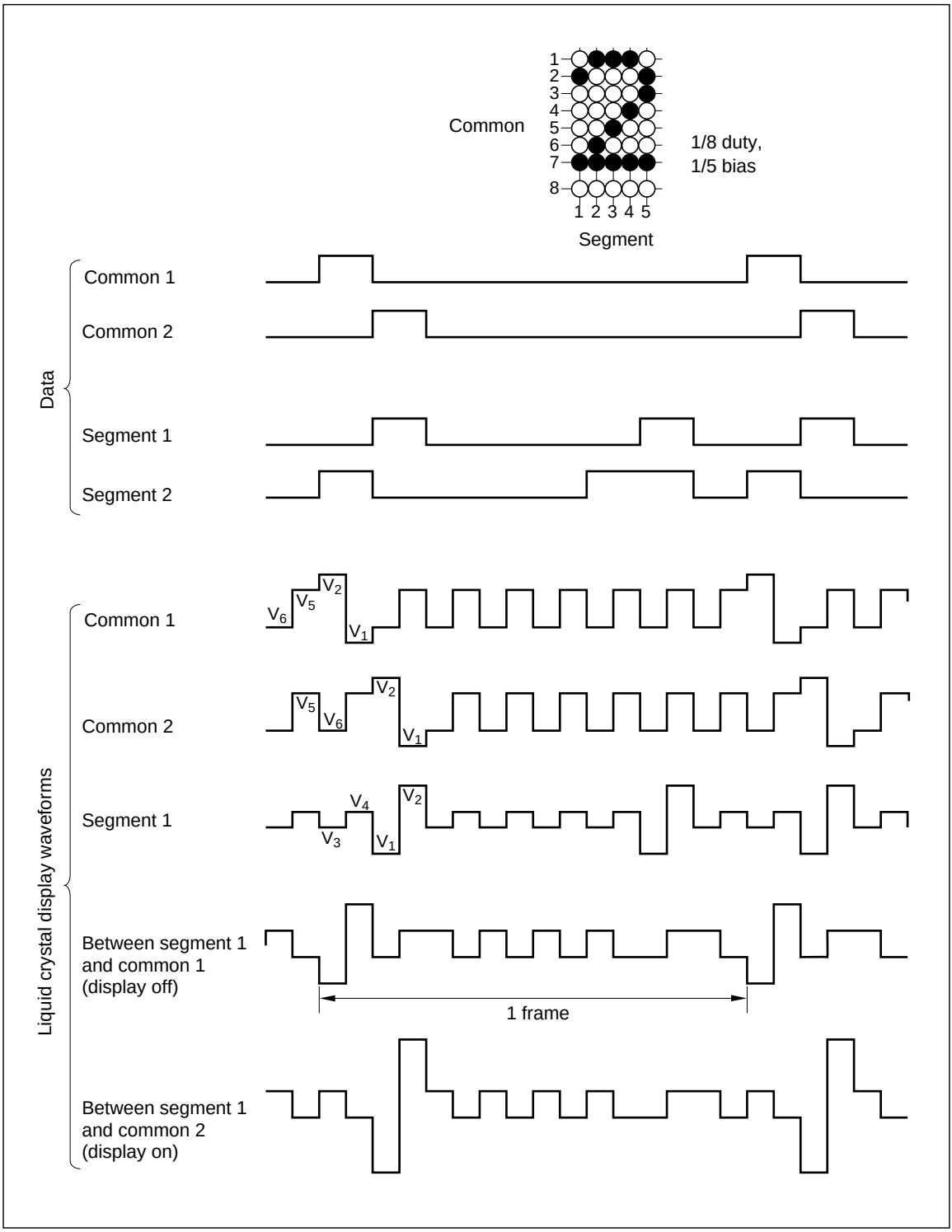


Figure 9 Example of Waveforms in 1/8 Duty Cycle Drive (A Type) (Example of HD44100R)

2.6 1/5 Bias, 1/16 Duty Cycle Drive

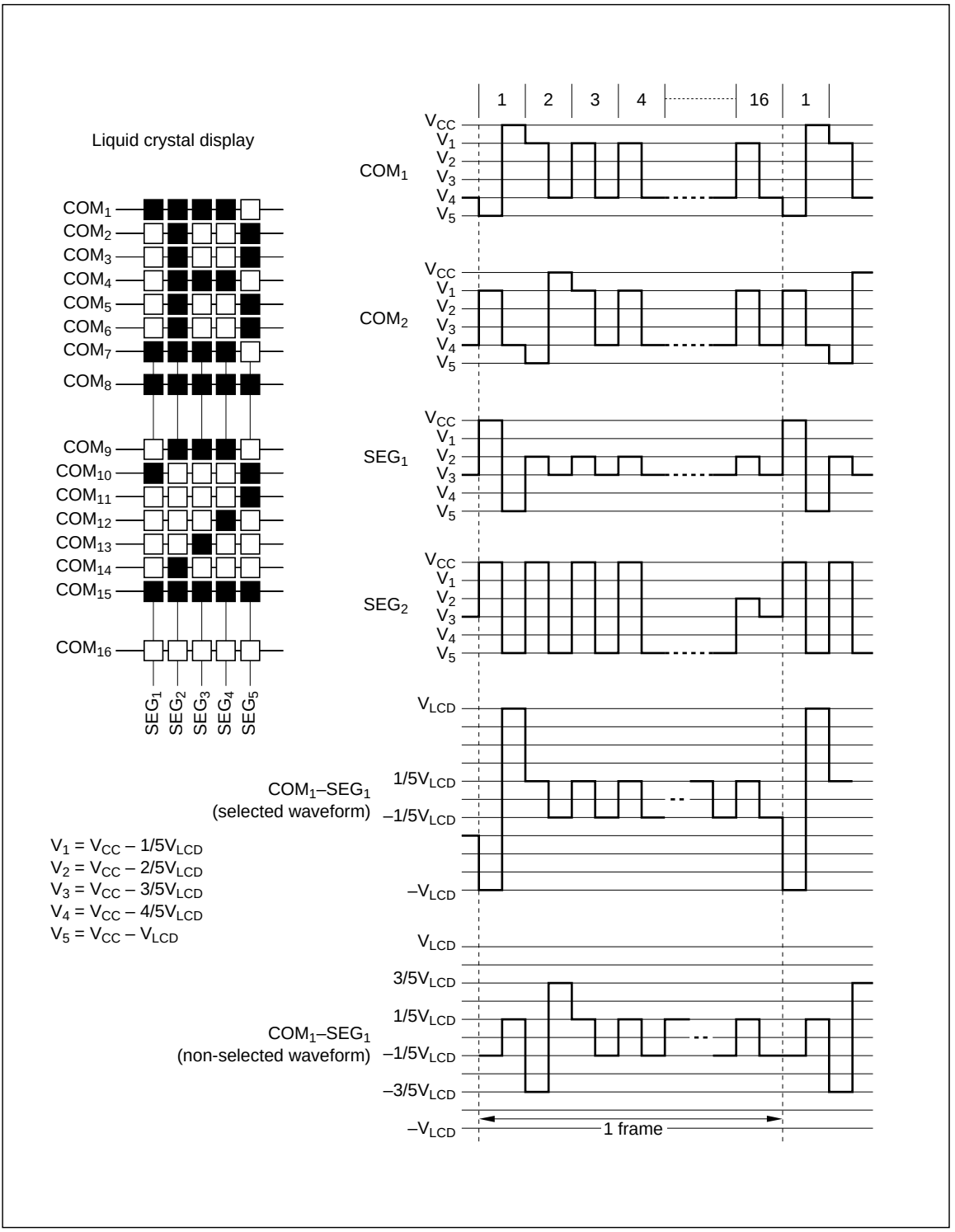


Figure 10 Example of Waveforms in 1/16 Duty Cycle Drive (A Type)
(Example of LCD-II)

2.7 1/5 Bias, 1/32 Duty Cycle Drive

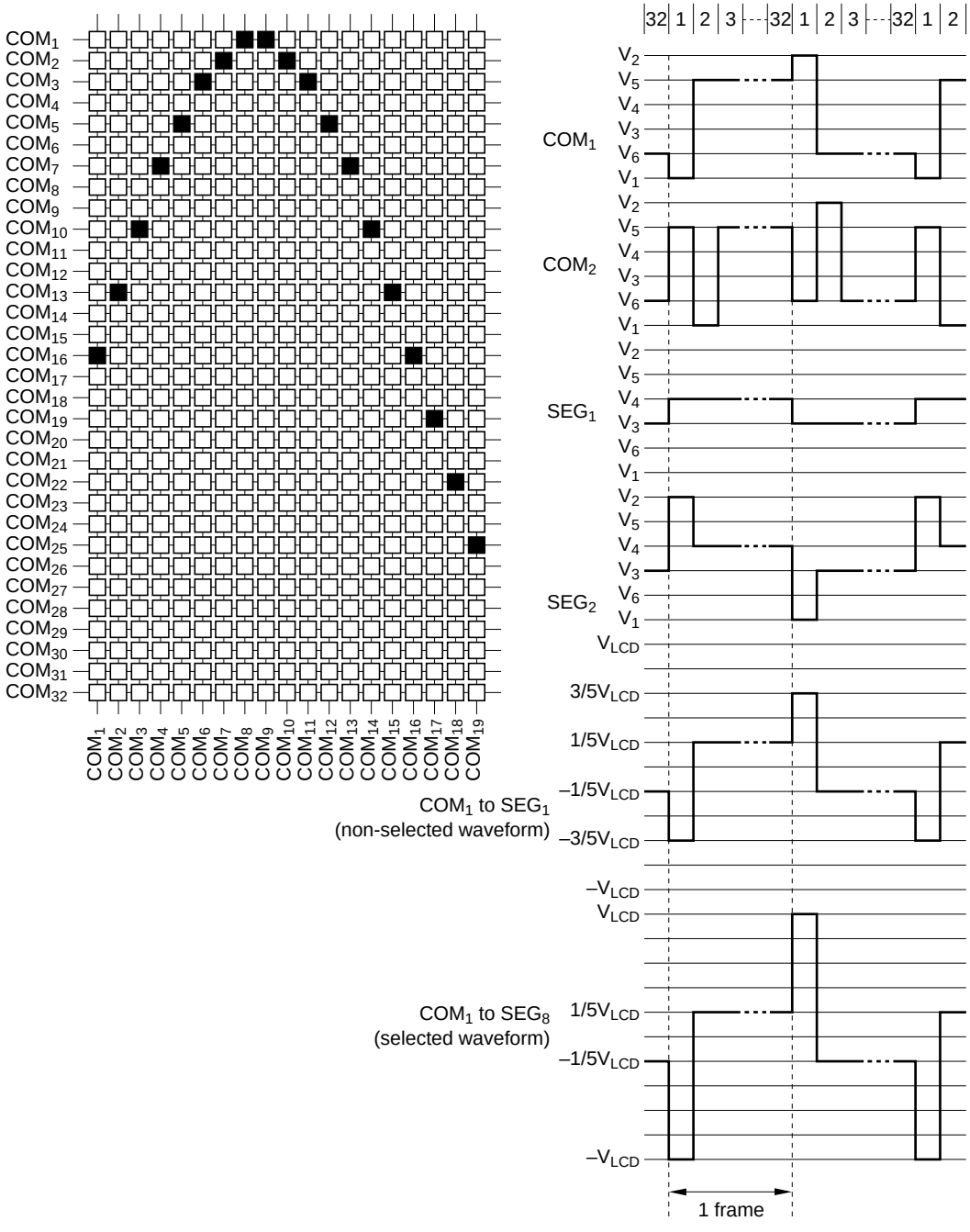


Figure 11 Example of Waveforms in 1/32 Duty Cycle Drive (Example of HD44102CH, HD44103CH)

3. Power Supply Circuit for Liquid Crystal Drive

Table 1 shows the relationship between the number of driving biases and display duty cycle ratios.

3.1 Resistive Dividing

Driving bias is generally generated by a resistive divider (figure 12).

The resistance value settings are determined by considering operating margin and power consumption. Since the liquid crystal display load is capacitive, the drive waveform itself is distorted due to charge/discharge current when the liquid crystal display drive waveform is applied. To reduce distortion, the resistance value should be decreased but this increases the power consumption because of the increase of the current through the dividing resistors. Since larger liquid crystal display panels have larger capacitance, the resistance value must be decreased proportionally.

Table 1 Relationship between the Number of Display Duty Cycle Ratio and the Number of Driving Biases

Display Duty Ratio	Static	1/2	1/3	1/4	1/7	1/8	1/11	1/12	1/14	1/16	1/24	1/32	1/64
Number of driving biases	2	3 (1/2 bias)	4 (1/3 bias)	4	5 (1/4 bias)	5	5	5	6 (1/5 bias)	6	6	6	6

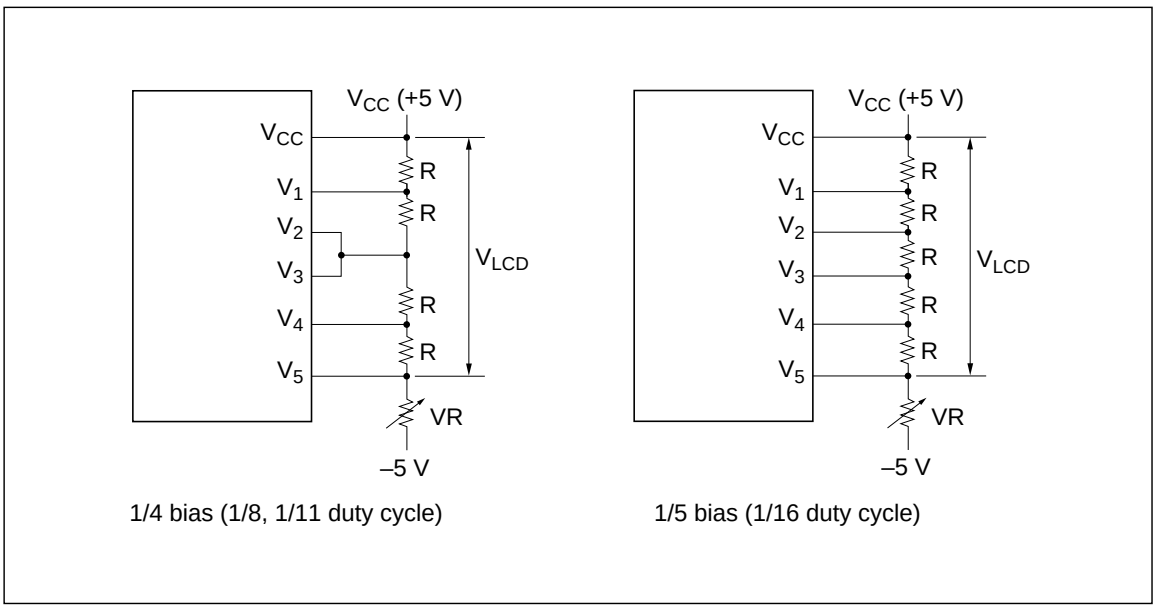


Figure 12 Example of Driving Voltage Supply

It is efficient to connect a capacitor to the resistors in parallel as shown in figure 13 in order to improve charge/discharge distortion. However, the effect is limited. Even if it is attempted to reduce the power consumption with a large resistor and improve waveform distortion with a large capacitor, a level shift occurs and the operating margin is not improved.

Since the liquid crystal display load is in a matrix configuration, the path of the charge/discharge current through the load is complicated. Moreover, it varies depending on display condition. Thus, a value of resistance cannot be simply determined from the load capacitance of liquid crystal display. It must be experimentally determined according to the demand for the power consumption of the equipment in which the liquid crystal display is incorporated.

Generally, R is 1 kΩ to 10 kΩ, and VR is 5 kΩ to 50 kΩ. No capacitor is required. A capacitor of 0.1 µF is usually used if necessary.

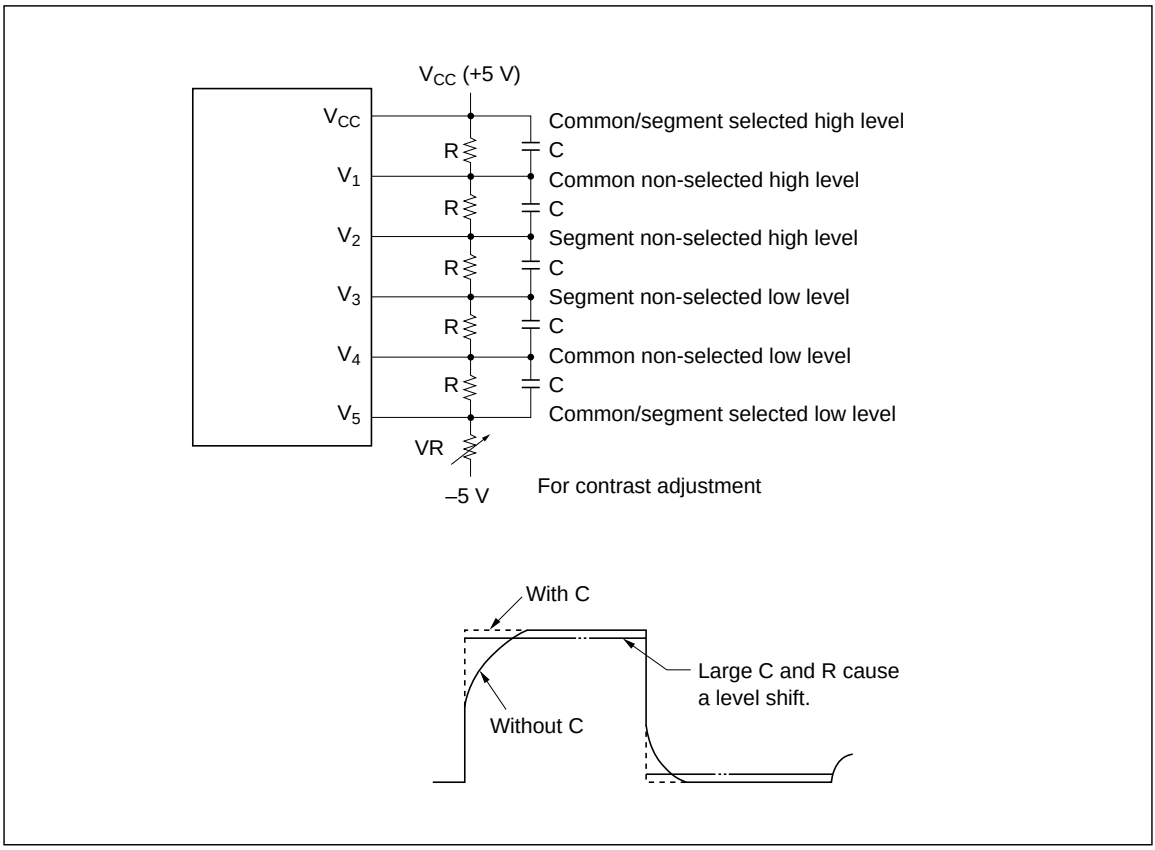


Figure 13 Example of Capacitor Connection for Improvement of Liquid Crystal Display Drive Waveform Distortion (1/5 Bias) (Example of LCD-II)

3.2 Drive by Operational Amplifier

In graphic displays, the size of the liquid crystal becomes larger and the display duty ratio becomes smaller, so the stability of liquid crystal drive level is more important than in small display system.

Since the liquid crystal for graphic displays is large and has many picture elements, the load capacitance becomes large. The high impedance of the power supply for liquid crystal drive produces distortion in the drive waveforms, and degrades display quality. For this reason, the liquid crystal drive level impedance should be reduced with operational amplifiers. Figure 14 shows an example of an operational amplifier configuration.

No load current flows through the dividing resistors because of the high input impedance of the operational amplifiers. A high resistance of R = 10 kΩ and VR = 50 kΩ can be used.

3.3 Generation of Liquid Crystal Drive Levels in LSI

The power supply circuit for liquid crystal drive level may be incorporated in the LSI, such as one for a portable calculator with liquid crystal display.

HD61602, HD61603 for small display systems has a built-in power supply circuit for liquid crystal drive levels.

3.4 Precaution on Power Supply Circuits

The LCD driver LSI has two types of power supplies: the one for logical circuits and the other for the liquid crystal display drive circuit. The power supply system is complicated because of several liquid crystal drive levels. For this reason, in the power supply design, take care not to deviate from the voltage range assured in the maximum rating at the rise of power supply and from the potential sequence of each power supply. If the input terminal level is indefinite, through current flows and the power consumption increases because of the use of CMOS process in the LCD driver.

Simultaneously, the potential sequence of each power supply becomes wrong, which may cause latch-up.

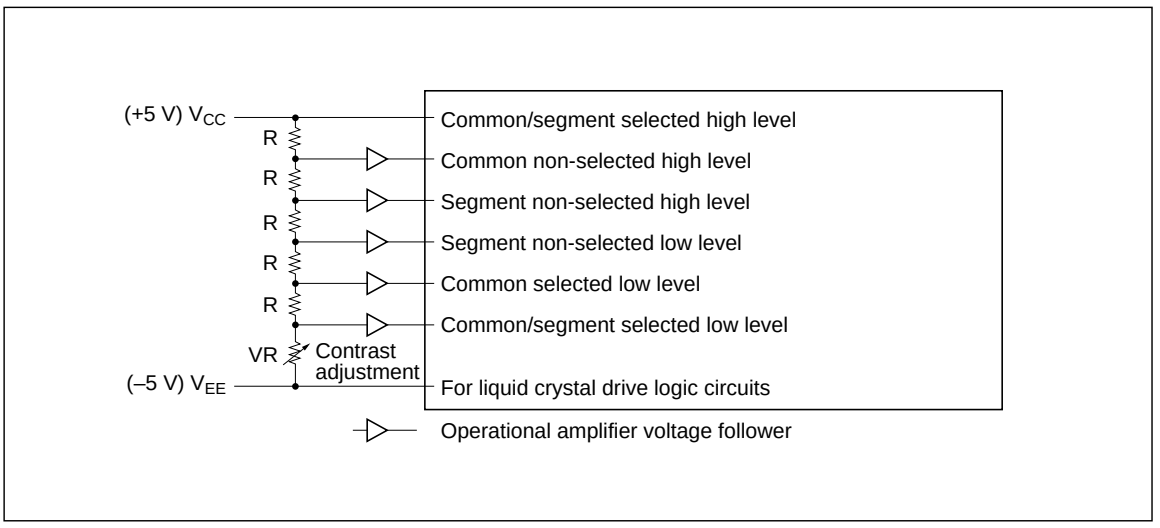


Figure 14 Drive by Operational Amplifier (1/5 Bias)

Data Sheet

HD44100R

(LCD Driver with 40-Channel Outputs)

HITACHI

Description

The HD44100R has two sets of 20-bit bidirectional shift registers, 20 data latch flipflops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

The HD44100R is a highly general liquid crystal display driver which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied as a common driver or segment driver.

Features

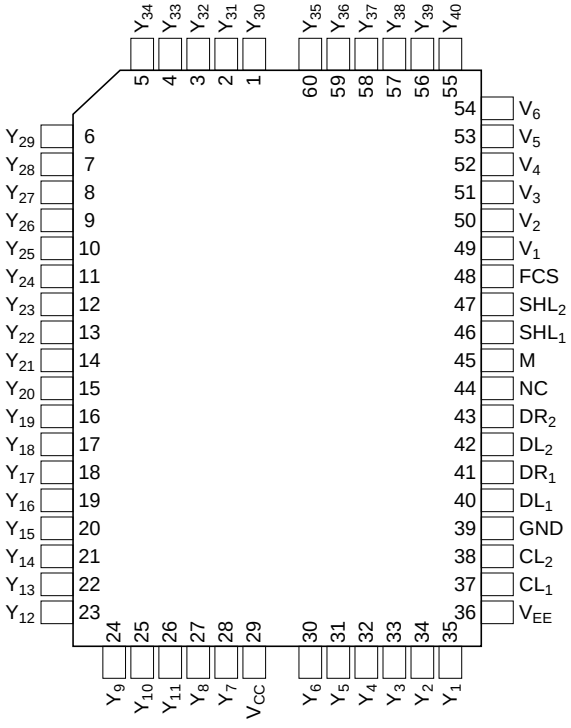
- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830/ 61830B), LCD-II (HD44780S, HD44780U), LCD-IIA (HD66780), LCD-II/E (HD66702), LCD-III (HD44790), HD66710
- 40 internal liquid crystal display drivers
- Internal serial/parallel conversion circuits
  - — 20-bit shift register × 2
  - — 20-bit data latch × 2
- Display bias: Static to 1/5
- Power supply
  - — Internal logic: V_{CC} = 2.7 to 5.5 V
  - — Liquid crystal display driver circuit: $V_{CC} - V_{EE}$ = 3 to 13 V
- Separation of internal logic from liquid crystal display driver circuit increases applicable controllers and liquid crystal types
- CMOS process
- 60 pin flat plastic package (FP-60A: short lead)

Ordering Information

Type No.	V_{CC} (V)	$V_{CC} - V_{EE}$ (V)	Package
HD44100RFS	2.7 to 5.5	3 to 13	60-pin plastic QFP (FP-60A)
HCD44100R	2.7 to 5.5	3 to 13	Chip

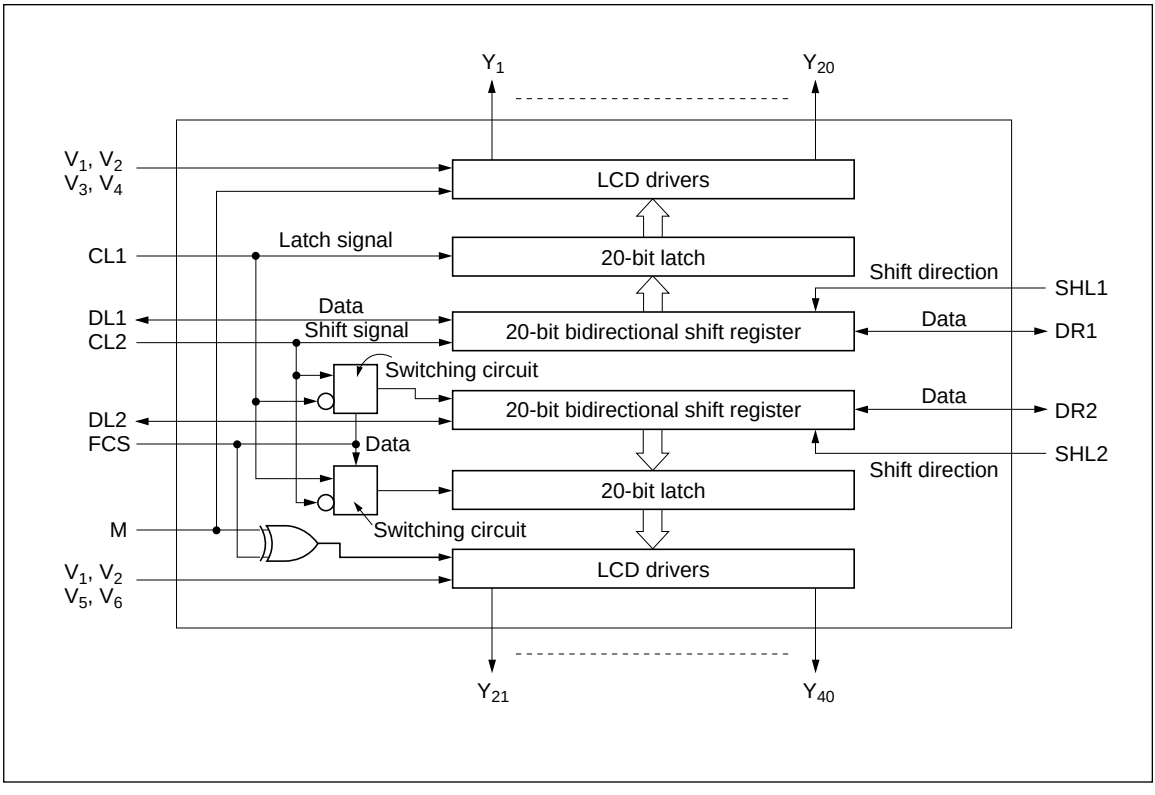
Hitachi semiconductor

Pin Arrangement



(Top view)

Block Diagram



Terminal Function

Table 1 Functional Description of Terminals

Signal Name	Number of Lines	Input/ Output	Connected to	Function
V_{CC}	1		Power supply	Power supply for logical circuit
GND	1		Power supply	0 V
V_{EE}	1		Power supply	Power supply for liquid crystal display drive
Y_1 to Y_{20}	20	Output	Liquid crystal	Liquid crystal drive output (channel 1)
Y_{21} to Y_{40}	20	Output	Liquid crystal	Liquid crystal driver output (channel 2)
V_1, V_2	2	Input	Power supply	Power supply for liquid crystal display drive (select level)
V_3, V_4	2	Input	Power supply	Power supply for liquid crystal display drive (non-select level for channel 1)
V_5, V_6	2	Input	Power supply	Power supply for liquid crystal display drive (non-select level for channel 2)
SHL1	1	Input	V_{CC} or GND	Selection of the shift direction of channel 1 shift register **SHL1 / DL1 / DR1** V_{CC} / Out / In GND / In / Out
SHL2	1	Input	V_{CC} or GND	Selection of the shift direction of channel 2 shift register **SHL2 / DL2 / DR2** V_{CC} / Out / In GND / In / Out
DL1, DR1	2	Input/ output	Controller or HD44100R	Data input/output of channel 1 shift register
DL2, DR2	2	Input/ output	Controller or HD44100R	Data input/output of channel 2 shift register
M	1	Input	Controller	Alternated signal for liquid crystal driver output
CL1	1	Input	Controller	Latch signal for channel 1 (⌐↓)*1 Used for channel 2 when FCS is GND
CL2	1	Input	Controller	Shift signal for channel 1 (⌐↓)*1 Used for channel 2 when FCS is GND

Table 1 Functional Description of Terminals (cont)

Signal Name	Number of Lines	Input/ Output	Connected to	Function
FCS	1	Input	V_{CC} or GND	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2. Thus, this signal exchanges the function of channel 2.
NC	1			Don't connect any wires to this terminal.

	Channel 2			
FCS Level	**Latch Signal**	**Shift Signal**	**M Polarity**	**Function**
V_{CC}	CL2 ↑	CL1 ↑	$\overline{M}$	For common drive
GND	CL1 ↓	CL2 ↓	M	For segment drive
	*1	*1		*2

Notes: 1. ↑ and ↓ indicate the latches at rise and fall times, respectively.

2. The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

			Output Level	
FCS	**Data**	**M**	**Channel 1 (Y_1 to Y_{20})**	**Channel 2 (Y_{21} to Y_{40})**
V_{CC} (1)	1 (select)	1	V_1	V_2
		0	V_2	V_1
	0 (non-select)	1	V_3	V_6
		0	V_4	V_5
GND (0)	1 (select)	1	V_1	V_1
		0	V_2	V_2
	0 (non-select)	1	V_3	V_5
		0	V_4	V_6

Note: 1 and 0 indicate high and low levels, respectively.

Applications

Segment Driver

When the HD44100R is used as a segment driver, FCS is set to GND to transfer display data with the timing shown in figure 1. In this case, both channel 1 and channel 2 shift data at the fall of CL2 and latch it at the fall of CL1. V_3 and V_5, V_4 and V_6 of the liquid crystal display driver power supply are short-circuited, respectively.

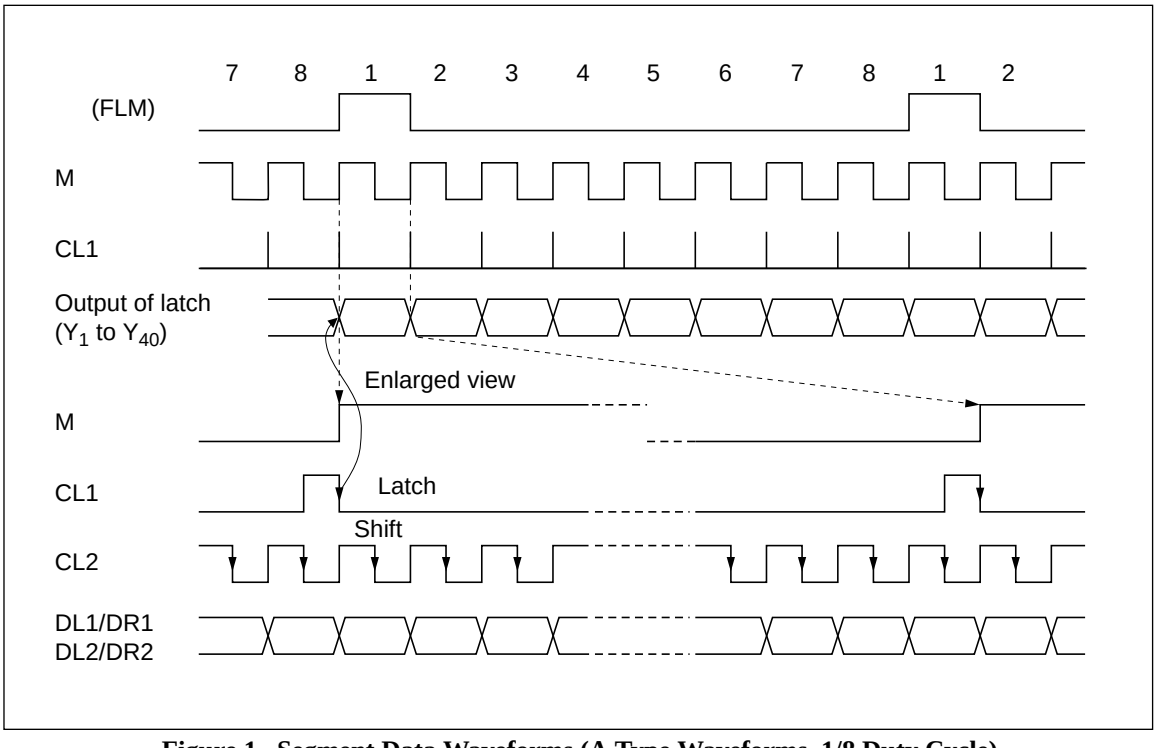


Figure 1 Segment Data Waveforms (A Type Waveforms, 1/8 Duty Cycle)

Common Driver

In this case, channel 1 is used as a segment driver and channel 2 as common driver.

When channel 2 of HD44100R is used as common driver, FCS is set to V_{CC} to transfer display data with the timing shown in figure 2.

In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 shifts and latches as shown in figure 1.

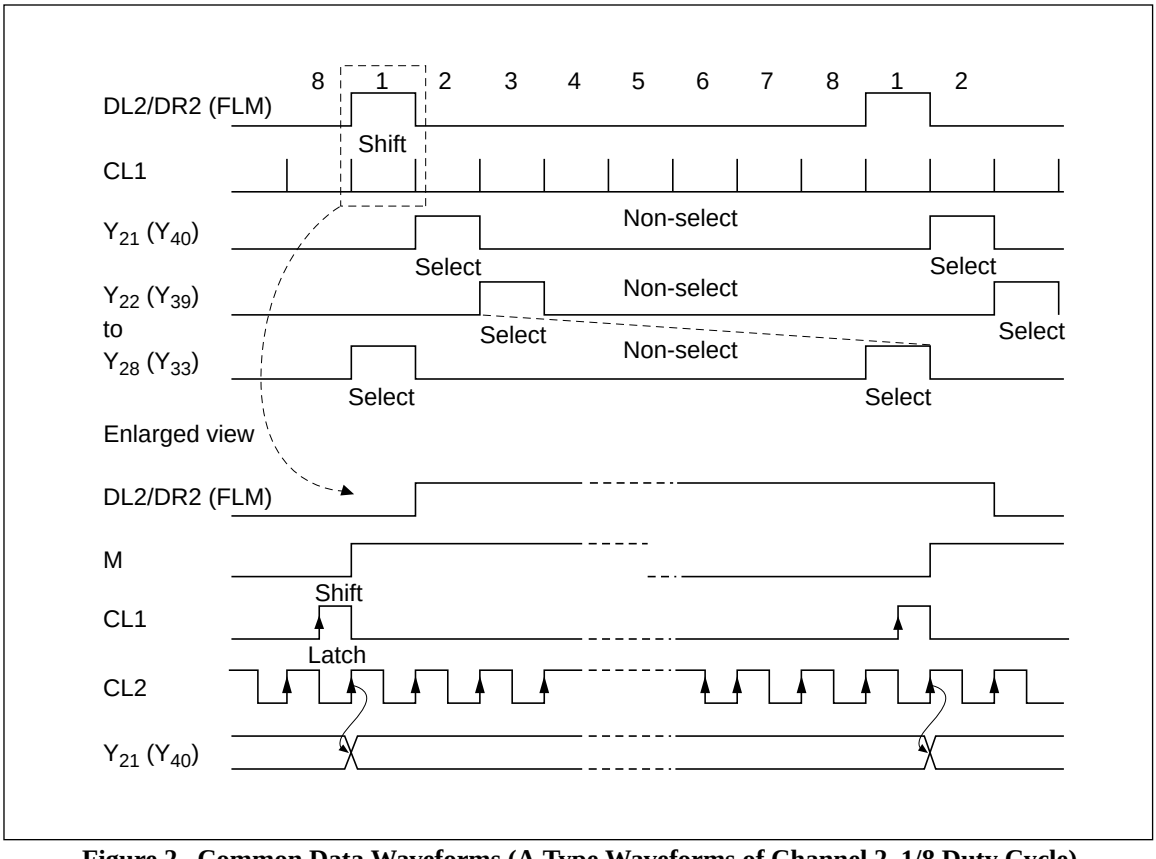


Figure 2 Common Data Waveforms (A Type Waveforms of Channel 2, 1/8 Duty Cycle)

Both Channel 1 and Channel 2 Used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100R are used common drivers, FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected as shown in figure 3.

In this case, connection of the liquid crystal display driver power supply is different from that of segment driver, so refer to figure 3.

- V_1, V_2: Select level of segment and common
- V_3, V_4: Non-select level of segment
- V_5, V_6: Non-select level of common

Static Drive

When the HD44100R is used in the static drive method (figure 4), data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of the liquid crystal display driver. The signal applied terminal M must have twice the frequency of CL1 and be synchronised at the fall of CL1. The power supply for liquid crystal display driver is used by short-circuiting V_1, V_4 and V_6, and V_2, V_3, and V_5 respectively.

One of the liquid crystal display driver output terminals can be used for a common output. In this case, FCS is set to GND and data is transferred so that 0 can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is 1, the segments of LCD light. They also light for common side = 1, and segment side 0.

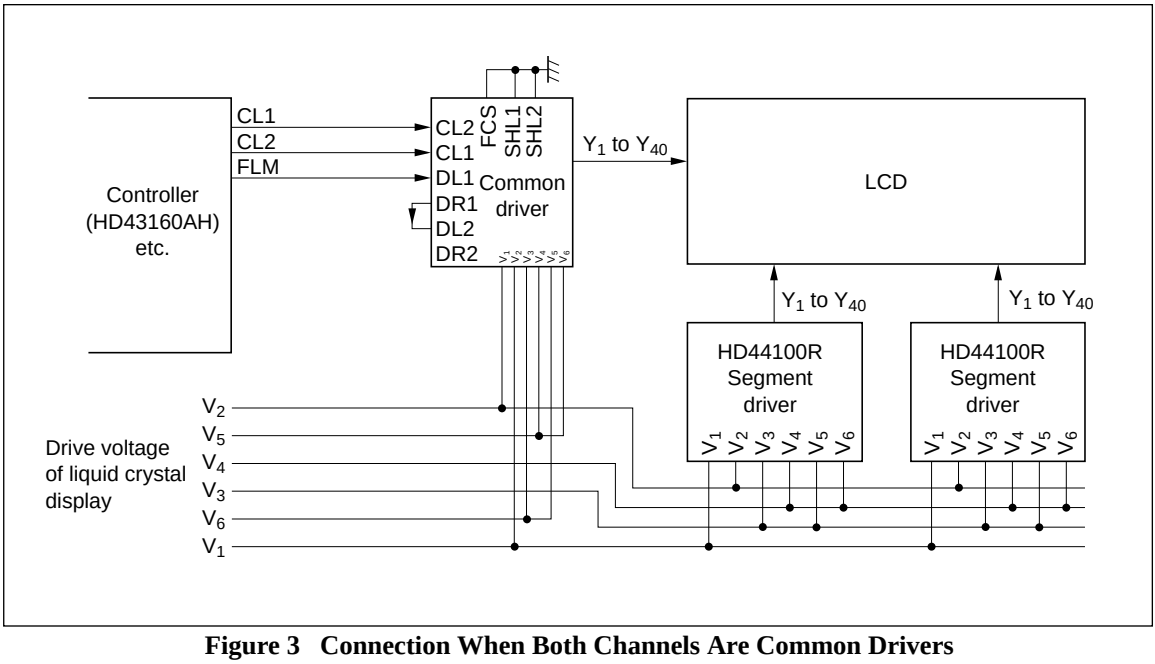


Figure 3 Connection When Both Channels Are Common Drivers

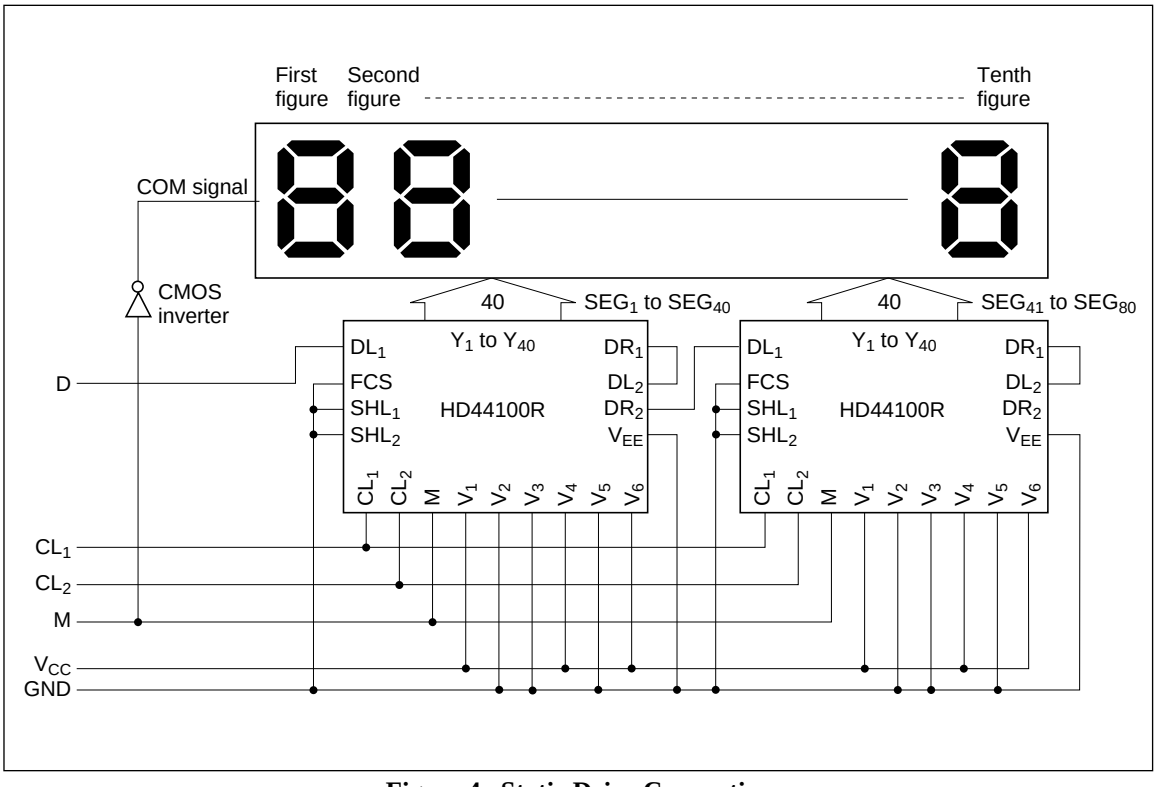
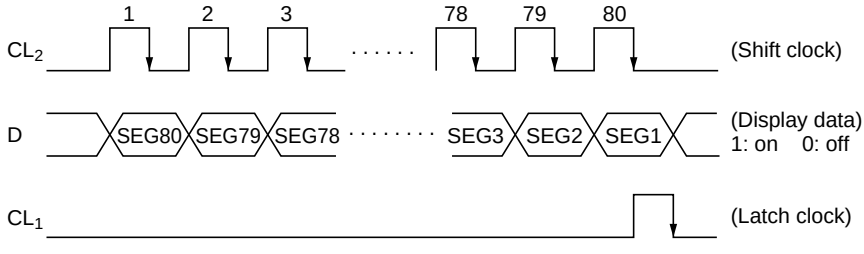
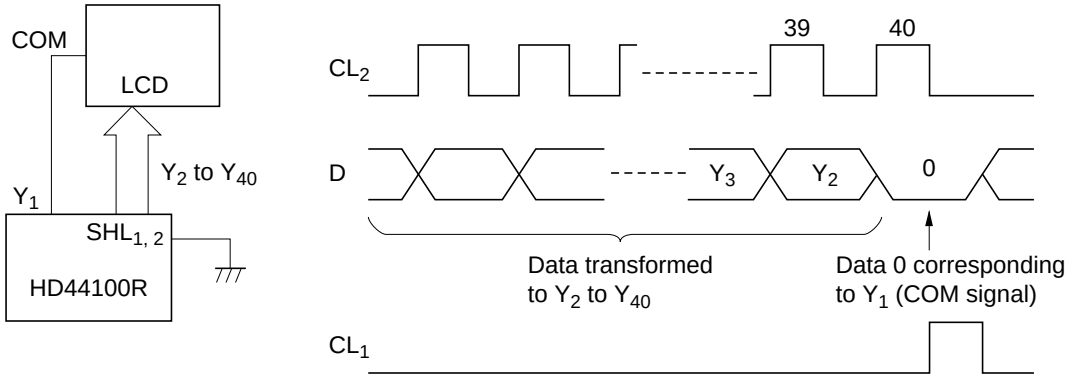


Figure 4 Static Drive Connection

Timing Chart of Input Waveforms





Notes:
1. Input square waves of 50% duty cycle (about 30 to 500 Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, have CL1 fall synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD44100R outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

Absolute Maximum Ratings

Item		Symbol	Value	Unit
Supply voltage	Logic	V_{CC} *1	–0.3 to +7.0	V
	LCD drivers	V_{EE} *2	V_{CC} – 15.0 to V_{CC} + 0.3	V
Input voltage		V_{T1} *1	–0.3 to V_{CC} + 0.3	V
Input voltage		V_{T2} *3	V_{CC} + 0.3 to V_{EE} – 0.3	V
Operating temperature		T_{opr}	–20 to +75	°C
Storage temperature		T_{stg}	–55 to +125	°C

Notes: 1. All voltage values are referred to GND.
2. Connect a protection resistor of 220 Ω ± 5% to V_{EE} power supply in series.
3. Applies to V_1 to V_6.

Electrical Characteristics (V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 3 to 13 V, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Input voltage	V_{IH}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS	0.7 V_{CC}	—	V_{CC}	V	V_{CC} = 4.5 to 5.5 V
			0.8 V_{CC}	—	V_{CC}	V	V_{CC} = 2.7 to 4.5 V
	V_{IL}		0	—	0.3 V_{CC}	V	V_{CC} = 4.5 to 5.5 V
			0	—	0.2 V_{CC}	V	V_{CC} = 2.7 to 4.5 V
Output voltage	V_{OH}	DL1, DL2, DR1, DR2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA
	V_{OL}		—	—	0.4	V	I_{OL} = +0.4 mA
On resistance	R_{ON}	*1	—	—	20	kΩ	$\pm I_d$ = 0.05 mA, $V_{CC} - V_{EE}$ = 4 V
Input leakage current	I_{IL}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS, NC	–5.0	—	5.0	µA	V_{in} = 0 to V_{CC}
Vi leakage current	I_{VL}	*2	–10.0	—	10.0	µA	V_{in} = V_{CC} to V_{EE}
Power supply current	I_{CC}	*3	—	—	1.0	mA	f_{CL2} = 400 kHz
	I_{EE}		—	—	10	µA	f_{CL1} = 1 kHz

Notes: 1. Applies to the resistance between V_i and Y_j when a current $\pm I_d$ = 0.05 mA flows through all of the Y pins.

2. Output Y1 to Y40 open.

3. Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

Timing Characteristics (V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 3 to 13 V, GND = 0 V, Ta = –20 to +75°C)

Item		Symbol	Applicable Terminals	Min	Typ	Max	Unit	Test Condition
Data shift frequency		f_{CL}	CL2	—	—	400	kHz	
Clock width	High level	t_{CWH}	CL1, CL2	800	—	—	ns	
	Low level	t_{CWL}	CL2	800	—	—	ns	
Data set-up time		t_{SU}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	
Clock set-up time		t_{SL}	CL1, CL2	500	—	—	ns	(CL2 → CL1)
Clock set-up time		t_{LS}	CL1, CL2	500	—	—	ns	(CL1 → CL2)
Data delay time		t_{pd}	DL1, DL2, DR1, DR2	—	—	500	ns	C_L = 15 pF
Clock rise/fall time		t_{ct}	CL1, CL2	—	—	200	ns	
Data hold time		t_{DH}	DL1, DL2, DR1, DR2, FLM	300	—	—	ns	

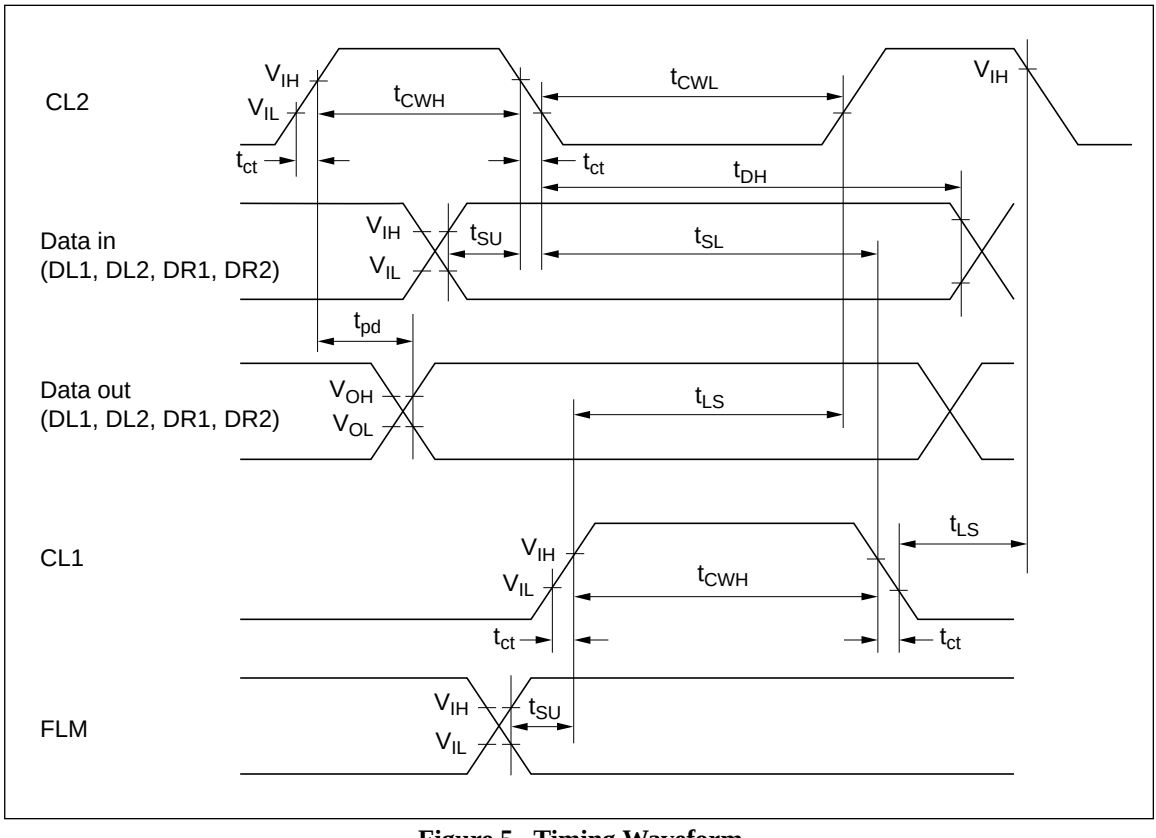


Figure 5 Timing Waveform

HD66100F

(LCD Driver with 80-Channel Outputs)

HITACHI

Description

The HD66100F description segment driver with 80 LCD drive circuits is the improved version of the no longer current HD44100H LCD driver with 40 circuits.

It is composed of a shift register, an 80-bit latch circuit, and 80 LCD drive circuits. Its interface is compatible with the HD44100H. It reduces the number of LSI's and lowers the cost of an LCD module.

Features

- LCD driver with serial/parallel converting function
- Interface compatible with the HD44100H; connectable with HD43160AH, HD61830, HD61830B, LCD-II (HD44780), LCD-III (HD44790)
- Internal output circuits for LCD drive: 80
- Internal serial/parallel converting circuits
  - — 80-bit bidirectional shift register
  - — 80-bit latch circuit
- Power supply
  - — Internal logic circuit: +5 V ±10%
  - — LCD drive circuit: 3.0 V to 6.0 V
- CMOS process

Comparison with HD44100H

Table 1 shows the main differences between HD66100F and HD44100H.

Table 1 Difference between Products HD66100F and HD44100H

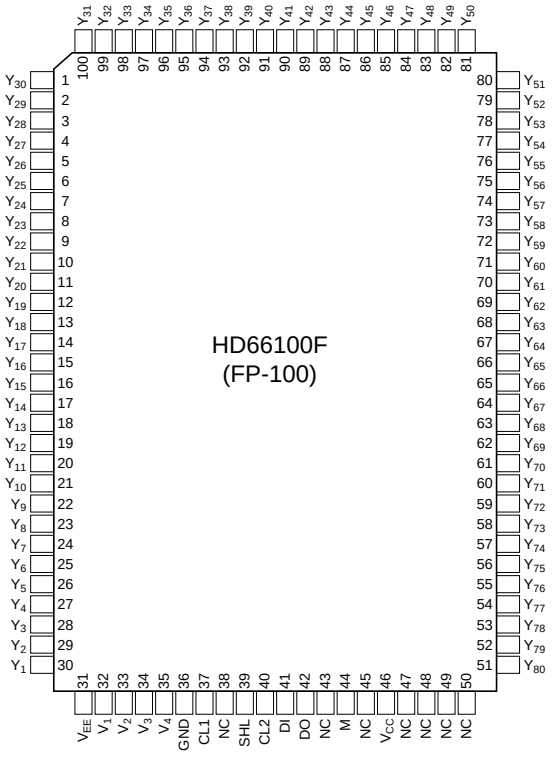
	HD66100F	HD44100H
LCD drive outputs	80 × 1 channel	20 × 2 channels
Supply voltage for LCD drive circuits	3 to 6 V	4.5 to 11 V
Multiplexing duty ratio	Static to 1/16 duty	Static to 1/32 duty
Package	100-pin plastic QFP	60-pin plastic QFP

Ordering Information

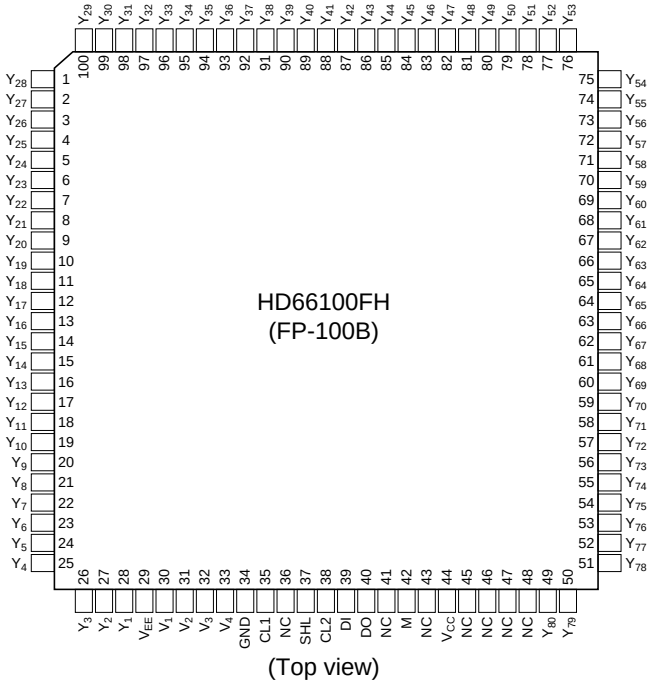
Type No.	Package
HD66100F	100-pin plastic QFP (FP-100)
HD66100FH	100-pin plastic QFP (FP-100B)
HD66100D	Chip

Hitachi semiconductor

Pin Arrangement



(Top view)



(Top view)

Pin Description

V_{CC}, GND, V_{EE}: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground. V_{EE} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1 to V_4 supply power for driving an LCD (figure 2).

CL1: HD66100F latches data at the negative edge of CL1.

CL2: HD66100F receives shift data at the negative edge of CL2.

M: Changes LCD drive outputs to AC.

DI: Inputs data to the shift register.

DO: Output data from the shift register.

SHL: Selects a shift direction of serial data. When the serial data is input in order of D_1, D_2,..., D_{79}, D_{80}, the relation between the data and the output Y is shown in table 3.

Y_1–Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 2).

NC: Do not connect any wire to these terminals.

Table 2 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	46	V_{CC}	—
GND	36	Ground	—
V_{EE}	31	V_{EE}	—
V_1	32	V_1	—
V_2	33	V_2	—
V_3	34	V_3	—
V_4	35	V_4	—
CL1	37	Clock 1	I
CL2	40	Clock 2	I
M	44	M	I
DI	41	Data in	I
DO	42	Data out	O
SHL	39	Shift left	I
Y_1–Y_{80}	1–30, 51–100	Y_1–Y_{80}	O
NC	38, 43, 45, 47–50	No connection	—

Table 3 Relation between SHL and Data Output

SHL	Y_1	Y_2	Y_3.....	Y_{79}	Y_{80}
High	D1	D2	D3.....	D79	D80
Low	D80	D79	D78.....	D2	D1

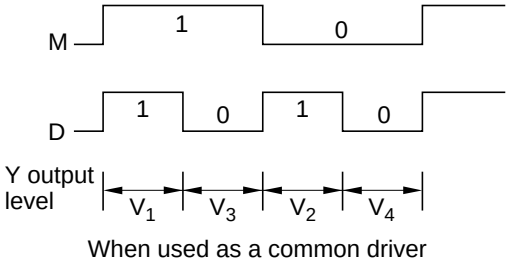


Figure 1 Selection of LCD Drive Output

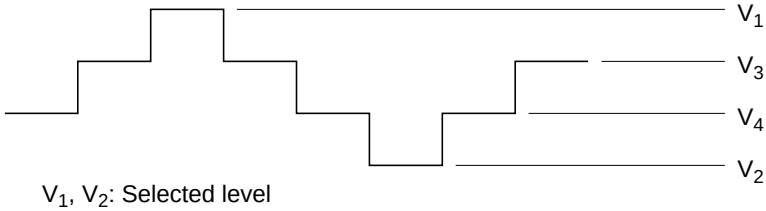


Figure 2 Power Supply for Driving an LCD

Block Functions

LCD Drive Circuits

Select one of four levels of voltage V_1, V_2, V_3, and V_4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

Latch Circuit

Latches the data input from the bidirectional shift register at the fall of CL1 and transfer its outputs to the LCD drive circuits.

Bidirectional Shift Register

Shifts the serial data at the fall of CL2 and transfers the output of each bit of the register to the latch circuit. When SHL = GND, the data input from DI shifts from bit 1 to bit 80 in order of entry. On the other hand, when SHL = V_{CC}, the data shifts from bit 80 to bit-1. In both cases, the data of the last bit of the register is latched to be output from DO at the rise of CL2.

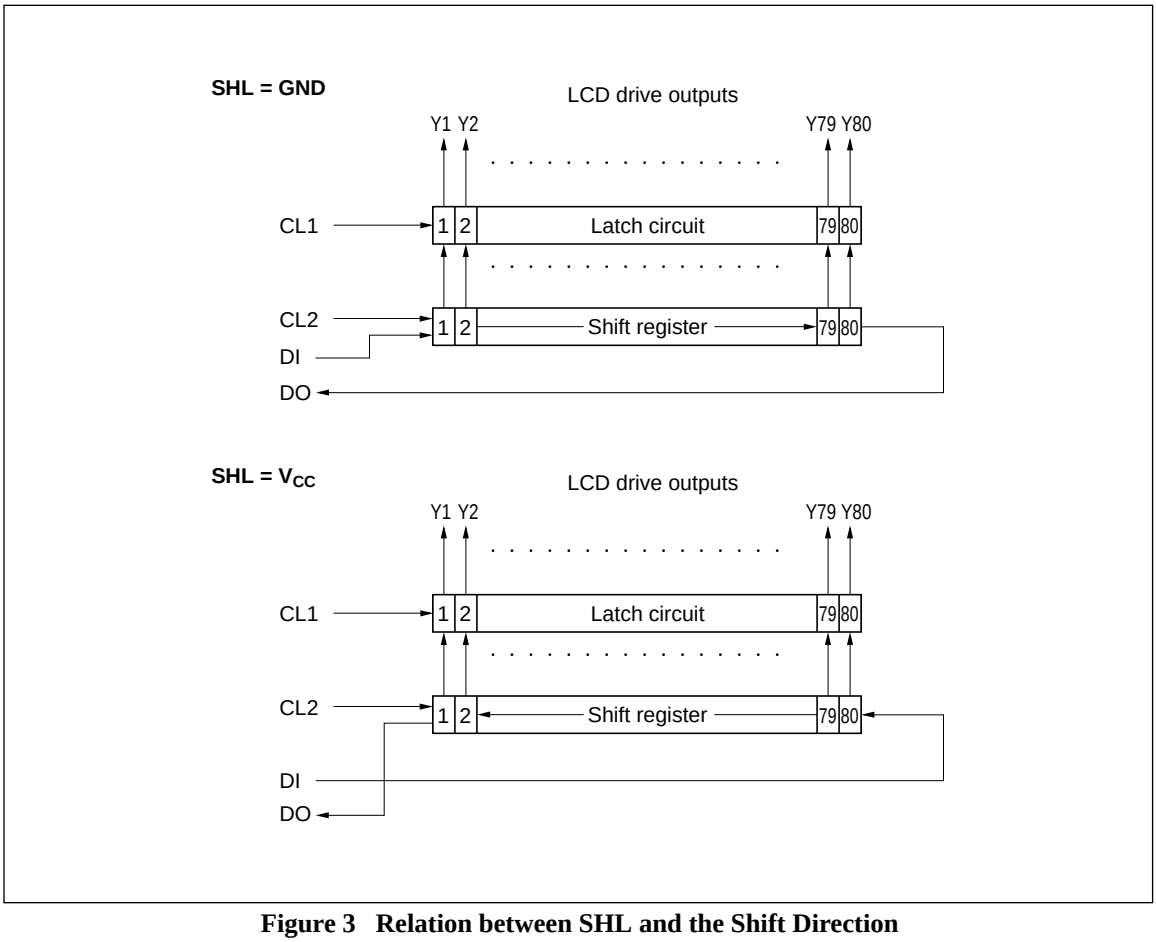


Figure 3 Relation between SHL and the Shift Direction

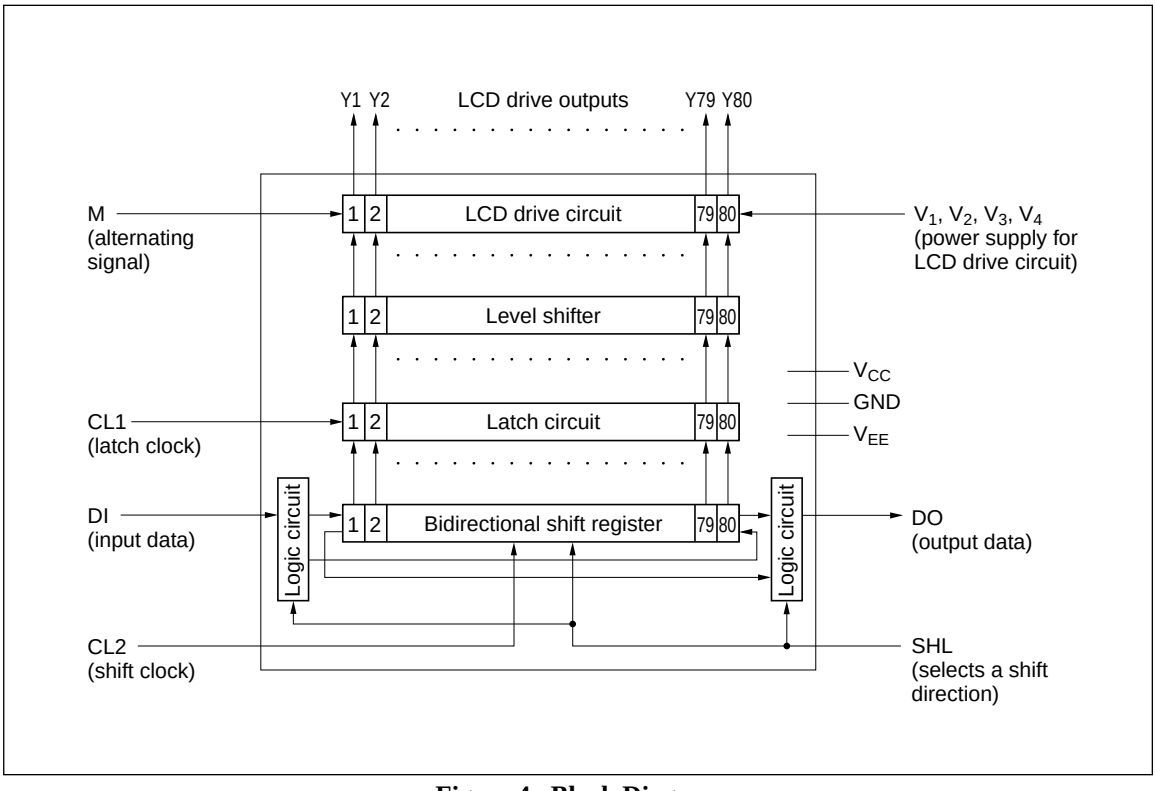


Figure 4 Block Diagram

Primary Operations

Shifting Data

The input data DI shifts at the fall of CL2 and the data delayed 80 bits by the shift register is output from the DO terminal. The output of DO changes synchronously with the rise of CL2. This operation is completely unaffected by the latch clock CL1.

Latching Data

The data of the shift register is latched at the negative edge of the latch clock CL1. Thus, the outputs Y_1–Y_{80} change synchronously with the fall of CL1.

Switching Data Shift Direction

When the shift direction switching signal SHL is connected with GND, the data D80, immediately before the negative edge of CL1, is output from the output terminal Y1. When SHL is connected with V_{CC}, it is output from Y_{80}.

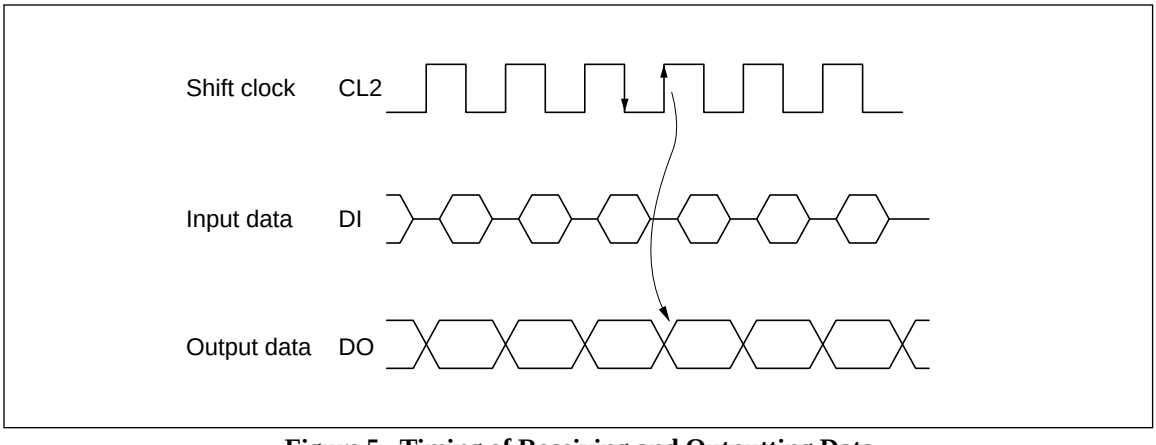


Figure 5 Timing of Receiving and Outputting Data

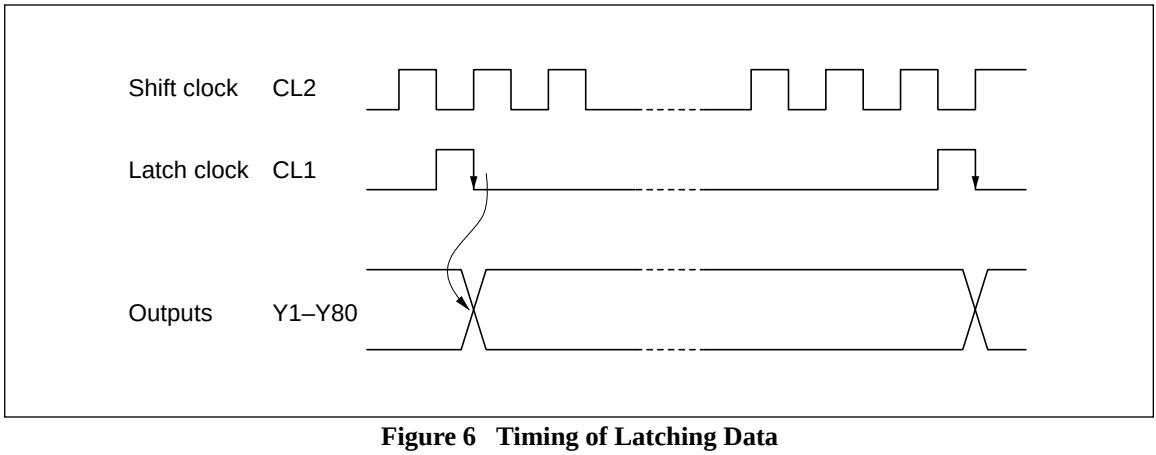


Figure 6 Timing of Latching Data

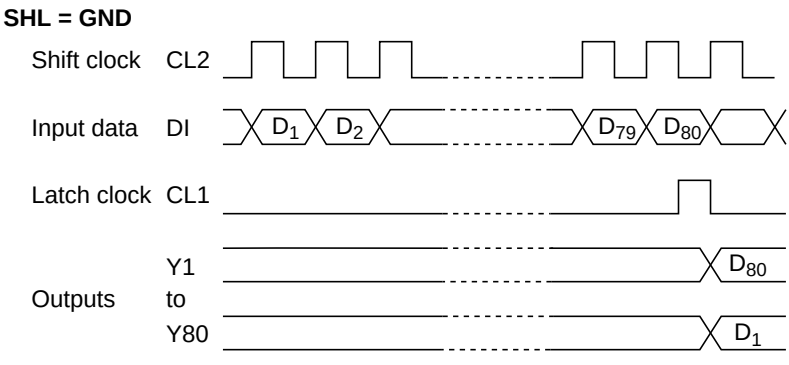


Figure 7 SHL and Waveforms of Data Shift

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Supply voltage	Logic circuits	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuits	V_{CC}–V_{EE}	–0.3 to +7.0	V	
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1
Input voltage (2)		V_{T2}	V_{CC} + 0.3 to V_{EE} – 0.3	V	2
Operation temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. A reference point is GND (= 0 V)
2. Applies to V_1–V_4.

Note: If used beyond the absolute maximum ratings, LSIs may be permanently destroyed. It is best to use them at the electrical characteristics for normal operations. If they are not used at these conditions, it may affect the reliability of the device.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, $V_{CC} - V_{EE}$ = 3.0 to 6.0 V, GND = 0 V, Ta = –20 to +75°C)

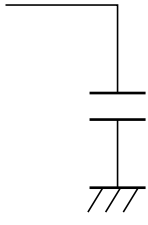
Item	Symbol	Terminals	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	CL1, CL2, M, DI, SHL	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	V_{IL}		0	—	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	DO	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}		—	—	0.4	V	I_{OL} = +0.4 mA	
On resistance Vi–Vj	R_{ON1}	Y_1–Y_{80} V_1–V_4	—	—	11	kΩ	I_{ON} = 0.1 mA to one Y terminal	
	R_{ON2}		—	—	30	kΩ	I_{ON} = 0.05 mA to each Y terminal	
Input leakage current	I_{IL}	CL1, CL2, M, DI, SHL	–5.0	—	5.0	µA	V_{in} = 0 V to V_{CC}	
Vi leakage current	I_{VL}	V_1–V_4	–5.0	—	5.0	µA	Output Y_1–Y_{80} open V_{in} = V_{CC} to V_{EE}	
Current dissipation	I_{GND}		—	—	2.0	mA	f_{CL2} = 1.0 MHz f_{CL1} = 2.5 kHz	1
	I_{EE}		—	—	0.1	mA		

Note: 1. Input/output currents are excluded; when an input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit.
To avoid this, V_{IH} and V_{IL} must be fixed at V_{CC} and GND level respectively.

AC Characteristics (V_{CC} = 5 V ± 10%, $V_{CC} - V_{EE}$ = 3.0 to 6.0 V, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Terminals	Min	Typ	Max	Unit	Note
Data shift frequency	f_{CL}	CL2	—	—	1	MHz	
Clock high level width	t_{CWH}	CL1, CL2	450	—	—	ns	
Clock low level width	t_{CWL}	CL2	450	—	—	ns	
Data set-up time	f_{SU}	D_I	100	—	—	ns	
Clock set-up time (1)	t_{SL}	CL2	200	—	—	ns	1
Clock set-up time (2)	t_{LS}	CL1	200	—	—	ns	2
Output delay time	t_{pd}	DO	—	—	250	ns	3
Data hold time	t_{DH}	DI	100	—	—	ns	
Clock rise/fall time	f_{CT}	CL1, CL2	—	—	50	ns	

Notes: 1. Set-up time from the fall of CL2 to that of CL1.
2. Set-up time from the fall CL1 to that of CL2.
3. Test terminal



C_L (Load capacitance on outputs) = 30 pF
(Including jig capacitance)

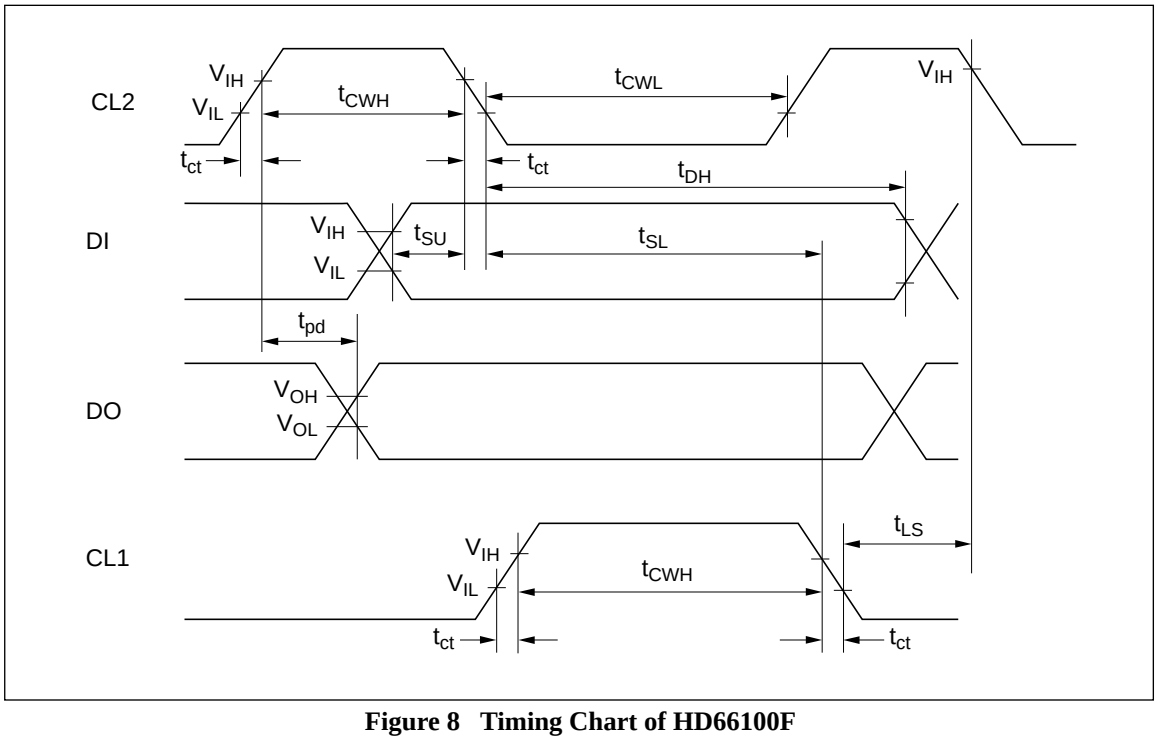


Figure 8 Timing Chart of HD66100F

Typical Applications

Connection with the LCD Controller HD44780

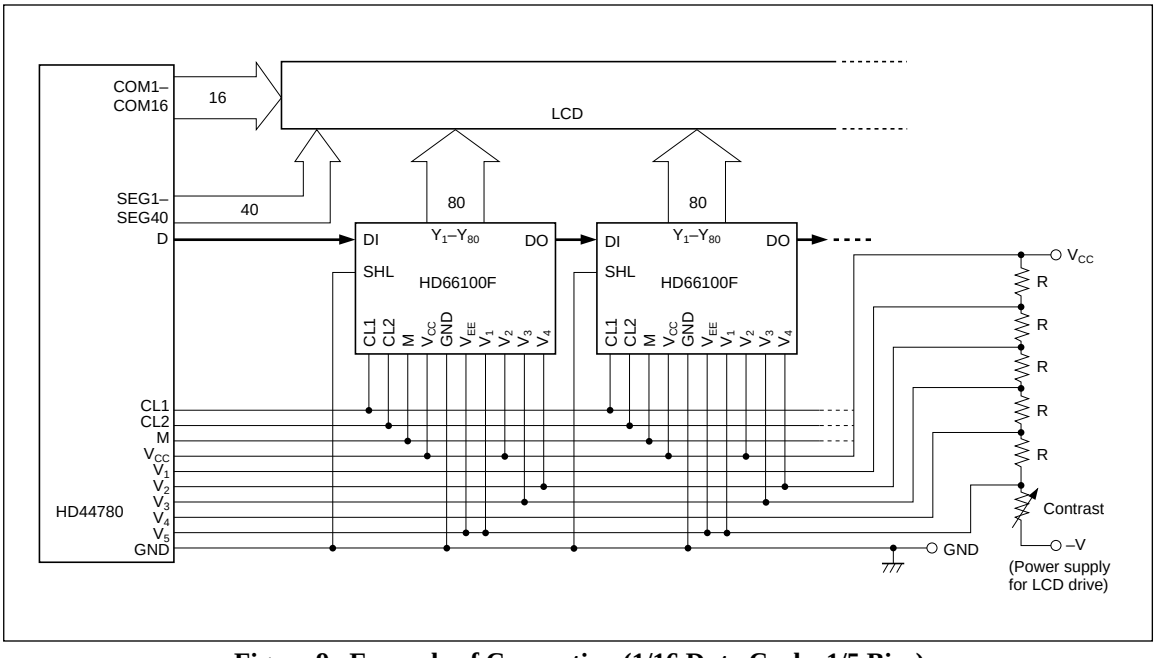


Figure 9 Example of Connection (1/16 Duty Cycle, 1/5 Bias)

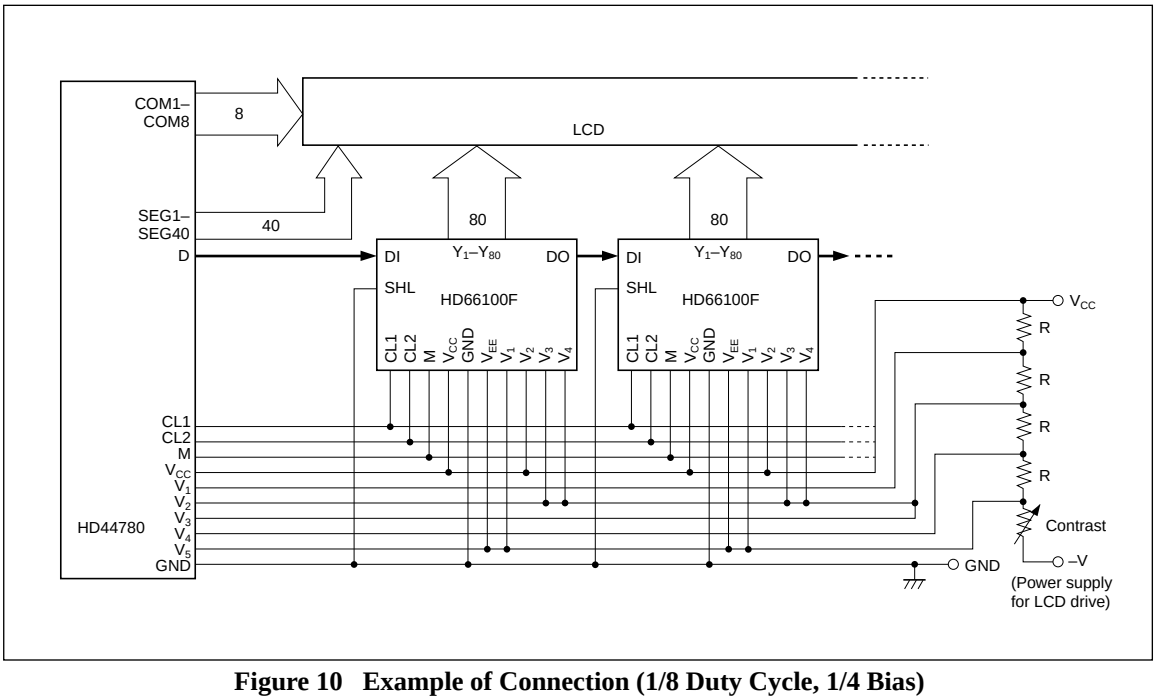


Figure 10 Example of Connection (1/8 Duty Cycle, 1/4 Bias)

Connection with LCD III (HD44790)

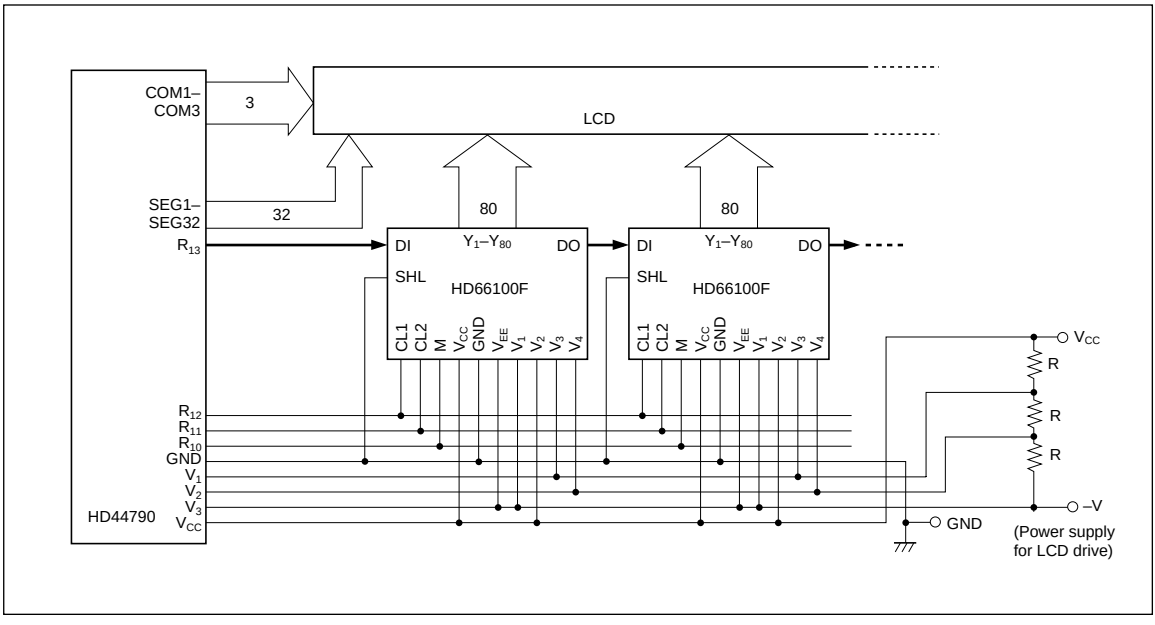


Figure 11 Example of Connection (1/3 Duty Cycle, 1/3 Bias)

Static Drive

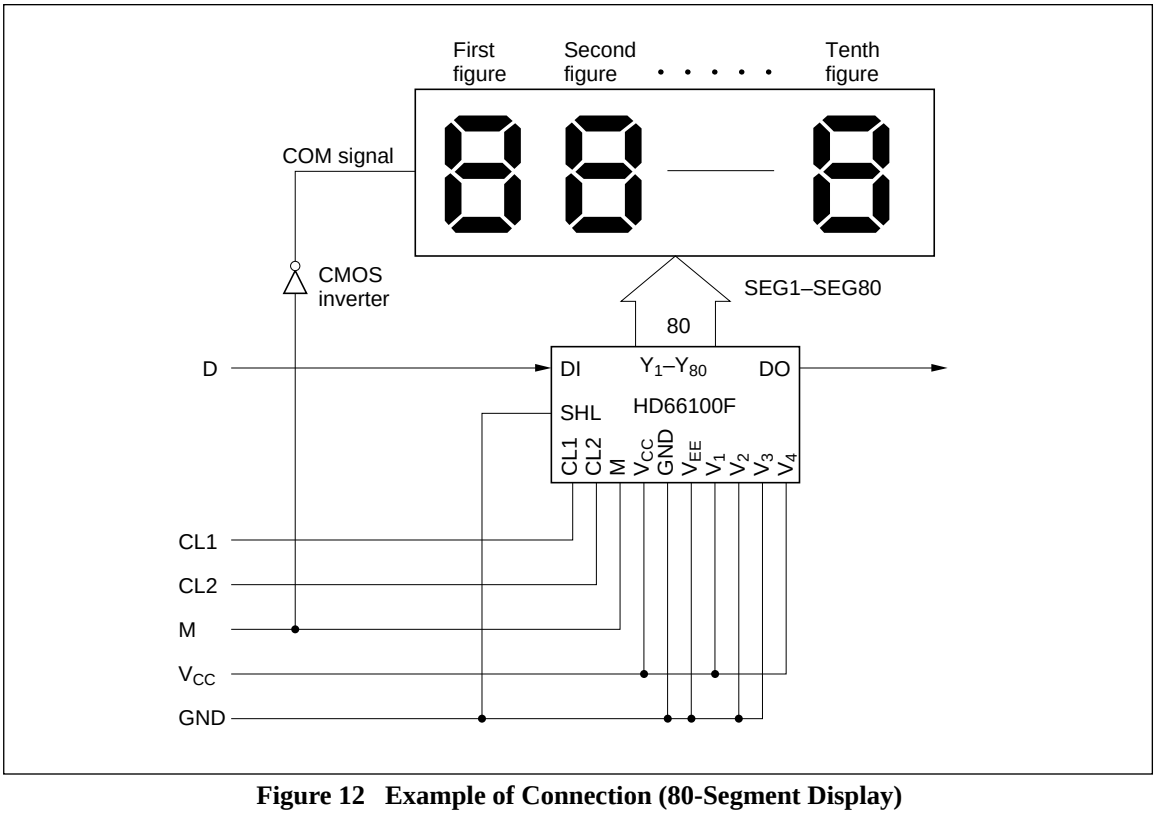


Figure 12 Example of Connection (80-Segment Display)

Timing Chart of Input Waveforms

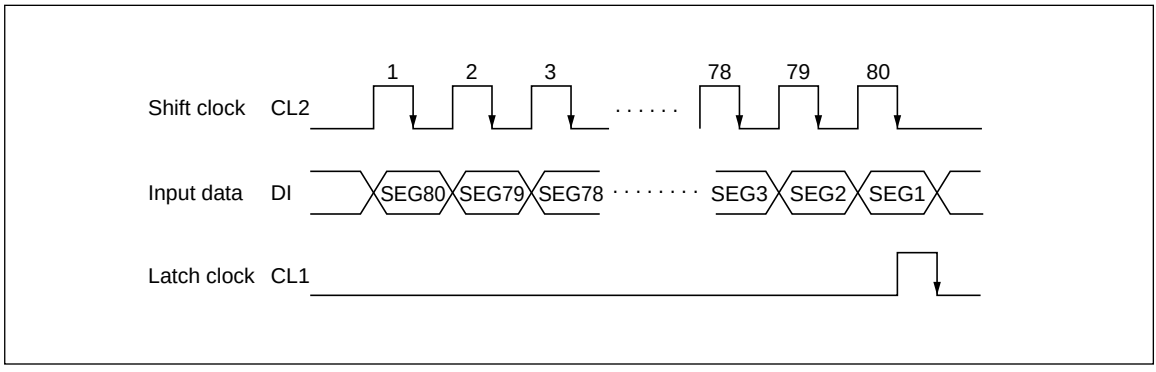


Figure 13 Timing Chart of Input Waveforms

Notes: 1. Input square waves of 50% duty cycle (about 30–500 Hz) to M. The frequency depends on the specifications of LCD panels.

2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, make CL1 fall synchronously with the one edge of M.

3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)

   Usually, one of the HD66100F outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

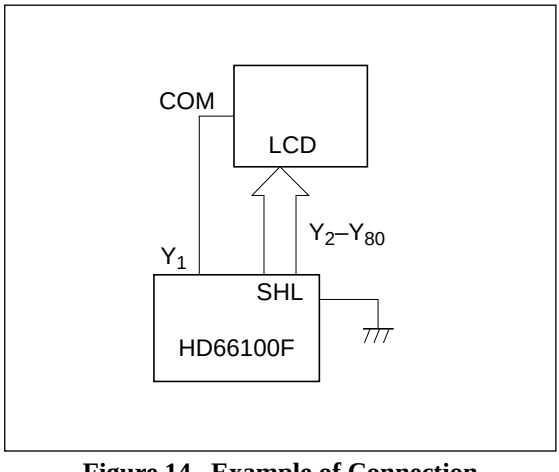


Figure 14 Example of Connection

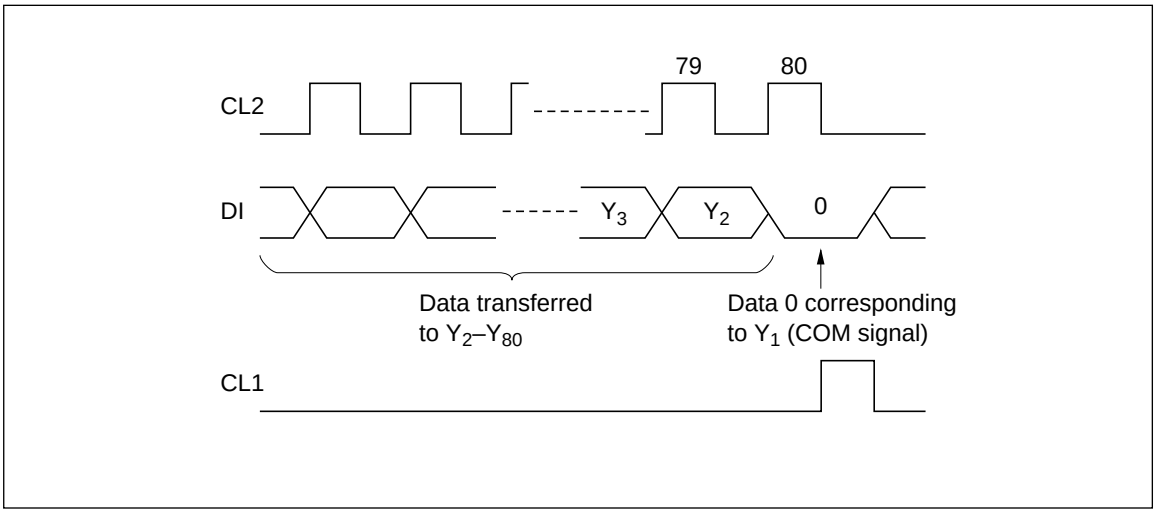


Figure 15 Timing Chart (when Y_1 is Used as a COM Signal)

HD61100A

(LCD Driver with 80-Channel Outputs)

HITACHI

Description

The HD61100A is a driver LSI for liquid crystal display systems. It receives serial display data from a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

It has liquid crystal driving outputs which correspond to internal 80-bit flip/flops. Both static drive and dynamic drive are possible according to the combination of transfer clock frequency and latch clock frequency.

Features

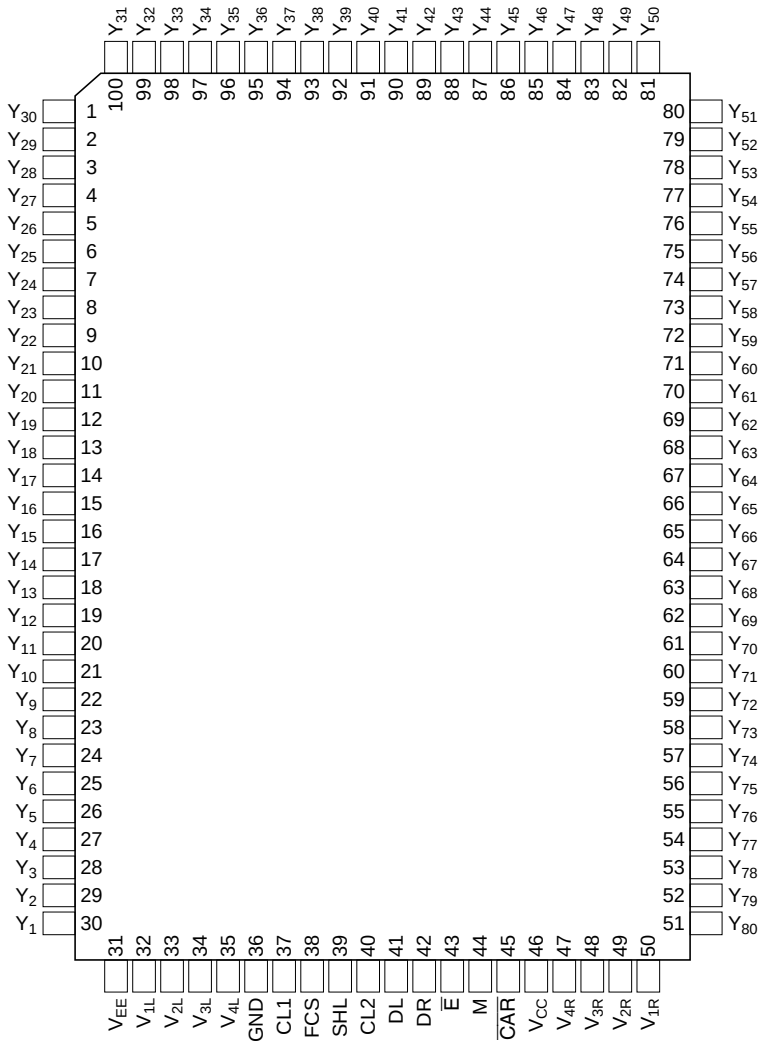
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Display duty cycle
  Any duty cycle is selectable according to combination of transfer clock and latch clock
- Data transfer rate: 2.5 MHz max.
- Power supply
  - — V_{CC}: +5.0 V ± 10% (internal logic)
  - — V_{CC}–V_{EE}: 5.5 to 17.0 V (liquid crystal display driver circuit)
- Liquid crystal driving level: 17.0 V max.
- CMOS process

Ordering Information

Type No.	Package
HD61100A	100-pin plastic QFP (FP-100)

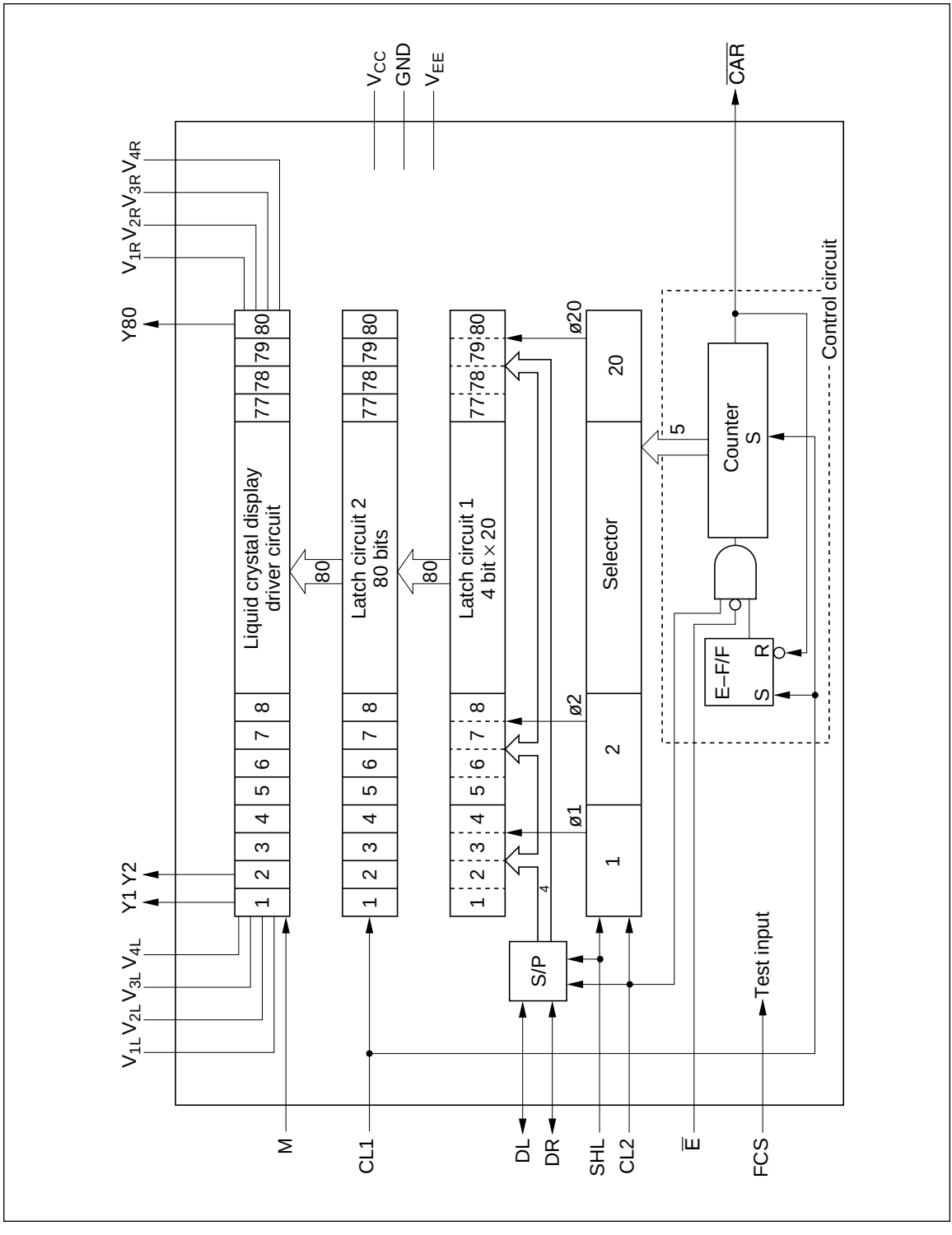
Hitachi semiconductor

Pin Arrangement



(Top view)

Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

80-Bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is “L” level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don’t connect any lines to terminal DR which is in the output status.

When SHL is “H” level, input data from terminal DR without connecting any lines to terminal DL.

80-Bit Latch Circuit 1

The 4-bit data is latched at ø1 to ø20 and output to latch circuit 2. When SHL is “L” level, the data from DL are latched one in order of 1 → 2 → 3 → ... 80 of each latch. When SHL is “H” level, they are latched in a reverse order (80 → 79 → 78 → ... 1).

Selector

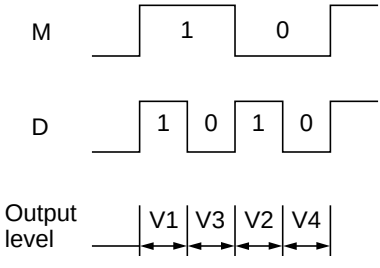
The selector decodes output signals from the counter and generates latch clock ø1 to ø20. When the LSI is not active, ø1 to ø20 are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E—F/F (enable F/F) indicates “1”, S/P conversion is started by inputting “L” level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into “L” level and E—F/F is reset to “0”, and consequently the conversion stops. E—F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at “H” level of CL1.

Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into “H” level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61100A.

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}–V_{4L} V_{1R}–V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1–Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger). Liquid crystal driver signals corresponding to the display data are output synchronized with the fall of CL1.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge trigger.
DL, DR	2	I/O	Controller	Input of serial display data (D). **(D) / Liquid Crystal Driver Output / Liquid Crystal Display** 1 (high) / Selection level / On 0 (low) / Non-selection level / Off I/O status of DL and DR terminals depends on SHL input level. **SHL / DL / DR** High / O / I Low / I / O

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of serial data.

When the serial data (D) is input in order of D1 → ... → D80, the relations between the data (D) and output Y are as follows.

<table><tr><th>SHL</th><th>Y1</th><th>Y2</th><th>Y3</th><th>...</th><th>Y80</th></tr><tr><td>Low</td><td>D1</td><td>D2</td><td>D3</td><td>...</td><td>D80</td></tr><tr><td>High</td><td>D80</td><td>D79</td><td>D78</td><td>...</td><td>D1</td></tr></table>
When SHL is low, data is input from the terminal DL. No lines should be connected to the terminal DR, as it is in the output state.

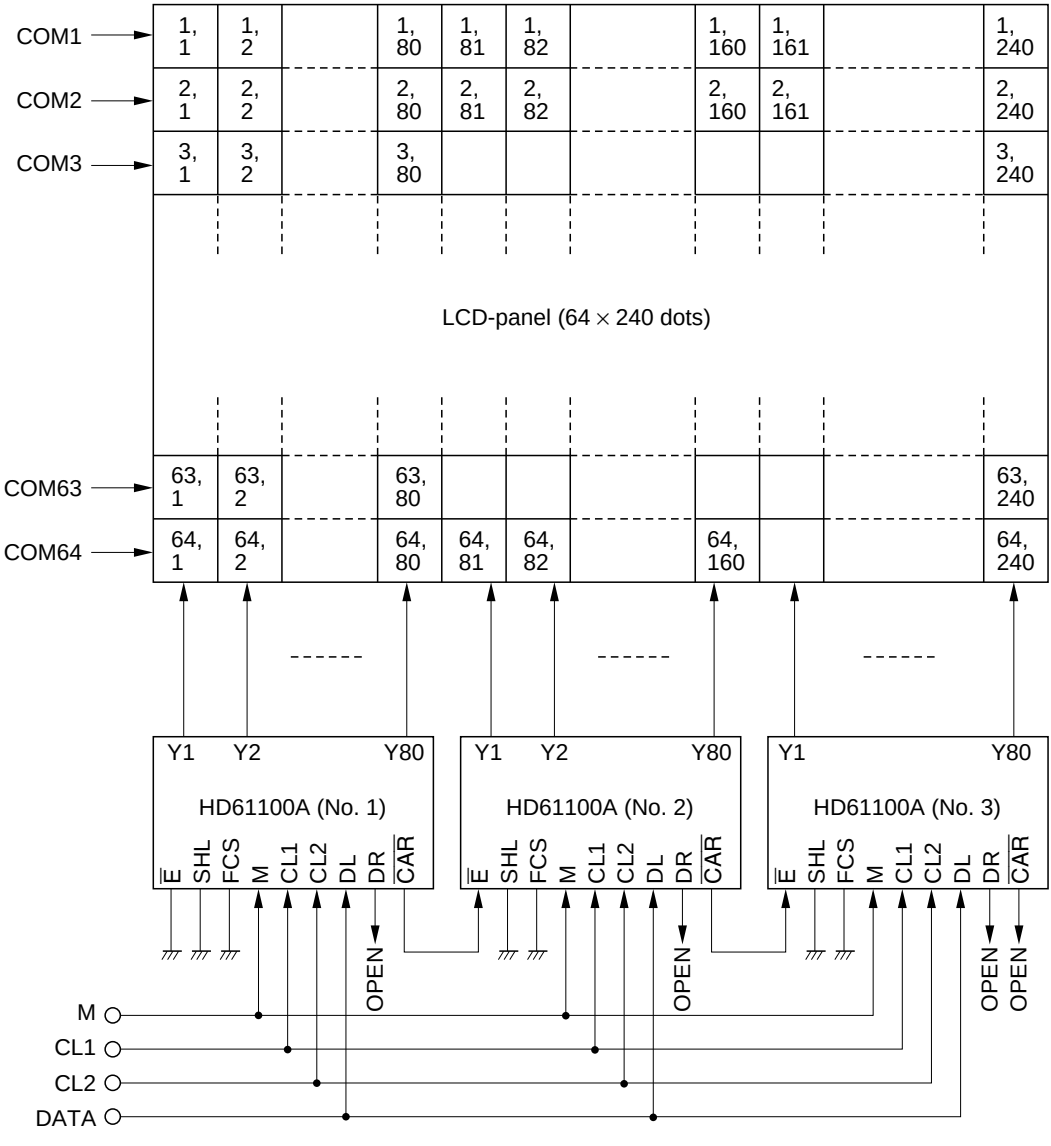
When SHL is high, the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61100A</td><td>Controls the S/P conversion.

The operation stops when $\overline{E}$ is high, and the S/P conversion starts when $\overline{E}$ is low.</td></tr>
<tr><td>$\overline{CAR}$</td><td>1</td><td>O</td><td>Input terminal $\overline{E}$ of the HD61100A</td><td>Used for cascade connection with the HD61100A to increase the number of bits which can be S/P converted.</td></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>GND</td><td>Input terminal for test.

Connect to GND.</td></tr>
</table>

Operation of the HD61100A

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61100A's. Figure 2 is a time chart of HD61100A I/O signals.



Cascade three HD61100As. Input data to the terminal DL of No. 1, No. 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don't connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61103A. (m, n) in LCD panel is the address corresponding to each dot. Timing chart for the example of connection, DL input (m, n) in this figure is the data that corresponds to each address (m, n) of LCD panel.

Figure 1 LCD Driver with 64 × 240 Dots

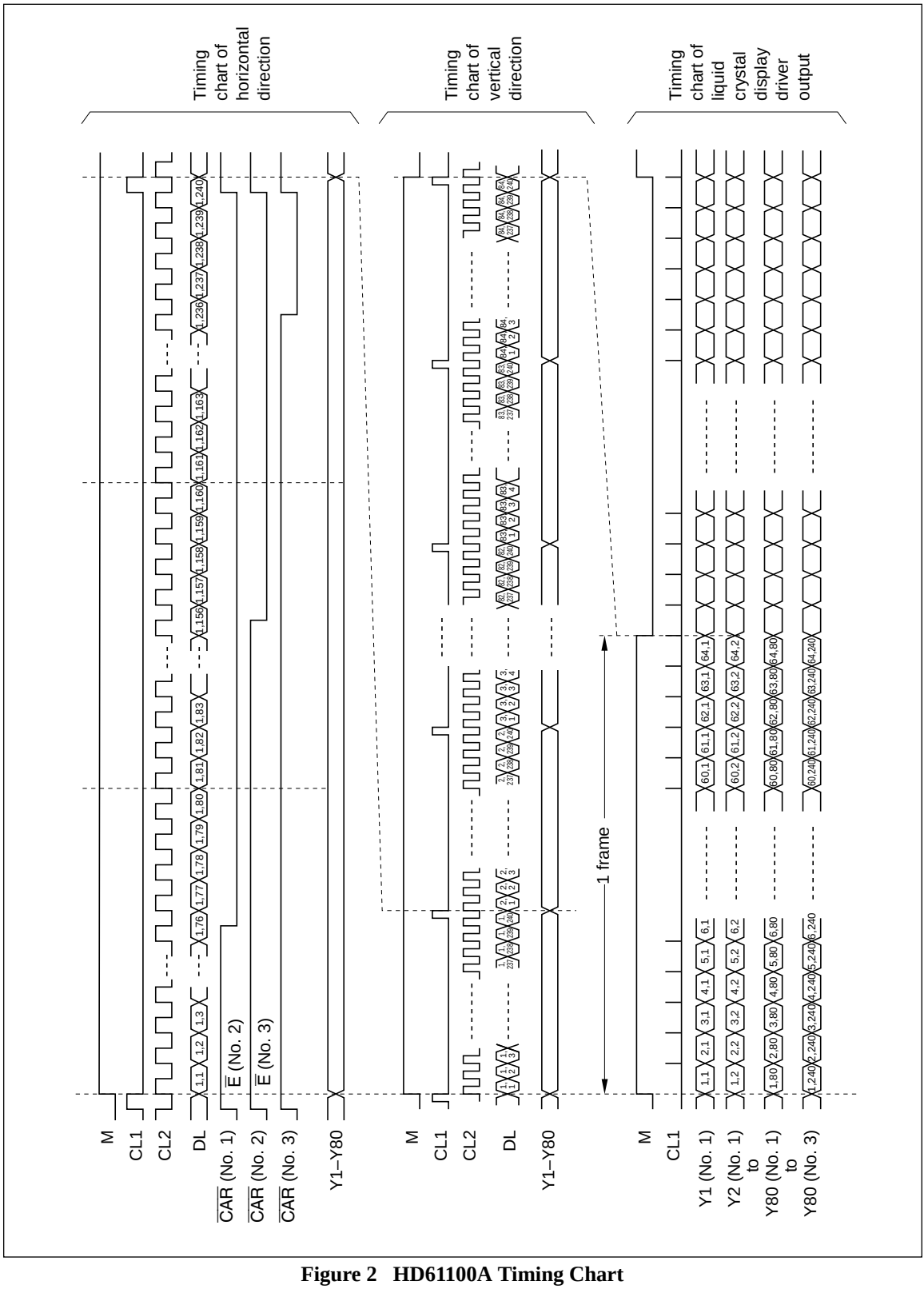


Figure 2 HD61100A Timing Chart

Application Examples

An Example of 128 × 240 Dot Liquid Crystal Display (1/64 Duty Cycle)

The liquid crystal panel (figure 3) is divided into upper and lower parts. These two parts are driven separately. HD61100As No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ of No. 3 in the order in which they were input (in the case of SHL = low). HD61100As No. 4 to No. 6 drive the lower half. Serial data, which are input from the DATA(2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 6 in the order in which they were input (in the case of SHL = high). As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

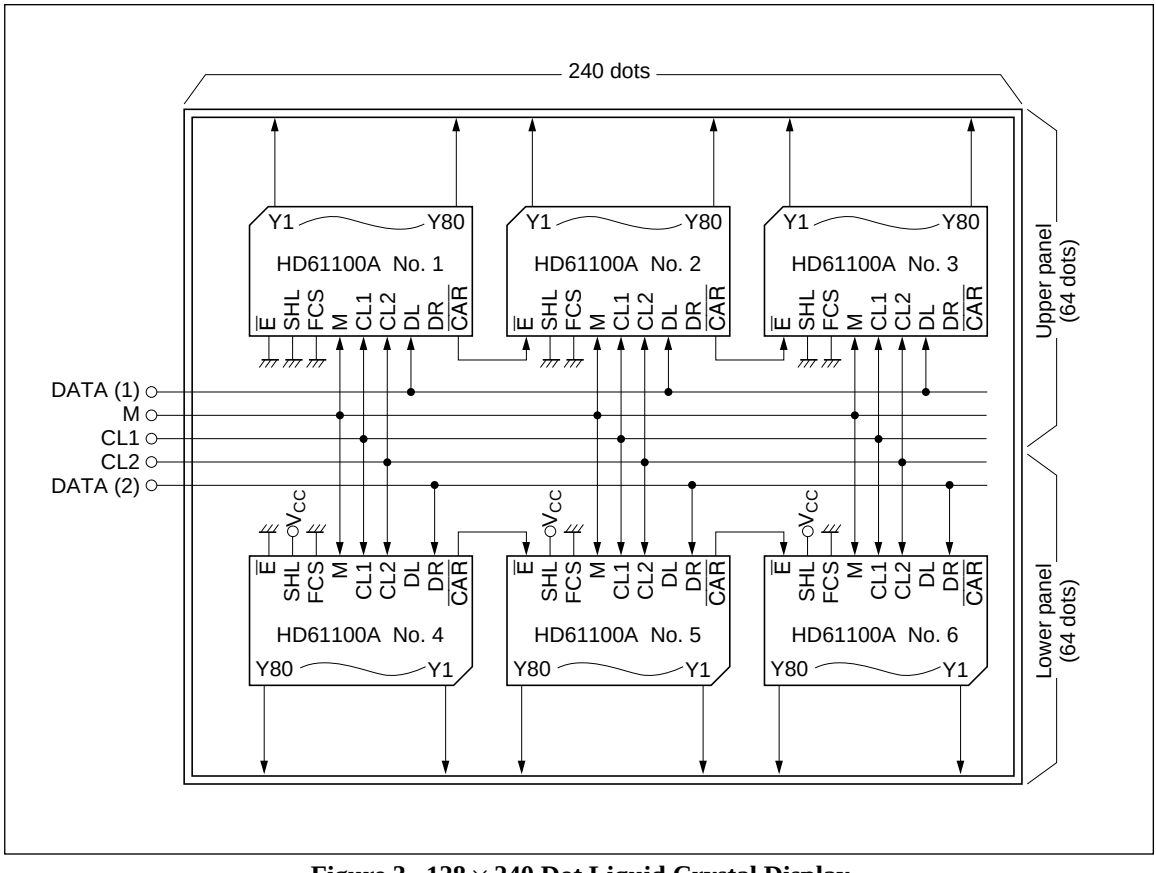


Figure 3 128 × 240 Dot Liquid Crystal Display

Example of 64 × 150 Dot Liquid Crystal Display (1/64 Duty Cycle, SHL = Low)

4-bit parallel process is used in this LSI to lessen the power dissipation.

Thus, the sum of the dots in horizontal direction should be multiple of 4.

If not, as this example (figure 4), consideration is needed for input signals (figure 5).

As the sum of dots in lateral direction is 150, 2 more dummy data bits are transferred (152 = 4 × 38).

Dummy data, which is output from Y71 and Y72 of No. 2, can be either 0 or 1 because these terminals do not connect with the liquid crystal display panel.

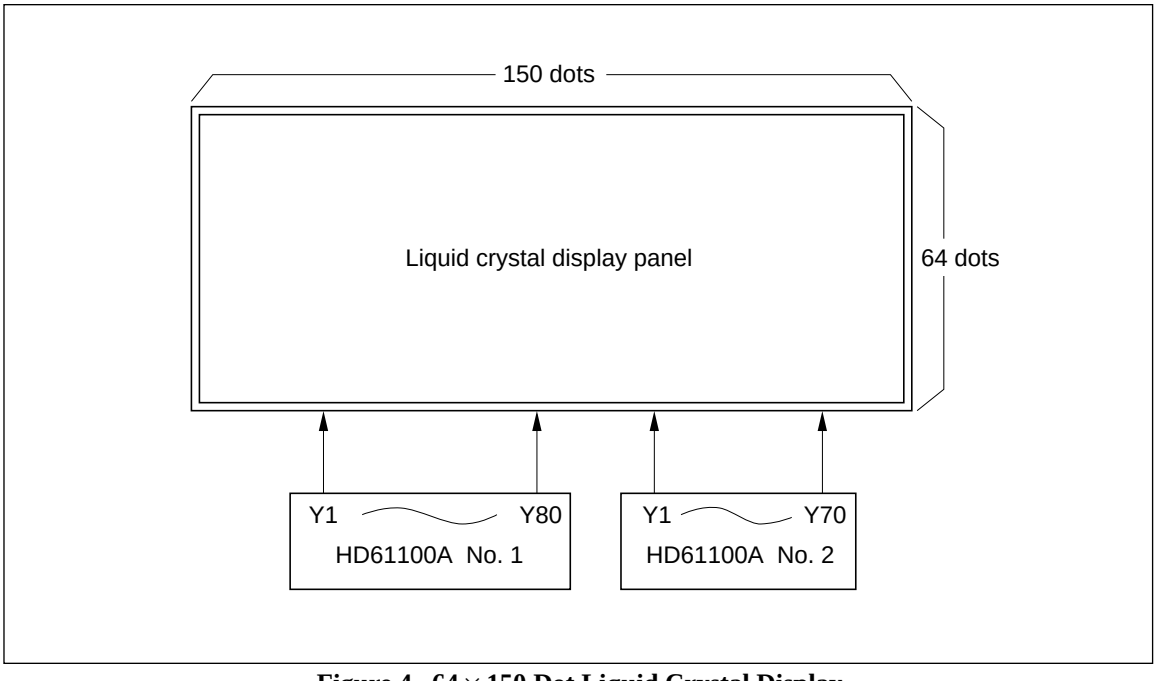


Figure 4 64 × 150 Dot Liquid Crystal Display

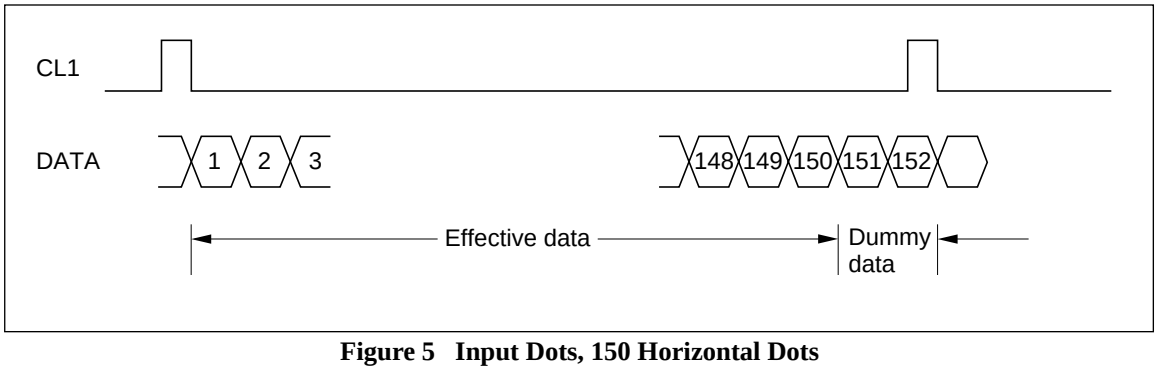


Figure 5 Input Dots, 150 Horizontal Dots

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using it beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referred to GND = 0 V.

3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, E, and M.

4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain:
   $V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$.
   Connect a protection resistor of 15 Ω ± 10% to each terminals in series.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, $V_{CC} - V_{EE}$ = 5.5 to 17 V, Ta = –20 to +75°C)

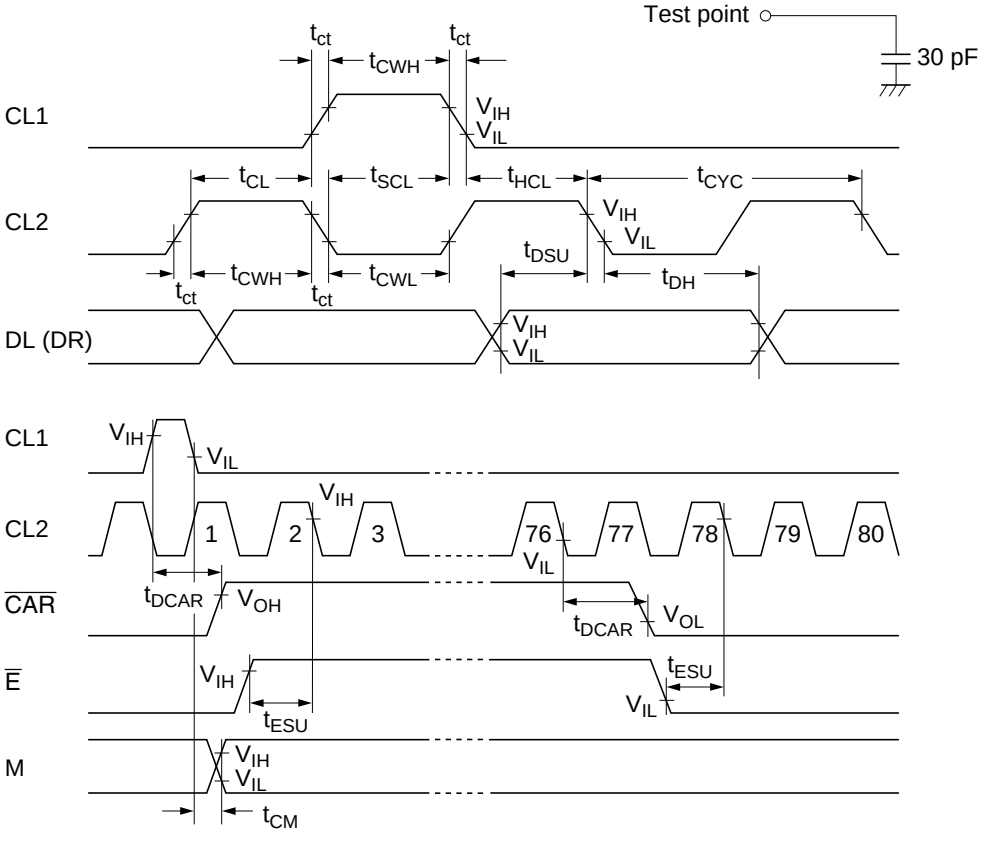
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	0	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = +400 µA	2
Driver resistance	R_{ON}	—	—	7.5	kΩ	V_{EE} = –10 V, load current = 100 µA	3
Input leakage current	I_{IL1}	–1	—	+1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–2	—	+2	µA	V_{IN} = V_{EE} to V_{CC}	4
Dissipation current (1)	I_{GND}	—	—	1.0	mA		5
Dissipation current (2)	I_{EE}	—	—	0.1	mA		5

Notes: 1. Applies to CL1, CL2, FCS, SHL, $\overline{E}$, M, DL, and DR.
2. Applies to DL, DR, and $\overline{CAR}$.
3. Applies to Y1–Y80.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
5. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)
   Specified when $V_{IH} = V_{CC}$, V_{IL} = GND and no load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.

AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 5.5 to 17 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{Ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
$\overline{E}$ setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuits are connected for specification:



HD61200

(LCD Driver with 80-Channel Outputs)

HITACHI

Description

The HD61200 is a column driver LSI for a large-area dot matrix LCD. It employs 1/32 or more duty cycle multiplexing method. It receives serial display data from a micro controller or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

Features

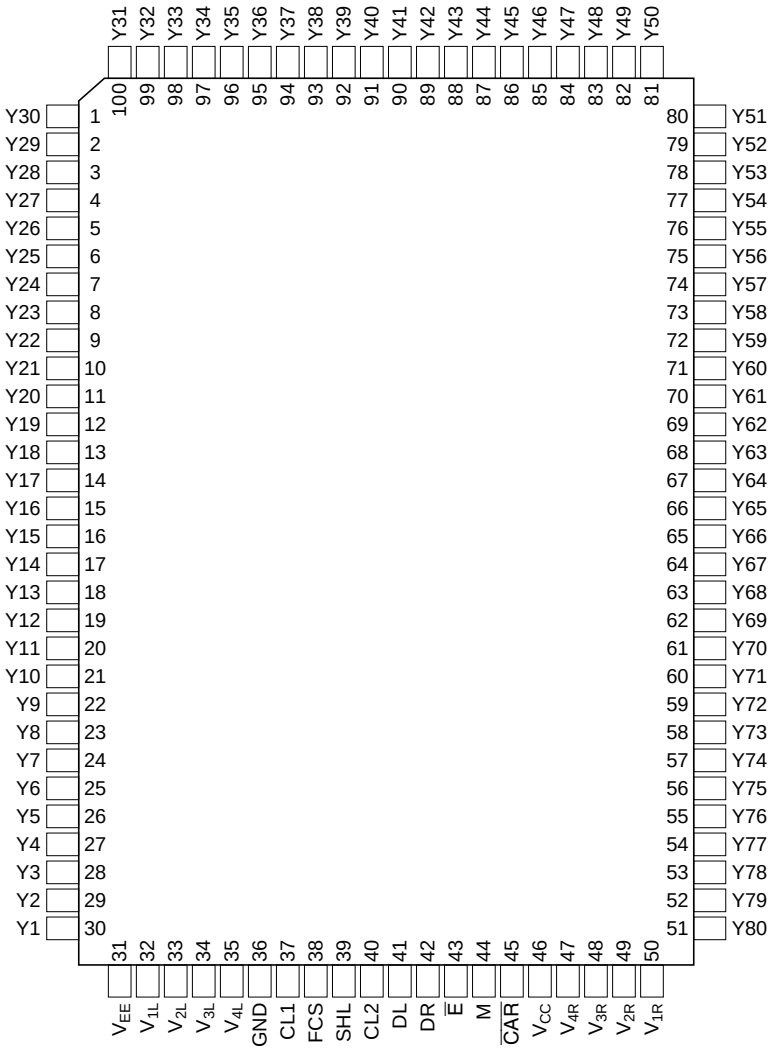
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Drives liquid crystal panels with 1/32–1/128 duty cycle multiplexing
- Can interface to LCD controllers, HD61830 and HD61830B
- Data transfer rate: 2.5 MHz max
- Power supply: V_{CC}: 5 V ± 10% (internal logic)
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process

Ordering Information

Type No.	Package
HD61200	100-pin plastic QFP (FP-100)

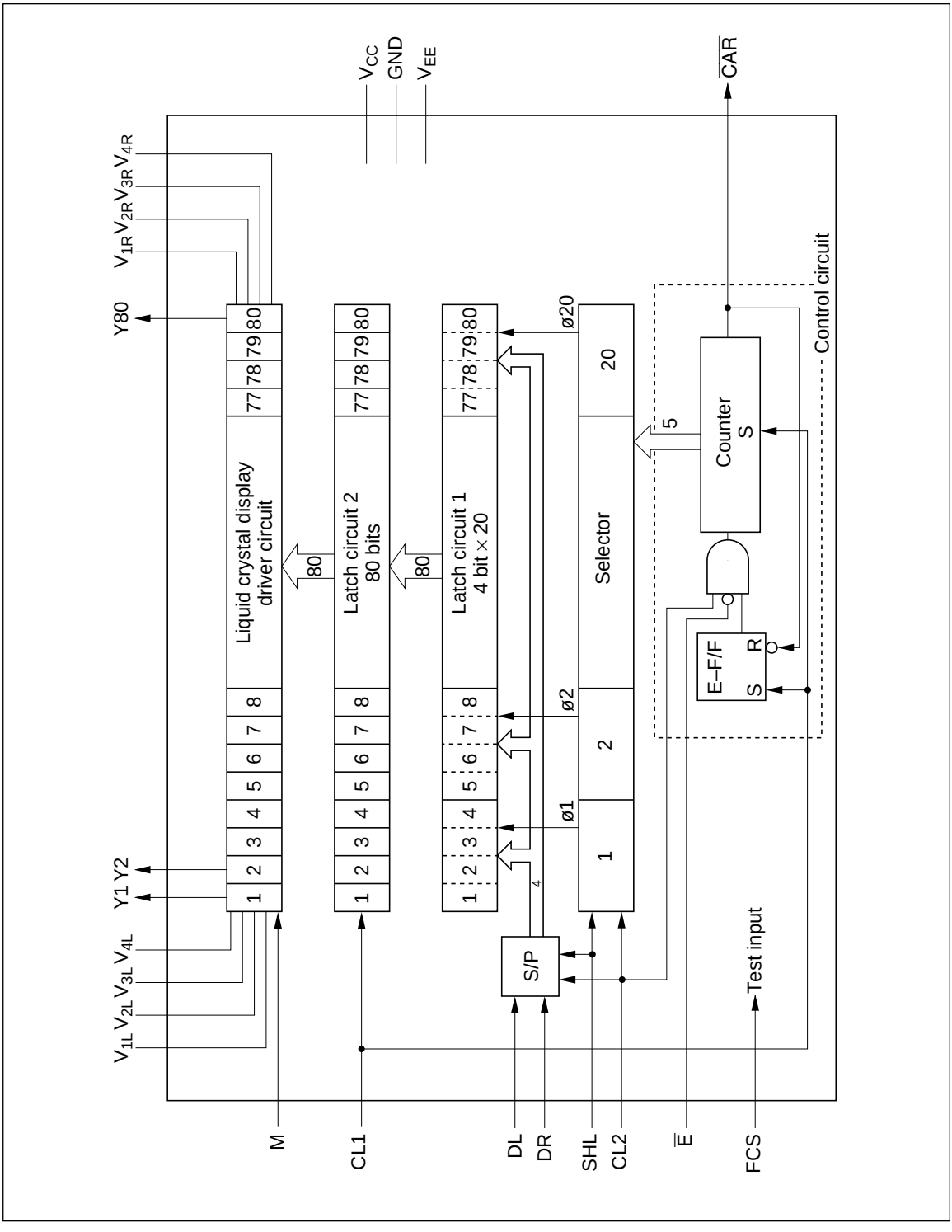
Hitachi semiconductor

Pin Arrangement



(Top view)

Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

80-Bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is low level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR.

When SHL is high level, input data from terminal DR without connecting any lines to terminal DL.

80-Bit Latch Circuit 1

The 4-bit data is latched at ø1 to ø20 and output to latch circuit 2. When SHL is low level, the data from DL are latched in order of 1 → 2 → 3 → ... 80 of each latch. When SHL is high level, they are latched in a reverse order (80 → 79 → 78 → ... 1).

Selector

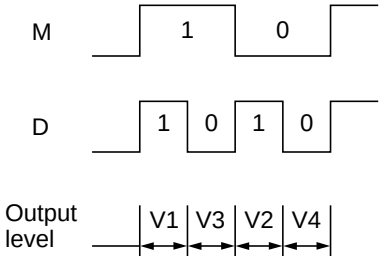
The selector decodes output signals from the counter and generates latch clock ø1 to ø20. When the LSI is not active, ø1 to ø20 are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E–F/F (enable F/F) indicates 1, S/P conversion is started by inputting low level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into low level and E–F/F is reset to 0, and consequently the conversion stops. E–F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at high level of CL1.

The counter consists of 7 bits, and the output signals upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into high level at the rise of CL1. The number of bits that can be S/P-converted can be increased by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61200.

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}–V_{4L} V_{1R}–V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1–Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M, and display data (D) is as follows: 
M	1	1	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Synchronous signal (a counter is reset at high level). Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
DL, DR	2	I	Controller	Input of serial display data (D).

(D)	Liquid Crystal Driver Output	Liquid Crystal Display
1 (high level)	Selection level	On
0 (low level)	Non-selection level	Off

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects the shift direction of serial data.

When the serial data (D) is input in order of D1 → ... → D80, the relations between the data (D) and output Y are as follows:

<table><tr><th>SHL</th><th>Y1</th><th>Y2</th><th>Y3</th><th>...</th><th>Y80</th></tr><tr><td>Low</td><td>D1</td><td>D2</td><td>D3</td><td>...</td><td>D80</td></tr><tr><td>High</td><td>D80</td><td>D79</td><td>D78</td><td>...</td><td>D1</td></tr></table>
When SHL is low, data is input from the DL terminal. No lines should be connected to the DR terminal.

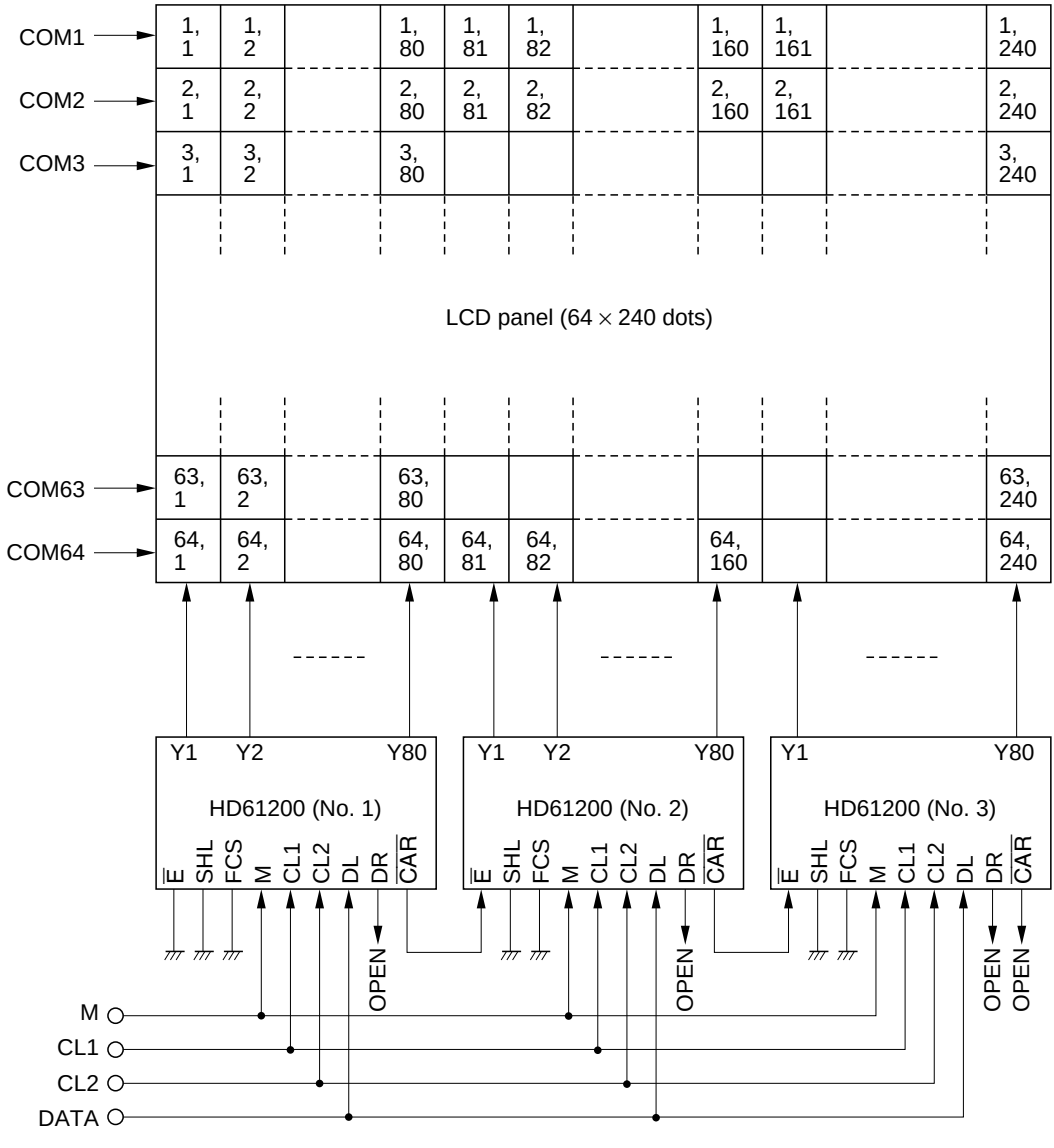
When SHL is high, the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61200</td><td>Controls the S/P conversion.

The operation stops on high level, and the S/P conversion starts on low level.</td></tr>
<tr><td>$\overline{CAR}$</td><td>1</td><td>O</td><td>Input terminal $\overline{E}$ of the HD61200</td><td>Used for cascade connection with the HD61200 to increase the number of bits that can be S/P converted.</td></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>GND</td><td>Input terminal for test.

Connect to GND.</td></tr>
</table>

Operation of the HD61200

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61200s. Figure 2 is a time chart of HD61200 I/O signals.



Cascade three HD61200s. Input data to the DL terminal of No. 1, No. 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don't connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61203. (m, n) of LCD panel is the address corresponding to each dot. Timing chart for the example of connection, DL input (m, n) in this figure is the data that corresponds to each address (m, n) of LCD panel.

Figure 1 LCD Driver with 64 × 240 Dots

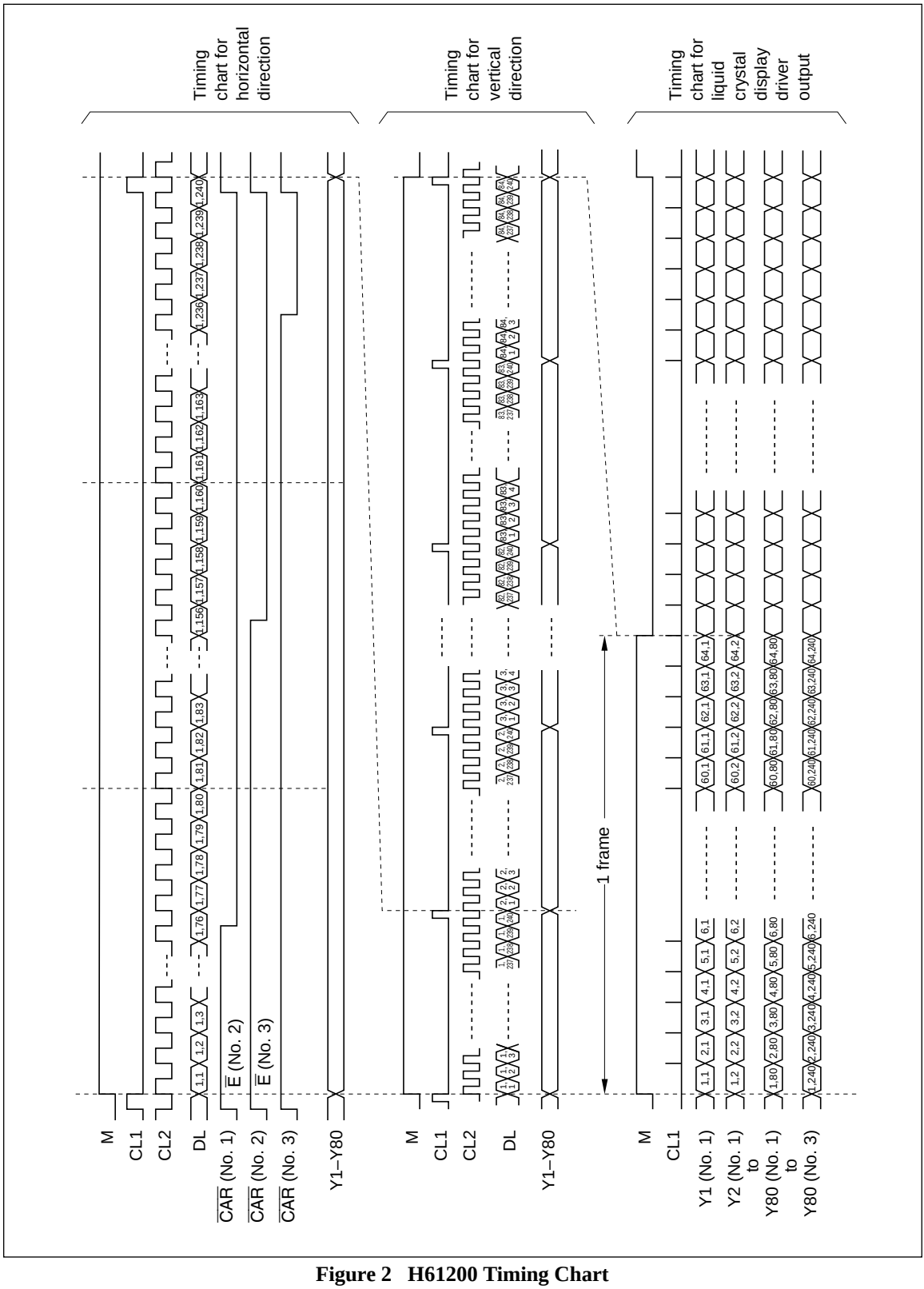


Figure 2 H61200 Timing Chart

Application Example

The liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61200s No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ of No. 3 in the order in which they were input (in the case of SHL = low). HD61200s No. 4 to No. 6 drive the lower half. Serial data, which are input from DATA(2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 6 in the order in which they were input (in the case of SHL = high).

As shown in this example, a PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

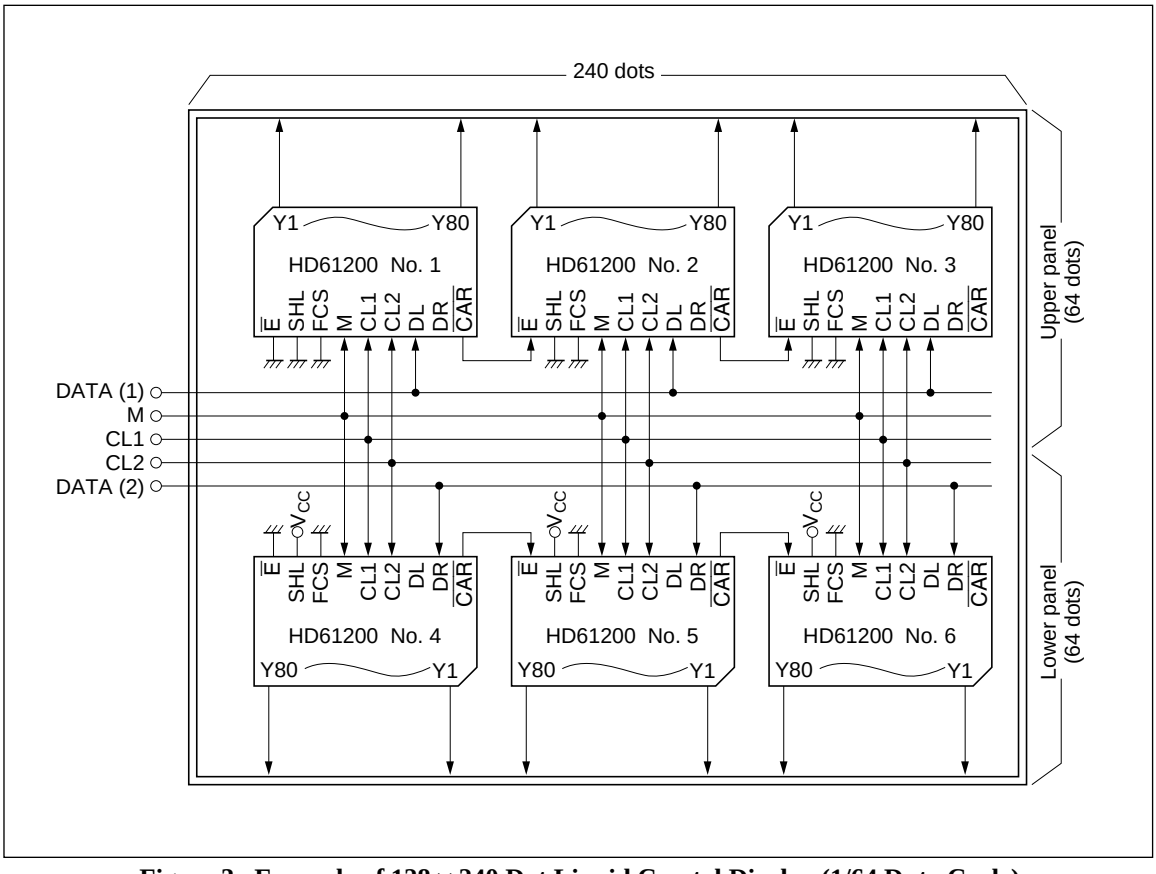


Figure 3 Example of 128 × 240 Dot Liquid Crystal Display (1/64 Duty Cycle)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referenced to GND = 0 V.

3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, E, and M.

4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}. Must maintain
$V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$.
Connect a protection resistor of 15 Ω ± 10% to each terminal in series.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, $V_{CC} - V_{EE}$ = 8 V to 17 V, Ta = –20 to 75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	0	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	2
Driver on resistance	R_{ON}	—	—	7.5	kΩ	Load current = 100 µA	5
Input leakage current	I_{IL1}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–2	—	2	µA	V_{IN} = V_{EE} to V_{CC}	3
Dissipation current (1)	I_{GND}	—	—	1.0	mA		4
Dissipation current (2)	I_{EE}	—	—	0.1	mA		4

Notes: 1. Applies to CL1, CL2, SHL, $\overline{E}$, M, DL, and DR.

2. Applies to $\overline{CAR}$.

3. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.

4. Specified when display data is transferred under following conditions:

   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)

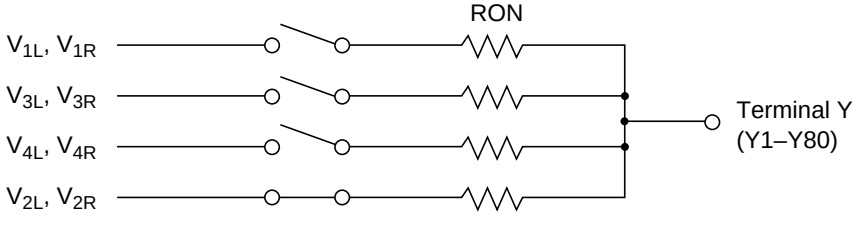
   Specified at $V_{IH} = V_{CC}$ (V), V_{IL} = 0 V and load on outputs.

   I_{GND}: currents between V_{CC} and GND.

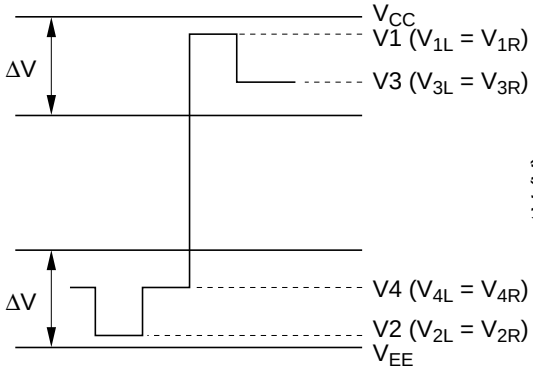
   I_{EE}: currents between V_{CC} and V_{EE}.

5. Resistance between terminal Y and terminal V (one of V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R} when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition:

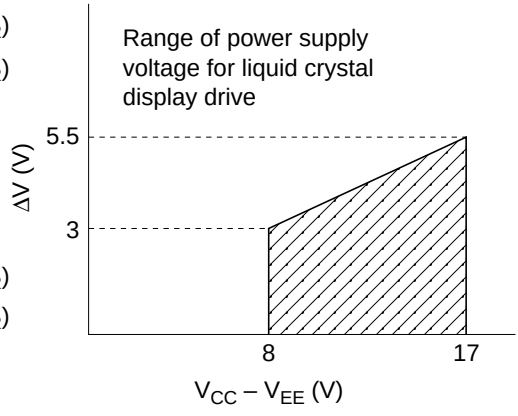
$$V_{CC} - V_{EE} = 17 \text{ V}$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{EE} + 2/7\ (V_{CC} - V_{EE})$$



The following here is a description of the range of power supply voltage for liquid crystal display drivers. Apply positive voltage to $V_{1L} = V_{1R}$ and $V_{3L} = V_{3R}$ and negative voltage to $V_{2L} = V_{2R}$ and $V_{4L} = V_{4R}$ within the ΔV range. This range allows stable impedance on driver output (RON). Notice the ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



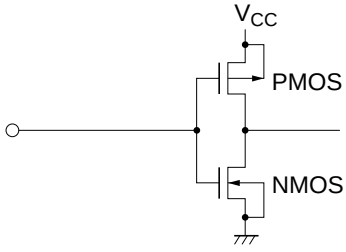
Correlation between driver output waveform and power supply voltage for liquid crystal display drive



Correlation between power supply voltage $V_{CC} - V_{EE}$ and ΔV

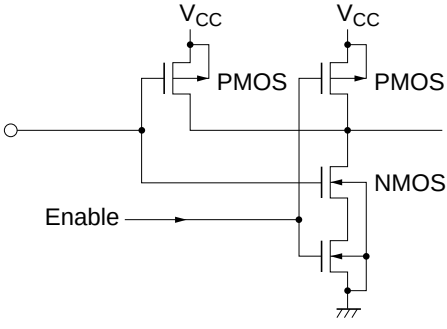
Terminal Configuration

Input Terminal

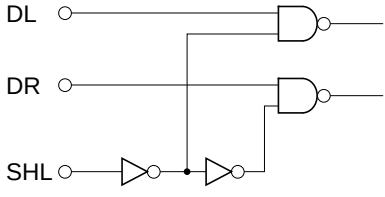


Applicable terminals:
CL1, CL2, SHL, $\overline{E}$, M

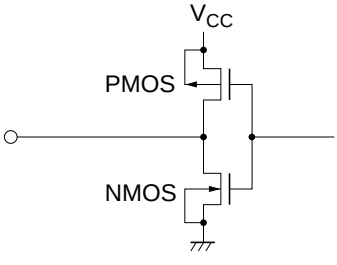
Input Terminal (With Enable)



Applicable terminals: DL, DR



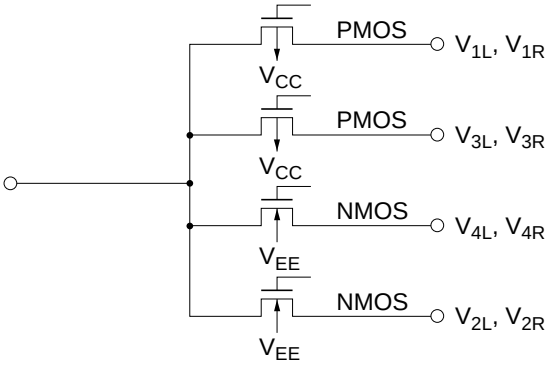
Output Terminal



Applicable terminal: $\overline{CAR}$

Output Terminal

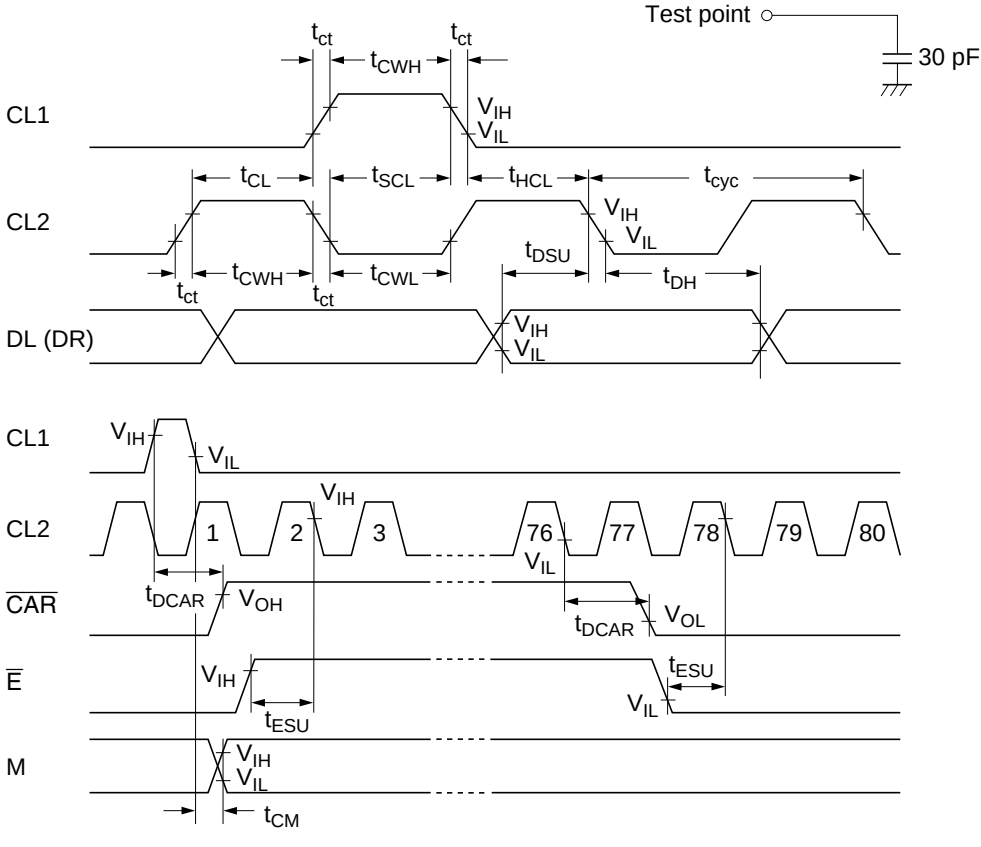
Applicable terminals:
Y1–Y80



AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{cyc}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
$\overline{E}$ setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuit is connected for specification:



HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7 V to 5.5 V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
  - 2.7 to 5.5 V
- Wide range of liquid crystal display driver power
  - 3.0 to 11 V
- Liquid crystal drive waveform
  - A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  - 2 MHz (when V_{CC} = 5 V)
- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  - 208 character fonts (5 × 8 dot)
  - 32 character fonts (5 × 10 dot)
- 64 × 8-bit character generator RAM
  - 8 character fonts (5 × 8 dot)
  - 4 character fonts (5 × 10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 × 8 dots with cursor
  - 1/11 for one line of 5 × 10 dots with cursor
  - 1/16 for two lines of 5 × 8 dots with cursor
- Wide range of instruction functions:
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

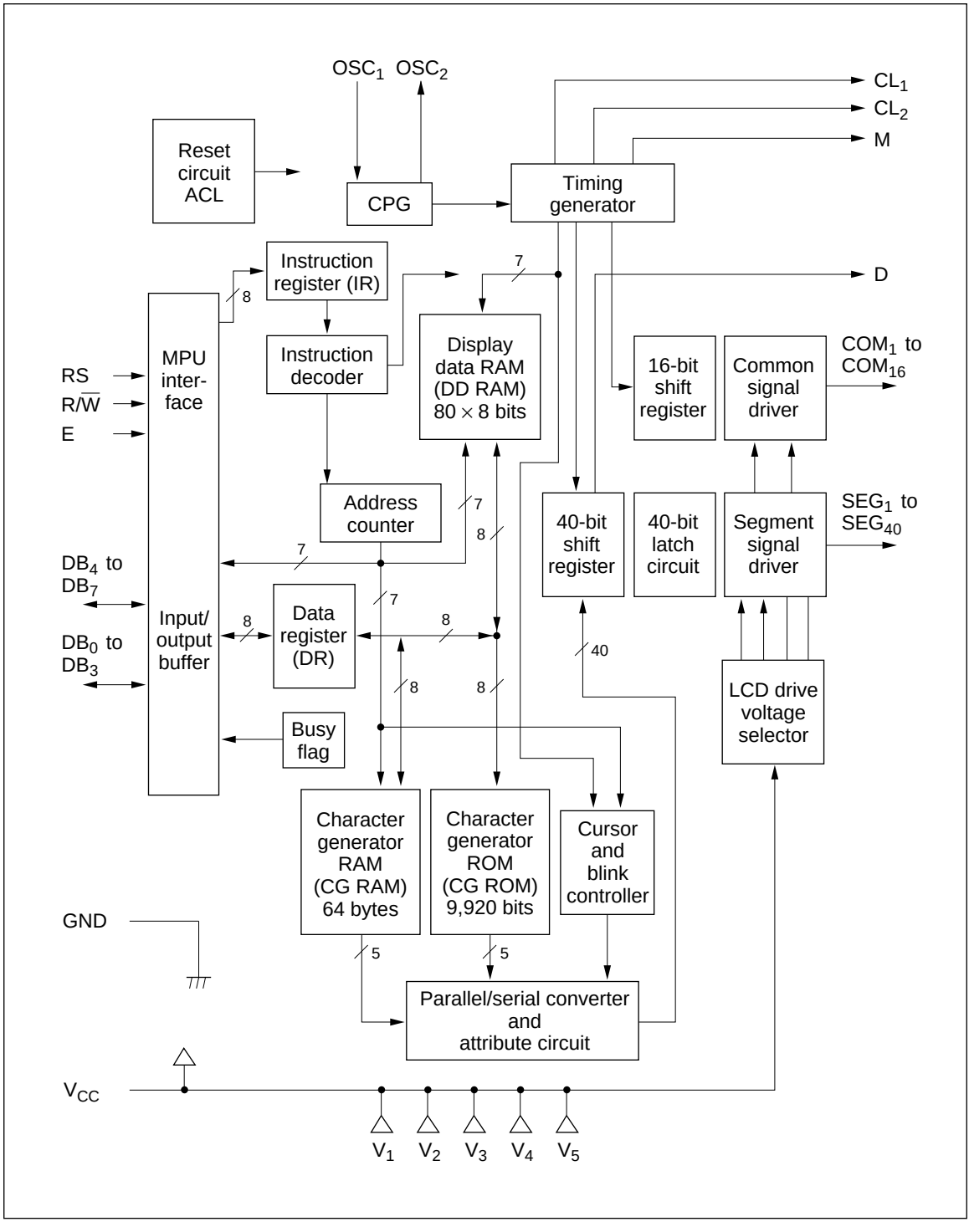
Hitachi semiconductor

Ordering Information

Type No.	Package	CG ROM
HD44780UA00FS	FP-80B	Japanese standard font
HCD44780UA00	Chip	
HD44780UA00TF	TFP-80	
HD44780UA01FS	FP-80B	Standard font for communication,
HD44780UA02FS	FP-80B	European standard font
HD44780UBxxFS	FP-80B	Custom font
HCD44780UBxx	Chip	
HD44780UBxxTF	TFP-80	

Note: xx: ROM code No.

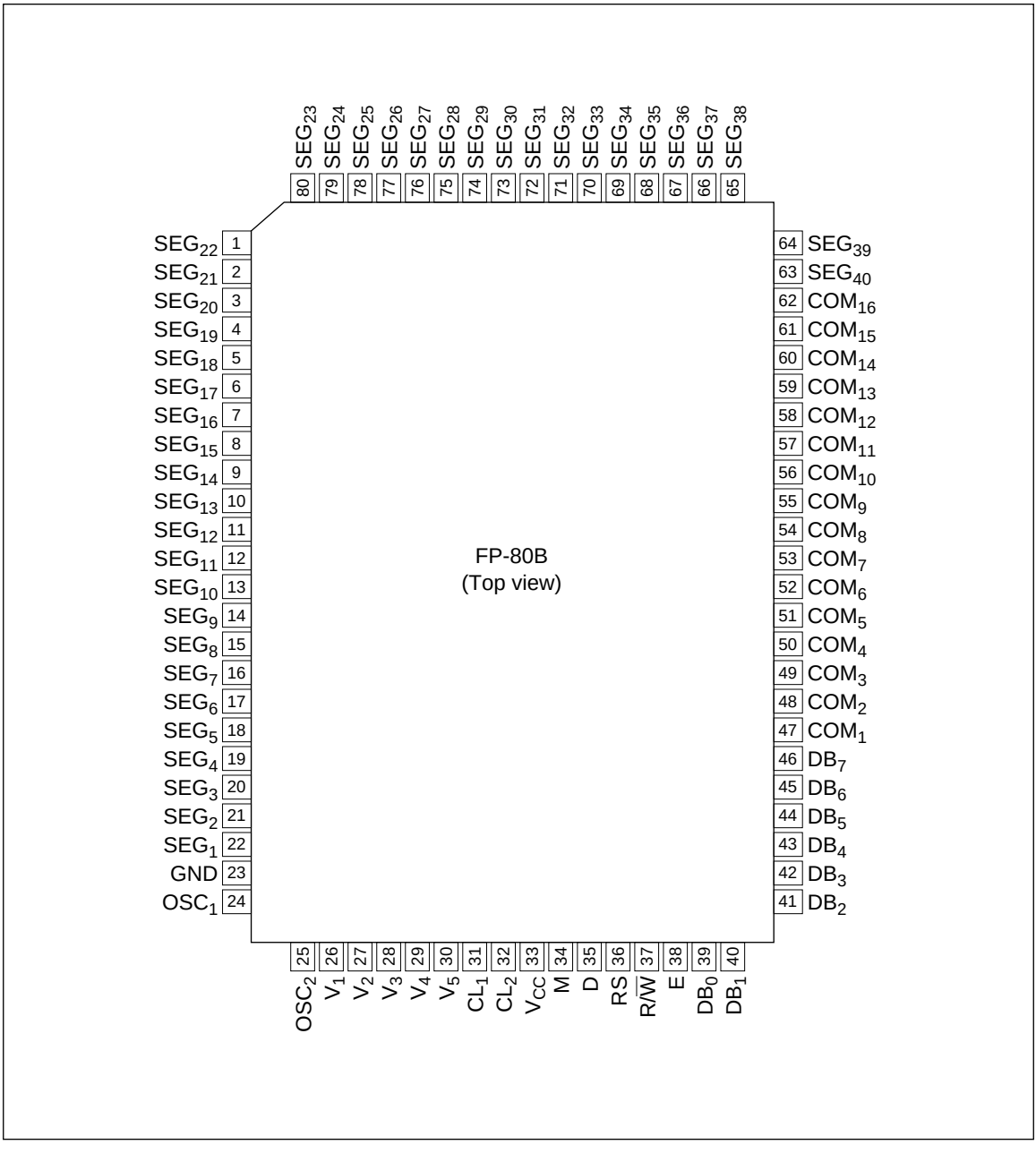
HD44780U Block Diagram



LCD-II Family Comparison

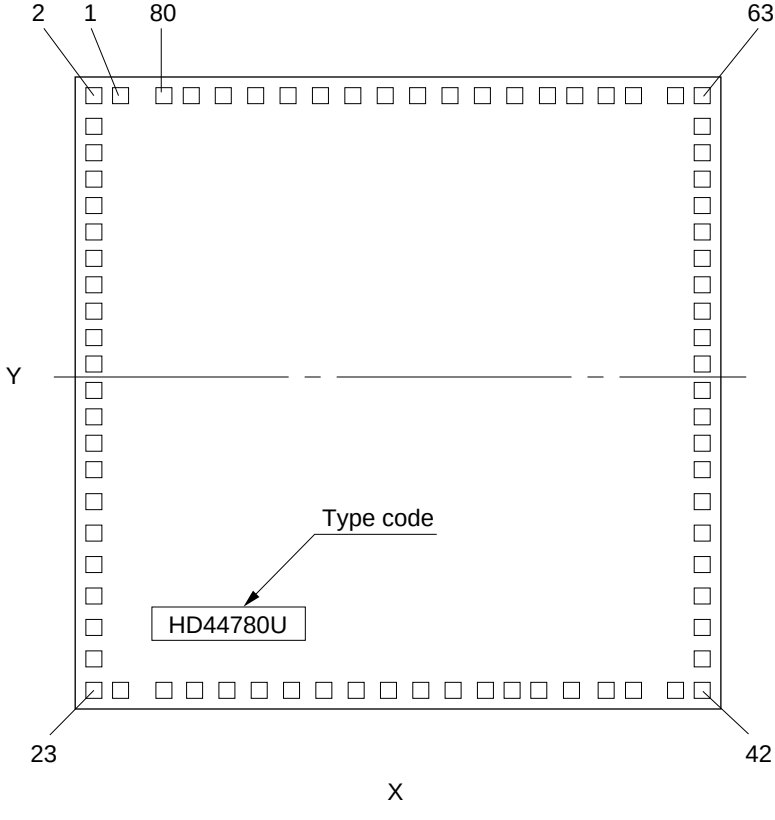
Item		HD44780S	HD44780U
Power supply voltage		5 V ±10%	2.7 to 5.5 V
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11.0 V	3.0 to 11.0 V
	1/5 bias	4.6 to 11.0 V	3.0 to 11.0 V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	16 digits (8 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)	9,920 bits (208 character fonts for 5 × 8 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes
DDRAM		80 bytes	80 bytes
Segment signals		40	40
Common signals		16	16
Liquid crystal drive waveform		A	A
Oscillator	Clock source	External resistor, external ceramic filter, or external clock	External resistor or external clock
	R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)
	R_f resistance	91 kΩ ±2%	91 kΩ ±2% (when V_{CC} = 5 V) 75 kΩ ±2% (when V_{CC} = 3 V)
Instructions		Fully compatible within the HD44780S	
CPU bus timing		1 MHz	1 MHz (when V_{CC} = 3 V) 2 MHz (when V_{CC} = 5 V)
Package		FP-80 FP-80A	FP-80B TFP-80

HD44780U Pin Arrangement



HD44780U Pad Arrangement

Chip size: 4.90×4.90 mm^2
Coordinate: Pad center (µm)
Origin: Chip center
Pad size: 114×114 µm^2



HCD44780U Pad Location Coordinates

Pad No.	Function	Coordinate X (um)	Coordinate Y (um)
1	SEG_{22}	–2100	2313
2	SEG_{21}	–2280	2313
3	SEG_{20}	–2313	2089
4	SEG_{19}	–2313	1833
5	SEG_{18}	–2313	1617
6	SEG_{17}	–2313	1401
7	SEG_{16}	–2313	1186
8	SEG_{15}	–2313	970
9	SEG_{14}	–2313	755
10	SEG_{13}	–2313	539
11	SEG_{12}	–2313	323
12	SEG_{11}	–2313	108
13	SEG_{10}	–2313	–108
14	SEG_{9}	–2313	–323
15	SEG_{8}	–2313	–539
16	SEG_{7}	–2313	–755
17	SEG_{6}	–2313	–970
18	SEG_{5}	–2313	–1186
19	SEG_{4}	–2313	–1401
20	SEG_{3}	–2313	–1617
21	SEG_{2}	–2313	–1833
22	SEG_{1}	–2313	–2073
23	GND	–2280	–2290
24	OSC_{1}	–2080	–2290
25	OSC_{2}	–1749	–2290
26	V_{1}	–1550	–2290
27	V_{2}	–1268	–2290
28	V_{3}	–941	–2290
29	V_{4}	–623	–2290
30	V_{5}	–304	–2290
31	CL_{1}	–48	–2290
32	CL_{2}	142	–2290
33	V_{CC}	309	–2290
34	M	475	–2290
35	D	665	–2290
36	RS	832	–2290
37	R/$\overline{W}$	1022	–2290
38	E	1204	–2290
39	DB_{0}	1454	–2290
40	DB_{1}	1684	–2290
41	DB_{2}	2070	–2290
42	DB_{3}	2260	–2290
43	DB_{4}	2290	–2099
44	DB_{5}	2290	–1883
45	DB_{6}	2290	–1667
46	DB_{7}	2290	–1452
47	COM_{1}	2313	–1186
48	COM_{2}	2313	–970
49	COM_{3}	2313	–755
50	COM_{4}	2313	–539
51	COM_{5}	2313	–323
52	COM_{6}	2313	–108
53	COM_{7}	2313	108
54	COM_{8}	2313	323
55	COM_{9}	2313	539
56	COM_{10}	2313	755
57	COM_{11}	2313	970
58	COM_{12}	2313	1186
59	COM_{13}	2313	1401
60	COM_{14}	2313	1617
61	COM_{15}	2313	1833
62	COM_{16}	2313	2095
63	SEG_{40}	2296	2313
64	SEG_{39}	2100	2313
65	SEG_{38}	1617	2313
66	SEG_{37}	1401	2313
67	SEG_{36}	1186	2313
68	SEG_{35}	970	2313
69	SEG_{34}	755	2313
70	SEG_{33}	539	2313
71	SEG_{32}	323	2313
72	SEG_{31}	108	2313
73	SEG_{30}	–108	2313
74	SEG_{29}	–323	2313
75	SEG_{28}	–539	2313
76	SEG_{27}	–755	2313
77	SEG_{26}	–970	2313
78	SEG_{25}	–1186	2313
79	SEG_{24}	–1401	2313
80	SEG_{23}	–1617	2313

Pin Functions

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write
DB_4 to DB_7	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB_7 can be used as a busy flag.
DB_0 to DB_3	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.
CL_1	1	O	HD44100	Clock to latch serial data D sent to the HD44100 driver
CL_2	1	O	HD44100	Clock to shift serial data D
M	1	O	HD44100	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	HD44100	Character pattern data corresponding to each segment signal
COM_1 to COM_{16}	16	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM_9 to COM_{16} are non-selection waveforms at 1/8 duty factor and COM_{12} to COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1 to SEG_{40}	40	O	LCD	Segment signals
V_1 to V_5	5	—	Power supply	Power supply for LCD drive $V_{CC} - V_5 = 11$ V (max)
V_{CC}, GND	2	—	Power supply	V_{CC}: 2.7 V to 5.5 V, GND: 0 V
OSC_1, OSC_2	2	—	Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC_1.

Function Description

Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM and temporarily stores data to be read from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into DD RAM or CG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM or CG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 1).

Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (table 1), the busy flag is output to DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DD RAM and CG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DD RAM or CG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM or CG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 1).

Table 1 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)

  — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See figure 3.

  When the display shift operation is performed, the DD RAM address shifts. See figure 3.

  — Case 2: For a 16-character display, the HD44780 can be extended using one HD44100 and displayed. See figure 4.

  When the display shift operation is performed, the DD RAM address shifts. See figure 4.

  — Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased through the use of two or more HD44100s can be considered as an extension of case #2.

  Since the increase can be eight digits per additional HD44100, up to 80 digits can be displayed by externally connecting nine HD44100s. See figure 5.

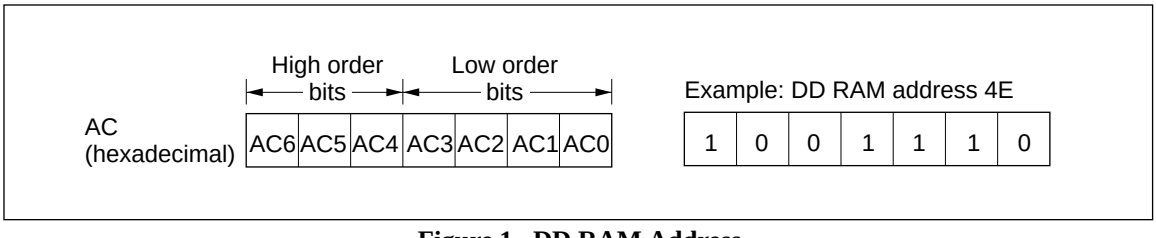


Figure 1 DD RAM Address

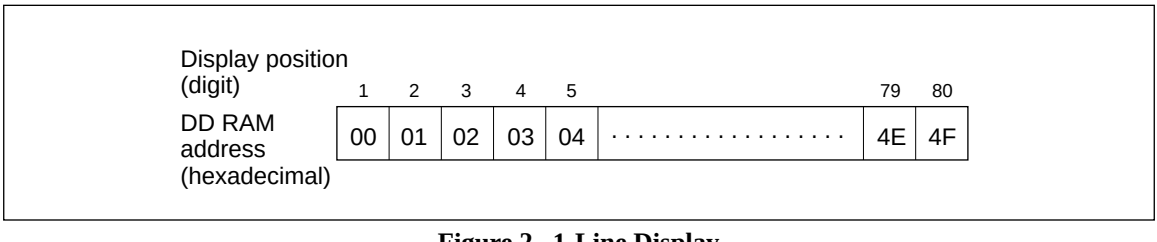


Figure 2 1-Line Display

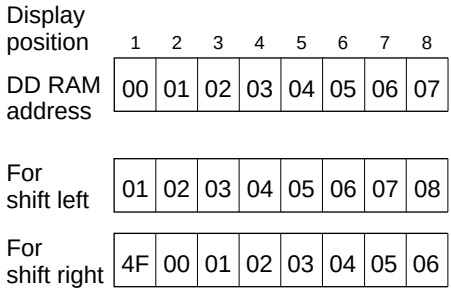


Figure 3 1-Line by 8-Character Display Example

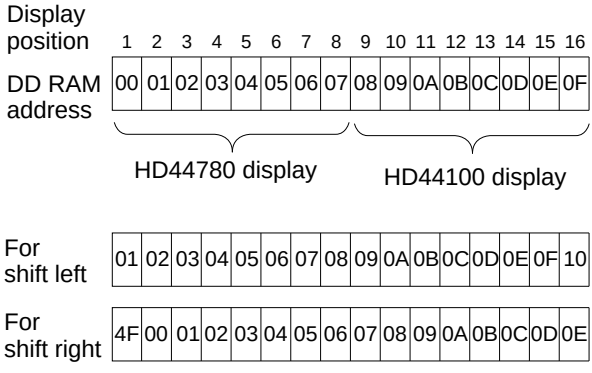


Figure 4 1-Line by 16-Character Display Example

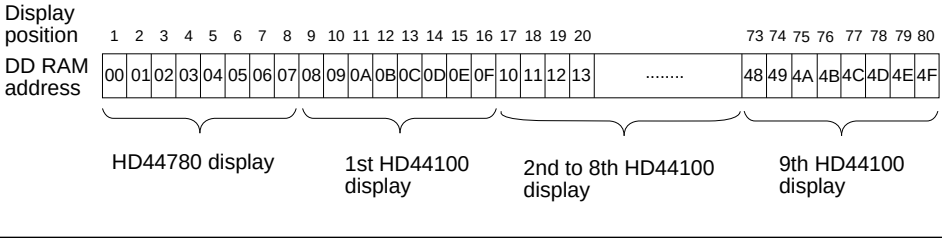


Figure 5 1-Line by 80-Character Display Example

- 2-line display (N = 1) (figure 6)

  — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters × 2 lines are displayed. See figure 7.

  When display shift operation is performed, the DD RAM address shifts. See figure 7.

Display position	1	2	3	4	5		39	40
DD RAM address (hexadecimal)	00	01	02	03	04	· · · · · · · · · · · · · · · · · ·	26	27
	40	41	42	43	44	· · · · · · · · · · · · · · · · · ·	66	67

Figure 6 2-Line Display

Display position	1	2	3	4	5	6	7	8
DD RAM address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For shift left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For shift right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 7 2-Line by 8-Character Display Example

— Case 2: For a 16-character × 2-line display, the HD44780 can be extended using one HD44100. See figure 8.

When display shift operation is performed, the DD RAM address shifts. See figure 8.

— Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased by using one HD44780U and two or more HD44100s, can be considered as an extension of case #2. See figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100, up to 40 digits × 2 lines can be displayed by externally connecting four HD44100s.

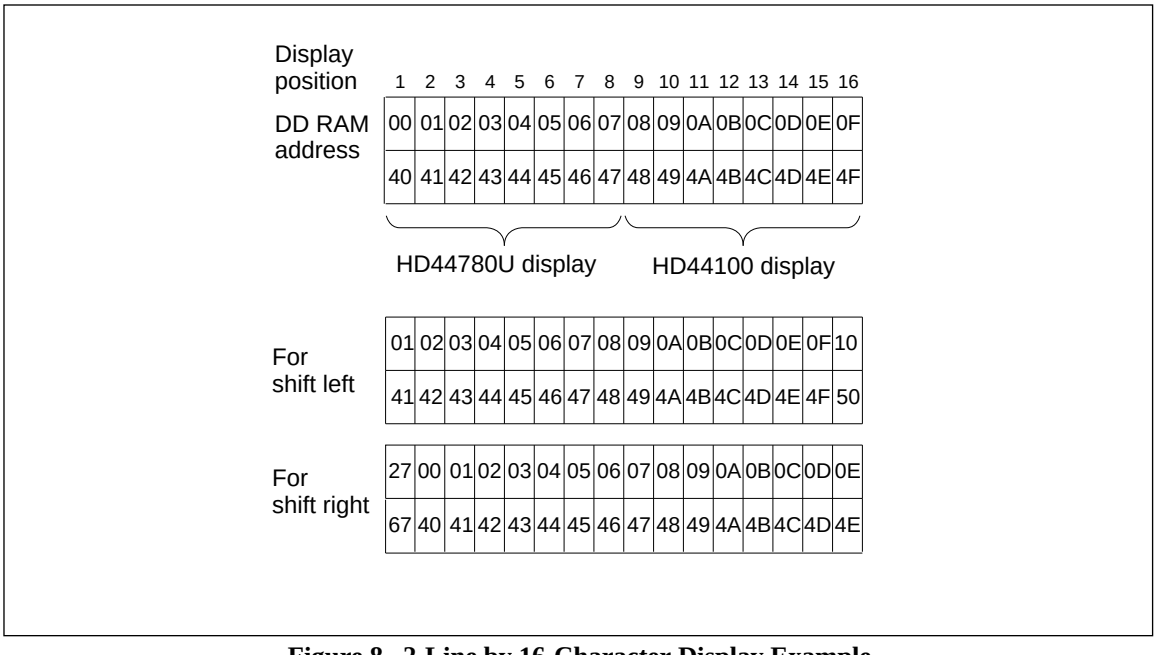


Figure 8 2-Line by 16-Character Display Example

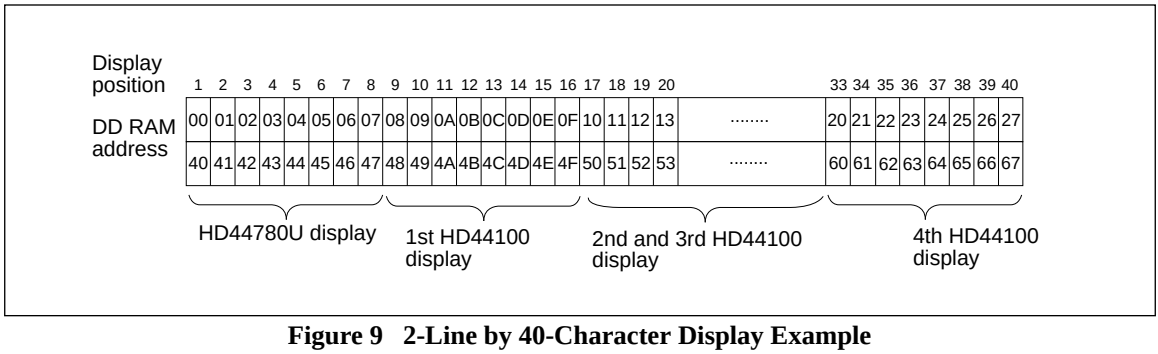


Figure 9 2-Line by 40-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot or 5 × 10 dot character patterns from 8-bit character codes (table 4). It can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 8 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written.

Write into DD RAM the character codes at the addresses shown as the left column of table 4 to show the character patterns stored in CG RAM.

See table 5 for the relationship between CG RAM addresses and data and display patterns.

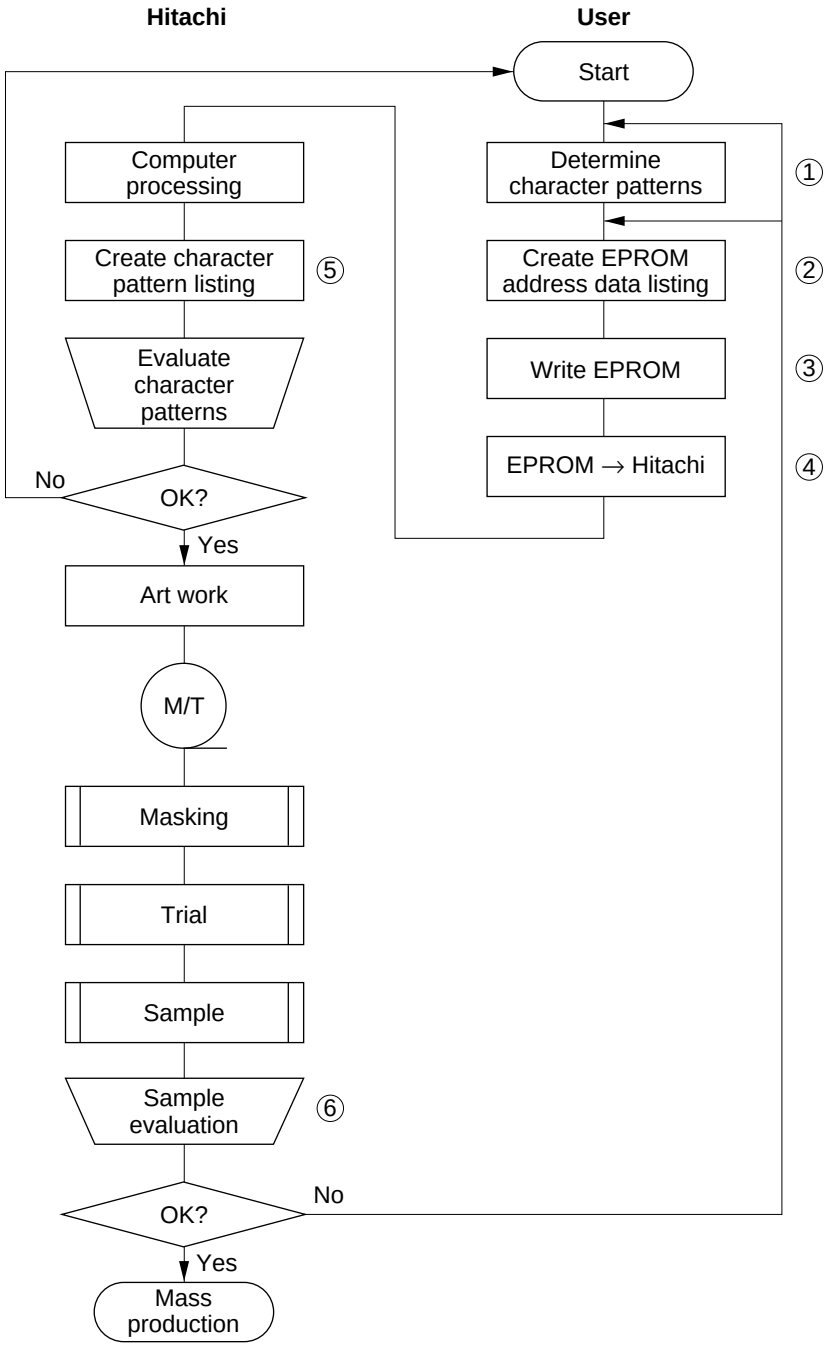
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 10 Character Pattern Development Procedure

- Programming character patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD44780U character generator ROM can generate 208 5×8 dot character patterns and 32 5×10 dot character patterns for a total of 240 different character patterns.

— Character patterns

EPROM address data and character pattern data correspond with each other to form a 5×8 or 5×10 dot character pattern (tables 2 and 3).

Table 2 Example of Correspondence between EPROM Address Data and Character Pattern (5×8 Dots)

EPROM Address												Data					
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	LSB O_0	
								0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← Cursor position
								1	0	0	0	0	0	0	0	0	
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	

Character code — Line position

Notes:
1. EPROM addresses A_{11} to A_3 correspond to a character code.
2. EPROM addresses A_3 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. EPROM data O_5 to O_7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 9 and the following lines must be blanked with 0s for a 5×8 dot character fonts.

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** Always input 0s.

2. **EPROM data in CG RAM area:** Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)

3. **EPROM data used when the user does not use any HD44780U character pattern:** According to the user application, handled in one of the two ways listed as follows.

a. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)

b. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5×10 Dots)

EPROM Address												Data				
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	LSB O_0
								0	0	0	0	0	0	0	0	0
								0	0	0	1	0	0	0	0	0
								0	0	1	0	0	1	1	0	1
								0	0	1	1	1	0	0	1	1
								0	1	0	0	1	0	0	0	1
								0	1	0	1	1	0	0	0	1
								0	1	1	0	0	1	1	1	1
0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1
								1	0	0	0	0	0	0	0	1
								1	0	0	1	0	0	0	0	1
								1	0	1	0	0	0	0	0	0
								1	0	1	1	0	0	0	0	0
								1	1	0	0	0	0	0	0	0
								1	1	0	1	0	0	0	0	0
								1	1	1	0	0	0	0	0	0
								1	1	1	1	0	0	0	0	0

← Cursor position

Character code

Line position

Notes: 1. EPROM addresses A_{11} to A_3 correspond to a character code.
2. EPROM addresses A_3 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. EPROM data O_5 to O_7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 11 and the following lines must be blanked with 0s for a 5×10 dot character fonts.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)

Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	(2)															
xxxx0010	(3)															
xxxx0011	(4)															
xxxx0100	(5)															
xxxx0101	(6)															
xxxx0110	(7)															
xxxx0111	(8)															
xxxx1000	(1)															
xxxx1001	(2)															
xxxx1010	(3)															
xxxx1011	(4)															
xxxx1100	(5)															
xxxx1101	(6)															
xxxx1110	(7)															
xxxx1111	(8)															

Note: The user can specify any pattern for character-generator RAM.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A01)

Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)																
xxxx0001	(2)																
xxxx0010	(3)																
xxxx0011	(4)																
xxxx0100	(5)																
xxxx0101	(6)																
xxxx0110	(7)																
xxxx0111	(8)																
xxxx1000	(1)																
xxxx1001	(2)																
xxxx1010	(3)																
xxxx1011	(4)																
xxxx1100	(5)																
xxxx1101	(6)																
xxxx1110	(7)																
xxxx1111	(8)																

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A02)

Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)																
xxxx0001	(2)																
xxxx0010	(3)																
xxxx0011	(4)																
xxxx0100	(5)																
xxxx0101	(6)																
xxxx0110	(7)																
xxxx0111	(8)																
xxxx1000	(1)																
xxxx1001	(2)																
xxxx1010	(3)																
xxxx1011	(4)																
xxxx1100	(5)																
xxxx1101	(6)																
xxxx1110	(7)																
xxxx1111	(8)																

Table 5 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

For 5 × 8 dot character patterns

Character Codes (DD RAM data)	CG RAM Address	Character Patterns (CG RAM data)	
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0	
High Low	High Low	High Low	
0 0 0 0 * 0 0 0	0 0 0	* * * 1 1 1 1 0	Character pattern (1)
	0 0 1	* * * 1 0 0 0 1	
	0 1 0	* * * 1 0 0 0 1	
	0 1 1	* * * 1 1 1 1 0	
	1 0 0	* * * 1 0 1 0 0	
	1 0 1	* * * 1 0 0 1 0	
	1 1 0	* * * 1 0 0 0 1	
	1 1 1	* * * 0 0 0 0 0	Cursor position
0 0 0 0 * 0 0 1	0 0 0	* * * 1 0 0 0 1	Character pattern (2)
	0 0 1	* * * 0 1 0 1 0	
	0 1 0	* * * 1 1 1 1 1	
	0 1 1	* * * 0 0 1 0 0	
	1 0 0	* * * 1 1 1 1 1	
	1 0 1	* * * 0 0 1 0 0	
	1 1 0	* * * 0 0 1 0 0	
	1 1 1	* * * 0 0 0 0 0	Cursor position
	0 0 0	* * *	
	0 0 1	* * *	
0 0 0 0 * 1 1 1	1 1 1		
	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1	* * *	

Notes: 1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).

2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.
   If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.

3. Character pattern row positions correspond to CG RAM data bits 0 to 4 (bit 4 being at the left).

4. As shown table 5, CG RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.

5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Table 5 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data) (cont)

For 5 × 10 dot character patterns

Character Codes (DD RAM data)	CG RAM Address	Character Patterns (CG RAM data)	
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low	7 6 5 4 3 2 1 0 High Low	
0 0 0 0 * 0 0 *	0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0	* * * 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 1 1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 * * * 0 0 0 0 0	Character pattern Cursor position
	1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* * * * * * * * * * * * * * * * * *	
	0 0 0 0 0 0 0 1	* * *	
0 0 0 0 * 1 1 *	1 1 1 0 0 1 1 0 1 0	* * *	
	1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* * * * * * * * * * * * * * * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CG RAM address bits 4 and 5 (2 bits: 4 types).

2. CG RAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.
   If the 11th line data is “1”, “1” bits will light up the 11th line regardless of the cursor presence.
   Since lines 12 to 16 are not used for display, they can be used for general data RAM.

3. Character pattern row positions are the same as 5 × 8 dot character pattern positions.

4. CG RAM character patterns are selected when character code bits 4 to 7 are all 0.
   However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area. This circuit also generates timing signals for the operation of the externally connected HD44100 driver.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the HD44100 driver. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs. The serial data can be sent to externally cascaded HD44100s used for displaying extended digit numbers.

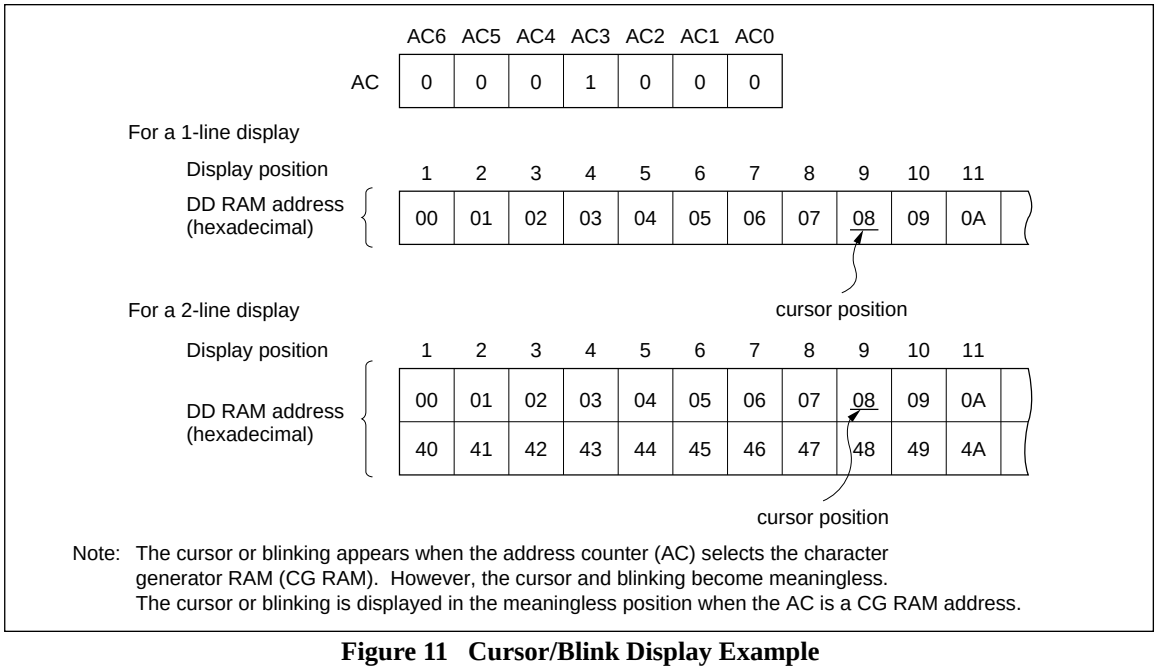
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display. The rest of the display, corresponding to latter addresses, are added with each additional HD44100.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DD RAM) address set in the address counter (AC).

For example (figure 11), when the address counter is 08H, the cursor position is displayed at DD RAM address 08H.



Note: The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CG RAM). However, the cursor and blinking become meaningless. The cursor or blinking is displayed in the meaningless position when the AC is a CG RAM address.

Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

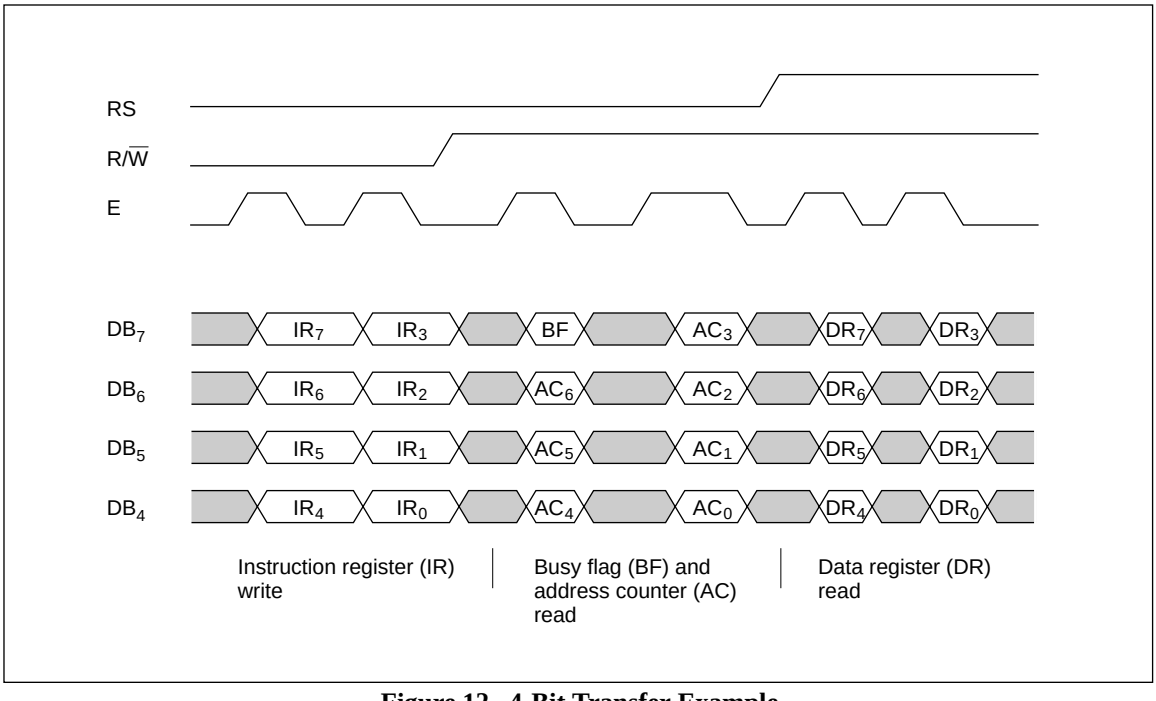


Figure 12 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD44780U can be controlled by the MPU. Before starting the internal operation of the HD44780U, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD44780U is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/write signal (R/$\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD44780U instructions (table 6). There are four categories of instructions that:

- Designate HD44780U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD44780U RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 11) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD44780U is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD44780U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 6 for the list of each instruction execution time.

Table 6 Instructions

Instruction	Code										Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.52 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CG RAM address	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set DD RAM address	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 6 Instructions (cont)

Instruction	Code RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 270 kHz)
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM.	37 µs t_{ADD} = 4 µs*
Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	37 µs t_{ADD} = 4 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 8 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 250 kHz, $37\ \mu s \times \frac{270}{250} = 40\ \mu s$

Note: — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

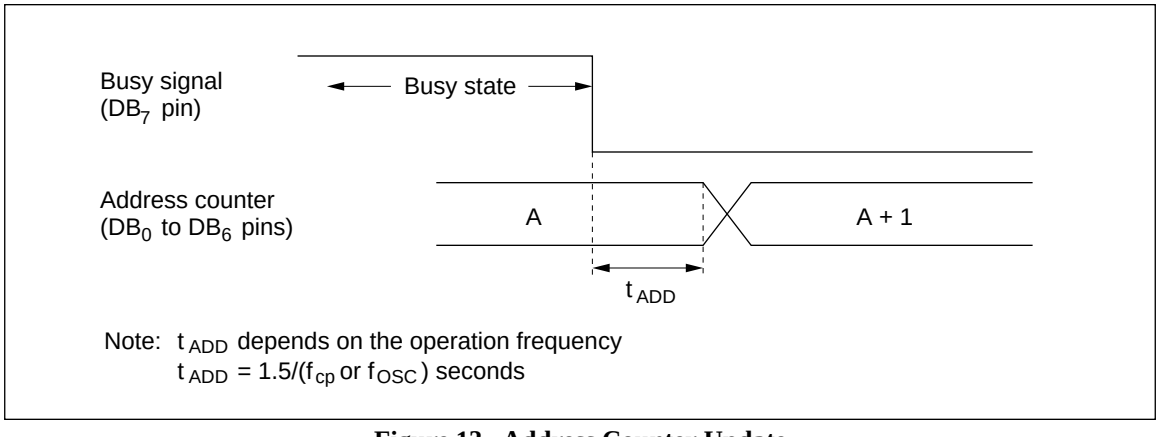


Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font selection and in the 11th line for the 5 × 10 dot character font selection (figure 16).

B: The character indicated by the cursor blinks when B is 1 (figure 16). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when f_{cp} or f_{OSC} is 250 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $409.6 \times 250/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 7). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

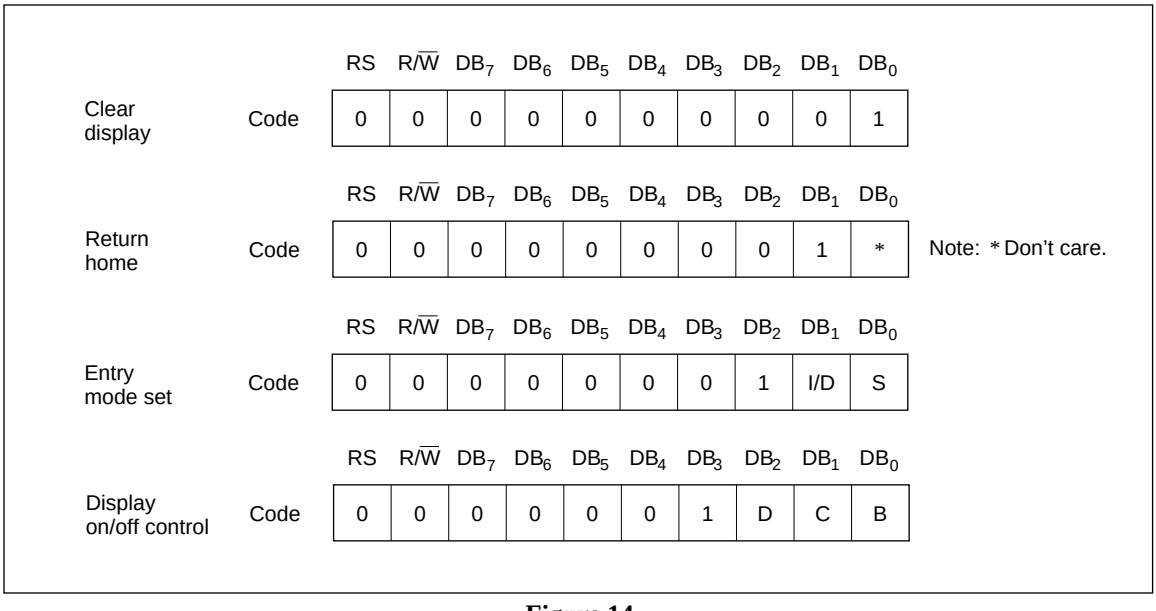


Figure 14

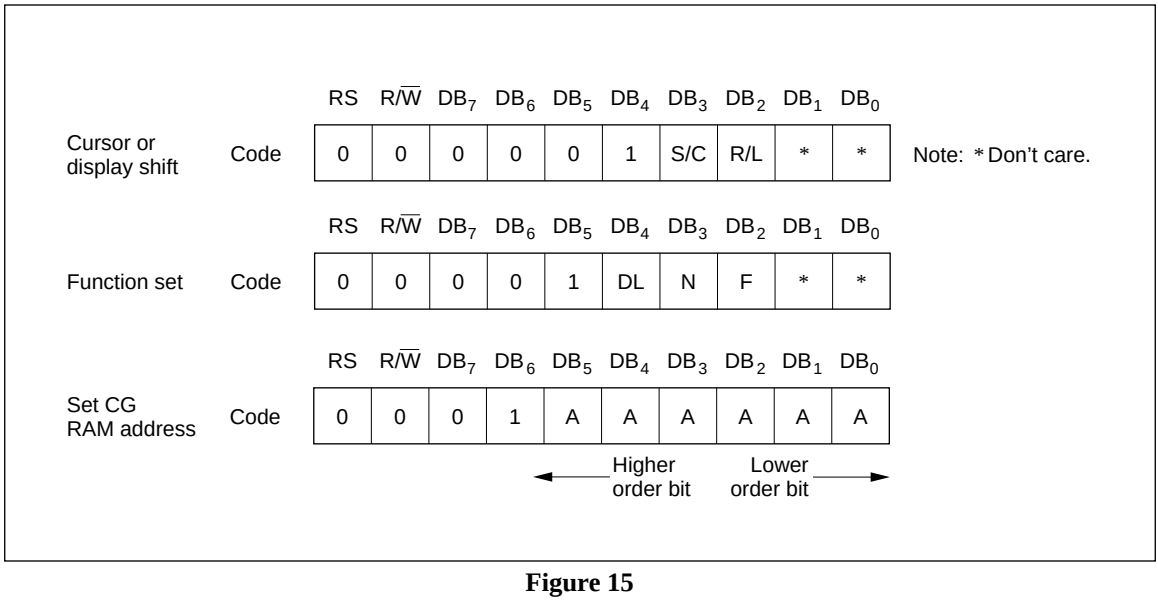


Figure 15

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DD RAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG RAM address and set DD RAM address.

Table 7 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 8 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 8 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 8 dots	1/16	Cannot display two lines for 5 × 10 dot character font

Note: * Indicates don't care.

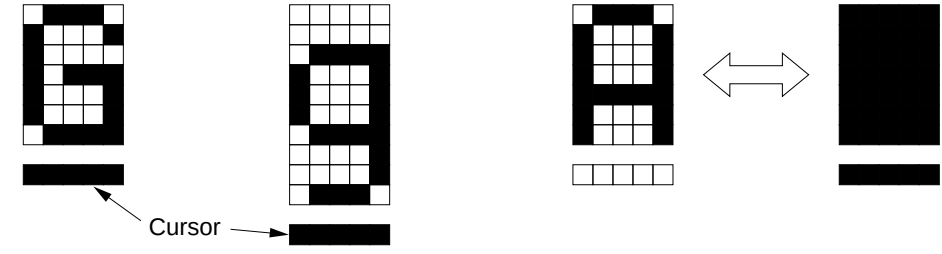


Figure 16 Cursor and Blinking

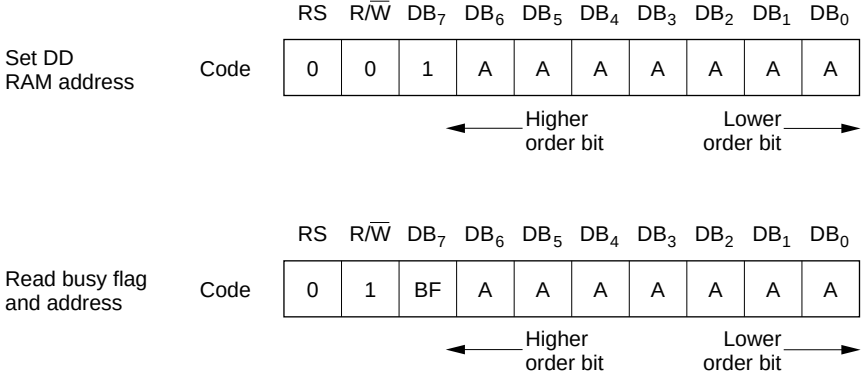


Figure 17

Write Data to CG or DD RAM

Write data to CG or DD RAM writes 8-bit binary data DDDDDDDD to CG or DD RAM.

To write into CG or DD RAM is determined by the previous specification of the CG RAM or DD RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DD RAM

Read data from CG or DD RAM reads 8-bit binary data DDDDDDDD from CG or DD RAM.

The previous designation determines whether CG or DD RAM is to be read. Before entering this read instruction, either CG RAM or DD RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD RAM). The operation of the cursor shift instruction is the same as the set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CG RAM or DD RAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

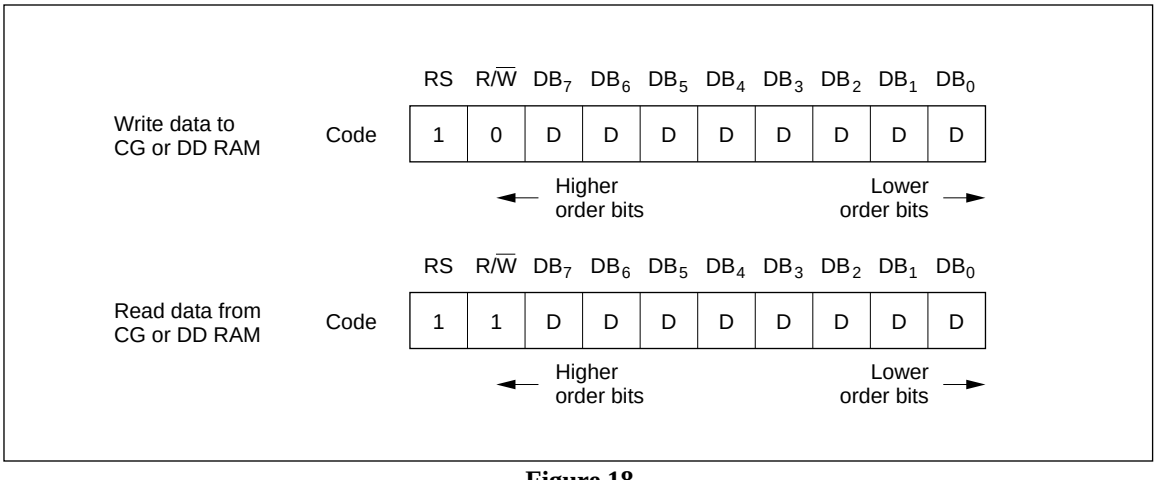


Figure 18

Interfacing the HD44780U

Interface to MPUs

- Interfacing to an 8-bit MPU through a PIA

  See figure 20 for an example of using a PIA or I/O port (for a single-chip microcomputer) as an interface device. The input and output of the device is TTL compatible.

In this example, PB_0 to PB_7 are connected to the data bus DB_0 to DB_7, and PA_0 to PA_2 are connected to E, R/$\overline{W}$, and RS, respectively.

Pay careful attention to the timing relationship between E and the other signals when reading or writing data using a PIA for the interface.

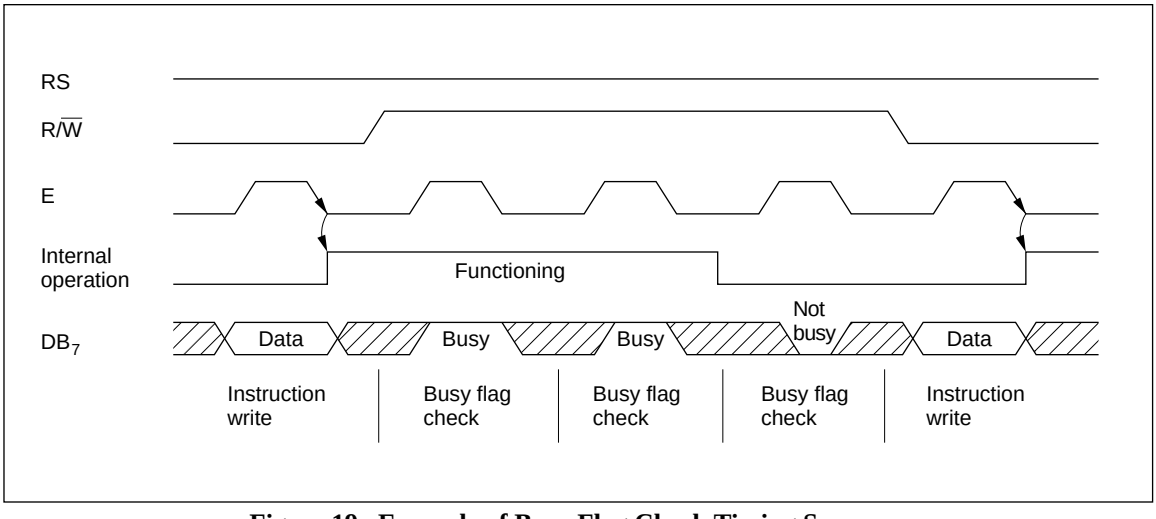


Figure 19 Example of Busy Flag Check Timing Sequence

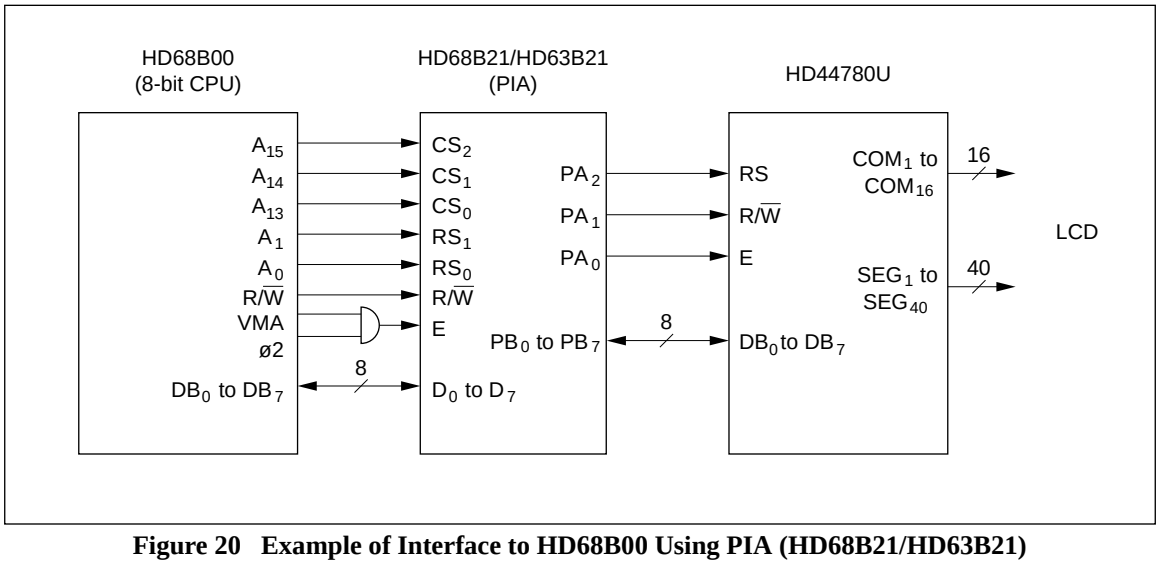


Figure 20 Example of Interface to HD68B00 Using PIA (HD68B21/HD63B21)

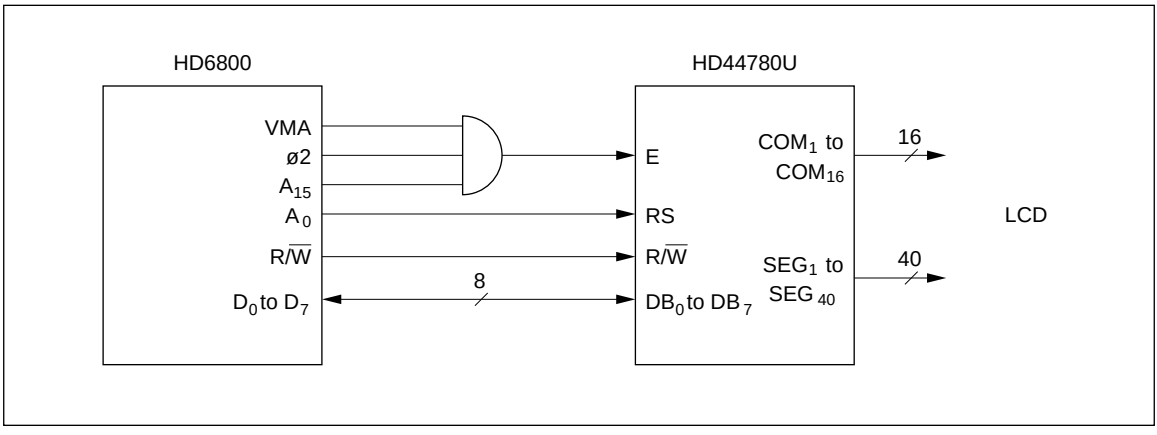


Figure 21 8-Bit MPU Interface

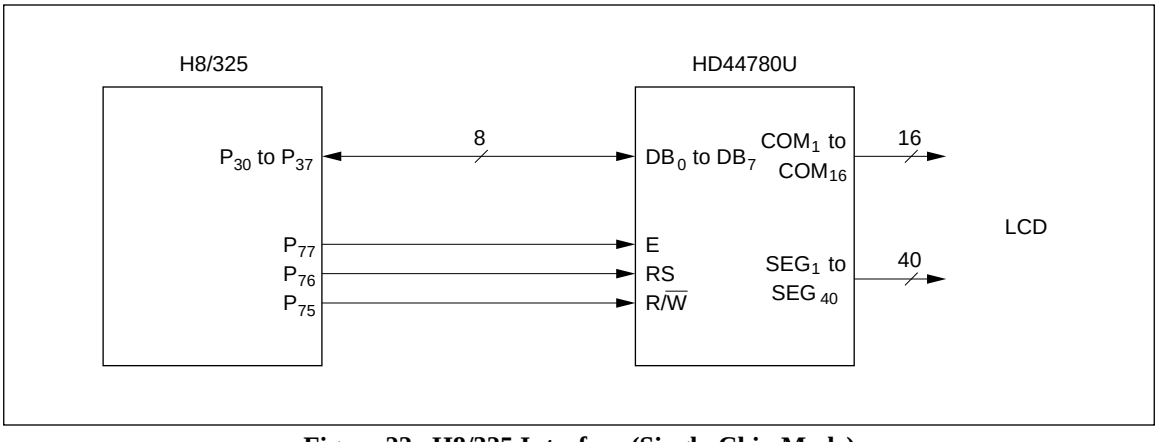


Figure 22 H8/325 Interface (Single-Chip Mode)

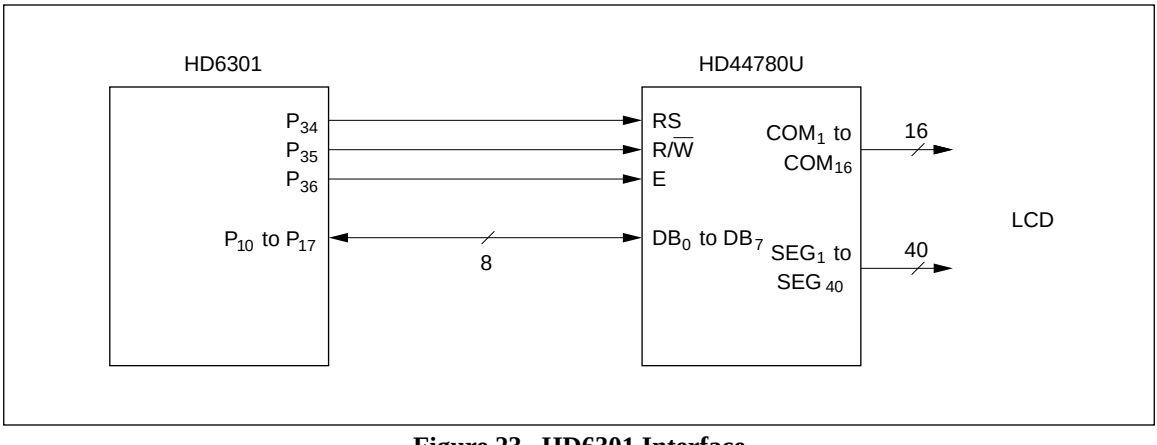


Figure 23 HD6301 Interface

- Interfacing to a 4-bit MPU

  The HD44780U can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See figure 24.)

  See figure 25 for an interface example to the HMCS4019R.

  Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.

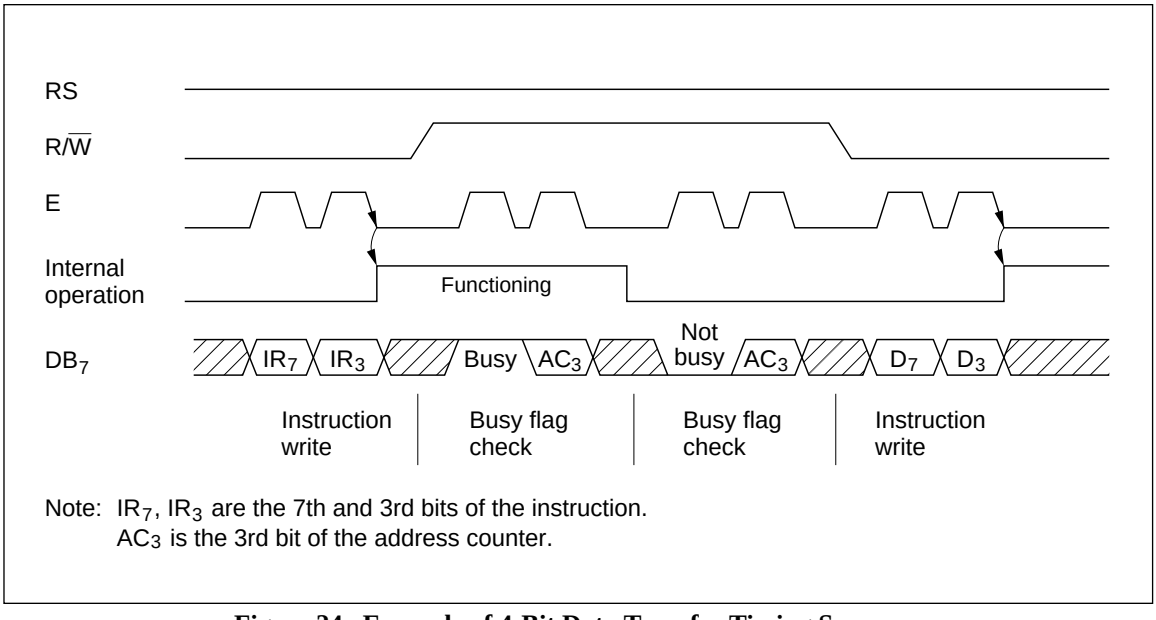


Figure 24 Example of 4-Bit Data Transfer Timing Sequence

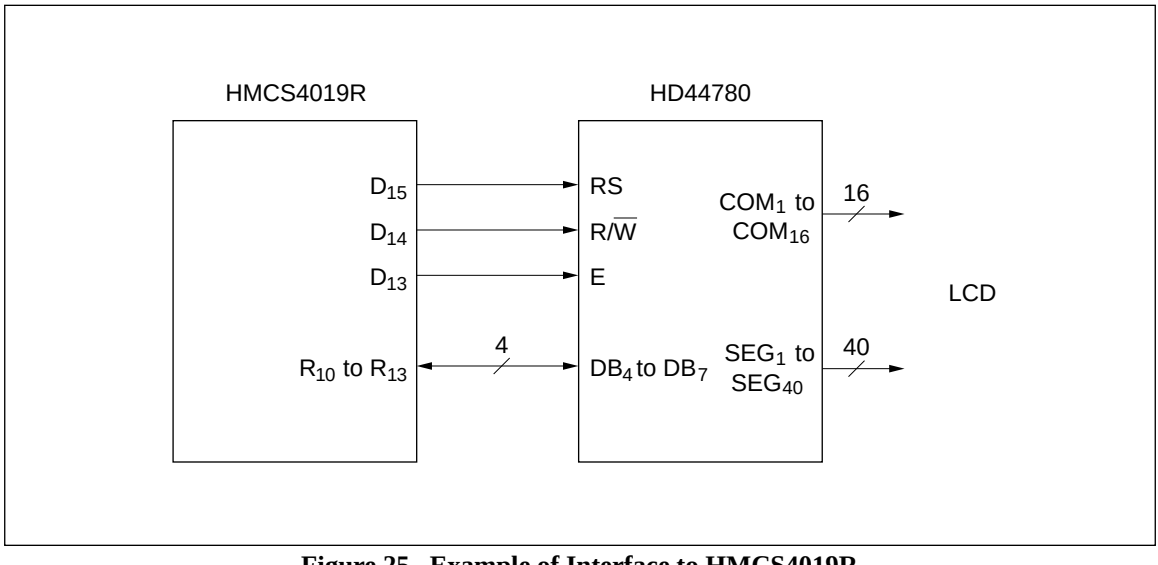


Figure 25 Example of Interface to HMCS4019R

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD44780U can perform two types of displays, 5 × 8 dot and 5 × 10 dot character fonts, each with a cursor.

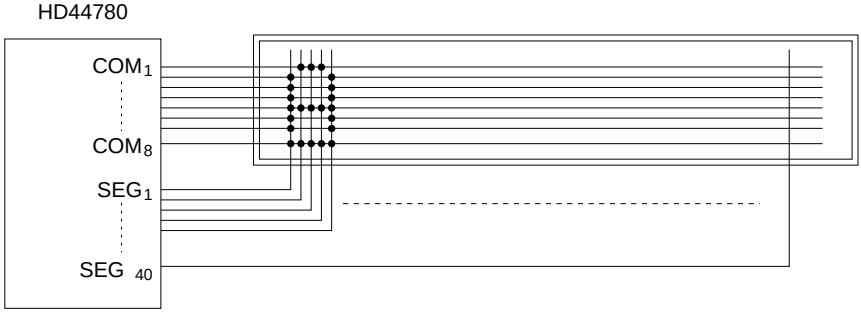
Up to two lines are displayed for 5 × 8 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (table 9).

The number of lines and font types can be selected by the program. (See table 6, Instructions.)

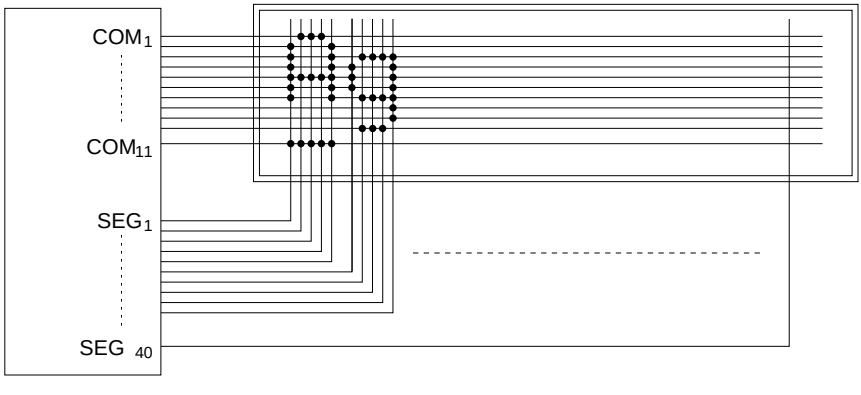
Connection to HD44780 and Liquid Crystal Display: See figure 26 for the connection examples.

Table 9 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 8 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 8 dots + cursor	16	1/16



Example of a 5×8 dot, 8-character × 1-line display (1/4 bias, 1/8 duty cycle)

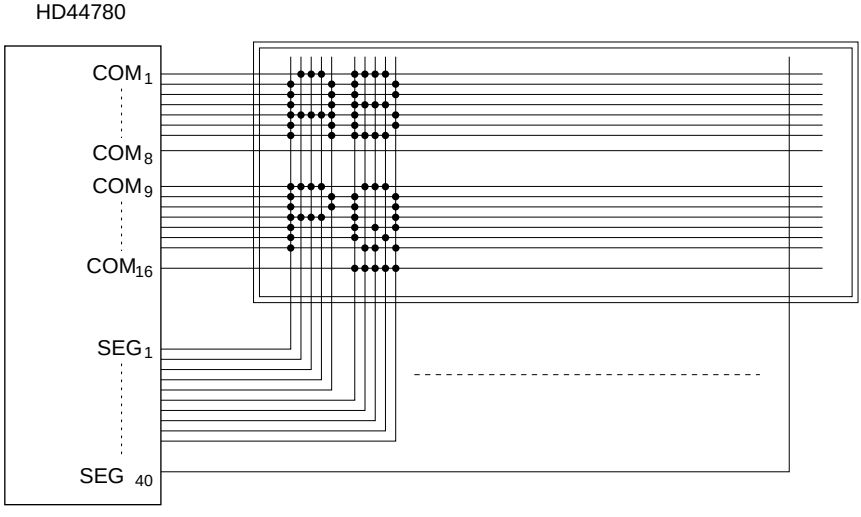


Example of a 5×10 dot, 8-character × 1-line display (1/4 bias, 1/11 duty cycle)

Figure 26 Liquid Crystal Display and HD44780 Connections

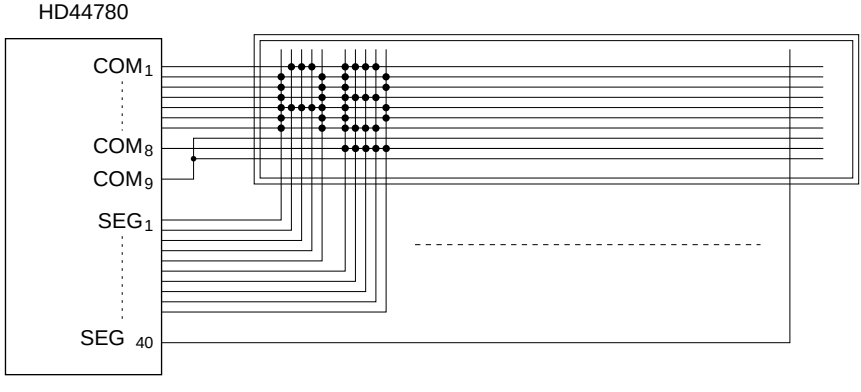
Since five segment signal lines can display one digit, one HD44780U can display up to 8 digits for a 1-line display and 16 digits for a 2-line display.

The examples in figure 26 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (figure 27).



Example of a 5×8 dot, 8-character × 2-line display (1/5 bias, 1/16 duty cycle)

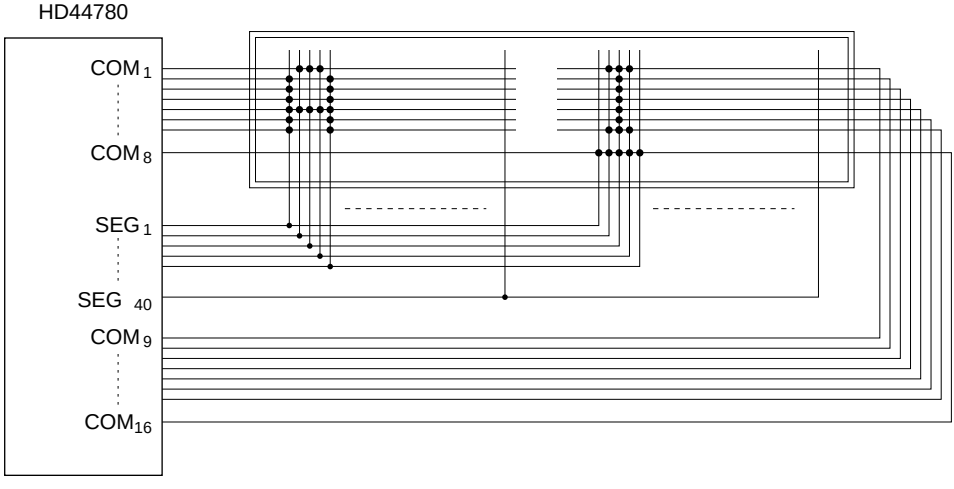
Figure 26 Liquid Crystal Display and HD44780 Connections (cont)



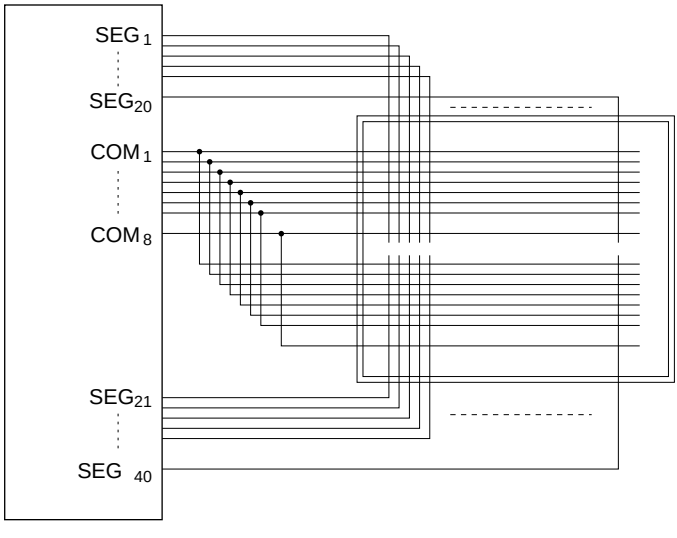
5 × 8 dot, 8-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 27 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (figure 28) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DD RAM) addresses for 4 characters × 2 lines and for 16 characters × 1 line are the same as in figure 26.



5 × 8 dot, 16-character × 1-line display
(1/5 bias, 1/16 duty cycle)



5 × 8 dot, 4-character × 2-line display
(1/4 bias, 1/8 duty cycle)

Figure 28 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V_1 to V_5 of the HD44780U to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (table 10).

V_{LCD} is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V_1 to V_5 (figure 29).

Table 10 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Power Supply	1/4	1/5
V_1	V_{CC}–1/4 V_{LCD}	V_{CC}–1/5 V_{LCD}
V_2	V_{CC}–1/2 V_{LCD}	V_{CC}–2/5 V_{LCD}
V_3	V_{CC}–1/2 V_{LCD}	V_{CC}–3/5 V_{LCD}
V_4	V_{CC}–3/4 V_{LCD}	V_{CC}–4/5 V_{LCD}
V_5	V_{CC}–V_{LCD}	V_{CC}–V_{LCD}

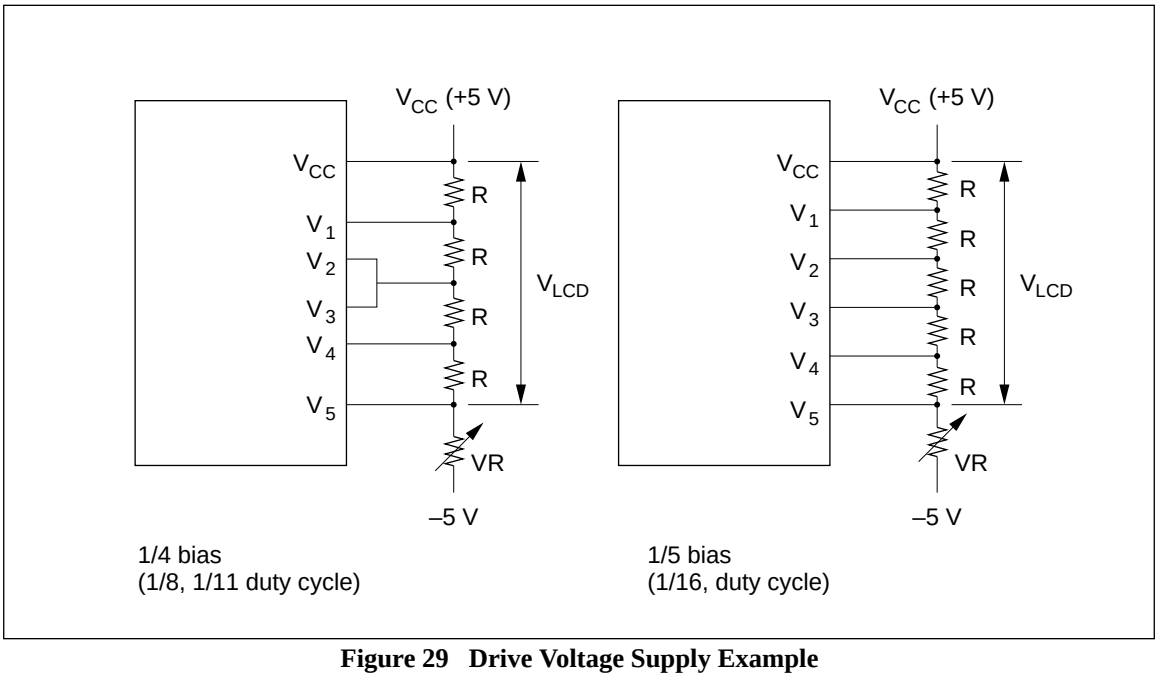


Figure 29 Drive Voltage Supply Example

Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of figure 30 apply only when the oscillation frequency is 270 kHz (one clock pulse of 3.7 µs).

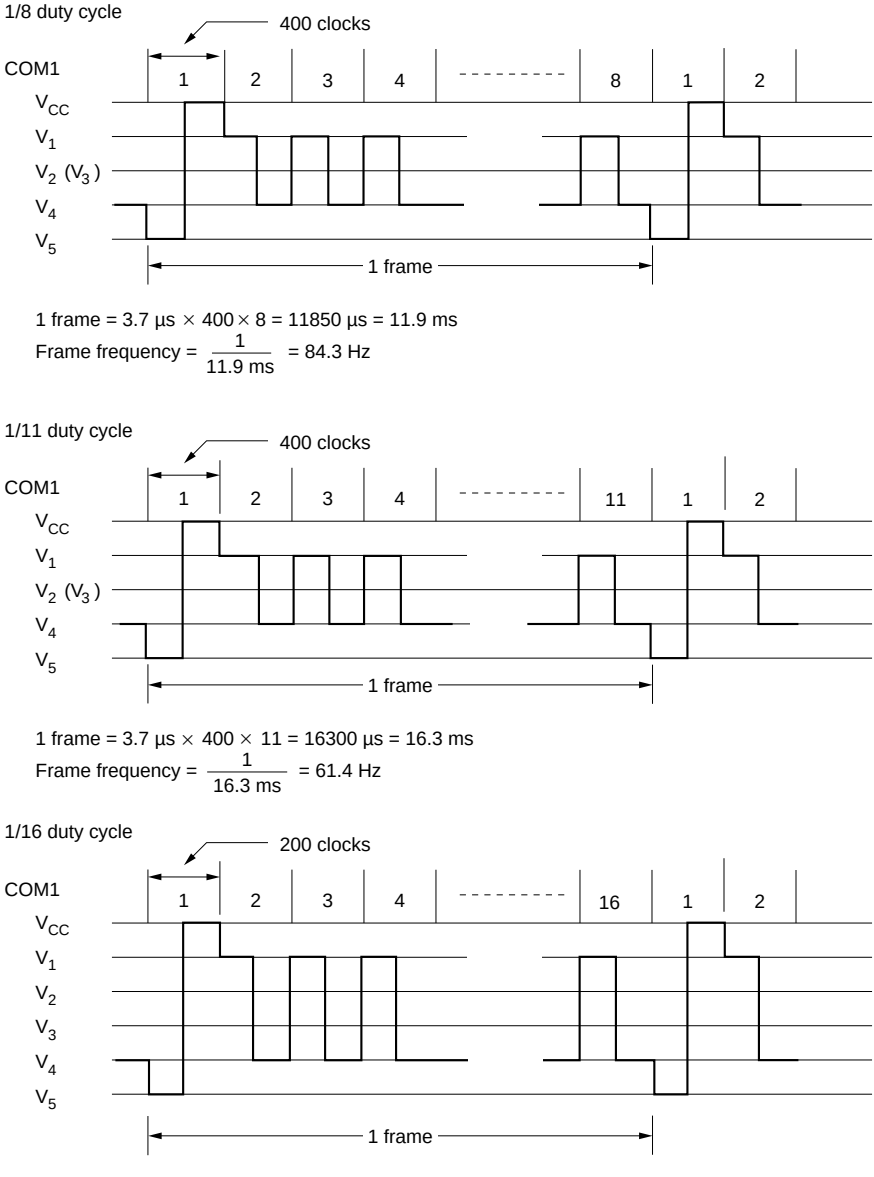


Figure 30 Frame Frequency

Connection with HD44100 Driver

By externally connecting an HD44100 liquid crystal display driver to the HD44780U, the number of display digits can be increased. The HD44100 is used as a segment signal driver when connected to the HD44780U. The HD44100 can be directly connected to the HD44780U since it supplies CL_1, CL_2, M, and D signals and power for the liquid crystal display drive (figure 31).

Caution: The connection of voltage supply pins V_1 through V_6 for the liquid crystal display drive is somewhat complicated.

Up to nine HD44100 units can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to four units for a 2-line display (duty factor 1/16). The RAM size limits the HD44780U to a maximum of 80 character display digits. The connection method for both 1-line and 2-line displays or for 5×8 and 5×10 dot character fonts can remain the same (figure 26).

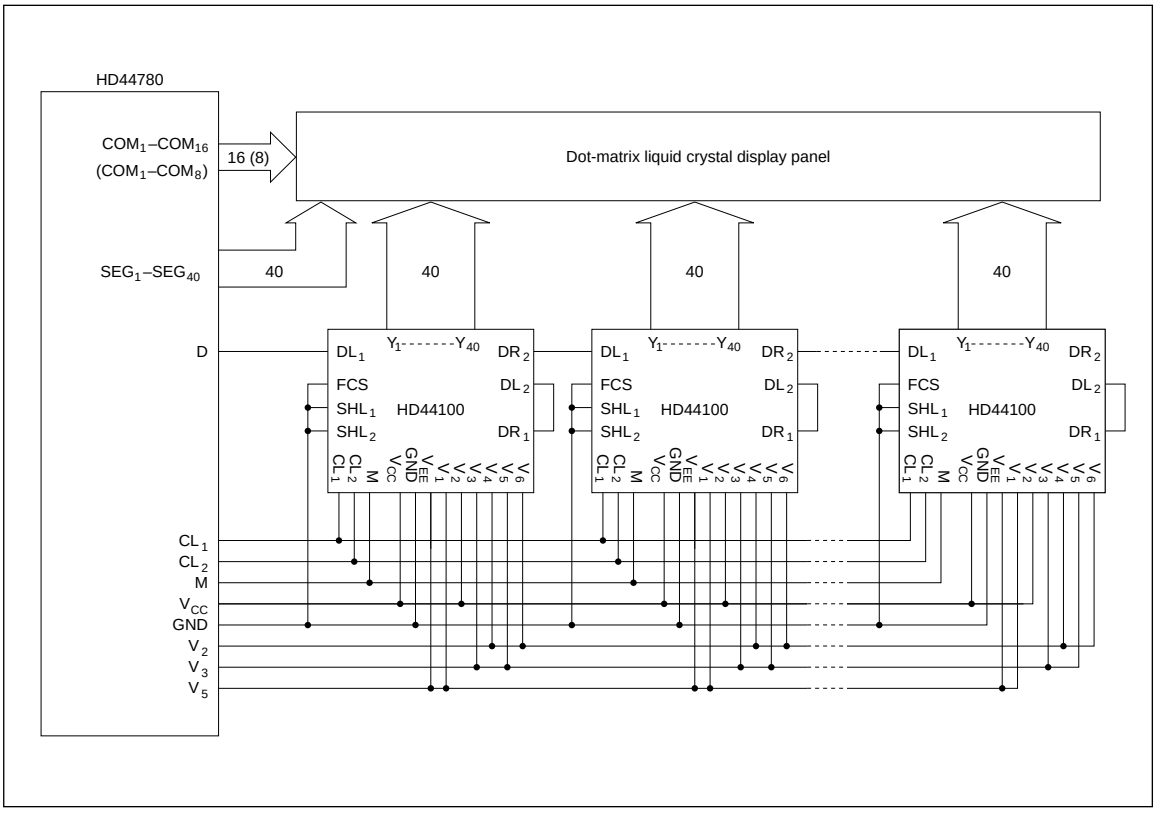


Figure 31 Example of Connecting HD44100s to HD44780

Instruction and Display Correspondence

- 8-bit operation, 8-digit × 1-line display with internal reset

  Refer to table 11 for an example of an 8-digit × 1-line display in 8-bit operation. The HD44780U functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

  Since the display shift operation changes only the display position with DD RAM contents unchanged, the first display data entered into DD RAM can be output when the return home operation is performed.

- 4-bit operation, 8-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (table 12). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 12). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 8-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be again set after the 8th character is completed. (See table 13.) Note that the display shift operation is performed for the first and second lines. In the example of table 13, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD44780U must be initialized by instructions. See the section, Initializing by Instruction.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	0	0	*	*	Sets to 8-bit operation and selects 1-line display and 5 × 8 dot character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	Writes I.
7	⋮										⋮	
8	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	Writes I.
9	Entry mode set	0	0	0	0	0	0	0	1	1	1	Sets mode to shift display at the time of write.
10	Write data to CG RAM/DD RAM	1	0	0	0	1	0	0	0	0	0	Writes a space.

Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
11	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	⋮										⋮	
13	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	⋮										⋮	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 12 4-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)							Initialized. No display.
2	Function set							Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
	0	0	0	0	1	0		
3	Function set							Sets 4-bit operation and selects 1-line display and 5 × 8 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
	0	0	0	0	1	0		
	0	0	0	0	*	*		
4	Display on/off control						_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0		
	0	0	1	1	1	0		
5	Entry mode set						_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0		
	0	0	0	1	1	0		
6	Write data to CG RAM/DD RAM						H_	Writes H. The cursor is incremented by one and shifts to the right.
	1	0	0	1	0	0		
	1	0	1	0	0	0		

Note: The control is the same as for 8-bit operation beyond step #6.

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	1	0	*	*		Sets to 8-bit operation and selects 2-line display and 5 × 8 dot character font.
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	. . . . .											. . . . .	
7	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
8	Set DD RAM address	0	0	1	1	0	0	0	0	0	0	HITACHI _	Sets DD RAM address so that the cursor is positioned at the head of the second line.

Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
9	Write data to CG RAM/DD RAM										HITACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
10					:						:	
11	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M. Display is shifted to the left. The first and second lines both shift at the same time.
	1	0	0	1	0	0	1	1	0	1		
14					:						:	
15	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to figures 32 and 33 for the procedures on 8-bit and 4-bit initializations, respectively.

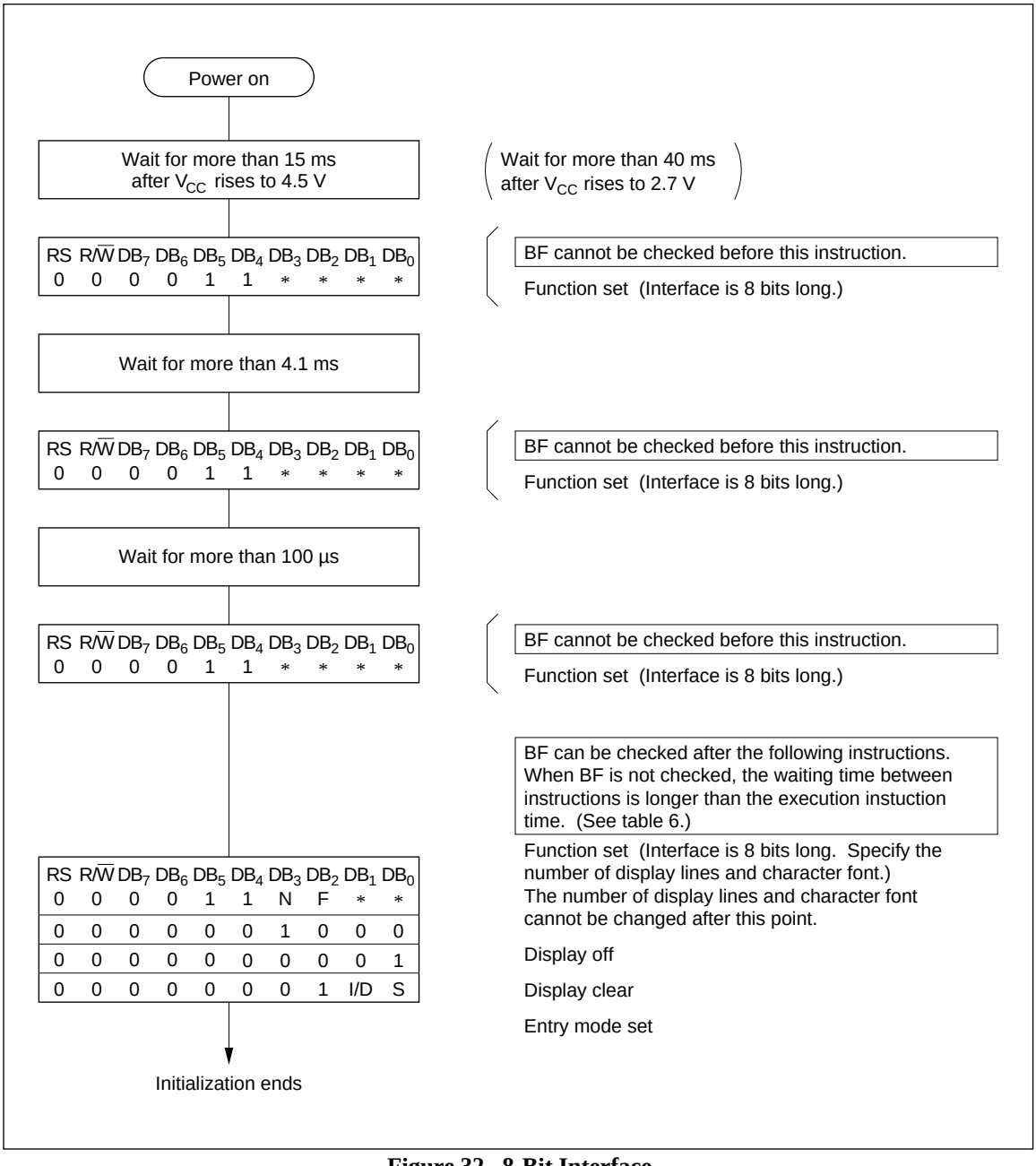


Figure 32 8-Bit Interface

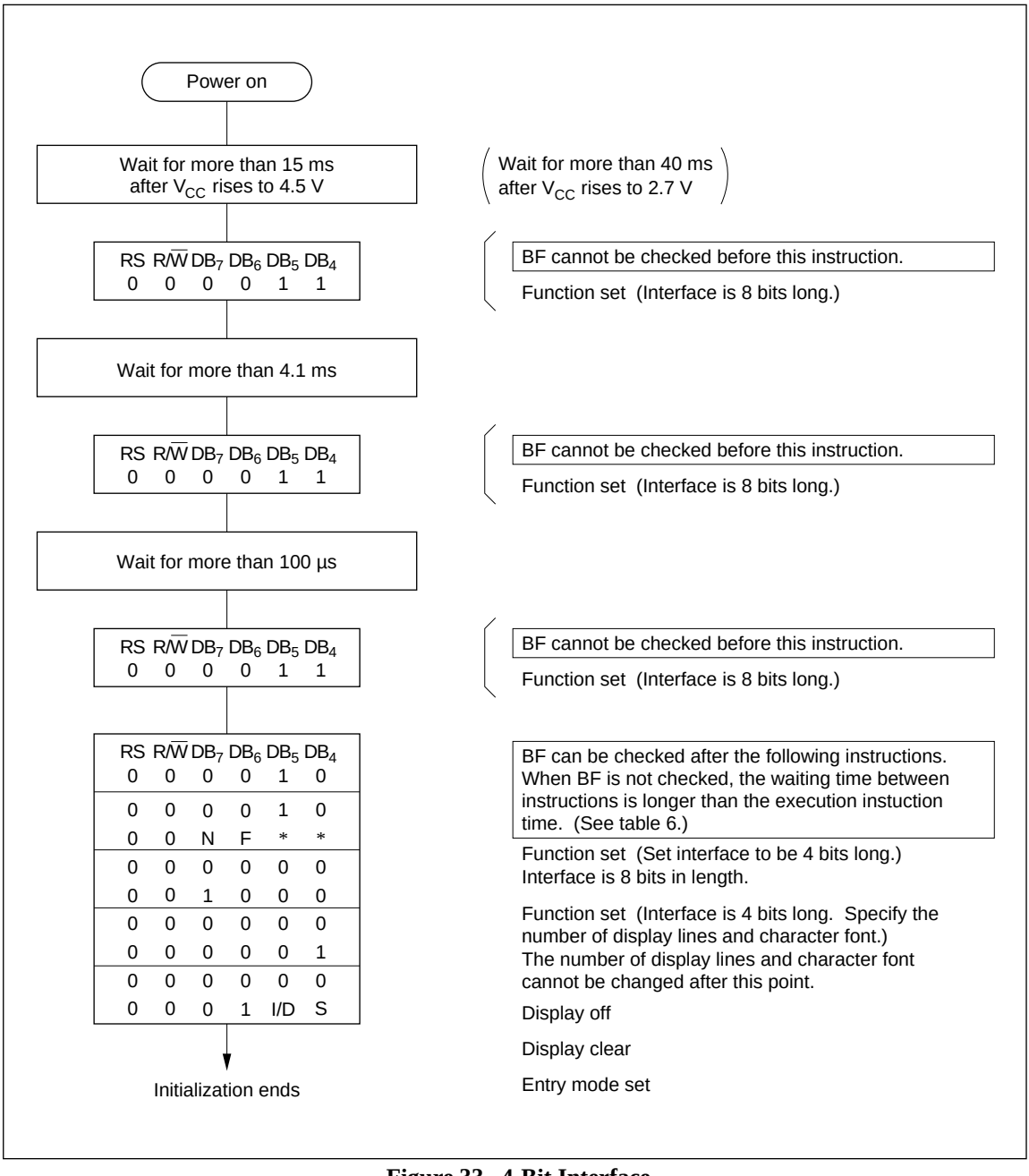


Figure 33 4-Bit Interface

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}–GND	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V_5	–0.3 to +13.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 to 4.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.55	V		6
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (DB_0–DB_7, RS, R/$\overline{W}$)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	11.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	11.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 to 4.5 V, T_a = –20 to +75°C[*3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Note*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 75 kΩ, V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 36
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 37
Power supply off time	t_{OFF}	1	—	—		

DC Characteristics (V_{CC} = 4.5 to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	2.2	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.6	V		6
Input high voltage (2) (OSC_1)	V_{IH2}	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	1.0	V		15
Output high voltage (1) (DB_0–DB_7)	V_{OH1}	2.4	—	—	V	$–I_{OH}$ = 0.205 mA	7
Output low voltage (1) (DB_0–DB_7)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA	7
Output high voltage (2) (except DB_0–DB_7)	V_{OH2}	0.9 V_{CC}	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except DB_0–DB_7)	V_{OL2}	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (DB_0–DB_7, RS, R/$\overline{W}$)	$–I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}	—	0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	11.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	11.0	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 4.5 to 5.5 V, T_a = –20 to +75°C[*3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	µs		11
	External clock fall time	t_{fcp}	—	—	0.2	µs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ V_{CC} = 5.0 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Interface Timing Characteristics with External Driver

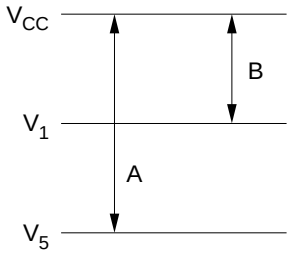
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 36
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 37
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V.

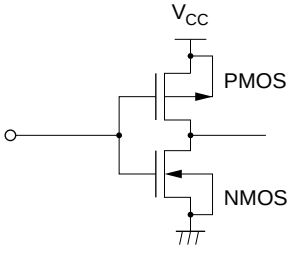


$A = V_{CC} - V_5$
$B = V_{CC} - V_1$
$A \geq 1.5$ V
$B \leq 0.25 \times A$

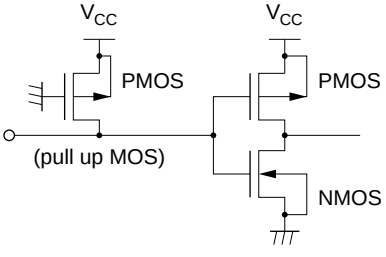
The conditions of V_1 and V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified as LCD voltage V_{LCD}.

2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

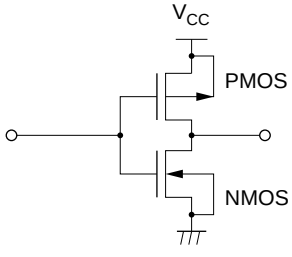
Input pin
Pin: E (MOS without pull-up)



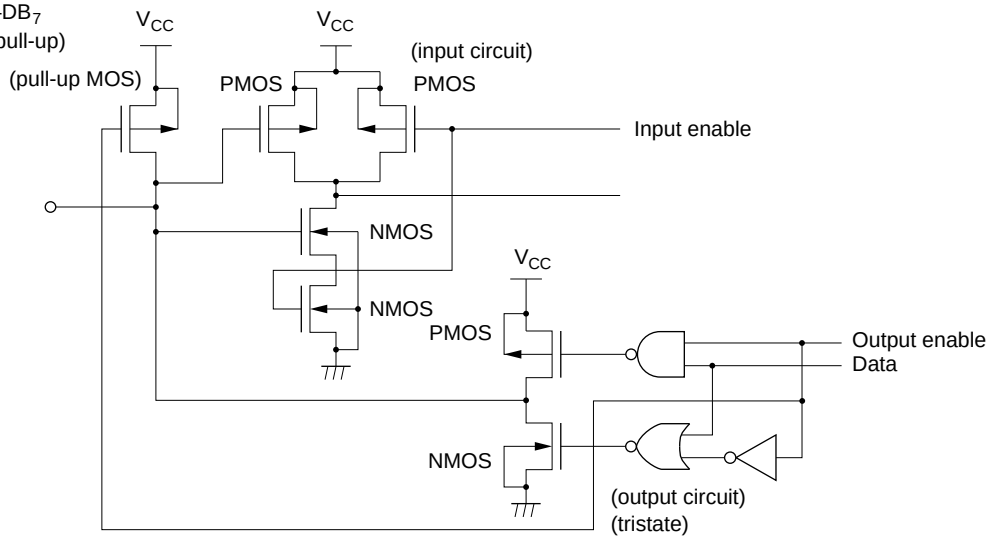
Pins: RS, R/$\overline{W}$ (MOS with pull-up)



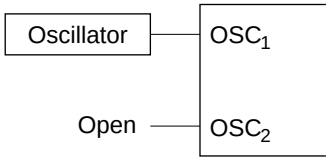
Output pin
Pins: CL_1, CL_2, M, D

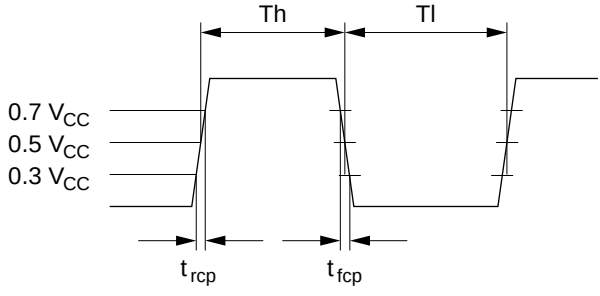


I/O Pin
Pins: DB_0–DB_7
(MOS with pull-up)



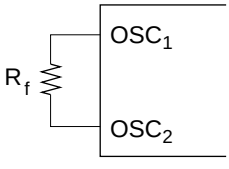
6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull–up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



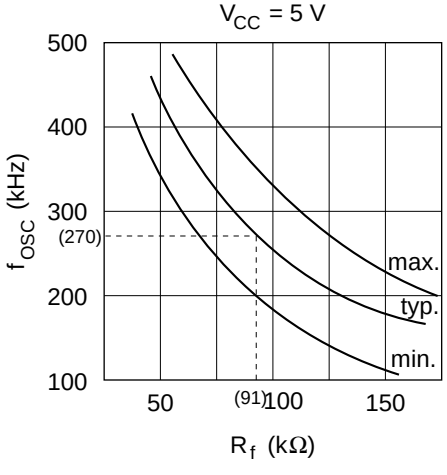


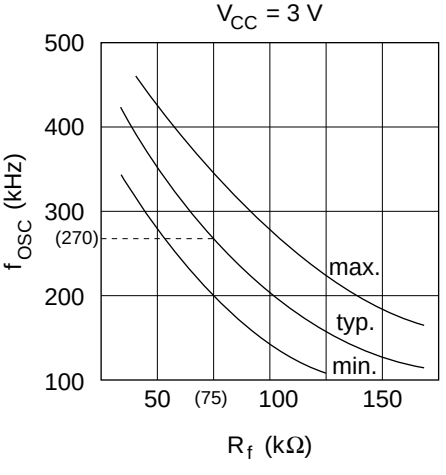
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



R_f: 75 kΩ ± 2% (when V_{CC} = 3 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 5 V)
Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.

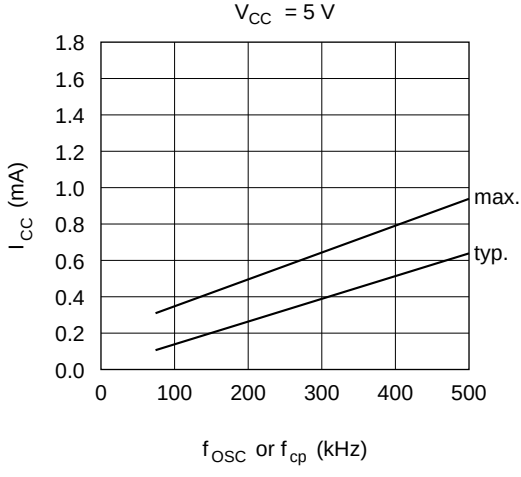


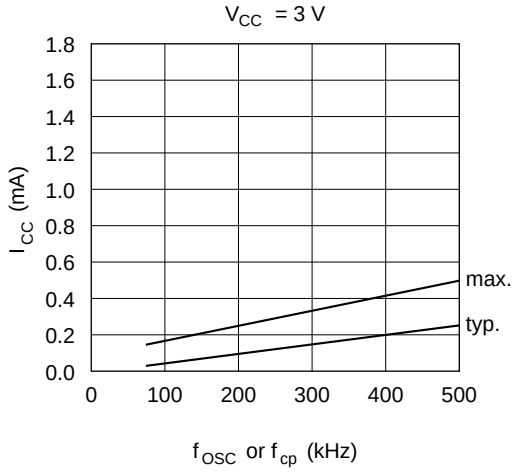


13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{40}).

14. The following graphs show the relationship between operation frequency and current consumption.

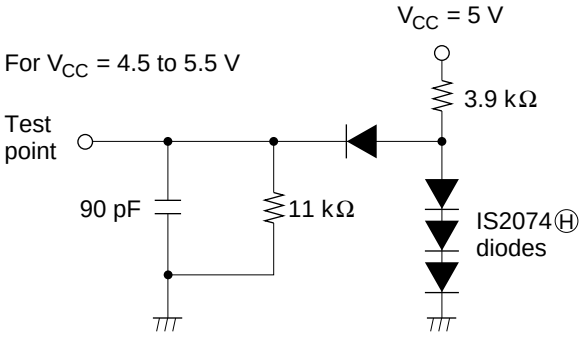


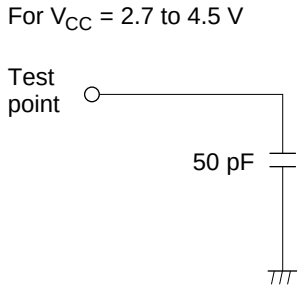


15. Applies to the OSC_1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

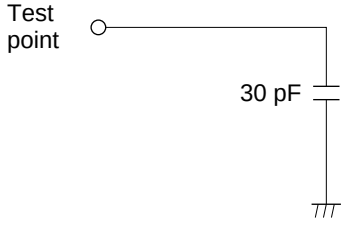
Load Circuits

Data Bus DB_0 to DB_7





External Driver Control Signals: CL_1, CL_2, D, M



Timing Characteristics

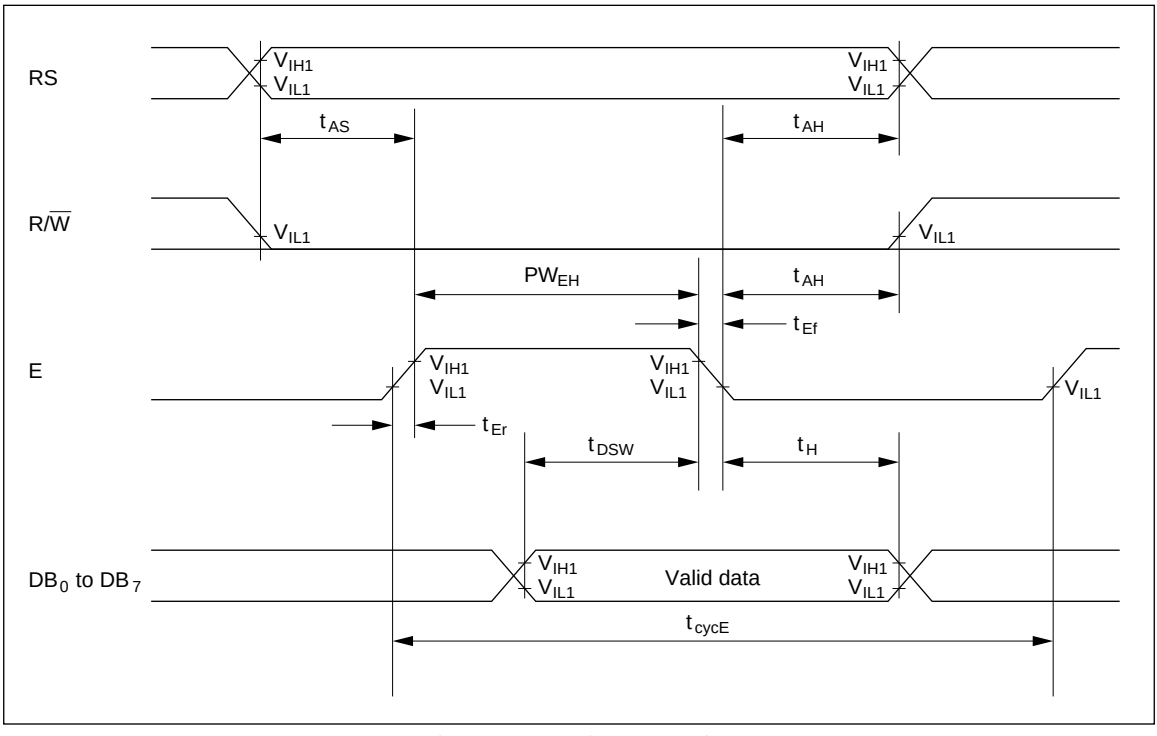
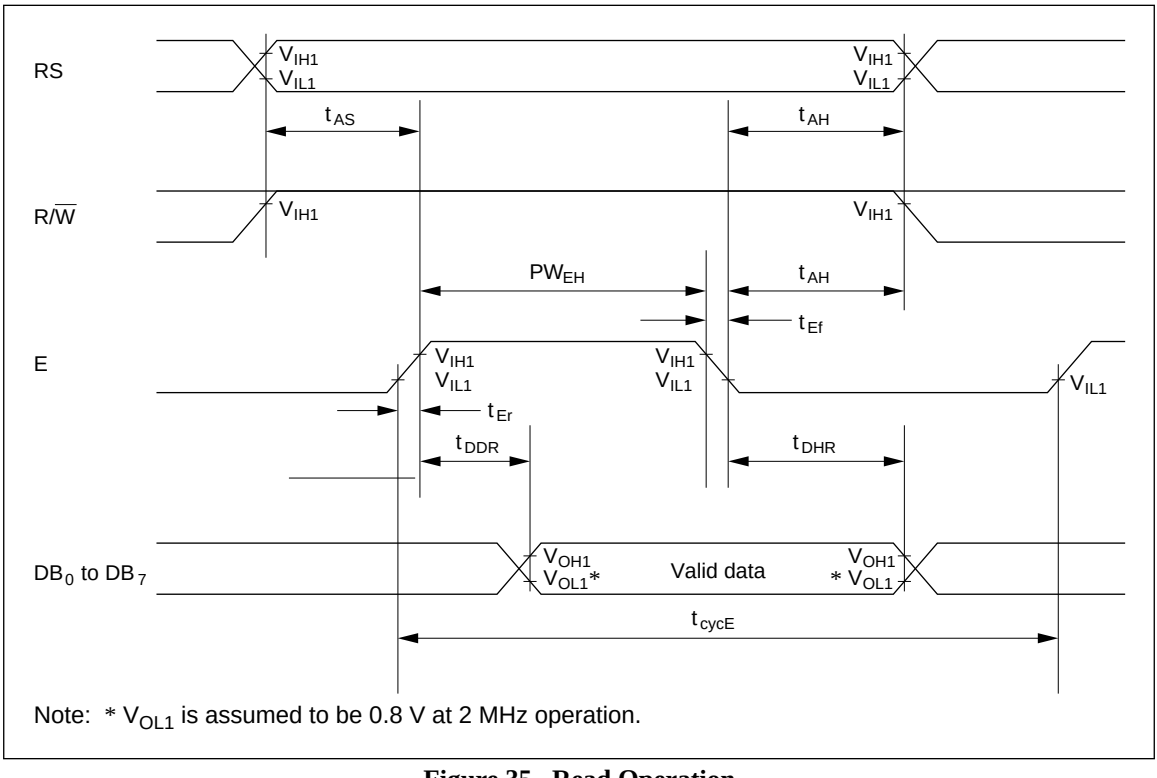


Figure 34 Write Operation



Note: * V_{OL1} is assumed to be 0.8 V at 2 MHz operation.

Figure 35 Read Operation

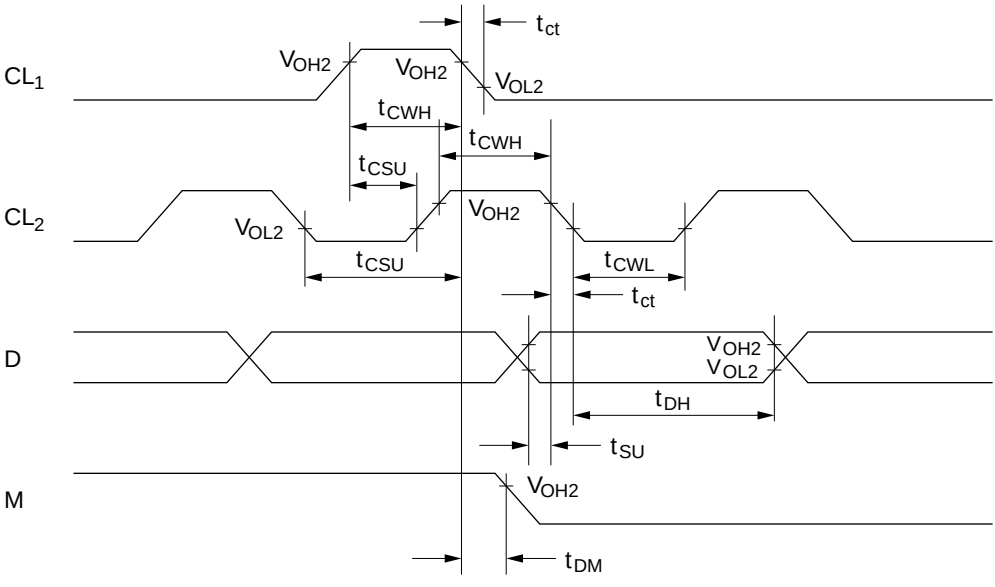
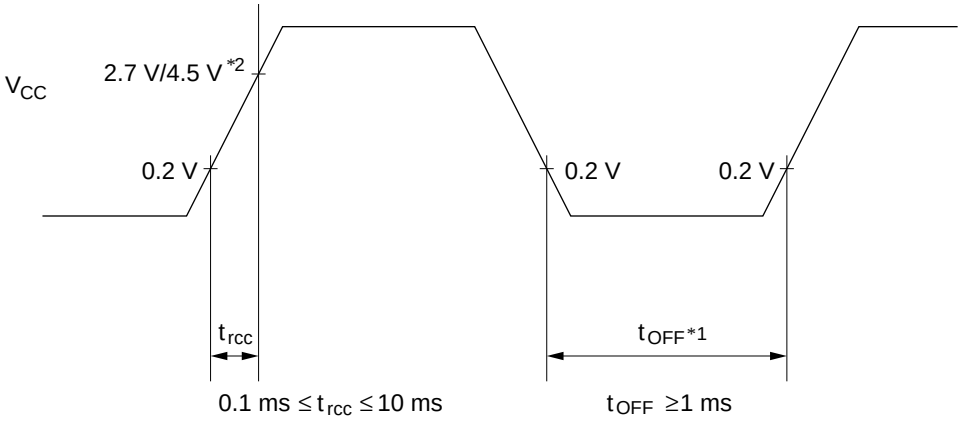


Figure 36 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. For if 4.5 V is not reached during 5-V operation, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 37 Internal Power Supply Reset

HD66702 (LCD-II/E20)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD66702 LCD-II/E20 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single LCD-II/E20 can display up to two 20-character lines. However, with the addition of HD44100 drivers, a maximum of up to two 40-character lines can be displayed.

The low 3-V power supply of the LCD-II/E20 under development is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 7 and 5 × 10 dot matrix possible
- 80 × 8-bit display RAM (80 characters max.)
- 7,200-bit character generator ROM
  - 160 character fonts (5 × 7 dot)
  - 32 character fonts (5 × 10 dot)
- 64 × 8-bit character generator RAM
  - 8 character fonts (5 × 7 dot)
  - 4 character fonts (5 × 10 dot)
- 16-common × 100-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 × 7 dots with cursor
  - 1/11 for one line of 5 × 10 dots with cursor
  - 1/16 for two lines of 5 × 7 dots with cursor
- Maximum display characters
  - One line

    1/8 duty cycle, 20-char. × 1-line (no extension), 28-char. × 1-line (extended with one HD44100R), 80-char. × 1-line (max. extension with eight HD44100s). 1/11 duty cycle, 20-char. × 1-line (no extension), 28-char. × 1-line (extended with one HD44100R), 80-char. × 1-line (max. extension with eight HD44100Rs)
  - Two lines

    1/16 duty cycle, 20-char. × 2-line (no extension), 28-char. × 2-line (extended with one HD44100R), 40-char. × 2-line (max. extension with eight HD44100Rs)
- Wide range of instruction functions
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Choice of power supply (V_{CC}): 4.5 to 5.5 V (standard), 2.7 to 5.5 V (low voltage)
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)
- Independent LCD drive voltage driven off of the logic power supply (V_{CC}): 3.0 to 8.3 V

Hitachi semiconductor

Ordering Information

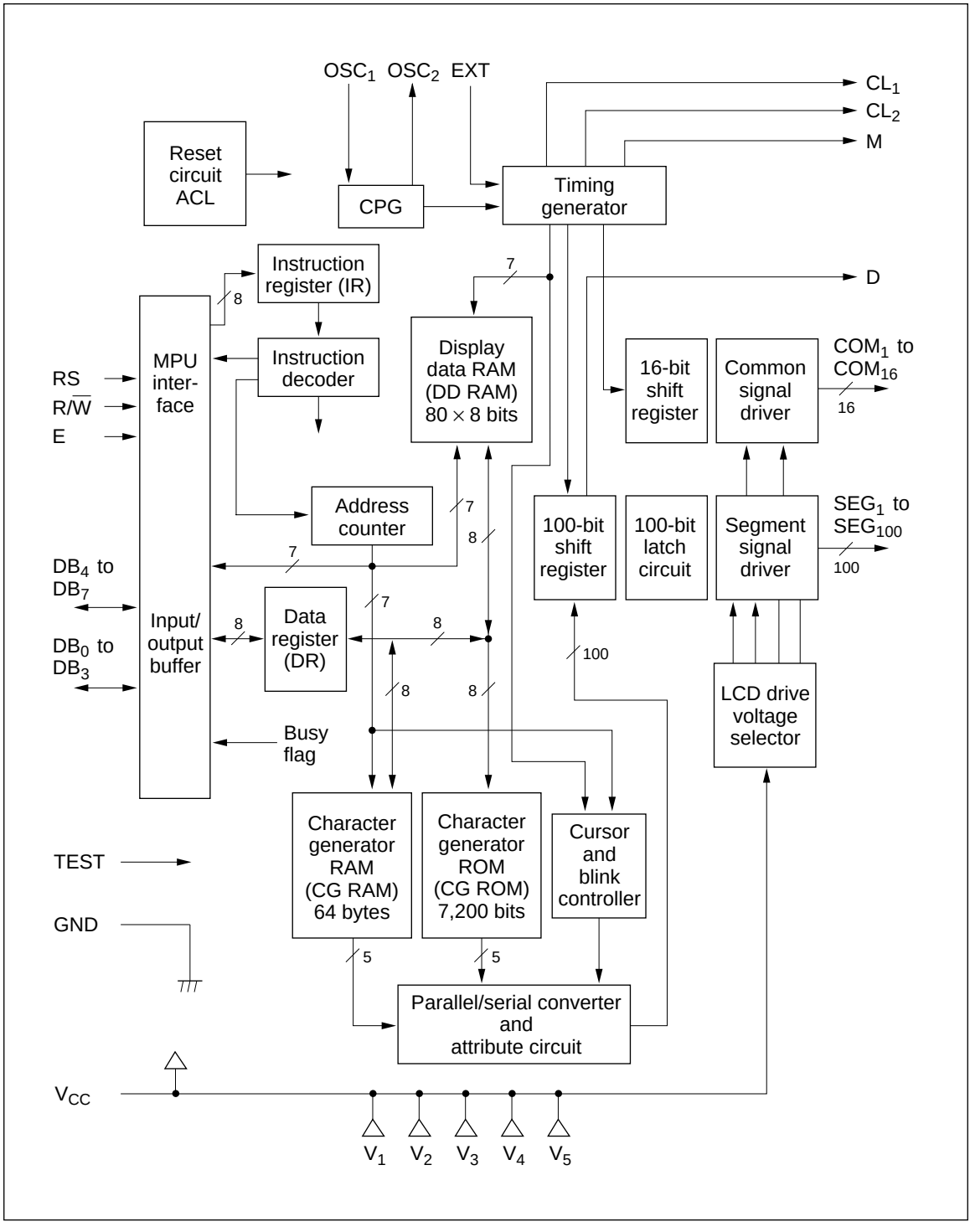
Type No.	Package	Operating Voltage	ROM Font
HCD66702RA00L	Chip	2.7 to 5.5 V	Standard Japanese font
HD66702RA00F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	
HD66702RA00FL	144-pin plastic QFP (FP-144A)	2.7 to 5.5 V	
HD66702RA01F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	Japanese font for comunication system
HD66702RA02F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	European font
HCD66702RBxxL	Chip	2.7 to 5.5 V	Custom font
HD66702RBxxF	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	
HD66702RBxxFL	144-pin plastic QFP (FP-144A)	2.7 to 5.5 V	

Note: xx: ROM code No.

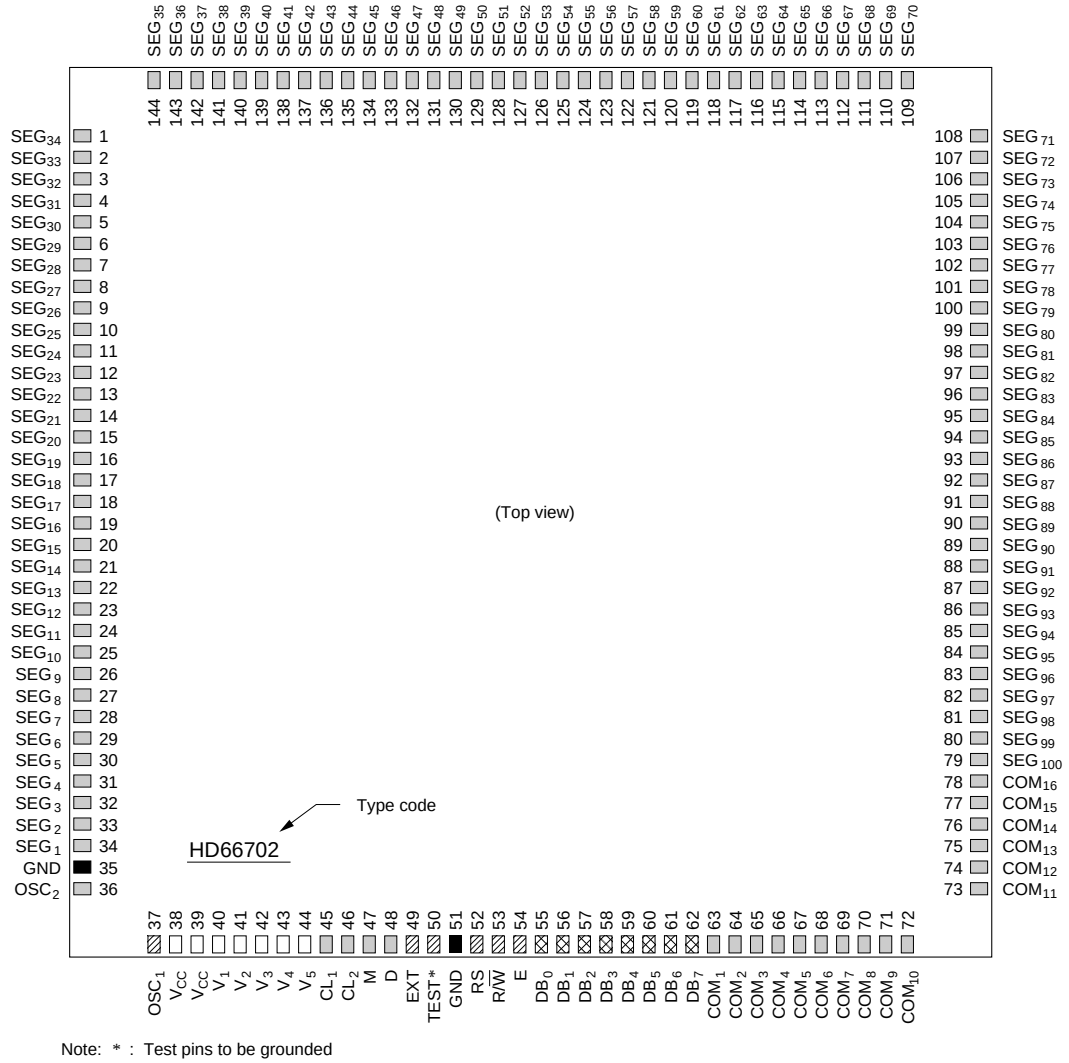
LCD-II Family Comparison

Item		LCD-II (HD44780U)	LCD-II/E20 (HD66702)
Power supply voltage		2.7 to 5.5 V	5 V ±10% (standard) 2.7 to 5.5 V (low voltage)
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11 V	3.0 to 8.3 V
	1/5 bias	3.0 to 11 V	3.0 to 8.3 V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	40 digits (20 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		9,600 bits (208 character fonts for 5 × 8 dot and 32 character fonts for 5 × 10 dot)	7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes
DDRAM		80 bytes	80 bytes
Segment signals		40	100
Common signals		16	16
Liquid crystal drive waveform		A	B
Ladder resistor for LCD power supply		External	External
Clock source		External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)		270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (69 to 128 Hz for 1/8 and 1/16 duty cycles; 50 to 93 Hz for 1/11 duty cycle)
R_f resistance		91 kΩ ±2% (5 V) 75 kΩ ±2% (3 V)	68 kΩ ±2% (5 V) 56 kΩ ±2% (3 V)
Instructions		Fully compatible within the LCD-II family	
CPU bus timing		1 MHz	1 MHz
Package		FP-80B, TFP-80, and 80-pin bare chip (no package)	144-pin bare chip (no package) and FP-144A

LCD-II/E20 Block Diagram



LCD-II/E20 Pad Arrangement



Note: * : Test pins to be grounded
□ : Power supply pins
■ : Power supply pins (ground)
▨ : Input pins
▯ : Output pins
⊠ : Input/Output pins

Minimum pad pitch = 130 µm

HCD66702 Pad Location Coordinates

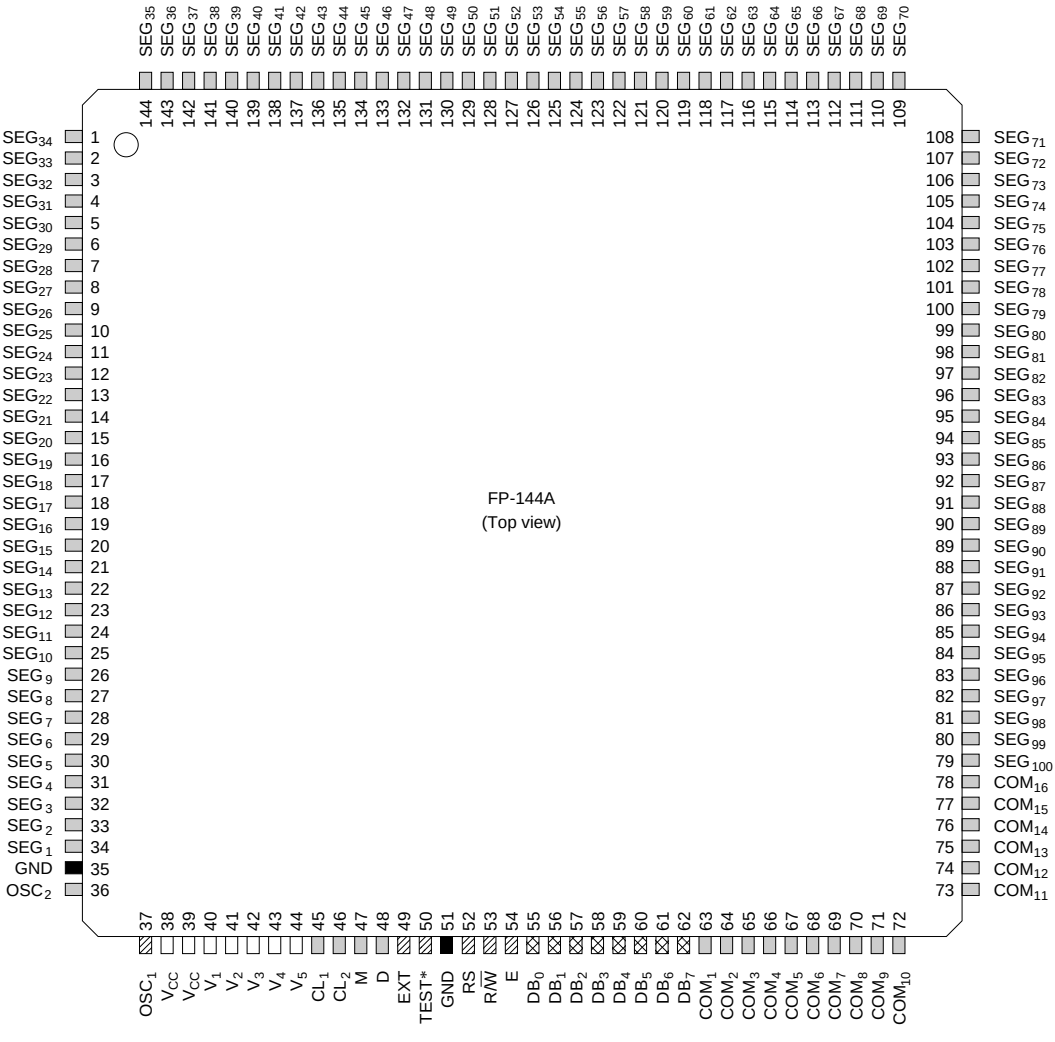
Pad No.	Pad Name	X (µm)	Y (µm)
1	SEG_{34}	–2475	2350
2	SEG_{33}	–2475	2205
3	SEG_{32}	–2475	2065
4	SEG_{31}	–2475	1925
5	SEG_{30}	–2475	1790
6	SEG_{29}	–2475	1655
7	SEG_{28}	–2475	1525
8	SEG_{27}	–2475	1395
9	SEG_{26}	–2475	1265
10	SEG_{25}	–2475	1135
11	SEG_{24}	–2475	1005
12	SEG_{23}	–2475	875
13	SEG_{22}	–2475	745
14	SEG_{21}	–2475	615
15	SEG_{20}	–2475	485
16	SEG_{19}	–2475	355
17	SEG_{18}	–2475	225
18	SEG_{17}	–2475	95
19	SEG_{16}	–2475	–35
20	SEG_{15}	–2475	–165
21	SEG_{14}	–2475	–295
22	SEG_{13}	–2475	–425
23	SEG_{12}	–2475	–555
24	SEG_{11}	–2475	–685
25	SEG_{10}	–2475	–815
26	SEG_{9}	–2475	–945
27	SEG_{8}	–2475	–1075
28	SEG_{7}	–2475	–1205
29	SEG_{6}	–2475	–1335
30	SEG_{5}	–2475	–1465
31	SEG_{4}	–2475	–1600
32	SEG_{3}	–2475	–1735
33	SEG_{2}	–2475	–1870
34	SEG_{1}	–2475	–2010
35	GND	–2475	–2180
36	OSC_2	–2475	–2325
37	OSC_1	–2445	–2475
38	V_{CC}	–2305	–2475
39	V_{CC}	–2165	–2475
40	V_1	–2025	–2475
41	V_2	–1875	–2475
42	V_3	–1745	–2475
43	V_4	–1595	–2475
44	V_5	–1465	–2475
45	CL_1	–1335	–2475
46	CL_2	–1185	–2475
47	M	–1055	–2475
48	D	–905	–2475
49	EXT	–775	–2475
50	TEST	–625	–2475
51	GND	–495	–2475
52	RS	–345	–2475
53	$R/\overline{W}$	–195	–2475
54	E	–45	–2475
55	DB_0	85	–2475
56	DB_1	235	–2475
57	DB_2	365	–2475
58	DB_3	515	–2475
59	DB_4	645	–2475
60	DB_5	795	–2475

Pad No.	Pad Name	X (µm)	Y (µm)
61	DB_6	925	–2475
62	DB_7	1075	–2475
63	COM_1	1205	–2475
64	COM_2	1335	–2475
65	COM_3	1465	–2475
66	COM_4	1595	–2475
67	COM_5	1725	–2475
68	COM_6	1855	–2475
69	COM_7	1990	–2475
70	COM_8	2125	–2475
71	COM_9	2265	–2475
72	COM_{10}	2410	–2475
73	COM_{11}	2475	–2290
74	COM_{12}	2475	–2145
75	COM_{13}	2475	–2005
76	COM_{14}	2475	–1865
77	COM_{15}	2475	–1730
78	COM_{16}	2475	–1595
79	SEG_{100}	2475	–1465
80	SEG_{99}	2475	–1335
81	SEG_{98}	2475	–1205
82	SEG_{97}	2475	–1075
83	SEG_{96}	2475	–945
84	SEG_{95}	2475	–815
85	SEG_{94}	2475	–685
86	SEG_{93}	2475	–555
87	SEG_{92}	2475	–425
88	SEG_{91}	2475	–295
89	SEG_{90}	2475	–165
90	SEG_{89}	2475	–35
91	SEG_{88}	2475	95
92	SEG_{87}	2475	225
93	SEG_{86}	2475	355
94	SEG_{85}	2475	485
95	SEG_{84}	2475	615
96	SEG_{83}	2475	745
97	SEG_{82}	2475	875
98	SEG_{81}	2475	1005
99	SEG_{80}	2475	1135
100	SEG_{79}	2475	1265
101	SEG_{78}	2475	1395
102	SEG_{77}	2475	1525
103	SEG_{76}	2475	1655
104	SEG_{75}	2475	1790
105	SEG_{74}	2475	1925
106	SEG_{73}	2475	2065
107	SEG_{72}	2475	2205
108	SEG_{71}	2475	2350
109	SEG_{70}	2320	2475
110	SEG_{69}	2175	2475
111	SEG_{68}	2035	2475
112	SEG_{67}	1895	2475
113	SEG_{66}	1760	2475
114	SEG_{65}	1625	2475
115	SEG_{64}	1495	2475
116	SEG_{63}	1365	2475
117	SEG_{62}	1235	2475
118	SEG_{61}	1105	2475
119	SEG_{60}	975	2475
120	SEG_{59}	845	2475

Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
121	SEG_{58}	715	2475	133	SEG_{46}	–845	2475
122	SEG_{57}	585	2475	134	SEG_{45}	–975	2475
123	SEG_{56}	455	2475	135	SEG_{44}	–1105	2475
124	SEG_{55}	325	2475	136	SEG_{43}	–1235	2475
125	SEG_{54}	195	2475	137	SEG_{42}	–1365	2475
126	SEG_{53}	65	2475	138	SEG_{41}	–1495	2475
127	SEG_{52}	–65	2475	139	SEG_{40}	–1625	2475
128	SEG_{51}	–195	2475	140	SEG_{39}	–1760	2475
129	SEG_{50}	–325	2475	141	SEG_{38}	–1895	2475
130	SEG_{49}	–455	2475	142	SEG_{37}	–2035	2475
131	SEG_{48}	–585	2475	143	SEG_{36}	–2175	2475
132	SEG_{47}	–715	2475	144	SEG_{35}	–2320	2475

Notes: 1. Coordinates originate from the chip center.
2. The above are preliminary specifications, and may be subject to change.

HD66702 Pin Arrangement



Note: * : Test pins to be grounded
□ : Power supply pins
■ : Power supply pins (ground)
▨ : Input pins
▭ : Output pins
⊠ : Input/Output pins

Pin Functions

Table 1 Pin Functional Description

Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	I	MPU	Selects read or write 0: Write 1: Read
E	I	MPU	Starts data read/write
DB_4 to DB_7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the LCD-II/E20. DB_7 can be used as a busy flag.
DB_0 to DB_3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the LCD-II/E20. These pins are not used during 4-bit operation.
CL_1	O	HD44100	Clock to latch serial data D sent to the HD44100H driver
CL_2	O	HD44100	Clock to shift serial data D
M	O	HD44100	Switch signal for converting the liquid crystal drive waveform to AC
D	O	HD44100	Character pattern data corresponding to each segment signal
COM_1 to COM_{16}	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM_9 to COM_{16} are non-selection waveforms at 1/8 duty factor and COM_{12} to COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1 to SEG_{100}	O	LCD	Segment signals
V_1 to V_5	—	Power supply	Power supply for LCD drive
V_{CC}, GND	—	Power supply	V_{CC}: +5 V or +3 V, GND: 0 V
TEST	I	—	Test pin, which must be grounded
EXT	I	—	0: Enables extension driver control signals CL_1, CL_2, M, and D to be output from its corresponding pins. 1: Drives CL_1, CL_2, M, and D as tristate, lowering power dissipation.
OSC_1, OSC_2	—	—	Pins for connecting the registers of the internal clock oscillation. When the pin input is an external clock, it must be input to OSC_1.

Function Description

Registers

The HD66702 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into DD RAM or CG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM or CG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66702 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output to DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DD RAM and CG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DD RAM or CG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM or CG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)

  — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66702, 20 characters are displayed. See figure 3.

  When the display shift operation is performed, the DD RAM address shifts. See figure 3.

  — Case 2: For a 28-character display, the HD66702 can be extended using one HD44100 and displayed. See figure 4.

  When the display shift operation is performed, the DD RAM address shifts. See figure 4.

  — Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased through the use of two or more HD44100s can be considered as an extension of case #2.

  Since the increase can be eight digits per additional HD44100, up to 80 digits can be displayed by externally connecting eight HD44100s. See figure 5.

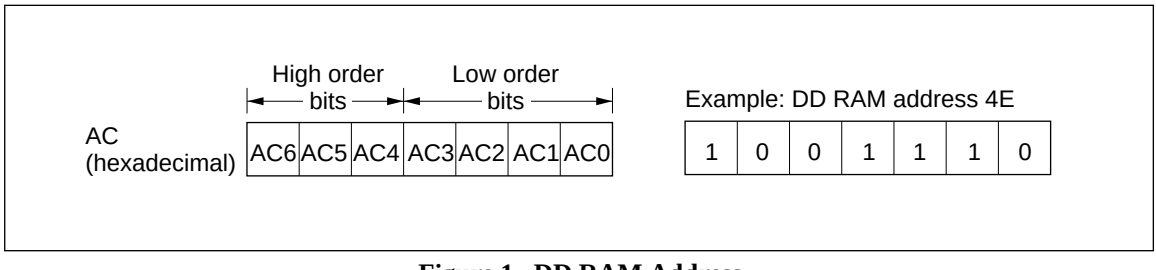


Figure 1 DD RAM Address

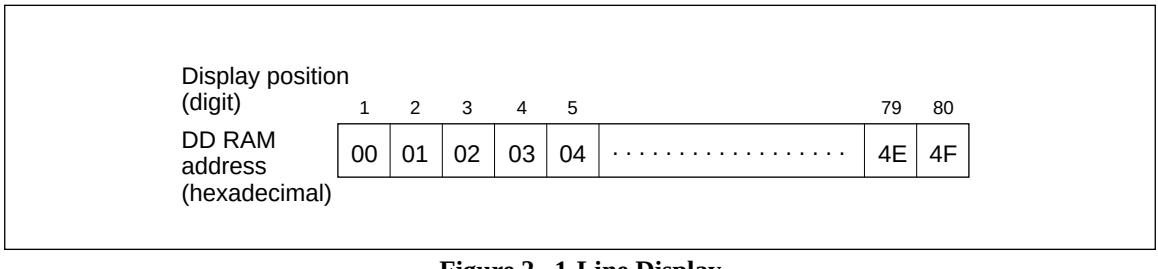


Figure 2 1-Line Display

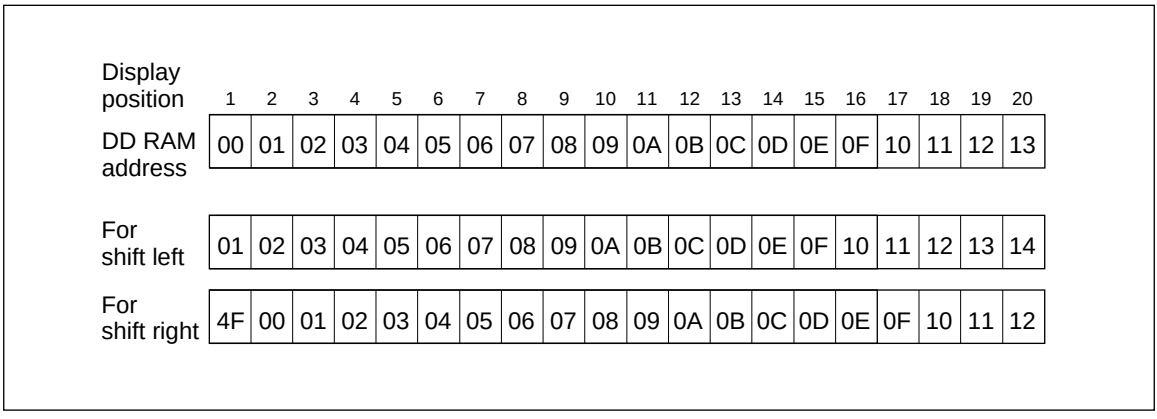


Figure 3 1-Line by 20-Character Display Example

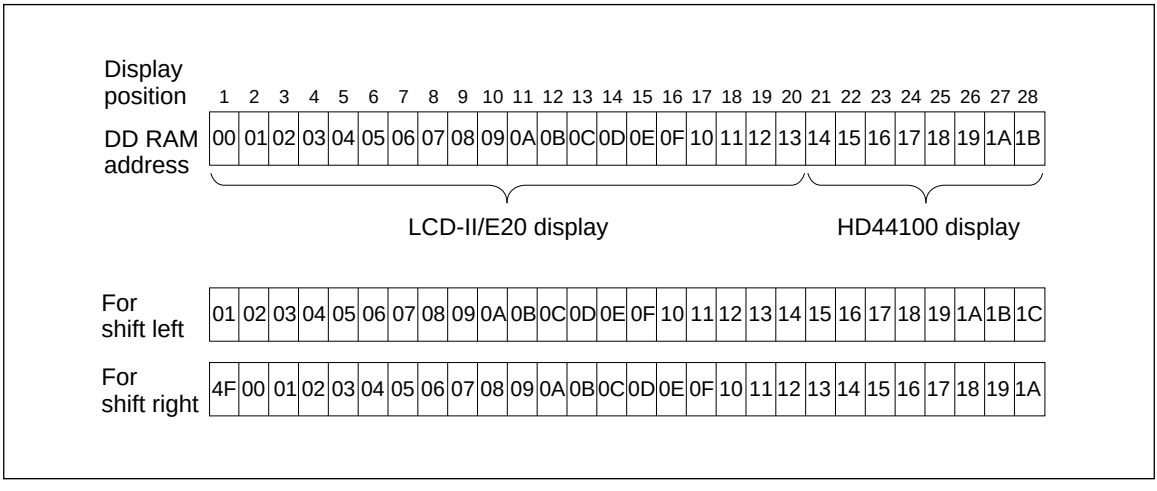


Figure 4 1-Line by 28-Character Display Example

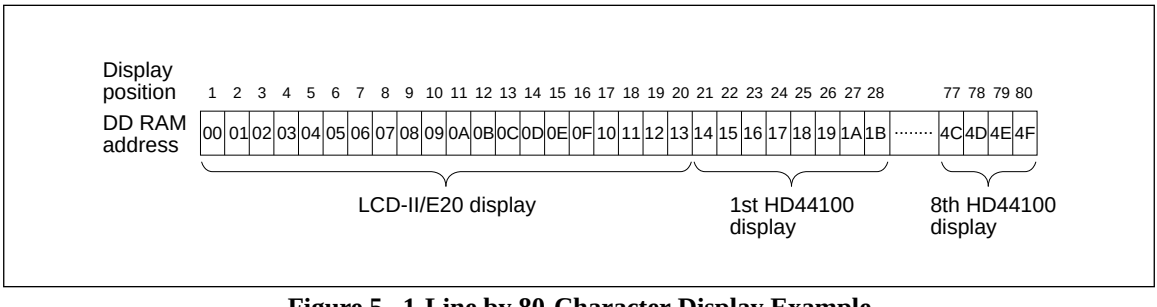


Figure 5 1-Line by 80-Character Display Example

- 2-line display (N = 1) (figure 6)

  — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD66702 is used, 20 characters × 2 lines are displayed. See figure 7.

  When display shift operation is performed, the DD RAM address shifts. See figure 7.

Display position	1	2	3	4	5		39	40
DD RAM address (hexadecimal)	00	01	02	03	04	· · · · · · · · · · · · · · · · · ·	26	27
	40	41	42	43	44	· · · · · · · · · · · · · · · · · ·	66	67

Figure 6 2-Line Display

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52

Figure 7 2-Line by 20-Character Display Example

— Case 2: For a 28-character × 2-line display, the HD66702 can be extended using one HD44100. See figure 8.

When display shift operation is performed, the DD RAM address shifts. See figure 8.

— Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased by using two or more HD44100s, can be considered as an extension of case #2. See figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100, up to 40 digits × 2 lines can be displayed by externally connecting three HD44100s.

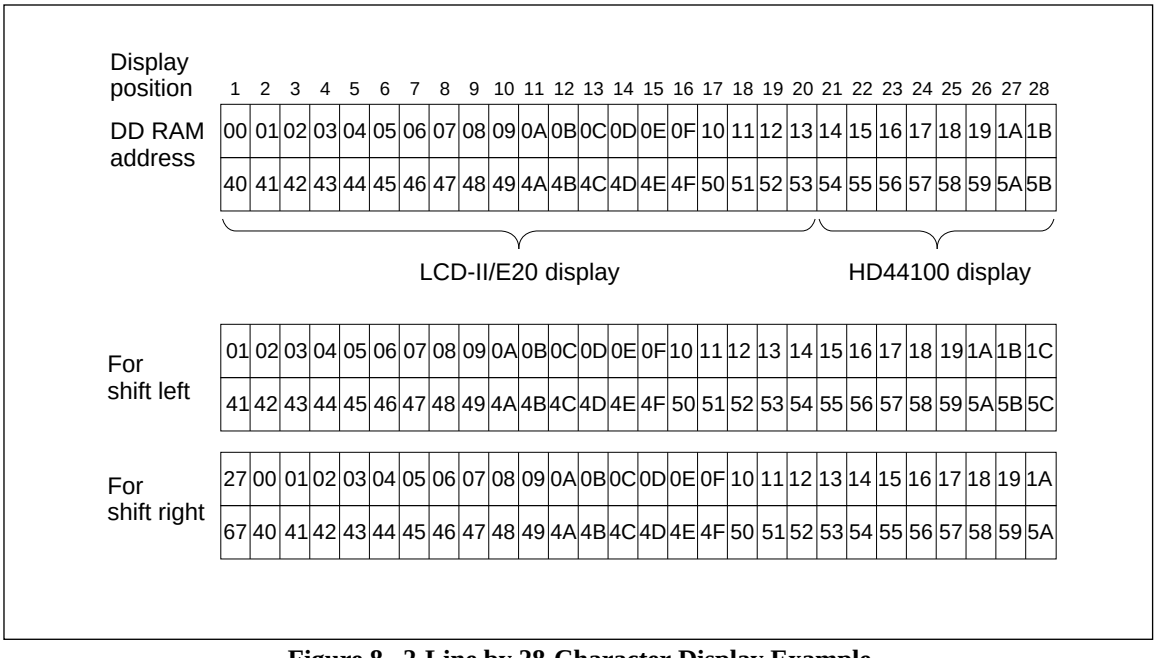


Figure 8 2-Line by 28-Character Display Example

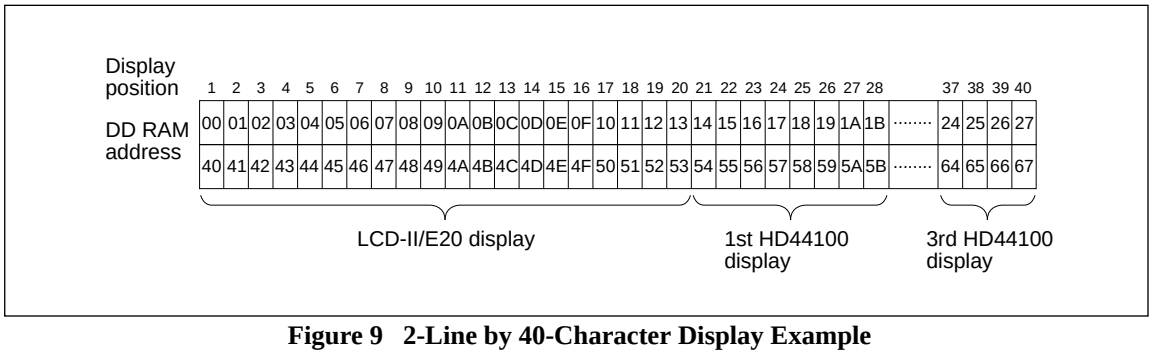


Figure 9 2-Line by 40-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes (table 5). It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 7 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written.

Write the character codes at the addresses shown as the left column of table 5 to show the character patterns stored in CG RAM.

See table 6 for the relationship between CG RAM addresses and data and display patterns.

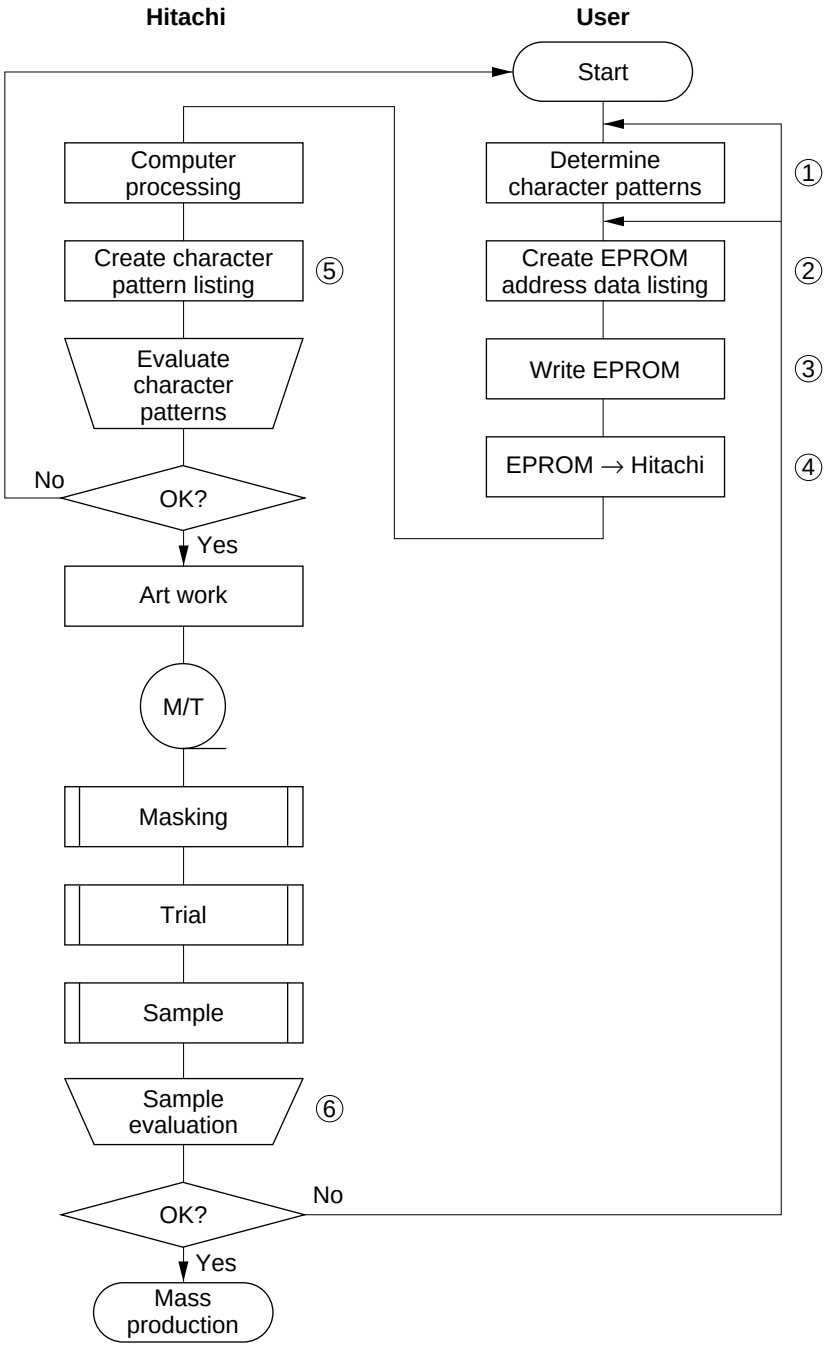
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 10 Character Pattern Development Procedure

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II/E20 character generator ROM can generate 160 5×7 dot character patterns and 32 5×10 dot character patterns for a total of 192 different character patterns.

— 5×7 dot character pattern

EPROM address data and character pattern data correspond with each other to form a 5×7 dot character pattern (table 3).

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5×7 dots)

EPROM Address											Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	LSB O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Character code — Line position

← Fill line 8 (cursor position) with 0s

Notes:
1. EPROM addresses A_{10} to A_3 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. A lit display position (black) corresponds to a 1.
5. Line 8 (cursor position) of the character pattern must be blanked with 0s.
6. EPROM data O_5 to O_7 are not used.

— 5 × 10 dot character pattern

EPROM address data and character pattern data correspond with each other to form a 5 × 10 dot character pattern (table 4).

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** Ignored by the character generator ROM for display operation so 0 or 1 is arbitrary.
2. **EPROM data in CG RAM area:** Ignored by the character generator ROM for display operation so 0 or 1 is arbitrary.
3. **EPROM data used when the user does not use any HD66702 character pattern:** According to the user application, handled in one of the two ways listed as follows.
   a. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)
   b. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM Address												Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		O_4	O_3	O_2	O_1	LSB O_0
								0	0	0		0	0	0	0	0
								0	0	1		0	0	0	0	0
								0	1	0		0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1		1	0	0	1	1
								1	0	0		1	0	0	0	1
								1	0	1		1	0	0	0	1
								1	1	0		0	1	1	1	1
								1	1	1		0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0		0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1		0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0		0	0	0	0	0

← Fill line 11 (cursor position) with 0s

Character code — Line position

Notes:
1. EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern lines 9, 10, and 11 to 0s.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. A lit display position (black) corresponds to a 1.
5. Blank out line 11 (cursor position) of the character pattern with 0s.
6. EPROM data O_5 to O_7 are not used.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A00)

Lower 4 Bits \ Upper 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

Note: The user can specify any pattern for character-generator RAM.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A01)

Upper 4 Bits / Lower 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A02)

Upper 4 Bits / Lower 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

Table 6 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

For 5 × 7 dot character patterns

Character Codes (DD RAM data)	CG RAM Address	Character Patterns (CG RAM data)	
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low	7 6 5 4 3 2 1 0 High Low	
0 0 0 0 * 0 0 0	0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * 0 0 0 0 0	Character pattern Cursor position
0 0 0 0 * 0 0 1	0 0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * 0 0 0 0 0	
0 0 0 0 * 1 1 1	1 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 0 1 1 1	* * *	

Notes: 1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).

2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.
   If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0 to 4 (bit 4 being at the left). Since CG RAM data bits 5 to 7 are not used for display, they can be used for general data RAM.
4. As shown tables 5 and 6, CG RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Table 6 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data) (cont)

For 5 × 10 dot character patterns

Character Codes (DD RAM data)	CG RAM Address	Character Patterns (CG RAM data)	
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low	7 6 5 4 3 2 1 0 High Low	
0 0 0 0 * 0 0 *	0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0	* * * 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 1 1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 * * * 0 0 0 0 0	Character pattern Cursor position
	1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* * * * * * * * * * * * * * * *	
0 0 0 0 * 1 1 *	0 0 0 0 0 0 0 1 1 0 0 1 1 0 1 0	* * * * * *	
	1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* * * * * * * * * * * * * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CG RAM address bits 4 and 5 (2 bits: 4 types).

2. CG RAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.
   If the 11th line data is 1, 1 bits will light up the 11th line regardless of the cursor presence.
   Since lines 12 to 16 are not used for display, they can be used for general data RAM.

3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4. CG RAM character patterns are selected when character code bits 4 to 7 are all 0.
   However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area. This circuit also generates timing signals for the operation of the externally connected HD44100 driver.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 100 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the HD44100 driver. Character pattern data is sent serially through a 100-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs. The serial data can be sent to externally cascaded HD44100s used for displaying extended digit numbers.

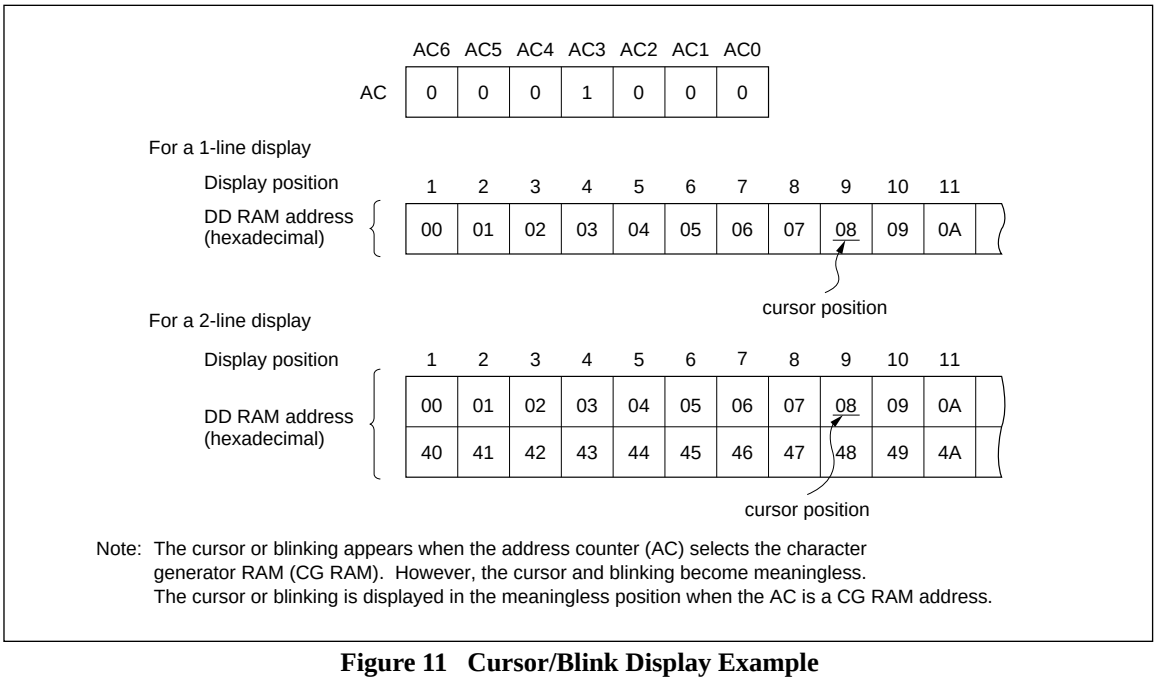
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66702 drives from the head display. The rest of the display, corresponding to latter addresses, are added with each additional HD44100.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DD RAM) address set in the address counter (AC).

For example (figure 11), when the address counter is 08H, the cursor position is displayed at DD RAM address 08H.



Note: The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CG RAM). However, the cursor and blinking become meaningless. The cursor or blinking is displayed in the meaningless position when the AC is a CG RAM address.

Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD66702 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66702 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

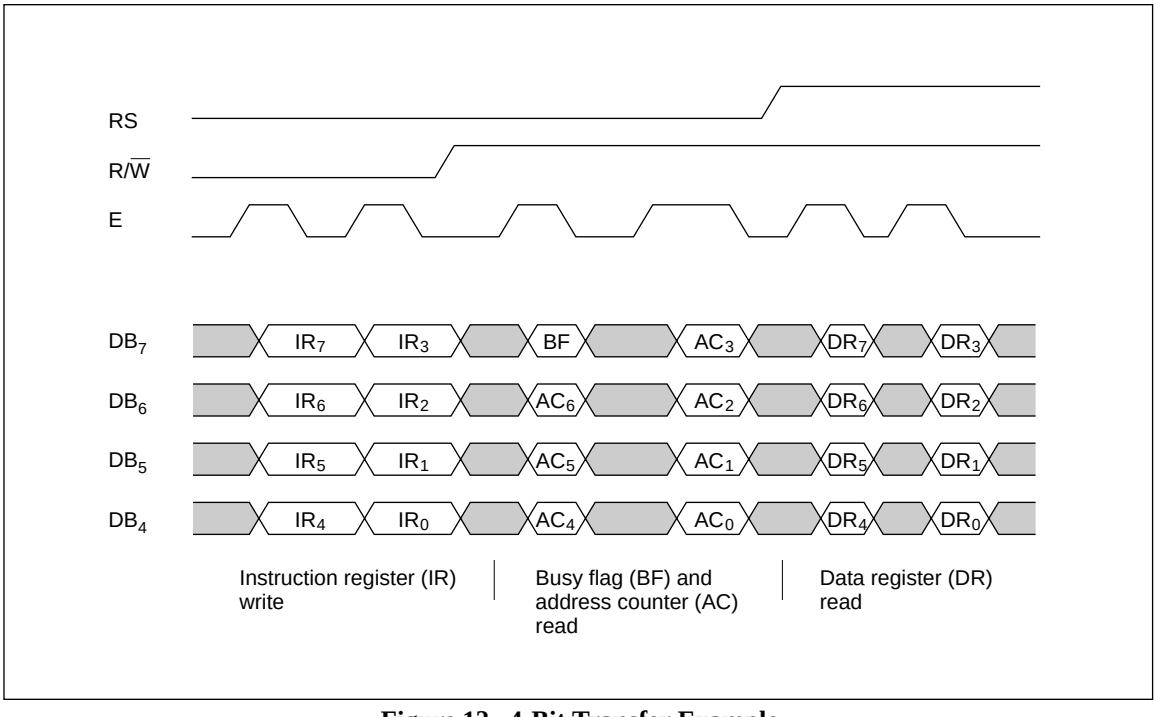


Figure 12 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66702 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 7 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66702. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66702 can be controlled by the MPU. Before starting the internal operation of the HD66702, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66702 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD66702 instructions (table 7). There are four categories of instructions that:

- Designate HD66702 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66702 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 12) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66702 is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD66702. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 7 for the list of each instruc-tion execution time.

Table 7 Instructions

Instruction	Code										Description	Execution Time (max) (when f_{cp} or f_{OSC} is 320 kHz)
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.28 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.28 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	31 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	31 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	31 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (L), and character font (F).	31 µs
Set CG RAM address	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	31 µs
Set DD RAM address	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	31 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 7 Instructions (cont)

Instruction	Code RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 320 kHz)
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM.	31 µs t_{ADD} = 4.7 µs*
Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	31 µs t_{ADD} = 4.7 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 7 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 270 kHz, $31\ \mu s \times \frac{320}{270} = 37\ \mu s$

Note: — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

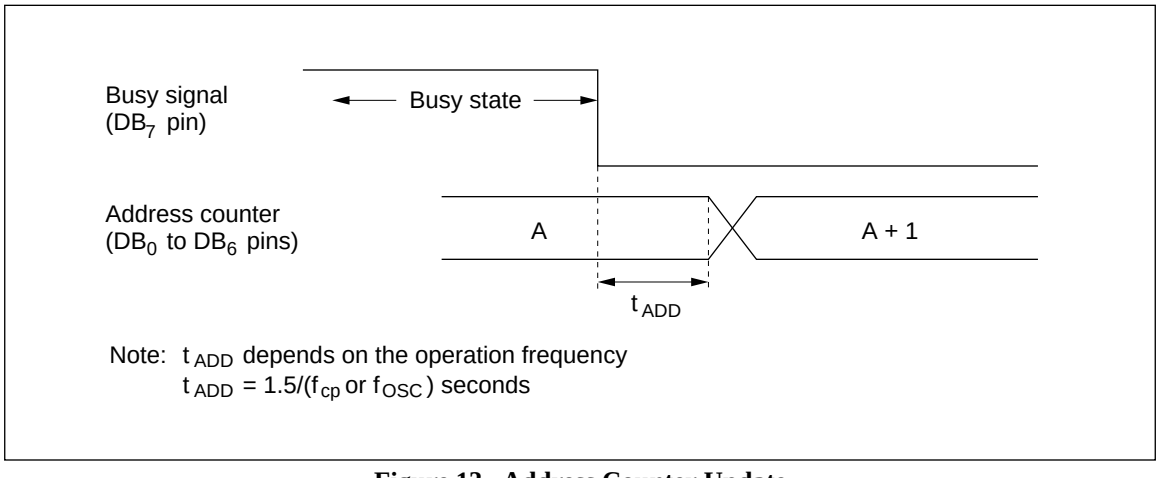


Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×7 dot character font selection and in the 11th line for the 5×10 dot character font selection (figure 16).

B: The character indicated by the cursor blinks when B is 1 (figure 16). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 320-ms intervals when f_{cp} or f_{OSC} is 320 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $320 \times 320/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

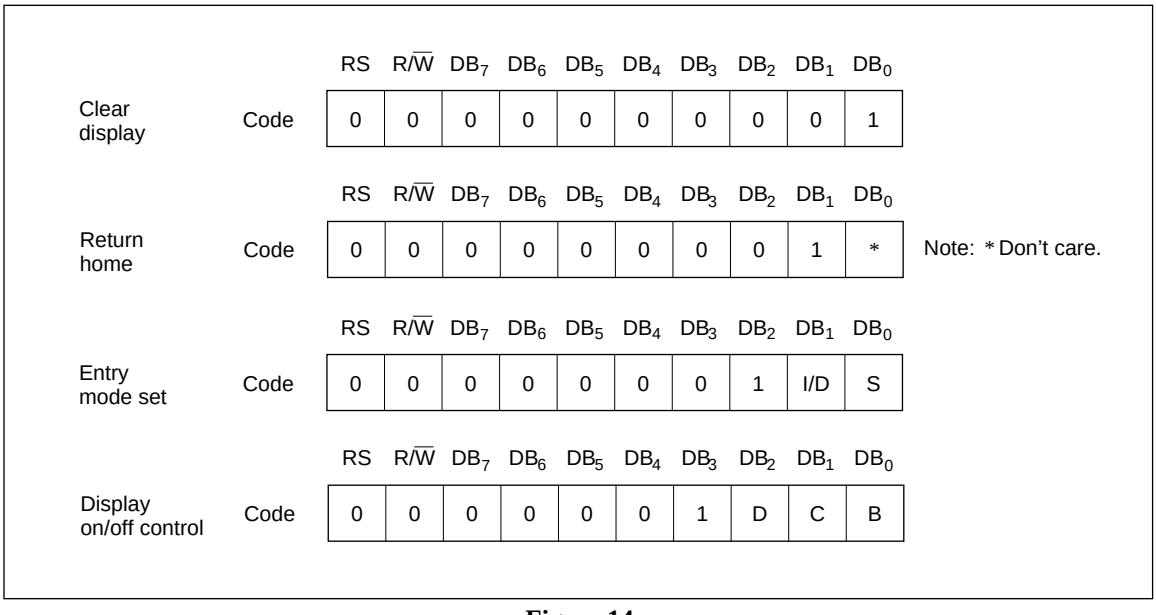


Figure 14

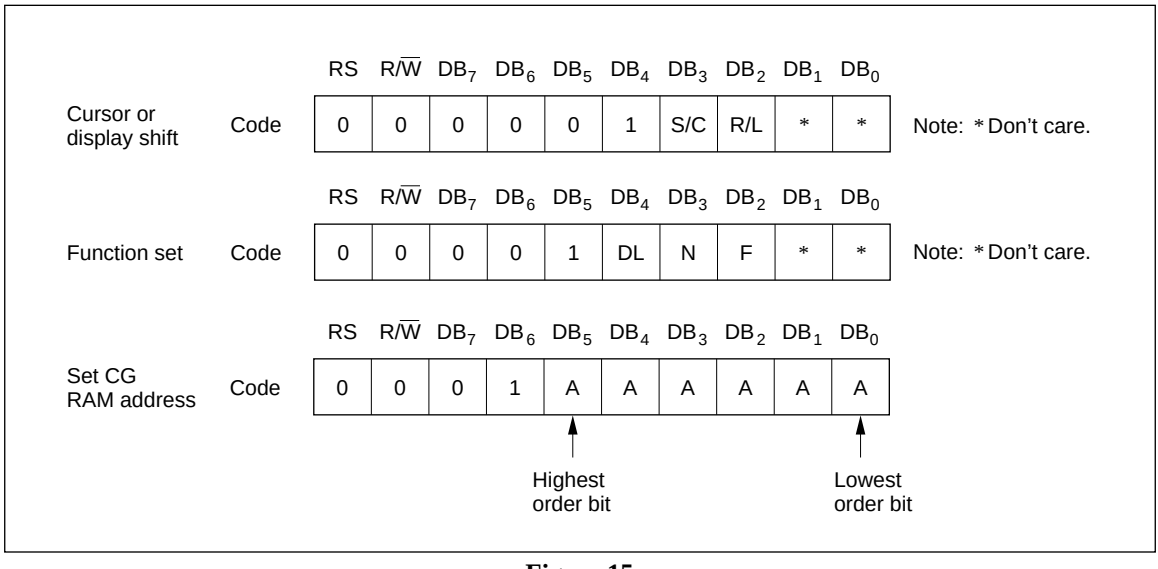


Figure 15

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DD RAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG RAM address and set DD RAM address.

Table 8 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 9 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 7 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 7 dots	1/16	Cannot display two lines for 5 × 10 dot character font.

Note: * Indicates don't care.

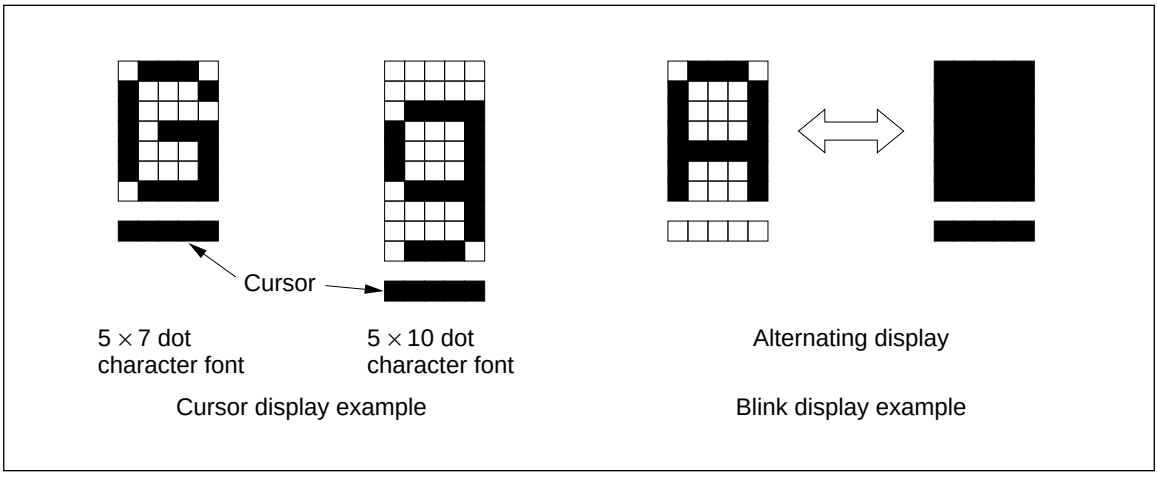


Figure 16 Cursor and Blinking

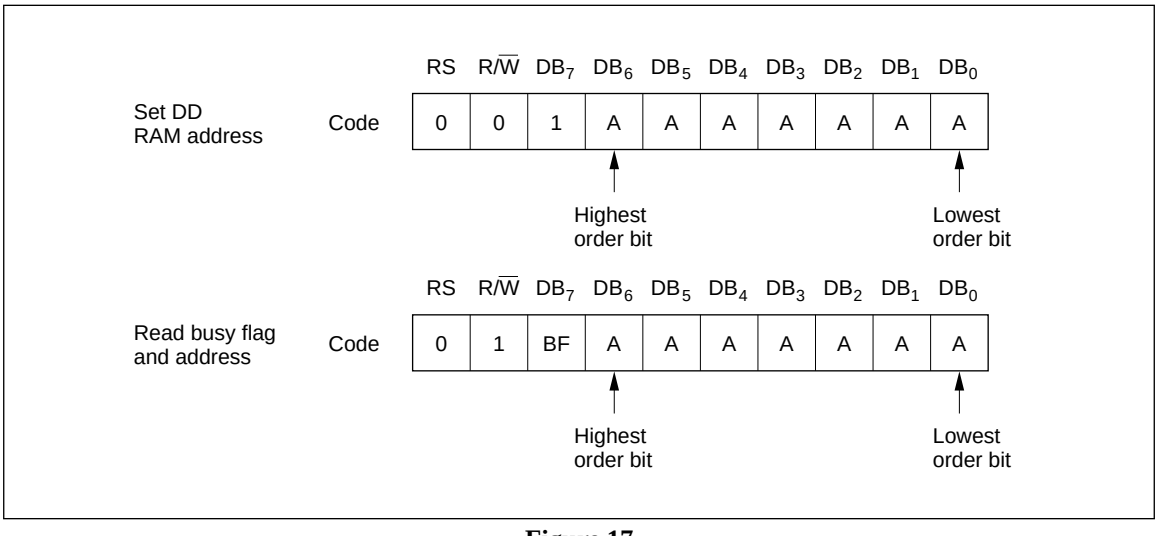


Figure 17

Write Data to CG or DD RAM

Write data to CG or DD RAM writes 8-bit binary data DDDDDDDD to CG or DD RAM.

To write into CG or DD RAM is determined by the previous specification of the CG RAM or DD RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DD RAM

Read data from CG or DD RAM reads 8-bit binary data DDDDDDDD from CG or DD RAM.

The previous designation determines whether CG or DD RAM is to be read. Before entering this read instruction, either CG RAM or DD RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD RAM). The operation of the cursor shift instruction is the same as the set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CG RAM or DD RAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

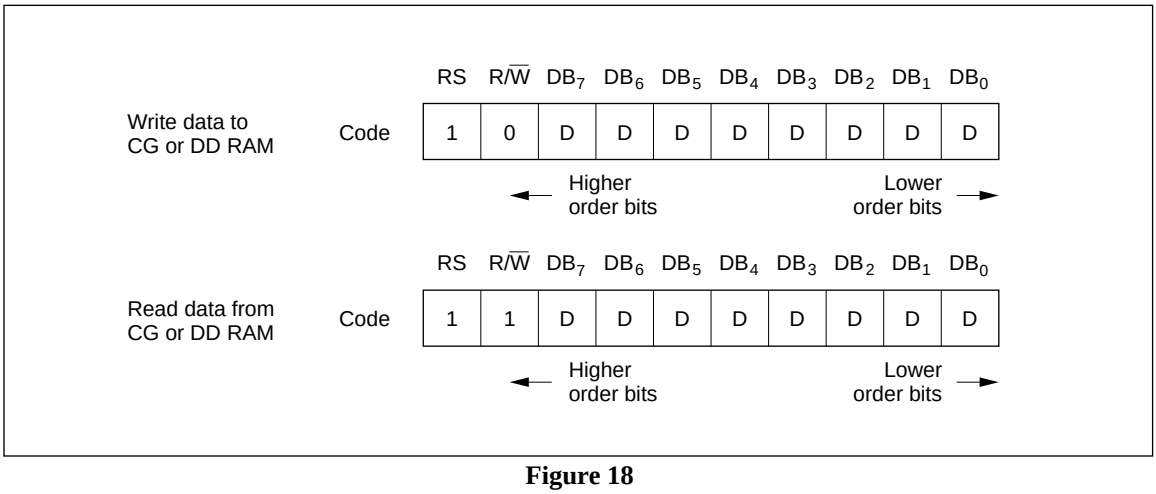


Figure 18

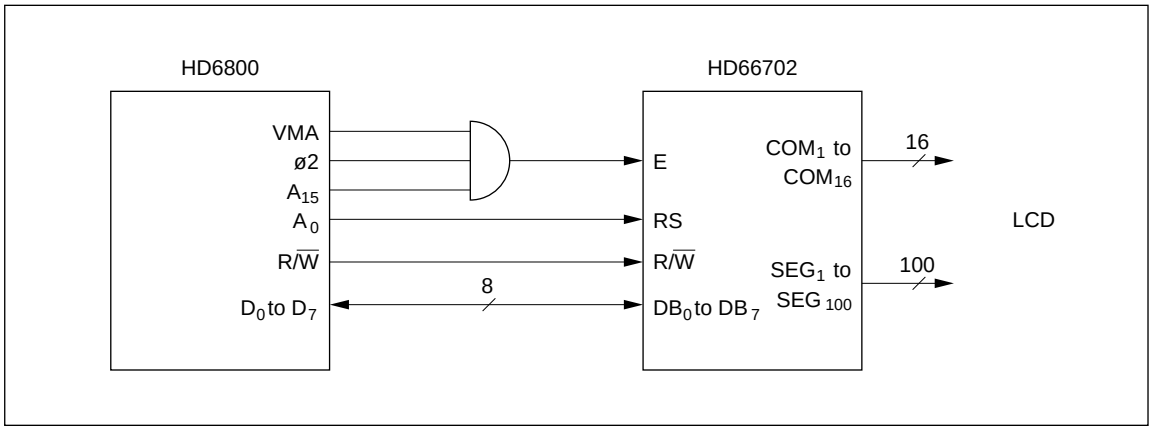


Figure 19 8-Bit MPU Interface

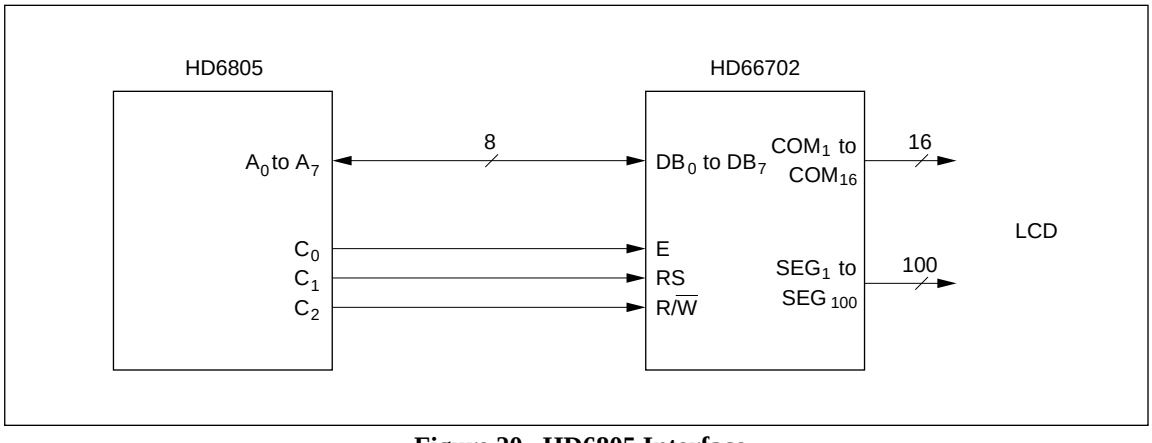


Figure 20 HD6805 Interface

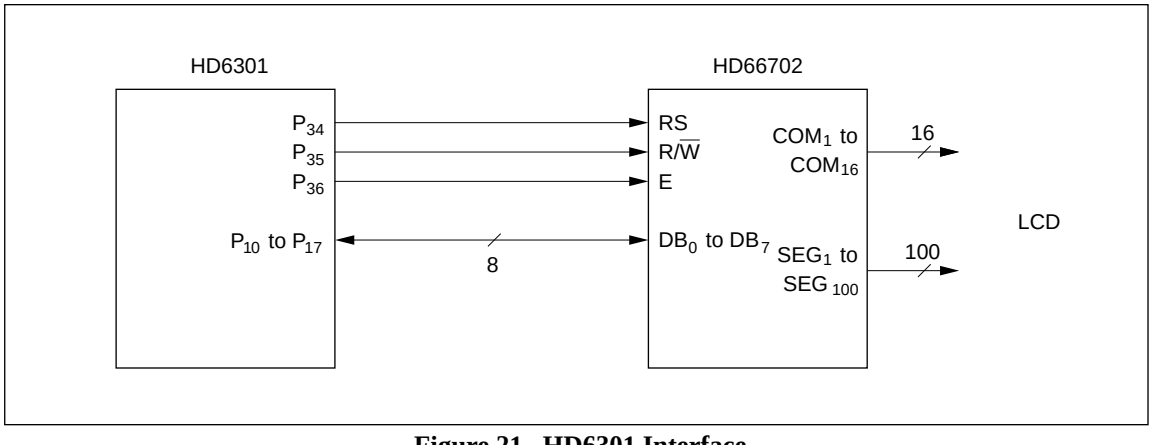


Figure 21 HD6301 Interface

Interfacing the HD66702

Interface to MPUs

- Interfacing to an 8-bit MPU through a PIA

  See figure 23 for an example of using a PIA or I/O port (for a single-chip microcomputer) as an interface device. The input and output of the device is TTL compatible.

In this example, PB_0 to PB_7 are connected to the data bus DB_0 to DB_7, and PA_0 to PA_2 are connected to E, R/$\overline{W}$, and RS, respectively.

Pay careful attention to the timing relationship between E and the other signals when reading or writing data using a PIA for the interface.

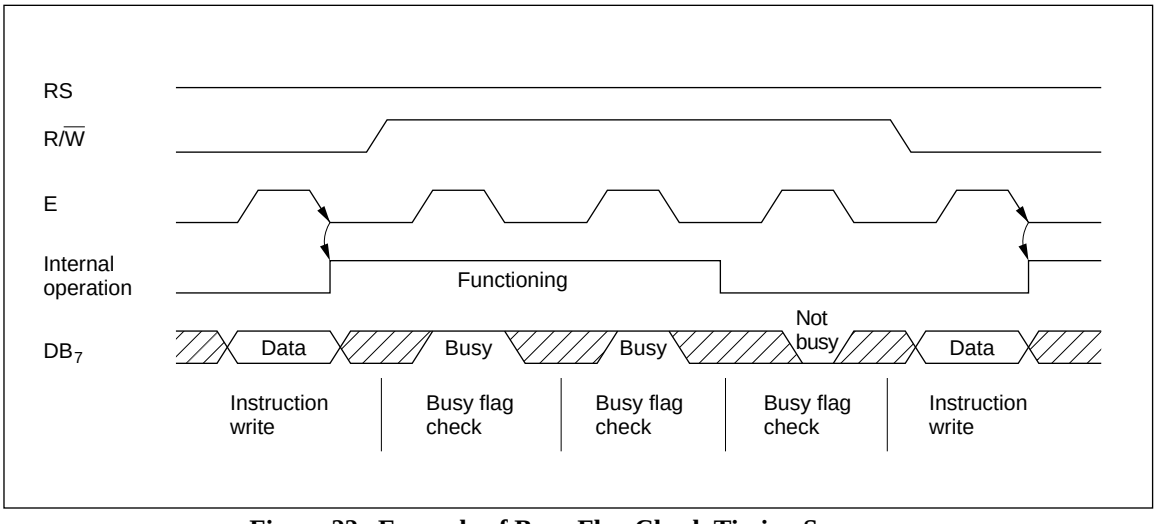


Figure 22 Example of Busy Flag Check Timing Sequence

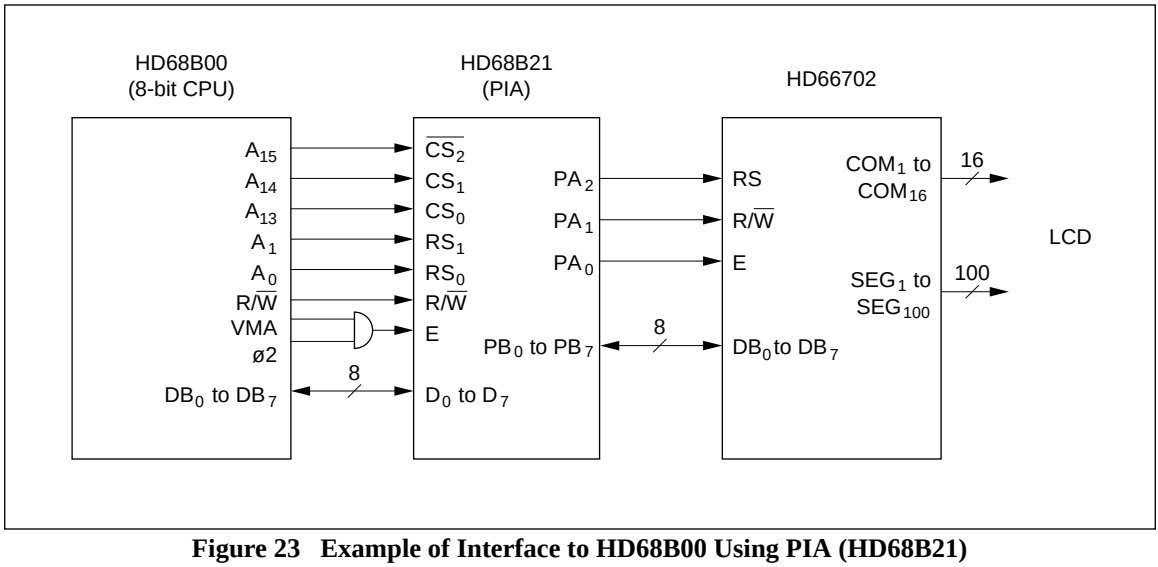


Figure 23 Example of Interface to HD68B00 Using PIA (HD68B21)

- Interfacing to a 4-bit MPU

  The HD66702 can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See figure 24.)

  See figure 25 for an interface example to the HMCS43C.

  Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.

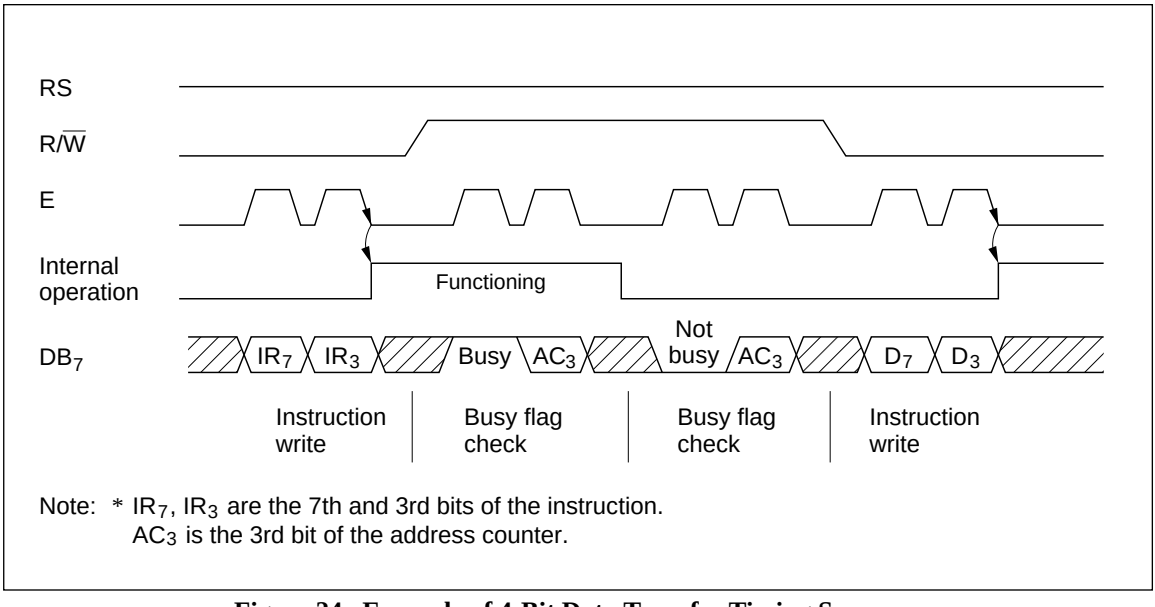


Figure 24 Example of 4-Bit Data Transfer Timing Sequence

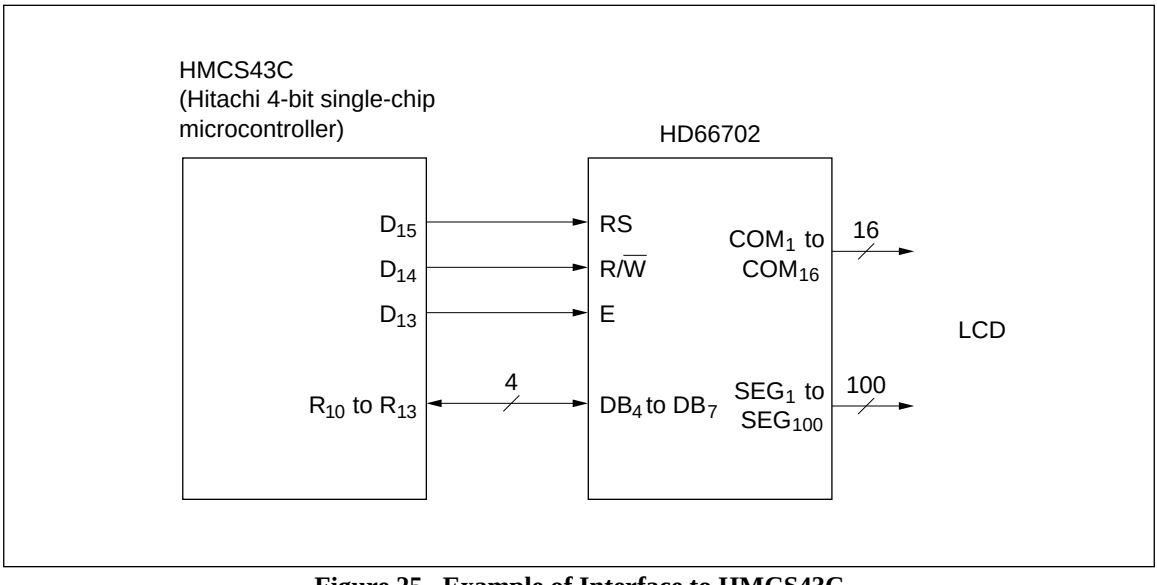


Figure 25 Example of Interface to HMCS43C

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66702 can perform two types of displays, 5 × 7 dot and 5 × 10 dot character fonts, each with a cursor.

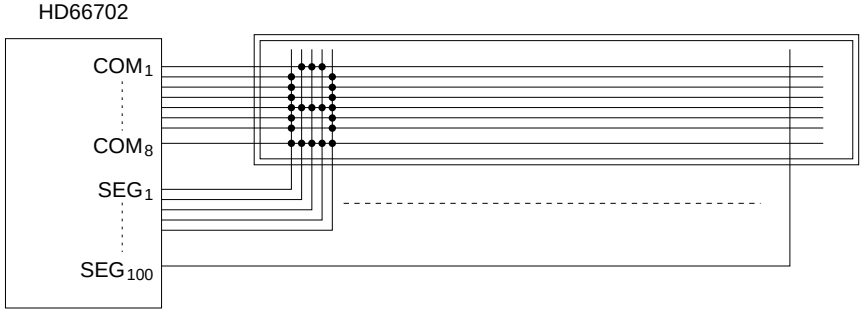
Up to two lines are displayed for 5 × 7 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (table 10).

The number of lines and font types can be selected by the program. (See table 7, Instructions.)

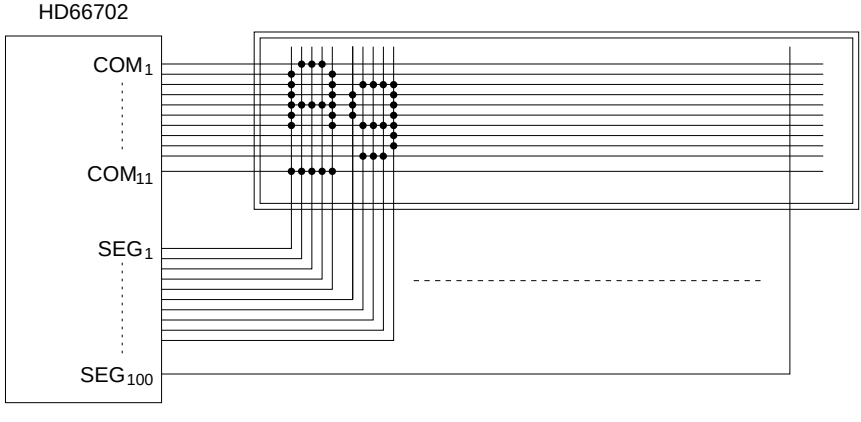
Connection to HD66702 and Liquid Crystal Display: See figure 26 for the connection examples.

Table 10 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 7 dots + cursor	16	1/16



Example of a 5×7 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

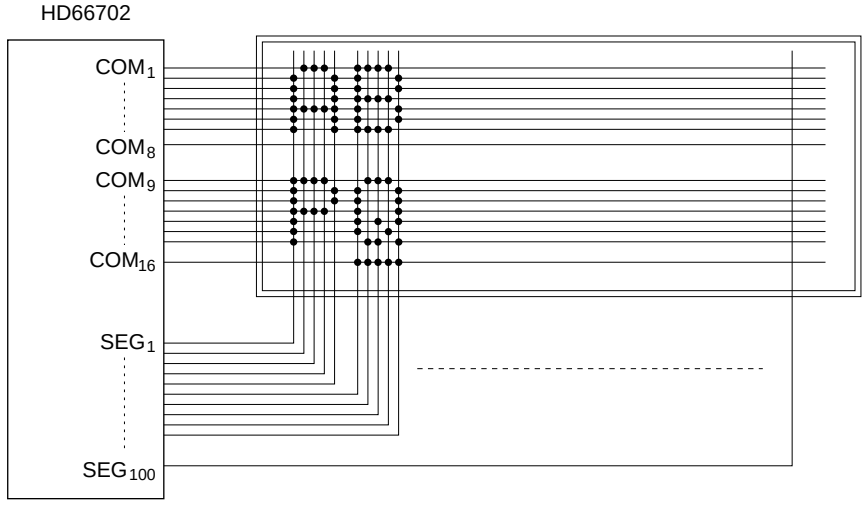


Example of a 5×10 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 26 Liquid Crystal Display and HD66702 Connections

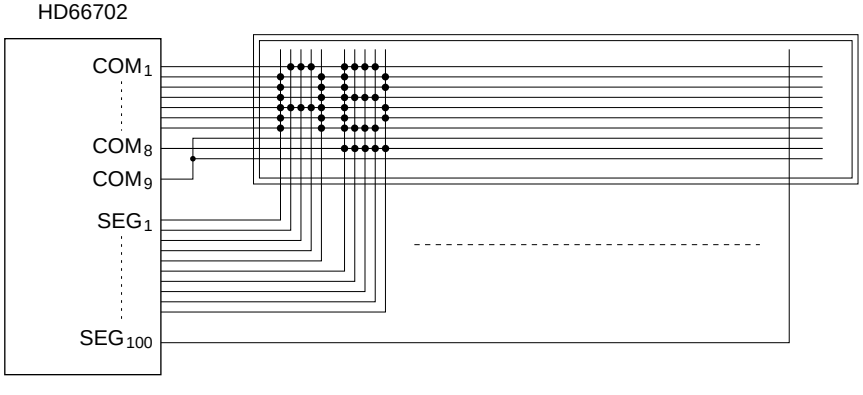
Since five segment signal lines can display one digit, one HD66702 can display up to 20 digits for a 1-line display and 40 digits for a 2-line display.

The examples in figure 26 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (figure 28).



Example of a 5×7 dot, 20-character × 2-line display (1/5 bias, 1/16 duty cycle)

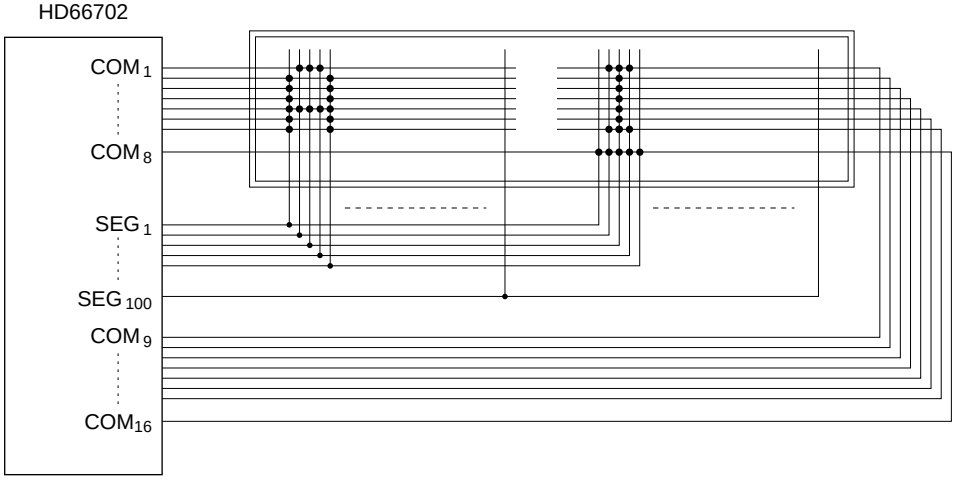
Figure 27 Liquid Crystal Display and HD66702 Connections (cont)



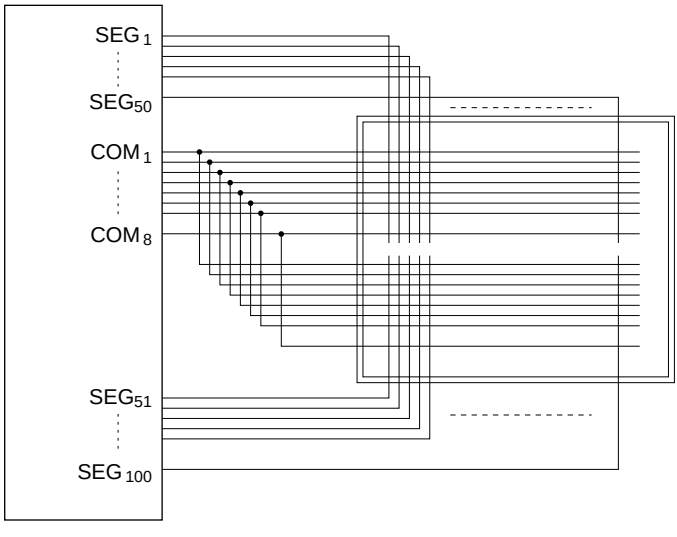
5 × 7 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 28 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (figure 29) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DD RAM) addresses for 10 characters × 2 lines and for 40 characters × 1 line are the same as in figure 27.



5 × 7 dot, 40-character × 1-line display
(1/5 bias, 1/16 duty cycle)



5 × 7 dot, 10-character × 2-line display
(1/4 bias, 1/8 duty cycle)

Figure 29 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V_1 to V_5 of the HD66702 to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (table 11).

V_{LCD} is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V_1 to V_5 (figure 30).

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Power Supply	1/4	1/5
V_1	V_{CC}–1/4 V_{LCD}	V_{CC}–1/5 V_{LCD}
V_2	V_{CC}–1/2 V_{LCD}	V_{CC}–2/5 V_{LCD}
V_3	V_{CC}–1/2 V_{LCD}	V_{CC}–3/5 V_{LCD}
V_4	V_{CC}–3/4 V_{LCD}	V_{CC}–4/5 V_{LCD}
V_5	V_{CC}–V_{LCD}	V_{CC}–V_{LCD}

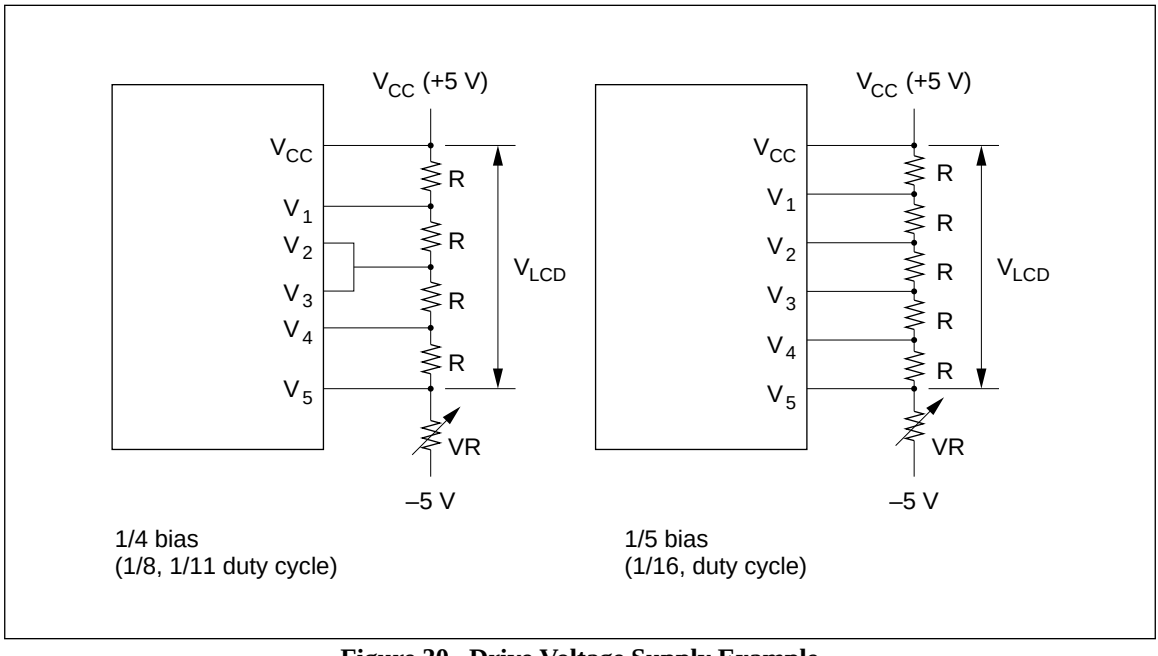


Figure 30 Drive Voltage Supply Example

Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of figure 31 apply only when the oscillation frequency is 320 kHz (one clock pulse of 3.125 µs).

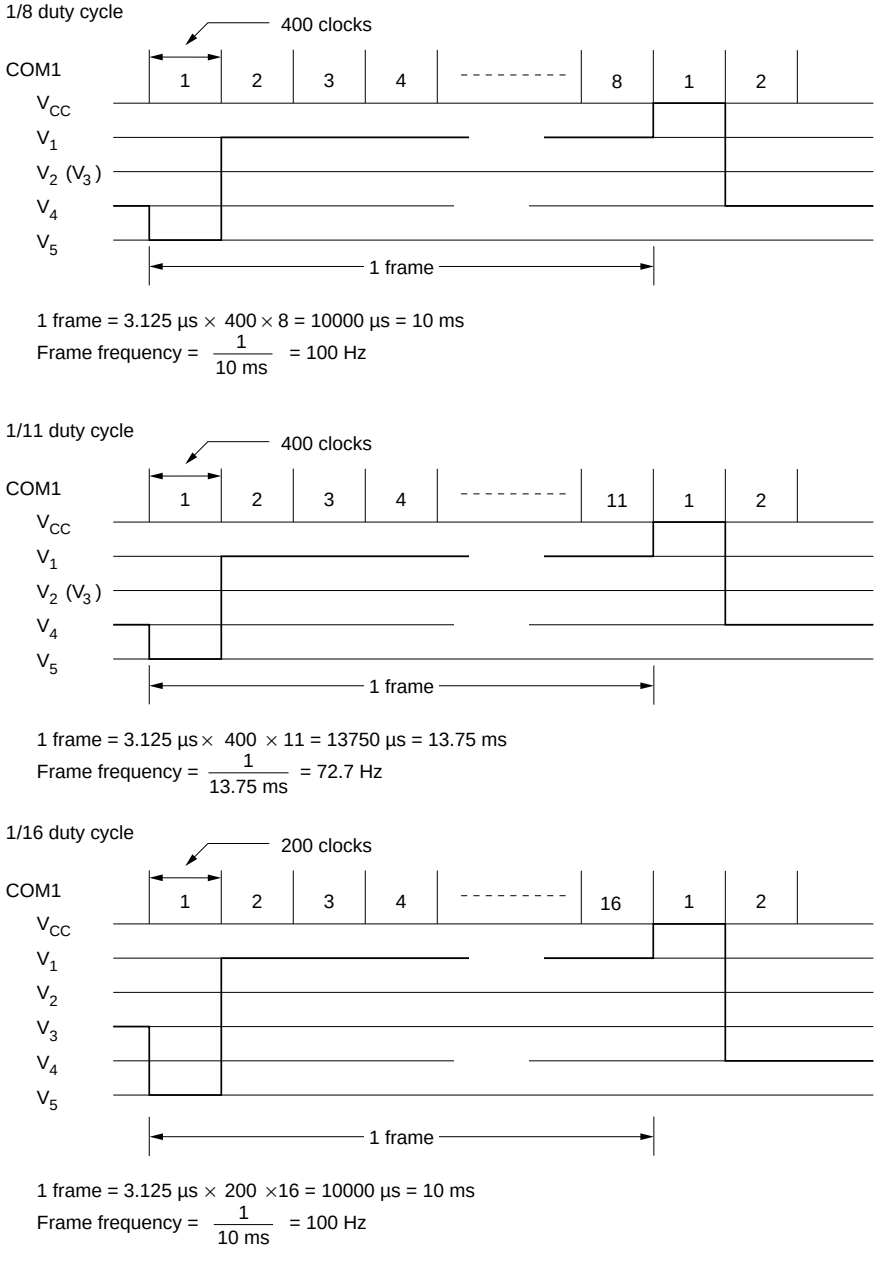


Figure 31 Frame Frequency

Connection with HD44100 Driver

By externally connecting an HD44100 liquid crystal display driver to the HD66702, the number of display digits can be increased. The HD44100 is used as a segment signal driver when connected to the HD66702. The HD44100 can be directly connected to the HD66702 since it supplies CL_1, CL_2, M, and D signals and power for the liquid crystal display drive (figure 32).

Caution: The connection of voltage supply pins V_1 through V_6 for the liquid crystal display drive is somewhat complicated. The EXT pin must be fixed low if the HD44100 is to be connected to the HD66702.

Up to eight HD44100 units can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to three units for a 2-line display (duty factor 1/16). The RAM size limits the HD66702 to a maximum of 80 character display digits. The connection method for both 1-line and 2-line displays or for 5 × 7 and 5 × 10 dot character fonts can remain the same (figure 32).

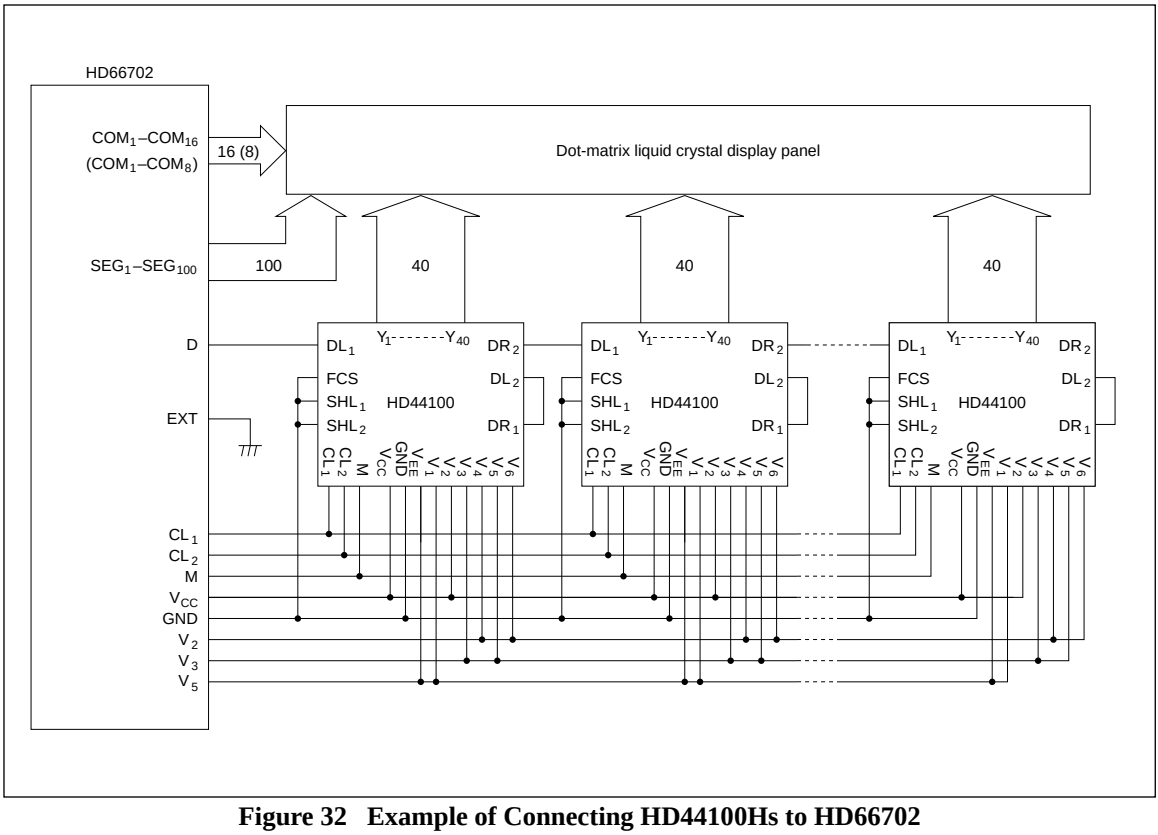


Figure 32 Example of Connecting HD44100Hs to HD66702

Instruction and Display Correspondence

- 8-bit operation, 20-digit × 1-line display with internal reset

Refer to table 12 for an example of an 8-bit × 1-line display in 8-bit operation. The HD66702 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

Since the display shift operation changes only the display position with DD RAM contents unchanged, the first display data entered into DD RAM can be output when the return home operation is performed.

- 4-bit operation, 20-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (table 13). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 13). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 20-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 20 characters in the first line, the DD RAM address must be again set after the 20th character is completed. (See table 14.) Note that the display shift operation is performed for the first and second lines. In the example of table 14, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the LCD-II/E20 must be initialized by instructions. (Because the internal reset does not function correctly when V_{CC} is 3 V, it must always be initialized by software.) See the section, Initializing by Instruction.

Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	0	0	*	*		Sets to 8-bit operation and selects 1-line display and character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HI_	Writes I.
7	⋮										⋮	
8	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
9	Entry mode set	0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CG RAM/DD RAM	1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
11	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	. . . . .										. . . . .	
13	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	. . . . .										. . . . .	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 13 4-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)							Initialized. No display.
2	Function set							Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
	0	0	0	0	1	0		
3	Function set							Sets 4-bit operation and selects 1-line display and 5 × 7 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
	0	0	0	0	1	0		
	0	0	0	0	*	*		
4	Display on/off control						_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0		
	0	0	1	1	1	0		
5	Entry mode set						_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0		
	0	0	0	1	1	0		
6	Write data to CG RAM/DD RAM						H_	Writes H. The cursor is incremented by one and shifts to the right.
	1	0	0	1	0	0		
	1	0	1	0	0	0		

Note: The control is the same as for 8-bit operation beyond step #6.

Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	1	1	1	0	*	*		Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
3	Display on/off control	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	. . . . .										. . . . .	
7	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
8	Set DD RAM address	0	0	1	1	0	0	0	0	0	0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.

Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
9	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	0	1	HITACHI M_	Writes M.
10	. . . . .										. . . . .	
11	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	1	1	HITACHI MICROCO_	Writes O.
12	Entry mode set 0	0	0	0	0	0	0	1	1	1	HITACHI MICROCO_	Sets mode to shift display at the time of write.
13	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	0	1	ITACHI ICROCOM_	Writes M. Display is shifted to the right. The first and second lines both shift at the same time.
14	. . . . .										. . . . .	
15	Return home 0	0	0	0	0	0	0	0	1	0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to figures 33 and 34 for the procedures on 8-bit and 4-bit initializations, respectively.

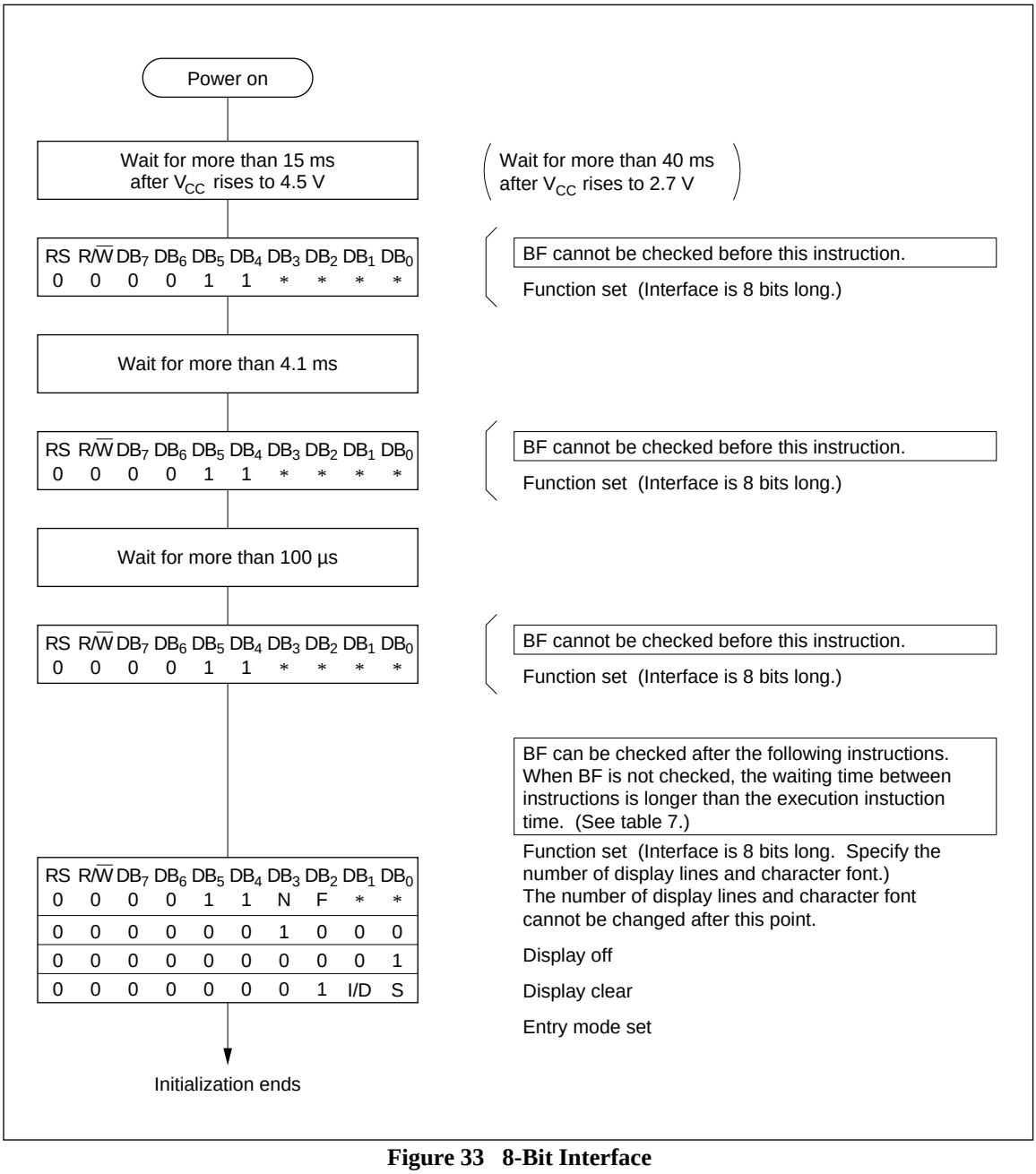


Figure 33 8-Bit Interface

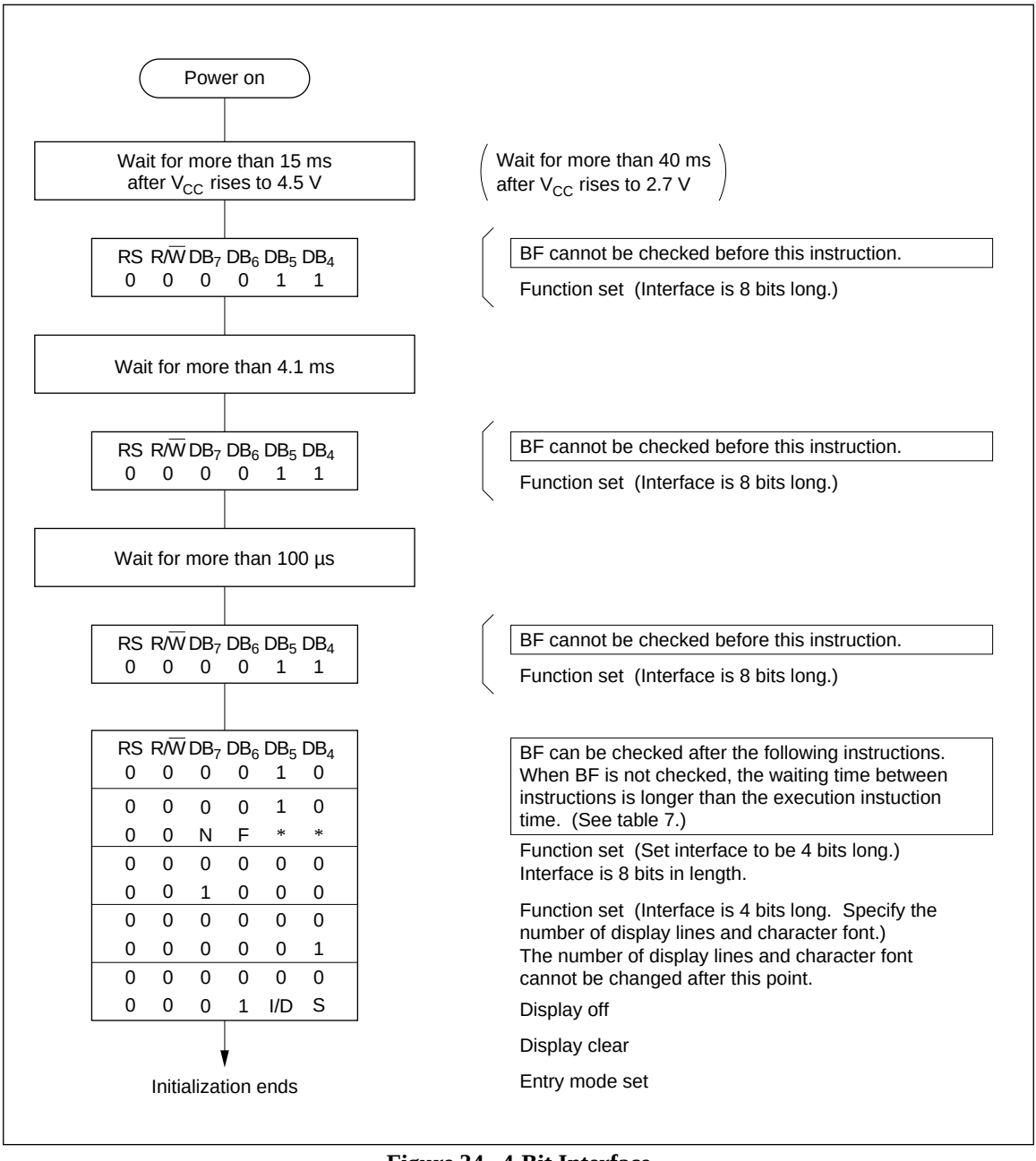


Figure 34 4-Bit Interface

[Low voltage version]

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +8.5	2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6, 17
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.55	V		6, 17
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RS, R/$\overline{W}$, D_0–D_7)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	8.3	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	8.3	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 to 5.5 V, T_a = –20 to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	240	320	390	kHz	R_f = 56 kΩ V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	350		
Data hold time	t_{DHR}	10	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 37
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 38
Power supply off time	t_{OFF}	1	—	—		

[Standard Voltage Version]

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +8.5	2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability. Refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	2.2	—	V_{CC}	V		6, 17
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.6	V		6, 17
Input high voltage (2) (OSC_1)	V_{IH2}	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	1.0	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	2.4	—	—	V	$–I_{OH}$ = 0.205 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.6 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	0.9 V_{CC}	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RS, R/$\overline{W}$, D_0–D_7)	$–I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}	—	0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	8.3	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	8.3	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C[*3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	µs		11
	External clock fall time	t_{fcp}	—	—	0.2	µs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	220	320	420	kHz	R_f = 68 kΩ V_{CC} = 5 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	320		
Data hold time	t_{DHR}	20	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 37
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

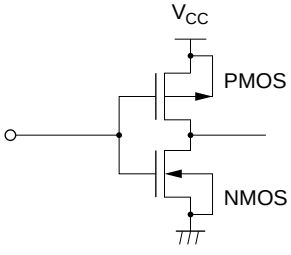
Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 38
Power supply off time	t_{OFF}	1	—	—		

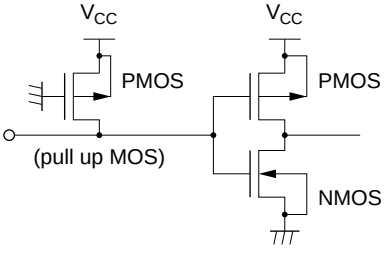
Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V.
2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

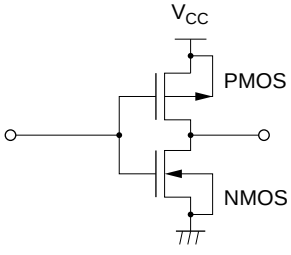
Input pin
Pin: E (MOS without pull-up)



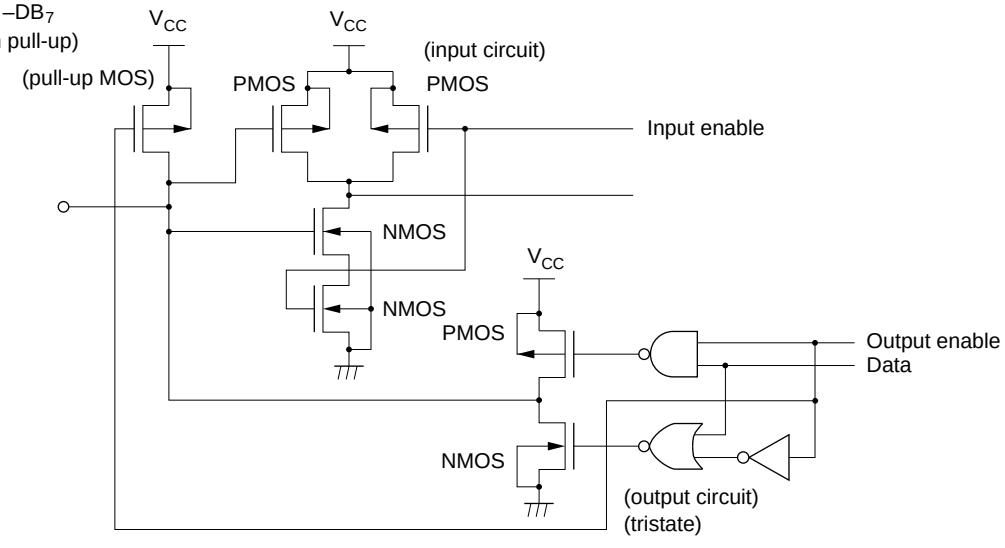
Pins: RS, R/$\overline{W}$ (MOS with pull-up)



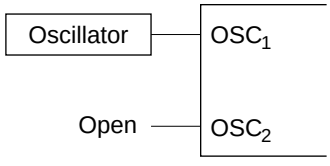
Output pin
Pins: CL_1, CL_2, M, D

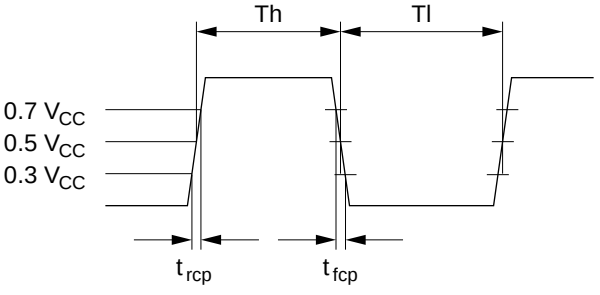


I/O Pin
Pins: DB_0–DB_7
(MOS with pull-up)



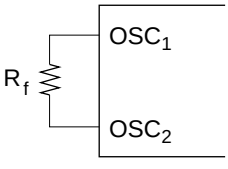
6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull–up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



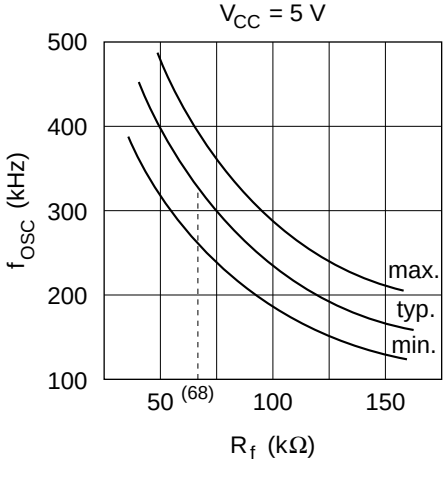


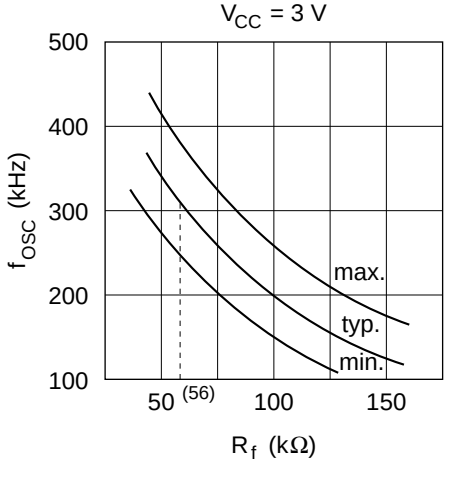
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



R_f : 56 kΩ ± 2% (when V_{CC} = 3 V)
R_f : 68 kΩ ± 2% (when V_{CC} = 5 V)
Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.

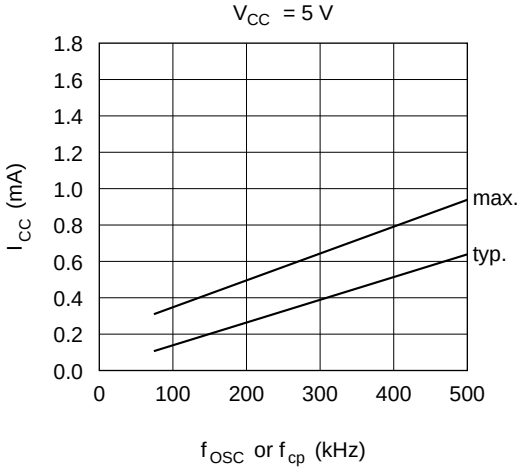


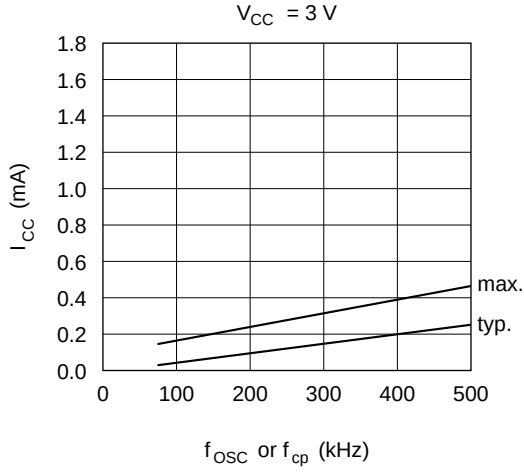


13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{100}).

14. The following graphs show the relationship between operation frequency and current consumption.

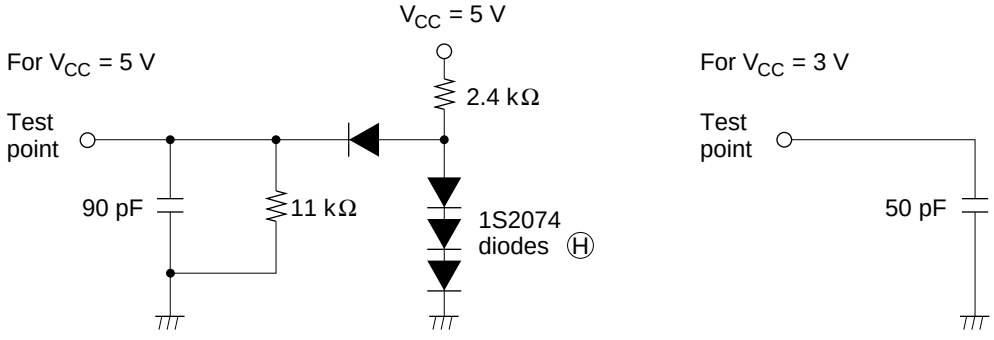




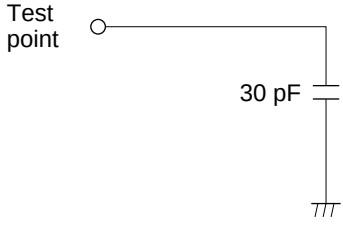
15. Applies to the OSC_1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.
17. The TEST pin should be fixed to GND and the EXT pin should be fixed to V_{CC} or GND.

Load Circuits

Data Bus DB_0 to DB_7



External Driver Control Signal: CL1, CL2, D, M



Timing Characteristics

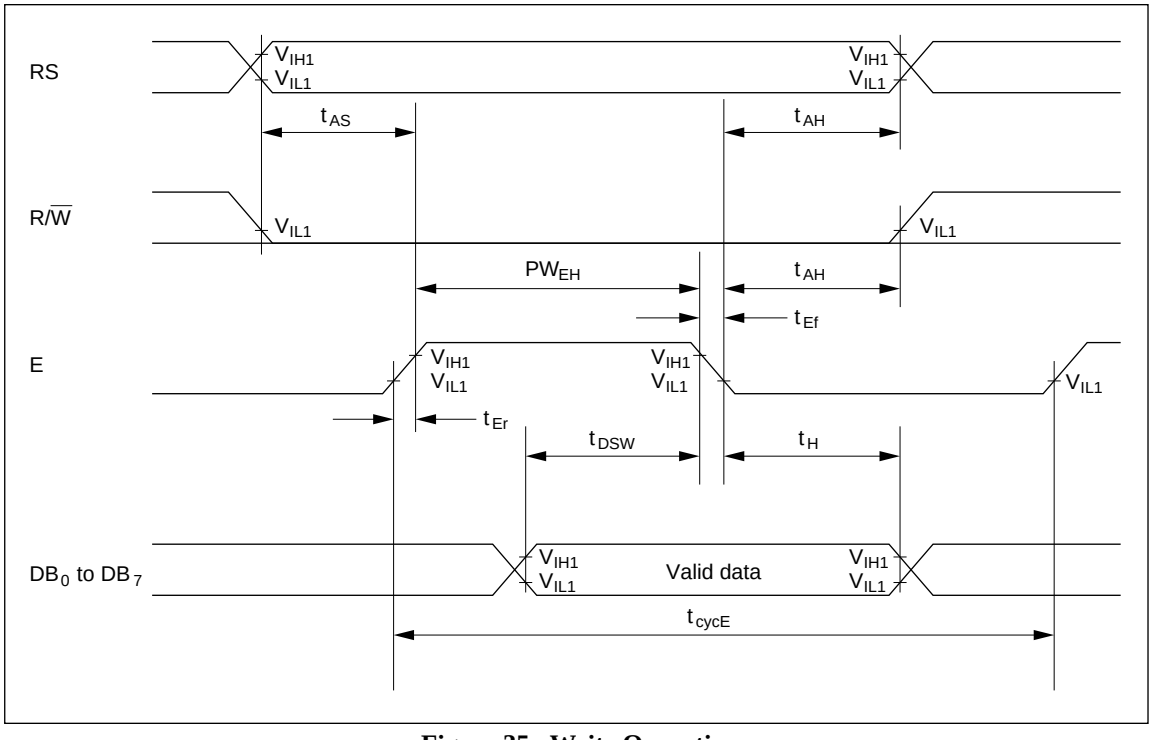


Figure 35 Write Operation

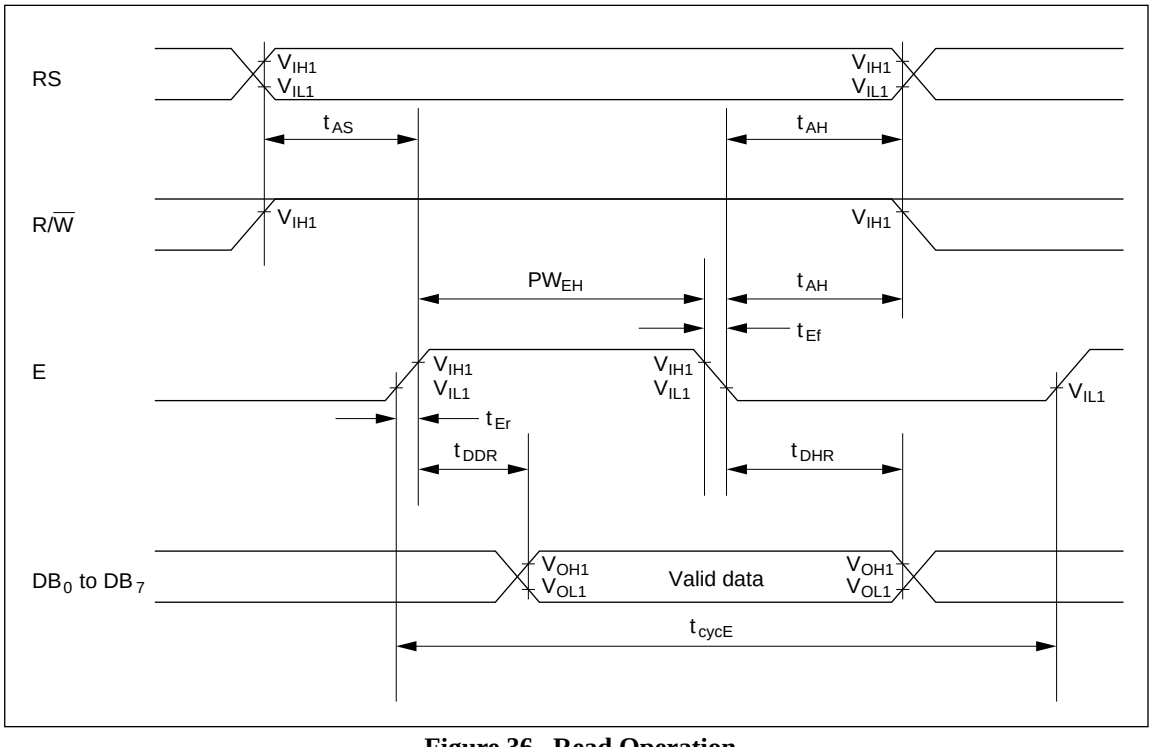


Figure 36 Read Operation

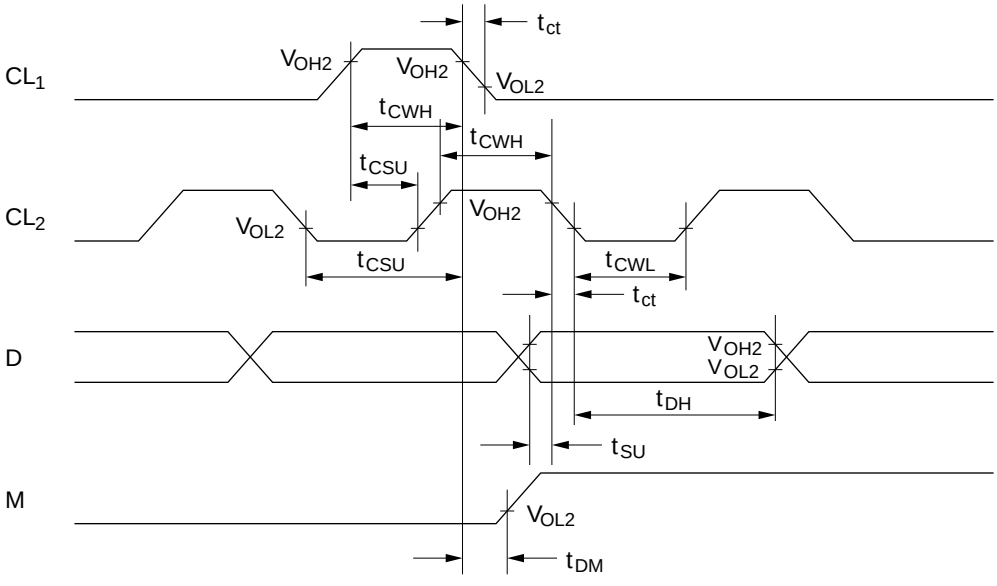
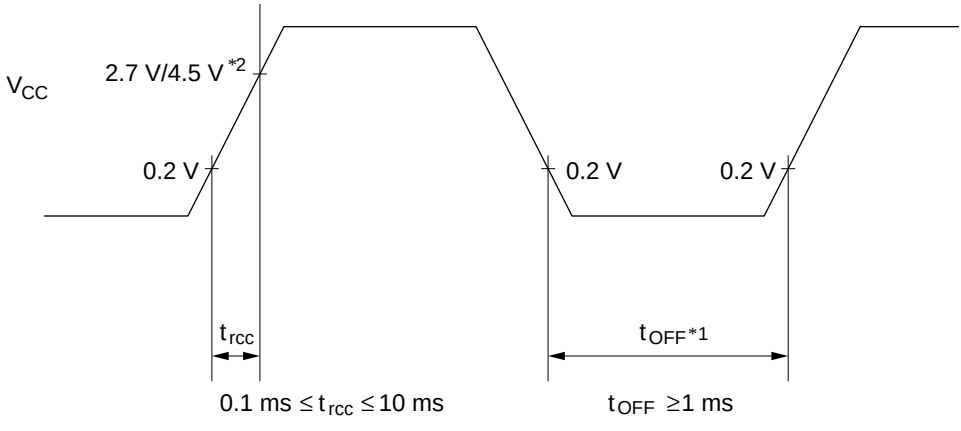


Figure 37 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. When the above condition cannot be satisfied, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 38 Internal Power Supply Reset

HD66710 (LCD-II/F8)

(Dot Matrix Liquid
Crystal Display Controller/Driver)

HITACHI

Description

The LCD-II/F8 (HD66710) dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, numbers, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimum system can be interfaced with this controller/driver.

A single LCD-II/F8 is capable of displaying a single16-character line, two 16-character lines, or up to four 8-character lines.

The LCD-II/F8 software is upwardly compatible with the LCDII (HD44780) which allows the user to easily replace an LCD-II with an HD66710. In addition, the HD66710 is equipped with functions such as segment displays for icon marks, a 4-line display mode, and a horizontal smooth scroll, and thus supports various display forms. This achieves various display forms. The HD66710 character generator ROM is extended to generate 240 5 × 8 dot characters.

The low voltage version (2.7 V) of the HD66710, combined with a low power mode, is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 dot matrix possible
- Low power operation support:
  - 2.7 V to 5.5 V (low voltage)
- Booster for liquid crystal voltage
  - Two/three times (13 V max.)
- Wide range of liquid crystal display driver voltage
  - 3.0 V to 13 V
- Extension driver interface
- High-speed MPU bus interface
  (2 MHz at 5-V operation)
- 4-bit or 8-bit MPU interface capability
- 80 × 8-bit display RAM (80 characters max.)
- 9,600-bit character generator ROM
  - 240 characters (5 × 8 dot)
- 64 × 8-bit character generator RAM
  - 8 characters (5 × 8 dot)
- 8 × 8-bit segment RAM
  - 40-segment icon mark
- 33-common × 40-segment liquid crystal display driver
- Programmable duty cycle
  (See list 1)
- Wide range of instruction functions:
  - Functions compatible with LCD-II: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
  - Additional functions: Icon mark control, 4-line display, horizontal smooth scroll, 6-dot character width control, white-black inverting blinking cursor
- Software upwardly compatible with HD44780
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with an external resistor
- Low power consumption
- QFP1420-100 pin, TQFP1414-100 pin bare-chip

Hitachi semiconductor

List 1 Programmable Duty Cycles

Number of Lines	Duty Ratio	Displayed Character	Maximum Number of Displayed Characters	
			Single-chip Operation	With Extention Driver
1	1/17	5 × 8-dot	One 16-character line + 40 segments	One 50-character line + 40 segments
2	1/33	5 × 8-dot	Two 16-character lines + 40 segments	Two 30-character lines + 40 segments
4	1/33	5 × 8-dot	Four 8-character lines + 40 segments	Four 20-character lines + 40 segments

Ordering Information

Type No.	Package	CGROM
HD66710A00FS	QFP1420-100 (FP-100A)	Japanese standard
HD66710A00TF	TQFP1414-100 (TFP-100B)	
HCD66710A00	Chip	
HD66710A01TF*	TQFP1414-100 (TFP-100B)	Communication
HD66710A02TF*	TQFP1414-100 (TFP-100B)	European font
HD66710BxxFS	QFP1420-100 (FP-100A)	Custom font
HD66710BxxTF	TQFP1414-100 (TFP-100B)	
HCD66710Bxx	Chip	

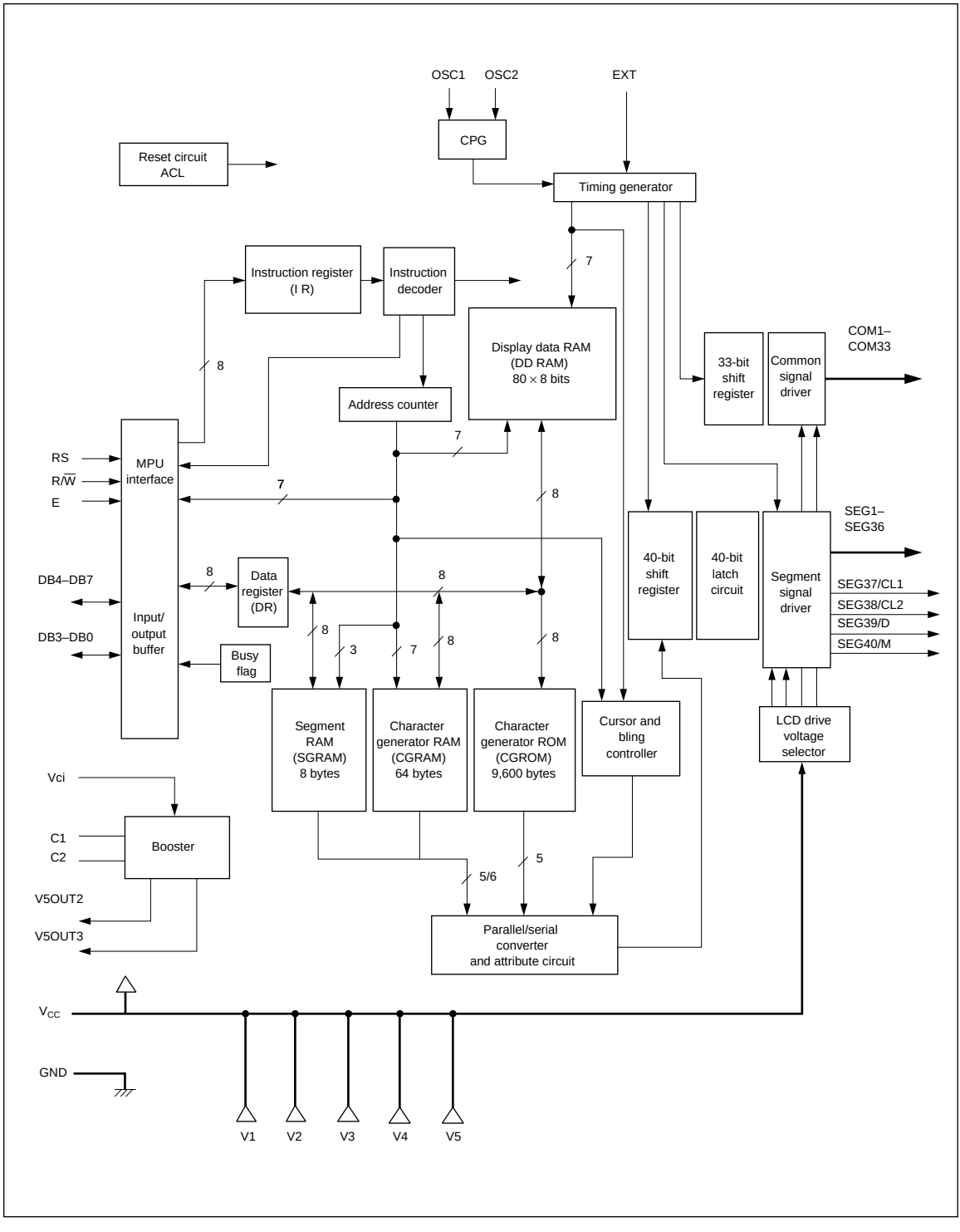
Note: * Under development
Bxx = ROM code No.

LCD-II Family Comparison

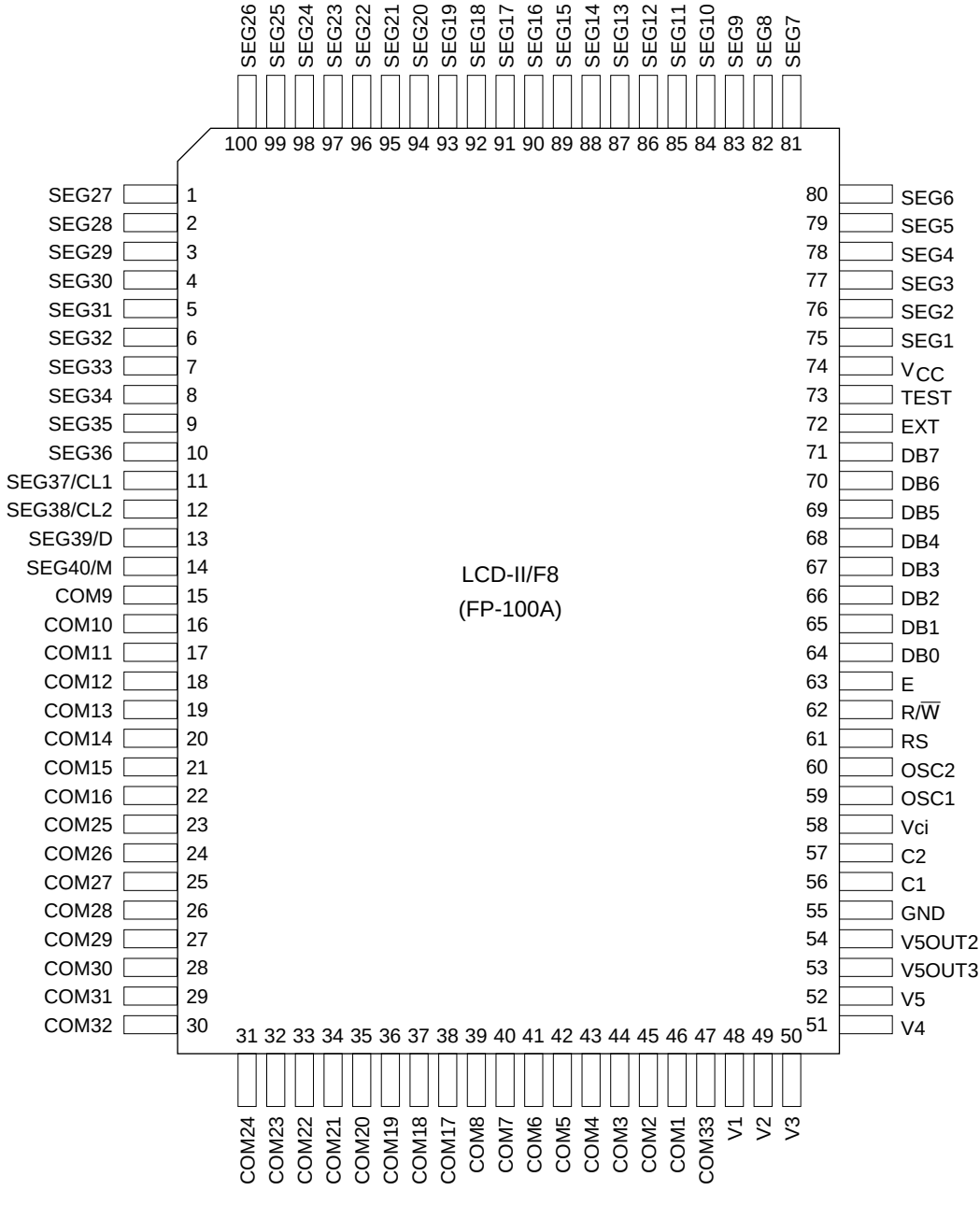
Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702R)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Power supply voltage	2.7 V to 5.5 V	5 V ±10% (standard) 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltage	3.0 V to 11 V	3.0 V to 8.3 V	3.0 V to 13.0 V	3.0 V to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines
Segment display	None	None	40 segments	60 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33	1/17 and 1/33
CGROM	9,920 bits (208 5 × 8 dot characters and 32 5 × 10 dot characters)	7,200 bits (160 5 × 7 dot characters and 32 5 × 10 dot characters)	9,600 bits (240 5 × 8 dot characters)	9,600 bits (240 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes	16 bytes
Segment signals	40	100	40	60
Common signals	16	16	33	34
Liquid crystal drive waveform	A	B	B	B
Bleeder resistor for LCD power supply	External (adjustable)	External (adjustable)	External (adjustable)	External (adjustable)
Clock source	Extenal resistor or external clock	External resistor or external clock	External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycle; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (70 to 130 Hz for 1/8 and 1/16 duty cycle; 51 to 95 Hz for 1/11 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)
R_f resistance	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	68 kΩ: 5-V operation; 56 kΩ: (3-V operation)	91 kΩ: 5-V operation; 75 kΩ: 3-V operation)	91 kΩ: 5-V operation; 75 kΩ: 3-V operation
Liquid crystal voltage booster circuit	None	None	2–3 times step-up circuit	2–3 times step-up circuit

Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702R)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Extension driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal
Reset function	Power on automatic reset	Power on automatic reset	Power on automatic reset	Power on automatic reset or reset input
Instructions	LCD-II (HD44780)	Fully compatible with the LCD-II	Upper compatible with the LCD-II	Upper compatible with the LCD-II
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
Low power mode	None	None	Available	Available
Horizontal scroll	Character unit	Character unit	Dot unit	Dot unit
Bus interface	4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial; 4 bits/8 bits
CPU bus timing	2 MHz: 5-V operation; 1 MHz: 3-V operation	1 MHz	2 MHz: 5-V operation; 1 MHz: 3-V operation	2 MHz: 5-V operation; 1 MHz: 3-V operation
Package	QFP-1420-80 80-pin bare chip	LQFP-2020-144 144-pin bare chip	QFP-1420-100 100-pin bare chip TQFP1414-100	QFP-1420-128 TCP-128 128-pin bare chip

HD66710 Block Diagram

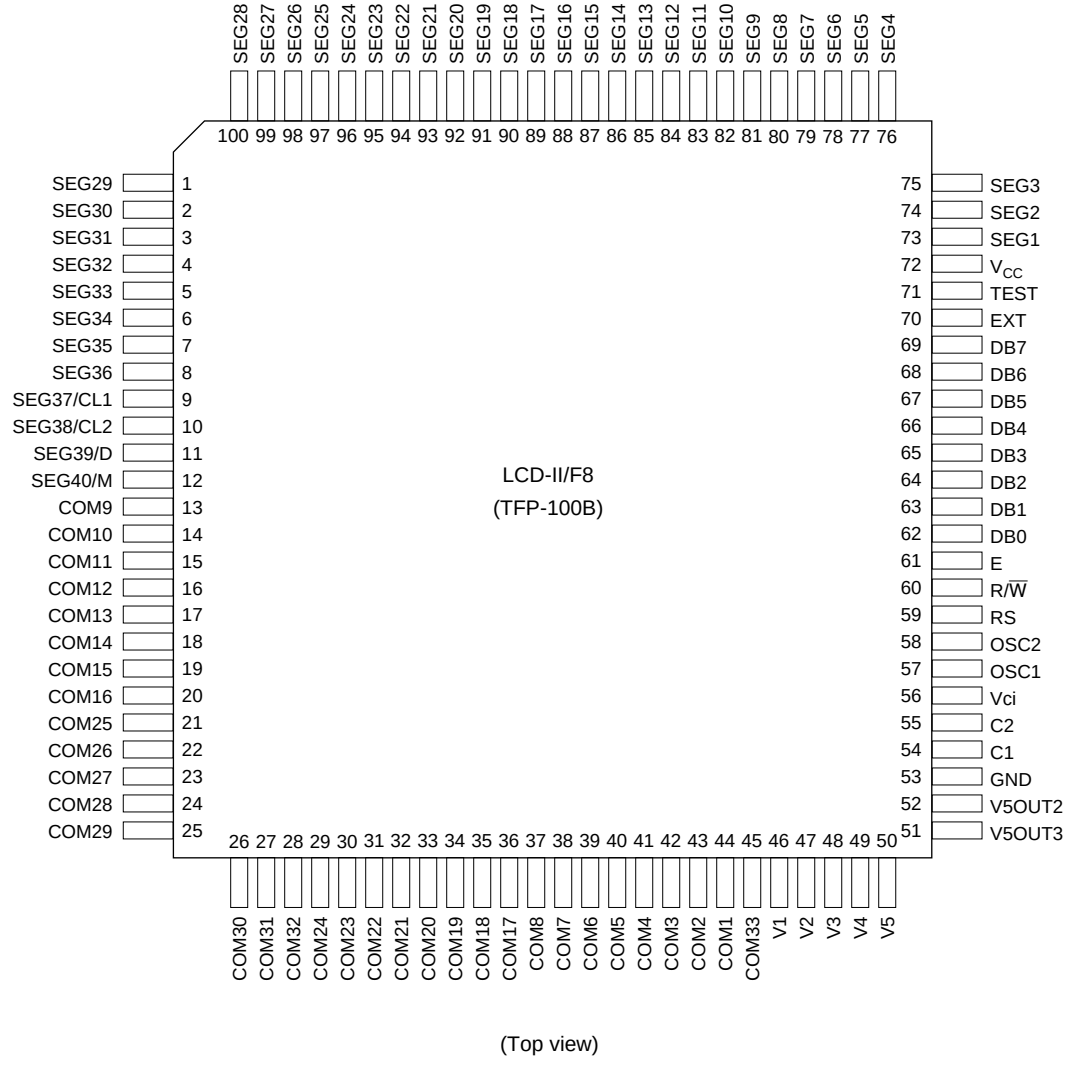


HD66710 Pin Arrangement



(Top view)

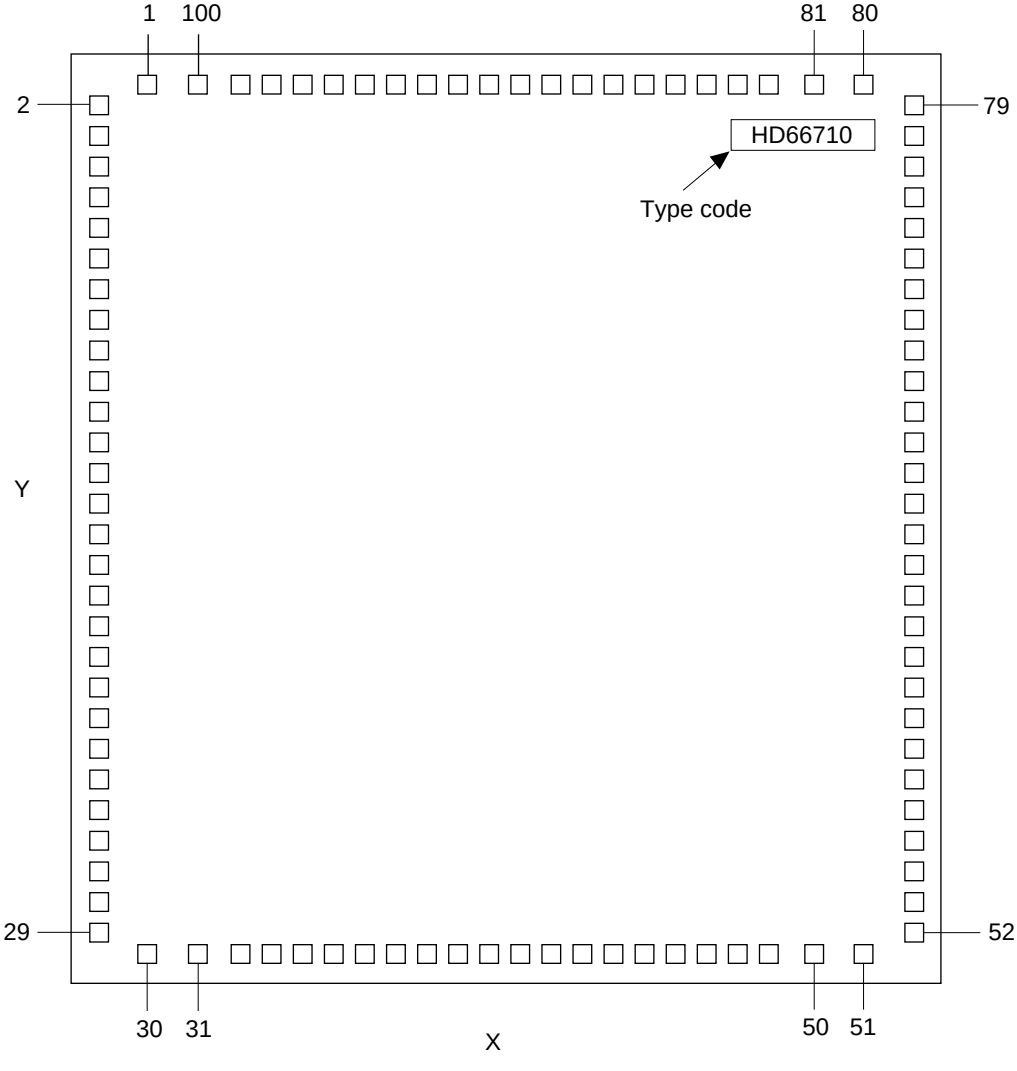
HD66710 Pin Arrangement (TQFP1414-100 Pin)



(Top view)

HD66710 Pad Arrangement

Chip size (X × Y): 5.63 mm × 6.06 mm
Coordinate : Pad center
Origin : Chip center
Pad size (X × Y) : 100 µm × 100 µm



HD66710 Pad Location Coordinates

Pin No.	Pad Name	X	Y
1	SEG27	–2495	2910
2	SEG28	–2695	2730
3	SEG29	–2695	2499
4	SEG30	–2695	2300
5	SEG31	–2695	2100
6	SEG32	–2695	1901
7	SEG33	–2695	1698
8	SEG34	–2695	1498
9	SEG35	–2695	1295
10	SEG36	–2695	1099
11	SEG37	–2695	900
12	SEG38	–2695	700
13	SEG39	–2695	501
14	SEG40	–2695	301
15	COM9	–2695	98
16	COM10	–2695	–113
17	COM11	–2695	–302
18	COM12	–2695	–501
19	COM13	–2695	–701
20	COM14	–2695	–900
21	COM15	–2695	–1100
22	COM16	–2695	–1303
23	COM25	–2695	–1502
24	COM26	–2695	–1702
25	COM27	–2695	–1901
26	COM28	–2695	–2101
27	COM29	–2695	–2300
28	COM30	–2695	–2500
29	COM31	–2695	–2731
30	COM32	–2495	–2910
31	COM24	–2051	–2910
32	COM23	–1701	–2910
33	COM22	–1498	–2910
34	COM21	–1302	–2910
35	COM20	–1102	–2910
36	COM19	–899	–2910
37	COM18	–700	–2910
38	COM17	–500	–2910
39	COM8	–301	–2910
40	COM7	–101	–2910
41	COM6	99	–2910
42	COM5	302	–2910
43	COM4	502	–2910
44	COM3	698	–2910
45	COM2	887	–2910
46	COM1	1077	–2910
47	COM33	1266	–2910
48	V1	1488	–2910
49	V2	1710	–2910
50	V3	2063	–2910
51	V4	2458	–2910
52	V5	2660	–2731
53	V5OUT3	2660	–2500
54	V5OUT2	2660	–2300
55	GND	2640	–2090
56	C1	2650	–1887
57	C2	2675	–1702
58	Vci	2675	–1502
59	OSC1	2675	–1303
60	OSC2	2675	–1103
61	RS	2675	–900
62	R/$\overline{W}$	2675	–701
63	E	2675	–501
64	DB0	2675	–302
65	DB1	2675	–99
66	DB2	2675	98
67	DB3	2675	301
68	DB4	2675	501
69	DB5	2675	700
70	DB6	2675	900
71	DB7	2675	1099
72	EXT	2675	1299
73	TEST	2675	1502
74	V_{CC}	2695	1698
75	SEG1	2695	1901
76	SEG2	2695	2104
77	SEG3	2695	2300
78	SEG4	2695	2503
79	SEG5	2695	2730
80	SEG6	2495	2910
81	SEG7	2049	2910
82	SEG8	1699	2910
83	SEG9	1499	2910
84	SEG10	1300	2910
85	SEG11	1100	2910
86	SEG12	901	2910
87	SEG13	701	2910
88	SEG14	502	2910
89	SEG15	299	2910
90	SEG16	99	2910
91	SEG17	–101	2910
92	SEG18	–301	2910
93	SEG19	–500	2910
94	SEG20	–700	2910
95	SEG21	–899	2910
96	SEG22	–1099	2910
97	SEG23	–1302	2910
98	SEG24	–1501	2910
99	SEG25	–1701	2910
100	SEG26	–2051	2910

Pin Functions

Table 1 Pin Functional Description

Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	I	MPU	Selects read or write 0: Write 1: Read
E	I	MPU	Starts data read/write
DB4 to DB7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66710. DB7 can be used as a busy flag.
DB0 to DB3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66710. These pins are not used during 4-bit operation.
COM1 to COM33	O	LCD	Common signals; those are not used become non-selected waveforms. At 1/17 duty rate, COM1 to COM16 are used for character display, COM17 for icon display, and COM18 to COM33 become non-selected waveforms. At 1/33 duty rate, COM1 to COM32 are used for character display, and COM33 for icon display.
SEG1 to SEG35	O	LCD	Segment signals
SEG36	O	LCD	Segment signal. When EXT = high, the same data as that of the first dot of the extension driver is output.
SEG37/CL1	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver latch pulse.
SEG38/CL2	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver shift clock.
SEG39/D	O	LCD/ Extension driver	Segment signal at EXT = low. At EXT = high, the extension driver data. Data on and after the 36th dot is output.
SEG40/M	O	LCD/ Extension driver	Segment signal when EXT = low. When EXT = high, outputs the extension driver AC signal.
EXT	I	—	Extension driver enable signal. When EXT = high, SEG37 to SEG40 become extension driver interface signals. At this time, make sure that V5 level is lower than GND level (0 V). V5 (low) ≤ GND (high).
V1 to V5	—	Power supply	Power supply for LCD drive V_{CC} – V5 = 13 V (max)

Table 1 Pin Functional Description (cont)

Signal	I/O	Device Interfaced with	Function
V_{CC}, GND	—	Power supply	V_{CC}: +2.7 V to 5.5 V, GND: 0 V
OSC1, OSC2	—	Oscillation resistor clock	When CR oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.
Vci	I	—	Input voltage to the booster, from which the liquid crystal display drive voltage is generated. Vci is reference voltage and power supply for the booster. Vci = 2.0 V to 5.0 V ≤ Vci
V5OUT2	O	V5 pin/ Booster capacitance	Voltage input to the Vci pin is boosted twice and output When the voltage is boosted three times, the same capacity as that of C1–C2 should be connected.
V5OUT3	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	—	Booster capacitance	External capacitance should be connected when using the booster.
TEST	I	—	Test pin. Should be wired to ground.

Function Description

Registers

The HD66710 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEG RAM). The MPU can only write to IR, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM, CG RAM, or SEG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66710 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (table 2), the busy flag is output from DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)
  - — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66710, 16 characters are displayed. See figure 3.

    When the display shift operation is performed, the DD RAM address shifts. See figure 3.
  - — Case 2: Figure 4 shows the case where the EXT pin is fixed high, and the HD66710 and the 40-output extension driver are used to extend the number of display characters. In this case, the start address from COM9 to COM16 of the LCD-II/F8 is 0AH. To display 24 characters, addresses starting at SEG11 should be used.

    When a display shift operation is performed, the DD RAM address shifts. See figure 4.

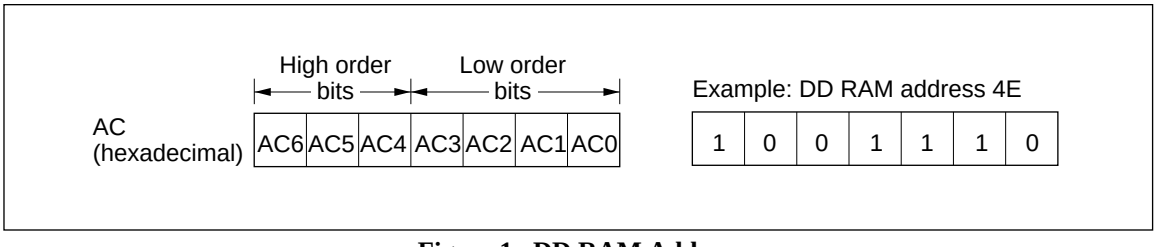


Figure 1 DD RAM Address

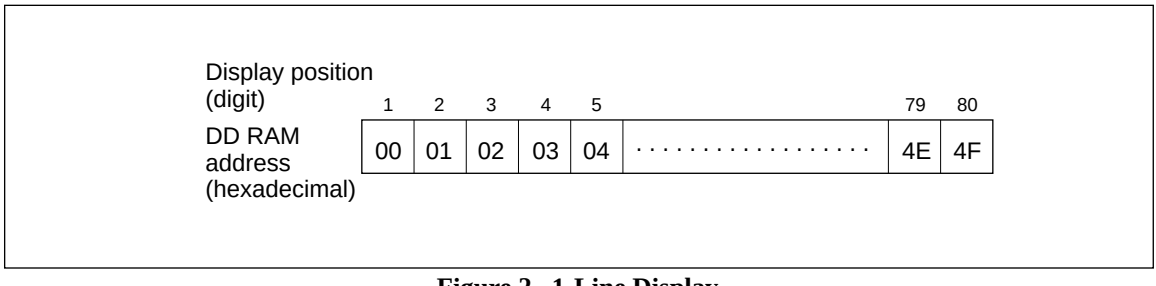


Figure 2 1-Line Display

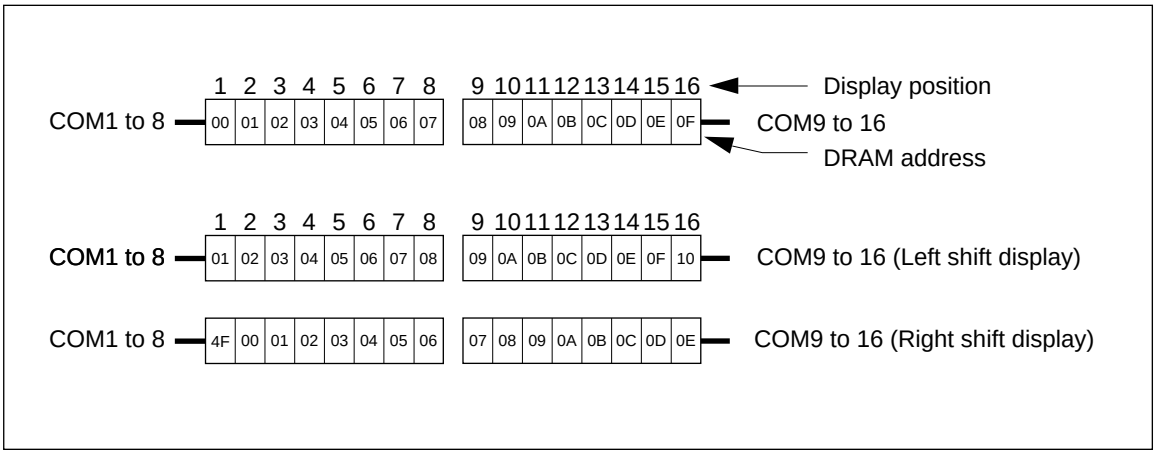


Figure 3 1-line by 16-Character Display Example

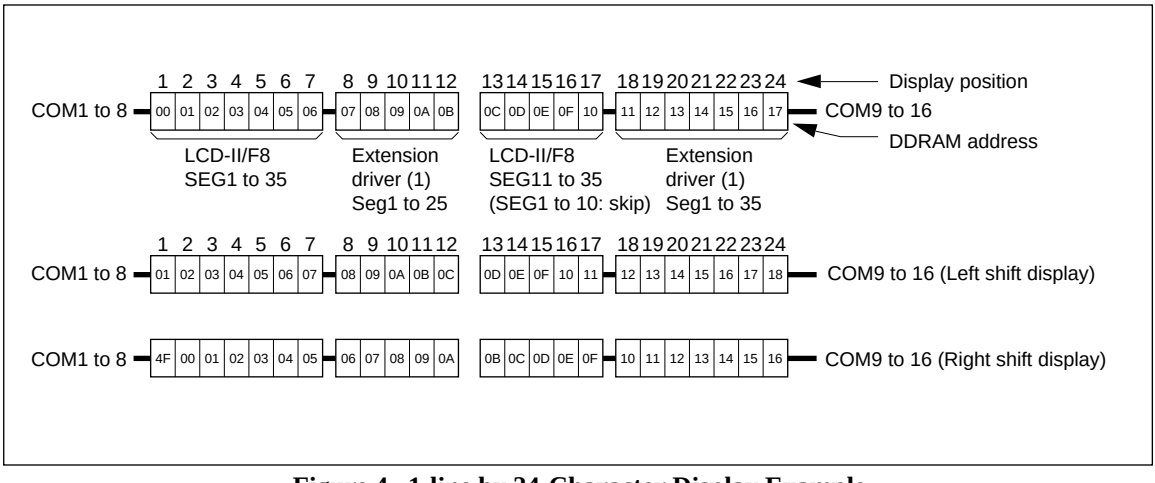


Figure 4 1-line by 24-Character Display Example

- 2-line display (N = 1, and NW = 0)

  — Case 1: The first line is displayed from COM1 to COM16, and the second line is displayed from COM17 to COM32. Care is required because the end address of the first line and the start address of the second line are not consecutive. For example, the case is shown in figure 6 where 16 × 2-line display is performed using the HD66710. When a display shift operation is performed, the DD RAM address shifts. See figure 5.

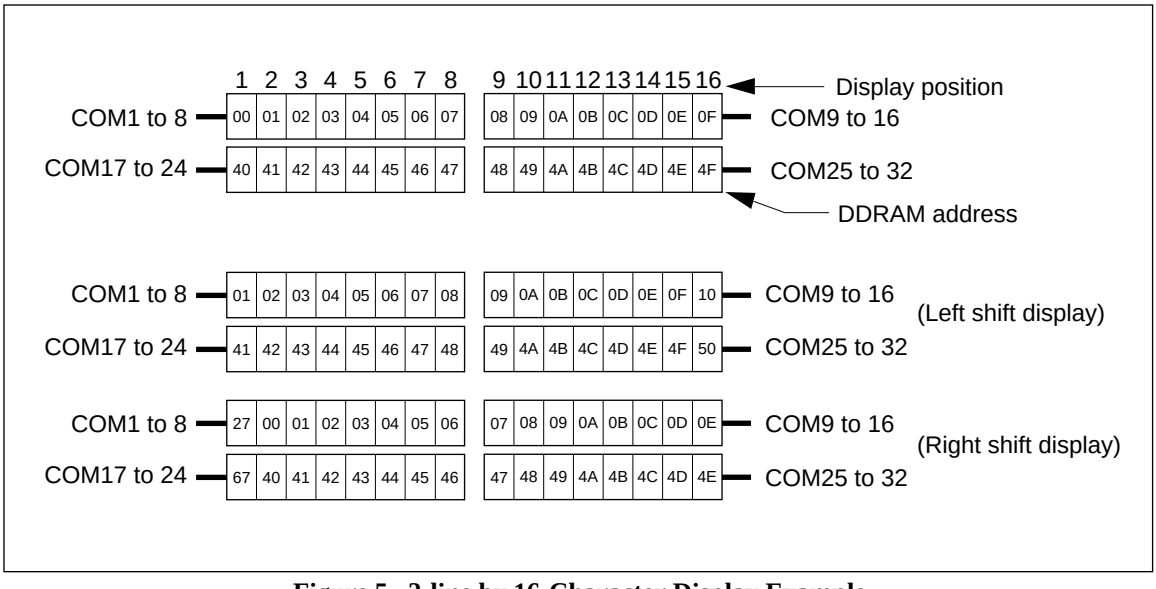


Figure 5 2-line by 16-Character Display Example

— Case 2: Figure 6 shows the case where the EXT pin is fixed to high, the HD66710 and the 40-output extension driver are used to extend the number of display characters.

In this case, the start address from COM9 to COM16 of the HD66710 is 0AH, and that from COM25 to COM32 of the HD66710 is 4AH. To display 24 characters, the addresses starting at SEG11 should be used.

When a display shift operation is performed, the DD RAM address shifts. See figure 6.

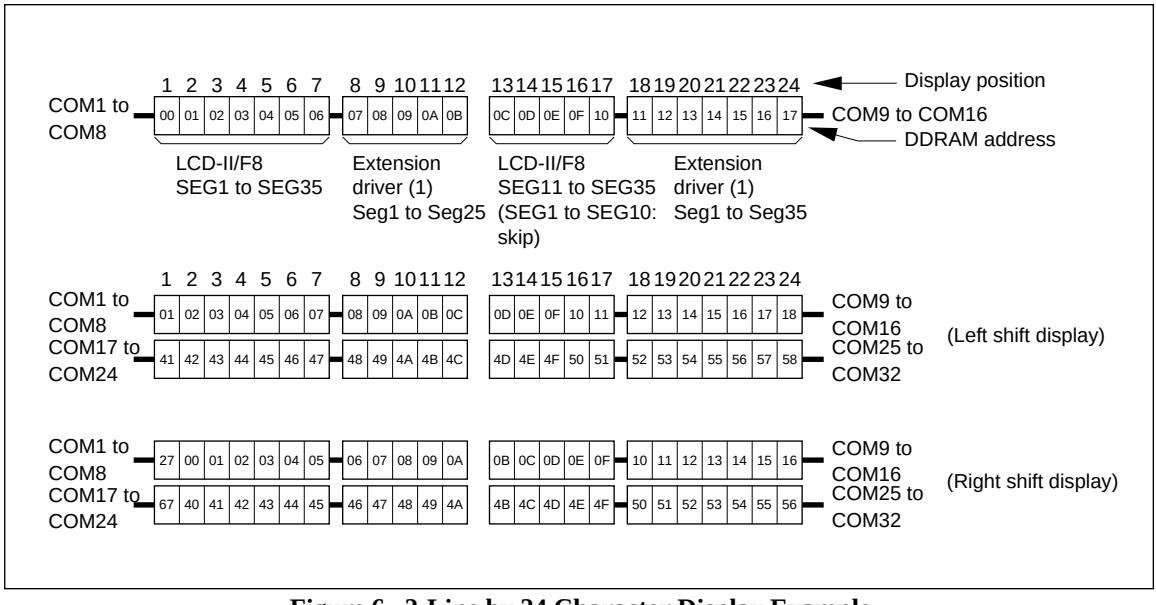


Figure 6 2-Line by 24 Character Display Example

- 4-line display (NW = 1)

  — Case 1: The first line is displayed from COM1 to COM8, the second line is displayed from COM9 to COM16, the third line is displayed from COM17 to COM24, and the fourth line is displayed from COM25 to COM32. Care is required because the DD RAM addresses of each line are not consecutive. For example, the case is shown in figure 7 where 8 × 4-line display is performed using the HD66710.

When a display shift operation is performed, the DD RAM address shifts. See figure 7.

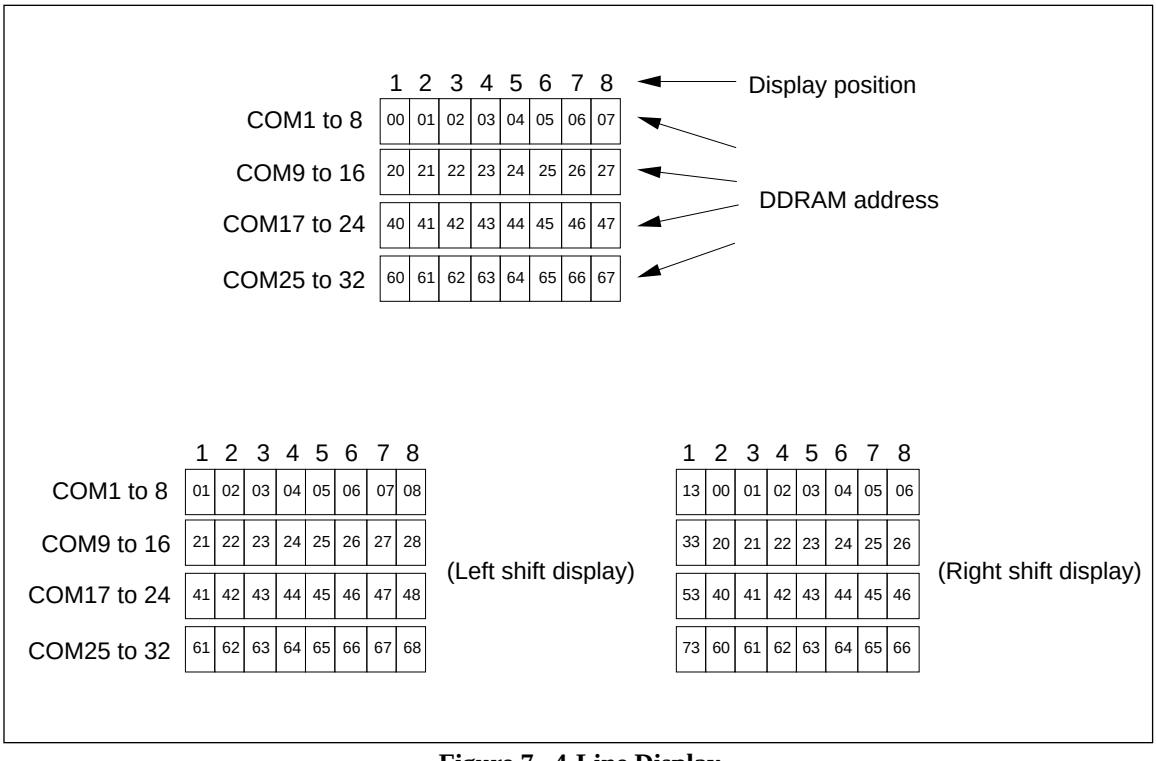


Figure 7 4-Line Display

— Case 2: The case is shown in figure where the EXT pin is fixed high, and the HD66710 and the 40-output extension driver are used to extend the number of display characters.

When a display shift operation is performed, the DD RAM address shifts. See figure 8.

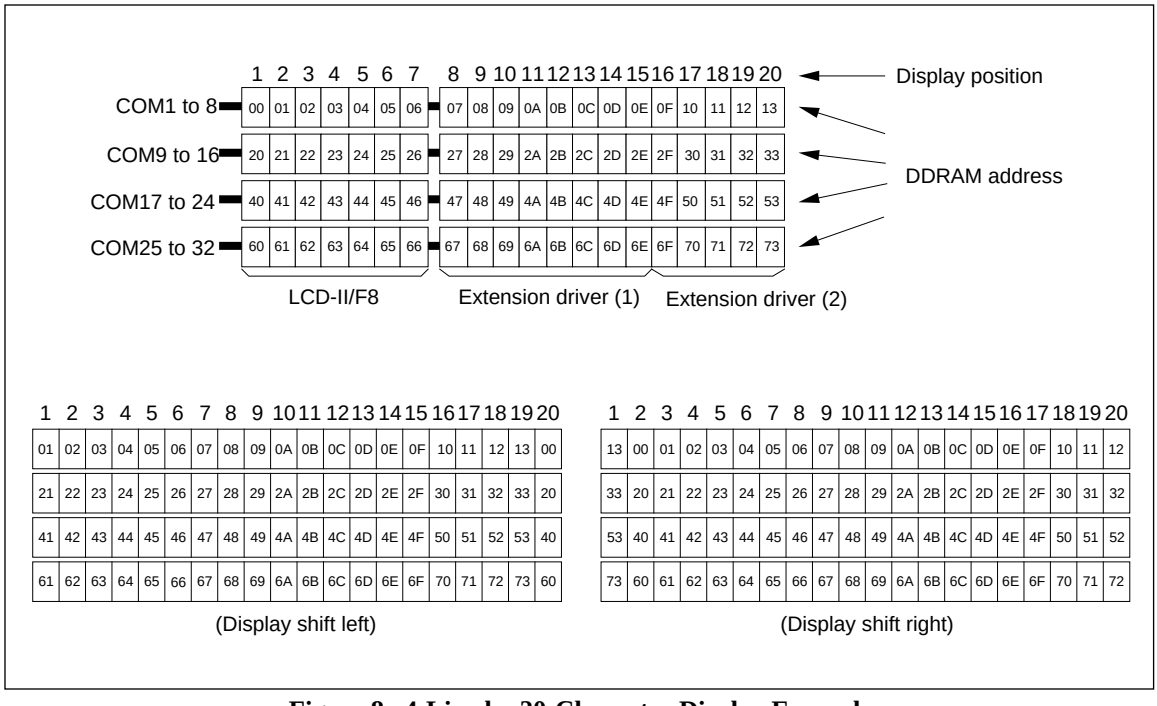


Figure 8 4-Line by 20-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM.

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of table 3 to show the character patterns stored in CG RAM.

See table 5 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEG RAM)

The segment RAM (SEG RAM) is used to enable control of segments such as an icon and a mark by the user program.

For a 1-line display, SEG RAM is read from the COM17 output, and as for 2- or 4-line displays, it is from the COM33 output, to performs 40-segment display.

As shown in table 6, bits in SEG RAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DD RAM and CG RAM.

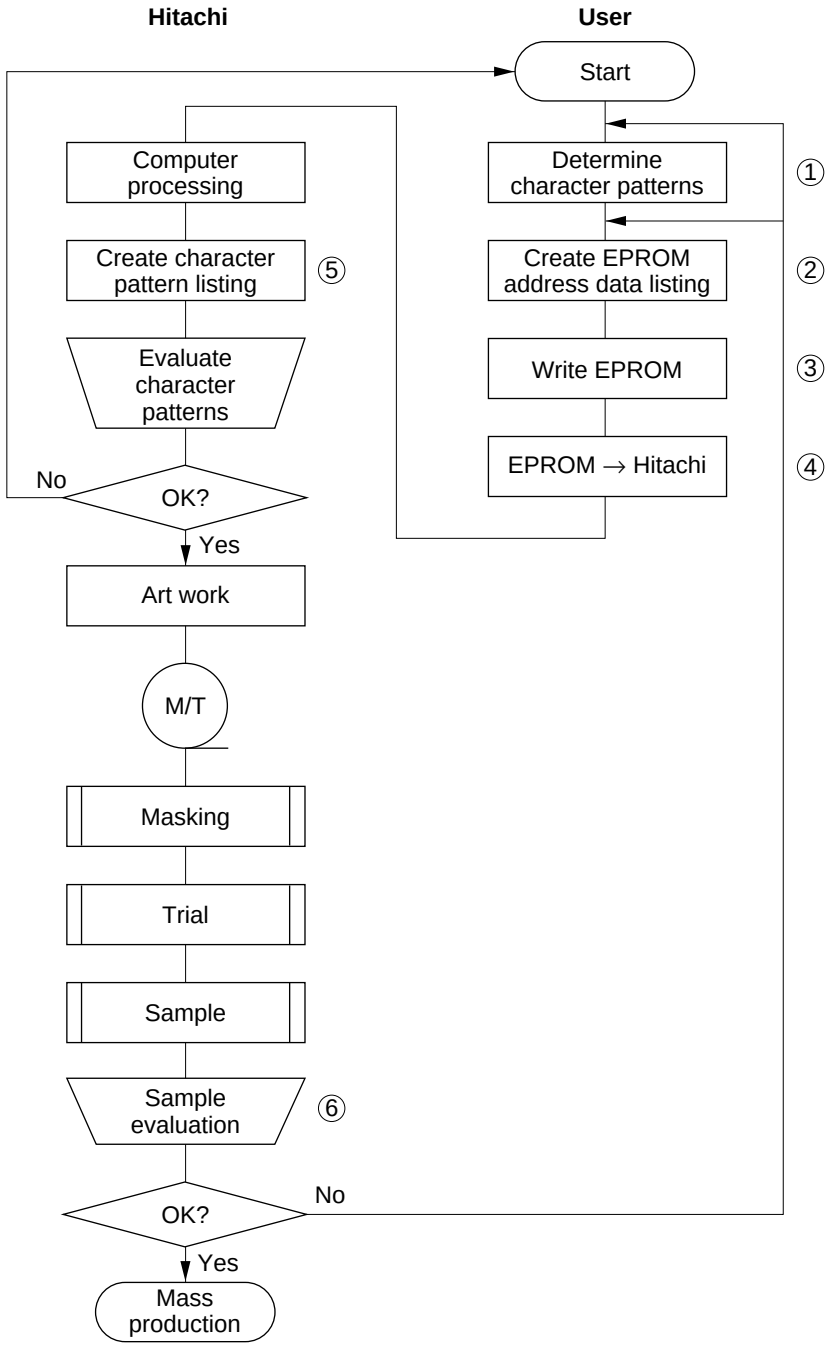
SEG RAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in figure 9:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 9 Character Pattern Development Procedure

Table 3 Correspondence between Character Codes and Character Patterns (Hitachi Standard HD66710)

Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	(2)															
xxxx0010	(3)															
xxxx0011	(4)															
xxxx0100	(5)															
xxxx0101	(6)															
xxxx0110	(7)															
xxxx0111	(8)															
xxxx1000	(1)															
xxxx1001	(2)															
xxxx1010	(3)															
xxxx1011	(4)															
xxxx1100	(5)															
xxxx1101	(6)															
xxxx1110	(7)															
xxxx1111	(8)															

Note: The user can specify any pattern in the character-generator RAM.

Table 4 Relationship between Character Codes and Character Pattern (ROM Code: A01)

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)																
xxxx0001	(2)																
xxxx0010	(3)																
xxxx0011	(4)																
xxxx0100	(5)																
xxxx0101	(6)																
xxxx0110	(7)																
xxxx0111	(8)																
xxxx1000	(1)																
xxxx1001	(2)																
xxxx1010	(3)																
xxxx1011	(4)																
xxxx1100	(5)																
xxxx1101	(6)																
xxxx1110	(7)																
xxxx1111	(8)																

Table 5 Relationship between Character Codes and Character Patterns (ROM Code: A02)

Upper 4 Bits / Lower 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	(2)														
xxxx0010	(3)														
xxxx0011	(4)														
xxxx0100	(5)														
xxxx0101	(6)														
xxxx0110	(7)														
xxxx0111	(8)														
xxxx1000	(1)														
xxxx1001	(2)														
xxxx1010	(3)														
xxxx1011	(4)														
xxxx1100	(5)														
xxxx1101	(6)														
xxxx1110	(7)														
xxxx1111	(8)														

Note: The character codes of the characters enclosed in the bold frame are the same as those of the first edition of the ISO8859 and the character code compatible.

• Programming character patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD66710 character generator ROM can generate 240 5×8 dot character patterns.

— Character patterns

EPROM address data and character pattern data correspond with each other to form a 5×8 dot character pattern (table 4).

Table 6 Example of Correspondence between EPROM Address Data and Character Pattern (5×8 Dots)

EPROM Address												Data					
												MSB					LSB
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0	
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1	
								0	0	0	1	1	0	0	0	1	
								0	0	1	0	1	0	0	0	1	
								0	0	1	1	0	1	0	1	0	
								0	1	0	0	0	0	1	0	0	
								0	1	0	1	0	0	1	0	0	
								0	1	1	0	0	0	1	0	0	
								0	1	1	1	0	0	0	0	0	

Character code “0” Line position

Notes:
1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern. EPROM address A3 should be set to 0.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Area which are lit (indicated by shading) are stored as 1, and unlit are as 0.
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits O_7 to O_5 are invalid. 0 should be written in all bits.

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** This is ignored by the character generator ROM for display operation so any data is acceptable.

2. **EPROM data in CG RAM area:** Always fill with zeros. (EPROM addresses 00H to FFH.)

3. **Treatment of unused user patterns in the HD66710 EPROM:** According to the user application, these are handled in either of two ways:

   a. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.

   b. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 7 Example of Correspondence between Character Code and Character Pattern (5 × 8 Dots) in CGRAM

a) When Character Pattern in 5 × 8 Dots

Character code (DDRAM data)								CGRAM address						MSB			CGRAM data					LSB	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0		
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1		
											0	0	1				1	0	0	0	1		
											0	1	0				1	0	0	0	1		
											0	1	1				0	1	0	1	0		
											1	0	0				0	0	1	0	0		
											1	0	1				0	0	1	0	0		
											1	1	0				0	0	1	0	0		
											1	1	1				0	0	0	0	0		
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1		
											0	0	1				1	0	0	0	1		
											0	1	0				1	0	0	0	1		
											0	1	1				0	1	0	1	0		
											1	0	0				0	0	1	0	0		
											1	0	1				0	0	1	0	0		
											1	1	0				0	0	1	0	0		
											1	1	1				0	0	0	0	0		

Character pattern (1)

Character pattern (8)

Table 7 Example of Correspondence between Character Code and Character Pattern (5 × 8 Dots) in CGRAM (cont)

b) When Character Pattern is 6 × 8 Dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in table 5. Characters with 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters with 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected.

   Bit 3 of the character code is invalid (*). Therefore, for example, the character codes 00 (hexadecimal) and 08 (hexadecimal) correspond to the same CGRAM address.
5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CGRAM.

   When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display.

   When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

* Indicates no effect.

Table 8 Relationships between SEGRAM Addresses and Display Patterns

SEGRAM address			SEGRAM data															
			a) 5-dot font width								b) 6-dot font width							
A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
			Blinking control			Pattern on/off					Blinking control		Pattern on/off					

Notes:
1. Data set to SEGRAM is output when COM17 is selected, as for a 1-line display, and output when COM33 is selected, as for a 2-line or a 4-line display.
2. S1 to S48 are pin numbers of the segment output driver.
   S1 is positioned to the left of the monitor.
   S37 to S48 are extension driver outputs for a 6-dot character width.
3. After S40 output at 5-dot font and S48 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on.off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEGRAM.
   When bit 7 is 1, only a bit set to “1” of the lower six bits is blinked on the display.
   When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the CGRAM data correspond to display selection, and zeros to non-selection.

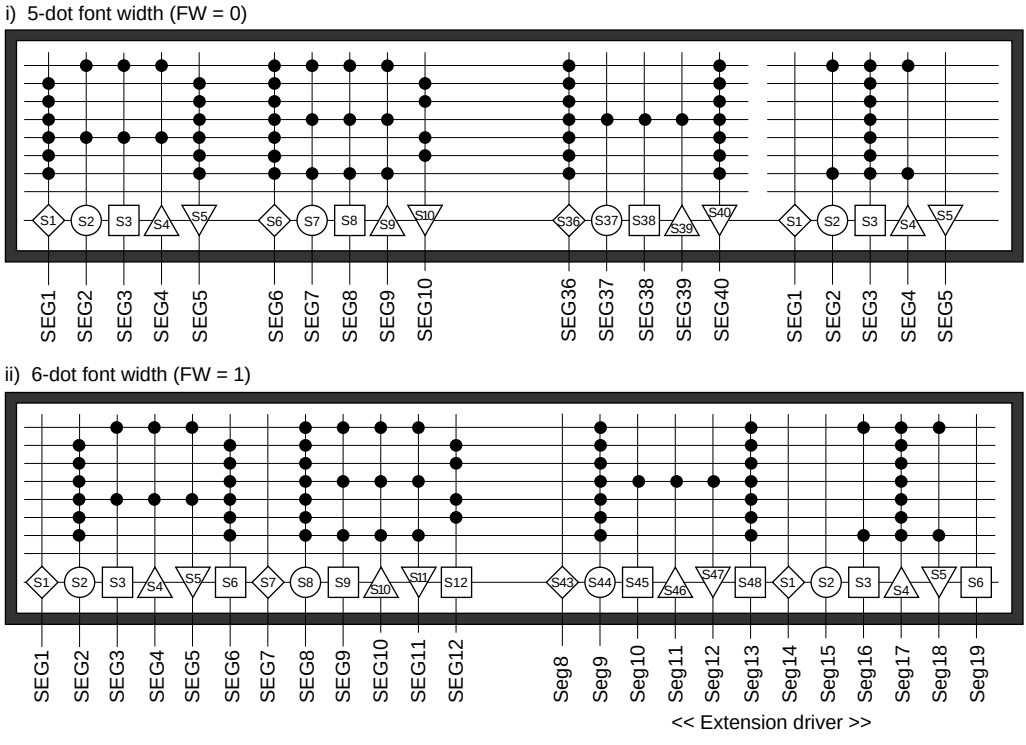


Figure 10 Relationships between SEGRAM Data and Display

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM, CG RAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 33 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs.

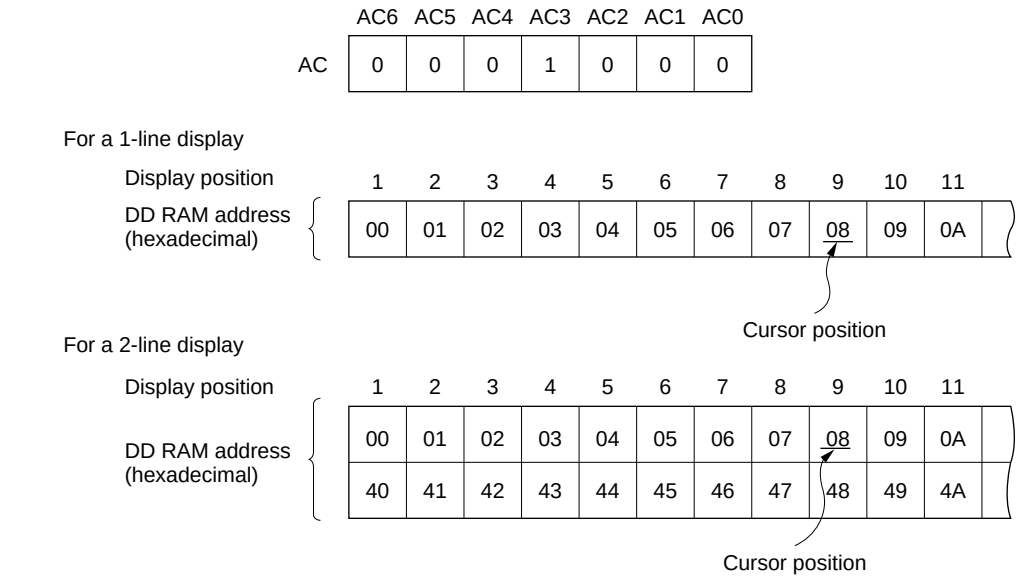
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66710 drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

For example (figure 11), when the address counter is 08H, a cursor is displayed at a position corresponding to DDRAM address 08H.



Note: Even if the address counter (AC) points to an address in the character generator RAM (CGRAM) or segment RAM (SEGRAM), cursor/blink black-white inversion will still occur, although it will produce meaningless results.

Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD66710 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66710 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transfered before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

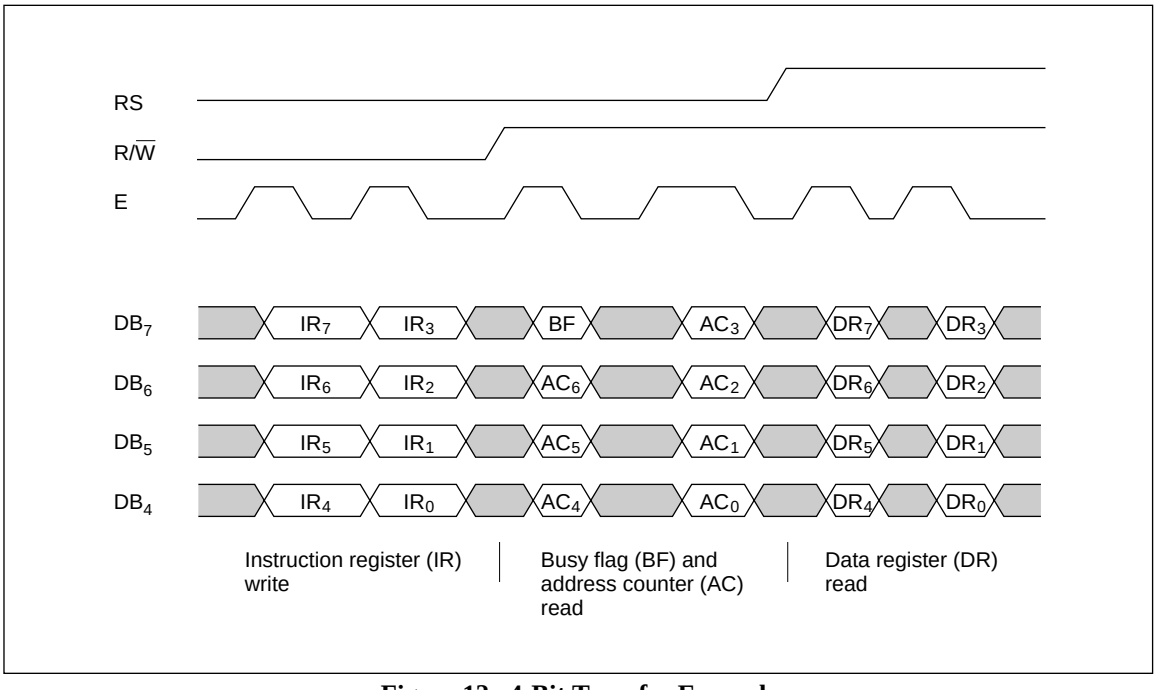


Figure 12 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66710 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the V_{CC} rises to 2.7 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   RE = 0; Extension register write disable
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
   BE = 0; CGRAM/SEGRAM blinking off
   LP = 0; Not in low power mode
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift
5. Extension function set:
   FW = 0; 5-dot character width
   B/W = 0; Normal cursor (eighth line)
   NW = 0; 1- or 2-line display (depending on N)
6. SEGRAM address set:
   HDS = 000; No scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66710. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66710 can be controlled by the MPU. Before starting internal operation of the HD66710, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66710 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{W}$), and the data bus (DB0 to DB7), make up the HD66710 instructions (table 7). There are four categories of instructions that:

- Designate HD66710 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66710 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 7) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66710 is not in the busy state (BF = 1) before sending an instruction from the MPU to the HD66710. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 7 for the list of each instruction execution time.

Table 9 Instructions

Instruction	Code RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (Max) (when f_{cp} or f_{OSC} is 270 kHz)
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.52 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control (RE = 0)	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Extension function set (RE = 1)	0	0	0	0	0	0	1	FW	B/W	NW	Sets a font width, a black-white inverting cursor (B/W), a 6-dot font width (FW), and a 4-line display (NW).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Function set (RE = 0)	0	0	0	0	1	DL	N	RE	—	—	Sets interface data length (DL), number of display lines (N), and extension register write enable (RE).	37 µs
(RE = 1)	0	0	0	0	1	DL	N	RE	BE	LP	Sets CGRAM/SEGRAM blinking enable (BE), and low power mode (LP). LP is available when the EXT pin is low.	37 µs
Set CGRAM address (RE = 0)	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set DDRAM address (RE = 0)	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Set SEGRAM address (RE = 1)	0	0	1	HDS	HDS	HDS	*—	ASG	ASG	ASG	Sets SEGRAM address. DDRAM data is sent and received after this setting. Also sets a horizontal dot scroll quantity (HDS).	37 µs

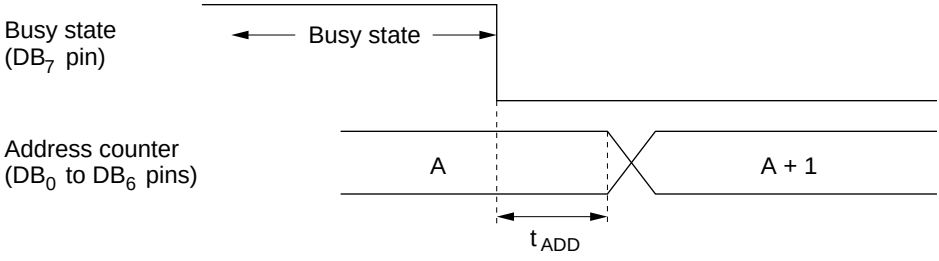
Table 9 Instructions (cont)

Instruction	Code RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (Max) (when f_{cp} or f_{OSC} is 270 kHz)
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write data to RAM (RE = 0/1)	1	0	Write data								Writes data into DD RAM, CG RAM, or SEGRAM. To write data to DD RAM CG RAM, clear RE to 0; or to write data to SEG RAM, set RE to 1.	37 µs t_{ADD} = 5.5 µs*
Read data from RAM (RE = 0/1)	1	1	Read data								Reads data from DD RAM, CG RAM, or SEGRAM. To read data from DD RAM or CG RAM, clear RE to 0; to read data from SEG RAM, set RE to 1.	37 µs t_{ADD} = 5.5 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift D = 1: Display on C = 1: Cursor on B = 1: Blink on FW = 1: 6-dot font width B/W = 1: Black-white inverting cursor on NW = 1: Four lines NW = 0: One or two lines S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line RE = 1: Extension register access enable BE = 1: CGRAM/SEGRAM blinking enable LP = 1: Low power mode BF = 1: Internally operating BF = 0: Instructions acceptable											DD RAM: Display data RAM CG RAM: Character generator RAM SEGRAM: Segment RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (corresponds to cursor address) ASEG: Segment RAM address HDS: Horizontal dot scroll quantity AC: Address counter used for both DD, CG, and SEG RAM addresses.	

Notes: 1. — indicates no effect.

* After execution of the CG RAM/DD RAM/SEGRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off.
In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. Extension time changes as frequency changes. For example, when f is 300 kHz, the execution time is: 37 µs × 270/300 = 33 µs.
3. Execution time in a low power mode (LP = 1 & EXT = low) becomes four times as long as for a 1-line mode, and twice as long as for a 2- or 4-line mode.



Note: t_{ADD} depends on the operation frequency
$t_{ADD} = 1.5/(f_{cp}$ or $f_{OSC})$ seconds

Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change. It resets the extended register enable bit (RE) to 0 in function set.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed). It resets the extended register enable bit (RE) to 0 in function set.

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. In a low power mode (LP = 1), do not set S = 1 because the whole display does not normally shift.

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font.

B: The character indicated by the cursor blinks when B is 1 (figure 14). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 370-ms intervals when f_{cp} or f_{OSC} is 270 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 300 kHz, 370 × 270/300 = 333 ms.)

Extended Function Set

When the extended register enable bit (RE) is 1, FW, B/W, and NW bit shown below are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the leftmost bit, and the font is displayed with a 5-bit character width. If the FW bit is changed, data in DD RAM and CG RAM SEG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See “Oscillator Circuit” for details.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white invertion. At this time, bits C and B in display on/off control register are “Don’t care”. When f_{CP} or f_{OSC} is 270 kHz, display is changed by switching every 370 ms.

NW: When NW is 1, 4-line display is performed. At this time, bit N in the function set register is “Don’t care”.

Note: After changing the N or NW or LP bit, please issue the return home or clear display instructions to cancel to shift display.

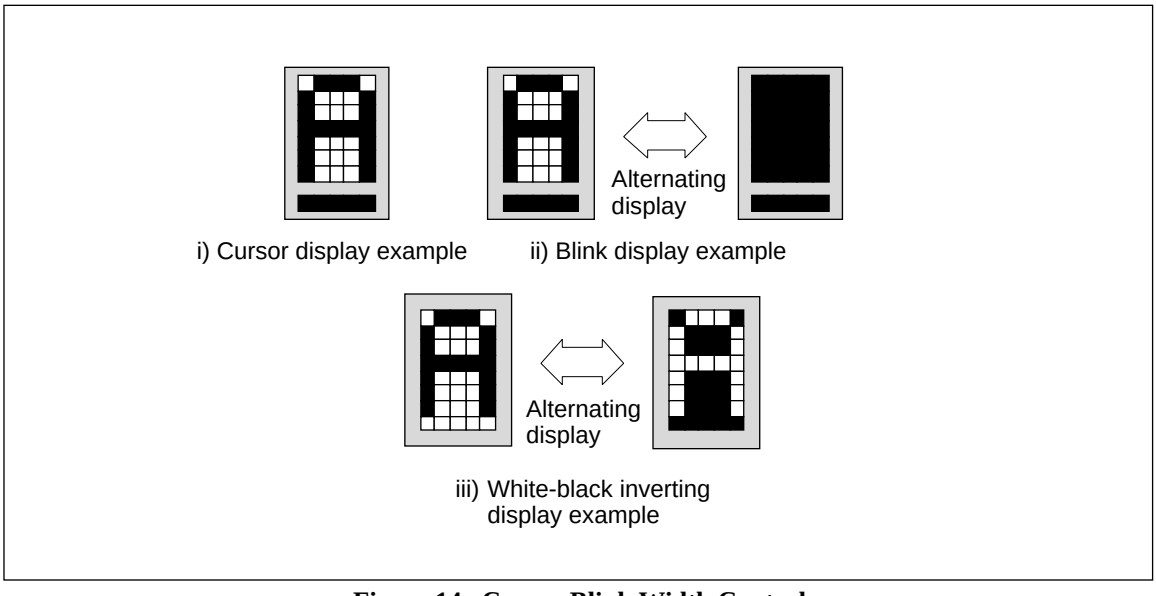


Figure 14 Cursor Blink Width Control

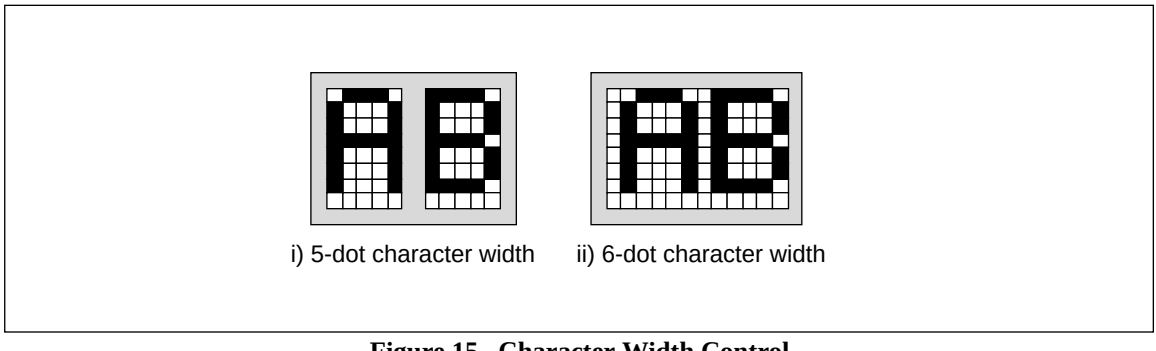


Figure 15 Character Width Control

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. In a 4-line display, the cursor moves to the second line when it passes the 20th character of the line. Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

These instruction reset the extended register enable bit (RE) to 0 in function set.

The address counter (AC) contents will not change if the only action performed is a display shift.

In low power mode (LP = 1), whole-display shift cannot be normally performed.

Function Set

Only when the extended register enable bit (RE) is 1, the BE bit shown below can be accessed. Bits DL and N can be accessed regardless of RE.

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

Table 10 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

N: When bit NW in the extended function set is 0, a 1- or a 2-line display is set. When N is 0, 1-line display is selected; when N is 1, 2-line display is selected. When NW is 1, a 4-line display is set. At this time, N is “Don’t care”.

RE: When the RE bit is 1, bit BE and LP in the extended function set registe, the SEGRAM address set register, and the extended function set register can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

To maintain compatibility with the HD44780, the RE bit should be fixed to 0.

Clear display, return home and cursor or display shift instruction a reset the RE bit to 0.

BE: When the RE bit is 1, this bit can be rewritten. When this bit is 1, the user font in CGRAM and the segment in SEGRAM can be blinked according to the upper two bits of CGRAM and SEGRAM.

LP: When the RE bit is 1, this bit can be rewritten. When LP is set to 1 and the EXT pin is low (without an extended driver), the HD66710 operates in low power mode. In 1-line display mode, the HD66710 operates on a 4-division clock, and in a 2-line or a 4-line display mode, the HD66710 operates on a 2-division clock. According to these operations, instruction execution takes four times or twice as long. Notice that in a low power mode, display shift cannot be performed.

Note: Perform the DL, N, NW, FW functions at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, if bit N, NW, or FW is changed after other instructions are executed, RAM contents may be lost.

After changing the N or NW or LP bit, please issue the return home or clear display instruction cancel to shift display.

Set CG RAM Address

A CG RAM address can be set while the RE bit is cleared to 0. Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

Table 11 Display Line Set

N	NW	No. of Display Lines	Character Font	Duty Factor	Maximum Number of Characters/ 1 Line with Extended Drivers
0	0	1	5 × 8 dots	1/17	50 characters
1	0	2	5 × 8 dots	1/33	30 characters
*	1	4	5 × 8 dots	1/33	20 characters

Note: * Indicates don’t care.

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter while the RE bit is cleared to 0.

Data is then written to or read from the MPU for DD RAM.

However, when N and NW is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 and NW is 0 (2-line display), AAAAAAA is (00)H to (27)H for the first line, and (40)H to (67)H for the second line. When NW is 1 (4-line display), AAAAAAA is (00)H to (13)H for the first line, (20)H to (33)H for the second line, (40)H to (53)H for the third line, and (60)H to (73)H for the fourth line.

Set SEGRAM Address

Only when the extended register enable bit (RE) is 1, HS2 to HS0 and the SEGRAM address can be set.

The SEGRAM address in the binary form AAA is set to the address counter. SEGRAM can then be written to or read from by the MPU.

Note: When performing a horizontal scroll is described above by connecting an extended driver, the maximum number of characters per line decreases by one. In other words, 49 characters, 29 characters, and 19 characters are displayed in 1-line, 2-line, and 4-line modes, respectively. Notice that in low power mode (LP = 1), the display shift and scroll cannot be performed.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by all CG, DD, and SEGRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for CG RAM, DD RAM, and SEGRAM address set instructions.

Table 12 HS2 to HS0 Settings

HS2	HS1	HS0	Description
0	0	0	No shift.
0	0	1	Shift the display position to the left by one dot.
0	1	0	Shift the display position to the left by two dots.
0	1	1	Shift the display position to the left by three dots.
1	0	0	Shift the display position to the left by four dots.
1	0	1	Shift the display position to the left by five dots.
1	1	0 or 1	No shift.

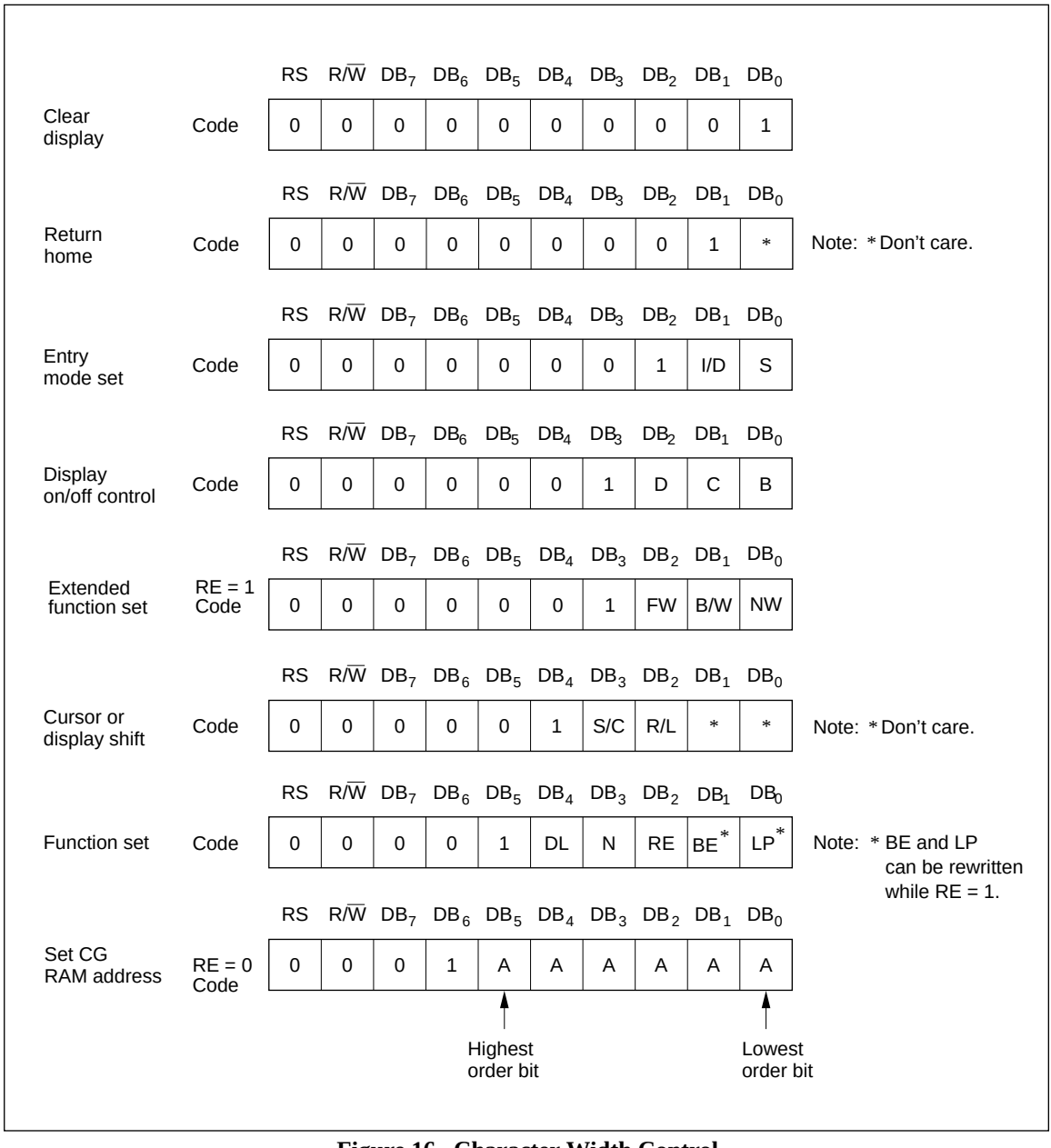


Figure 16 Character Width Control

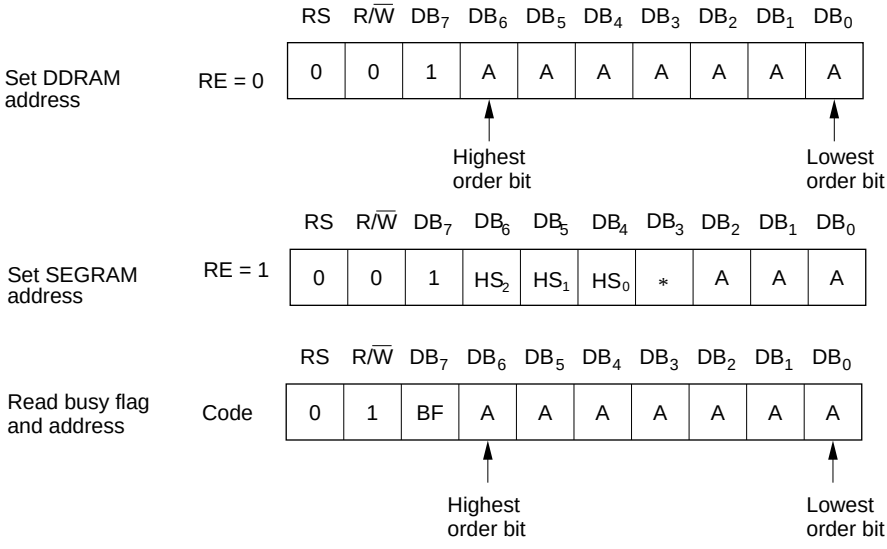


Figure 16 Character Width Control (cont)

Write Data to CG, DD, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG, DD or SEGRAM. If the RE bit is cleared, CG or DD RAM is selected, as determined by the previous specification of the address set instruction; if the RE bit is set, SEG RAM is selected. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG, DD, or SEG RAM. If the RE bit is cleared, CG or DD RAM is selected, as determined by the previous specification of the address set instruction; if the RE bit is set, SEG RAM is selected. If no address is specified, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

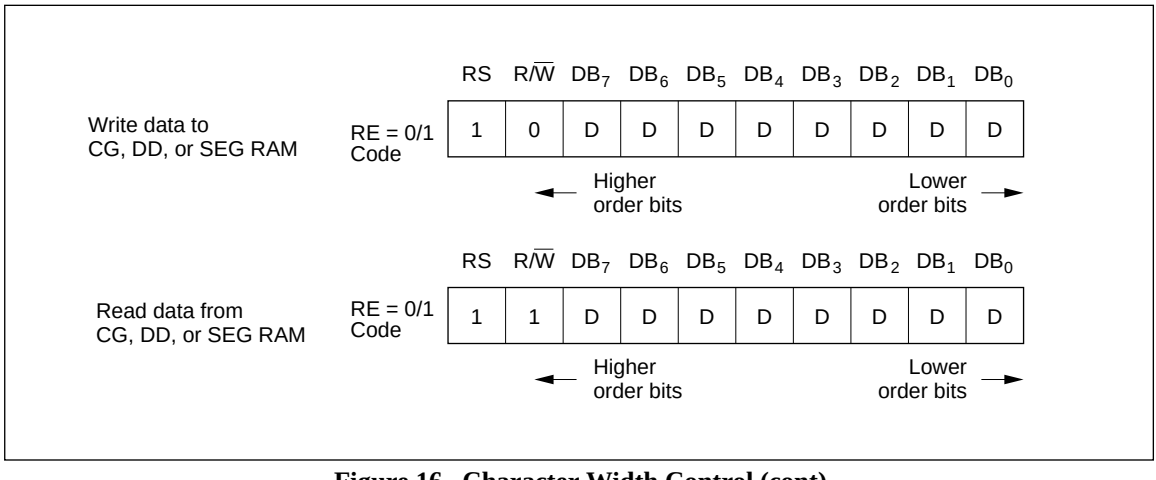


Figure 16 Character Width Control (cont)

Interfacing the HD66710

1) Interface to 8-Bit MPUs

HD66710 can interface to 8-bit MPU directly with E clock, or to 8-bit MCU through I/O port. When number of I/O port in MCU, or interfacing bus width, 4-bit interface function is useful.

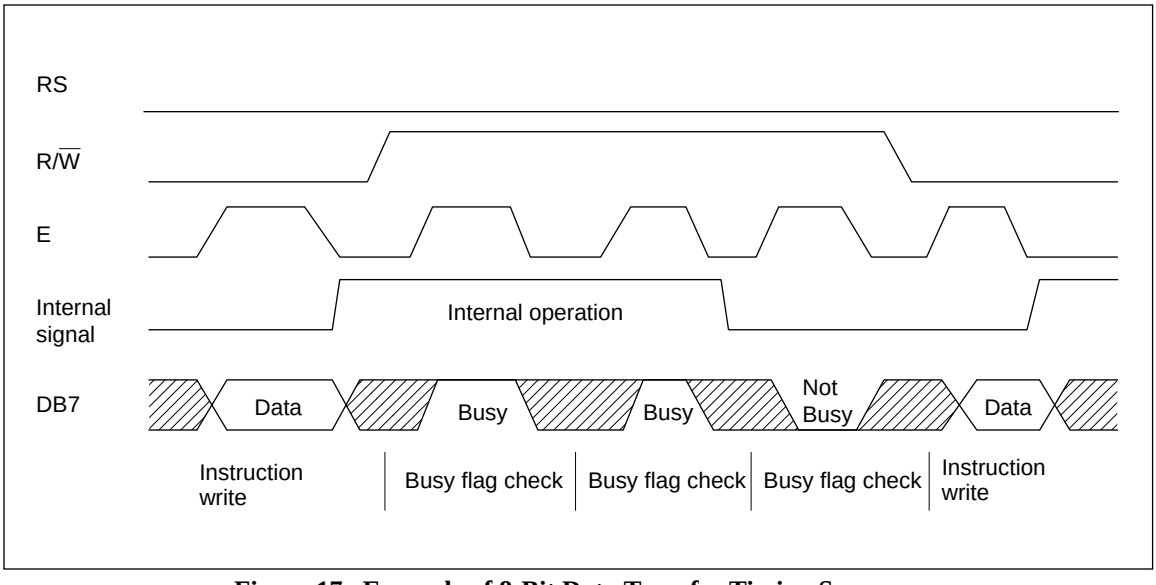
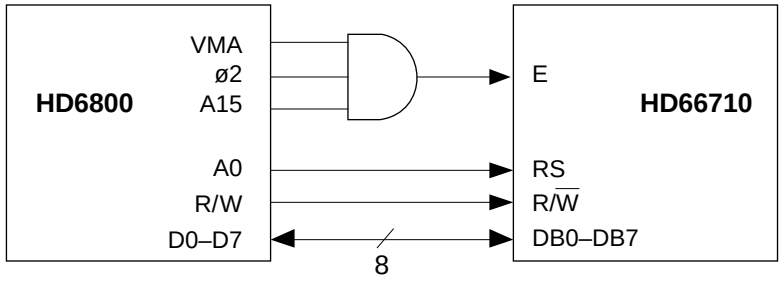
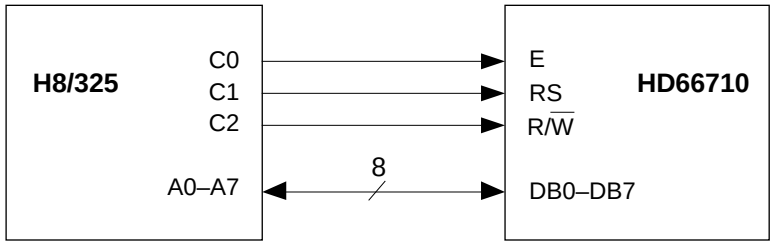


Figure 17 Example of 8-Bit Data Transfer Timing Sequence

i) Connection to 8-bit MPU bus line



ii) Connection to H8/325 with port (when single chip mode)



iii) Connection to HD6301 with port

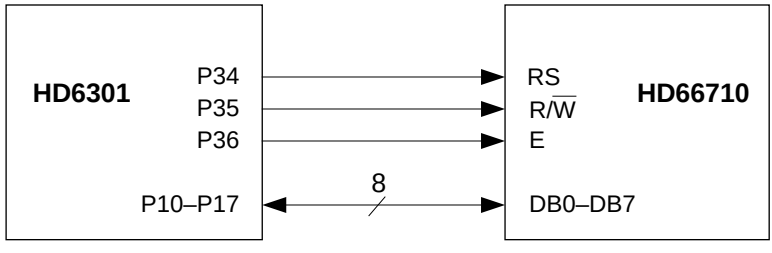


Figure 18 8-Bit MPU Interface

2) Interface to 4-Bit MPUs

HD66710 can interface to 4-bit MCU through I/O port. 4-bit data for high and low order must be transferred twice continuously. The DL bit in function set selects the interface data length.

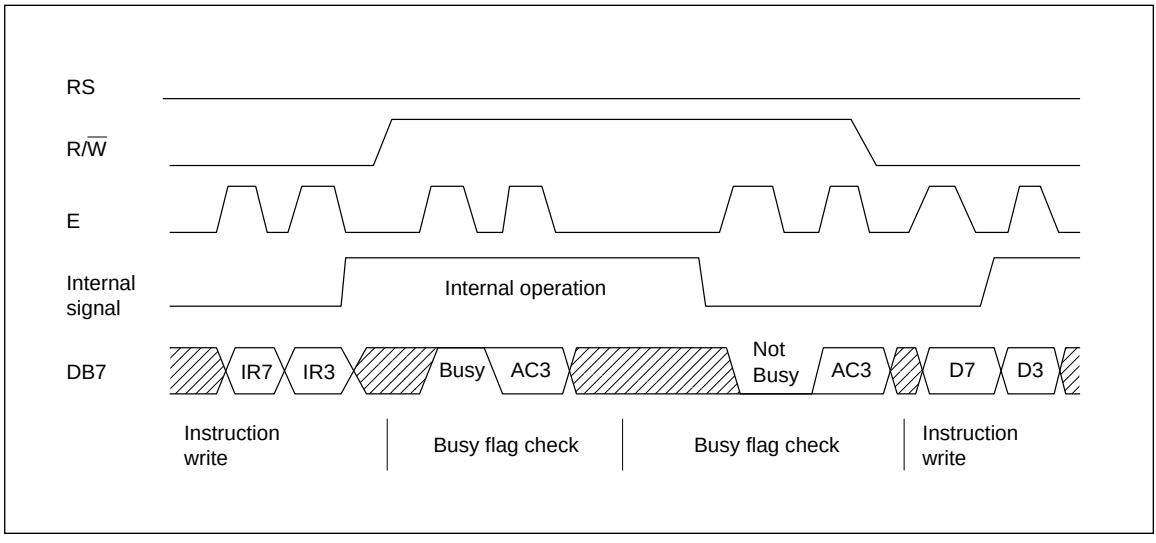


Figure 19 Example of 4-Bit Data Transfer Timing Sequence

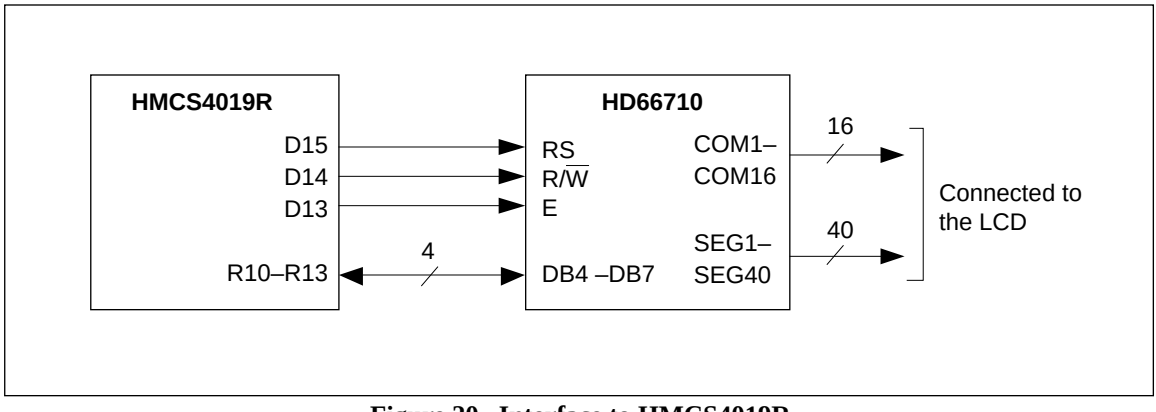


Figure 20 Interface to HMCS4019R

Oscillator Circuit

- Relationship between Oscillation frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of figure 22 apply only when the oscillation frequency is 270 kHz (one clock period: 3.7 µs).

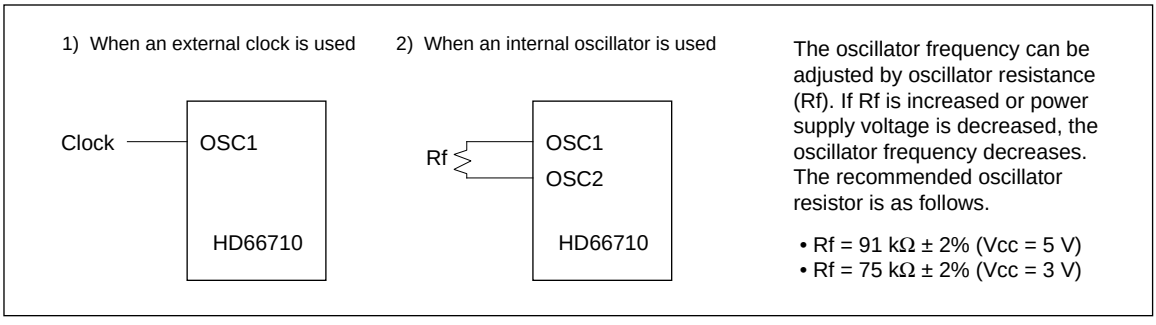
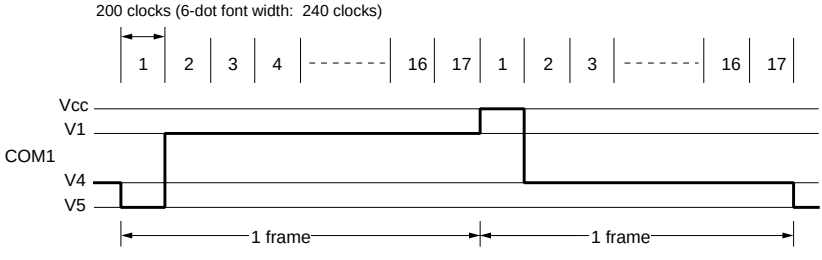


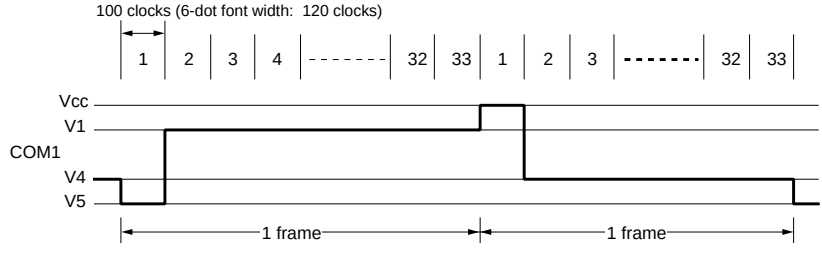
Figure 21 Oscillator Circuit

(1) 1 /17 duty cycle



	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	200 clocks	240 clocks	50 clocks	60 clocks
Frame frequency	79.4 Hz	66.2 Hz	79.4 Hz	66.2 Hz

(2) 1 /33 duty cycle

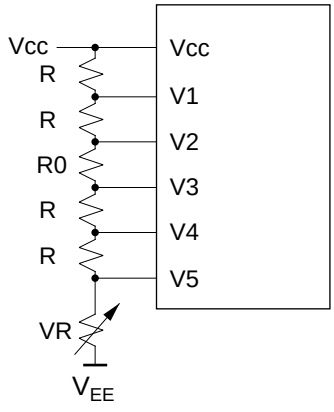


	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	100 clocks	120 clocks	50 clocks	60 clocks
Frame frequency	81.8 Hz	68.2 Hz	81.8 Hz	68.2 Hz

Figure 22 Frame Frequency

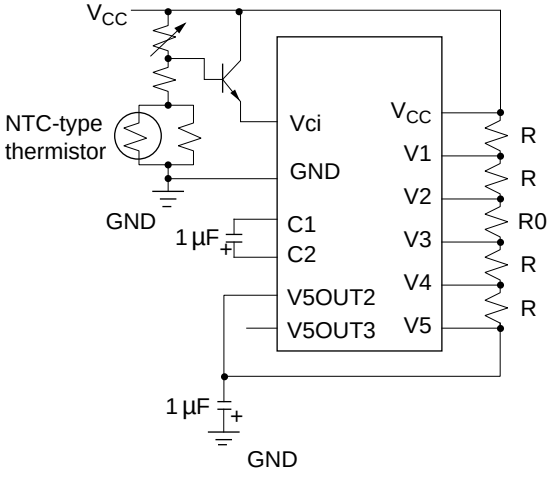
Power Supply for Liquid Crystal Display Drive

1) When an external power supply is used

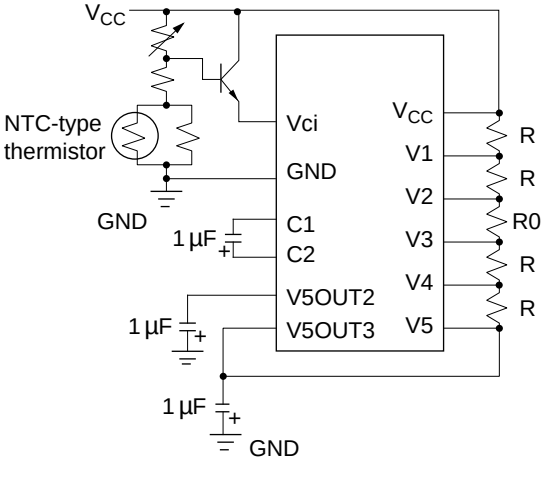


2) When an internal booster is used

(Boosting twice)



(Boosting three times)



Notes: 1. Boosting output voltage should not exceed the power supply voltage (2) (15 V max.) in the absolute maximum ratings. Especially, voltage of over 5 V should not be input to the reference voltage (Vci) when boosting three times.

2. Vci input terminal is used for reference voltage and power supply for the internal booster. Input current into the Vci pin needs three times or more of load current through the bleeder resistor for LCD. So, when it adjusts LCD driving voltage (Vlcd), input voltage should be controlled with transistor to supply LCD load current.

3. Please notice connection (+/–) when it uses capacitors with poler.

Table 13 Duty Factor and Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2/4
Duty factor		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

Note: R changes depending on the size of liquid crystal penel. Normally, R must be 4.7 kΩ to 20 kΩ.

Extension Driver LSI Interface

By bringing the EXT pin high, segment driver pins (SEG37 to SEG40) functions as the extended driver interface outputs. From these pins, a latch pulse (CL1), a shift clock (CL2), data (D), and an AC signal (M) are output. The same data is output from the SEG36 pin of the HD66710 and the start segment pin (Seg1) of the extension driver. Due to the character baundary, the Seg1 output is used for the 5-dot font width. For the 6-dot font width, the SEG36 output is used, and the Seg1 output of the extension driver must not be used. When the extension driver LSI interface is used, ground level (GND) must be higher than the V5 level.

Table 14 Required Number of 40-Output Extension Driver

Controller	HD66710*		HD44780	HD66702
Display Line	**5-Dot Width**	**6-Dot Width**	**5-Dot Width**	**5-Dot Width**
16 × 2 lines	Not required	1	1	Not required
20 × 2 lines	1	1	2	Not required
24 × 2 lines	1	2	2	1
40 × 2 lines	Disabled	Disabled	4	3
12 × 4 lines	1	1	Disabled	Disabled
16 × 4 lines	2	2	Disabled	Disabled
20 × 4 lines	2	3	Disabled	Disabled

Note: * The number of display lines can be extended to 30 × 2 lines or 20 × 4 lines.

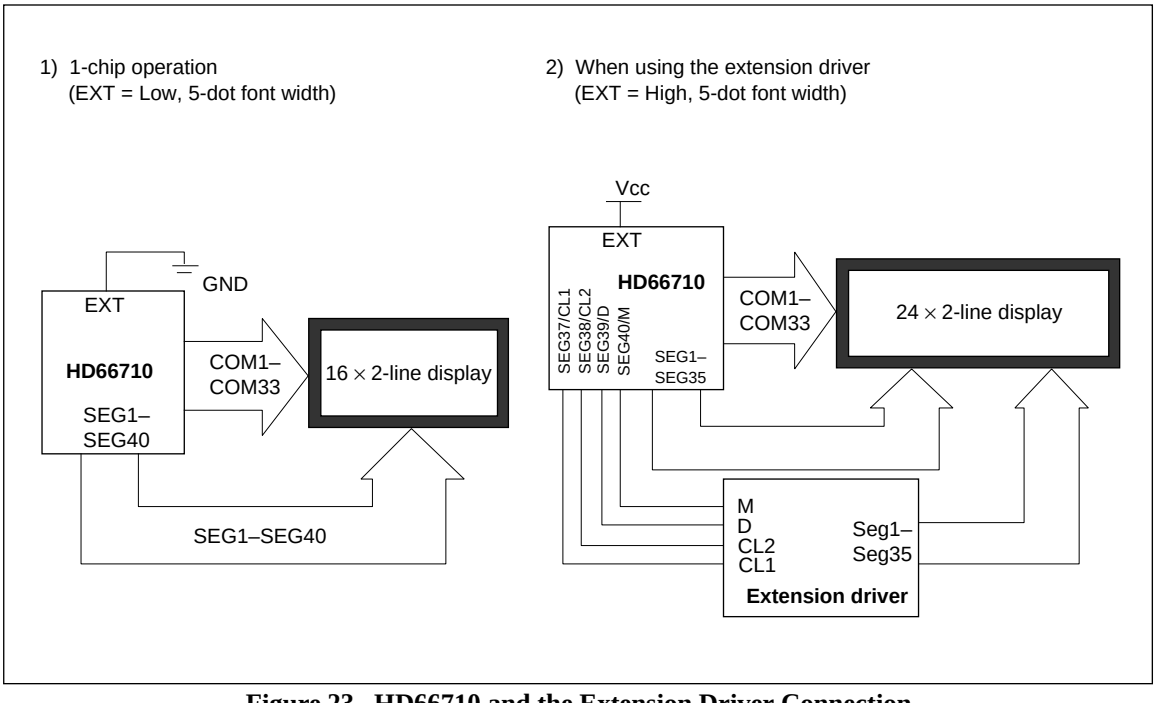


Figure 23 HD66710 and the Extension Driver Connection

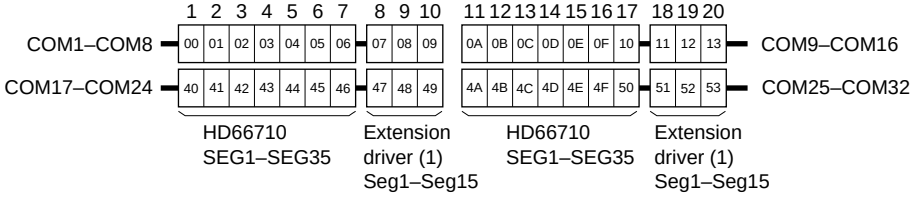
When using one HD66710, the start address of COM9–COM16/COM25–COM33 is calculated by adding 8 to the start address of COM9–COM16 COM25–COM32. When extending the address, the start address is calculated by adding A(10) to COM9–COM16/COM25 to COM32. The relationship betweenmodes and display start addresses is shown below.

Table 15 Display Start Address in Each Mode

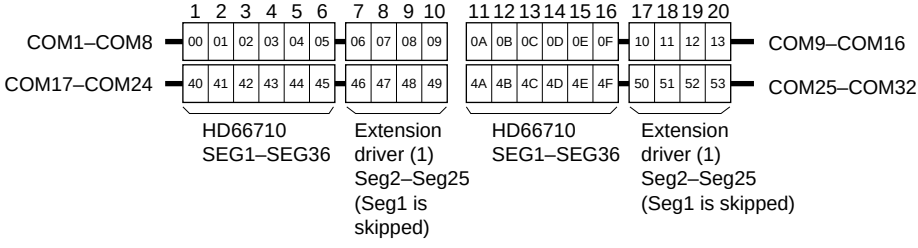
	Number of Lines				
	1-Line Mode		2-Line Mode		4-Line Mode
Output	EXT Low	EXT High	EXT Low	EXT High	EXT Low/High
COM1–COM8	D00±1	D00±1	D00±1	D00±1	D00±1
COM9–COM16	D08±1	D0A±1	D08±1	D0A±1	D20±1
COM17–COM24	—	—	D40±1	D40±1	D40±1
COM25–COM32	—	—	D48±1	D4A±1	D60±1
COM17	S00	S00	—	—	—
COM33	—	—	S00	S00	S00

Notes: 1. When an EXT pin is low, the extension driver is not used; otherwise, the extension driver is used.
2. D— is the start address of display data RAM (DDRAM) for each display line.
3. S— is the start address of segment RAM (SEGRAM).
4. ±1 following D— indicates increment or decrement at display shift.

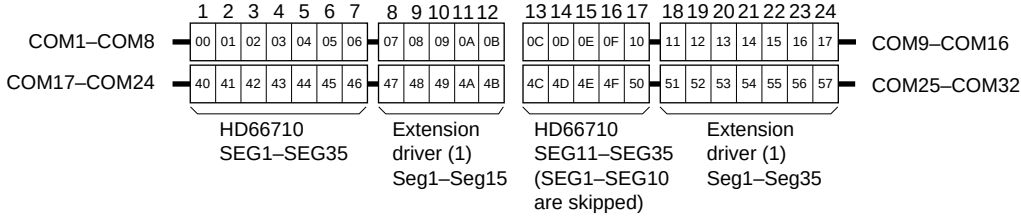
a) 5-dot font width: 20 × 2-line display



b) 6-dot font width: 20 × 2-line display



c) 5-dot font width: 24 × 2-line display



d) 6-dot font width: 24 × 2-line display

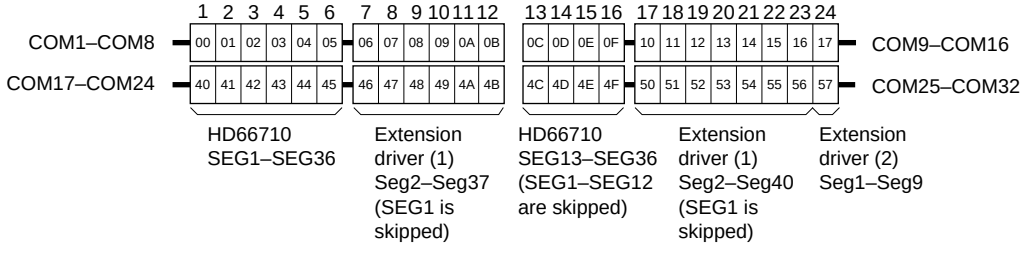
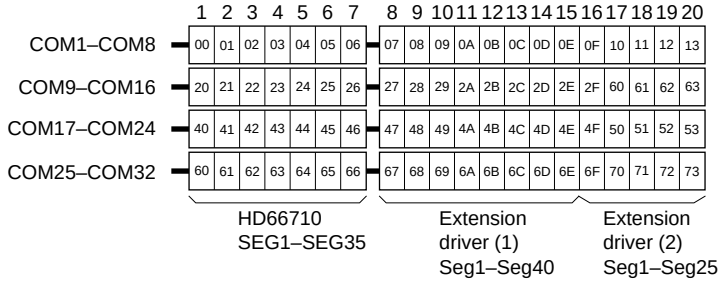


Figure 24 Correspondence between the Display Position at Extension Display and the DDRAM Address

e) 5-dot font width: 20 × 4-line display



f) 6-dot font width: 20 × 4-line display

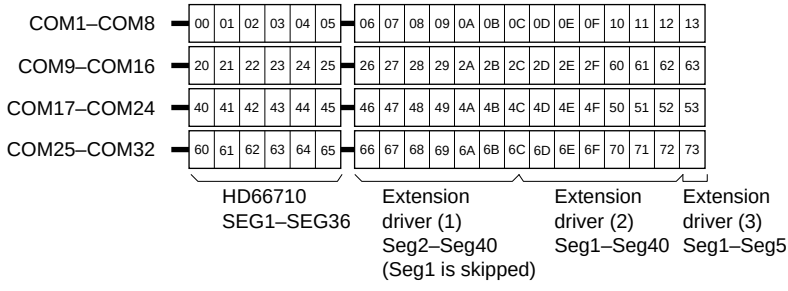


Figure 24 Correspondence between the Display Position at Extension Display and the DDRAM Address (cont)

Interface to Liquid Crystal Display

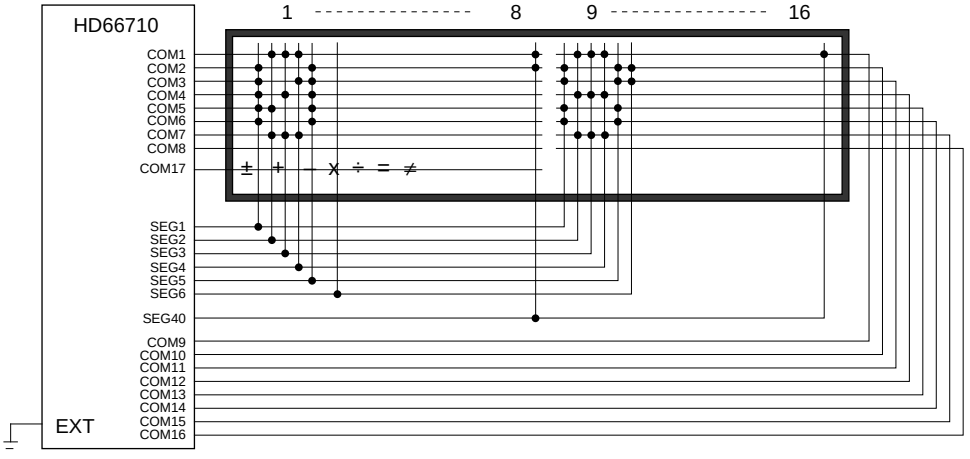
Set the extended driver interface, the number of display lines, and the font width with the EXT pin, an extended register NW, and the FW bit, respectively. The relationship between the EXT pin, register set value, and the display lines are given below.

Table 16 Relationship between EXT, Register Setting, and Display Lines

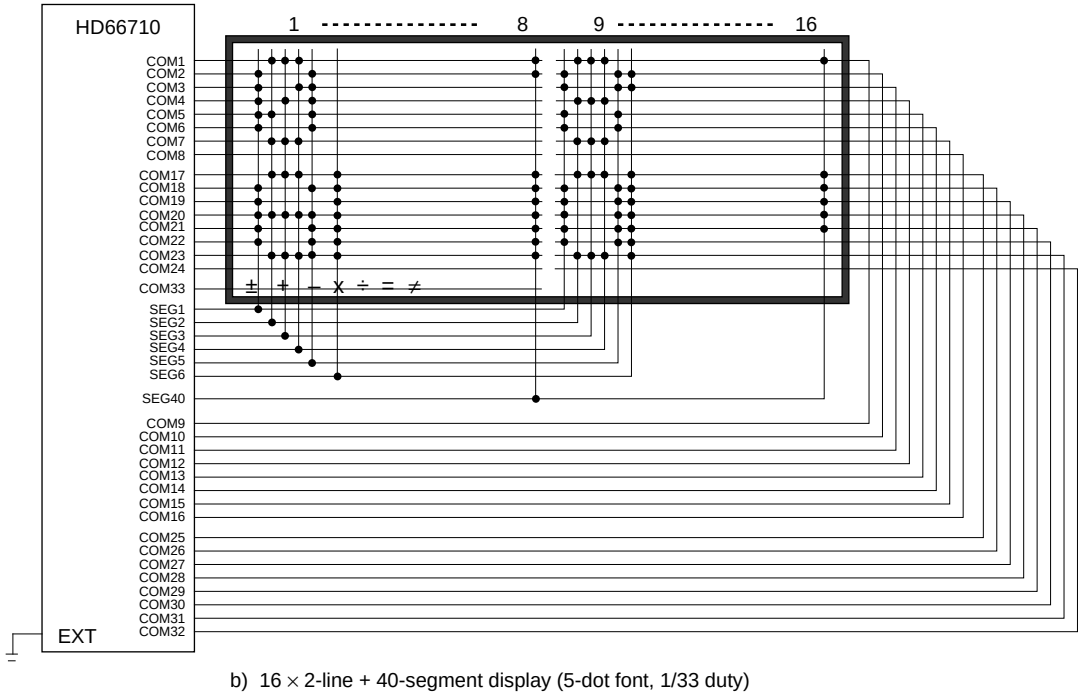
No. of Lines	No. of Charactrers	EXT Pin	Extended Driver	5-Dot Font N	RE	NW	FW	EXT Pin	Extended Driver	6-Dot Font N	RE	NW	FW	Duty
1	16	L	—	0	0	0	0	H	1	0	1	0	1	1/17
	20	H	1	0	0	0	0	H	1	0	1	0	1	1/17
	24	H	1	0	0	0	0	H	2	0	1	0	1	1/17
2	16	L	—	1	0	0	0	H	1	1	1	0	1	1/33
	20	H	1	1	0	0	0	H	1	1	1	0	1	1/33
	24	H	1	1	0	0	0	H	2	1	1	0	1	1/33
4	16	H	1	*	1	1	0	H	1	*	1	1	1	1/33
	20	H	2	*	1	1	0	H	2	*	1	1	1	1/33
	24	H	2	*	1	1	0	H	3	*	1	1	1	1/33

Note: — means not required.

• Example of 5-dot font width connection

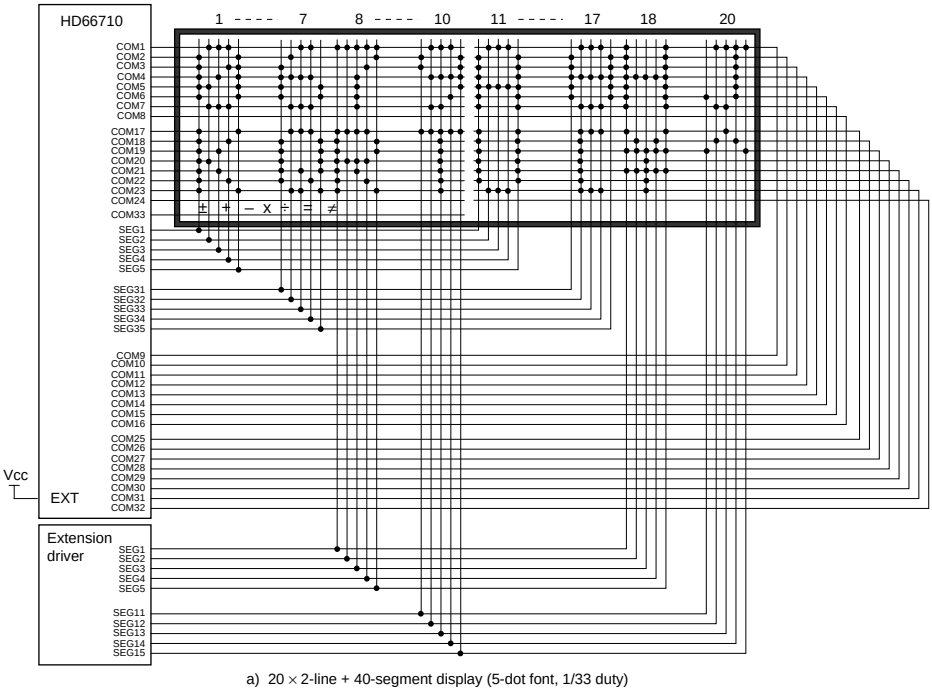


a) 16 × 1-line + 40-segment display (5-dot font, 1/17 duty)

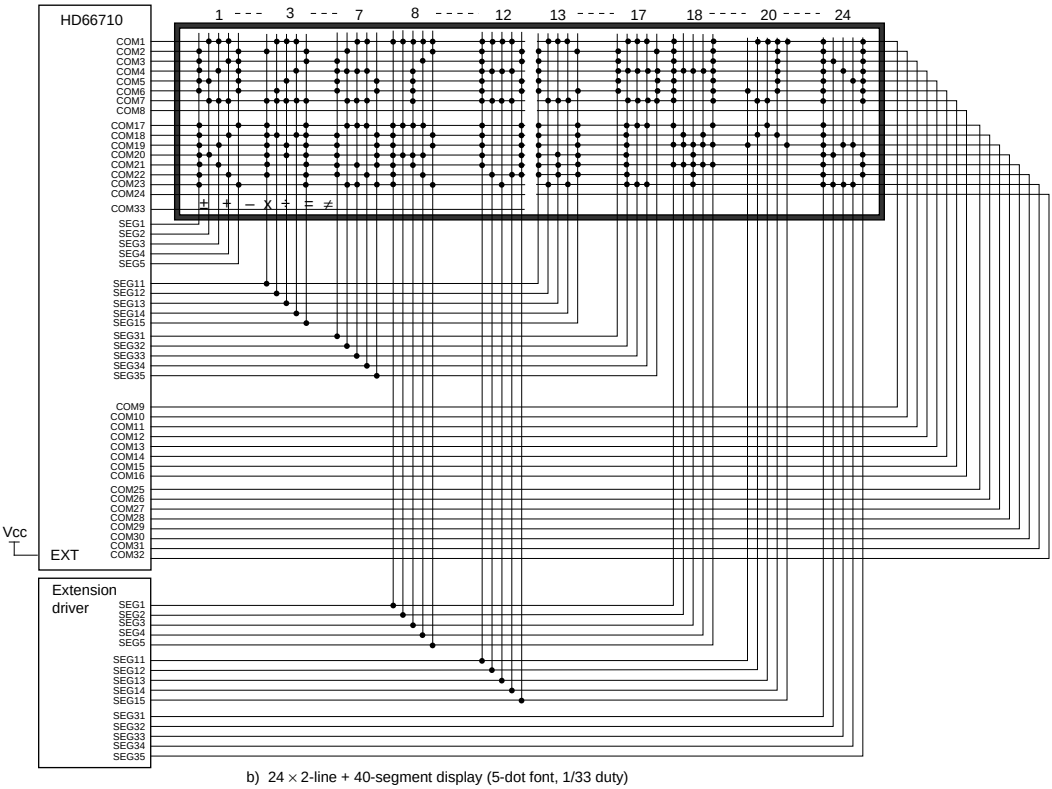


b) 16 × 2-line + 40-segment display (5-dot font, 1/33 duty)

Figure 25 Liquid Crystal Display and HD66710 Connections (Single-Chip Operation)

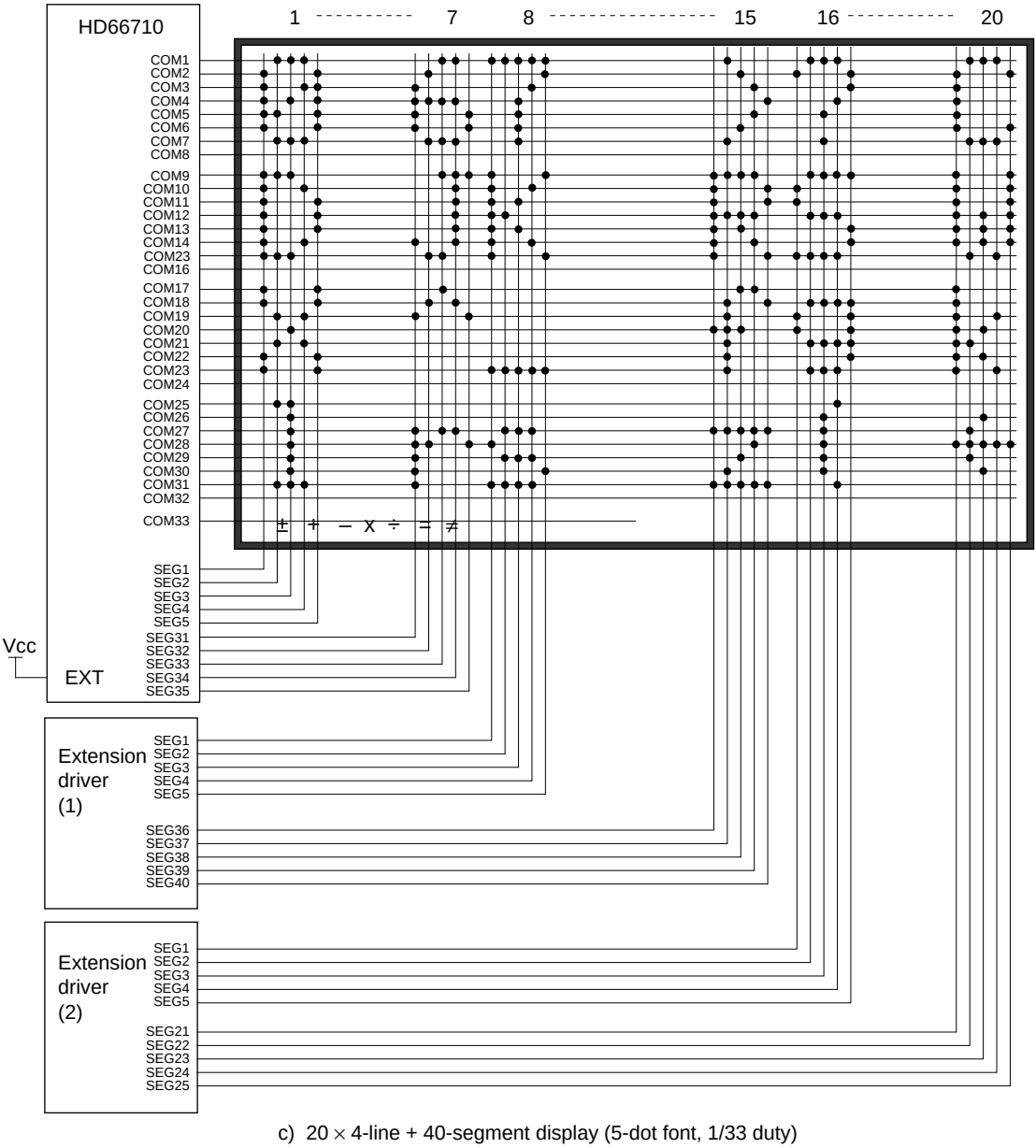


a) 20 × 2-line + 40-segment display (5-dot font, 1/33 duty)



b) 24 × 2-line + 40-segment display (5-dot font, 1/33 duty)

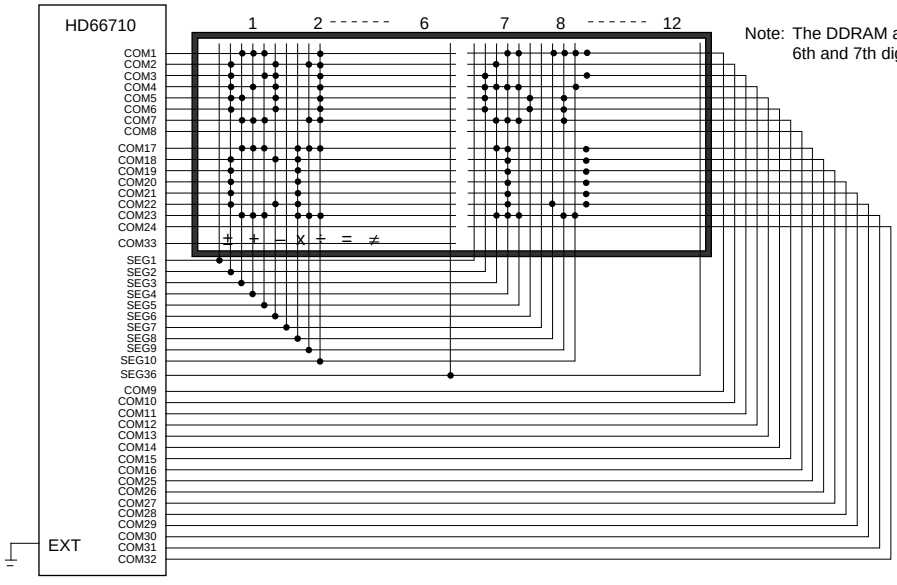
Figure 26 Liquid Crystal Display and HD66710 Connections (with the Extended Driver)



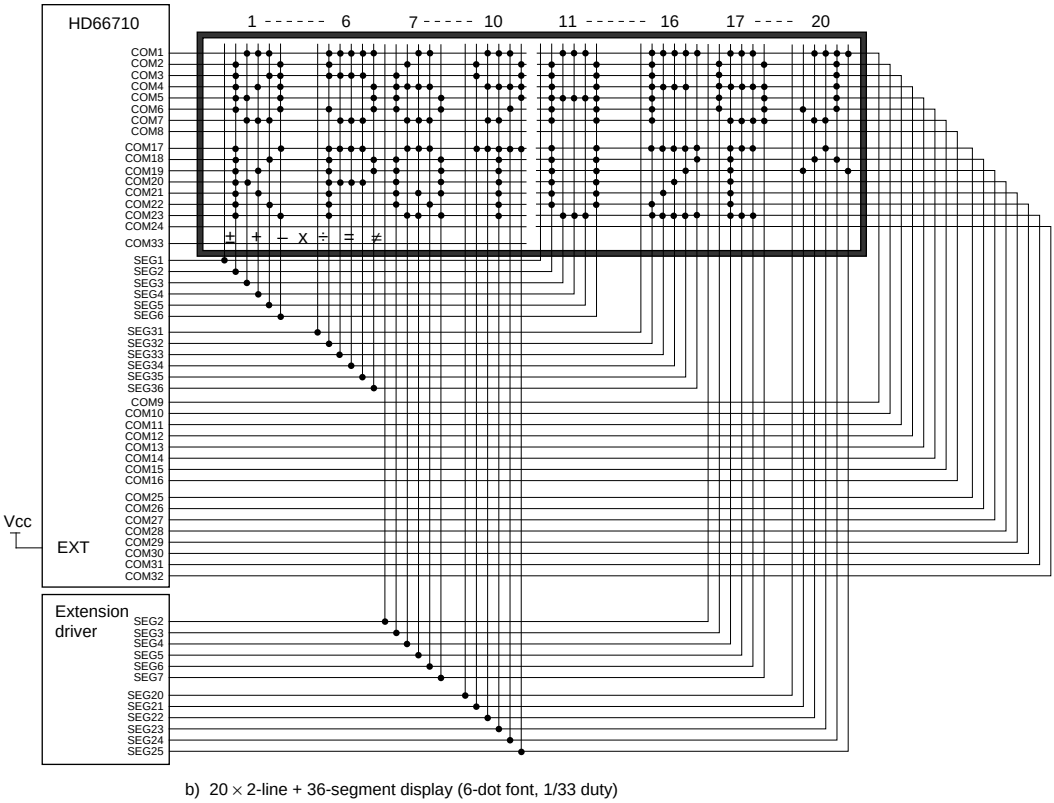
c) 20 × 4-line + 40-segment display (5-dot font, 1/33 duty)

Figure 26 Liquid Crystal Display and HD66710 Connections (with the Extended Driver) (cont)

- Example of 6-dot font width connection



a) 12 × 2-line + 36-segment display (6-dot font, 1/33 duty)



b) 20 × 2-line + 36-segment display (6-dot font, 1/33 duty)

Figure 27 Liquid Crystal Display and HD66710 Connections (6-Dot Font Width)

Instruction and Display Correspondence

- 8-bit operation, 16-digit × 1-line display with internal reset

  Refer to table 16 for an example of an 16-digit × 1-line display in 8-bit operation. The HD66710 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, a character unit scroll can be performed by a display shift instruction. A dot unit smooth scroll can also be performed by a horizontal scroll instruction. Since data of display RAM (DDRAM) is not changed by a display shift instruction, the display can be returned to the first set display when the return home operation is performed.

- 4-bit operation, 16-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (table 16). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 16). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 16-digit × 2-line display with internal reset

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 16 characters in the first line, the DD RAM address must be again set after the 16th character is completed. (See table 17.)

  The display shift is performed for the first and second lines. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

- 8-bit operation, 8-digit × 4-line display with internal reset

  The RE bit must be set by the function set instruction and then the NW bit must be set by an extension function set instruction. In this case, 4-line display is always performed regardless of the N bit setting (table 18).

  In a 4-line display, the cursor automatically moves from the first to the second line after the 20th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set again after the 8th character is completed. Display shifts are performed on all lines simultaneously.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD66710 must be initialized by instructions. See the section, Initializing by Instruction.

Table 17 8-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	0	0	*	*		Sets to 8-bit operation and selects 1-line display. Bit 2 must always be cleared.
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
6	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HI_	Writes I.
7	. . . . .										. . . . .	
8	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
9	Entry mode set	0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CG RAM/DD RAM	1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 17 8-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
11	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	. . . . .										. . . . .	
13	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	. . . . .										. . . . .	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 18 4-Bit Operation, 16-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 4-bit operation. Clear bit 2. In this case, operation is handled as 8 bits by initialization. *
	0	0	0	0	1	0	—	—	—	—		
	—	—	—	—	—	—	—	—	—	—		
3	Function set											Sets 4-bit operation and selects 1-line display. Clear BE, LP bits. 4-bit operation starts from this step.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	1	0	0	—	—	—	—		
4	Function set											Sets 4-bit operation and selects 1-line display. Clear RE bit.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	0	*	*	—	—	—	—		
5	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	0	1	0	—	—	—	—		
6	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	—	—	—	—		
	0	0	1	1	1	0	—	—	—	—		
7	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	1	1	0	—	—	—	—		
8	Write data to CG RAM/DD RAM										H_	Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	—	—	—	—		
	1	0	1	0	0	0	—	—	—	—		

Note: 1. The control is the same as for 8-bit operation beyond step #8.

2. When DB3 to DB0 pins are open in 4-bit mode, the RE, BE, LP bits are set to “1” at step #2. So, these bits are clear to “0” at step #3.

Table 19 8-Bit Operation, 16-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	1	1	1	0	*	*		Sets to 8-bit operation and selects 1-line display. Clear bit 2.
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
6	. . . . .											. . . . .	
7	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
8	Set DD RAM address	0	0	1	1	0	0	0	0	0	0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.

Table 19 8-Bit Operation, 16-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
9	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	0	1	HITACHI M_	Writes a space.
10					:						:	
11	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	1	1	HITACHI MICROCO_	Writes O.
12	Entry mode set 0	0	0	0	0	0	0	1	1	1	HITACHI MICROCO_	Sets mode to shift display at the time of write.
13	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	0	1	ITACHI ICROCOM_	Writes M.
14					:						:	
15	Return home 0	0	0	0	0	0	0	0	1	0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).

Table 20 8-Bit Operation, 8-Digit × 4-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
1	Power supply on (the HD66710 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	0	1	*	*		Sets to 8 bit operation and the extended register enable bit.
3	4-line mode set	0	0	0	0	0	0	1	0	0	1		Sets 4-line display.
4	Function set Clear extended register enable bit	0	0	0	0	1	1	0	0	*	*		Clears the extended register enable bit. Setting the N bit is “don’t care”.
5	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
6	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
7	Write data to CGRAM/DDRAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DDRAM has already been selected by initialization when the power was turned on.
8	—												

Table 20 8-Bit Operation, 8-Digit × 4-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Display	Operation
9	Write data to CGRAM/DDRAM 1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
10	Set DDRAM address 0	0	1	0	1	0	0	0	0	0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.
11	Write data to CGRAM/DDRAM 1	0	0	0	1	1	0	0	0	0	HITACHI 0_	Writes 0.

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

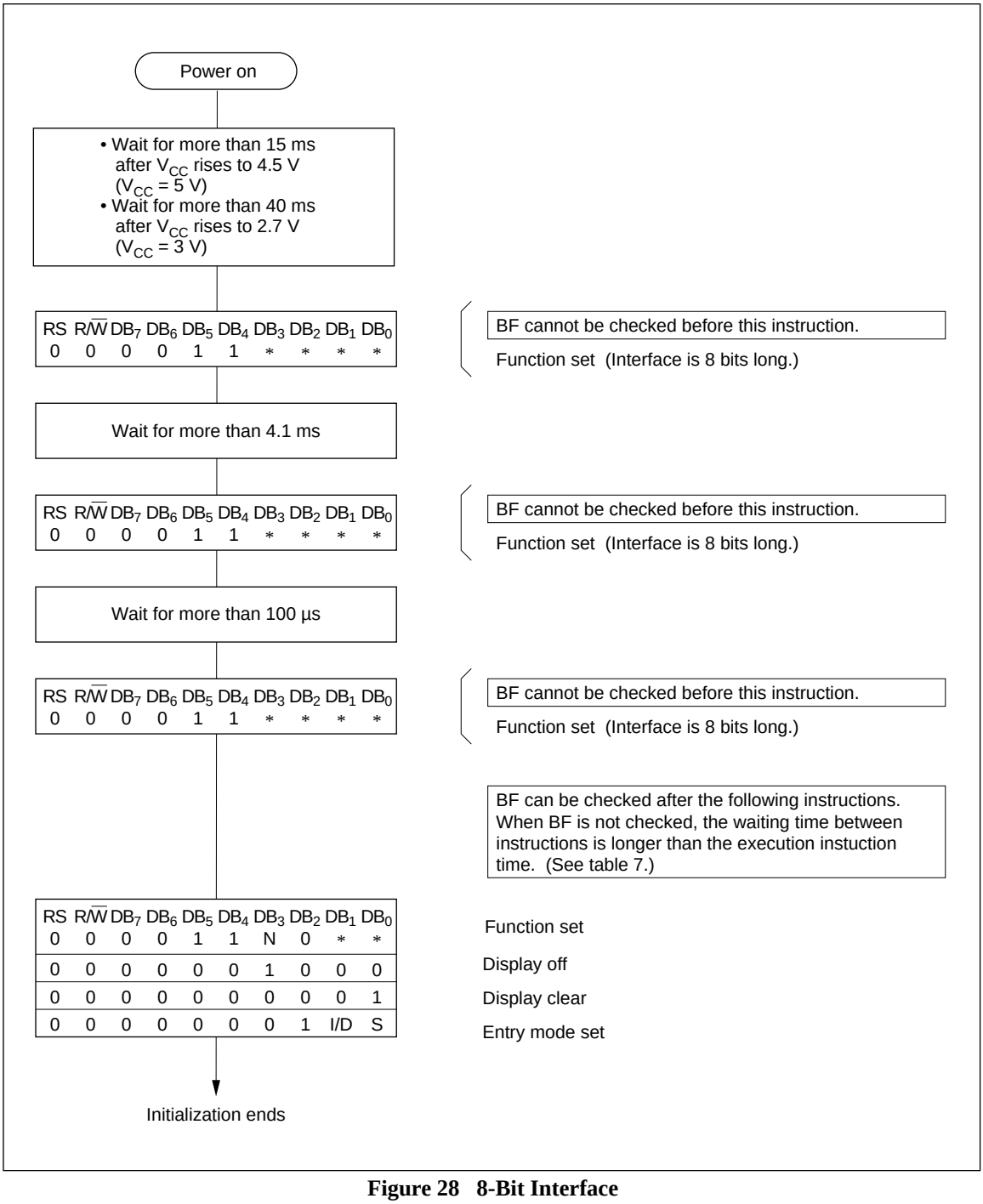


Figure 28 8-Bit Interface

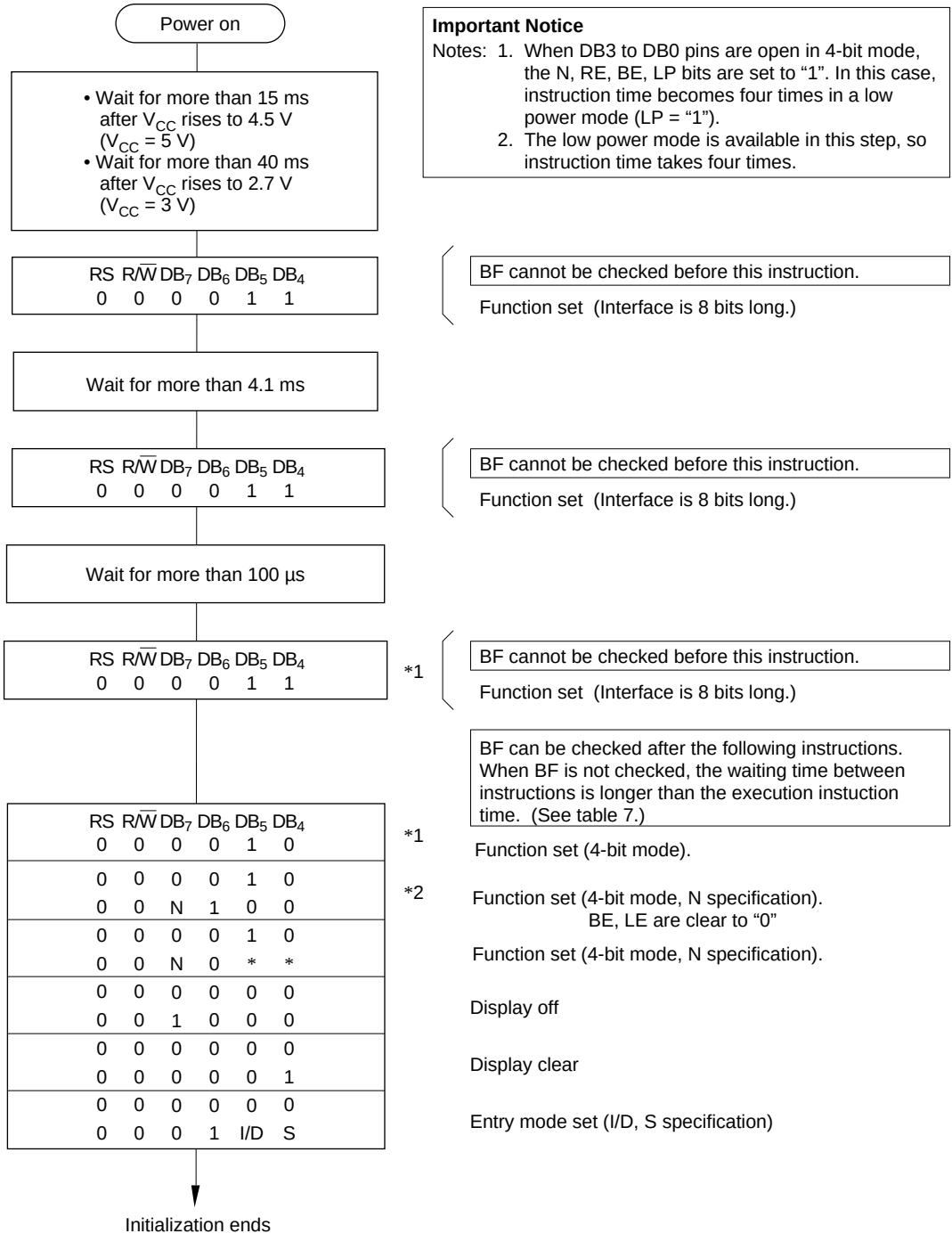


Figure 29 4-Bit Interface

Horizontal Dot Scroll

Dot unit shifts are performed by setting the horizontal dot scroll bit (HDS) when the extension register is enabled (RE = 1). By combining this with character unit display shift instructions, smooth horizontal scrolling can be performed on a 6-dot font width display as shown below.

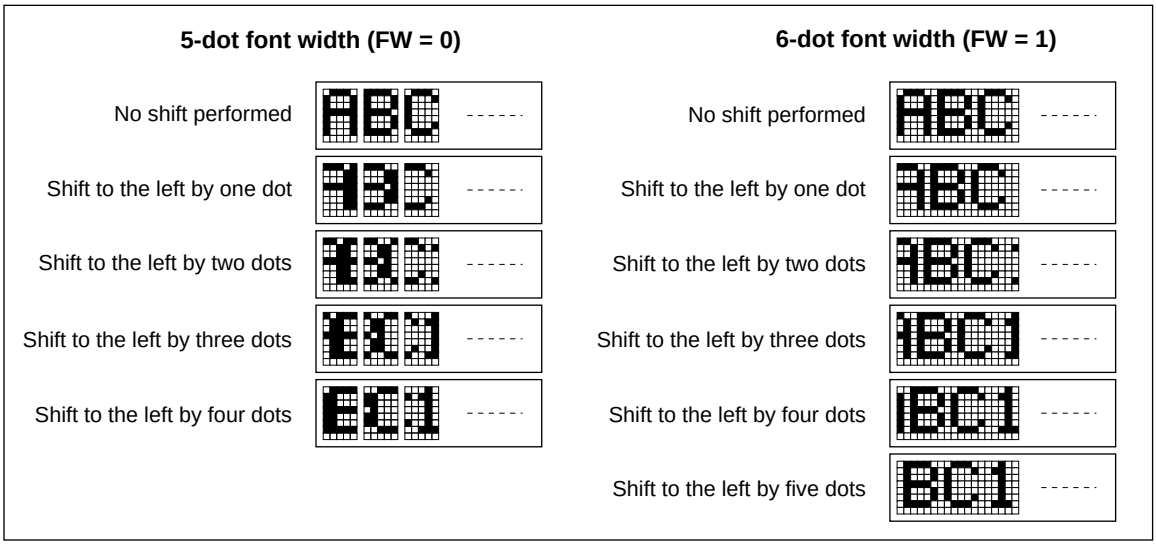


Figure 30 Shift in 5- and 6-Dot Font Width

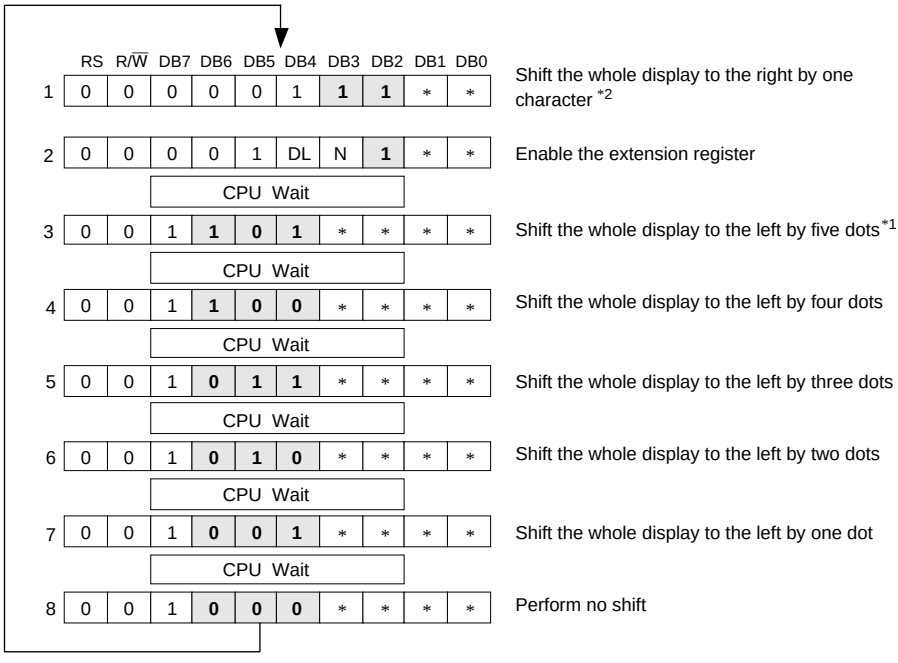
(1) Method of smooth scroll to the left

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	1	DL	N	**1**	*	*	Enable the extension register
2	0	0	1	**0**	**0**	**1**	*	*	*	*	Shift the whole display to the left by one dot
	CPU Wait										
3	0	0	1	**0**	**1**	**0**	*	*	*	*	Shift the whole display to the left by two dots
	CPU Wait										
4	0	0	1	**0**	**1**	**1**	*	*	*	*	Shift the whole display to the left by three dots
	CPU Wait										
5	0	0	1	**1**	**0**	**0**	*	*	*	*	Shift the whole display to the left by four dots
	CPU Wait										
6	0	0	1	**1**	**0**	**1**	*	*	*	*	Shift the whole display to the left by five dots *1
	CPU Wait										
7	0	0	1	**0**	**0**	**0**	*	*	*	*	Perform no shift
8	0	0	0	0	0	1	**1**	**0**	*	*	Shift the whole display to the left by one character *2
	CPU Wait										

Notes: 1. When the font width is five (FW = 0), this step is skipped.
2. The extended register enable bit (RE) is cleared.

Figure 31 Smooth Scroll to the Left

(2) Method of smooth scroll to the right



Notes: 1. When the font width is five (FW = 0), this step is skipped.
2. The extended register enable bit (RE) is cleared.

Figure 31 Smooth Scroll to the Left (cont)

Low Power Mode

When LP bit is 1 and the EXT pin is low (without an extended driver), the HD66710 operates in low power mode. In 1-line display mode, the HD66710 operates on a 4-division clock, and in 2-line or 4-line display mode, it operates on 2-division clock. So, instruction execution takes four times or twice as long. Notice that in this mode, display shift and scroll cannot be performed. Clear display shift with the return home instruction, and the horizontal scroll quantity.

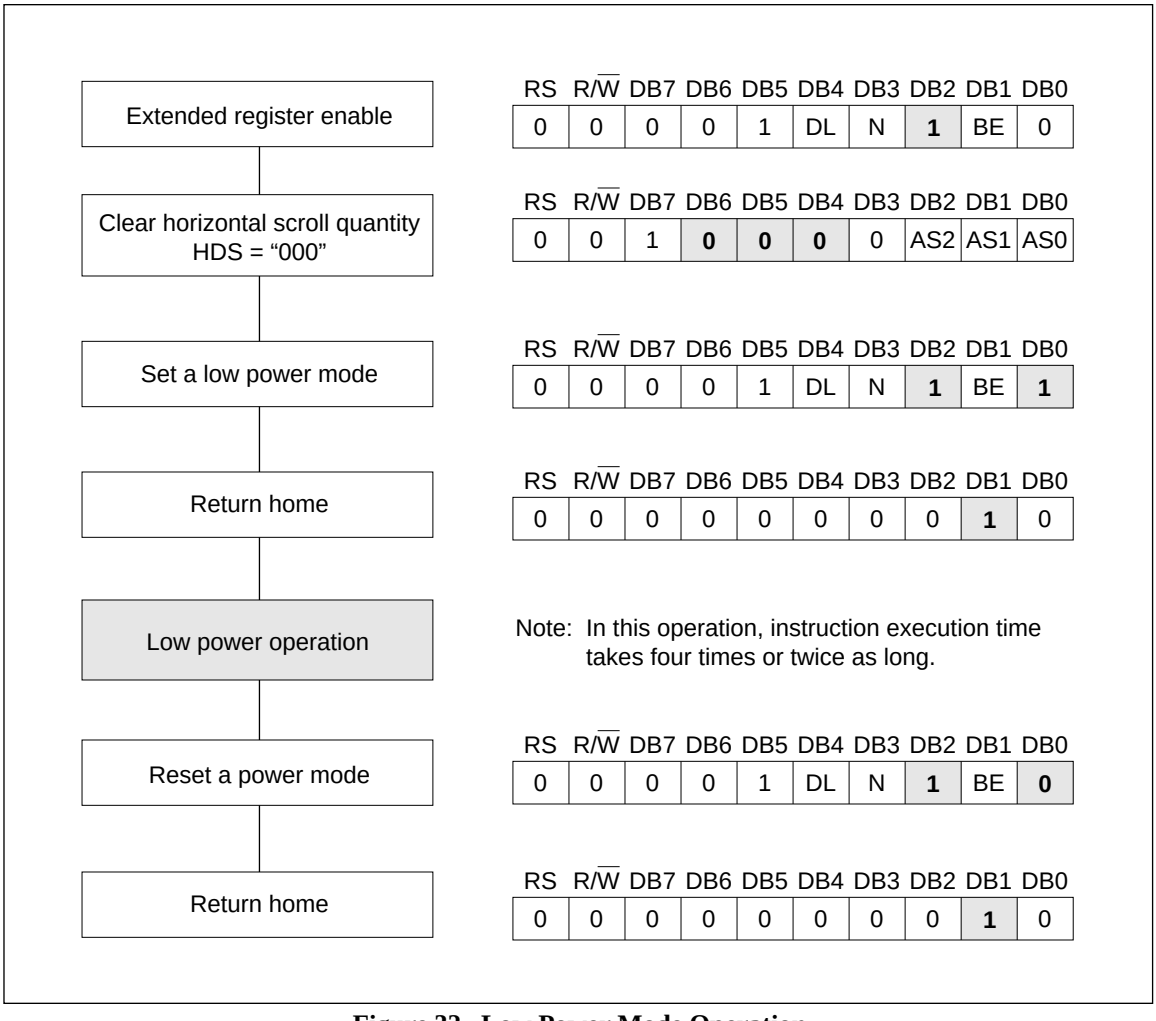


Figure 32 Low Power Mode Operation

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes*
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V_5	–0.3 to +15.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Notes: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

* Refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20°C to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	$0.2V_{CC}$	V		6
		–0.3	—	0.6			
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM) V_{LCD} = 4 V	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG) V_{LCD} = 4 V	13
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (D_0–D_7, RS, R/$\overline{W}$)	–Ip	5	50	120	µA	V_{CC} = 3 V V_{IN} = 0 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	13.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	13.0	V	V_{CC}–V_5, 1/6.7 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	V_{ci} = 4.5 V, I_0 = 0.25 mA, C = 1 µF, f_{OSC} = 270 kHz, T_a = 25°C	18, 19
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.7	—	V	V_{ci} = 2.7 V, I_0 = 0.25 mA, C = 1 µF, f_{OSC} = 270 kHz, T_a = 25°C	18, 19
Input voltage	V_{Ci}	2.0	—	5.0	V		18, 19, 20

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20°C to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ, V_{CC} = 5 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20°C to +75°C*3)

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 33
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Bus Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20°C to +75°C[*3])

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 33
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 34
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20°C to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	500	—	—	ns	Figure 35
	Low level	t_{CWL}	500	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	600		

Power Supply Conditions Using Internal Reset Circuit

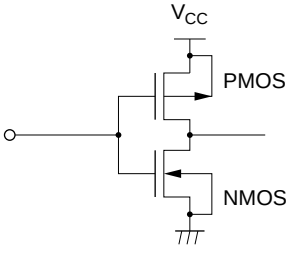
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 36
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

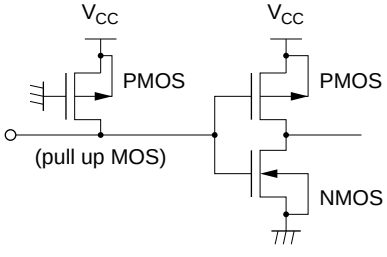
1. All voltage values are referred to GND = 0 V. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained. In addition, if the SEG37/CL1, SEG38/CL2, SEG39/D, and SEG40/M are used as extension driver interface signals (EXT = high), GND ≥ V5 must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

Input pin

Pin: E (MOS without pull-up)



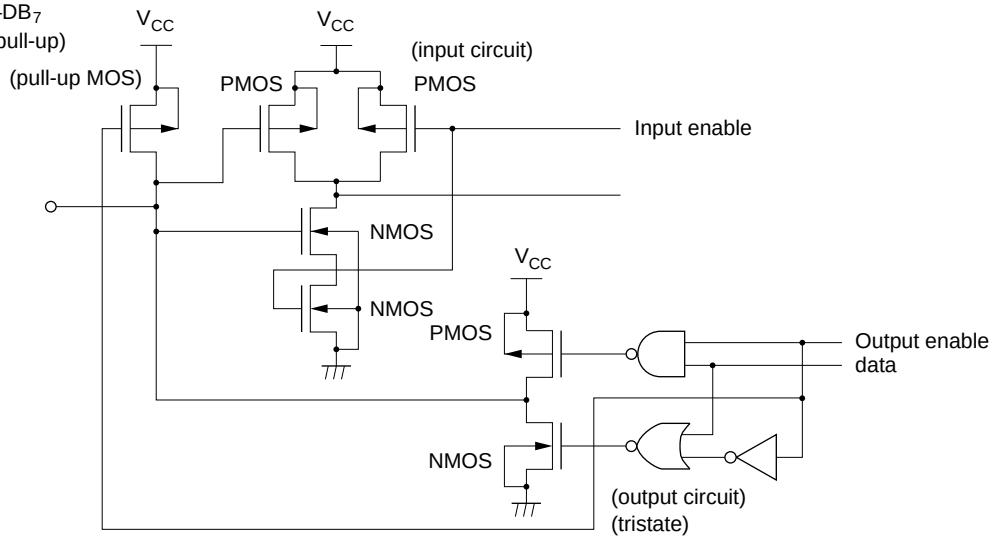
Pins: RS, R/$\overline{W}$ (MOS with pull-up)



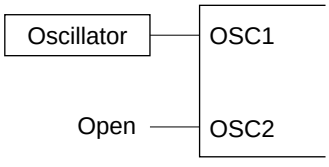
I/O pin

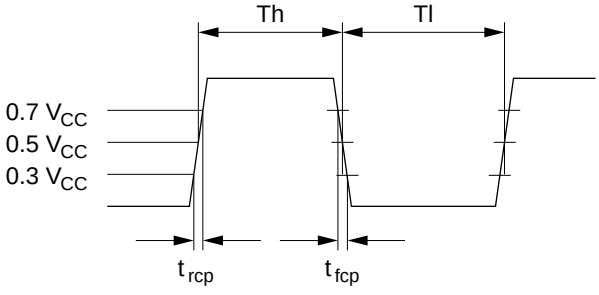
Pins: DB_0–DB_7

(MOS with pull-up)



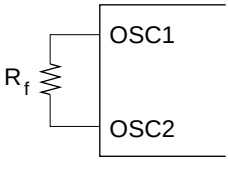
6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



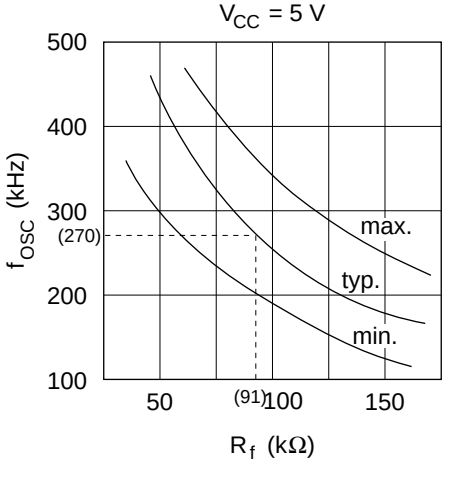


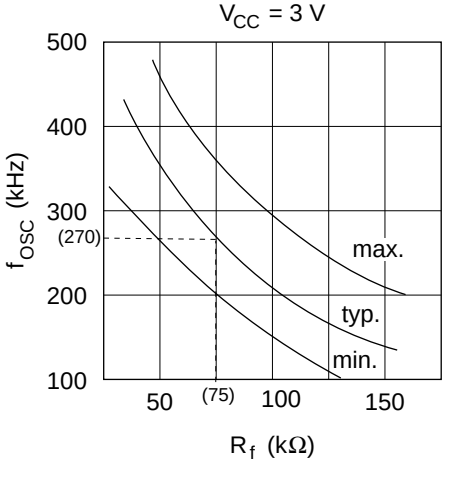
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



R_f: 75 kΩ ± 2% (when V_{CC} = 3 V to 4 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 4 V to 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

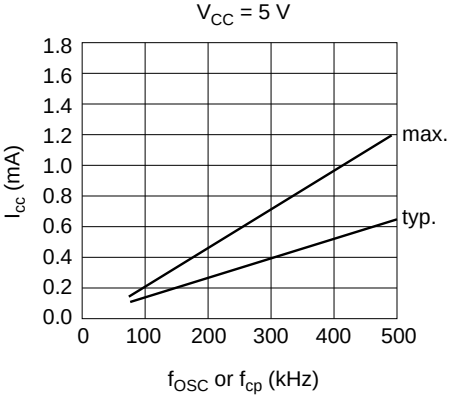


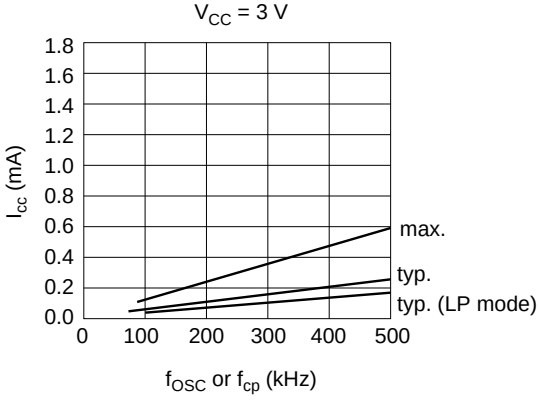


13. R_{COM} is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM1 to COM33).

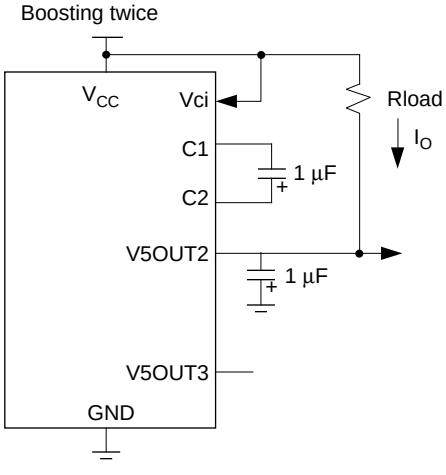
    R_{SEG} is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

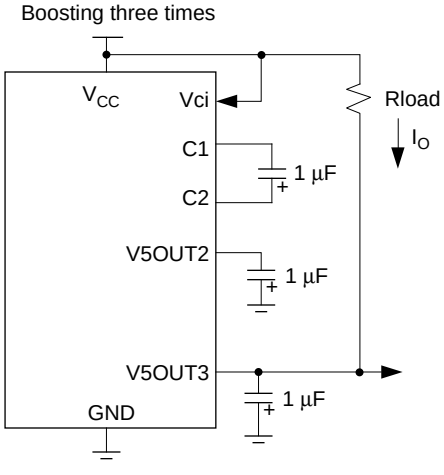
14. The following graphs show the relationship between operation frequency and current consumption.





15. Applies to the OSC1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.
17. The TEST pin must be fixed to the ground, and the EXT or V_{CC} pin must also be connected to the ground.
18. Booster characteristics test circuits are shown below.





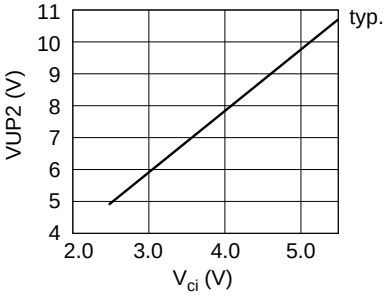
19. Reference data

The following graphs show the liquid crystal voltage booster characteristics.

VUP2 = V_{CC}–V5OUT2
VUP3 = V_{CC}–V5OUT3

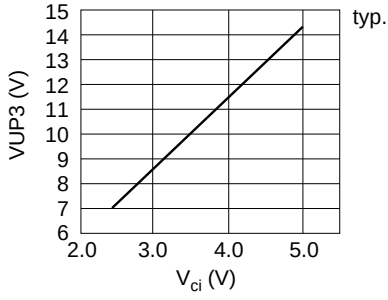
(1) VUP2, VUP3 vs V_{ci}

Boosting twice



Test condition: $V_{ci} = V_{CC}$, f_{cp} = 270 kHz
T_a = 25°C, Rload = 25 kΩ

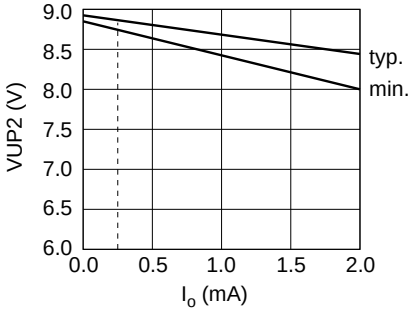
Boosting three times



Test condition: $V_{ci} = V_{CC}$, f_{cp} = 270 kHz
Ta = 25°C, Rload = 25 kΩ

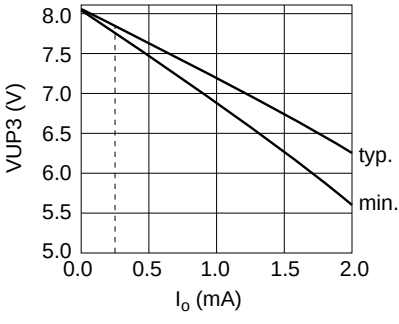
(2) VUP2, VUP3 vs I_o

Boosting twice



Test condition: $V_{ci} = V_{CC}$ = 4.5 V
R_f = 91 kΩ, T_a = 25°C

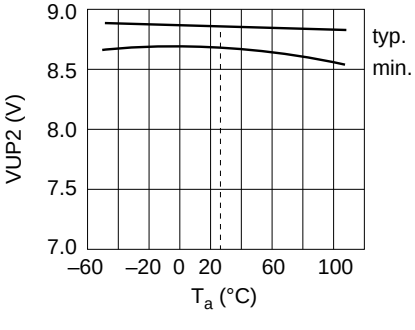
Boosting three times



Test condition: $V_{ci} = V_{CC}$ = 2.7 V
R_f = 75 kΩ, T_a = 25°C

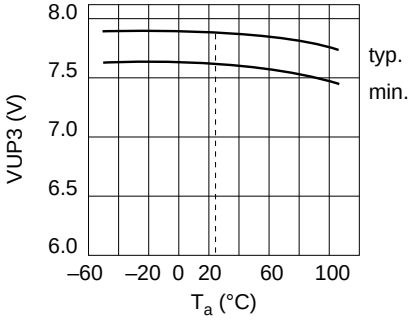
(3) VUP2, VUP3 vs T_a

Boosting twice



Test condition: $V_{ci} = V_{CC}$ = 4.5 V
R_f = 91 kΩ, I_o = 0.25 mA

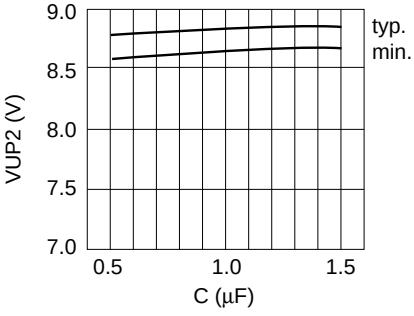
Boosting three times



Test condition: $V_{ci} = V_{CC}$ = 2.7 V
R_f = 75 kΩ, I_o = 0.25 mA

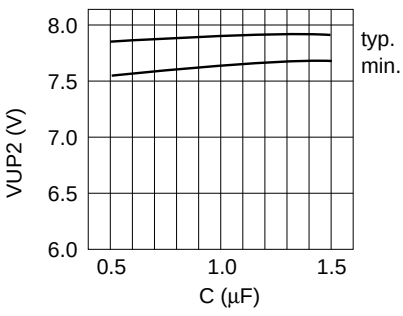
(4) VUP2, VUP3 vs Capacitance

Boosting twice



Test condition: $V_{ci} = V_{CC} = 4.5$ V
$R_f = 91$ kΩ, $I_o = 0.25$ mA

Boosting three times



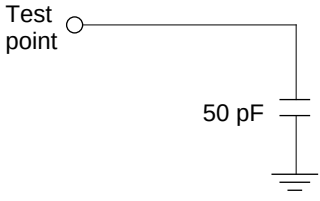
Test condition: $V_{ci} = V_{CC} = 2.7$ V
$R_f = 75$ kΩ, $I_o = 0.25$ mA

20. $V_{ci} \leq V_{CC}$ must be maintained.

Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB0–DB7



Segment extension signals: CL1, CL2, D, M

Timing Characteristics

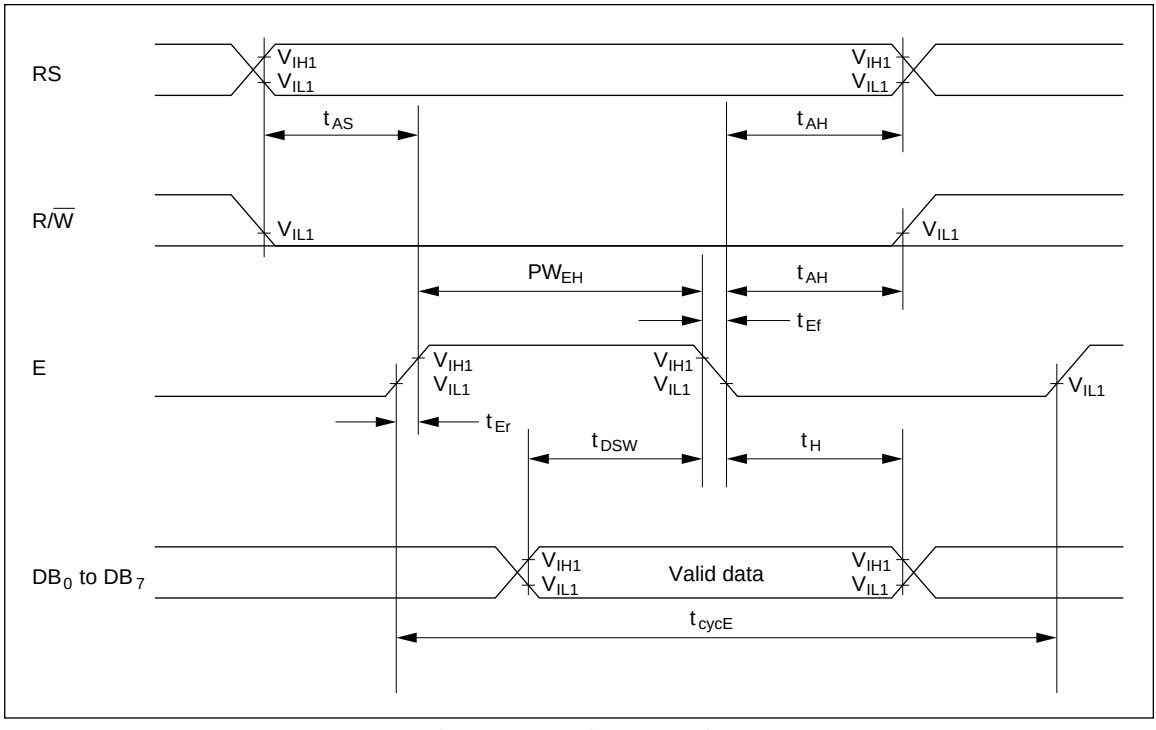
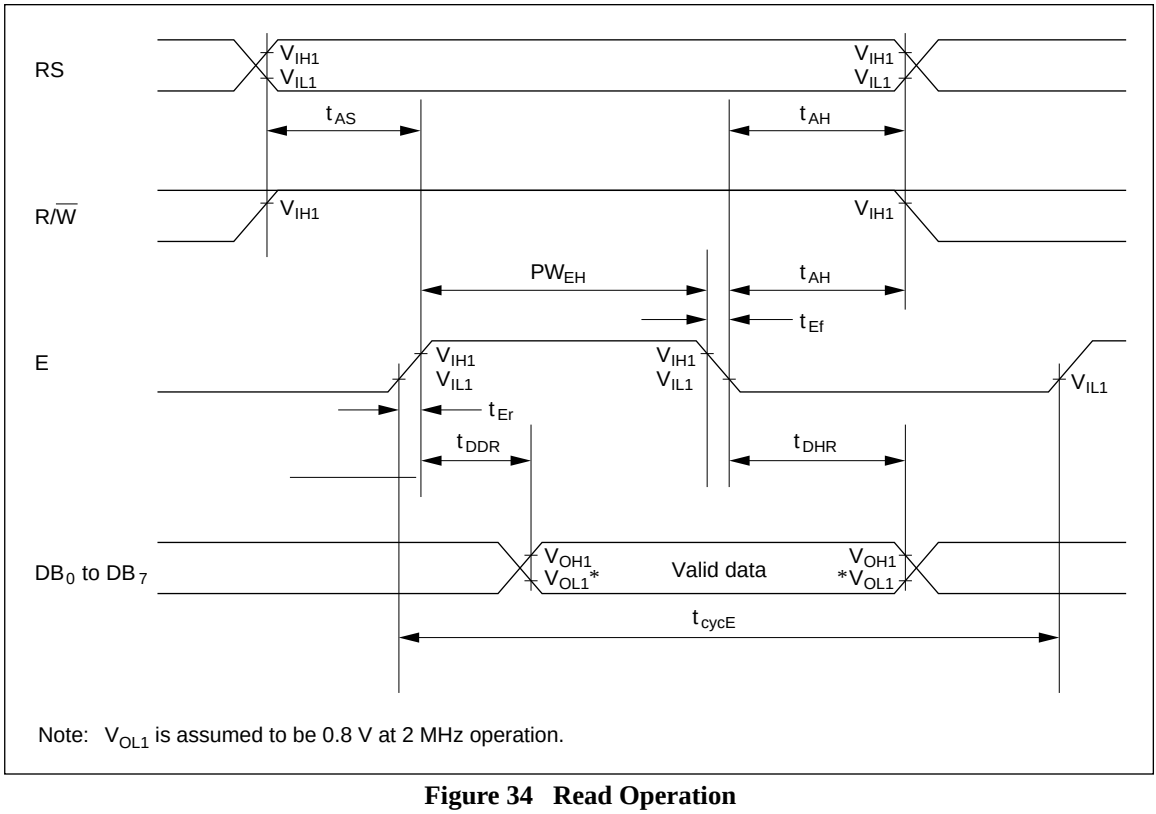


Figure 33 Write Operation



Note: V_{OL1} is assumed to be 0.8 V at 2 MHz operation.

Figure 34 Read Operation

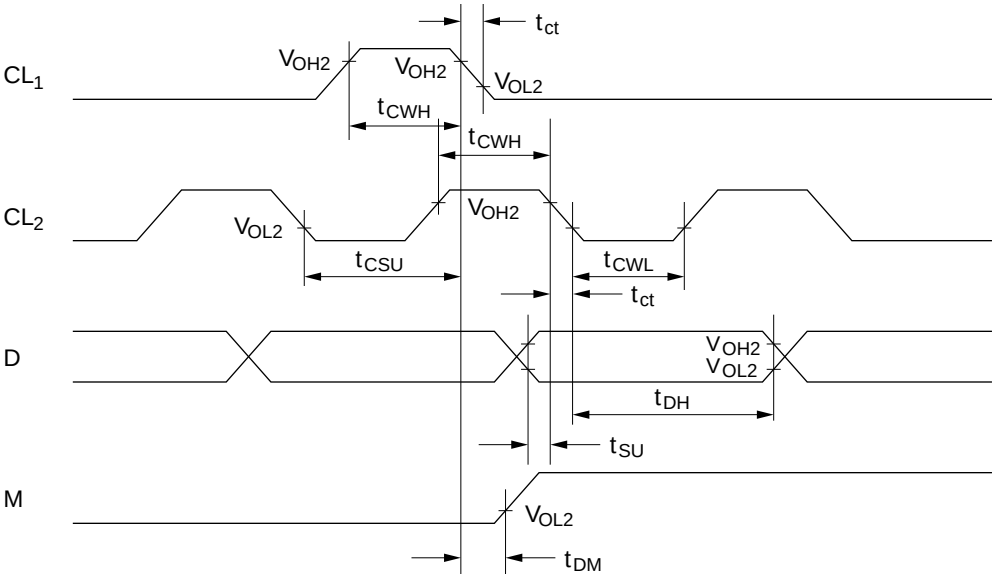
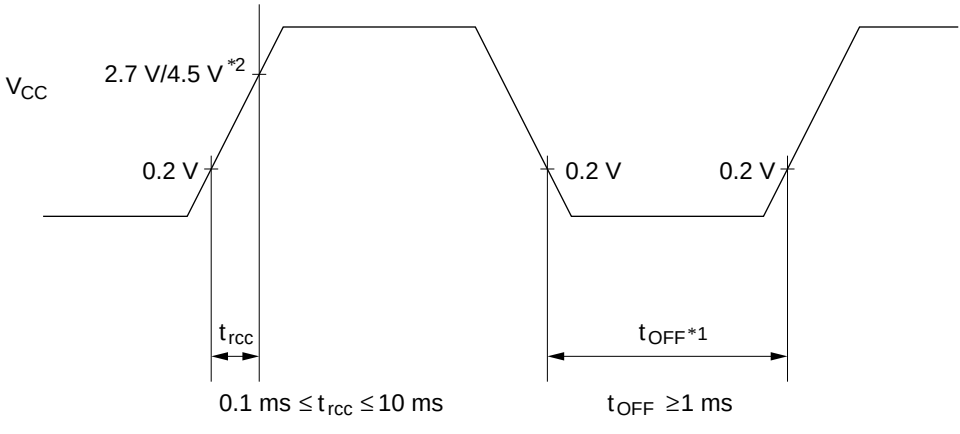


Figure 35 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for standard voltage operation, and at 2.7 V for low voltage operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 36 Power Supply Sequemce

HD66712 (LCD-II/F12)

(Dot-Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD66712 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, numbers, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a serial or a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimum system can be interfaced with this controller/driver.

A single HD66712 is capable of displaying a single 24-character line, two 24-character lines, or four 12-character lines.

The HD66712 software is upwardly compatible with the LCDII (HD44780) which allows the user to easily replace an LCD-II with an HD66712. In addition, the HD66712 is equipped with functions such as segment displays for icon marks, a 4-line display mode, and a horizontal smooth scroll, and thus supports various display forms. This achieves various display forms. The HD66712 character generator ROM is extended to generate 240 5 × 8 dot characters.

The low-voltage operation (2.7 V) of the HD66712, combined with a low-power mode, is suitable for any portable battery-driven product requiring low power consumption.

Features

- 5 × 8 dot matrix possible
- Clock-synchronized serial interface capability; can interface with 4- or 8-bit MPU
- Low-power operation support:
  - 2.7 to 5.5 V (low voltage)
  - Wide liquid-crystal voltage range: 3.0 to 13.0 V max.
- Booster for liquid crystal voltage
  - Two/three times (13 V max.)
- High-speed MPU bus interface
  (2MHz at 5-V operation)
- Extension driver interface
- Character display and independent 60-icon mark display possible
- Horizontal smooth scroll by 6-dot font width display possible
- 80 × 8-bit display RAM (80 characters max.)
- 9,600-bit character generator ROM
  - 240 characters (5 × 8 dot)
- 64 × 8-bit character generator RAM
  - 8 characters (5 × 8 dot)
- 16 × 8-bit segment icon mark
  — 96-segment icon mark
- 34-common × 60-segment liquid crystal display driver
- Programmable duty cycle
  (See list 1)
- Software upwardly compatible with HD44780
- Wide range of instruction functions:
  - Functions compatible with LCD-II: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
  - Additional functions: Icon mark control, 4-line display, horizontal smooth scroll, 6-dot character width control, white-black inverting blinking cursor
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)

Hitachi semiconductor

- Internal oscillator with an external resistor
- Low power consumption
- QFP 1420-128 pin, TCP-128 pin, bare-chip

List 1 Programmable Duty Cycles

Number of Lines	Duty Ratio	5-Dot Font Width			
		Single-Chip Operation		With Extension Driver	
		Displayed Characters	Icons	Displayed Characters	Icons
1	1/17	One 24-character line	60	One 52-character line	80
2	1/33	Two 24-character lines	60	Two 32-character lines	80
4	1/33	Four 24-character lines	60	Four 20-character lines	80

Number of Lines	Duty Ratio	6-Dot Font Width			
		Single-Chip Operation		With Extension Driver	
		Displayed Characters	Icons	Displayed Characters	Icons
1	1/17	One 20-character line	60	One 50-character line	96
2	1/33	Two 20-character lines	60	Two 30-character lines	96
4	1/33	Four 10-character lines	60	Four 20-character lines	96

Ordering Information

Type No.	Package	CGROM
HD66712A00FS	QFP1420-128 (FP-128)	Japanese standard
HD66712A00TA0	Standard TCP-128	
HD66712A00TB0*	Folding TCP-128	
HCD66712A00	Chip	
HCD66712A01	Chip	Communication
HD66712A02FS	QFP1420-128 (FP-128)	European font
HCD66712A02	Chip	
HCD66712A03	Chip	Japanese + European font
HD66712BxxFS	QFP1420-128 (FP-128)	Custom font
HCD66712Bxx	Chip	

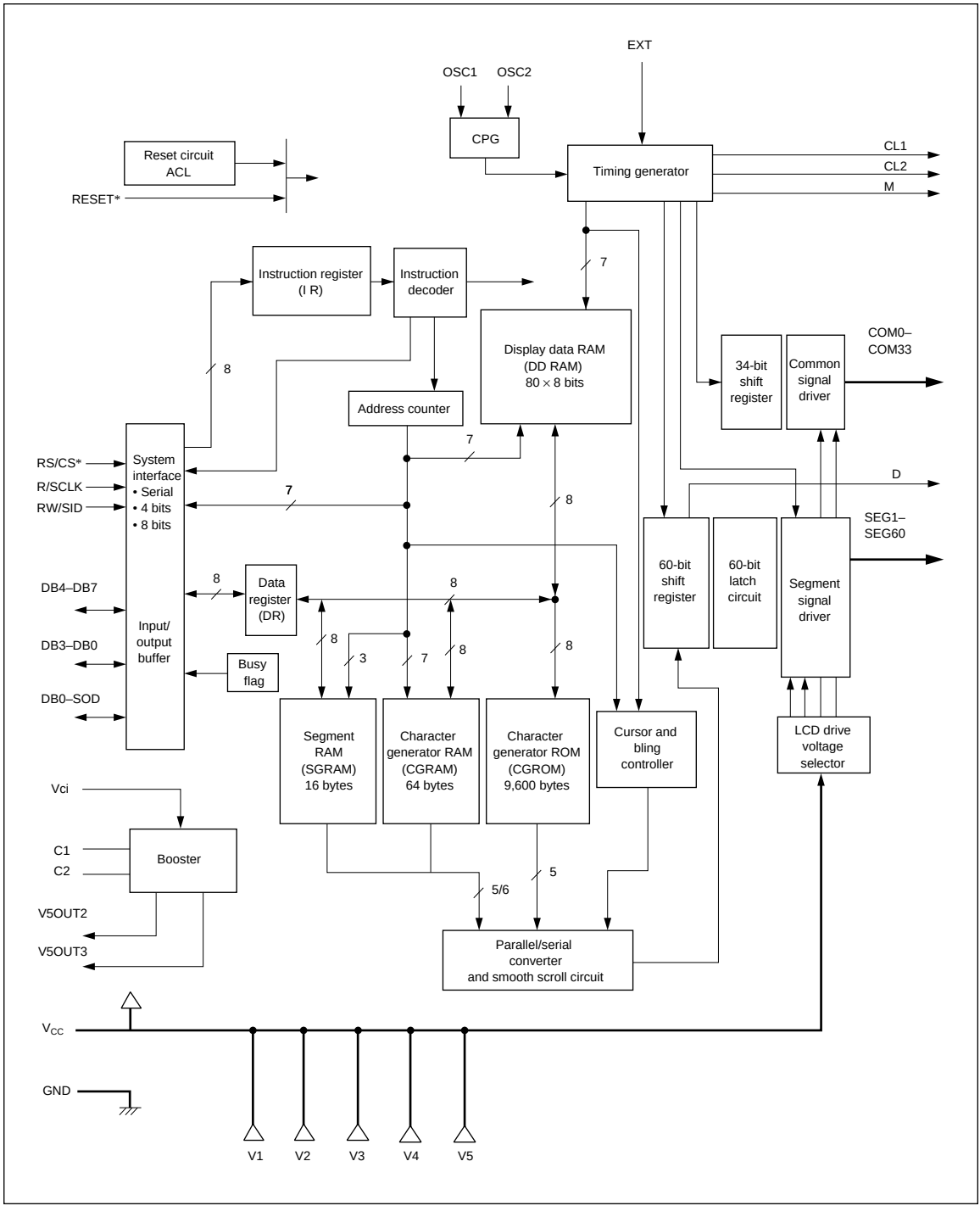
Note: Bxx = ROM code No.
* Under development

LCD-II Family Comparison

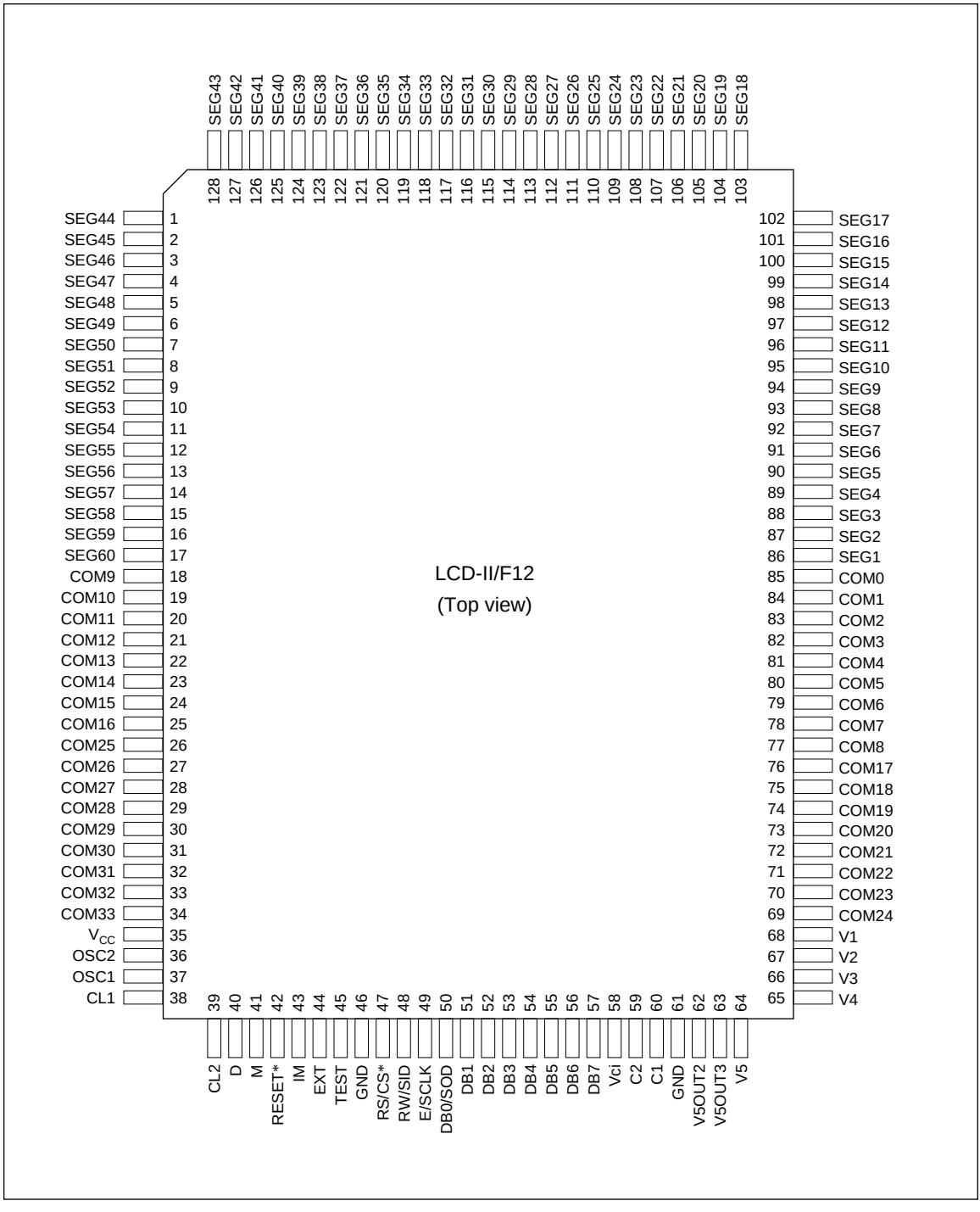
Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Power supply voltage	2.7 V to 5.5 V	5 V ±10 % (standard) 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltage	3.0 V to 11 V	3.0 V to 8.3 V	3.0 V to 13.0 V	3.0 V to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines
Segment display	None	None	40 segments	60 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33	1/17 and 1/33
CGROM	9,920 bits (208 5 × 8 dot characters and 32 5 × 10 dot characters)	7,200 bits (160 5 × 7 dot characters and 32 5 × 10 dot characters)	9,600 bits (240 5 × 8 dot characters)	9,600 bits (240 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes	16 bytes
Segment signals	40	100	40	60
Common signals	16	16	33	34
Liquid crystal drive waveform	A	B	B	B
Bleeder resistor for LCD power supply	External (adjustable)	External (adjustable)	External (adjustable)	External (adjustable)
Clock source	External resistor or external clock	External resistor or external clock	External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycle; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (70 to 130 Hz for 1/8 and 1/16 duty cycle; 51 to 95 Hz for 1/11 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)
R_f resistance	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	68 kΩ: 5-V operation; 56 kΩ: (3-V operation)	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	91 kΩ: 5-V operation; 75 kΩ: 3-V operation

Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Liquid crystal voltage booster circuit	None	None	2–3 times step-up circuit	2–3 times step-up circuit
Extension driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal
Reset function	Power on automatic reset	Power on automatic reset	Power on automatic reset	Power on automatic reset or Reset input
Instructions	LCD-II (HD44780)	Fully compatible with the LCD-II	Upper compatible with the LCD-II	Upper compatible with the LCD-II
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
Low power mode	None	None	Available	Available
Horizontal scroll	Character unit	Character unit	Dot unit	Dot unit
Bus interface	4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial; 4 bits/8 bits
CPU bus timing	2 MHz: 5-V operation; 1 MHz: 3-V operation	1 MHz	2 MHz: 5-V operation; 1 MHz: 3-V operation	2 MHz: 5-V operation; 1 MHz: 3-V operation
Package	QFP-1420-80 80-pin bare chip	LQFP-2020–144 144-pin bare chip	QFP-1420-100 TQFP-1414-100 100-pin bare chip	QFP-1420-128 TCP-128 128-pin bare chip

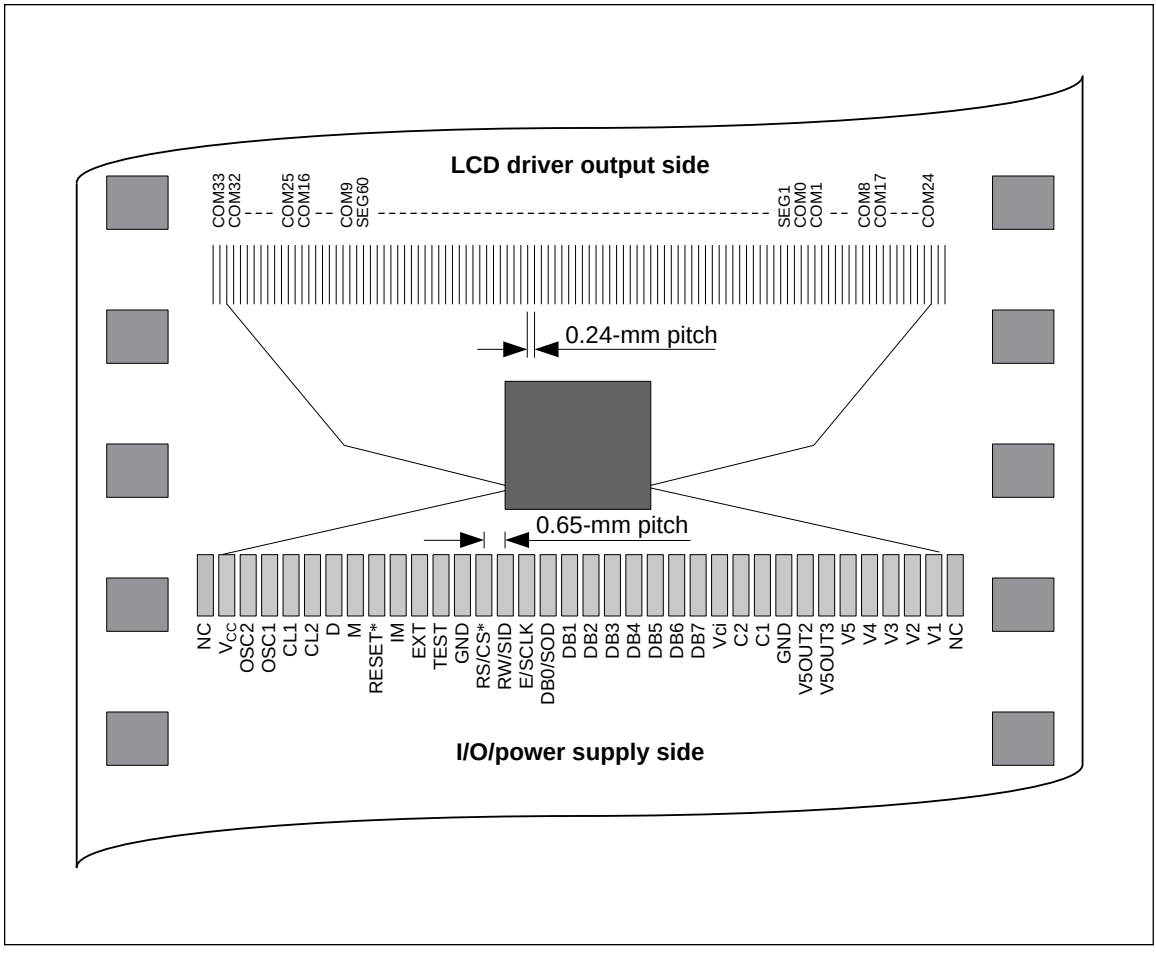
HD66712 Block Diagram



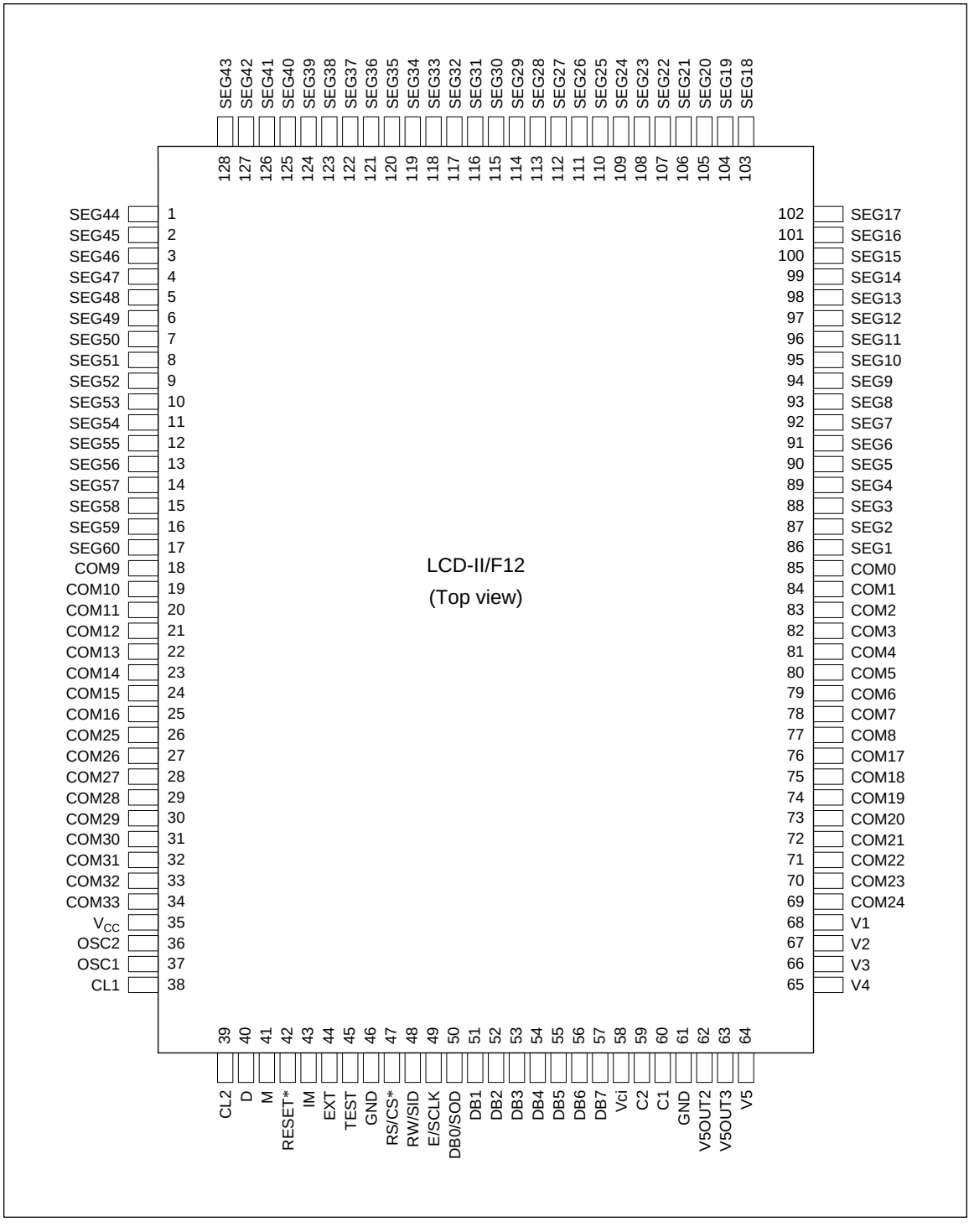
HD66712 Pin Arrangement



TCP Dimensions



HD66712 Pad Arrangement



Pin Functions

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
IM	1	I	—	Selects interface mode with the MPU; Low: Serial mode High: 4-bit/8-bit bus mode (Bus width is specified by instruction.)
RS/CS*	1	I	MPU	Selects registers during bus mode: Low: Instruction register (write); Busy flag, address counter (read) High: Data register (write/read) Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
RW/SID	1	I	MPU	Selects read/write during bus mode; Low: Write High: Read Inputs serial data during serial mode.
E/SCLK	1	I	MPU	Starts data read/write during bus mode; Inputs (Receives) serial clock during serial mode.
DB_4 to DB_7	4	I/O	MPU	Four high-order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66712. DB_7 can be used as a busy flag. Open these pins during serial mode since these signals are not used.
DB_1 to DB_3	3	I/O	MPU	Three low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66712. Open these pins during 4-bit operation or serial mode since they are not used.
DB0/ SOD	1	I/O /O	MPU	The lowest bidirectional data bit (DB0) during 8-bit bus mode. Open these pins during 4-bit mode since they are not used. Outputs (transfers) serial data during serial mode. Open this pin if reading (transfer) is not performed.
COM_0 to COM_{33}	34	O	LCD	Common signals; those that are not used become non-selected waveforms. At 1/17 duty rate, COM_1 to COM_{16} are used for character display, COM_0 and COM_{17} for icon display, and COM_{18} to COM_{33} become non-selected waveforms. At 1/33 duty rate, COM_1 to COM_{32} are used for character display, and COM_0 and COM_{33} for icon display. Because two COM signals output the same level simultaneously, apply them according to the wiring pattern of the display device.
SEG_1 to SEG_{60}	60	O	LCD	Segment output signals

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
CL1	1	O	Extension driver	When EXT = high, outputs the extension driver latch pulse.
CL2	1	O	Extension driver	When EXT = high, outputs the extension driver shift clock.
D	1	O	Extension driver	When EXT = high, outputs extension driver data; data from the 61st dot on is output.
M	1	O	Extension driver	When EXT = high, outputs the extension driver AC signal.
EXT	1	I	—	When EXT = high, outputs the extension driver control signal. When EXT = low, the signal becomes tristate and can suppress consumption current.
V_1 to V_5	5	—	Power supply	Power supply for LCD drive $V_{CC} - V_5$ = 13 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +2.7 V to +5.5 V, GND: 0 V
OSC_1/OSC_2	2	—	Oscillation resistor clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC_1.
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Vci is reference voltage and power supply for the booster. Vci = 2.0 V to 5.0 V ≤ Vci
V_5OUT_2	1	O	V_5 pin/ booster capacitance	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, the same capacitance as that of C1–C2 should be connected here.
V_5OUT_3	1	O	V_5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitance	External capacitance should be connected here when using the booster.
RESET*	1	I	—	Reset pin. Initialized to “low.”
TEST	1	I	—	Test pin. Should be wired to ground.

Function Description

System Interface

The HD66712 has three types of system interfaces: synchronized serial, 4-bit bus, and 8-bit bus. The serial interface is selected by the IM-pin, and the 4/8-bit bus interface is selected by the DL bit in the instruction register.

The HD66712 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEGRAM). The MPU can only write to IR, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEGRAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEGRAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEGRAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEGRAM at the next address is sent to the DR for the next read from the MPU.

These two registers can be selected by the registor selector (RS) signal in the 4/8 bit bus interface, and by the RS bit in start byte data in synchronized serial interface (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66712 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output from DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEGRAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Resistor Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM.

The DD RAM address (A_{DD}) is set in the address counter (AC) as a hexadecimal number, as shown in figure 1.

The relationship between DD RAM addresses and positions on the liquid crystal display is described and shown on the following pages for a variety of cases.

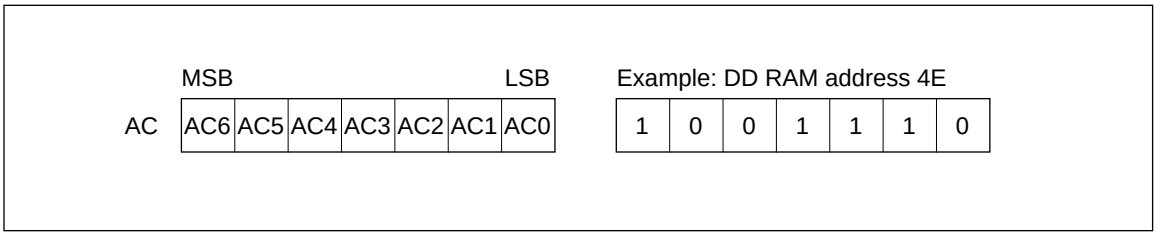


Figure 1 DD RAM Address

- 1-line display (N = 0, and NW = 0)

  — Case 1: When there are fewer than 80 display characters, the display begins at the beginning of DD RAM. For example, when 24 5-dot font-width characters are displayed using one HD66712, the display is generated as shown in figure 2.

  When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

  When 20 6-dot font-width characters are displayed using one HD66712, the display is generated as shown in figure 3. Note that COM9 to COM16 begins at address (0A)H in this case 20 characters are displayed.

  When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

  — Case 2: Figure 4 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to display 24 6-dot font-width characters. In this case, COM9 to COM16 begins at (0A)H.

  When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

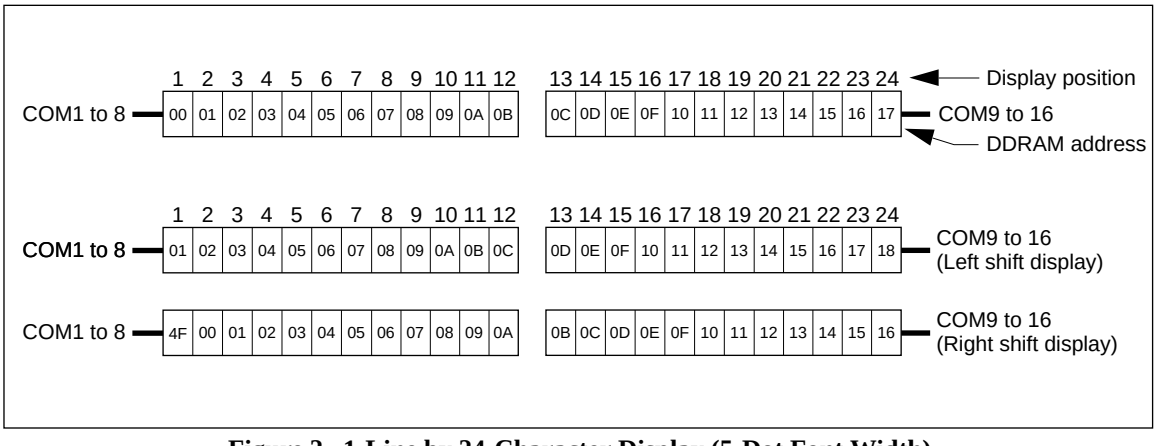


Figure 2 1-Line by 24-Character Display (5-Dot Font Width)

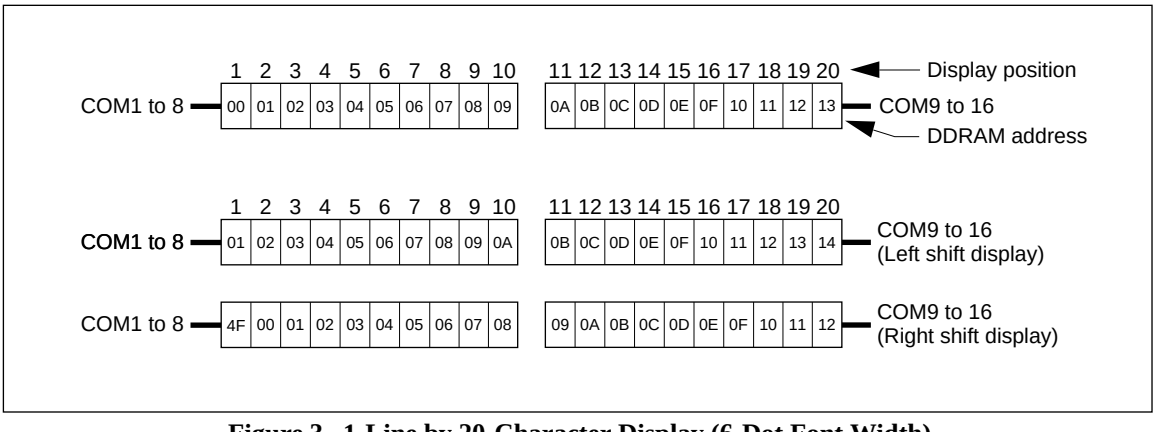


Figure 3 1-Line by 20-Character Display (6-Dot Font Width)

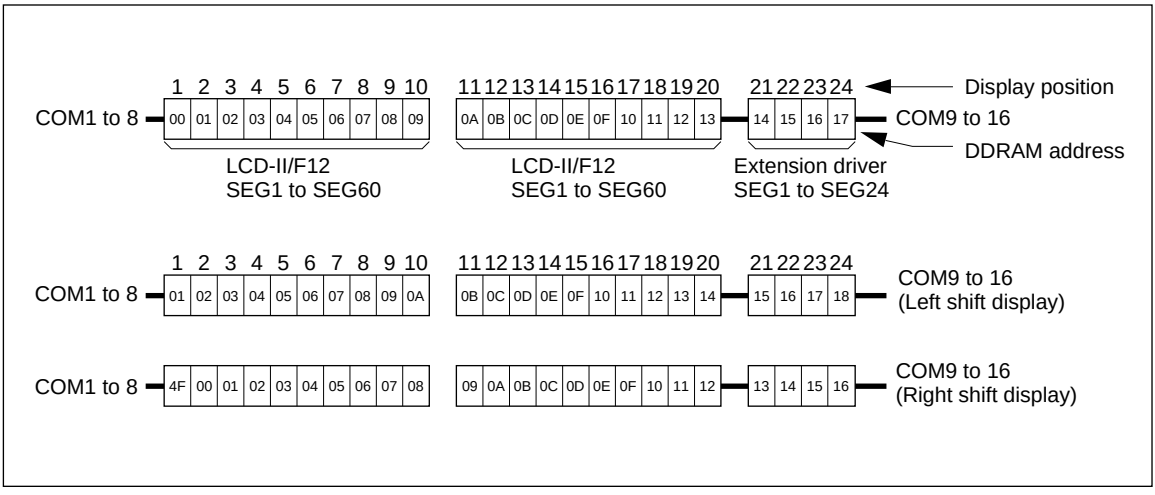


Figure 4 1-Line by 24-Character Display (6-Dot Font Width)

- 2-line display (N = 1, and NW = 0)

  — Case 1: The first line is displayed from COM1 to COM16, and the second line is displayed from COM17 to COM32. Note that the last address of the first line and the first address of the second line are not consecutive. Figure 5 shows an example where a 5-dot font-width 24 × 2-line display is performed using one HD66712. Here, COM9 to COM16 begins at (0C)H, and COM25 to COM32 at (4C)H. When a display shift is performed, the DD RAM addresses shift as shown. Figure 6 shows an example where a 6-dot font-width 20 × 2-line display is performed using one HD66712. COM9 to COM16 begins at (0A)H, and COM25 to COM32 at (4A)H.

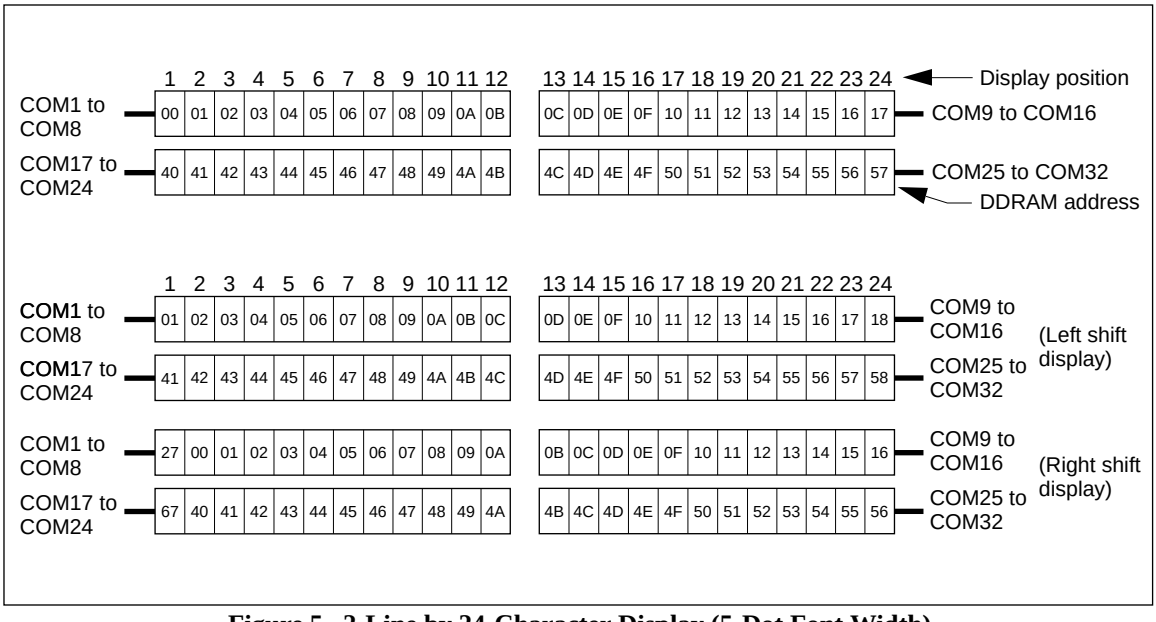


Figure 5 2-Line by 24-Character Display (5-Dot Font Width)

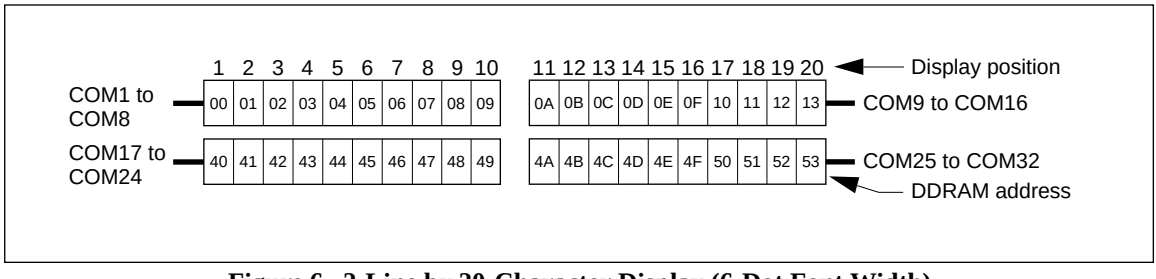


Figure 6 2-Line by 20-Character Display (6-Dot Font Width)

— Case 2: Figure 7 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to extend the number of display characters to 32 5-dot font-width characters.

In this case, COM9 to COM16 begins at (0C)H, and COM25 to COM32 at (4C)H.

When a display shift is performed, the DD RAM addresses shift as shown.

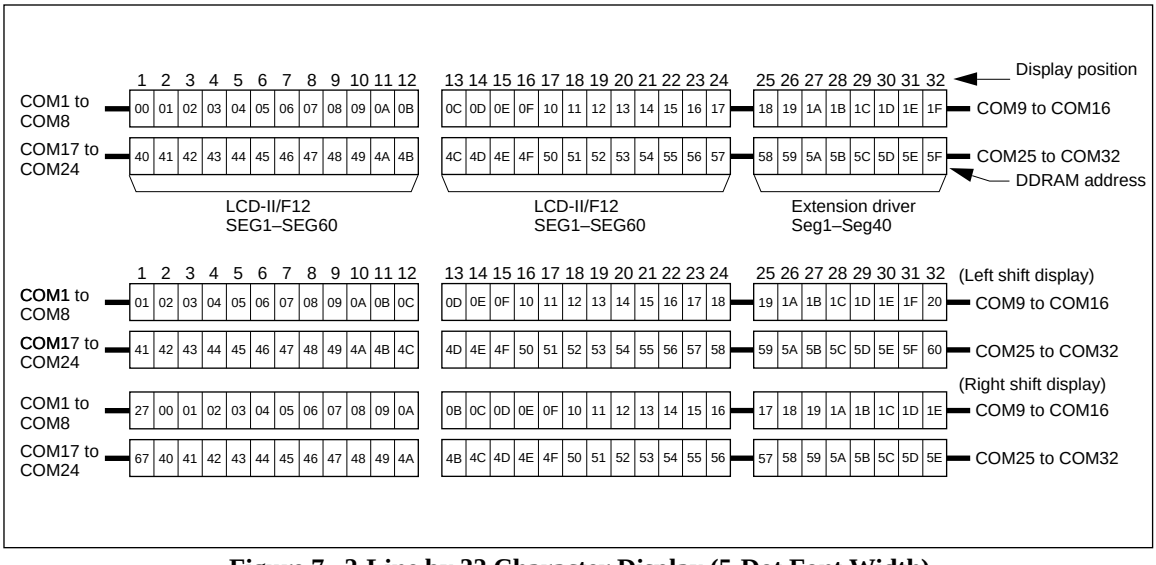


Figure 7 2-Line by 32 Character Display (5-Dot Font Width)

- 4-line display (NW = 1)

  — Case 1: The first line is displayed from COM1 to COM8, the second line is displayed from COM9 to COM16, the third line is displayed from COM17 to COM24, and the fourth line is displayed from COM25 to COM32.

Note that the DD RAM addresses of each line are not consecutive. Figure 8 shows an example where a 12 × 4-line display is performed using one HD66712.

When a display shift is performed, the DD RAM addresses shift as shown.

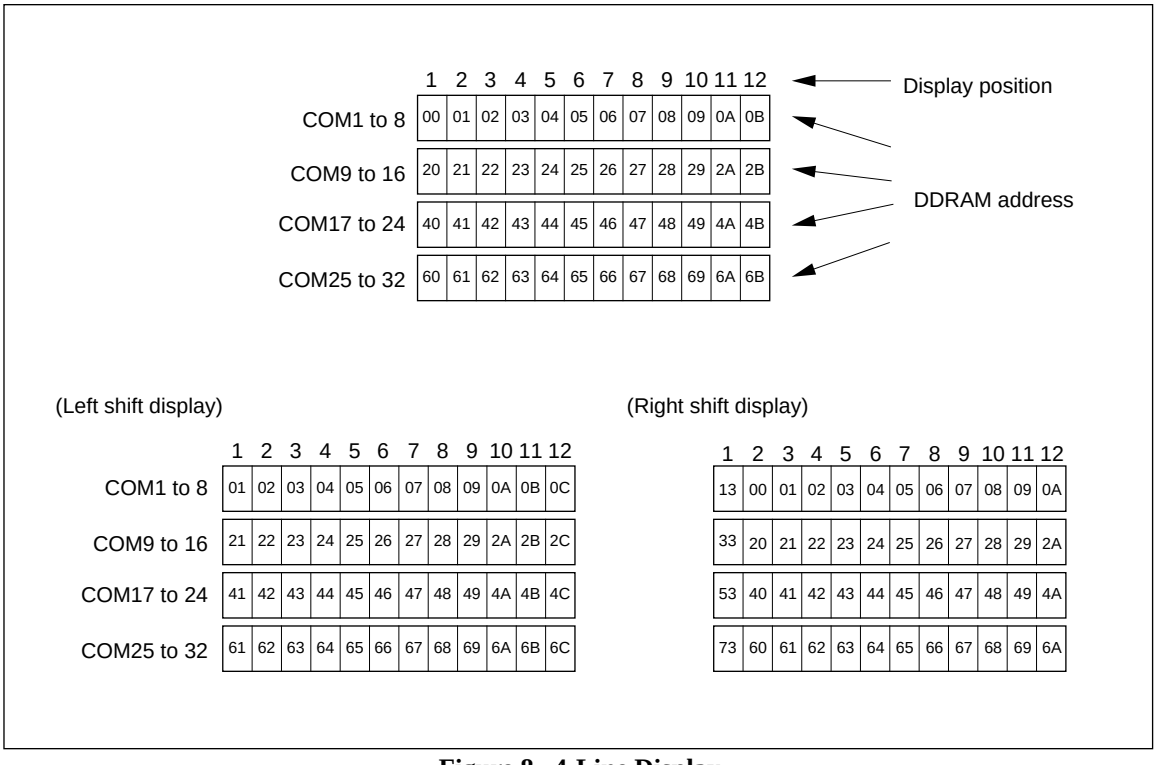


Figure 8 4-Line Display

— Case 2: Figure 9 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to extend the number of display characters.

When a display shift is performed, the DD RAM addresses shift as shown.

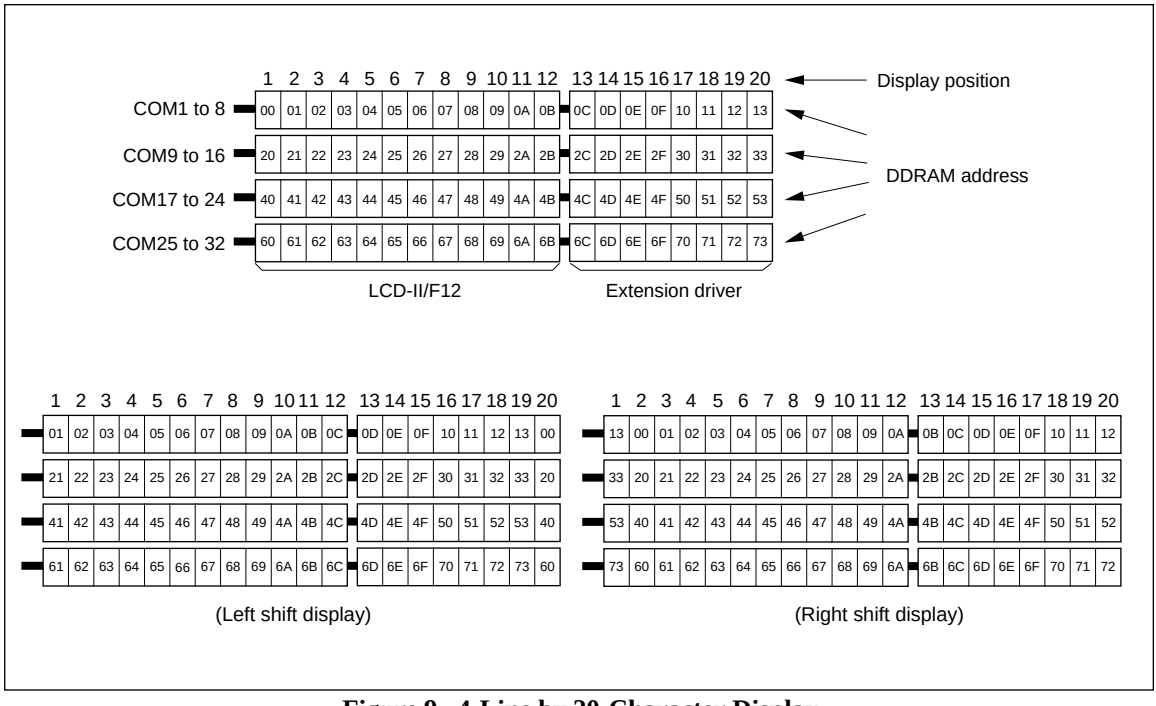


Figure 9 4-Line by 20-Character Display

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3 to 6). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM (see "Modifying Character Patterns.")

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of table 3 to 6 to show the character patterns stored in CG RAM.

See table 7 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to enable control of segments such as an icon and a mark by the user program.

For a 1-line display, SEGRAM is read from the COM0 and the COM17 output, and for 2- or 4-line displays, it is read from the COM0 and the COM33 output, to perform 60-segment display (80-segment display when using the extension driver).

As shown in table 8, bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

SEGRAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 34 common signal drivers and 60 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Character pattern data is sent serially through a 60-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66712 drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

For example (figure 10), when the address counter is (08)H, a cursor is displayed at a position corresponding to DDRAM address (08)H.

Scroll Control Circuit

The scroll control circuit is used to perform a smooth-scroll in the unit of dot. When the number of characters to be displayed is greater than that possible at one time on the liquid crystal module, this horizontal smooth scroll can be used to display all characters.

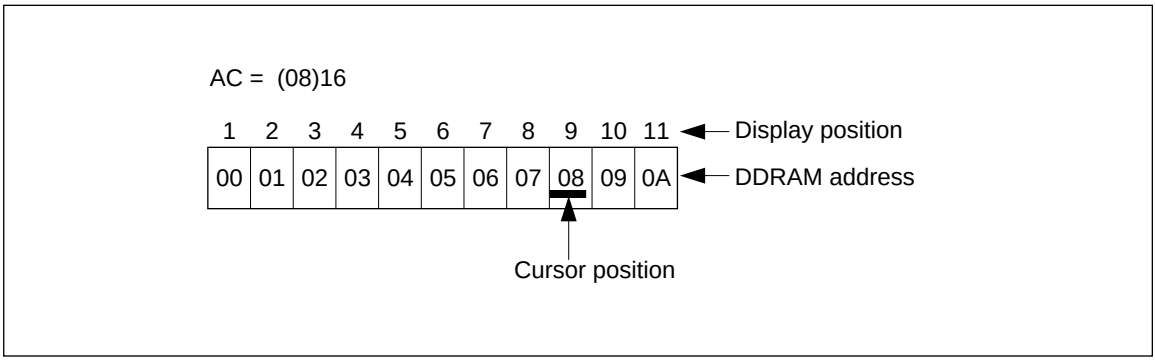


Figure 10 Cursor/Blink Display Example

Table 3 Relationship between Character Codes and Character Patterns (ROM Code: A00)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 4 Relationship between Character Codes and Character Pattern (ROM Code: A01)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 5 Relationship between Character Codes and Character Patterns (ROM Code: A02)

Note: The character codes of the characters enclosed in the bold frame are the same as those of the first edition of the ISO8859 and the character code compatible.

Table 6 Relationship between Character Codes and Character Pattern (ROM Code: A03)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 7 Example of Relationships between Character Code (DDRAM) and Character Pattern(CGRAM Data)

a) When character pattern is 5 × 8 dots

Character code (DDRAM data)								CGRAM address						CGRAM data (MSB → LSB)								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	Character pattern (1)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern (8)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	

a) When character pattern is 6 × 8 dots

Character code (DDRAM data)								CGRAM address						CGRAM data (MSB → LSB)								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in the figure above. Characters of 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters of 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected.
   Bit 3 of the character code is invalid (*). Therefore, for example, the character codes (00)H and (08)H correspond to the same CGRAM address.
5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CGRAM.
   When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display.
   When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

* Indicates no effect.

Table 8 Relationship between SEGRAM Addresses and Display Patterns

SEGRAM address				SEGRAM data															
				a) 5-dot font width								b) 6-dot font width							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	*	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	*	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	*	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	*	S56	S7	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	*	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	*	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	*	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	*	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96
				Blinking control			Pattern on/off					Blinking control			Pattern on/off				

Notes: 1. Data set to SEGRAM is output when COM0 and COM17 are selected, as for a 1-line display, and output when COM0 and COM33 are selected, as for a 2-line or a 4-line display. COM0 and COM17 for a 1-line display and COM0 and COM33 for a 2-line or a 4-line display are the same signals.

2. S1 to S96 are pin numbers of the segment output driver. S1 is positioned to the left of the display. When the LCD-II/F12 is used by one chip, segments from S1 to S60 are displayed. An extension driver displays the segments after S61.
3. After S80 output at 5-dot font and S96 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on.off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEGRAM.

   When bit 7 is 1, only a bit set to “1” of the lower six bits is blinked on the display.

   When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the SEGRAM data correspond to display selection, and zeros to non-selection.

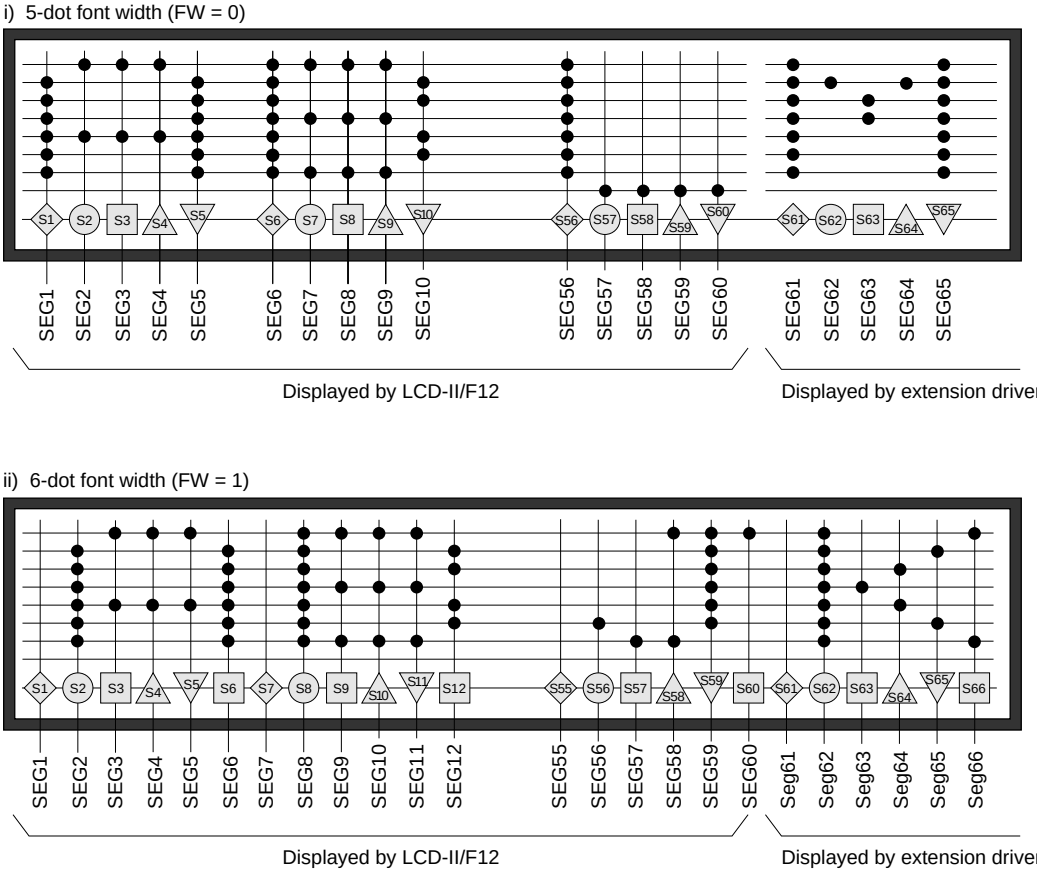


Figure 11 Correspondence between SEGRAM and Segment Display

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in figure 12:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.

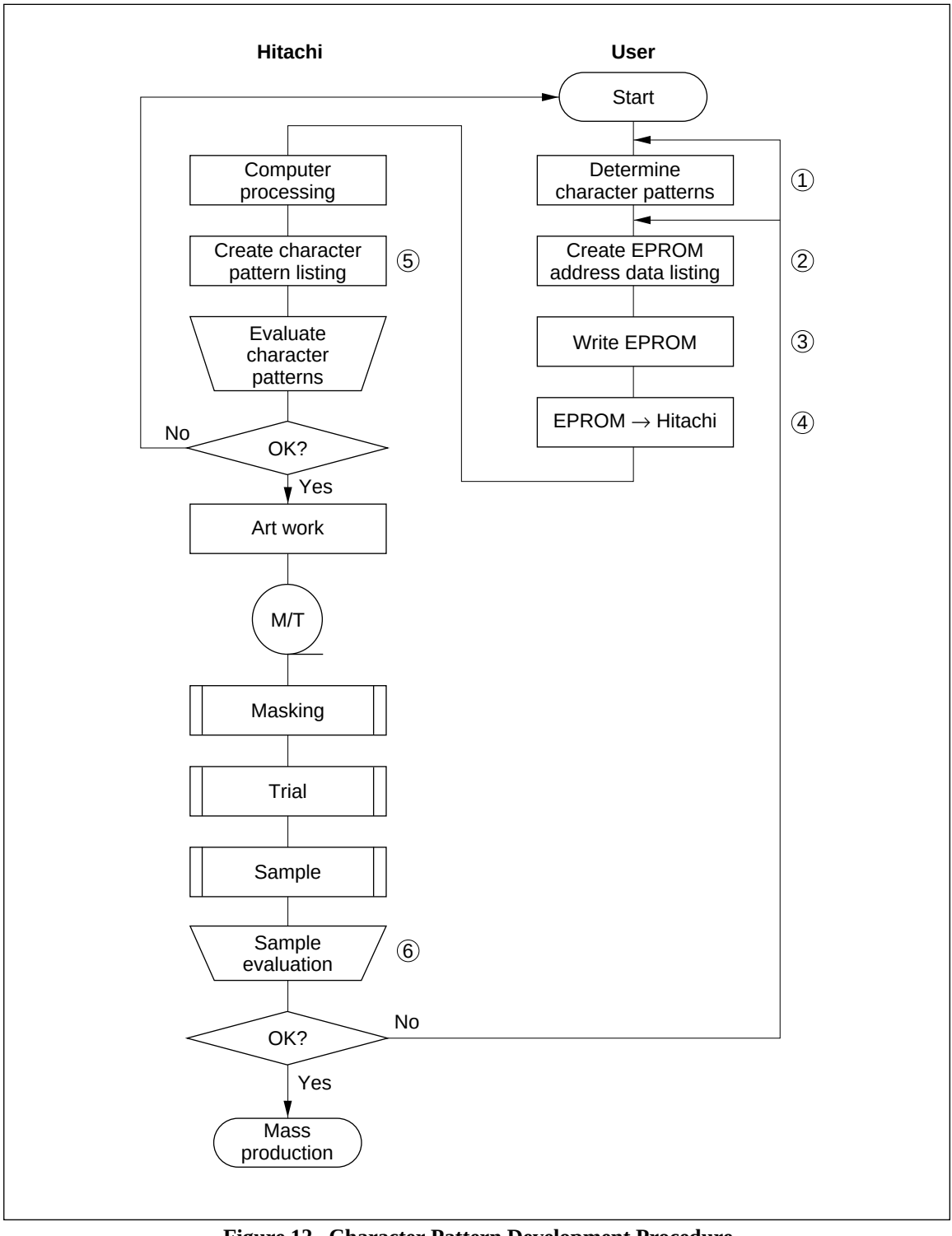


Figure 12 Character Pattern Development Procedure

Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

- Programming to EPROM

  The HD66712 character generator ROM can generate 240 5 × 8 dot character patterns. Table 9 shows correspondence between the EPROM address data and the character pattern.

Handling Unused Character Patterns

1. EPROM data outside the character pattern area: This is ignored by the character generator ROM for display operation so any data is acceptable.
2. EPROM data in CG RAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66712 EPROM: According to the user application, these are handled in either of two ways:
   a When unused character patterns are not programmed: If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   b When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 9 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 Dots)

EPROM Address												Data				
												MSB				LSB
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0

Character code “0” Line position

Notes:
1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify the line position of the character pattern. EPROM address A3 should be set to “0.”
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Areas which are lit (indicated by shading) are stored as “1,” and unlit areas as “0.”
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits 0_7 to 0_5 are invalid. 0 should be written in all bits.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66712 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the V_{CC} rises to 2.7 V.

1. Display clear:
   (20)H to all DDRAM

2. Set functions:
   DL = 1: 8-bit interface data
   N = 1: 2-line display
   RE = 0: Extension register write disable
   BE = 0: CGRAM/SEGRAM blink off
   LP = 0: Not in low power mode

3. Control display on/off:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blinking off

4. Set entry mode:
   I/D = 1: Increment by 1
   S = 0: No shift

5. Set extension function:
   FW = 0: 5-dot character width
   B/W = 0: Normal cursor (eighth line)
   NW = 0: 1- or 2-line display (depending on N)

6. Enable scroll:
   HSE = 0000: Scroll unable

7. Set scroll amount:
   HDS = 000000: Not scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66712.

Initializing by Hardware Reset Input

The LCD-II/F12 also has a reset input pin: RESET*. If this pin is made low during operation, an internal reset and initialization is performed. This pin is ignored, however, during the internal reset period at power-on.

Interfacing to the MPU

The HD66712 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66712 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

- When the IM pin is low, the HD66712 uses a serial interface. See “Transferring Serial Data.”

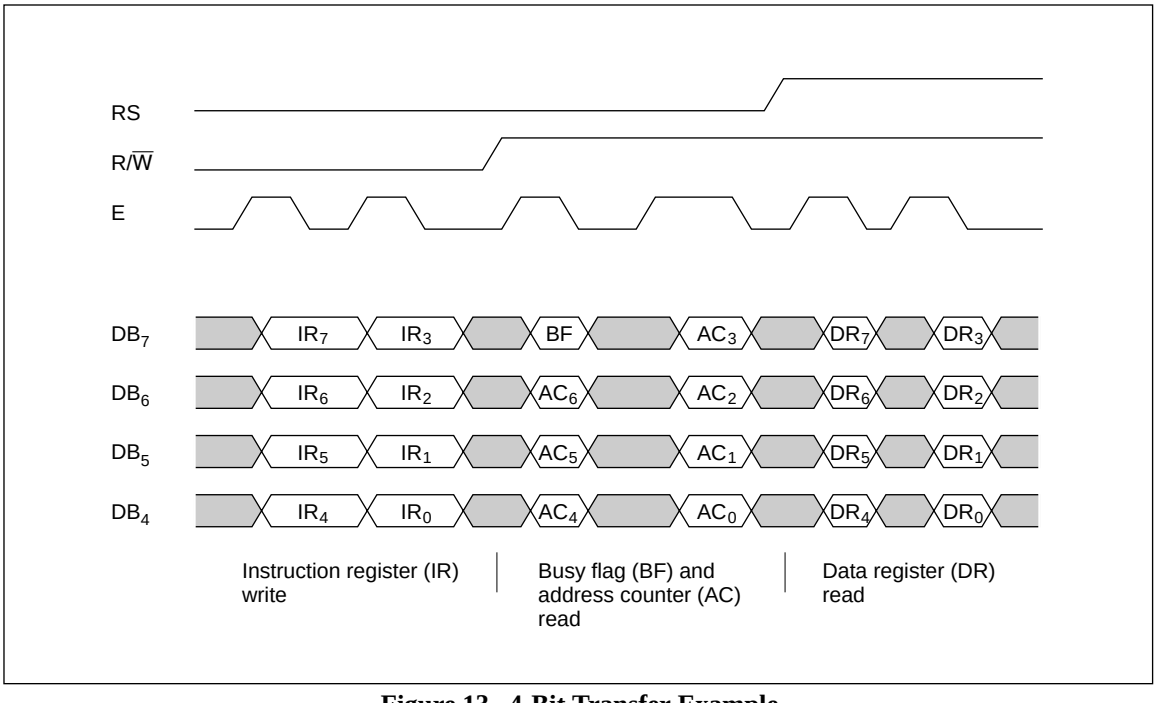


Figure 13 4-Bit Transfer Example

Transferring Serial Data

When the IM pin (interface mode) is low, the HD66712 enters serial interface mode. A three-line clock-synchronous transfer method is used. The HD66712 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66712 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the LCD-II/F12 can be reset and serial transfer synchronized by making chip select (CS*) high.

Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In the case of a minimum 1 to 1 transfer system with the LCD-II/F12 used as a receiver only, an interface can be established by the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS*) should be fixed to low.

The transfer clock (SCLK) is independent from operational clock (CLK) of the LCD-II/F12. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see continuous transfer) must be considered since the LCD-II/F12 does not have an internal transmit/ receive buffer.

To begin with, transfer the start byte. By receiving five consecutive bits (synchronizing bit string) at the beginning of the start byte, the transfer counter of the LCD-II/F12 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction (R/$\overline{W}$ bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

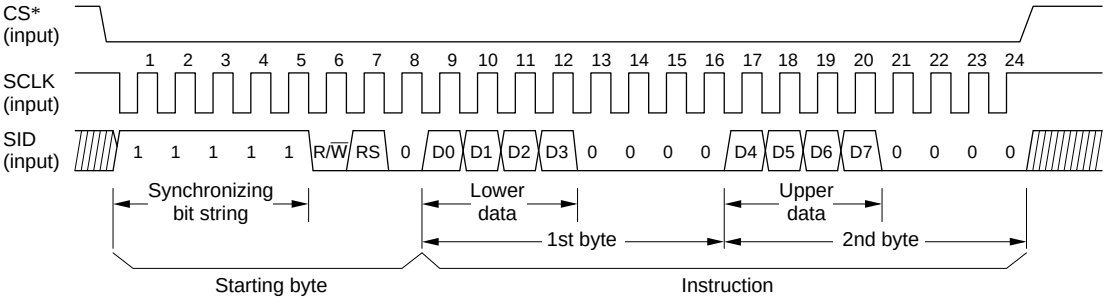
After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail below.

- Receiving (write)

  After receiving the start synchronization bits, the R/$\overline{W}$ bit (= 0), and the RS bit with the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are continuously received with R/$\overline{W}$ bit and RS bit unchanged, continuous transfer is possible (see “Continuous Transfer” below).

a) Basic transfer serial data input (receive)



b) Basic transfer of serial data output (transmit)

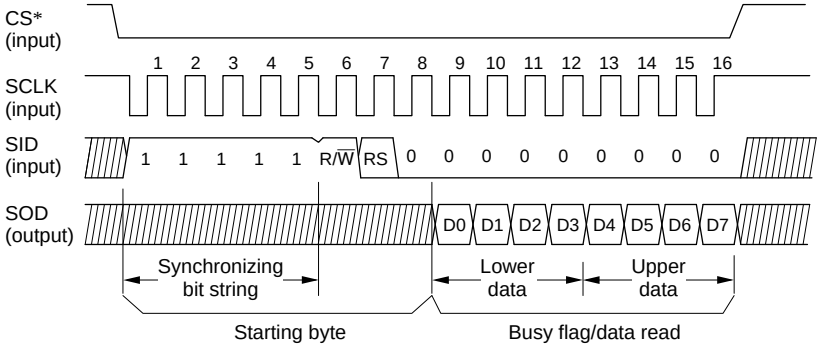


Figure 14 Basic Procedure for Transferring Serial Data

- Transmitting (read)

  After receiving the start synchronization bits, the R/$\overline{W}$ bit (= 1), and the RS bit with the start byte, 8-bit read data is transmitted in the same way as receiving. When read data is continuously transmitted with R/$\overline{W}$ bit and RS bit unchanged, continuous transfer is possible (see “Continuous Transfer” below).

  Even at the time of the transmission (the data output), since the HD66712 monitors the start synchronization bit string (“11111”) by the SID input, the HD66712 receives the R/W bit and RS bit after detecting the start synchronization. Therefore, in the case of a continuous transfer, fix the SID input “0.”

- Continuous transfer

  When instructions are continuously received with the R/$\overline{W}$ bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.

After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it.

To execute the next instruction, the instruction execution time of the LCD-II/F12 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.

In addition, if the next unit of data is read before read execution of previous data is completed for busy flag/address counter/RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, it is possible to transfer without reading the busy flag if wiring for transmission (SOD pin) needs to be reduced or if the burden of polling on the CPU needs to be removed. In this case, insert a transfer wait so that the current instruction first completes execution during instruction transfer.

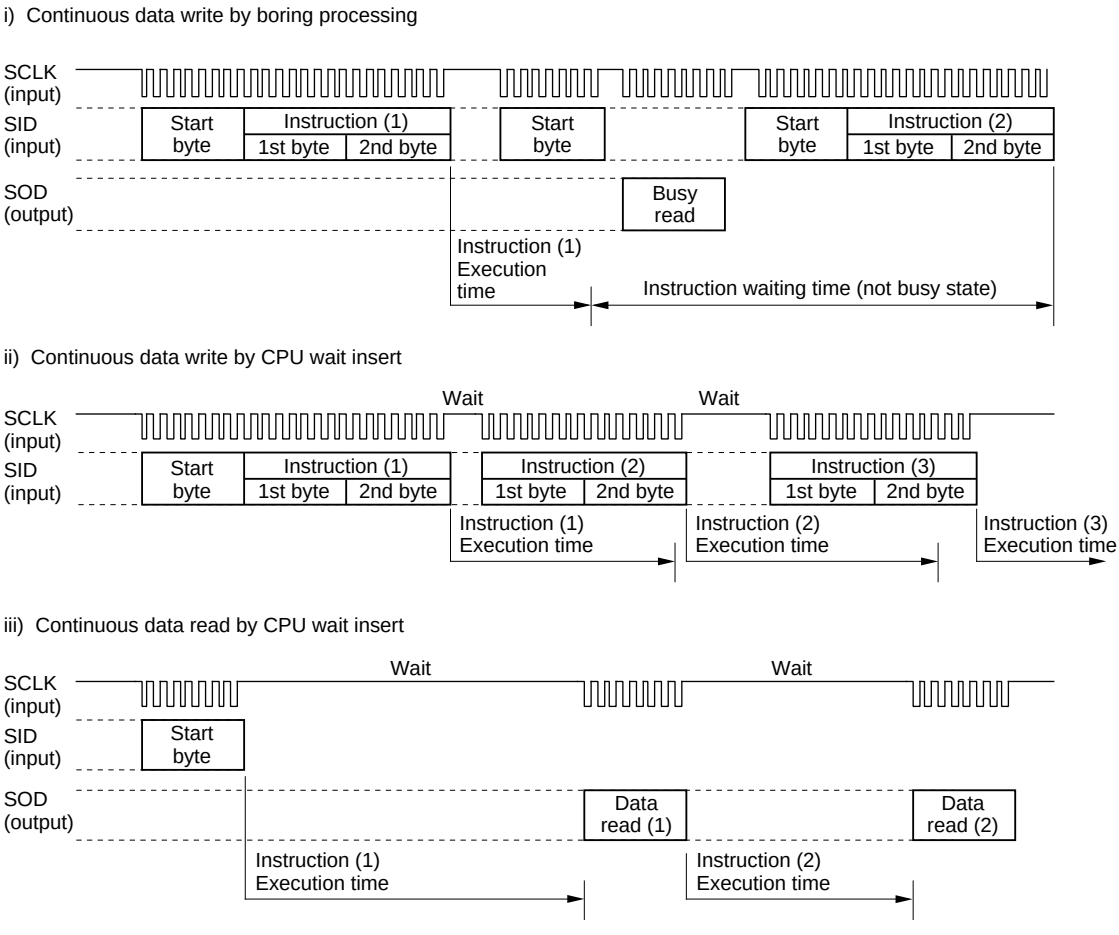


Figure 15 Procedure for Continuous Data Transfer

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66712 can be controlled by the MPU. Before starting internal operation of the HD66712, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66712 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD66712 instructions (table 12). There are four categories of instructions that:

- Designate HD66712 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66712 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 10) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/ address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66712 is not in the busy state (BF = 1) before sending an instruction from the MPU to the HD66712. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 12 for the list of each instruction execution time.

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). In addition, flicker may occur in a moment at the time of this instruction issue.

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. In a low power mode (LP = 1), do not set S = 1 because the whole display does not normally shift.

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font.

B: The character indicated by the cursor blinks when B is 1. The blinking is displayed as switching between all blank dots and displayed characters at a speed of 370-ms intervals when f_{cp} or f_{OSC} is 270 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 300 kHz, 370 × 270/300 = 333 ms.)

Extended Function Set

When the extended register enable bit (RE) is 1, FW, B/W, and NW bit shown below are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the left most bit, and the font is displayed with a 5-bit character width. If the FW bit is changed, data in DD RAM and CG RAM SEG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See “Oscillator Circuit” for details.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white inversion. At this time, bits C and B in display on/off control register are "Don't care." When f_{CP} or f_{OSC} is 270 kHz, display is changed by switching every 370 ms.

NW: When NW is 1, 4-line display is performed. At this time, bit N in the function set register is "Don't care."

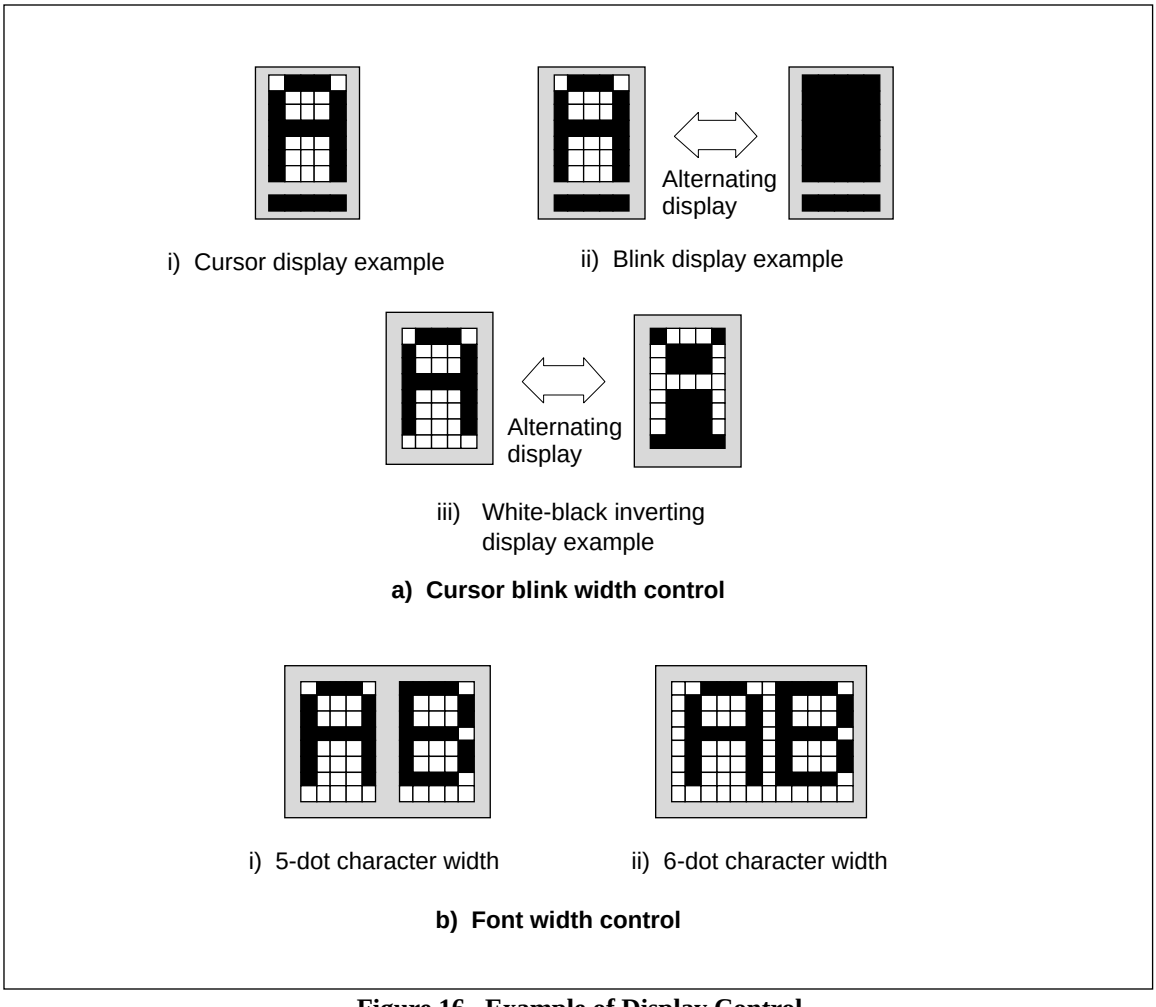


Figure 16 Example of Display Control

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 10). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. In a 4-line display, the cursor moves to the second line when it passes the 20th character of the line. Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position. When this instruction is executed, extended register enable bit (RE) is reset.

The address counter (AC) contents will not change if the only action performed is a display shift. In low power mode (LP = 1), whole-display shift cannot be normally performed.

Scroll Enable

When extended register enable bit (RE) is 1, scroll enable bits can be set.

This HSE resister specifies scrolled line with the scroll quantity register. This register consists of 4 bits for each display line, so a specified line can be shifted by dot unit. When the bit 0 of HSE is 1 in four line mode (NW = 1), the first line can be shifted, and the bit 1 is specified to shift the second line, the bit 2 is specified for the third line, and bit 3 is specified for the fourth line. When it shifts the first line in two line mode (N = 1, NW = 0), both the bit 0 and bit 1 should be set to 1. The bit 2 and bit 3 is specified for the second line.

In 1 line mode (N = 0, NW = 0), the bit 0 and bit 1 should be specified.

Function Set

Only when the extended register enable bit (RE) is 1, the BE and the LP bits shown below can be accessed. Bits DL and N can be accessed regardless of RE.

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0. When 4-bit length is selected, data must be sent or received twice.

N: When bit NW in the extended function set is 0, a 1- or a 2-line display is set. When N is 0, 1-line display is selected; when N is 1, 2-line display is selected. When NW is 1, a 4-line display is set. At this time, N is “Don’t care.”

Note: After changing the N or NW or LP bit, please issue the Return Home or Clear Display instruction to cancel to shift display.

RE: When bit RE is 1, bit BE in the extended function set register, the SEGRAM address set register, and the function set register can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

To maintain compatibility with the HD44780, the RE bit should be fixed to 0.

Table 10 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

BE: When the RE bit is 1, this bit can be rewritten. When this bit is 1, the user font in CGRAM and the segment in SEGRAM can be blinked according to the upper two bits of CGRAM and SEGRAM.

LP: When bit RE is 1, this bit can be rewritten. When LP is set to 1 and the EXT pin is low (without an extended driver), the HD66712 operates in low power mode. In 1-line display mode, the HD66712 operates on a 4-division clock, and in a 2-line or a 4-line display mode, the HD66712 operates on a 2-division clock. According to these operations, instruction execution takes four times or twice as long. Note that in low power mode, display shift cannot be performed. The frame frequency is reduced to 5/6 that of normal operation. See “Oscillator Circuit” for details.

Note: Perform the DL, N, NW, and FW fucntions at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, if bits N, NW, or FW are changed after other instructions are executed, RAM contents may be broken.

Set CG RAM Address

A CG RAM address can be set while the RE bit is cleared to 0.

Set CG RAM address into the address counter displayed by binary AAAAAA. After this address set, data is written to or read from the MPU for CG RAM.

Set SEGRAM Address

Only when the extended register enable (RE) bit is 1, HS2 to HS0 and the SEGRAM address can be set.

The SEGRAM address in the binary form AAAA is set to the address counter. After this address set, SEGRAM can be written to or read from by the MPU.

Set DD RAM Address

A DD RAM address can be set while the RE bit is cleared to 0. Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

After this address set, data is written to or read from the MPU for DD RAM.

However, when N and NW is 0 (1-line display), AAAAAAA can be (00)H to (4F)H. When N is 1 and NW is 0 (2-line display), AAAAAAA is (00)H to (27)H for the first line, and (40)H to (67)H for the second line. When NW is 1 (4-line display), AAAAAAA is (00)H to (13)H for the first line, (20)H to (33)H for the second line, (40)H to (53)H for the third line, and (60)H to (73)H for the fourth line.

Set Scroll Quantity

When extended registor enable bit (RE) is 1, HDS5 to HDS0 can be set.

HDS5 to HDS0 specifies horizontal scroll quantity to the left of the display in dot units. The HD66712 uses the unused DDRAM area to execute a desired horizontal smooth scroll from 1 to 48 dots.

Note: When performing a horizontal scroll as described above by connecting an extended driver, the maximum number of characters per line decreases by the quantity set by the above horizontal scroll. For example, when the maximum 24-dot scroll quantity (4 characters) is used with 6-dot font width and 4-line display, the maximum numbers of characters is 20 – 4 = 16. Notice that in low power mode (LP = 1), display shift and scroll cannot be performed.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG, DD, and SEGRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for CG RAM, DD RAM, and SEGRAM address set instructions.

Write Data to CG, DD, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG, DD or SEGRAM. CG, DD or SEGRAM is selected by the previous specification of the address set instruction (CG RAM address set / DD RAM address set / SEGRAM address set). After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG, DD, or SEG RAM. CG, DD or SEGRAM is selected by the previous specification of the address set instruction. If no address is specified, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

Table 11 HS5 to HS0 Settings

HDS5	HDS4	HDS3	HDS2	HDS1	HDS0	Description
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift the display position to the left by one dot.
0	0	0	0	1	0	Shift the display position to the left by two dots.
0	0	0	0	1	1	Shift the display position to the left by three dots.
				⋮		
1	0	1	1	1	1	Shift the display position to the left by forty-seven dots.
1	1	*	*	*	*	Shift the display position to the left by forty-eight dots.

Table 12 Instructions

Instruction	RE Bit	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (Max) (when f_{cp} or f_{OSC} is 270 kHz)
Clear display	0/1	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.52 ms
Return home	0/1	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 IN address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0/1	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Extension function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Sets a font width, a black-white inverting cursor (B/W), and a 4-line display (NW).	37 µs
Cursor or display shift	0	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Scroll enable	1	0	0	0	0	0	1	HSE	HSE	HSE	HSE	Specifies which display lines to undergo horizontal smooth scroll.	37 µs
Function set	0	0	0	0	0	1	DL	N	RE	—	—	Sets interface data length (DL), number of display lines (L), and extension register write enable (RE).	37 µs
	1	0	0	0	0	1	DL	N	RE	BE	LP	Sets CGRAM/SEGRAM blinking enable (BE), and power-down mode (LP). LP is available when the EXT pin is low.	37 µs
Set CGRAM address	0	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set SEGRAM address set	1	0	0	0	1	*	*	A_{SEG}	A_{SEG}	A_{SEG}	A_{SEG}	Sets SEGRAM address. SEGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Set scroll quantity	1	0	0	1	*	HDS	HDS	HDS	HDS	HDS	HDS	Sets horizontal dot scroll quantity.	37 µs

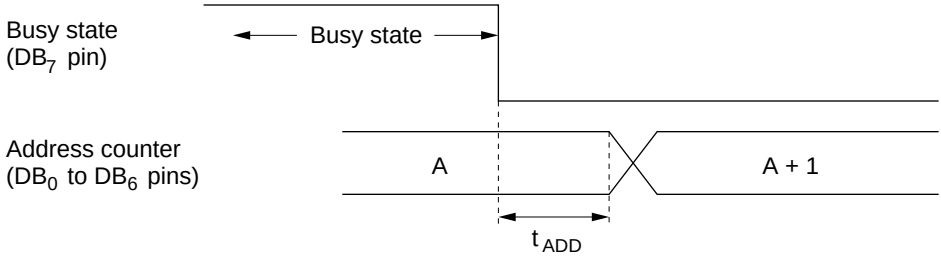
Table 12 Instructions (cont)

Instruction	RE Bit	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (Max) (when f_{cp} or f_{OSC} is 270 kHz)
Read busy flag & address	0/1	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write data to RAM	0/1	1	0	Write data								Writes data into DD RAM, CG RAM, or SEGRAM.	7 µs t_{ADD} = 5.5 µs*
Read data from RAM	0/1	1	1	Read data								Reads data from DD RAM, CG RAM, or SEGRAM.	37 µs t_{ADD} = 5.5 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift D = 1: Display on C = 1: Cursor on B = 1: Blink on FW = 1: 6-dot font width B/W = 1: Black-white inverting cursor on NW = 1: Four lines NW = 0: One or two lines S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line RE = 1: Extension register access enable BE = 1: CGRAM/SEGRAM blinking enable LP = 1: Low-power mode BF = 1: Internally operating BF = 0: Instructions acceptable											DD RAM: Display data RAM A_{DD}: DD RAM address (corresponds to cursor address) CG RAM: Character generator RAM A_{CG}: CG RAM address SEGRAM: Segment RAM A_{SEG}: Segment RAM address HSE: Specifies horizontal scroll lines HDS: Horizontal dot scroll quantity AC: Address counter used for both DD, CG, and SEG RAM addresses.	

Note: 1. — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 17, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. Extension time changes as frequency changes. For example, when f is 300 kHz, the execution time is: 37 µs × 270/300 = 33 µs.
3. Execution time in a low-power mode (LP = 1 and EXT = low) becomes four times for a 1-line mode, and twice for a 2- or 4-line mode.



t_{ADD} depends on the operation frequency.
t_{ADD} = 1.5/(f_{cp} or f_{OSC}) seconds

Figure 17 Address Counter Update

Interfacing the HD66712

Interface with 8-Bit MPUs: The HD66712 can interface directly with an 8-bit MPU using the E clock, or with an 8-bit MCU through an I/O port. When the number of I/O ports in the MCU, or the interfacing bus width, if limited, a 4-bit interface function is used.

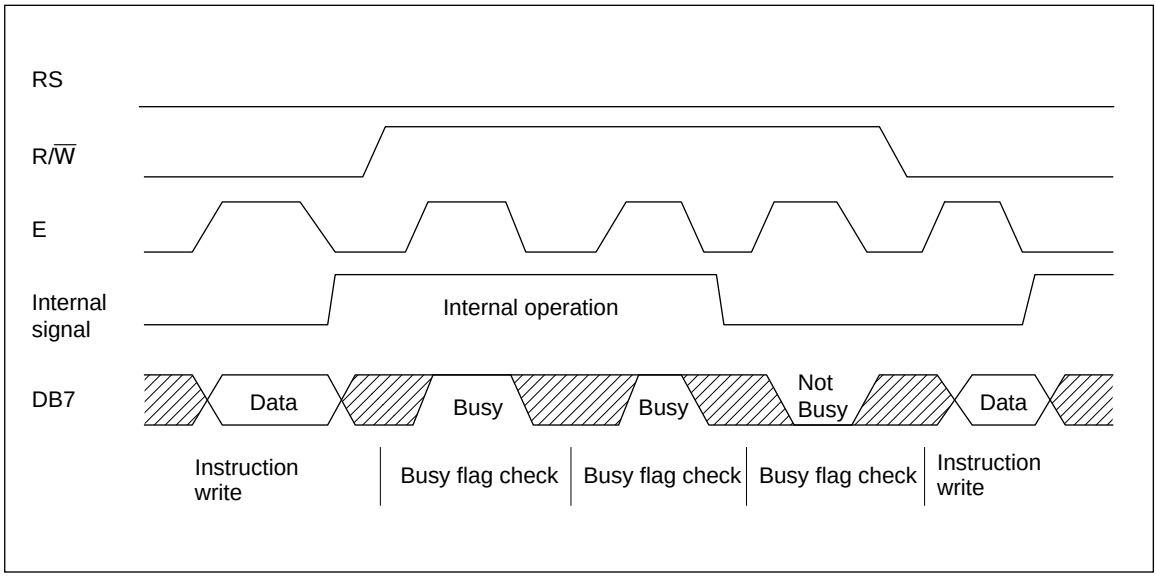
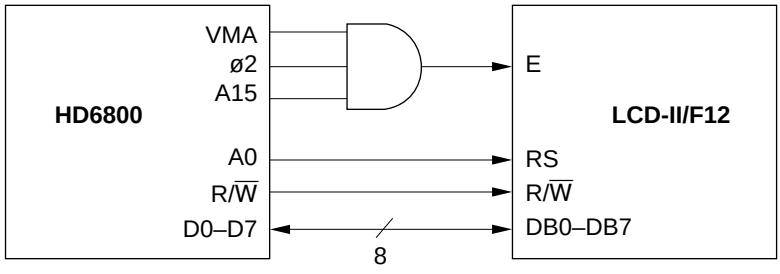


Figure 18 Example of 8-Bit Data Transfer Timing Sequence

i) Bus line interface



ii) I/O port interface

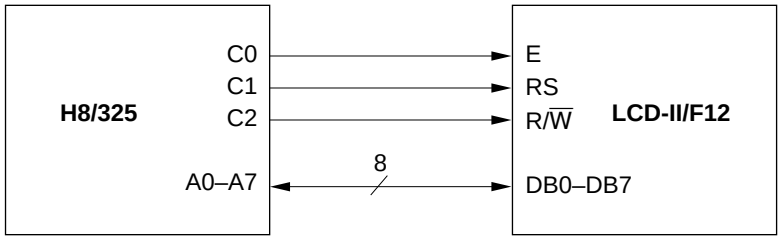


Figure 19 8-Bit MPU Interface

Interface with 4-Bit MPUs: The HD66712 can interface with a 4-bit MCU through an I/O port. 4-bit data representing high and low order bits must be transferred sequentially.

The DL bit in function-set selects 4-bit or 8-bit interface data length.

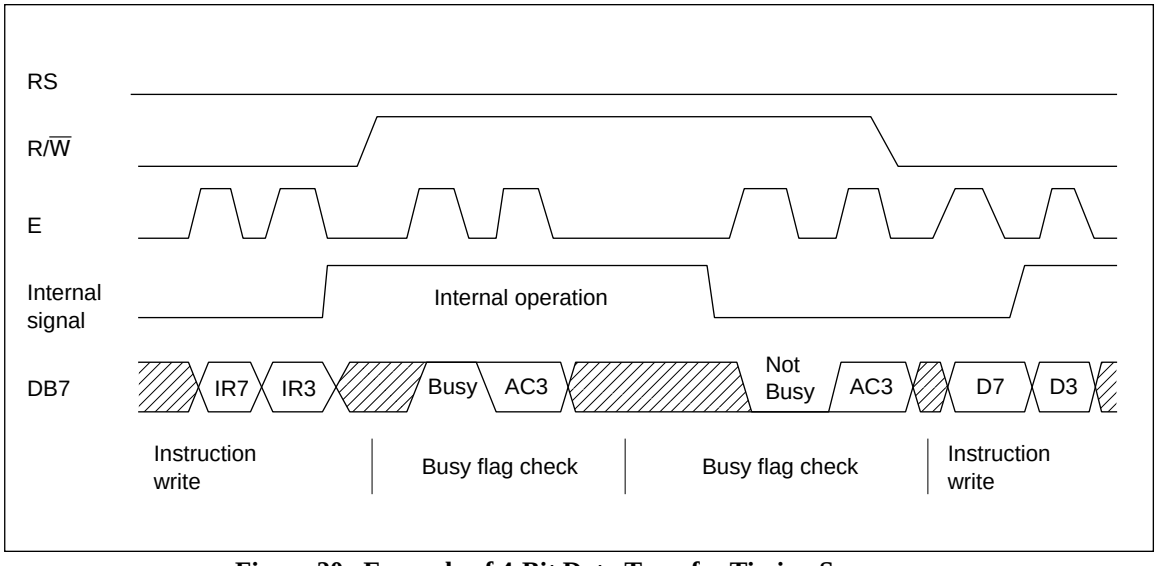


Figure 20 Example of 4-Bit Data Transfer Timing Sequence

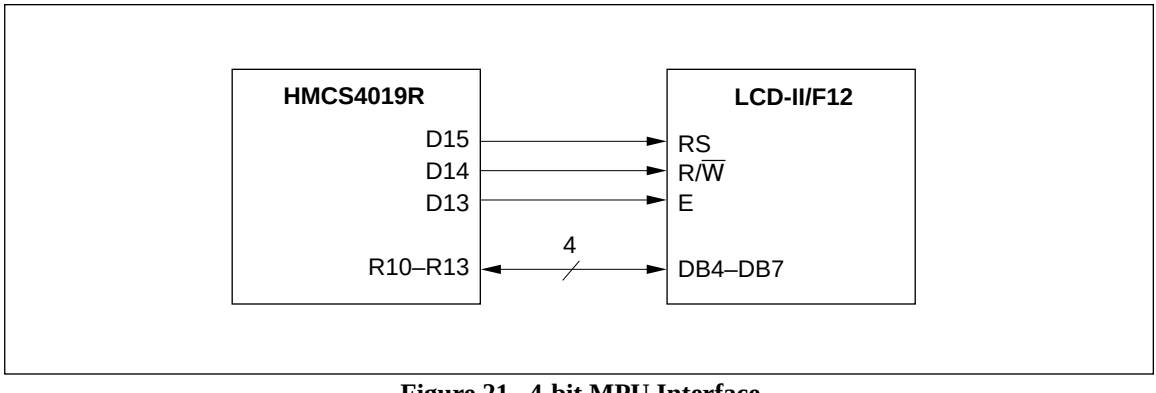
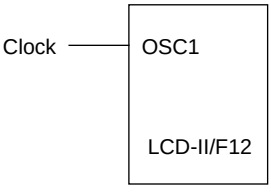


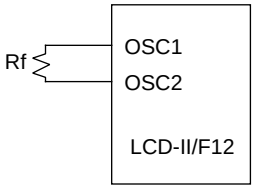
Figure 21 4-bit MPU Interface

Oscillator Circuit

1) When an external clock is used



2) When an internal oscillator is used

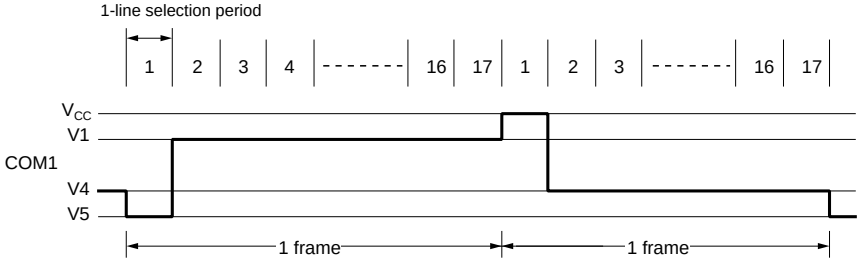


The oscillator frequency can be adjusted by oscillator resistance (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. The recommended oscillator resistor is as follows.

- Rf = 91 kΩ ± 2% (V_{CC} = 5 V)
- Rf = 75 kΩ ± 2% (V_{CC} = 3 V)

Figure 22 Oscillator Circuit

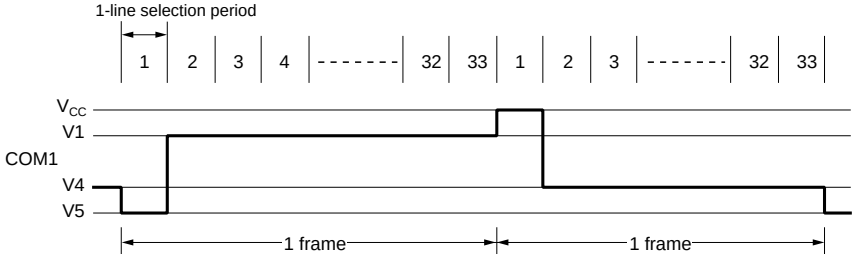
(1) 1 /17 duty cycle



	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	200 clocks	240 clocks	60 clocks	72 clocks
Frame frequency	79.4 Hz	66.2 Hz	66.2 Hz	55.1 Hz

Note: At the calculation example above for displayed frame frequency, all oscillator frequencies are 270 kHz (1 clock = 3.7 µs).

(2) 1 /33 duty cycle



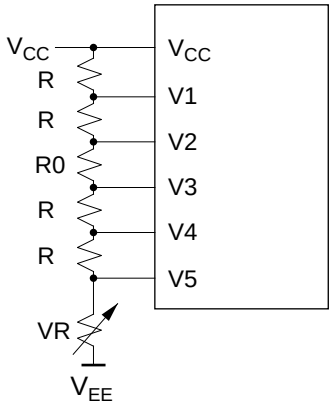
	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	100 clocks	120 clocks	60 clocks	72 clocks
Frame frequency	81.8 Hz	68.2 Hz	68.2 Hz	56.8 Hz

Note: At the calculation example above for displayed frame frequency, all oscillator frequencies are 270 kHz (1 clock = 3.7 µs).

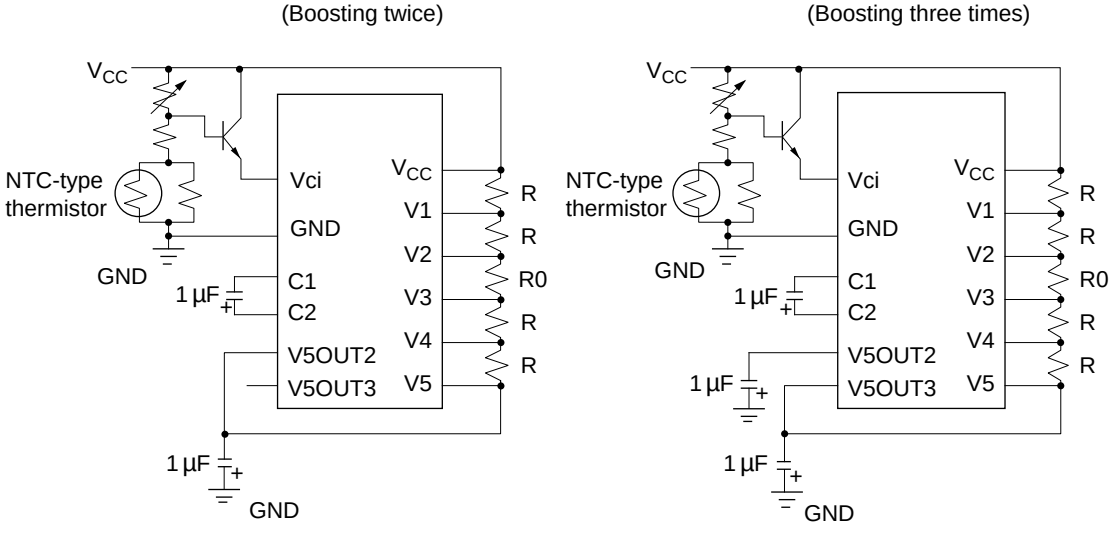
Figure 23 Frame Frequency

Power Supply for Liquid Crystal Display Drive

1) When an external power supply is used



2) When an internal booster is used



Notes: 1. Boosting output voltage should not exceed the power supply voltage (2) (15 V max.) in the absolute maximum ratings. Especially, voltage of over 5 V should not be input to the reference voltage (Vci) when boosting three times.

2. Vci input terminal is used for reference voltage and power supply for the internal booster. Input current into the Vci pin needs three times or more of load current through the bleeder resistor for LCD. So, when it adjusts LCD driving voltage (Vlcd), input voltage should be controlled with transistor to supply LCD load current. Please notice connection (+/–) when it uses capacitors with poler.

3. The Vci must be set below the power supply (V_{CC}).

Table 13 Duty Factor and Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2/4
Duty factor		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

Note: R changes depending on the size of liquid crystal panel. Normally, R must be 4.7 kΩ to 20 kΩ.

Extension Driver LSI Interface

By bringing the EXT pin high, extended driver interface signals (CL1, CL2, D, and M) are output.

Table 14 Relationships between the Number of Display Lines and 40-Output Extension Driver

	Controller					
	LCD-II/F12		LCD-II/F8		HD44780	HD66702
Display Lines	5-Dot Width	6-Dot Width	5-Dot Width	6-Dot Width	5-Dot Width	5-Dot Width
16 × 2 lines	Not required	Not required	Not required	1	1	Not required
20 × 2 lines	Not required	Not required	1	1	2	Not required
24 × 2 lines	Not required	1	1	2	2	1
40 × 2 lines	Disabled	Disabled	Disabled	Disabled	4	3
12 × 4 lines	Not required	1	1	1	Disabled	Disabled
16 × 4 lines	1	1	1	2	Disabled	Disabled
20 × 4 lines	1	2	2	3	Disabled	Disabled

Note: The number of display lines can be extended to 32 × 2 lines or 20 × 4 lines in the LCD-II/F12.
The number of display lines can be extended to 30 × 2 lines or 20 × 4 lines in the LCD-II/F8.

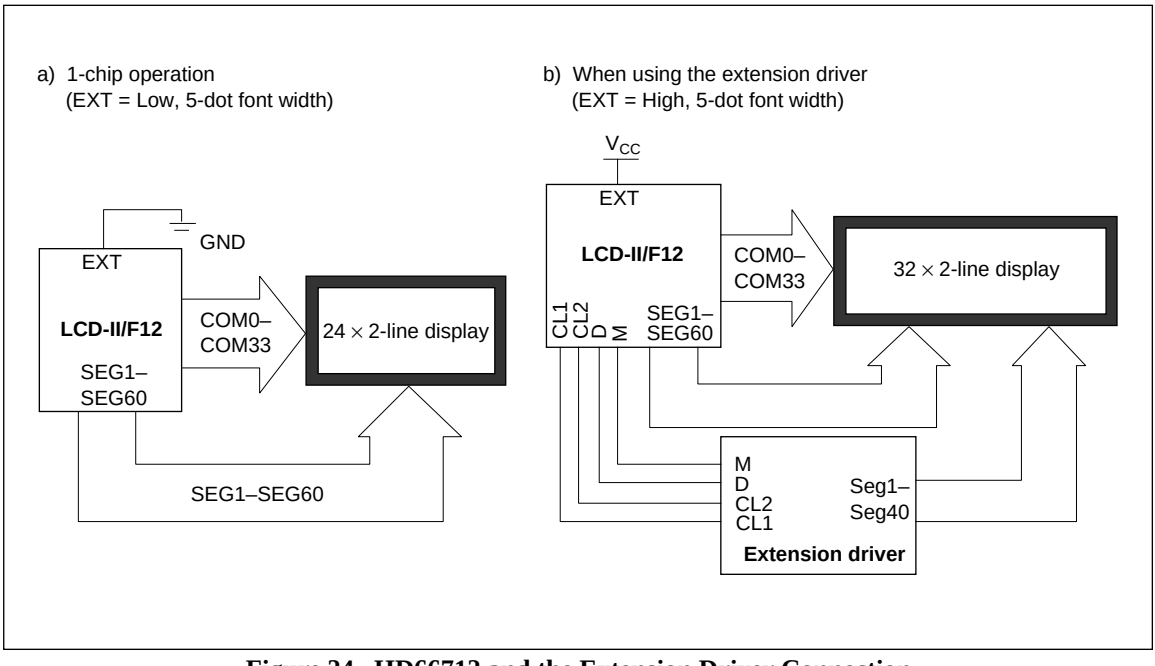


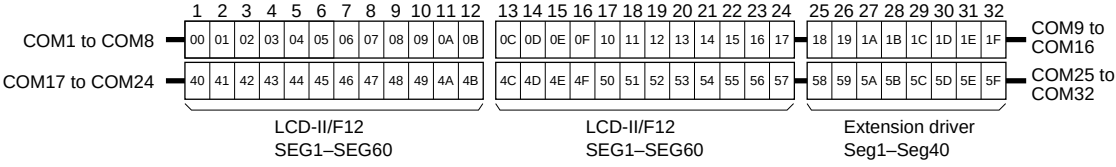
Figure 24 HD66712 and the Extension Driver Connection

Table 15 Display Start Address in Each Mode

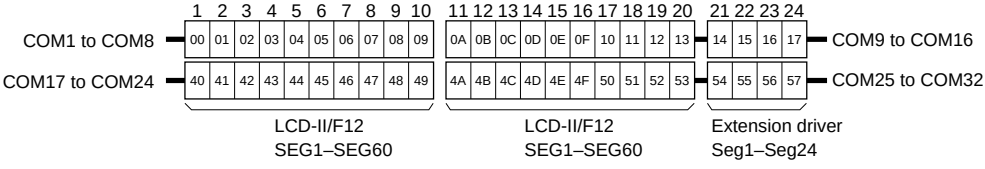
	Number of Lines				
	1-Line Mode		2-Line Mode		4-Line Mode
Output	**5 Dot**	**6 Dot**	**5 Dot**	**6 Dot**	**5 Dot/6 Dot**
COM1–COM8	D00±1	D00±1	D00±1	D00±1	D00±1
COM9–COM16	D0C±1	D0A±1	D0C±1	D0A±1	D20±1
COM17–COM24	—	—	D40±1	D40±1	D40±1
COM25–COM32	—	—	D4C±1	D4A±1	D60±1
COM0/COM17	S00	S00	—	—	—
COM0/COM33	—	—	S00	S00	S00

Notes: 1. The number of display lines is determined by setting the N/NW bit. The font width is determined by the FW bit.
2. D** is the start address of display data RAM (DDRAM).
3. S** is the start address of segment RAM (SEGRAM).
4. ±1 following D** indicates increment or decrement at display shift.

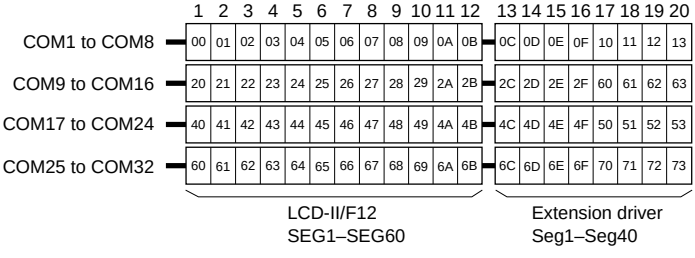
a) 5-dot font width: 32 × 2-line display



b) 6-dot font width: 24 × 2-line display



c) 5-dot font width: 20 × 4-line display



d) 6-dot font width: 20 × 4-line display

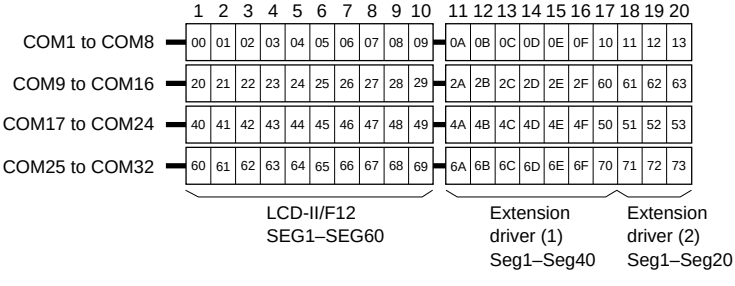


Figure 25 Correspondence between the Display Position at Extension Display and the DDRAM Address

Interface to Liquid Crystal Display

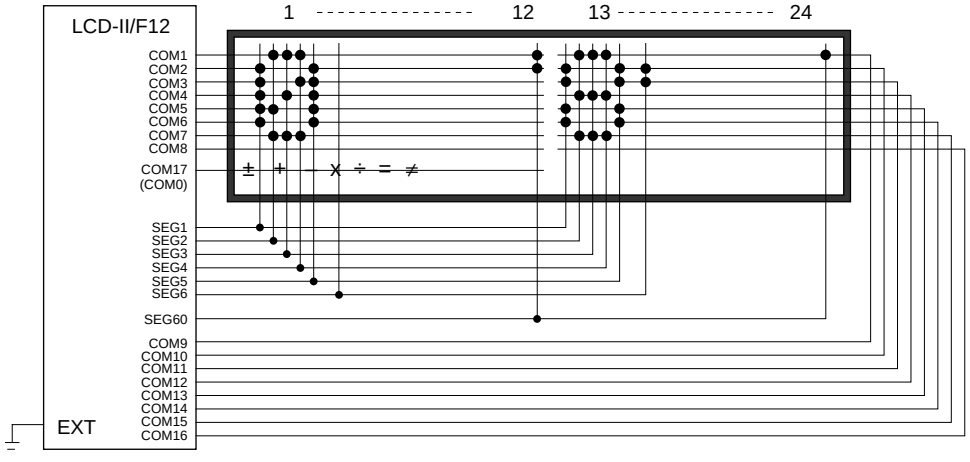
Set the extended driver control signal output, the number of display lines, and the font width with the EXT pin, an extended register NW, and the FW bit, respectively. The relationship between the number of display lines, EXT pin, and register value is given below.

Table 16 Relationship between Display Lines, EXT Pin, and Register Setting

		5 Dot Font						6 Dot Font						
				Registor Setting						Registor Setting				
No. of Lines	No. of Character	EXT Pin	Extended Driver	N	RE	NW	FW	EXT Pin	Extended Driver	N	RE	NW	FW	Duty
1	20	L	—	0	0	0	0	L	—	0	1	0	1	1/17
	24	L	—	0	0	0	0	H	1	0	1	0	1	1/17
	40	H	2	0	0	0	0	H	3	0	1	0	1	1/17
2	20	L	—	1	0	0	0	L	—	1	1	0	1	1/33
	24	L	—	1	0	0	0	H	1	1	1	0	1	1/33
	32	H	1	1	0	0	0	H	2	1	1	0	1	1/33
4	12	L	—	*	1	1	0	H	1	*	1	1	1	1/33
	16	H	1	*	1	1	0	H	1	*	1	1	1	1/33
	20	H	1	*	1	1	0	H	2	*	1	1	1	1/33

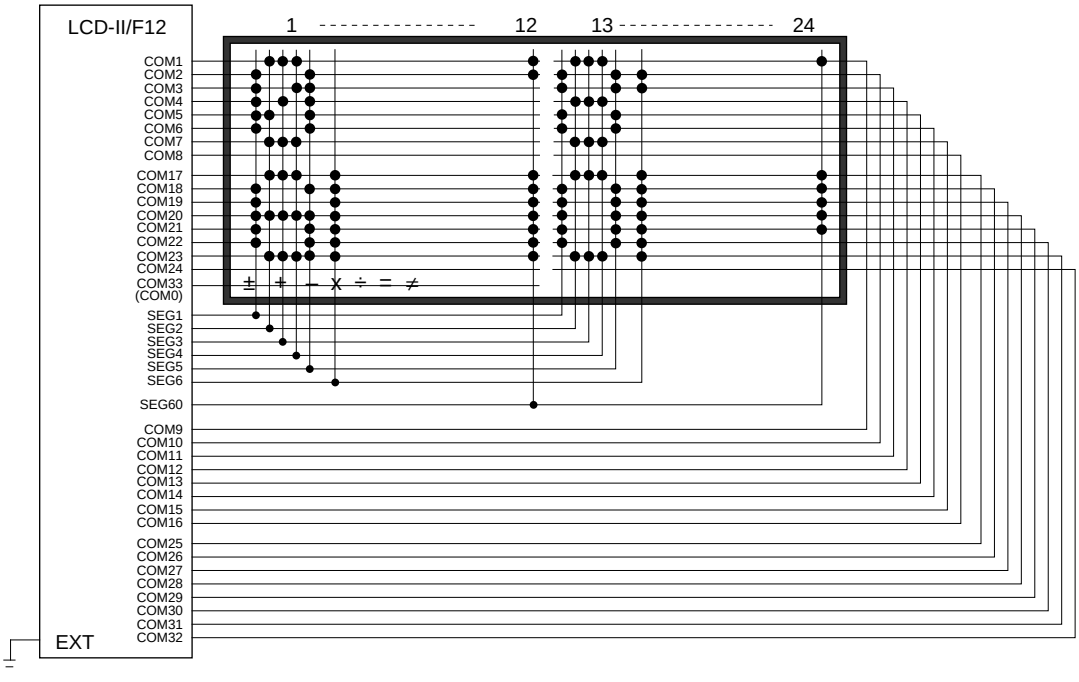
Note: — means not required.

- Example of 5-dot font width connection



Note: COM0 and COM17 output the same signals. Apply them according to the wiring pattern.

Figure 26 24 × 1-Line + 60-Segment Display (5-Dot Font, 1/17 Duty)



Note: COM0 and COM33 output the same signals. Apply them according to the wiring pattern.

Figure 27 24 × 1-Line + 60-Segment Display (5-Dot Font, 1/33 Duty)

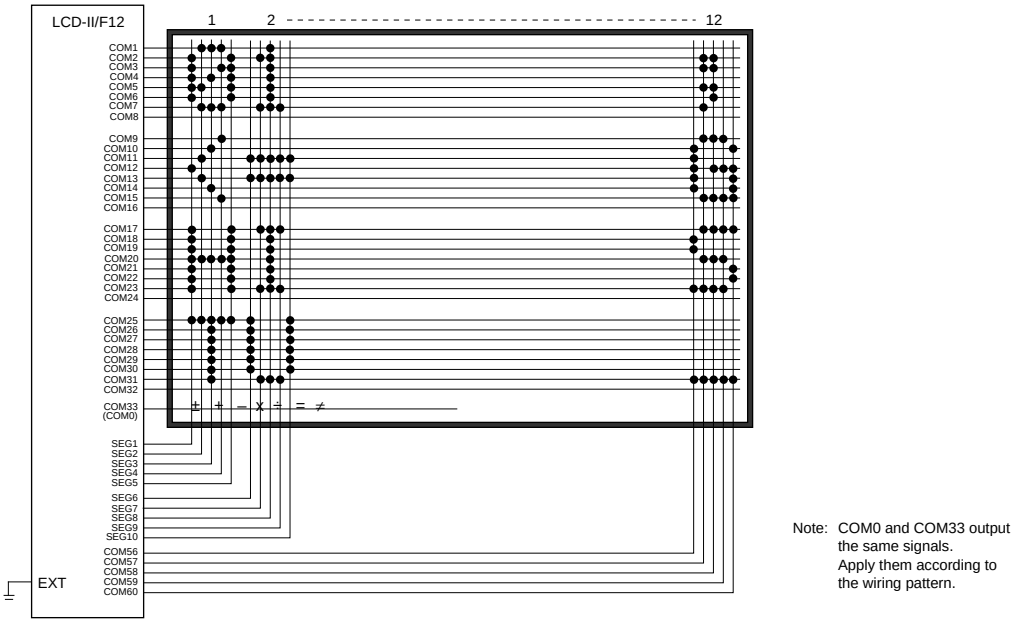


Figure 28 12 × 4-Line + 60 Segment Display (5-Dot Font, 1/33 Duty)

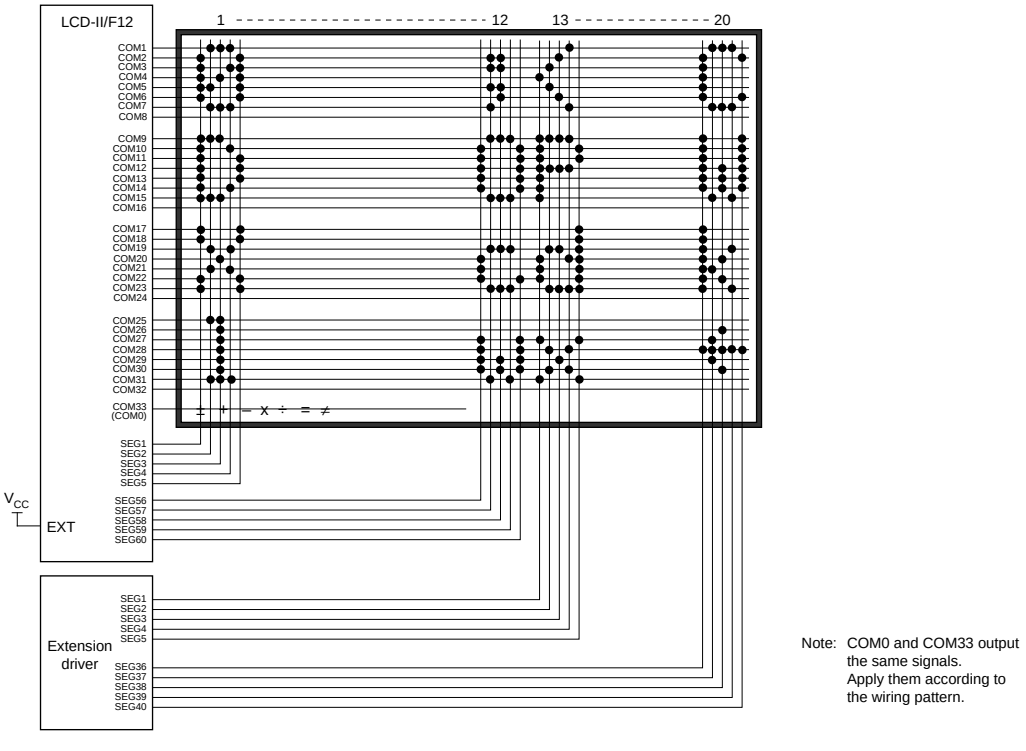
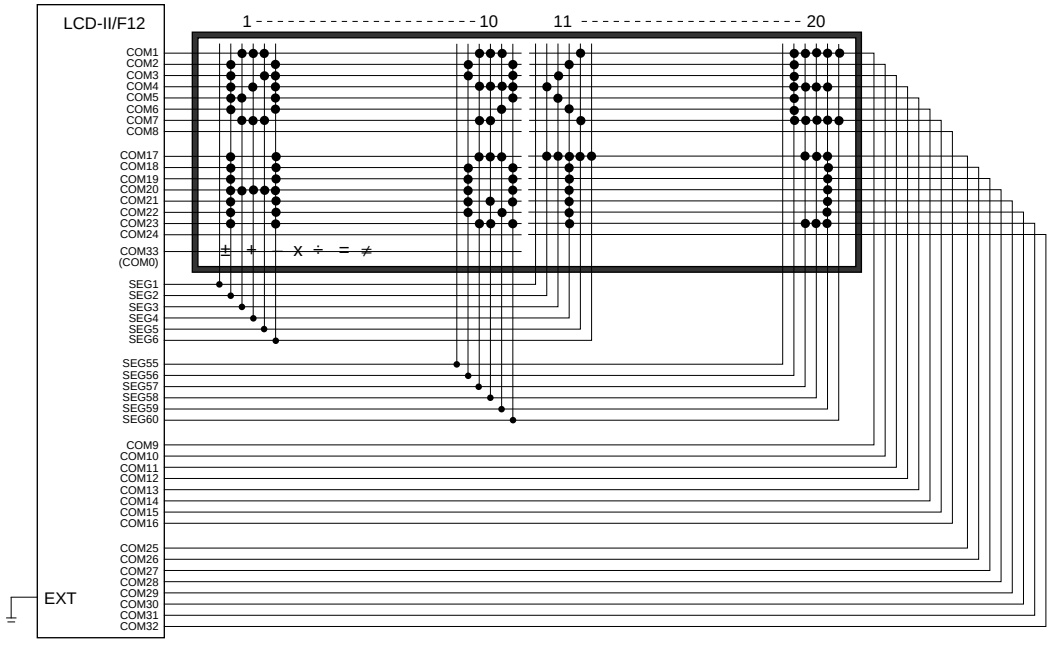


Figure 29 20 × 4-Line + 80 Segment Display (5-Dot Font, 1/33 Duty)



Note: COM0 and COM33 output the same signals. Apply them according to the wiring pattern.

Figure 30 20 × 2-Line + 60 Segment Display (6-Dot Font, 1/33 Duty)

Instruction and Display Correspondence

- 8-bit operation, 24-digit × 1-line display with internal reset

  Refer to table 17 for an example of an 24-digit × 1-line display in 8-bit operation. The LCD-II/F12 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, a character unit scroll can be performed by a display shift instruction. A dot unit smooth scroll can also be performed by a horizontal scroll instruction. Since data of display RAM (DDRAM) is not changed by a display shift instruction, the display can be returned to the first set display when the return home operation is performed.

- 4-bit operation, 24-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (see table 18). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions. Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 24-digit × 2-line display with internal reset

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 16 characters in the first line, the DD RAM address must be again set after the 16th character is completed. (See table 19.)

  The display shift is performed for the first and second lines. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

- 8-bit operation, 12-digit × 4-line display with internal reset

  The RE bit must be set by the function set instruction and then the NW bit must be set by an extension function set instruction. In this case, 4-line display is always performed regardless of the N bit setting (see table 20).

  In a 4-line display, the cursor automatically moves from the first to the second line after the 20th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set again after the 8th character is completed. Display shifts are performed on all lines simultaneously.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the LCD-II/F12 must be initialized by instructions. See the section, Initializing by Instruction.

Table 17 8-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 1-line display. Bit 2 must always be cleared.
	RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
	0	0	0	0	1	1	0	0	*	*		
3	Return home											Return both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		
4	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
5	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
6	Write data to CG RAM/DD RAM										H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
	1	0	0	1	0	0	1	0	0	0		
7	Write data to CG RAM/DD RAM										HI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	. . . . .										. . . . .	
9	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
10	Entry mode set										HITACHI_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
11	Write data to CG RAM/DD RAM										ITACHI _	Writes a space.
	1	0	0	0	1	0	0	0	0	0		

Table 17 8-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
12	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
13					⋮						⋮	
14	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
17	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
18	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
19	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
20	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
21					⋮						⋮	
22	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 18 4-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 4-bit operation. Clear bit 2. In this case, operation is handled as 8 bits by initialization. *1
	RS	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
	0	0	0	0	1	0	—	—	—	—		
	—	—	—	—	—	—	—	—	—	—		
3	Function set											Sets 4-bit operation and selects 1-line display. Clear BE, LP bits. 4-bit operation starts from this step.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	1	0	0	—	—	—	—		
4	Function set											Sets 4-bit operation and selects 1 line display. Clear bit 2 (RE).
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	0	*	*	—	—	—	—		
5	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	0	1	0	—	—	—	—		
6	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	—	—	—	—		
	0	0	1	1	1	0	—	—	—	—		
7	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	1	1	0	—	—	—	—		
8	Write data to CG RAM/DD RAM										H_	Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	—	—	—	—		
	1	0	1	0	0	0	—	—	—	—		
					.							Based on 8-bit operation after this instruction.
					.							
					.							

Note: The control is the same as for 8-bit operation beyond step #8.

1. When DB3 to DB0 pins are open in 4-bit mode, the RE, BE, LP bits are set to “1” at step #2. So, these bits are clear to “0” at step #3.

Table 19 8-Bit Operation, 24-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display. Clear bit 2.
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control											Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0	_	
4	Entry mode set											Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0	_	
5	Write data to CG RAM/DD RAM											Writes “H.” DD RAM has already been selected by initialization at power-on.
	1	0	0	1	0	0	1	0	0	0	H_	
6	⋮										⋮	
7	Write data to CG RAM/DD RAM											Writes I.
	1	0	0	1	0	0	1	0	0	1	HITACHI_	
8	Set DD RAM address											Sets DD RAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0	HITACHI _	

Table 19 8-Bit Operation, 24-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CG RAM/DD RAM										HITACHI M_	Writes a space.
	1	0	0	1	0	0	1	1	0	1		
10					⋮						⋮	
11	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
14					⋮						⋮	
15	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 20 8-Bit Operation, 12-Digit × 4-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	0	1	*	*		Sets 8-bit operation and enables write to the extension register.
3	4-line mode set	0	0	0	0	0	0	1	0	0	1		Sets 4-line operation.
4	Return home	0	0	0	0	0	0	0	0	1	0		Return both display and cursor to the original position.
5	Function set Inhibit write to extension register	0	0	0	0	1	1	0	0	*	*		Inhibits write to extension register. Invalidates selection of 1-line/2-line by bit 3.
6	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is cleared because of initialization.
7	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right when writing to RAM. Display is not shifted.
8	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DDRAM has already been selected by initialization.
9	. . . . .											. . . . .	

Table 20 8-Bit Operation, 12-Digit × 4-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
10	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
11	Set DD RAM address 0	0	1	0	1	0	0	0	0	0	HITACHI _	Sets DD RAM address to (20)H so that the cursor is positioned at the beginning of the second line.
12	Write data to CG RAM 1	0	0	0	1	1	0	0	0	0	HITACHI 0_	Writes 0.

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

- Initializing when a length of interface is 8-bit system. (See figure 31.)
- Initializing when a length of interface is 4-bit system. (See figure 32.)

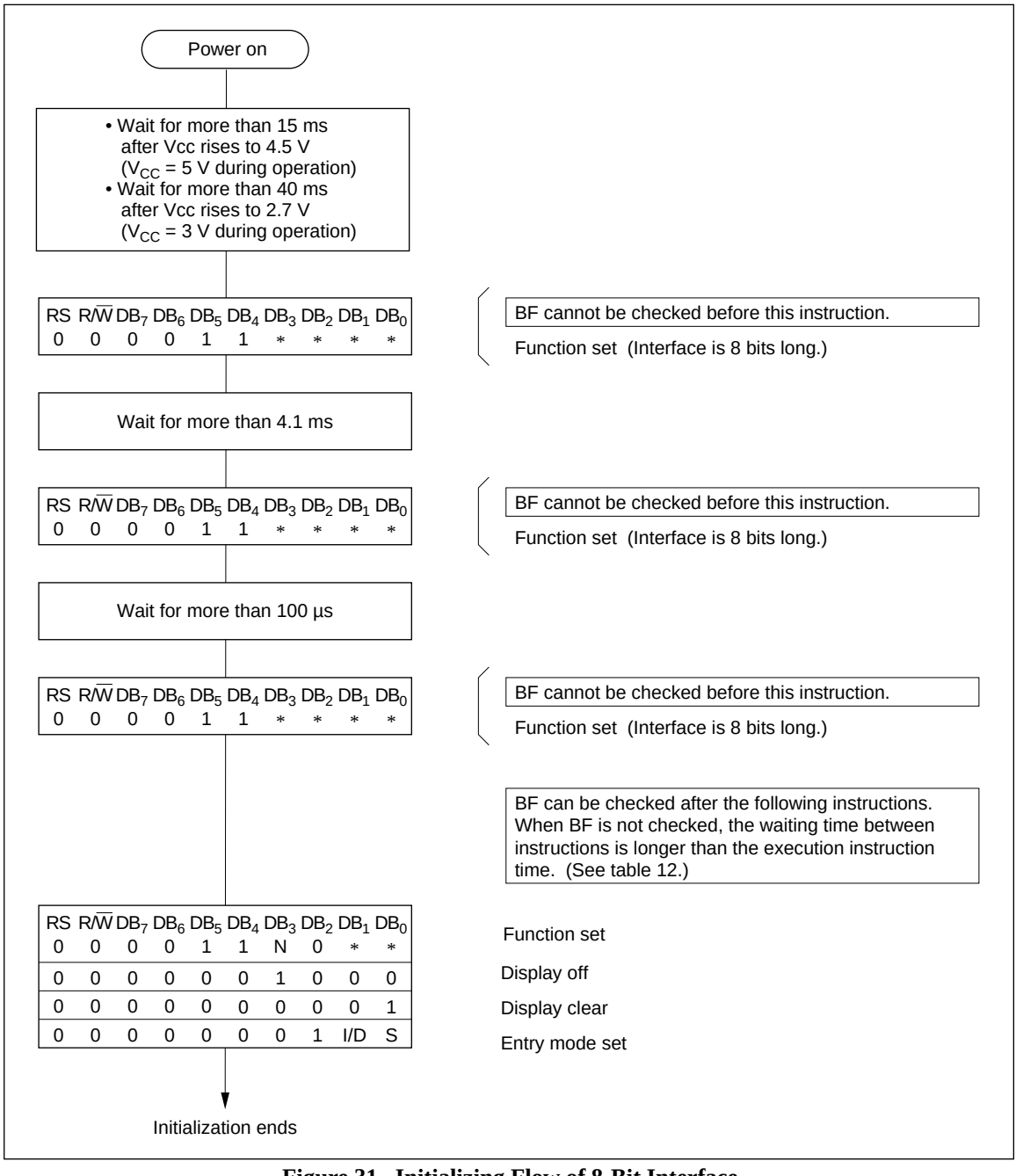


Figure 31 Initializing Flow of 8-Bit Interface

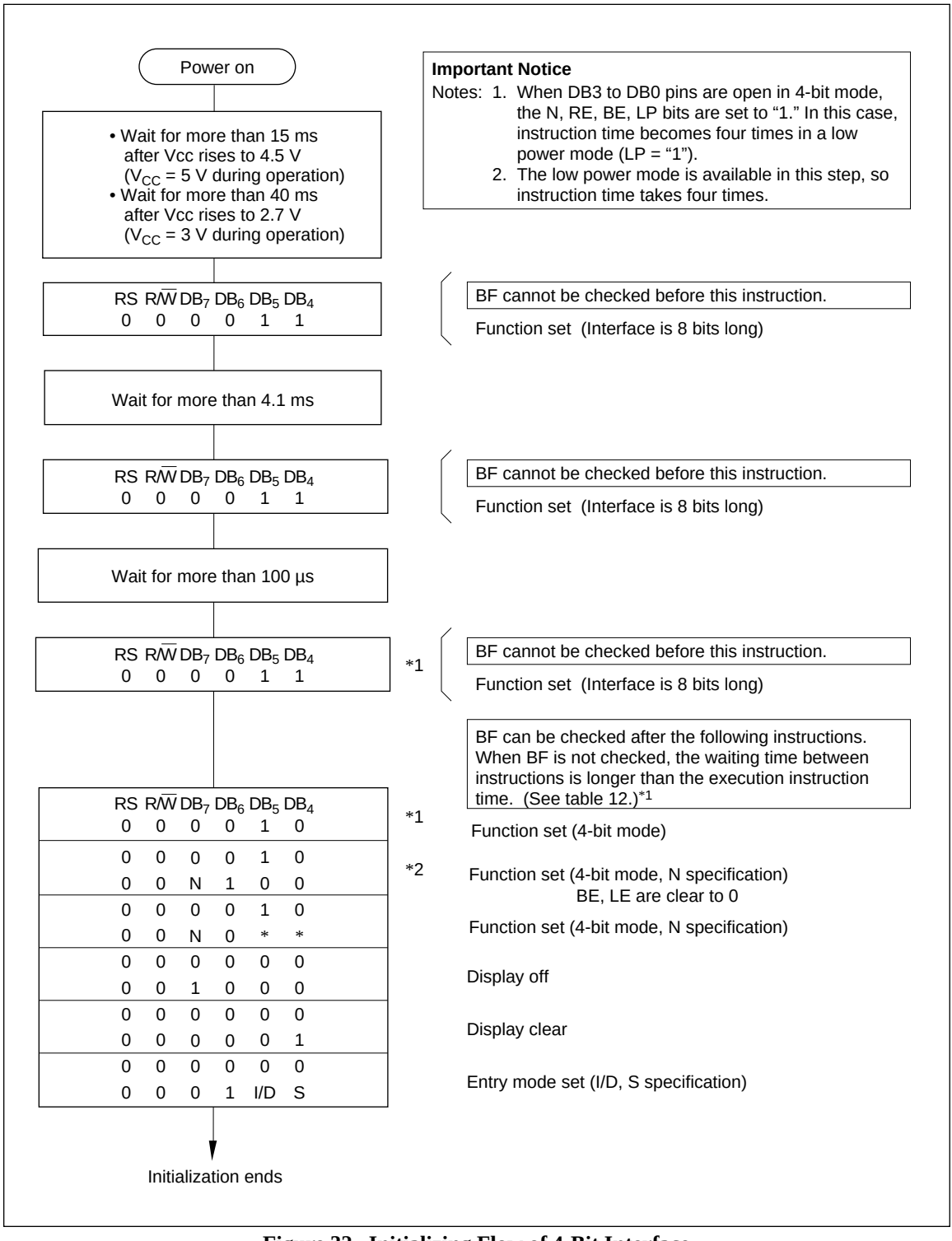


Figure 32 Initializing Flow of 4-Bit Interface

Horizontal Dot Scroll

Dot unit scrolls are performed by setting the horizontal dot scroll quantity resister (HDS) when the extension register is enabled (RE = “1”). And the shifted line can be selected with the scroll enable register (HDE). So, it can control dot unit shifts by each display line.

To scroll smoothly, LCD-II/F12 supports 6 dots-font width mode (FW = 1). The below figures are examples of scroll display.

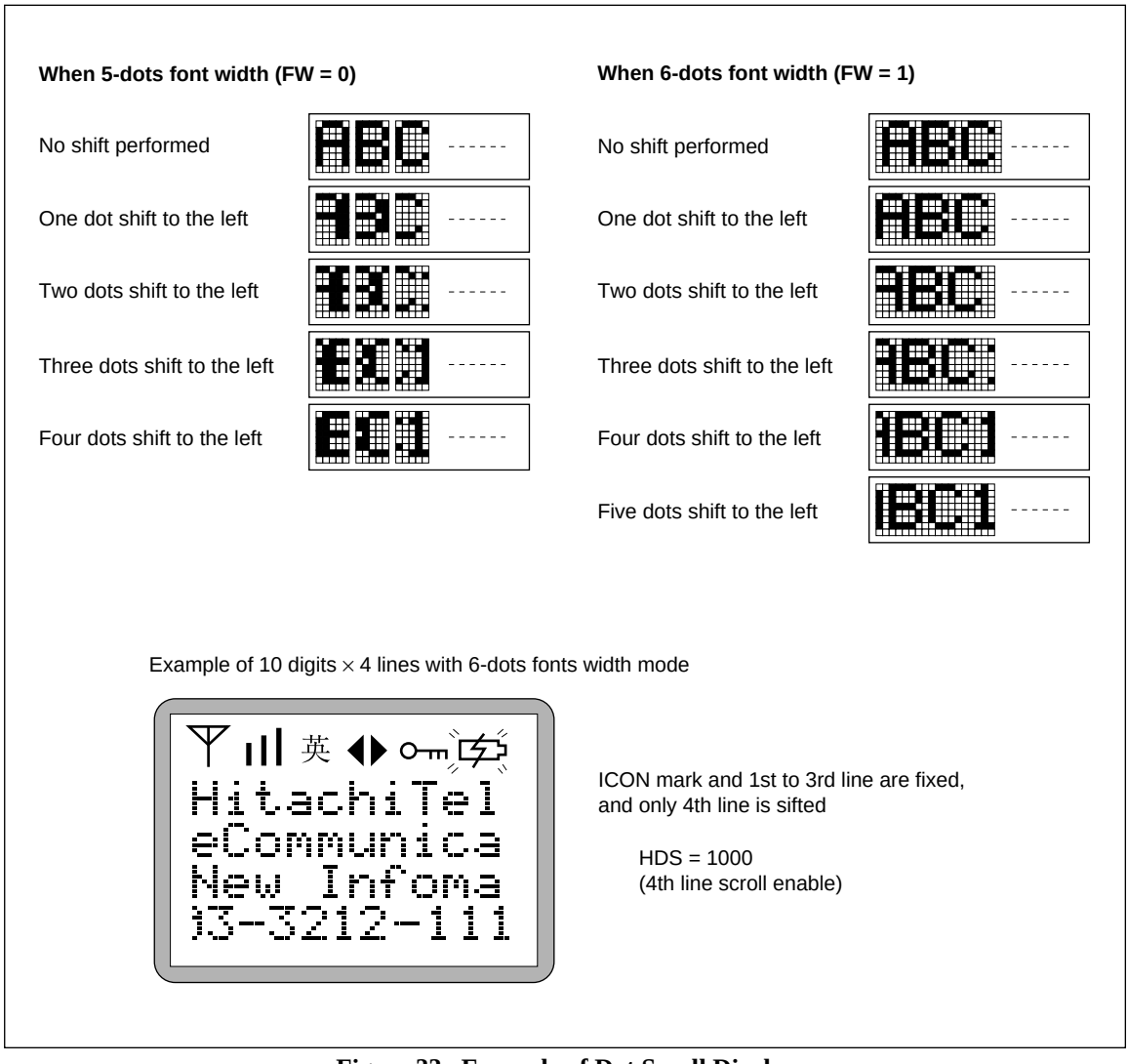


Figure 33 Example of Dot Scroll Display

6-dots font width mode (FW = 1)
4 line display mode (NW = 1)

	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	1	DL	N	**1**	BE	LP	Enable extension resistor.
2	0	0	0	0	0	1	**1**	**0**	**0**	**0**	4th line scroll enable.
3	0	0	1	0	**0**	**0**	**0**	**0**	**0**	**1**	One dot shift in 4th line to the left.
					CPU Wait						
4	0	0	1	0	**0**	**0**	**0**	**0**	**1**	**0**	Two dots shift in 4th line to the left.
					CPU Wait						
5	0	0	1	0	**0**	**0**	**0**	**0**	**1**	**1**	Three dots shift in 4th line to the left.
					CPU Wait						
6	0	0	1	0	**0**	**0**	**0**	**1**	**0**	**0**	Four dots shift in 4th line to the left.
					CPU Wait						
					⋮						
49	0	0	1	1	**1**	**0**	**1**	**1**	**1**	**1**	47 dots shift in 4th line to the left.
					CPU Wait						
50	0	0	1	0	**1**	**1**	**0**	**0**	**0**	**0**	48 dots shift in 4th line to the left.

Note: When perfoming a dot scroll with an extended driver, the maximum number or characters per line decreases by quantity set by the dot scroll. For example, when the maximum 24-dot scroll quantity (4 characters) is used with 6-dot font width and 4-line display, the maximum numbers of character is 20 – 4 = 16. Notice that in low power mode (LP = 1), display shift and dot scroll cannot be performed.

Figure 34 Method of Smooth Scroll Display

Low Power Mode

When the extension driver is not used (EXT = Low) with extension register enabled (RE = 1), the HD66712 enters low power mode by setting the low-power mode bit (LP) to 1. During low-power mode, as the internal operation clock is divided by 2 (2-line/4-line display mode) or by 4 (1-line display mode), the execution time of each instruction becomes two times or four times longer than normal. In addition, as the frame frequency decreases to 5/6, display quality might be affected.

In addition, since the display is not shifted in low power mode, display shift must be cleared with the return home instruction before setting low power mode. The amount of horizontal scroll must also be cleared (HDS = 000000). Moreover, because the display enters a shift state after clearing low-power mode, the home return instruction must be used to clear display shift at that time.

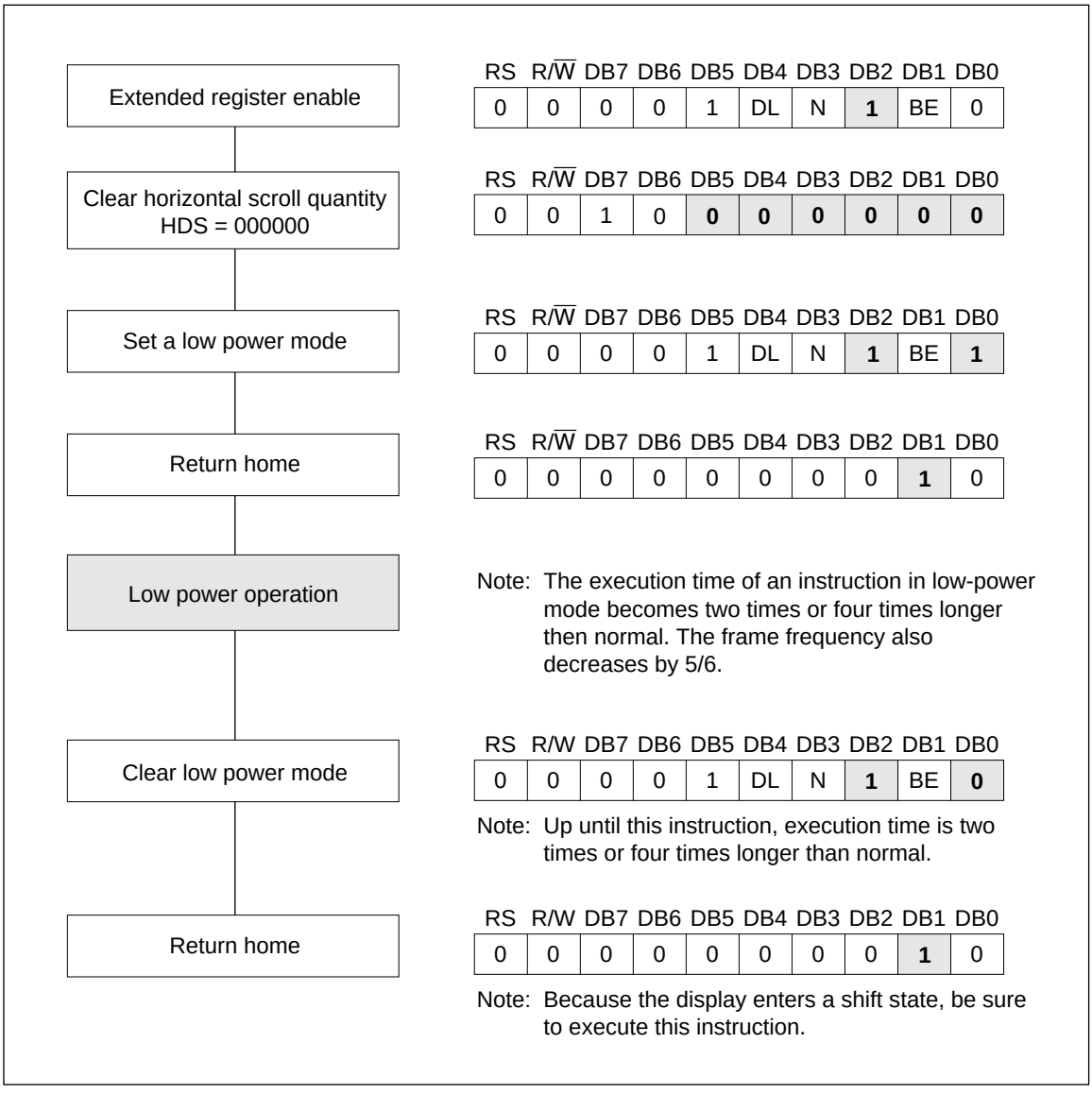


Figure 35 Usage of Low Power Mode

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +15.0	1, 2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	$0.2V_{CC}$	V	V_{CC} = 2.7 to 3.0 V	6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM) V_{LCD} = 4 V	13
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG) V_{LCD} = 4 V	13
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (D_0–D_7, RESET* pin)	–Ip	10	50	120	µA	V_{CC} = 3 V Vin = 0 V	
Power supply current	Icc	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	13.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	13.0	V	V_{CC}–V_5, 1/6.7 bias	16

Note: * Refer to Electrical Characteristics Notes following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	V_{ci} = 4.5 V, I_0 = 0.25 mA, C = 1 µF, f_{OSC} = 270 kHz T_a = 25°C	18, 19
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.7	—	V	V_{ci} = 2.7 V, I_0 = 0.25 mA, C = 1 µF, f_{OSC} = 270 kHz T_a = 25°C	18, 19
Input voltage	V_{Ci}	2.0	—	5.0	V	Vci ≤ V_{CC} Ta = 25°C	18, 19 20

Note: * Refer to Electrical Characteristics Notes following these tables.

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{rcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ, V_{CC} = 5 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

System Interface Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C[*3])

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 37
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 38
Serial clock (high level width)	t_{SCH}	400	—	—	ns	
Serial clock (low level width)	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	0	—	—		

System Interface Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C[*3])

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_{H}	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 37
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Sequence

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 38
Serial clock (high level width)	t_{SCH}	200	—	—	ns	
Serial clock (low level width)	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100	—	—		
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	0	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 39
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Reset Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

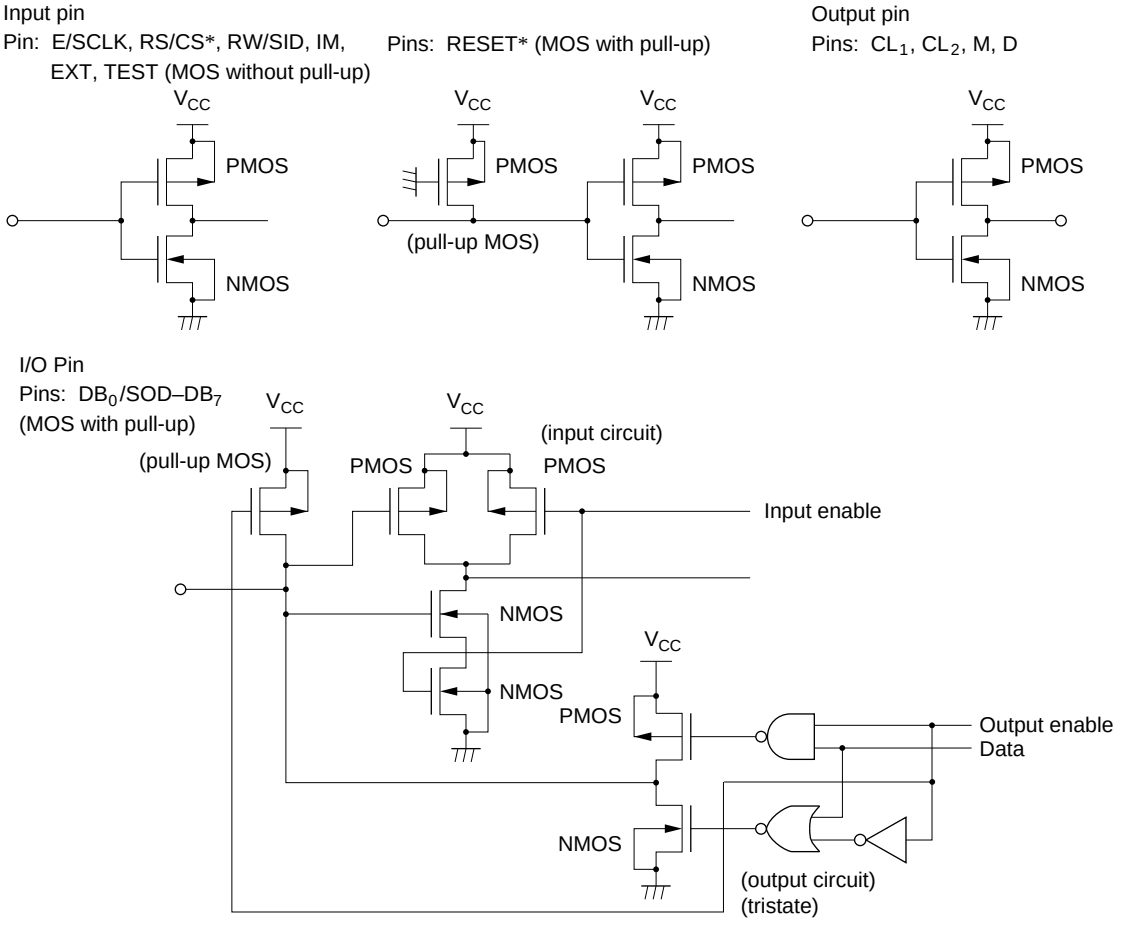
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 40

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 41
Power supply off time	t_{OFF}	1	—	—		

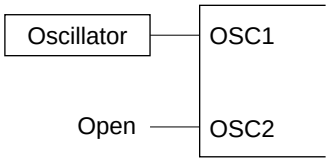
Electrical Characteristics Notes

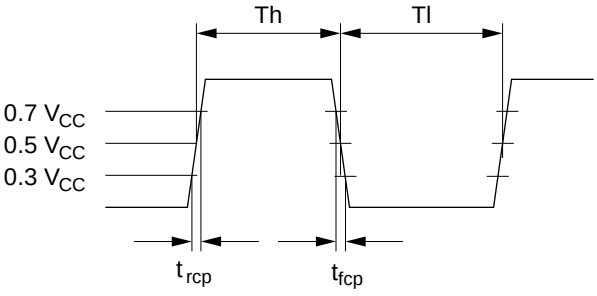
1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic are also exceeded, the LSI may malfunction or exhibit poor reliability.
2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.



6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

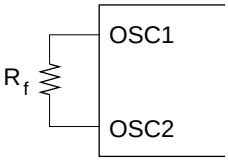
11. Applies only to external clock operation.





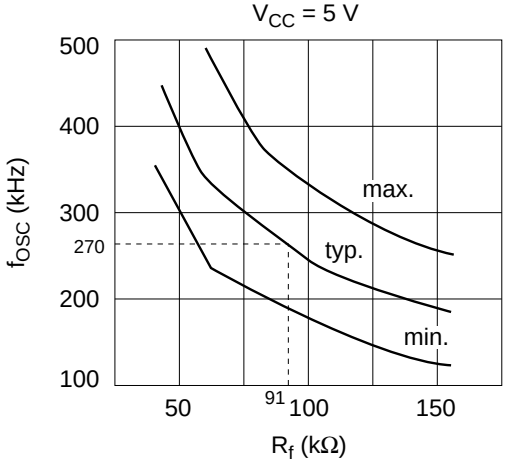
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

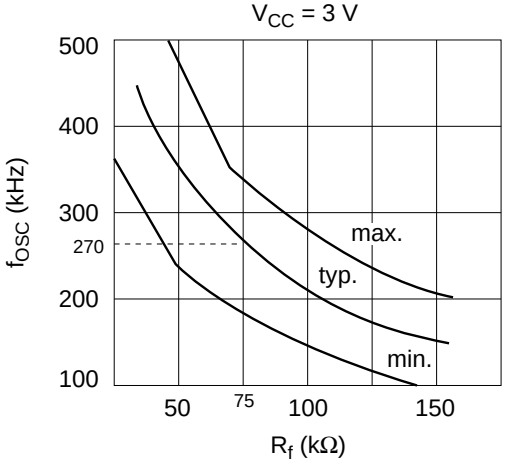
12. Applies only to the internal oscillator operation using oscillation resistor R_f.



R_f: 75 kΩ ± 2% (when V_{CC} = 3 V to 4 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 4 V to 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Referential data

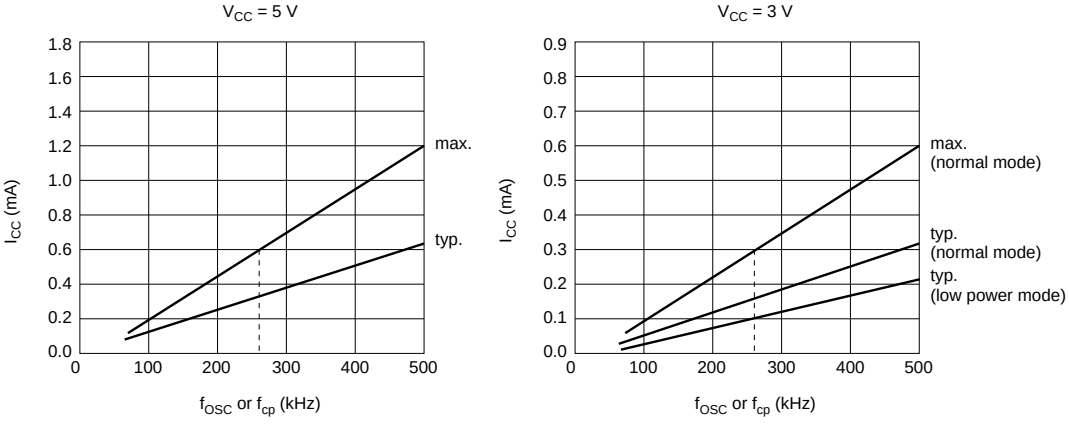




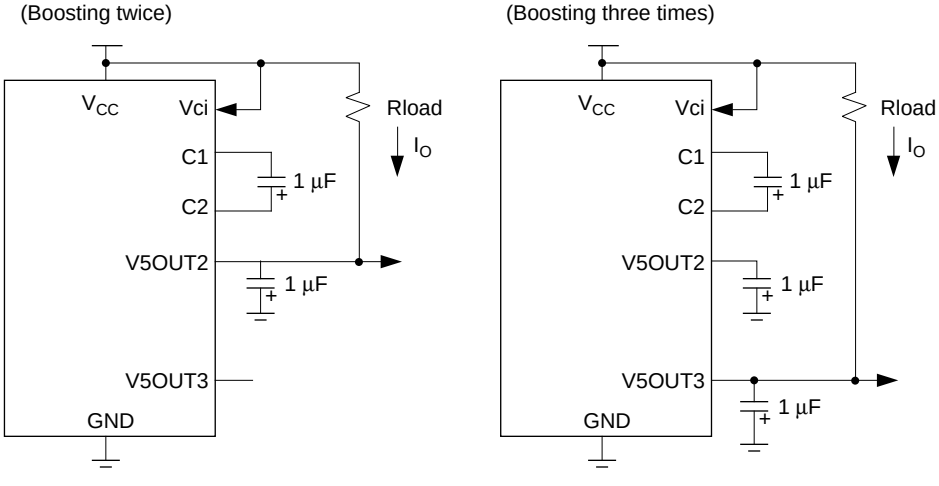
13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_0 to COM_{33}).

R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{60}).

14. The following graphs show the relationship between operation frequency and current consumption.



15. Applies to the OSC_1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.
17. The TEST pin must be fixed to ground, and the IM or EXT pin must also be connected to V_{CC} or ground.
18. Booster characteristics test circuits are shown below.



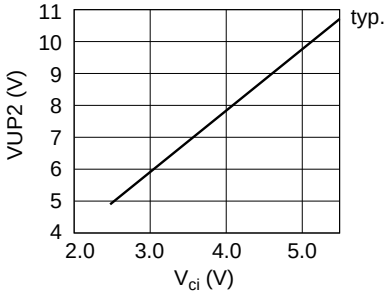
19. Reference data

The following graphs show the liquid crystal voltage booster characteristics.

VUP2 = V_{CC}–V5OUT2
VUP3 = V_{CC}–V5OUT3

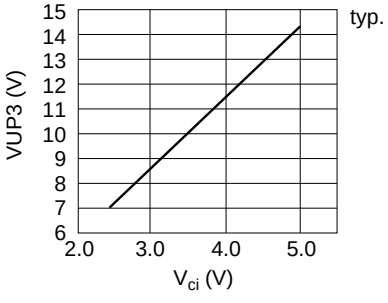
(1) VUP2, VUP3 vs V_{ci}

Boosting twice



Test condition: $V_{ci} = V_{CC}$, f_{cp} = 270 kHz,
T_a = 25°C, Rload = 25 kΩ

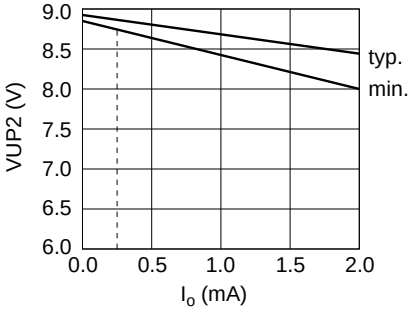
Boosting three times



Test condition: $V_{ci} = V_{CC}$, f_{cp} = 270 kHz,
Ta = 25°C, Rload = 25 kΩ

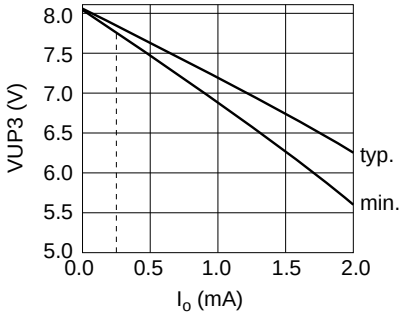
(2) VUP2, VUP3 vs I_o

Boosting twice



Test condition: $V_{ci} = V_{CC}$ = 4.5 V,
R_f = 91 kΩ, T_a = 25°C

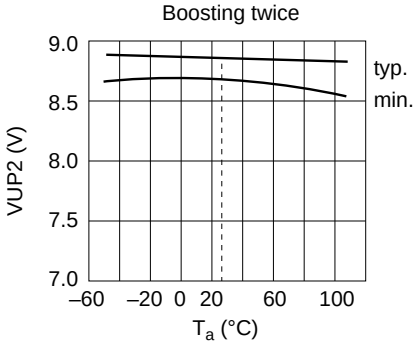
Boosting three times



Test condition: $V_{ci} = V_{CC}$ = 2.7 V,
R_f = 75 kΩ, T_a = 25°C

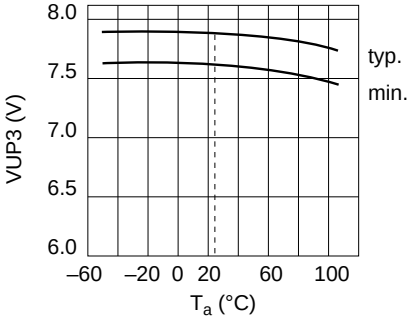
(3) VUP2, VUP3 vs T_a

Boosting twice



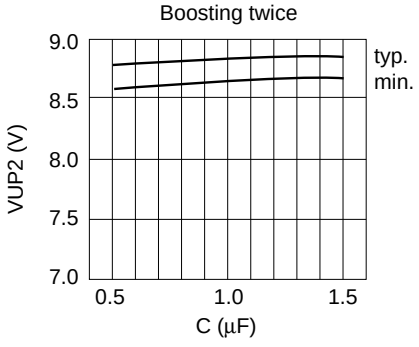
Test condition: $V_{ci} = V_{CC}$ = 4.5 V,
R_f = 91 kΩ, I_o = 0.25 mA

Boosting three times

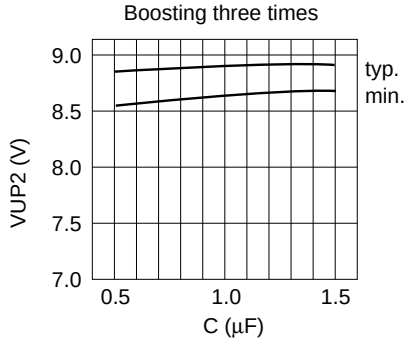


Test condition: $V_{ci} = V_{CC}$ = 2.7 V,
R_f = 75 kΩ, I_o = 0.25 mA

(4) VUP2, VUP3 vs capacitance



Test condition: $V_{ci} = V_{CC} = 4.5$ V,
$R_f = 91$ kΩ, $I_o = 0.25$ mA



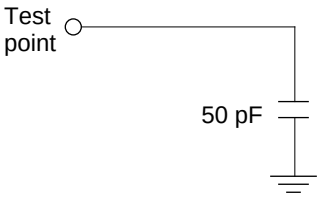
Test condition: $V_{ci} = V_{CC} = 2.7$ V,
$R_f = 75$ kΩ, $I_o = 0.25$ mA

20. Must maintain (“High”) $V_{CC} \geq V_{ci}$ (“Low”).

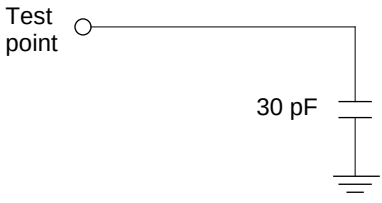
Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB0–DB7, SOD



Segment extension signals: CL1, CL2, D, M



Timing Characteristics

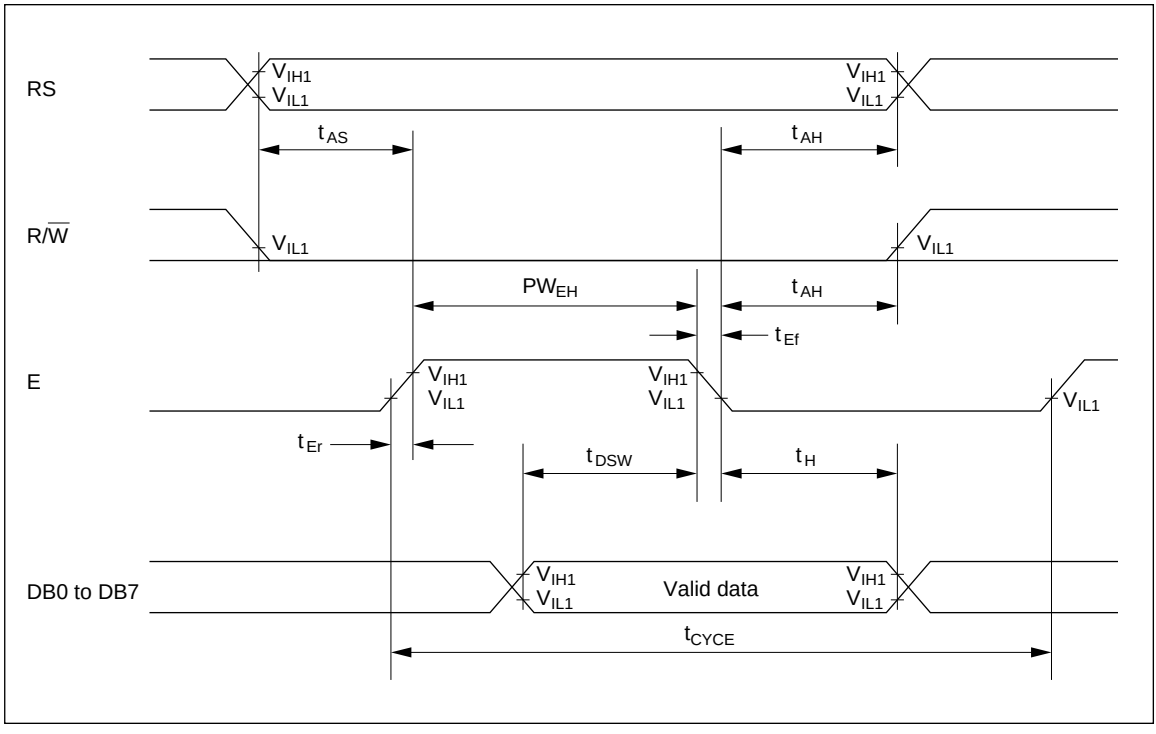


Figure 36 Bus Write Operation

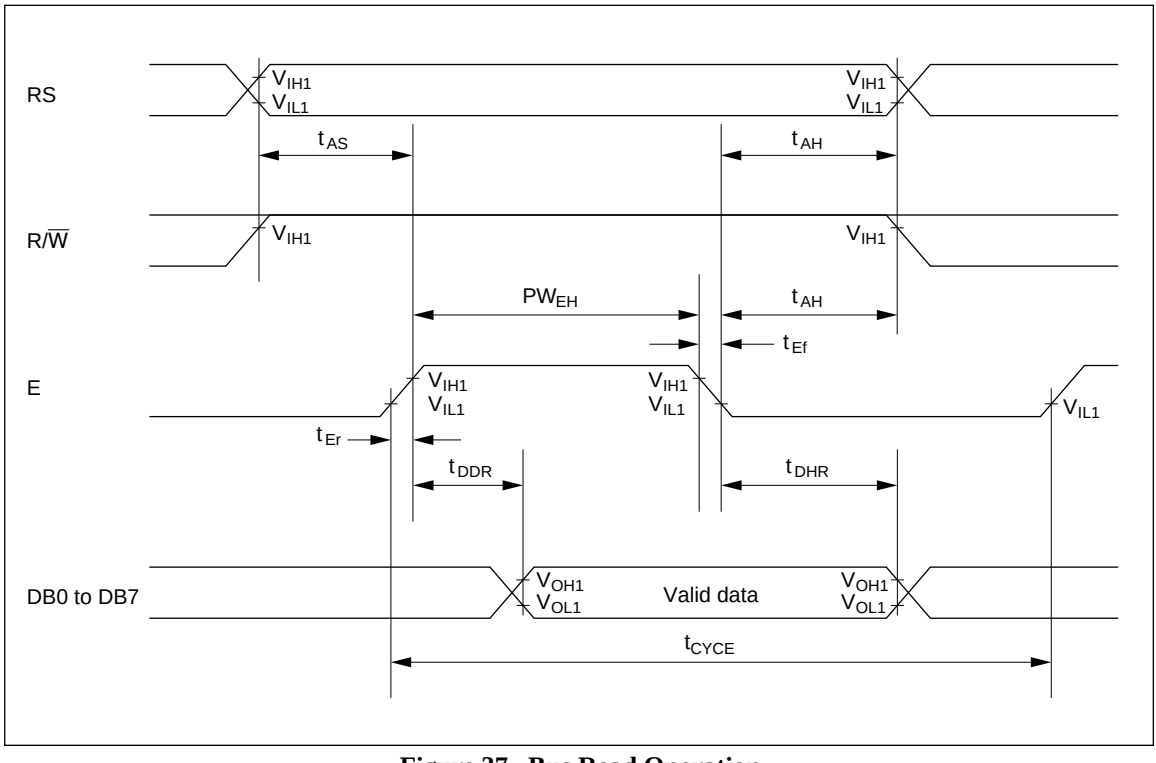


Figure 37 Bus Read Operation

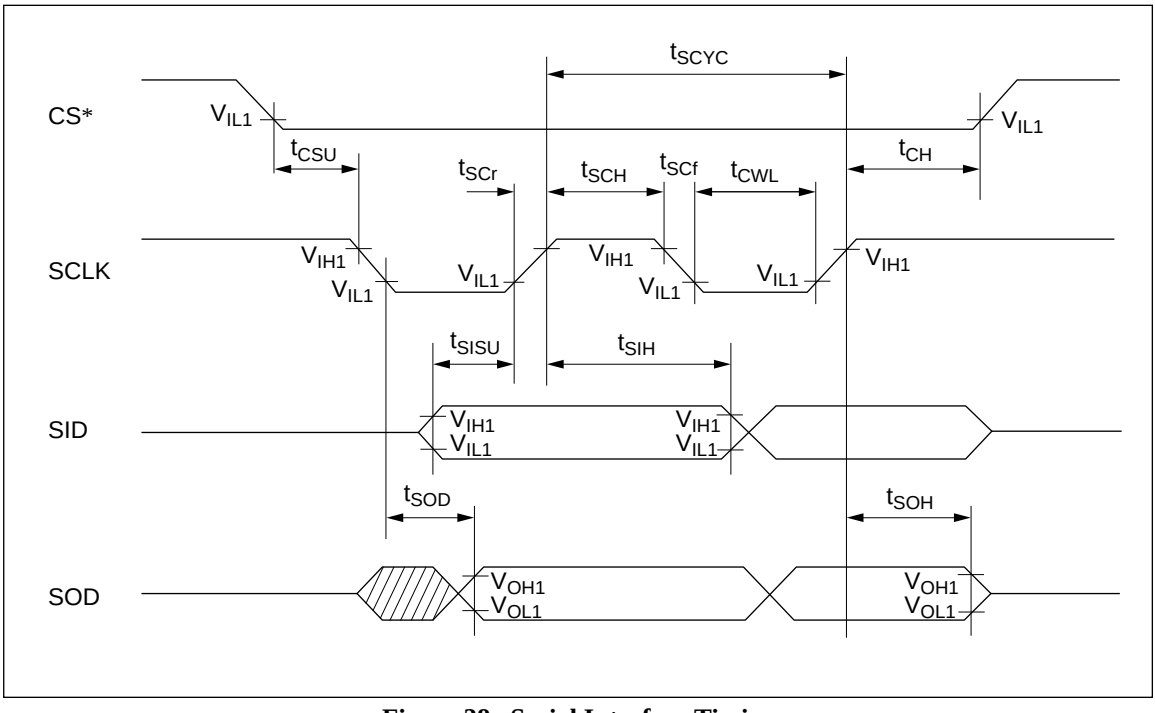


Figure 38 Serial Interface Timing

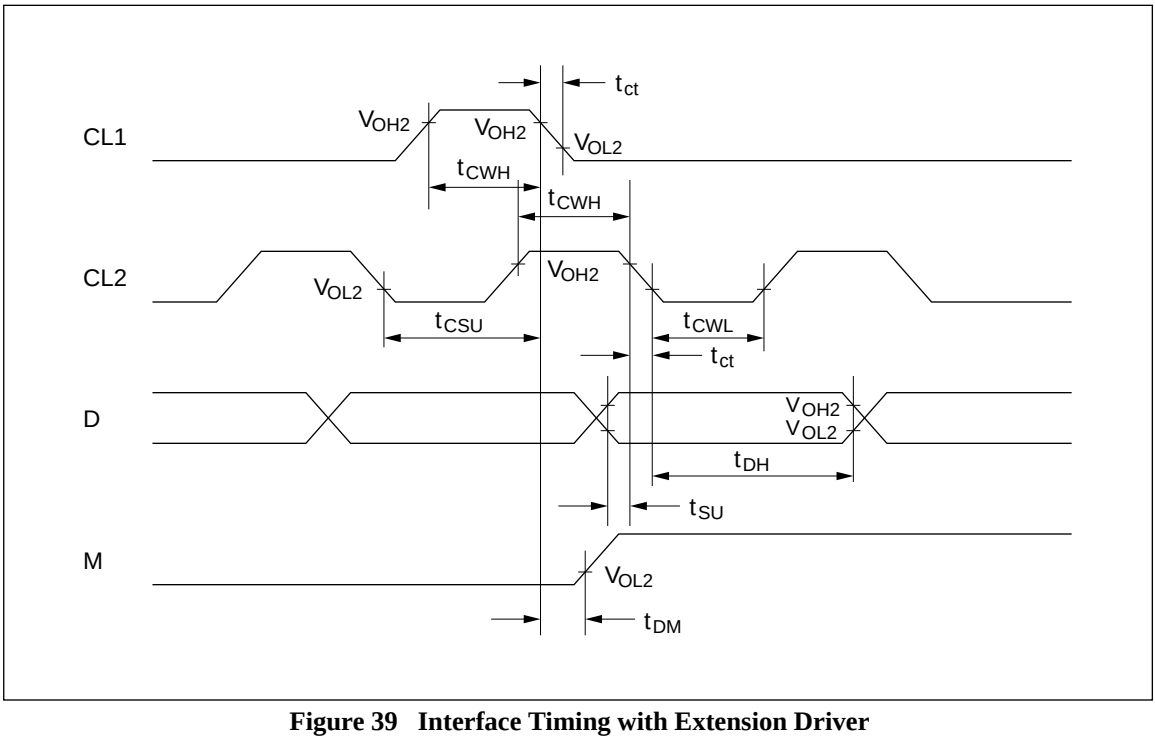
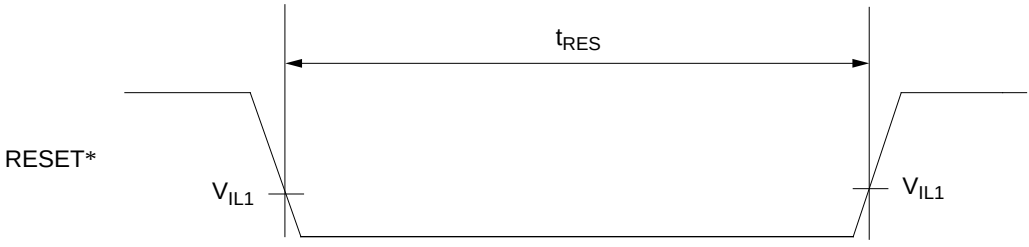
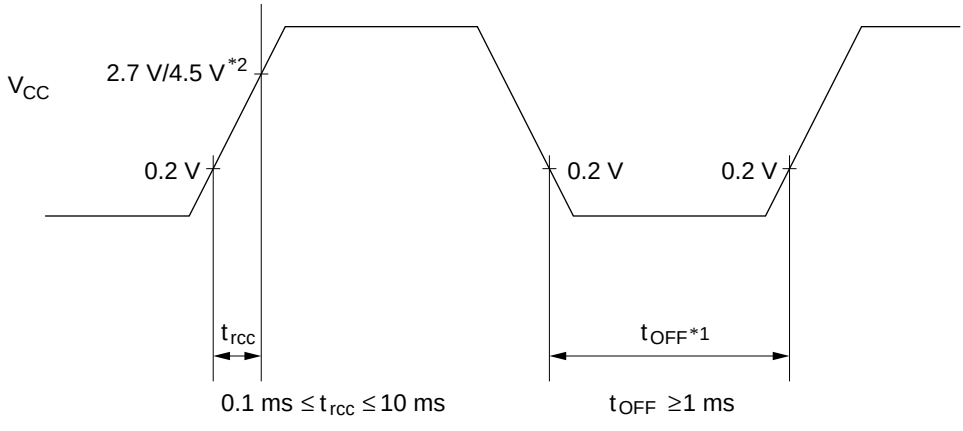


Figure 39 Interface Timing with Extension Driver



Note: When power is supplied, initializing by the internal reset circuit has priority. Accordingly, the above RESET* input is ignored during internal reset period.

Figure 40 Reset Timing



Notes:
1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, initialized by instruction. (Refer to the Initializing by Instruction section.)

Figure 41 Power Supply Sequence

HD66720 (LCD-II/K8)

(Panel Controller/Driver for Dot-Matrix Liquid Crystal Display with Key-Matrix)

Preliminary

HITACHI

Description

The HD66720 dot-matrix liquid crystal display controller (LCD) and driver LSI incorporates a key-scan function and an LED display function, and displays alphanumeric character and symbols. A single HD66720 is capable of displaying a single 10-character line or two 8-character lines. In addition, a single line of up to 40 characters can be displayed with extension drivers.

Since the HD66720 incorporates a 5 × 6 matrix key scan circuit and two LED drive circuits, it can control front panels of telephone, car stereos, audio equipment, printers, or facsimiles with a single chip. A three-line clock synchronous serial transfer method is adopted for interfacing with a microcomputer, which greatly decreases the number of interface signals and makes it easy to miniaturize systems.

This LSI is especially suitable for panels which can display five European languages (English, French, German, Italian, and Spanish), as used in new media products including car tuners for the radio data system (RDS), mini disc players (MD), and digital compact cassette players (DCC), personal handly phone, cellular phone.

Features

- Control and drive of a dot matrix LCD with built-in scanning
- Wide field-of-division display with low duty cycle of 1/9 (1 line) and 1/17 (2 lines)
- 10-character single line (5 × 8-dot font) and 50-segment display with a single chip (two 8-character line display by setting a register)
- Maximum 40-character single line display with extension drivers (see list 1)
- Built-in key scan matrix buffer circuit: 5 × 6 (30 keys) input (at strobe cycle: 5 ms to 40 ms, f_{osc} = 160 kHz)
- Wake-up function with IRQ signal after key stroke
- Two general purpose output ports (for LED displays, etc.)
- Serial bus interface: Three-line clock synchronous serial transfer
- Booster for liquid crystal drive voltage: Two/three times power supply
- Maximum 40-character display RAM
- Character generator ROM: 240 5 × 8-dot characters
- Character generator RAM: 8 user characters
- 80-segment RAM
- Horizontal smooth scroll: Displayed line selection and displayed character selection scroll possible
- Oscillator (external resistor needed) and power-on reset circuit incorporated
- Wide range of operating power supply voltage: 2.7 to 5.5 V
  Liquid crystal display voltage: 3.0 to 11.0 V
- QFP 1420-100 (0.65-mm pitch), TQFP 1414-100 (0.5-mm pitch), bare-chip

Hitachi semiconductor

List 1 Programmable Duty Cycles

		5-Dot Font Width					
		Single-Chip Operation		With Single HD44100R		Maximum Display Extension	
Number of Lines	Duty Ratio	Displayed Characters	Segments	Displayed Characters	Segments	Displayed Characters	Segments
1	1/9	10	50	18	80	40	80
2	1/17	8	42	16	80	20	82

		6-Dot Font Width					
		Single-Chip Operation		With Single HD44100R		Maximum Display Extension	
Number of Lines	Duty Ratio	Displayed Characters	Segments	Displayed Characters	Segments	Displayed Characters	Segments
1	1/9	8	50	15	90	40	96
2	1/17	7	42	13	82	20	96

List 2 Ordering Information

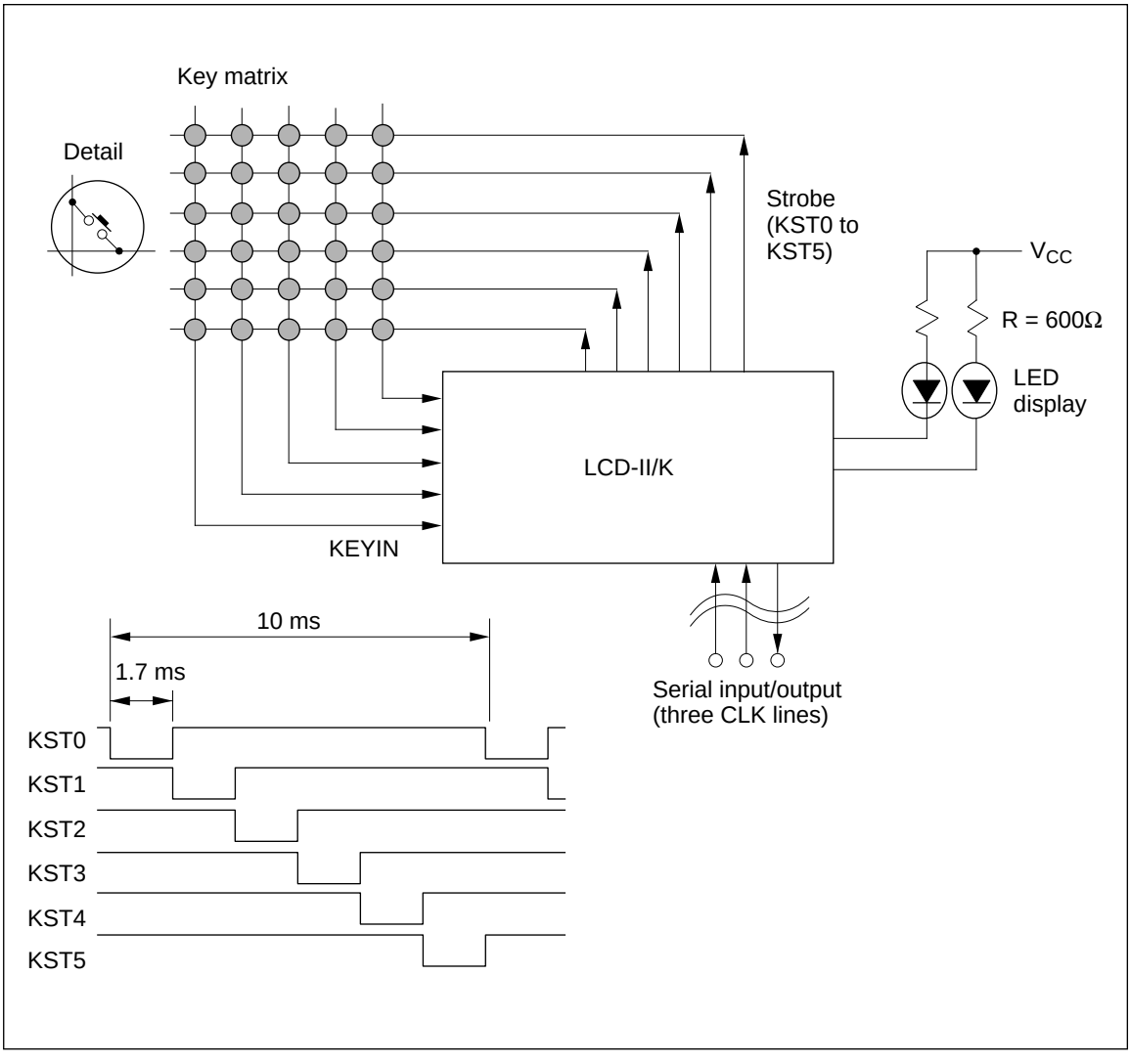
Type No.	Package	CGROM
HD66720A03FS	FP-100A	Japanese + European font
HD66720A03TF	TFP-100B	
HCD66720A03	Chip	

LCD-II Family Comparison

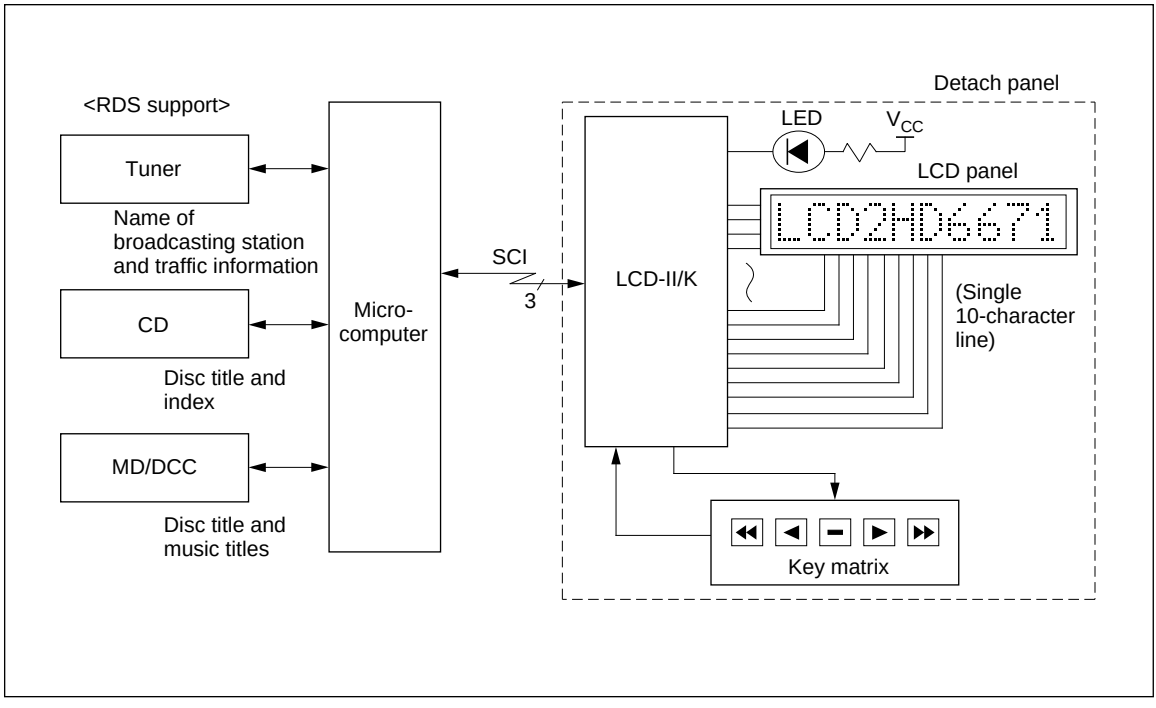
Item	LCD-II HD44780U	LCD-II/E20 HD66702R	LCD-II/F8 HD66710	LCD-II/F12 HD66712	LCD-II/K8 HD66720
Power supply voltage	2.7 V to 5.5 V	5 V ± 10% (standard), 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltage	3.0 V to 11.0 V	3.0 V to 8.3 V	3.0 V to 13.0 V	3.0 V to 13.0 V	3.0 V to 11.0 V
Maximum display characters per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines	10 characters × 1 line/ 8 characters × 2 lines
Segment display	None	None	40 segments	60 segments (80 segments with extension)	50 segments (80 segments with extension)
Display duty cycle	1/8, 1/11, 1/16	1/8, 1/11, 1/16	1/17, 1/33	1/17, 1/33	1/9, 1/17
Key scan circuit	None	None	None	None	5 × 6 (30 circuits)
LED display circuit	None	None	None	None	2 circuits
CGROM	9,920 bits (208 5 × 8-dot characters and 32 5 × 10-dot characters)	7,200 bits (160 5 × 7-dot characters and 32 5 × 10-dot characters)	9,600 bits (240 5 × 8-dot characters)	9,600 bits (240 5 × 8-dot characters)	9,600 bits (240 5 × 8-dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes	40 bytes
SEGRAM	None	None	8 bytes	16 bytes	16 bytes
Segment signal	40 signals	100 signals	40 signals	60 signals	50 signals (42 signals)
Common signal	16 signals	16 signals	33 signals	34 signals	9 signals (17 signals)
Liquid crystal waveform	A	B	B	B	B

Item		LCD-II HD44780U	LCD-II/E20 HD66702R	LCD-II/F8 HD66710	LCD-II/F12 HD66712	LCD-II/K8 HD66720
Clock generator	Clock source	External resistor External clock input	External resistor External clock input	External resistor External clock input	External resistor External clock input	External resistor External clock input
	Rf oscillation frequency	270 kHz ± 30%	320 kHz ± 30%	270 kHz ± 30%	270 kHz ± 30%	160 kHz ± 30%
	Frame frequency	59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle	70 to 130 Hz for 1/8 and 1/16 duty cycles; 51 to 95 Hz for 1/11 duty cycle	56 to 103 Hz for 1/7 duty cycles; 57 to 106 Hz for 1/33 duty cycle	56 to 103 Hz for 1/7 duty cycles; 57 to 106 Hz for 1/33 duty cycle	58 to 108 Hz for 1/9 duty cycles; 62 to 115 Hz for 1/17 duty cycle
	Rf resistance	91 kΩ for 5-V operation; 75 kΩ for 3-V operation	68 kΩ for standard version; 56 kΩ for L version	91 kΩ for 5-V operation; 75 kΩ for 3-V operation	91 kΩ for 5-V operation; 75 kΩ for 3-V operation	200 kΩ for 5-V operation; 160 kΩ for 3-V operation
Liquid crystal display voltage booster circuit		None	None	2–3 times step-up circuit	2–3 times step-up circuit	2–3 times step-up circuit
Extension driver control signal		Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal	Independent control signal
Reset function		Internal reset	Internal reset	Internal reset	Internal reset and input	Internal reset and input
Instructions		LCD-II (HD44780)	Fully compatible with the LCD-II	Upwardly compatible with the LCD-II	Upwardly compatible with the LCD-II	Upwardly compatible with the LCD-II
Horizontal scroll		Character unit	Character unit	Dot unit	Dot unit and line unit scroll	Dot unit and line unit scroll
Number of displayed lines		1 or 2	1 or 2	1, 2, or 4	1, 2, or 4	1 or 2
Low power mode		None	None	Available	Available	Available
Bus interface		4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial/4 bits/ 8 bits	Serial
CPU bus timing		2 MHz for 5-V operation; 1 MHz for 3-V operation	1 MHz	2 MHz for 5-V operation; 1 MHz for 3-V operation	2 MHz for 5-V operation; 1 MHz for 3-V operation	2 MHz for 5-V operation; 1 MHz for 3-V operation
Package		QFP-1420-80 TQFP-1414-80 80-pin bare chip	LQFP-2020-144 144-pin bare chip	QFP-1420-100 TQFP-1414-100 100-pin bare chip	QFP-1420-128 TCP-128 128-pin bare chip	QFP-1420-100 TQFP-1414-100 100-pin bare chip

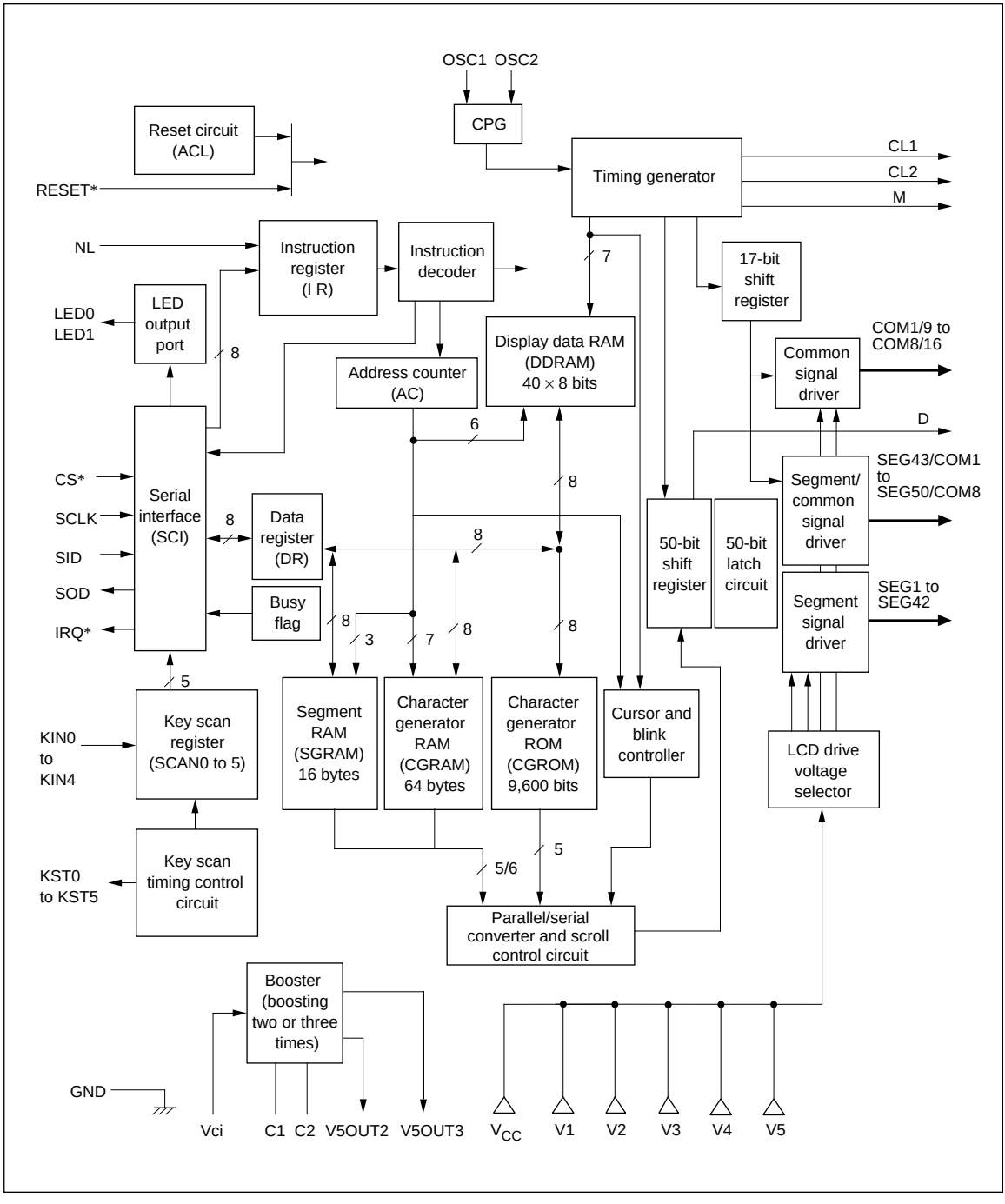
Key Input Sampling and LED Display



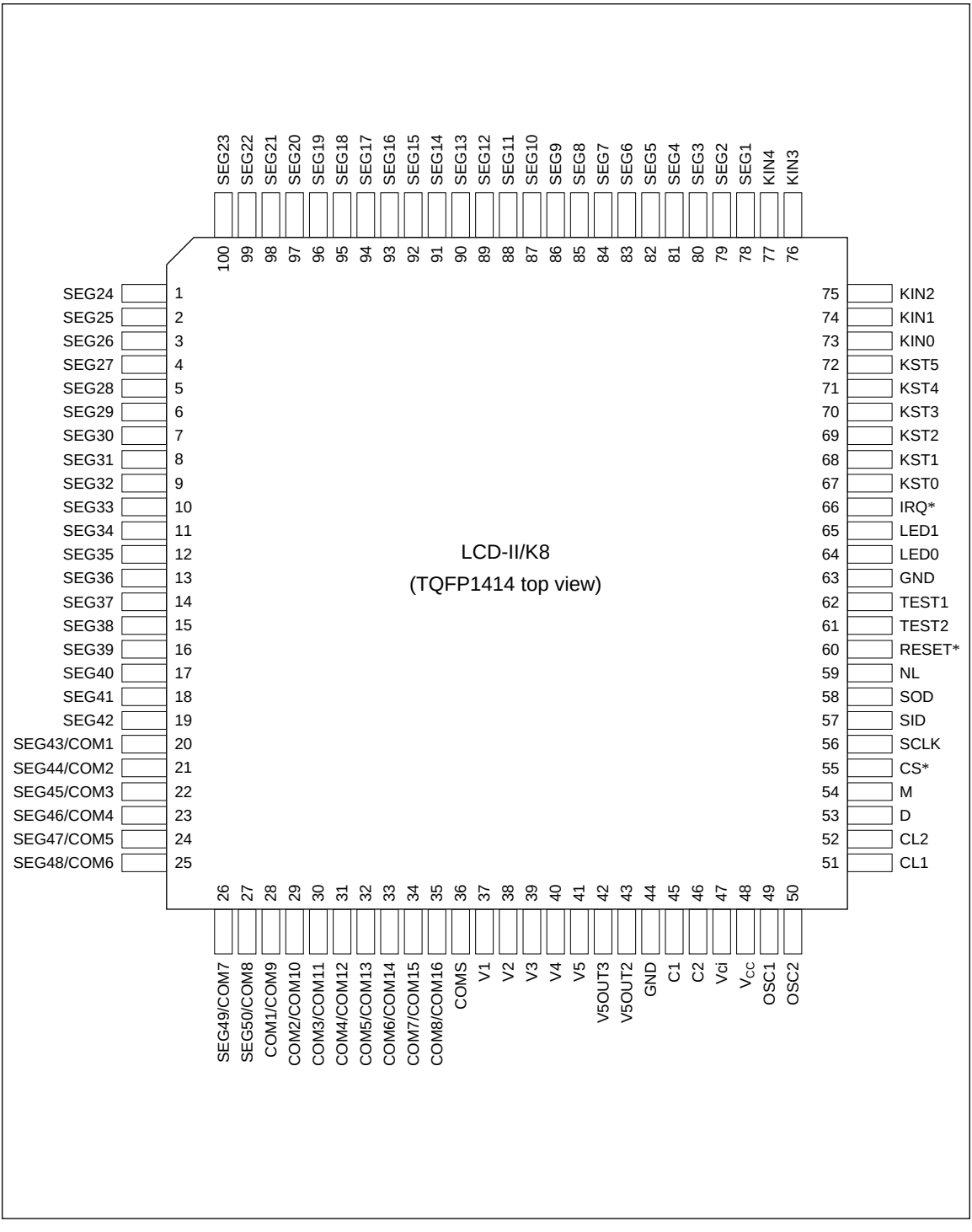
Application Example for Car Stereo

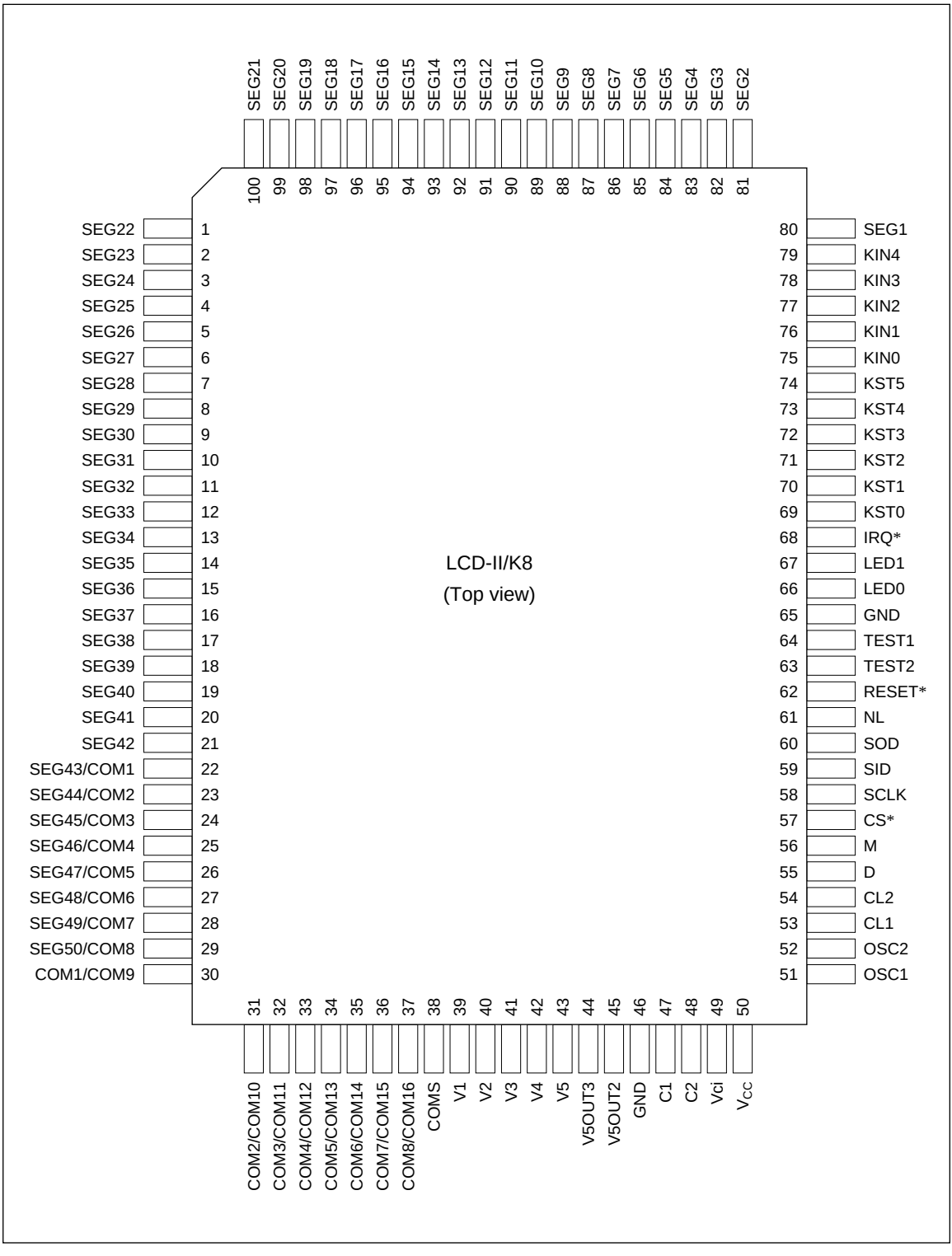


Block Diagram

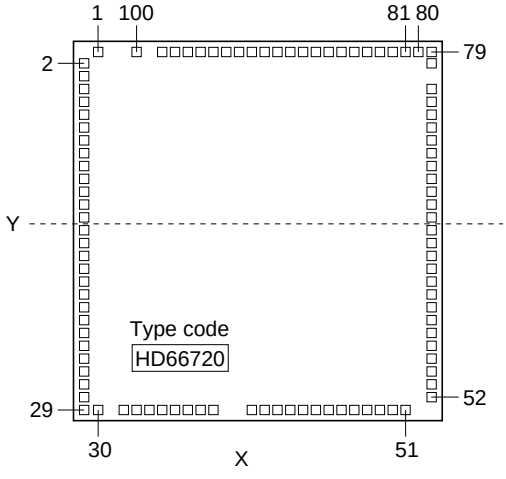


Pin Arrangement




LCD-II/K8
(Top view)
1 SEG22
2 SEG23
3 SEG24
4 SEG25
5 SEG26
6 SEG27
7 SEG28
8 SEG29
9 SEG30
10 SEG31
11 SEG32
12 SEG33
13 SEG34
14 SEG35
15 SEG36
16 SEG37
17 SEG38
18 SEG39
19 SEG40
20 SEG41
21 SEG42
22 SEG43/COM1
23 SEG44/COM2
24 SEG45/COM3
25 SEG46/COM4
26 SEG47/COM5
27 SEG48/COM6
28 SEG49/COM7
29 SEG50/COM8
30 COM1/COM9
31 COM2/COM10
32 COM3/COM11
33 COM4/COM12
34 COM5/COM13
35 COM6/COM14
36 COM7/COM15
37 COM8/COM16
38 COMS
39 V1
40 V2
41 V3
42 V4
43 V5
44 V5OUT3
45 V5OUT2
46 GND
47 C1
48 C2
49 Vci
50 VCC
51 OSC1
52 OSC2
53 CL1
54 CL2
55 D
56 M
57 CS*
58 SCLK
59 SID
60 SOD
61 NL
62 RESET*
63 TEST2
64 TEST1
65 GND
66 LED0
67 LED1
68 IRQ*
69 KST0
70 KST1
71 KST2
72 KST3
73 KST4
74 KST5
75 KIN0
76 KIN1
77 KIN2
78 KIN3
79 KIN4
80 SEG1
81 SEG2
82 SEG3
83 SEG4
84 SEG5
85 SEG6
86 SEG7
87 SEG8
88 SEG9
89 SEG10
90 SEG11
91 SEG12
92 SEG13
93 SEG14
94 SEG15
95 SEG16
96 SEG17
97 SEG18
98 SEG19
99 SEG20
100 SEG21

HCD66720



Chip size (XxY): 5.60 mm × 6.0 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X x Y): 100 μm × 100 μm

(Unit: μm)

Pad No.	Function	Coordinate X	Coordinate Y
1	SEG22	–2400	2877
2	SEG23	–2677	2700
3	SEG24	–2677	2500
4	SEG25	–2677	2300
5	SEG26	–2677	2100
6	SEG27	–2677	1900
7	SEG28	–2677	1700
8	SEG29	–2677	1500
9	SEG30	–2677	1300
10	SEG31	–2677	1100
11	SEG32	–2677	900
12	SEG33	–2677	700
13	SEG34	–2677	500
14	SEG35	–2677	300
15	SEG36	–2677	100
16	SEG37	–2677	–100
17	SEG38	–2677	–300
18	SEG39	–2677	–500
19	SEG40	–2677	–700
20	SEG41	–2677	–900
21	SEG42	–2677	–1100
22	SEG43/COM1	–2677	–1300
23	SEG44/COM2	–2677	–1500
24	SEG45/COM3	–2677	–1700
25	SEG46/COM4	–2677	–1900
26	SEG47/COM5	–2677	–2100
27	SEG48/COM6	–2677	–2300
28	SEG49/COM7	–2677	–2677
29	SEG50/COM8	–2677	–2877
30	COM1/COM9	–2400	–2877
31	COM2/COM10	–1900	–2877
32	COM3/COM11	–1700	–2877
33	COM4/COM12	–1500	–2877
34	COM5/COM13	–1300	–2877

Pad No.	Function	Coordinate X	Coordinate Y
35	COM6/COM14	–1100	–2877
36	COM7/COM15	–900	–2877
37	COM8/COM16	–700	–2877
38	COMS	–500	–2877
39	V1	–150	–2853
40	V2	100	–2853
41	V3	300	–2853
42	V4	500	–2853
43	V5	800	–2853
44	V5OUT3	1020	–2809
45	V5OUT2	1200	–2809
46	GND	1400	–2790
47	C1	1600	–2853
48	C2	1800	–2809
49	VCI	2000	–2809
50	VCC	2200	–2853
51	OSC1	2400	–2853
52	OSC2	2653	–2700
53	CL1	2653	–2500
54	CL2	2653	–2300
55	D	2653	–2100
56	M	2653	–1900
57	CS*	2653	–1700
58	SCLK	2653	–1500
59	SID	2653	–1300
60	SOD	2653	–1100
61	NL	2653	–900
62	RESET*	2653	–700
63	TEST2	2653	–500
64	TEST1	2653	–300
65	GND	2653	–30
66	LED0	2653	174
67	LED1	2653	350
68	IRQ*	2653	540

Pad No.	Function	Coordinate X	Coordinate Y
69	KST0	2653	730
70	KST1	2653	920
71	KST2	2653	1110
72	KST3	2653	1300
73	KST4	2653	1500
74	KST5	2653	1700
75	KIN0	2653	1900
76	KIN1	2653	2100
77	KIN2	2653	2300
78	KIN3	2653	2653
79	KIN4	2653	2853
80	SEG1	2400	2877
81	SEG2	1900	2877
82	SEG3	1700	2877
83	SEG4	1500	2877
84	SEG5	1300	2877
85	SEG6	1100	2877
86	SEG7	900	2877
87	SEG8	700	2877
88	SEG9	500	2877
89	SEG10	300	2877
90	SEG11	100	2877
91	SEG12	–100	2877
92	SEG13	–300	2877
93	SEG14	–500	2877
94	SEG15	–700	2877
95	SEG16	–900	2877
96	SEG17	–1100	2877
97	SEG18	–1300	2877
98	SEG19	–1500	2877
99	SEG20	–1700	2877
100	SEG21	–1900	2877

Pin Functions

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
CS*	1	I	MPU	Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
SCLK	1	I	MPU	Acts as a serial clock input (receive).
SID	1	I	MPU	Inputs serial data during serial mode.
IRQ*	1	O	MPU	Generates key scan interrupt signal.
SOD	1	O	MPU	Outputs (transmits) serial data during serial mode. Open this pin if reading (transmission) is not performed.
SEG_1 to SEG_{42}	42	O	LCD	Acts as a segment output signal.
SEG_{43}/ COM_1 to SEG_{50}/ COM_8	8	O	LCD	Acts as segment output during 1-line display mode. Acts as common output during 2-line display mode.
COM_1/ COM_9 to COM_8/ COM_{16}	8	O	LCD	Acts as common output during 1-line display mode. Acts as common output during 2-line display mode.
COMS	1	O	LCD	Common output signal for segment (icon).
CL1	1	O	Extension driver	Outputs the extension driver latch pulse.
CL2	1	O	Extension driver	Outputs the extension driver shift clock.
D	1	O	Extension driver	Outputs extension driver data; data from the 51st dot on is output during single-line display, and data from the 43rd dot on is output during two-line display.
M	1	O	Extension driver	Outputs the extension driver AC signal.
KST0* to KST5*	6	O	Key matrix	Generates strobe signals for latching data from the key matrix at specific time intervals.
KIN0* to KIN4*	5	I	Key matrix	Samples key state from key matrix synchronously with strobe signals.
LED0* to LED1*	2	O	LEDs	LED display control signals; can also be used as a general output port.
V1 to V5	5	—	Power supply	Power supply for LCD drive V_{CC} –V5 = 11 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +2.7 V to +5.5 V, GND: 0 V
OSC1/OSC2	2	—	Oscillation resistor clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC1.

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Keep this voltage within the range: 2.0 V to 4.5 V without exceeding V_{CC}.
V5OUT2	1	O	V5 pin/ Booster capacitor	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, the same capacitance as that of C1–C2 should be connected here.
V5OUT3	1	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitor	External capacitor should be connected here when using the booster.
RESET*	1	I	—	Reset pin. When active (low), this pin turns the display off and initializes the registers.
NL	1	I	—	Number of display lines. One line is displayed when this pin is low (1/9 duty), and two lines are displayed when this pin is high (1/17 duty).
TEST	2	I	—	Test pin. Should be wired to ground.

Block Function

System Interface

The HD66720 interfaces with the system through a three-line clock-synchronous serial method. This greatly decreases the number of interface connections with the MPU because all data transmission/reception, such as setting registers, writing data to RAM, and reading key-scan data can be performed with three control signals.

The HD66720 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEG RAM). The IR can only be written to by the MPU, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM, CG RAM, or SEG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEG RAM at the next address is sent to the DR for the next read from the MPU.

These two registers can be selected by the RS bit in start byte data in synchronized serial interface (table 2). For detail, refer to Transferring Serial Data.

Busy Flag (BF)

When the busy flag is 1, the HD66720 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output from DB7. The next instruction must be written after ensuring that the busy flag is 0.

Key Scan Register (SCAN0 to SCAN5)

Scanning from the key matrix senses the key state at the rising edge of key strobe signals (KST0 to KST5) output from the HD66720. These strobe signals sample 5 states: KIN0 to KIN4, enabling key scan of 30 types.

Key states KIN0 to KIN4 sampled by key strobe signal KST0 is latched to register SCAN0. In the same way, data sampled with strobe signals KST1 to KST5 are latched to registers SCAN1 to SCAN5, respectively. For details, refer to Key Scan Control.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and key scan register (DB_0 to DB_4)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEG RAM, the AC is automatically incremented by 1 (decremented by 1).

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 40 × 8 bits, or 40 characters. The area in display data RAM (DD RAM) that is not used for display can be used as buffer data RAM when scrolling.

The DD RAM address (ADD) is set in the address counter (AC) as a hexadecimal number, as shown in figure 1.

The relationship between DD RAM addresses and positions on the liquid crystal display is described and shown on the following pages for a variety of cases.

- 1-line display (NL = low)

  — Case 1: When there are fewer than 40 display characters, the display begins at the beginning of DD RAM. For example, when 10 5-dot font-width characters are displayed using one HD66720, the display is generated as shown in figure 3.

  When a display shift is performed, the DD RAM addresses shift as shown.

  When 8 6-dot font-width characters are displayed using one HD66720, the display is generated as shown in figure 3.

  When a display shift is performed, the DD RAM addresses shift as shown.

  — Case 2: Figure 4 shows the case where the HD66720 and the 40-output extension driver are used to display 15 6-dot font-width characters.

  When a display shift is performed, the DD RAM addresses shift as shown in the figure.

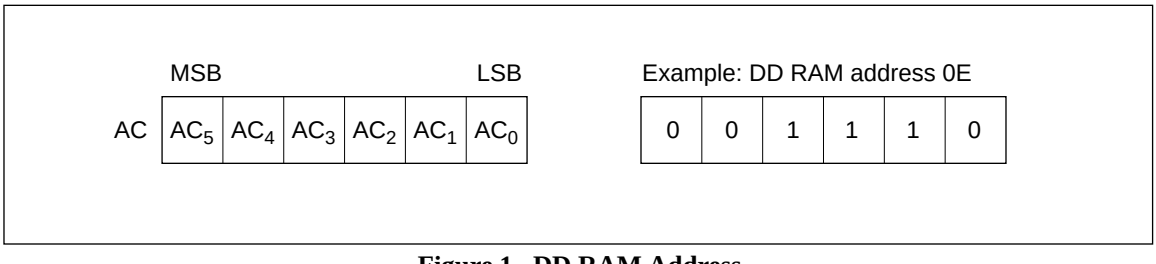


Figure 1 DD RAM Address

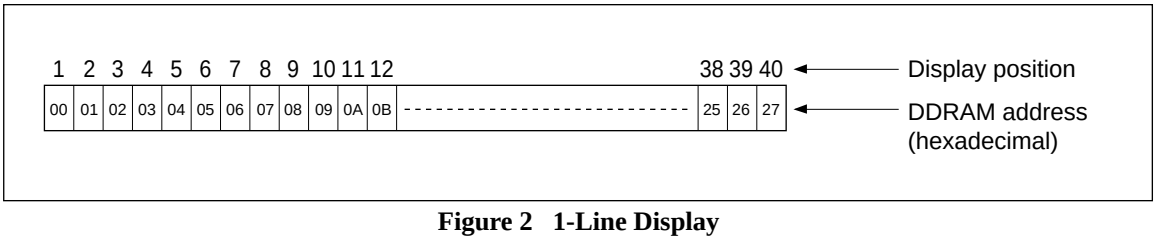


Figure 2 1-Line Display

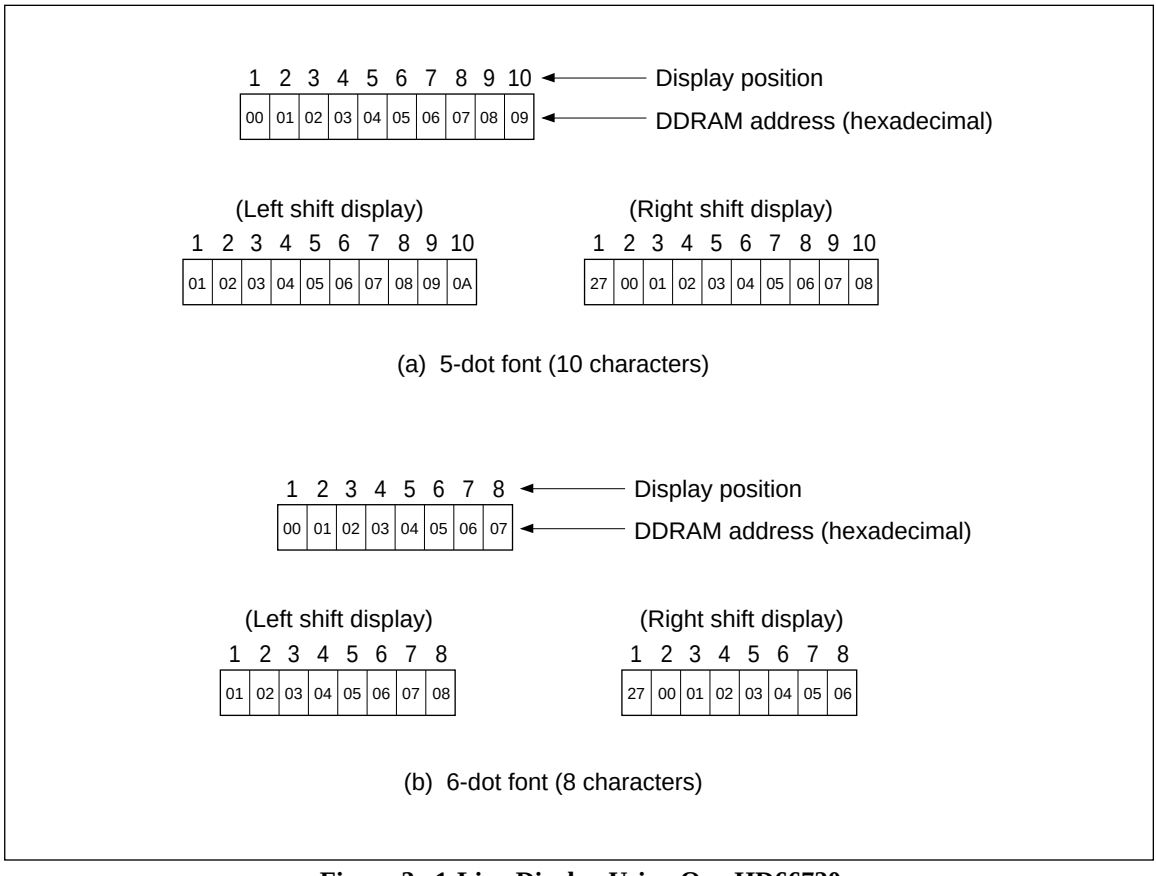


Figure 3 1-Line Display Using One HD66720

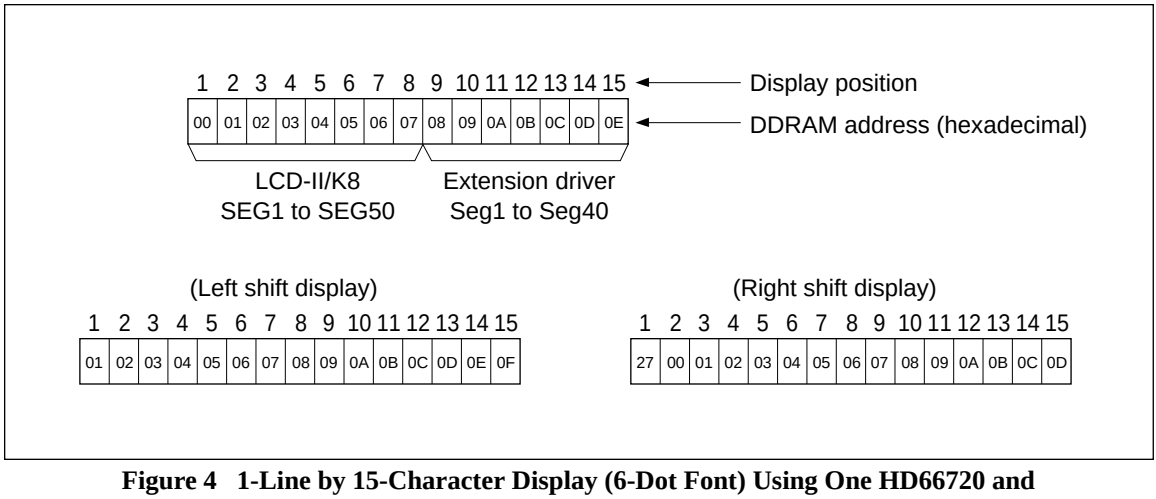


Figure 4 1-Line by 15-Character Display (6-Dot Font) Using One HD66720 and One Extension Driver

- 2-line display (NL = 1)

  — Case 1: The first line is displayed from COM1 to COM8, and the second line is displayed from COM9 to COM16. Note that the last address of the first line and the first address of the second line are not consecutive. Figure 6 shows an example where a 5-dot font-width 8 × 2-line display is performed using one HD66720.

  When a display shift is performed, the DD RAM addresses shift as shown.

  — Case 2: Figure 6 shows an example where a 5-dot font-width 16 × 2-line display is performed using one HD66720 and one extension driver.

  When a display shift is performed, the DDRAM addresses shift as shown.

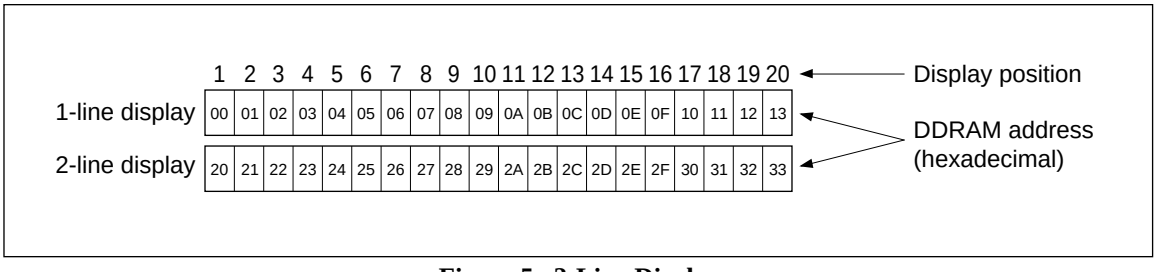


Figure 5 2-Line Display

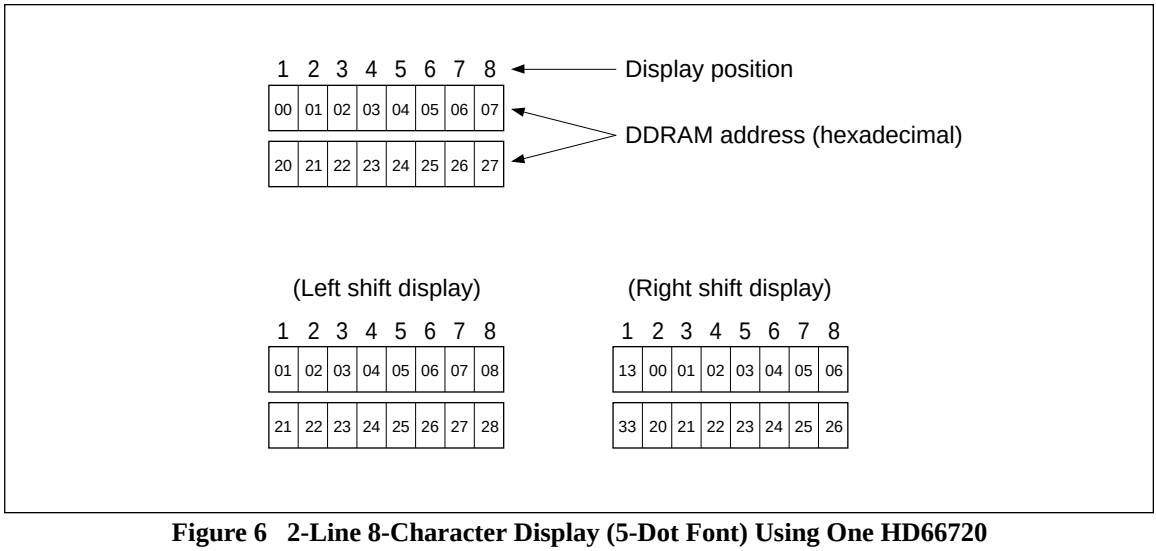


Figure 6 2-Line 8-Character Display (5-Dot Font) Using One HD66720

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3 to 5). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM (see Modifying Character Patterns).

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of table 6 to show the character patterns stored in CG RAM.

See table 6 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEG RAM)

The segment RAM (SEG RAM) is used to enable control of segments such as an icon and a mark by the user program. Data is read from SEG RAM and is output via the COMS pin to perform segment display. As shown in table 7, bits in SEG RAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DD RAM and CG RAM. Scrolling or display shifting will not be performed.

SEG RAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

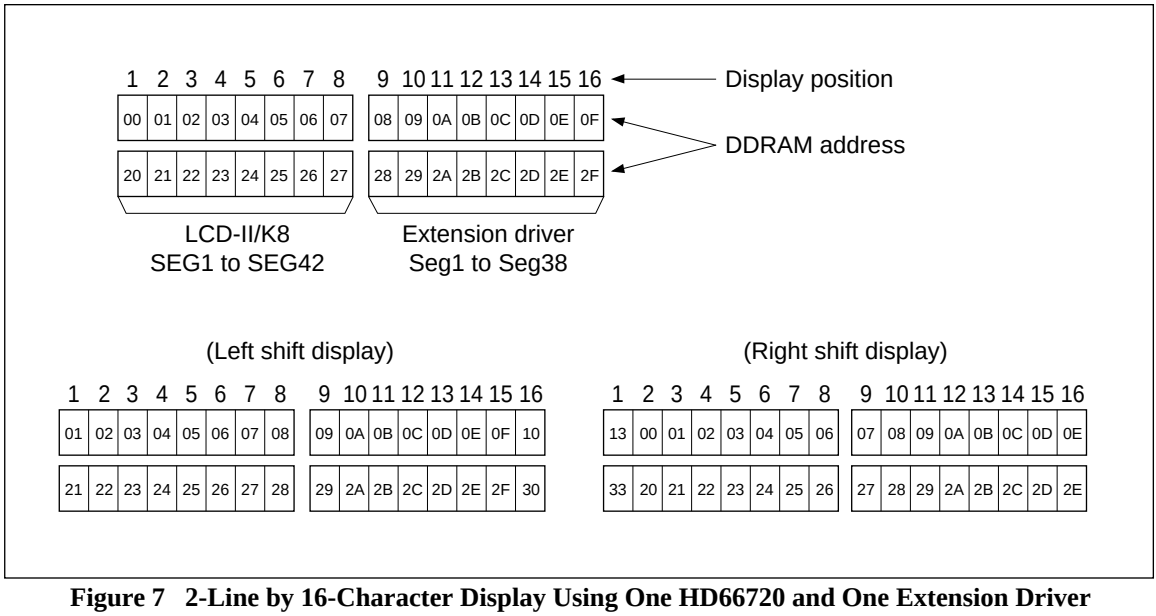


Figure 7 2-Line by 16-Character Display Using One HD66720 and One Extension Driver

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DD RAM, CG ROM, CG RAM, and SEG RAM. RAM read timing for display and internal operation timing by MPU access are generated in a time sharing method. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of common signal drivers and segment signal drivers. For a 1-line display, there will be 9 common signals and 16 segment signals. For a 2-line display, there will be 17 common signals and 42 segment signals. If the NL pin is set, display lines can be selected automatically.

Character pattern data is sent serially through a 50-bit (42-bit) shift register and latched when all needed data has arrived. The latched data then enables the LCD driver to generate drive waveform outputs.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66720 drives from the head display.

Table 3 Relationship between Character Codes and Character Patterns (ROM Code: A03)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 4 Relationship between Character Codes and Character Patterns (ROM Code: A01)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 5 Relationship between Character Codes and Character Patterns (ROM Code: A02)

Upper Bits / Lower Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)																
xxxx0001	CG RAM (2)																
xxxx0010	CG RAM (3)																
xxxx0011	CG RAM (4)																
xxxx0100	CG RAM (5)																
xxxx0101	CG RAM (6)																
xxxx0110	CG RAM (7)																
xxxx0111	CG RAM (8)																
xxxx1000	CG RAM (1)																
xxxx1001	CG RAM (2)																
xxxx1010	CG RAM (3)																
xxxx1011	CG RAM (4)																
xxxx1100	CG RAM (5)																
xxxx1101	CG RAM (6)																
xxxx1110	CG RAM (7)																
xxxx1111	CG RAM (8)																

Note: The character codes of the characters enclosed in the bold frame are the same as those of the first edition of the ISO8859 and the character code compatible.

Table 6 Relationships between CG RAM Address, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

a) When character pattern is 5 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	Character pattern (1)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern (8)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	

a) When character pattern is 6 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

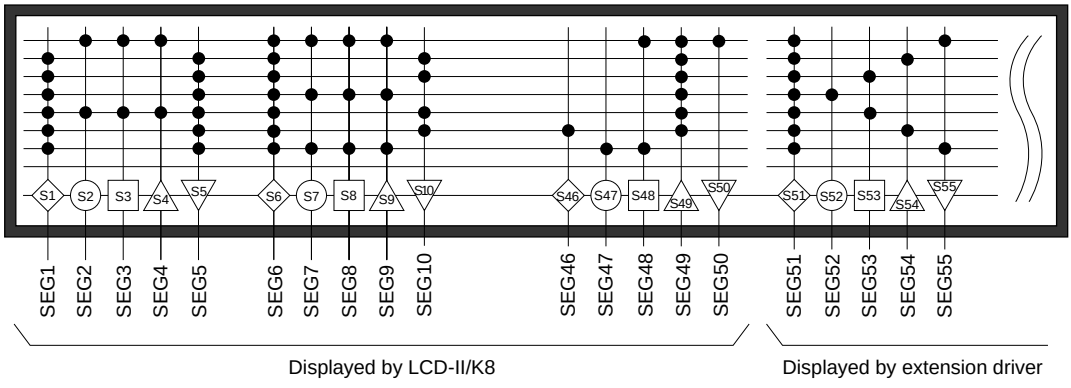
Notes:
1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).
2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in the figure above. Characters of 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters of 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected. Bit 3 of the character code is invalid (*). Therefore, for example, the character codes (00)H and (08)H correspond to the same CGRAM address.
5. A set bit in the CG RAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CG RAM. When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display. When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

Table 7 Relationship between SEGRAM Addresses and Display Patterns

SEGRAM address				SEGRAM data															
				a) 5-dot font width								b) 6-dot font width							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	*	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	*	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	*	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	*	S56	S7	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	*	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	*	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	*	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	*	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96
				Blinking control			Pattern on/off					Blinking control			Pattern on/off				

Notes:
1. Data set to SEG RAM is output when COMS is selected.
2. S1 to S96 are pin numbers of the segment output driver. S1 is positioned to the left of the display. When the HD66720 is used by one chip, segments from S1 to S50 and S1 to S42 are displayed for a 1-line display and a 2-line display, respectively. An extension driver displays the segments after S50 and S42.
3. After S80 output at 5-dot font and S96 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on/off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEG RAM. When bit 7 is 1, only a bit set to 1 of the lower six bits is blinked on the display. When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the SEG RAM data correspond to display selection, and zeros to non-selection.

i) 5-dot font width (FW = 0)



ii) 6-dot font width (FW = 1)

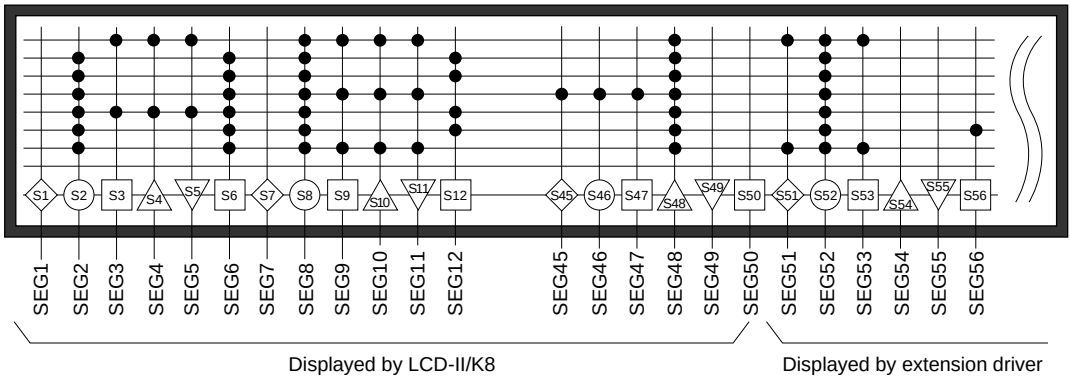


Figure 8 Correspondence between SEG RAM and Segment Display

- Cursor/Blink Control Circuit

  The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

  For example (figure 9), when the address counter is (08)H, a cursor is displayed at a position corresponding to DDRAM address (08)H.

Note: Cursor/blink/black and white inversion is performed even when the address counter (AC) is selecting CG RAM or SEG RAM. However, in that case, cursor/blink/black and white inversion does not have any meaning.

- Scroll Control Circuit

  The scroll control circuit is used to perform a smooth-scroll in units of dots. When the number of characters to be displayed is greater than that possible at one time on the liquid crystal module, this horizontal smooth scroll can be used to display all characters. Since display lines to scroll can be specified by the register function, random lines can only be scrolled in 2-line mode. Refer to Horizontal Dot Scroll, for details.

- LED Output Control

  The HD66720 has two register-controlled general-purpose output ports. Like other registers, these ports can be set by the MPU via a serial interface to control LED illumination, so there is no need for special control signals.

Oscillator

The HD66720 has a built-in R-C oscillator that can be operated with the addition of a single external resistor. Since this resistor is externally mounted, it can be adjusted to produce the required frequency. Note that changing the operating frequency will effect the frame refresh frequency, the blink rates of the cursors, segments and characters, and the key scan frequency.

The system can also be synchronized with other equipment by inputting an external clock.

LCD Booster Circuit

The LCD booster circuit produces a drive voltage for the LCD by boosting the standard supply voltage by two or three times. All that is needed to operate this circuit is either two or three (depending on the boost factor) external capacitors of about 1 µF each. When driving a large LCD that draws a high load current, there will be an excessive voltage drop at the output of the booster—if this occurs, please use an external LCD power supply.

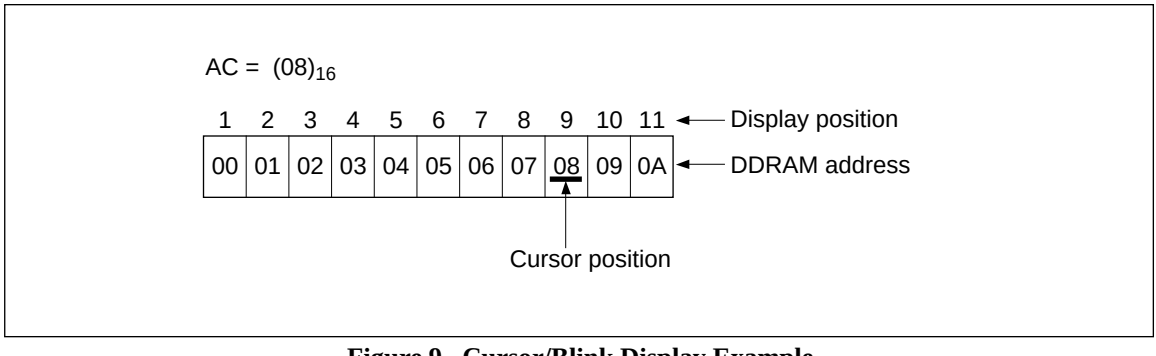


Figure 9 Cursor/Blink Display Example

Modifying Character Patterns

Character Pattern Development Procedure

The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.

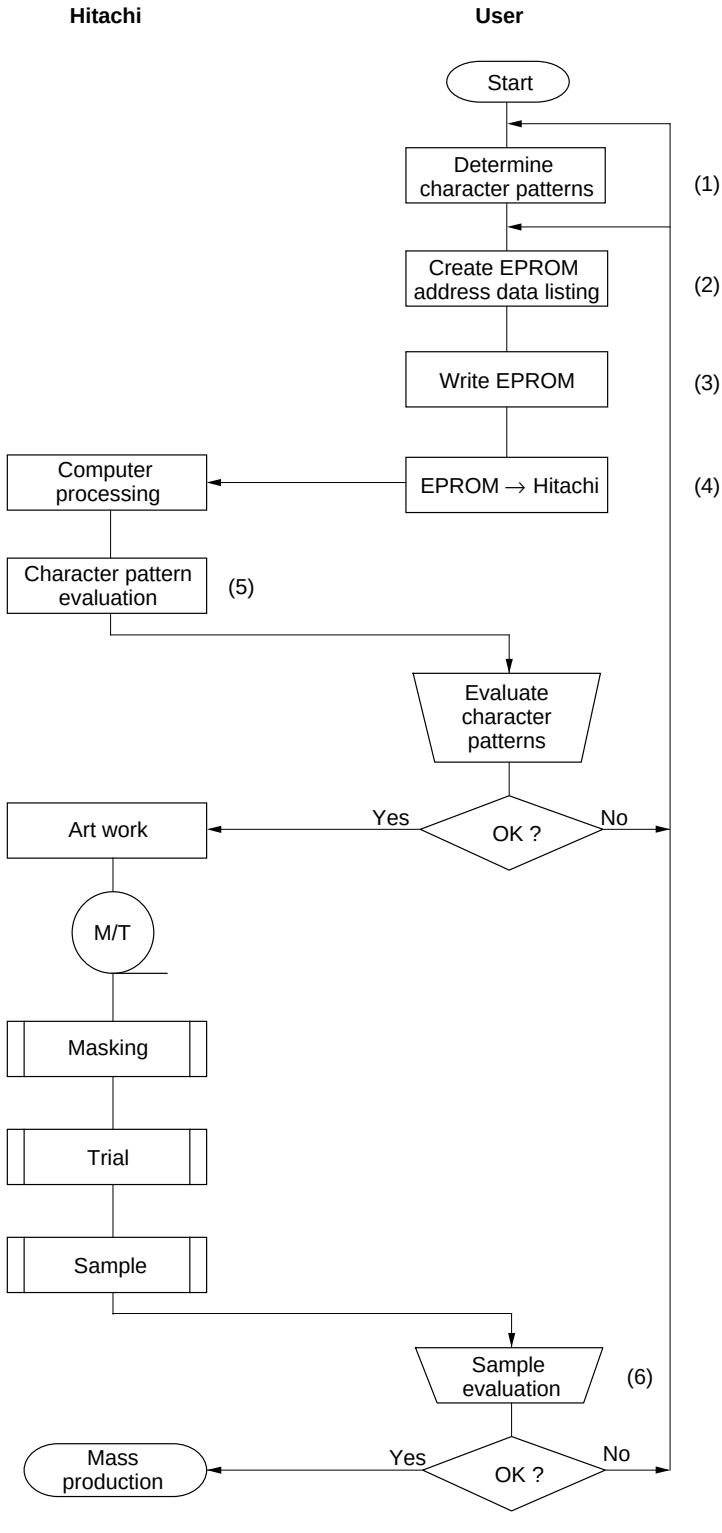


Figure 10 Character Pattern Development Procedure

Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

- Programming to EPROM

  The HD66720 character generator ROM can generate 240 5 × 8 dot character patterns. Table 8 shows correspondence between the EPROM address, data, and the character pattern.

- Handling unused character patterns

1. **EPROM data outside the character pattern area:** This is ignored and so any data is acceptable because it does not affect display operation using the character generator ROM.
2. **EPROM data in CG RAM area:** Always fill with zeros.
3. **Treatment of unused user patterns in the HD66720 EPROM:** According to the user application, these are handled in either of two ways:
   a. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   b. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 8 Correspondence Example between EPROM Address

EPROM Address												Data				
												MSB				LSB
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0

Character code 0 Line position

Notes:
1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify the line position of the character pattern. EPROM address A_3 should be set to 0.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Areas which are lit (indicated by shading) are stored as 1, and unlit areas as 0.
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits O_7 to O_5 are invalid. 0 should be written in all bits.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66720 can be controlled by the MPU. Before starting internal operation of the HD66720, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66720 is determined by signals sent from the MPU. These signals, which include register selection bit (RS), read/write bits (R/W), and the data bus bits (DB_0 to DB_7), make up the HD66720 instructions (table 13). There are four categories of instructions that:

- Designate HD66720 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66720 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction can perform concurrently with display data write, the user can minimize system efficiently.

When an instruction is being executed for internal operation (BF = 1), no instruction other than the busy flag/scan data instruction can be executed.

Adjust the transmission rate so that the last bit of the next instruction is transmitted after executing the current instruction. Refer to table 13 Instruction for instruction execution times. The execution times depend on the operation frequency (oscillation frequency). When using the R-C oscillator, be careful when determining the transmission rate, because it will vary greatly by the power supply voltage, operating temperature, and manufacturing tolerances.

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. If S is 0, the display does not shift.

RS	R/W	DB_7							DB_0
0	0	0	0	0	0	0	0	0	1

Figure 11 Clear Display Instruction

RS	R/W	DB_7							DB_0
0	0	0	0	0	0	0	0	1	0

Figure 12 Return Home Instruction

RS	R/W	DB_7							DB_0
0	0	0	0	0	0	0	1	I/D	S

Figure 13 Entry Mode Set Instruction

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, and can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font.

B: The character indicated by the cursor blinks when B is 1. The blinking is displayed as switching between all blank dots and displayed characters at a speed of 384-ms intervals when fOSC is 150 kHz with a 5 dot font width. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to the reciprocal of either f_{cp} or f_{OSC}. For example, when f_{cp} is 180 kHz, 384 × 150/180 = 320 ms.)

Extension Function Set

When the extended register enable bit (RE) is 1, FW, FR, and B/W bits shown are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the rightmost bit, and the font is displayed with a 5-dot character width. If the FW bit is changed, data in DD RAM and CG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See Oscillator for details. FW can only be set at the head of a program before any other instructions (except for Read Busy Flag & Scan Data). If the value of bit FW is modified after executing other instruction, the data in RAM may be damaged.

FR: When FR is 1, the display data stored in CG ROM/CG RAM/SEG RAM is reflected horizontally. Select FR according to how the LSI is mounted. The display location of each character does not change.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white inversion. At this time, bits C and B in display on/off control register are “Don’t care”. When f_{cp} or f_{osc} is 150 kHz, display is changed by switching every 384 ms.

	RS	R/W	DB_7						DB_0
RE = 0	0	0	0	0	0	0	1	D	C	B

Figure 14 Display On/Off Control Instruction

	RS	R/W	DB_7						DB_0
RE = 1	0	0	0	0	0	0	1	FW	FR	B/W

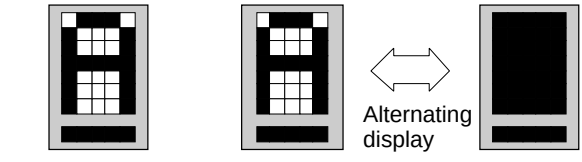
Figure 15 Extended Function Set Instruction

Cursor or Display Shift

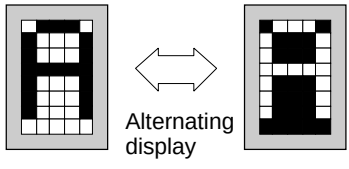
Only when the extended register bit (RE) is 0, the S/C and R/L bits can be set.

S/C, R/L: Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 9). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 20th digit of the first line.

Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position. When this instruction is executed, extended register enable bit (RE) is reset. The address counter (AC) contents will not change if only a display shift is performed.

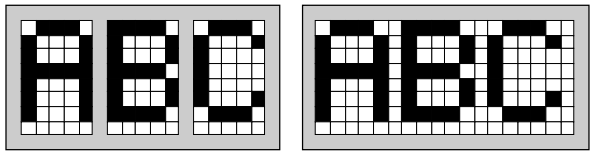


i) Cursor display example ii) Blink display example

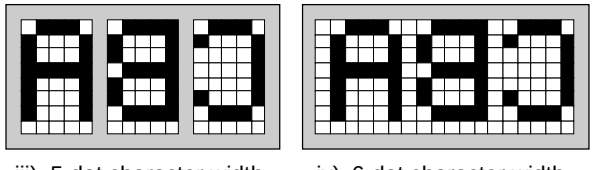


iii) White-black inverting display example

a) Cursor blink width control



i) 5-dot character width (without mirror reflection) ii) 6-dot character width (without mirror reflection)



iii) 5-dot character width (with mirror reflection) iv) 6-dot character width (with mirror reflection)

b) Font width control

Figure 16 Example of Display Control

Scroll/LED Control

Only when the extended register bit (RE) is 1, the LED and HSE bits can be set.

LED: This bit controls the LEDs. The data set in bits LED0 and LED1 is reversed and output from pins LED0 and LED1. In other words, if 1 is set in bit LED0, a low level is output from pin LED0. This register function can also be used as a general output port instead of LED control.

HSE: This bit specifies which display line or lines are to be dot shifted by the amount indicated in the set scroll quantity register. When HSE is 1 the first line scrolls and when HSE2 is 1 the second line scrolls.

Table 9 Cursor or Display Shift Function

S/C	R/L	Description
0	0	Shifts the cursor position to the left (AC is decremented by one)
0	1	Shifts the cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

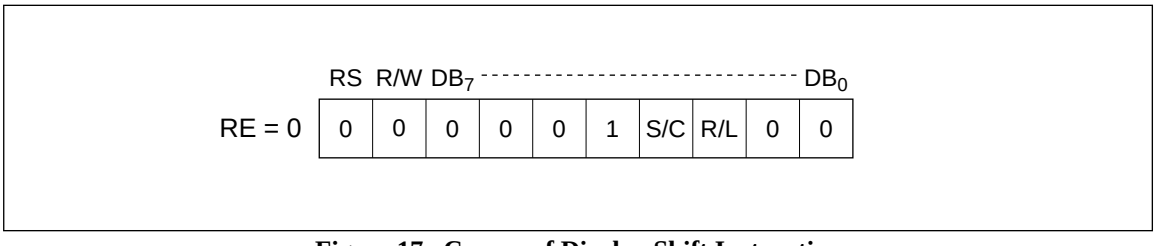


Figure 17 Cursor of Display Shift Instruction

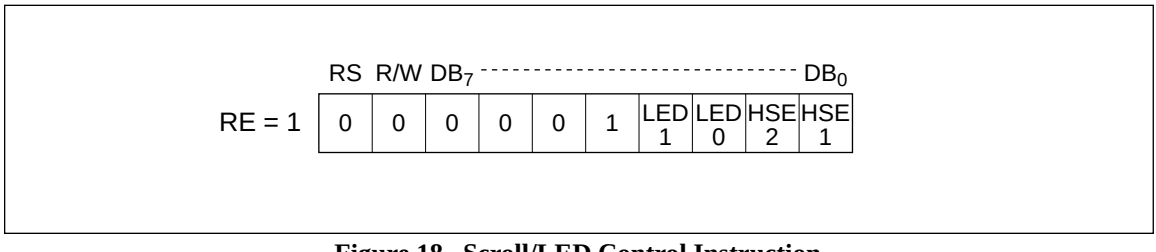


Figure 18 Scroll/LED Control Instruction

Function Set

Only when the extended register enable bit (RE) is 0, the KF bit can be accessed, and only when 1, the BE and the LP bits can be accessed. Bits IRE and SLP can be accessed regardless of RE.

IRE: When bit IRE is 1, key scan interrupts are generated. When a key is pressed, pin IRQ becomes low level.

SLP: When SLP is 1, the LSI enters sleep mode. During sleep mode, the display is disabled because the internal operation clock is divided by 16. However, the key scan cycle is not affected. For details, refer to Sleep Mode. In this mode, the frame frequency is also divided by 16, and a scanning line may appear. To avoid this, the LCD driving voltage (V_{LCD}) should be cut off.

RE: When bit RE is 1, extension function set register, scroll/LED control register, set scroll quantity register, the set SEG RAM address register, and bit BE in the function set register, can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

KF: When RE is 0, these bits specify the key scan cycle. Set these bits according to the mechanical characteristic of the keys. The key scan cycles relies on the operation cycles(oscillation frequency). Table 10 shows the key scan cycles for the case when the operation frequency (oscillation frequency) is 160 kHz.

BE: When bit RE is 1, this bit can be rewritten. When this bit is 1, the user font in CG RAM and the segment in SEG RAM can be blinked according to the upper two bits of CG RAM and SEG RAM.

LP: When bit RE is 1, this bit can be rewritten. When LP is set to 1, the HD66720 operates in low power mode. In 1-line display mode, the HD66720 operates by dividing the oscillation frequency by four, and in a 2-line display mode, the HD66720 operates at the oscillation frequency divided by two. Thus, 10 characters at the most are displayed in one line. According to these operations, instruction execution takes four times or twice as long. When performing display shift and smooth scroll during low power mode, the resulting display will differ from the normal mode display (refer to Low Power Mode for details). When this LP bit is changed, data in RAMs may be broken, so re-write data into RAMs.

Table 10 Key Scan Cycle

KF1	KF0	Key Scan Cycle
0	0	10 ms
0	1	5 ms
1	0	20 ms
1	1	40 ms

*: For the case when f_{cp} (f_{osc}) is 160 kHz.

	RS	R/W	DB_7							DB_0
RE = 0	0	0	0	0	1	IRE	SLP	RE	KF1	KF0
RE = 1	0	0	0	0	1	IRE	SLP	RE	BE	LP

Figure 19 Function Set Instruction

Set CGRAM Address

A CG RAM address can be set while the RE bit is cleared to 0.

Set CG RAM address sets the address indicated by binary AAAAAA into the address counter. After this address set, CG RAM can be written to or read from by the MPU.

Set SEG RAM Address

Only when the extended register enable (RE) bit is 1, the SEG RAM address can be set.

The SEG RAM address in the binary form AAAA is set to the address counter. After this address set, SEG RAM can be written to or read from by the MPU.

Set DD RAM Address

A DD RAM address can be set while the RE bit is cleared to 0.

Set DD RAM address sets the DD RAM address binary indicated by AAAAAAA into the address counter. After this address set, DD RAM can be written to or read from by the MPU.

When NL is low (1-line display), AAAAAA can be H(00) to H(27). When NL is high (2-line display), AAAAAA can be H(00) to H(13) for the first line, and H(20) toH(33) for the second line.

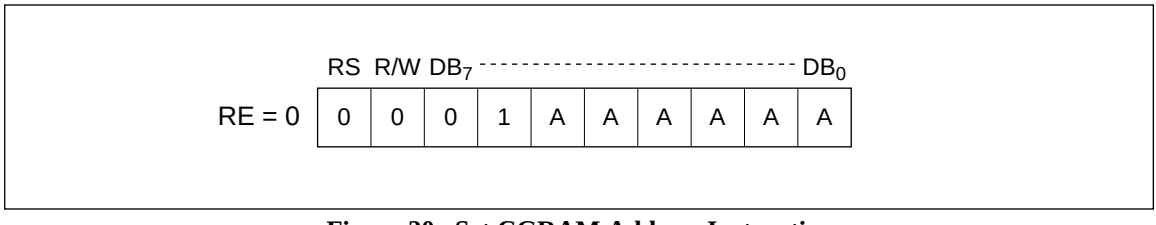


Figure 20 Set CGRAM Address Instruction

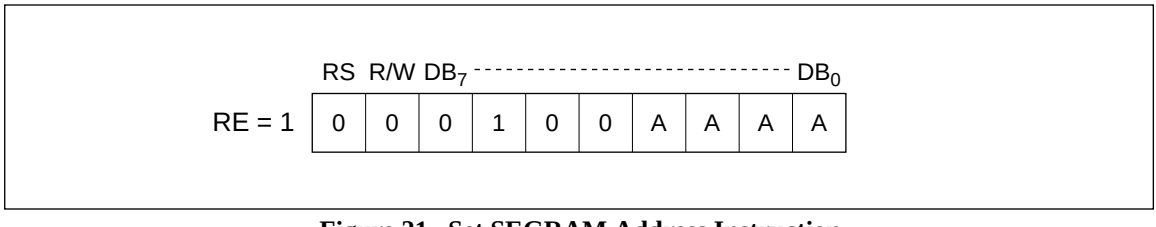


Figure 21 Set SEGRAM Address Instruction

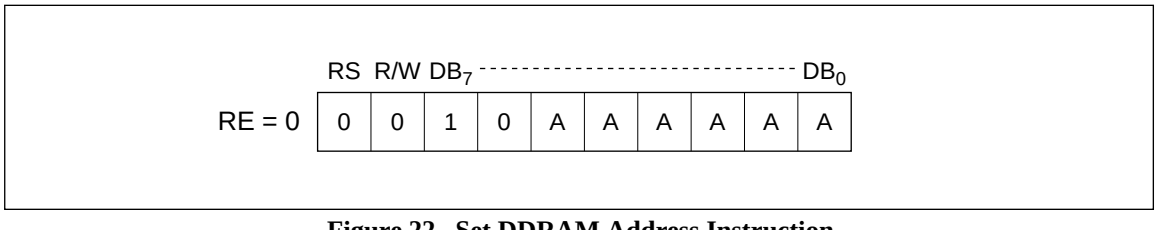


Figure 22 Set DDRAM Address Instruction

Set Scroll Quantity

When extended register enable bit (RE) is 1, PS 1/0 and HDS4 to HDS0 can be set.

PS: PS1 and PS0 specify the number of characters at the left side of the display that are unaffected by horizontal scrolls and are left intact while the rest of the display is scrolled (table 11).

HDS: HDS4 to HDS0 specify horizontal scroll quantity to the left of the display in dot units. The HD66720 uses the unused DD RAM area to execute a desired horizontal smooth scroll from 1 to 24 dots (table 12).

Note: When performing a horizontal scroll as described above by connecting an extension driver, the maximum number of characters per line decreases by the quantity corresponding to the specified scroll distance.

Table 11 Partial Smooth Scroll

PS1	PS0	Description
0	0	FIxes all characters
0	1	Fixes leftmost character in smooth scroll
1	0	Fixes the two leftmost characters in smooth scroll
1	1	Fixes the three leftmost characters in smooth scroll

Table 12 Smooth Scroll Quantity

HDS4	HDS3	HDS2	HDS1	HDS0	Description
0	0	0	0	0	No shift
0	0	0	0	1	Shifts the display position to the left by one dot
0	0	0	0	0	Shifts the display position to the left by two dots
0	0	0	1	1	Shifts the display position to the left by three dots
		•			
		•			
1	0	1	1	1	Shifts the display position to the left by 23 dots
1	*	*	*	*	Shifts the display position to the left by 24 dots

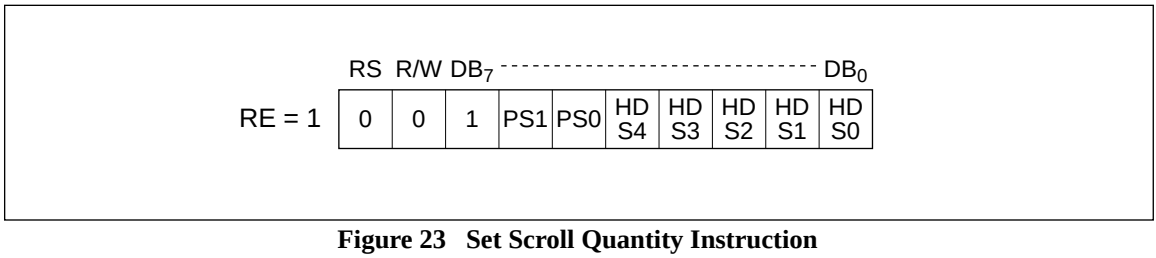


Figure 23 Set Scroll Quantity Instruction

Read Busy Flag & Scan Data

Scan data SD4 to SD0 latches into scan registers SCAN0 to SCAN5 and scan cycle state SF1 and SF0 is read sequentially. Refer to Key Scan Control for details. At the same time, busy flag (BF) is read. When BF is 1, the HD66720 is still processing an instruction already accepted, and does not accept another instruction until BF becomes 0. Adjust the transfer rate so that the HD66720 receives the last bit of the next instruction after BF has become 0.

Write Data to CG RAM, DD RAM, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG RAM, DD RAM or SEG RAM. CG RAM, DD RAM or SEG RAM is selected by the previous specification of the address set instruction (set CG RAM address/set DD RAM address/set SEG RAM address). After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

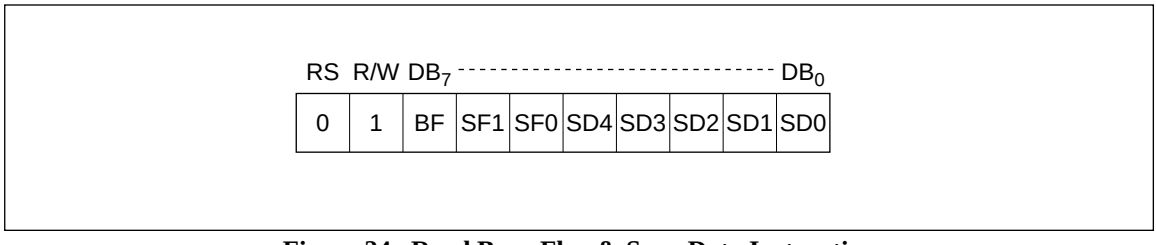


Figure 24 Read Busy Flag & Scan Data Instruction

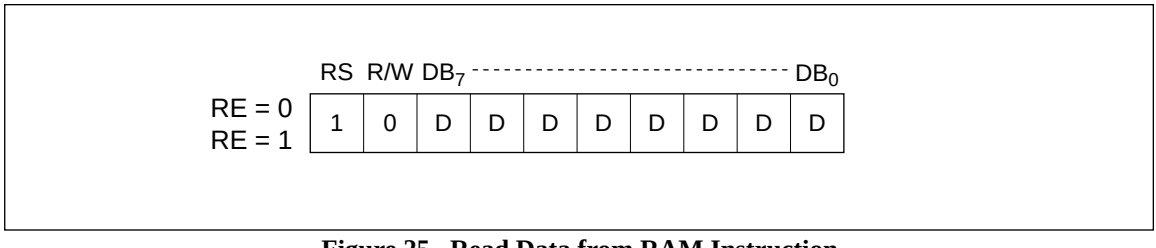


Figure 25 Read Data from RAM Instruction

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG RAM, DD RAM, or SEG RAM. CG RAM, DD RAM or SEG RAM is selected by the previous specification of the address set instruction. If no address is specified, the first data read will be invalid. When executing serial read instructions, data is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

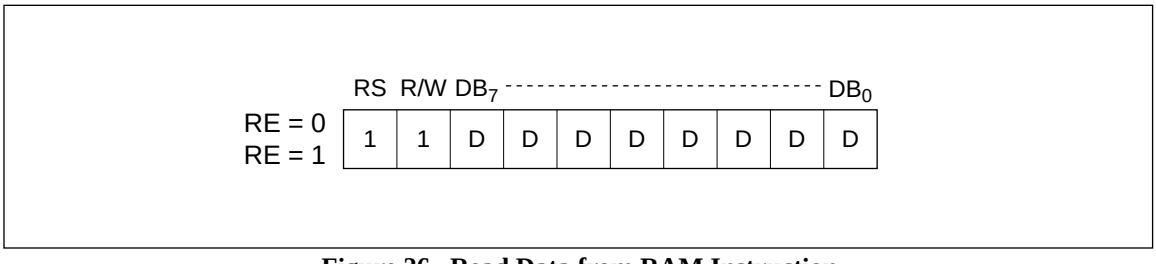


Figure 26 Read Data from RAM Instruction

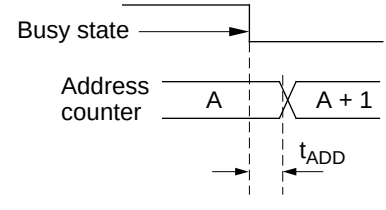
Table 13 Instructions

Instruction	RE Bit	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 160 kHz)
Clear display	0/1	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	2.67 ms
Return home	0/1	0	0	0	0	0	0	0	0	1	0	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	2.67 ms
Entry mode set	0/1	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	63 µs
Display on/off control	0	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C), and blinking of cursor position character (B).	63 µs
Extension function set	1	0	0	0	0	0	0	1	FW	FR	B/W	Sets a font width (FW), font reverse (FR), and a black-white inverting cursor (B/W).	63 µs
Cursor or display shift	0	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DD RAM contents.	63 µs
Scroll/LED output control	1	0	0	0	0	0	1	LED	LED	HSE	HSE	Specifies which display lines to undergo horizontal smooth scroll and controls the output of LED.	63 µs
Function set	0	0	0	0	0	1	IRE	SLP	RE	KF	KF	Set interrupt enable (IRE) sleep mode (SLP), extension register write enable (RE). Sets key scan cycle (KF) and extension register write enable.	63 µs
	1	0	0	0	0	1	IRE	SLP	RE	BE	LP	Sets CG RAM/SEG RAM blinking enable (BE), and low-power mode (LP).	63 µs
Set CGRAM address	0	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	63 µs
Set SEGRAM address	1	0	0	0	1	0	0	A_{SEG}	A_{SEG}	A_{SEG}	A_{SEG}	Sets SEG RAM address. SEG RAM data is sent and received after this setting.	63 µs

Table 13 Instructions (cont)

Instruction	RE Bit	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 160 kHz)
Set DDRAM address	0	0	0	1	0	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	63 µs
Set scroll quantity	1	0	0	1	PS	PS	HDS	HDS	HDS	HDS	HDS	Sets horizontal dot scroll quantity (HDS) and partial scroll characters (PS).	63 µs
Read busy flag & scan data	0/1	0	1	BF	SF	SF	SD	SD	SD	SD	SD	Reads busy flag (BF), data in scan register (SD), and scan state (SF).	0 µs
Write data to RAM	0/1	1	0			Write data						Writes data into DD RAM, CG RAM, or SEG RAM.	63 µs t_{ADD} = 9.3 µs*
Read data from RAM	0/1	1	1			Read data						Reads data from DD RAM, CG RAM, or SEG RAM.	63 µs t_{ADD} = 9.3 µs*

I/D	= 1: Increment	LP	= 1: Low-power mode
I/D	= 0: Decrement	BF	= 1: Internally operating
S	= 1: Accompanies display shift	BF	= 0: Instructions acceptable
D	= 1: Display on	DD RAM	: Display data RAM
C	= 1: Cursor on	ADD	: DDRAM corresponding to cursor address
B	= 1: Blink on		
FW	= 1: 6-dot font width	CG RAM	: Character generator RAM
FR	= 1: Horizontal font reflection	A_{CG}	: CG RAM address
B/W	= 1: Black-white inverting cursor on	SEGRAM	: Segment RAM
S/C	= 1: Display shift	A_{SEG}	: Segment RAM address
S/C	= 0: Cursor move	HSE	: Specifies horizontal scroll lines
R/L	= 1: Shift to the right	HDS	: Horizontal dot scroll quantity
R/L	= 0: Shift to the left	PS	: Specifies partial scroll quantity
IRQ	= 1: Interrupt (IRQ) generation enable	LED	: LED control
SLP	= 1: Sleep mode	KF	: Key scan cycle
RE	= 1: Extension register write enable	SD	: Key scan data
BE	= 1: CGRAM/SEGRAM blinking enable	SF	: Key scan state



t_{ADD} depends on the operation frequency
$t_{ADD} = 1.5/f_{cp}$ or f_{osc} (sec)

Figure 27 t_{ADD} State

Note: 1. *After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag is cleared.

It_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. The execution time mentioned above are for the case of 5-dot font. With a 6-dot font, it will take 20% more to execute an instruction. The execution time will also change if the frequency changes. For example, the execution time will be reduced to 80% when f is 200 kHz.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66720 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the V_{CC} rises to 2.7 V.

1. Clear display
   (20)H to all DDRAM

2. Function set
   IRE = 0: Interrupt (IRQ) generation disable
   SLP = 0: Clear sleep mode
   RE = 0: Extension register write disable
   KF = 0: Key scan cycle 10 ms
   BE = 0: CGRAM/SEGRAM blinking off
   LP = 0: Not in low power mode

3. Display on/off control
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blinking off

4. Entry mode set
   I/D = 1: Increment by 1
   S = 0: No shift

5. Extension function set
   FR = 0: Without font reverse
   B/W = 0: Normal cursor (8th line)

6. Scroll/LED control
   HSE = 00: Scroll unable
   LED = 00: LED output level = high

7. Set scroll quantity
   HDS = 00000: Not scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66720.

Initializing by Hardware Reset Input

The HD66720 also has a reset input pin (RESET*). If this pin is made low during operation, an internal reset and initialization is performed except for key scan cycle setting bit (KF). A hardware reset can turn off display when the HD66720 is switched off. A reset input is ignored, however, during internal reset after power-on. In other words, the internal reset has priority. The level of the reset pin must always be pulled up to V_{CC} when the hardware reset input is not used.

Transferring Serial Data

A three-line clock-synchronous transfer method is used. The HD66720 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66720 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the HD66720 can be reset and serial transfer synchronized by making chip select (CS*) high. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single HD66720 interfaces to a single MPU, an interface can be constructed from the transfer clock (SCLK) and serial data lines (SID and SOD). In this case, chip select (CS*) should be fixed to low.

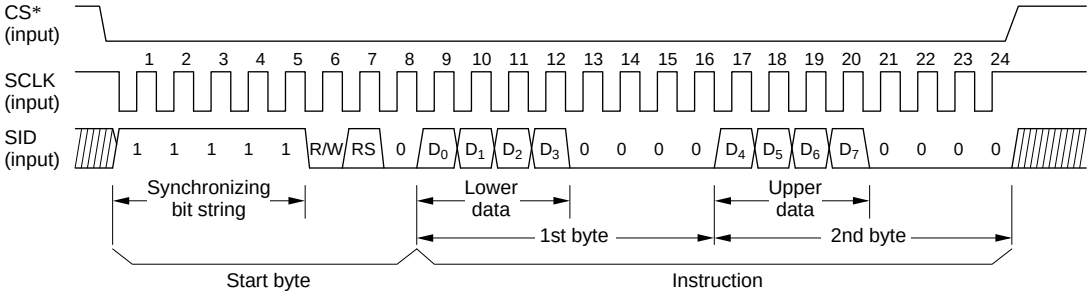
The transfer clock (SCLK) is independent from operational clock (CLK) of the HD66720. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see continuous transfer) must be considered since the HD66720 does not have an internal transmit/ receive buffer.

To begin with, transfer the start byte. By receiving five consecutive bits (synchronizing bit string) at the beginning of the start byte, the transfer counter of the LCD-II/K8 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction (R/W bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail in the following.

a) Serial data input (receiving)



b) Serial data output (transmitting)

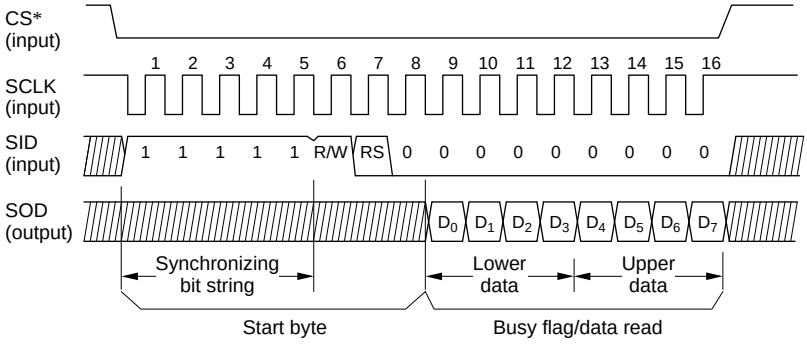


Figure 28 Basic Procedure for Transferring Serial Data

- Receiving (write)

  After receiving the start synchronizing bit string, the R/W bit (= 0), and the RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are continuously received with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

- Transmitting (read)

  After receiving the synchronizing bit string, the R/W bit (= 0), and the RS bit with the start byte, 8-bit read data is transmitted from pin SOD in the same way as receiving. When read data is continuously transmitted with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

  If data is read when bit RS is set to 0, scan data latched into SCAN0 to SCAN5 resisters is transmitted as the lower 5-bit data. After receiving the start byte, transmission starts from data in SCAN resister latched at KST0 strobe. After transmitting data from the SCAN5 register, SCAN0 data is retransmitted.

  When reading RAM data with bit RS set to 1, it is necessary to wait for at least the duration of a RAM data read period.

  During transmission (data output), the SID input is continuously monitored for a start synchronizing bit string (11111). Once this has been detected, the R/W and RS bits are received. Accordingly, 0 must always be input to SID when transmitting data continuously.

- Continuous Transfer

  When instructions are continuously received with the R/W bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.

  After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it. To execute the next instruction, the instruction execution time of theHD66720 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.

  In addition, if the next unit of data is read before read execution of previous data is completed for busy flag/scan data`/RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, it is possible to transfer without reading the busy flag if the burden of polling on the CPU needs to be removed. In this case, insert a transfer wait between instructions so that the current instruction first completes execution.

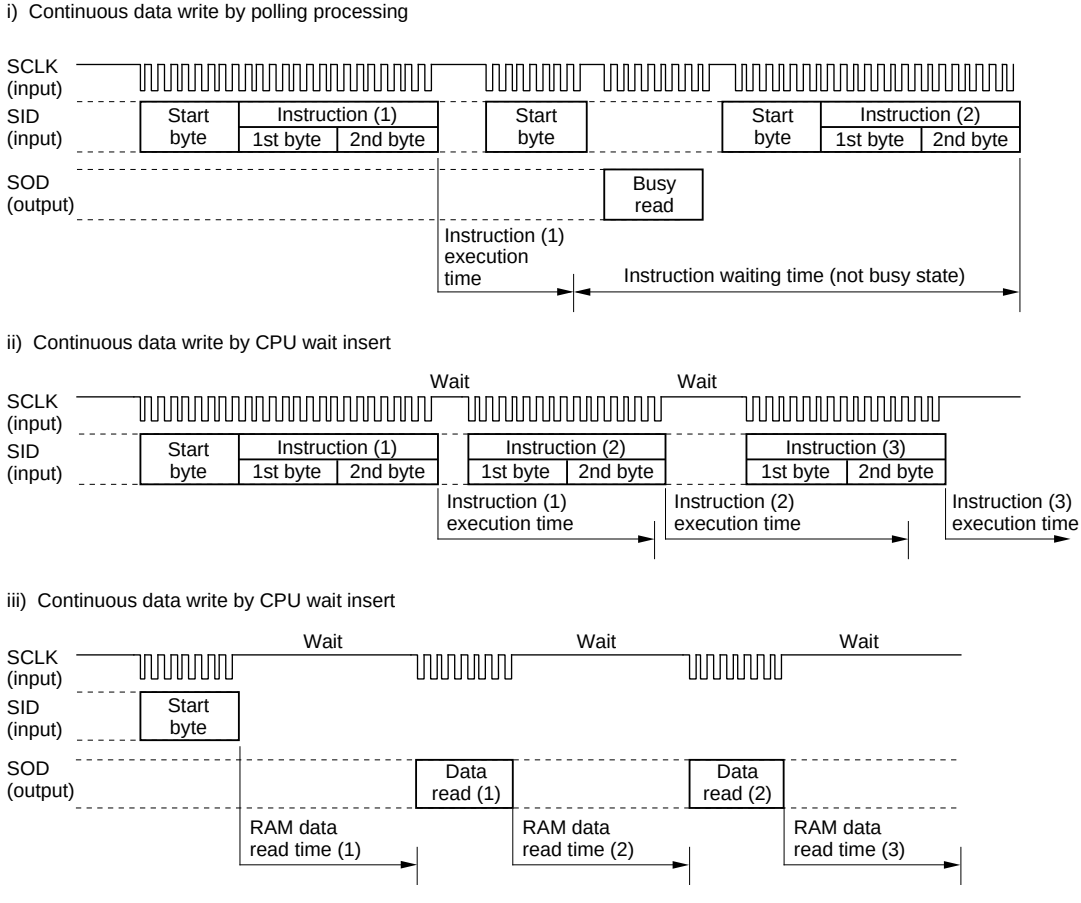


Figure 29 Procedure for Continuous Data Transfer

Key Scan Control

The key matrix scanner senses the key states at each rising edge of the key strobe signals (KST) that are output by the HD66720. The key strobe signals are output as time-multiplexed signals from KST0 to KST4. After passing through the key matrix, these strobe signals are used to sample the key status on five inputs KIN0 to KIN4, enabling up to 30 keys to be scanned.

The states of inputs KIN0 to KIN4 are sampled by key strobe signal KST0 and latched into register SCAN0. Similarly, the data sampled by strobe signals KST1 to KST5 is latched into registers SCAN1 to SCAN5, respectively.

The generation cycle and pulse width of the key strobe signals depends on the operating frequency (oscillation frequency) of the HD66720 and the key scan cycle determined by KF0 and KF1. For example, when the operating frequency is 150 kHz and KF0 and KF1 are both 0, the generation cycle is 10 ms and the pulse width is 1.7 ms. When the operating frequency (oscillation frequency) is changed, the above generation cycle and the pulse width are also changed in inverse proportion.

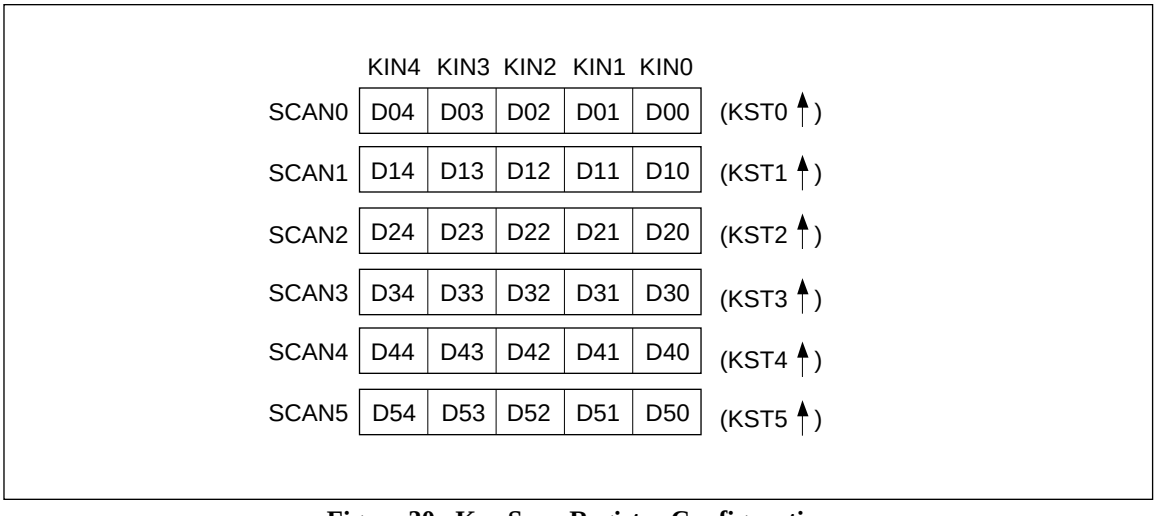


Figure 30 Key Scan Register Configuration

In order to compensate for the mechanical features of the keys, such as chattering and noise and for the key-strobe generation cycle and the pulse width, software should be used to ensure that the scanned data has been read two or three times in succession before it is assumed to be valid. Multiple keypress combinations should also be processed in software. Note that any multiple key combination is possible, however, if the key combination creates a cross pattern the scanned data will include unnecessary data. For example, if keys D12, D11, and D22 are pressed simultaneously, key D21 will also be pressed. The input pins KIN0 to KIN4 are pulled up to V_{CC} by MOS transistors (see Electrical Characteristics). External resistors may also be required to pull up the voltages further when the internal pull-ups are insufficient due to noise margins or other reasons.

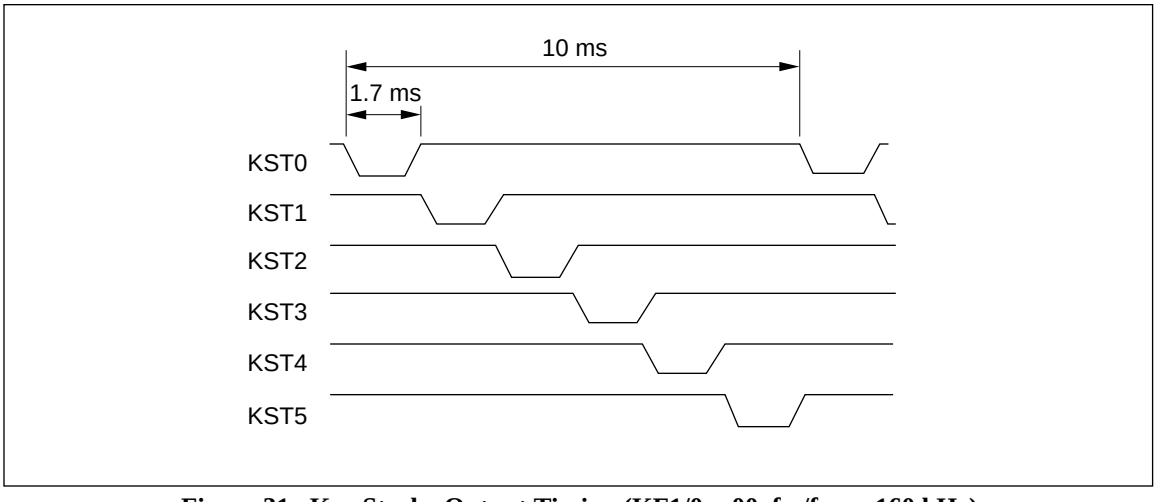


Figure 31 Key Strobe Output Timing (KF1/0 = 00, f_{cp}/f_{osc} = 160 kHz)

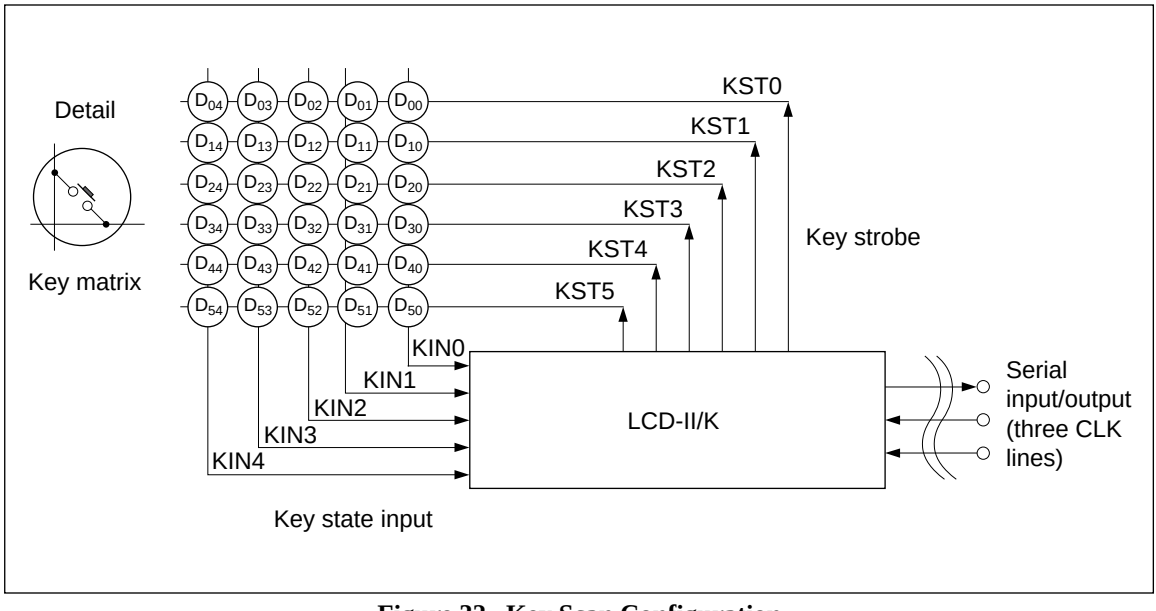


Figure 32 Key Scan Configuration

The key-scanned data is read via a three-line clock synchronous serial interface using the following procedure. First of all, a start byte is transferred. This must contain five bits of 1 (synchronous bit string), a transfer direction bit (R/W) of 1, a register select bit (RS) of 1, and one bit of 0 in that order. The synchronizing bit string is used to reset the transfer counter of the HD66720, thus synchronizing the serial transfer.

After the HD66720 has received the above start byte, it reads scan data SD0 to SD4 from the SCAN0 register starting from the LSB. The HD66720 reads data from SCAN1, SCAN2, SCAN3, SCAN4, and SCAN5 in that order. After reading SCAN5, the HD66720 starts at SCAN0 again.

The HD66720 transfer counter can also be reset to synchronize serial transfer by driving the chip select (CS*) high. In this case, the data currently transferred is cleared; therefore, transfer the start byte again to restart the transfer.

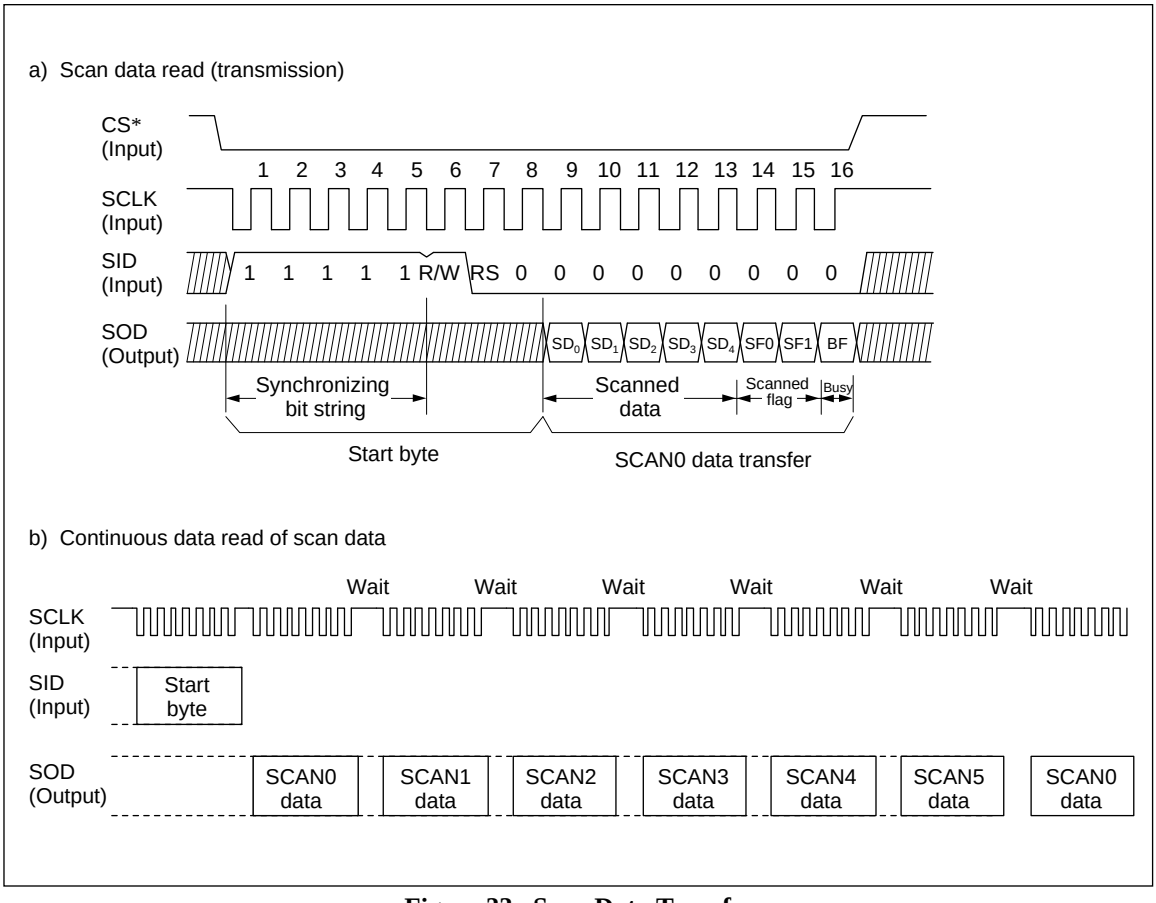


Figure 33 Scan Data Transfer

Key Scan Interrupt (Wake-Up Function)

If the MPU has set the interrupt enable bit (IRE) to 1, the LCD sends an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQ* output pin to low level. An interrupt signal can be generated by pressing any key in a 30-key matrix. The interrupt level continues to be output during the key-scan cycle in which the key is being pushed.

Key scanning is performed and interrupts can occur during LCD-II/K8 sleep mode (SLP = “1”). The interrupt signal from LCD-II/K8 can trigger the MPU even though the whole system is in a sleep state (or standby state), thus, minimizing power consumption.The LCD cannot be displayed when the LCD-II/K8 is in sleep mode. Refer to Sleep Mode for details.

The output pin of IRQ* is pulled up to the V_{CC} with a MOS of 50 kΩ; however, pull up can be made stronger by adding external resistors as needed. Interrupts may occur if noise occurs in KIN input during key scanning. Interrupts maybe inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

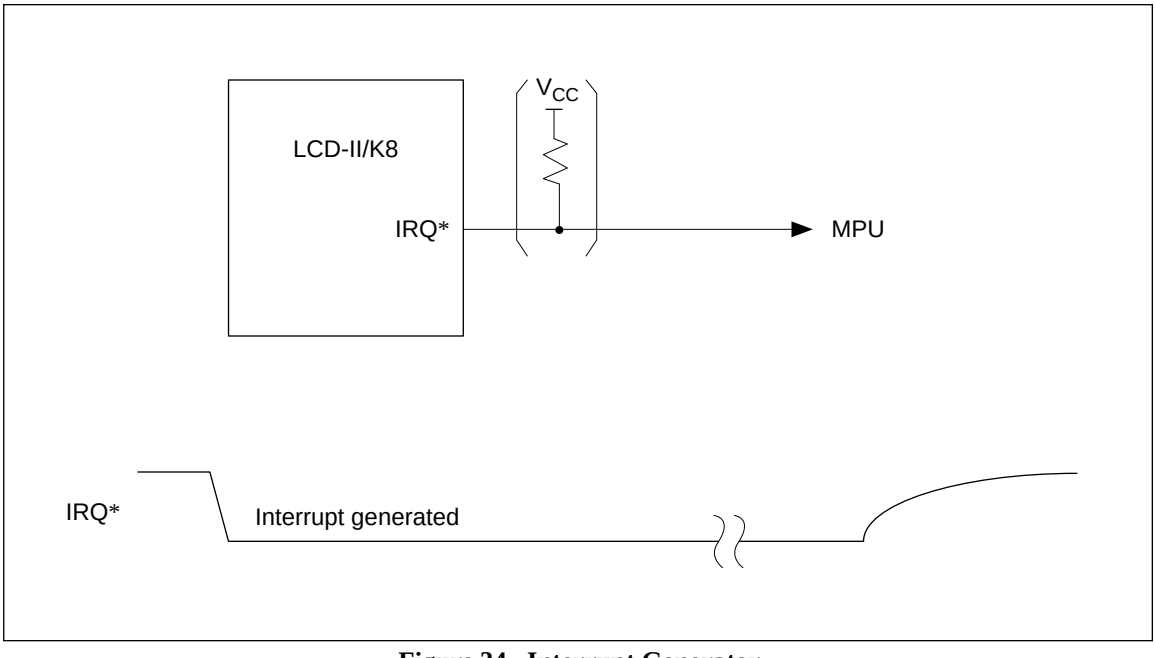


Figure 34 Interrupt Generator

Extension Driver LSI Interface

The number of displayed characters can be increased by using an extension driver. For example, by adding a single HD44100R extension driver with 40 LCD driver output, a 2-line 16 character display with a 5-dot font width can be achieved Moreover, a maximum 2-line 20 character or single-line 40 character display can be achieved by increasing the number of extension drivers.

The extension driver can be interfaced with signals CL1, CL2, D1 and M. The following figure shows an example of LCD-II/K8 and an HD44100R. The extension driver displays data from the 51st dot in 1-line display mode, and from the 43rd dot in 2-line display mode. The extension driver can be driven by the LCD-II/K8; however, the output voltage drop of the booster circuit increases as the load on the booster circuit increases.

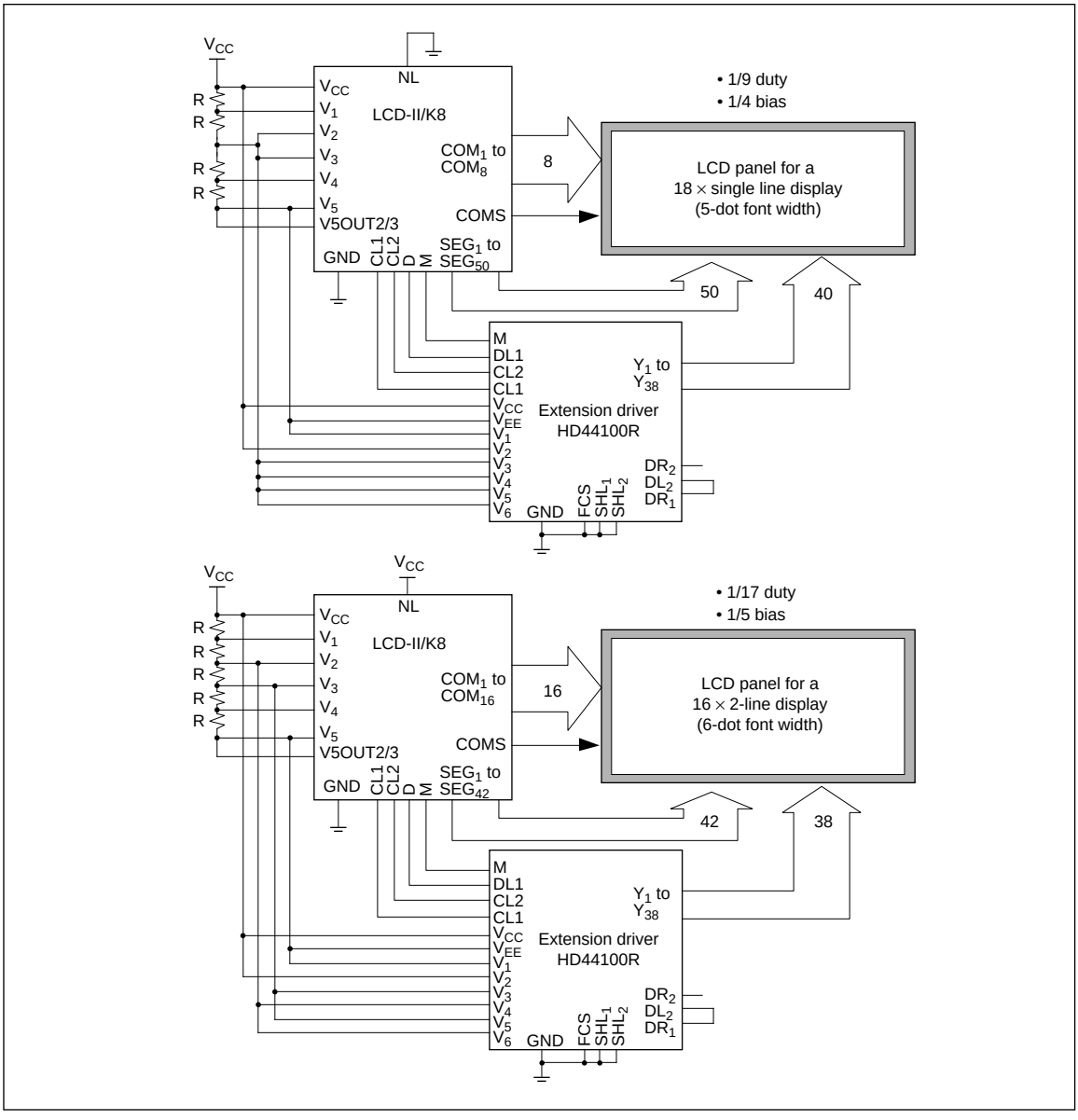


Figure 35 HD66720 and the Extension Driver (HD44100R) Connection

Interface to the Liquid Crystal Display

Set the number of display lines with the N bit and the font width with the FW bit. The relationship between the number of display lines and register values is given below.

Table 14 Relationship between Display Lines, EXT Pin, and Register Setting

		5-Dot Font					6-Dot Font						
				Register Setting					Register Setting				
Lines	Char.	Seg-ment	Extension Driver	N	RE	FW	Seg-ment	Extension Driver	N	RE	FW	Scroll Display	Duty Cycle
1	8	50	—	0	0	0	50	—	0	1	1	Enabled	1/9
	10	50	—	0	0	0	90	1	0	1	1	Enabled	1/9
	12	80	1	0	0	0	90	1	0	1	1	Enabled	1/9
	16	80	1	0	0	0	96	2	0	1	1	Enabled	1/9
	20	80	2	0	0	0	96	2	0	1	1	Enabled	1/9
	40	80	4	0	0	0	96	5	0	1	1	Disabled	1/9
2	8	42	—	1	0	0	82	1	1	1	1	Enabled	1/17
	12	80	1	1	0	0	82	1	1	1	1	Enabled	1/17
	16	80	1	1	0	0	96	2	1	1	1	Enabled	1/17
	20	80	2	1	0	0	96	2	1	1	1	Disabled	1/17

Note: — means not required.

Example of 5-Dot Font Width Connection

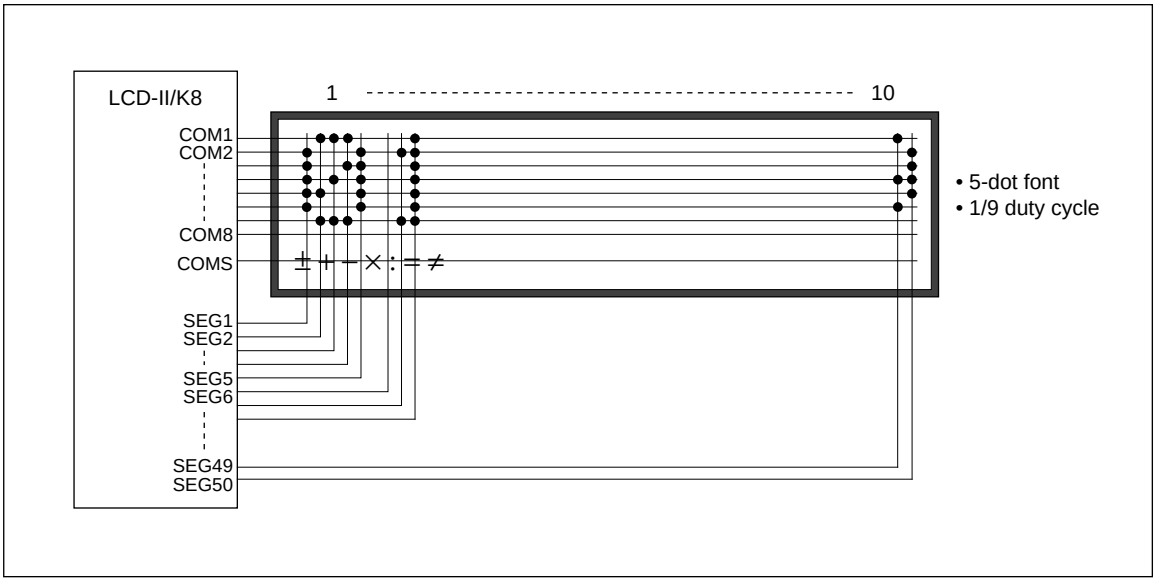


Figure 36 10 × 1-Line + 50-Segment Display

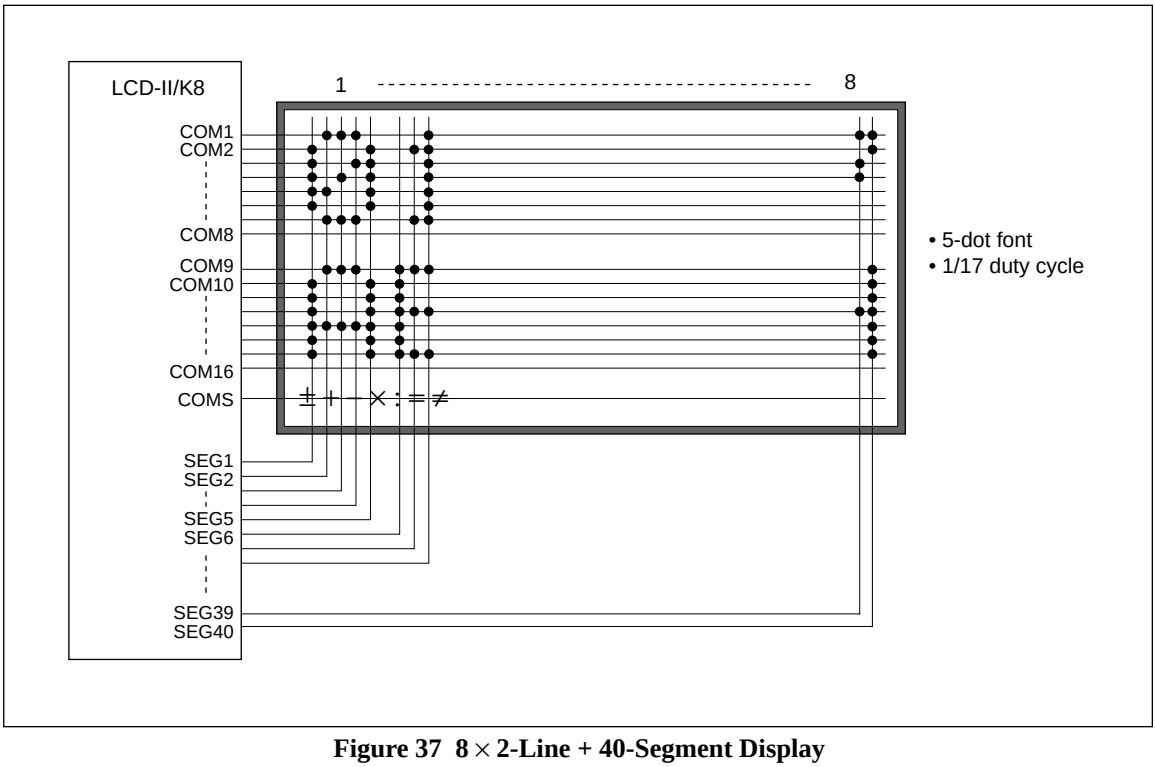


Figure 37 8 × 2-Line + 40-Segment Display

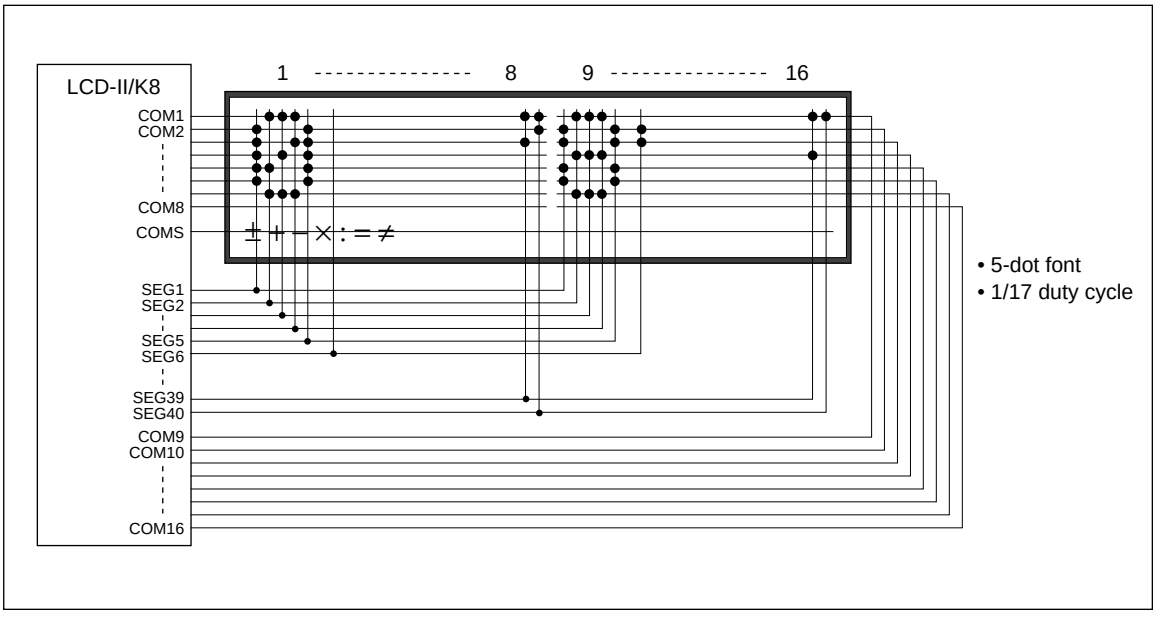


Figure 38 16 × 1-Line + 40-Segment Display (Using the 8 × 2-line Operation Mode)

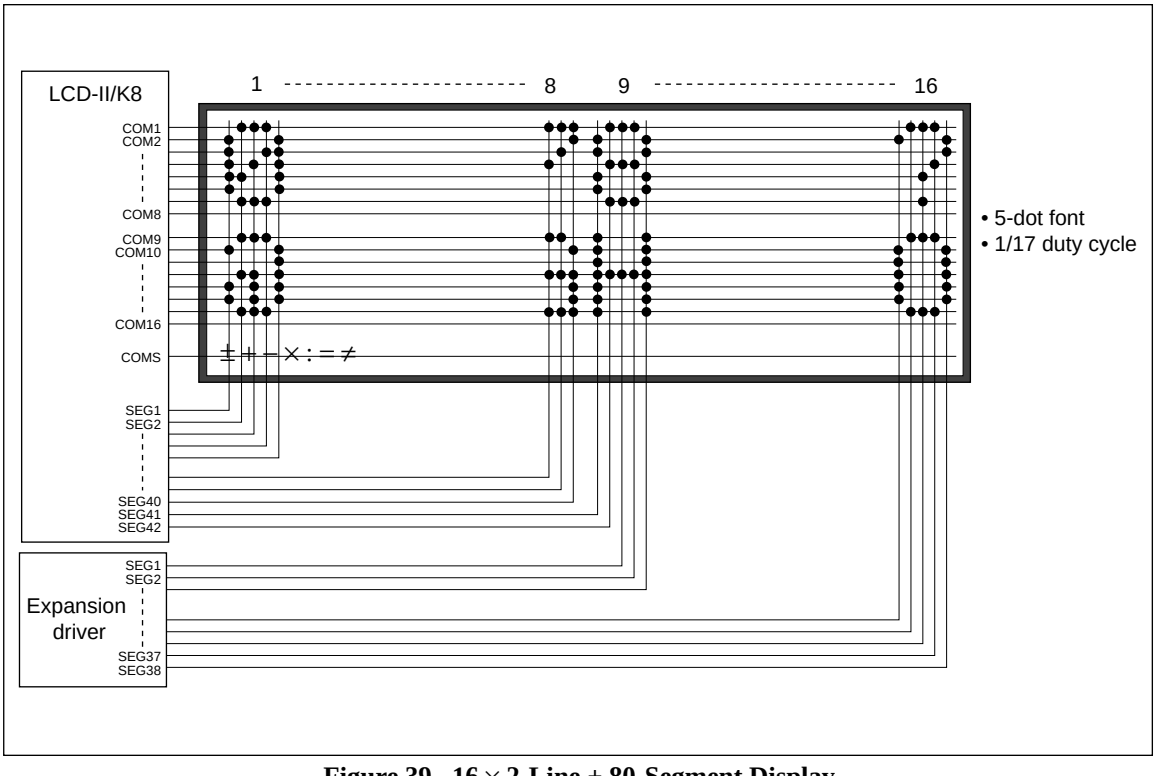


Figure 39 16 × 2-Line + 80-Segment Display

Example of 6-dot font width connection

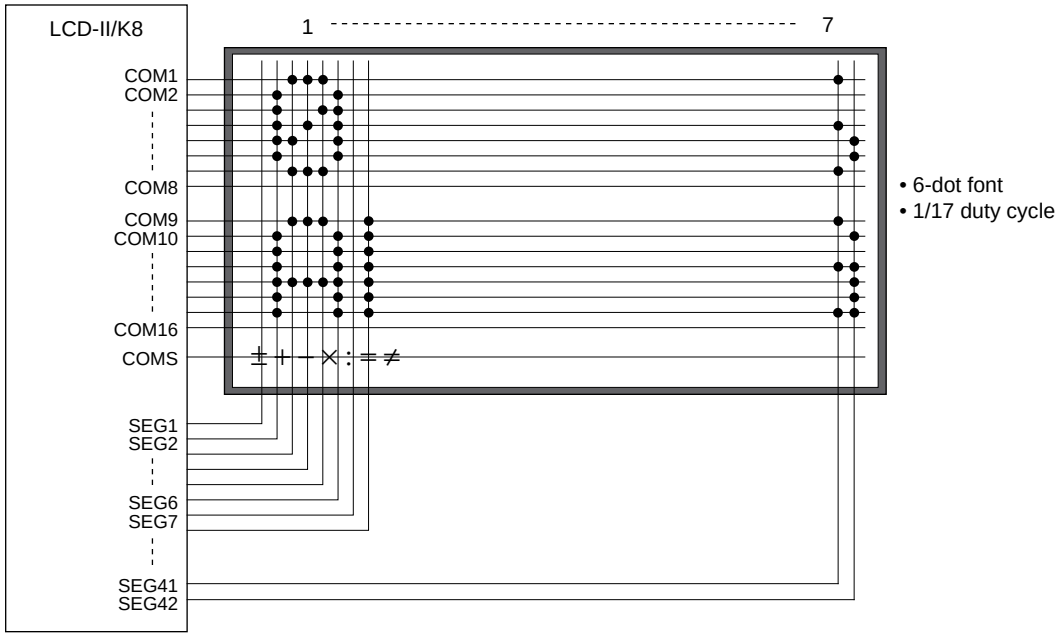


Figure 40 7 × 2-Line + 42-Segment Display

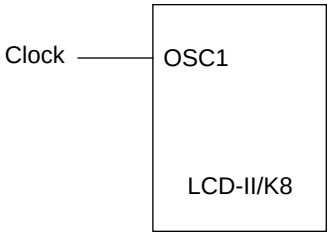
Table 15 Relationship between Oscillation Circuit and Liquid Crystal Display Frame Frequency

		1-Line Display		2-Line Display	
		5-Dot Font Width	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
1-Line Selection period	Normal mode	200 clock cycles	240 clock cycles	100 clock cycles	120 clock cycles
	LP mode	50 clock cycles	60 clock cycles	50 clock cycles	60 clock cycles
Frame frequency		88.9 Hz	74.1 Hz	94.1 Hz	78.4 Hz

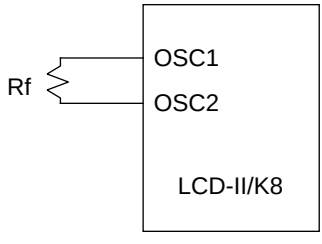
Note: The above values are obtained when the oscillation frequency is 160 kHz (1 clock cycle is 6.25 µs).

Oscillator

1) When an external clock is used



2) When an internal oscillator is used

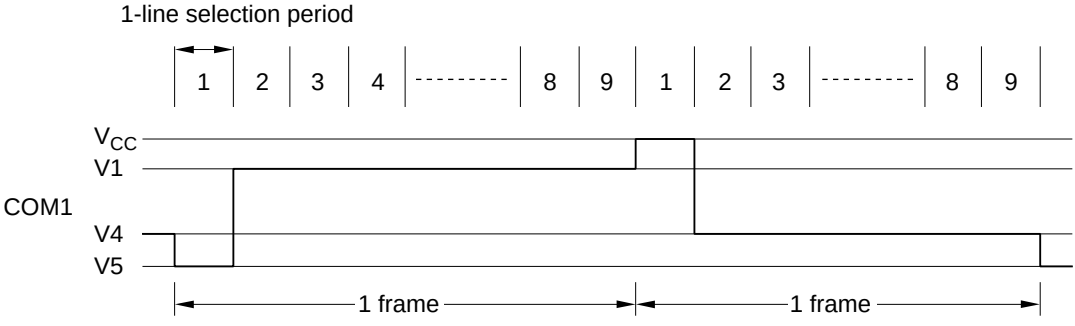


The oscillator frequency can be adjusted by an oscillator resistor (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. The recommended oscillator resistance is as follows.

- Rf = 200 kΩ ± 2% (V_{CC} = 5 V)
- Rf = 160 kΩ ± 2% (V_{CC} = 3 V)

Figure 41 Oscillator

(1) 1/9 duty cycle



(2) 1/17 duty cycle

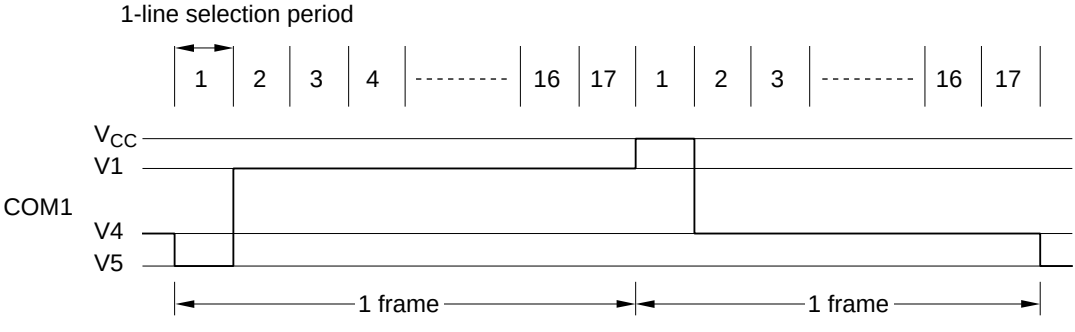


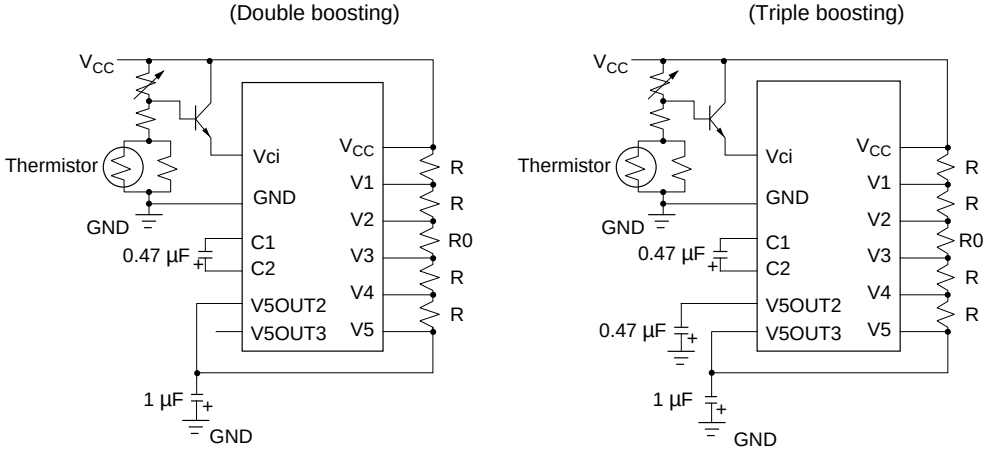
Figure 42 Frame Frequency

Power Supply for Liquid Crystal Display Drive

The LCD-II/K8 incorporates a booster for raising the LCD voltage 2-3 times that of the reference voltage input below V_{CC}. A 2-3 times boosted voltage can be obtained by externally attaching 2 or 3 capacitors.

If the LCD panel is large and needs a large amount of drive current, the value of bleeder resistor that generate the V1 to V5 potential are made smaller. However, the load current in the booster and the voltage drop increases in this case.

We recommend setting the resistance value of each bleeder larger than 4.7 kΩ and to hold down the DC load current to 0.4 mA if using a booster circuit. An external power supply should supply LCD voltage if the DC load current exceeds 0.7 mA. Refer to Electrical Characteristics showing the relationship between the load current and booster voltage output.



Notes:
1. The reference voltage input (Vci) must be set below the power supply (V_{CC}).
2. Current that flows into reference voltage input (Vci) is 2-3 times larger than the load current flowing through a bleeder resistor. Note that a reference voltage drop occurs due to the current flowing into the Vci input when a reference voltage (Vci) is generated by resistor division.
3. The amount of output voltage (V5OUT2/V5OUT3) drop of a booster circuit also increases as the load current flowing through bleeder resistors increases. Thus, set the bleeder resistance as large as possible (4.7 kΩ or greater) without affecting display picture quality.
4. Adjust the reference voltage input (Vci) according to the fluctuation of booster characteristics because the output voltage (V5OUT2/V5OUT3) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors and manufacturing tolerance. Refer to Electrical Characteristics for details.
5. Adjust the reference voltage input (Vci) so that the output voltage (V5OUT2/V5OUT3) after boosting will not exceed the absolute maximum rating of liquid crystal power supply voltage (13 V).
6. Make sure that you connect polarized capacitors correctly.

Figure 43 Example of Power Supply for Liquid Crystal Display Drive (with Internal Boost Circuit)

Table 16 Duty Factor and Bleeder Resistor Value for Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2
Duty factor		1/9	1/17
Bias		1/4	1/5
Bleeder resistance value	R	R	R
	R0	To be short-circuited	R

Note: R changes depending on the size of a liquid crystal panel. Normally, R must be 5 kΩ to 10 kΩ.

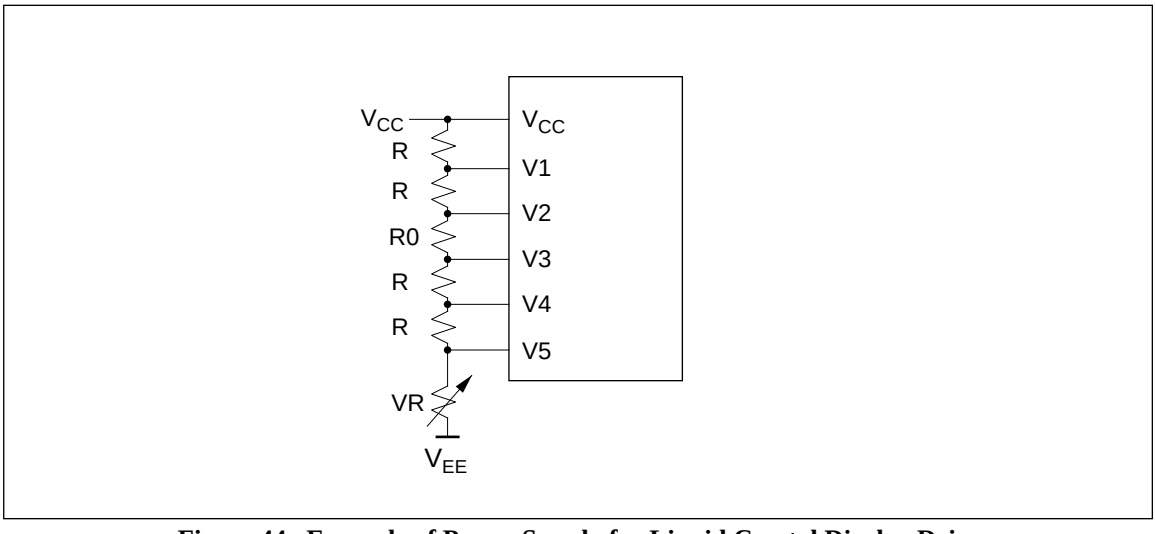


Figure 44 Example of Power Supply for Liquid Crystal Display Drive (with External Power Supply)

Font Display Control

The font width can be specified as 5 dots or 6 dots by setting the font width bit (FW) when the extension register is enabled (RE = 1). Although all fonts stored in CGROM have a 5-dot width, a smoother scroll can be displayed with a 6-dot wide font. Display data stored in CGROM/CGRAM/SEGRAM can be displayed as a mirror image (reflection) in the horizontal direction by setting the font reverse bit (FR). Select according to the LSI mounting method. Set character codes in DDRAM by software since the display read-order of DDRAM does not change.

Horizontal Dot Scroll

Dot unit scrolls are performed by setting the horizontal dot scroll bit (HDS) when the extension register is enabled (RE = 1). By combining this with scroll enable registers, smooth horizontal scrolling in the unit of display line can be performed. In this case, smoother scroll can be performed for a 6-dot font-width display.

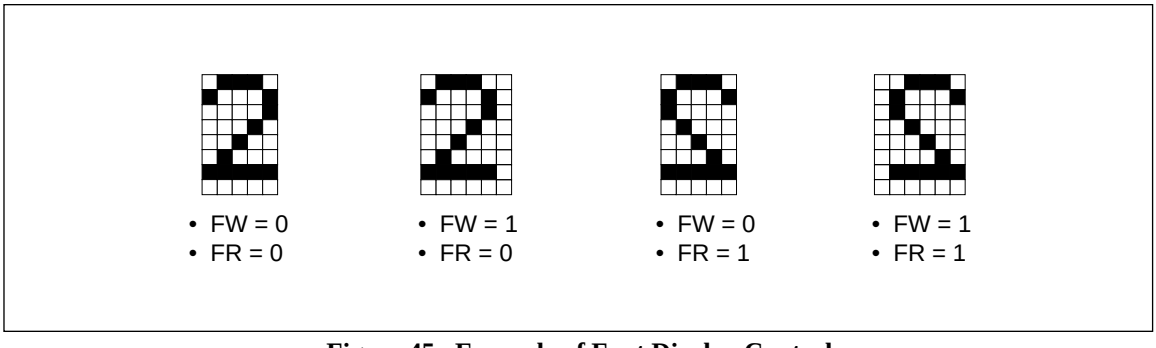


Figure 45 Example of Font Display Control

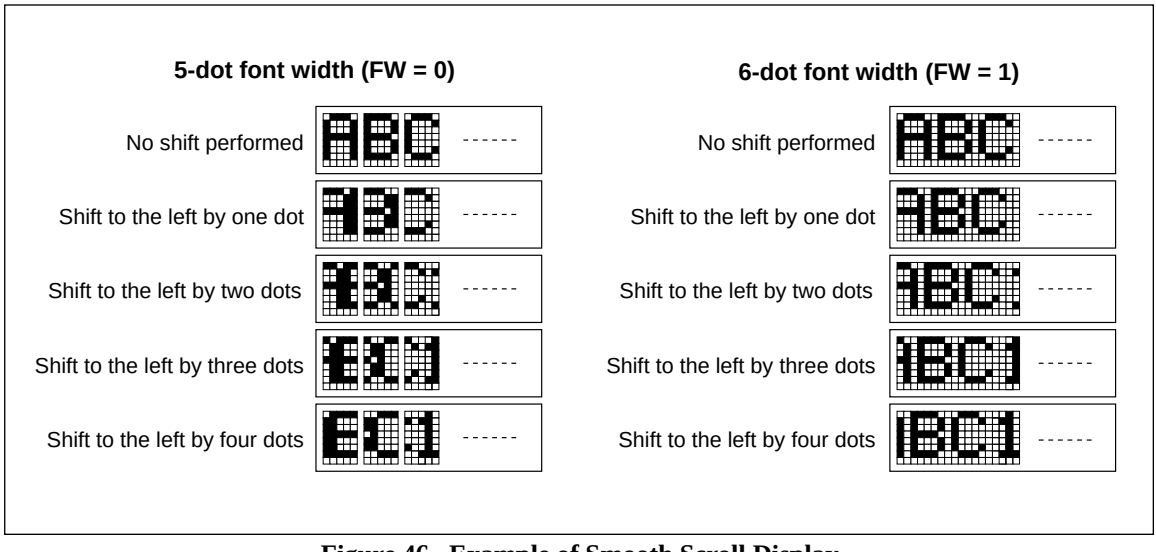
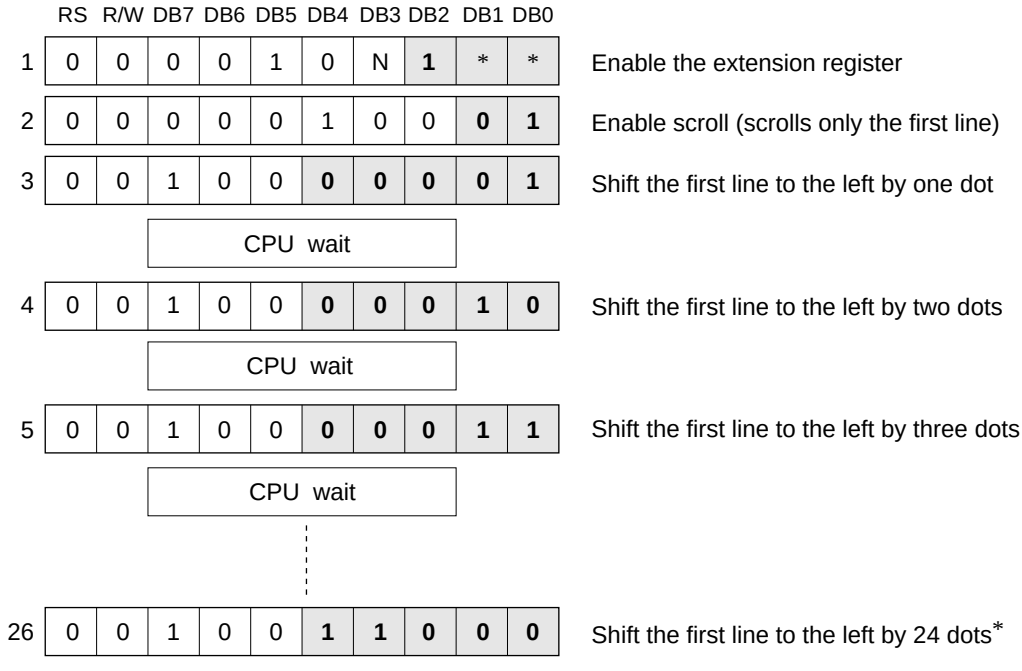


Figure 46 Example of Smooth Scroll Display

Smooth Scroll to the Left

The following shows an example of smooth scroll to the left for no font reflection (FR = 0) and a 6-dot font width (FW = 1). Because the maximum setting for dot smooth scroll (HDS) is 24 dots, scrolling for more than this number can be achieved by shifting to the left by four characters with a display shift instruction or by moving the data in DD RAM by four characters, rewriting them, and then scrolling again. When shifting the display character position with a display shift instruction, the 1st and 2nd line are shifted at the same time and then displayed.

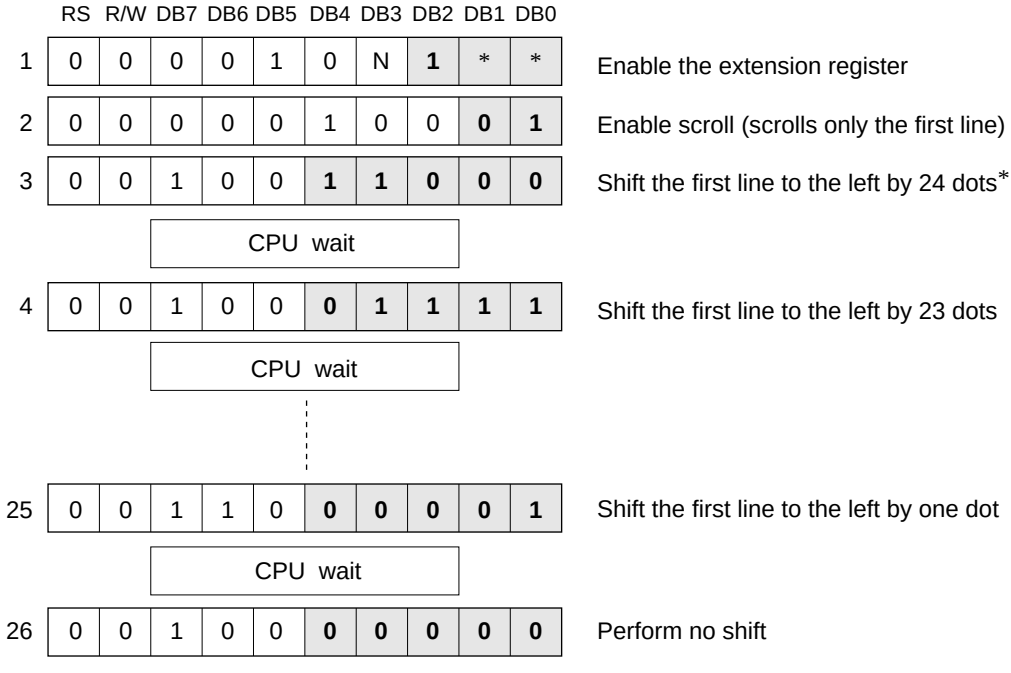


Note: * The sum of the number of characters displayed on the liquid crystal panel and the number of scroll characters must be smaller than the maximum number of display digits.
For example, when 16-digit, 2 lines are displayed with 6-dot font, the maximum number of display digits will be 20, and 4 characters maximum (24 dots) can be specified for scrolling.

Figure 47 Method of Smooth Scroll to the Left

Smooth Scroll to the Right

The following shows an example of smooth scroll to the right for no font reflection (FR = 0) and a 6-dot font width (FW = 1). Because the setting for dot smooth scroll (HDS) specifies a scroll to the left, scrolling to the right can be performed by first shifting the display character position to the right by four characters with a display shift instruction, or by moving the data in DDRAM for only lines to be scrolled by four characters, rewriting, and then scrolling from the 24th dot. When shifting the display character position with a display shift instruction, the 1st and 2nd line are shifted at the same time and then displayed.



Note: * The sum of the number of characters displayed on the liquid crystal panel and the number of scroll characters must be smaller than the maximum number of display digits.
For example, when 16-digit, 2 lines are displayed with 6-dot font, the maximum number of display digits will be 20, and 4 characters maximum (24 dots) can be specified for scrolling.

Figure 48 Method of Smooth Scroll to the Right

Partial Smooth Scroll (Limiting the Number of Characters Scrolled)

Partial smooth scroll displays some characters as fixed and the remaining ones in a horizontal smooth scroll. Here, only the number of left-most characters specified by the PS I/O bits can be fixed. The following shows an example of a smooth scroll performed in dot units from the second character to the eighth character with the PS1/O set to 01 so that the left-most character on the display panel is fixed. For a 2-line display, partial smooth scroll is performed for the display line specified by the scroll enable bits (SE2/1).

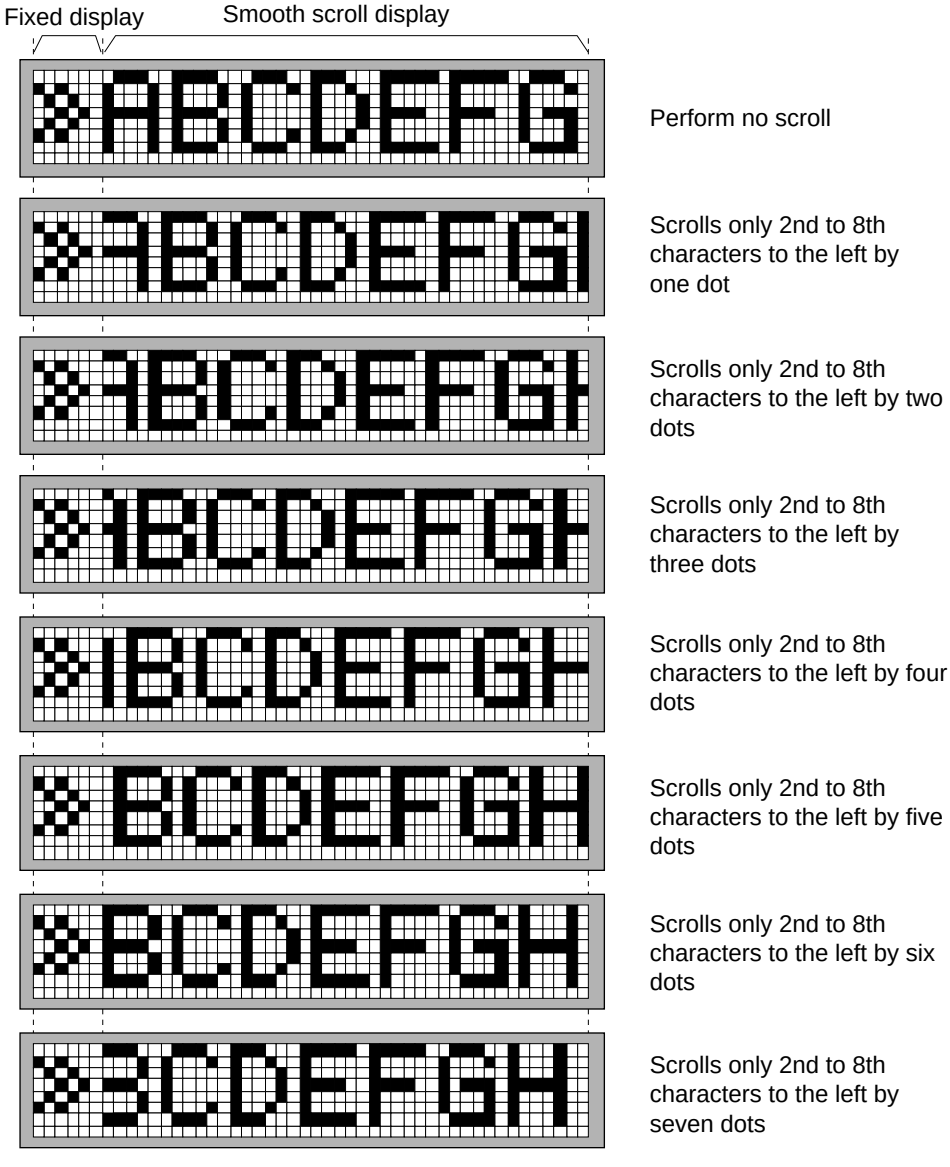


Figure 49 Partial Smooth Scroll

Low Power Mode

The HD66720 enters low power mode by setting the low-power mode bit (LP) to 1. During low-power mode, as the internal operation frequency is divided by 2 (1-line display mode) or by 4 (2-line display mode), the execution time of each instruction becomes two times or four times longer than normal. Be careful when writing instructions without performing busy flag checking.

During low power mode, a maximum of 10 characters are displayed per line. The DDRAM setting value become invalid from the 11th character. Note that the display differs from normal mode when display shifts or horizontal smooth scrolls are performed.

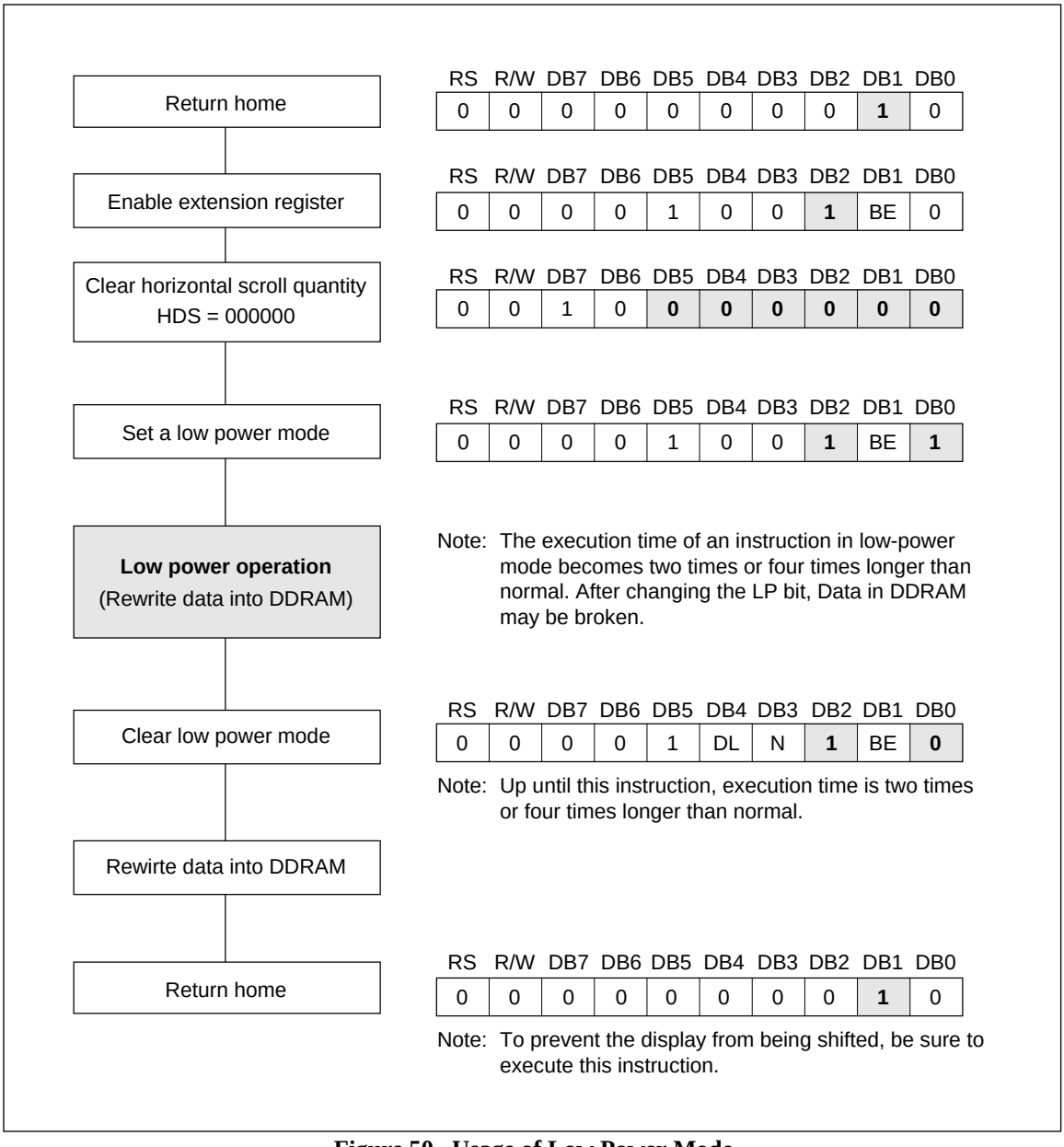


Figure 50 Usage of Low Power Mode

Sleep Mode

The HD66720 enters sleep mode by setting the sleep mode bit (SLP) to 1. During sleep mode, the display controller and LCD internal operation frequency is divided by 16, significantly reducing consumption current. However, the LCD will not perform normally at this time because the LCD frame frequency is also divided by 32, and the display should be turned off (D = 0). In this case, a scanning line may appear. To avoid this, the LCD driving voltage (V_{LCD}) should be cut off. The VLCD can be decreased by controlling the voltage of the Vci terminal flowing into the internal booster. In addition, execution time of each instruction becomes 16 times longer, and caution is needed when writing instructions without performing busy flag checking. The key scan circuit during sleep mode operates at the usual operation frequency. Key scan such as power-on keys can be performed by suppressing consumption current during system standby.

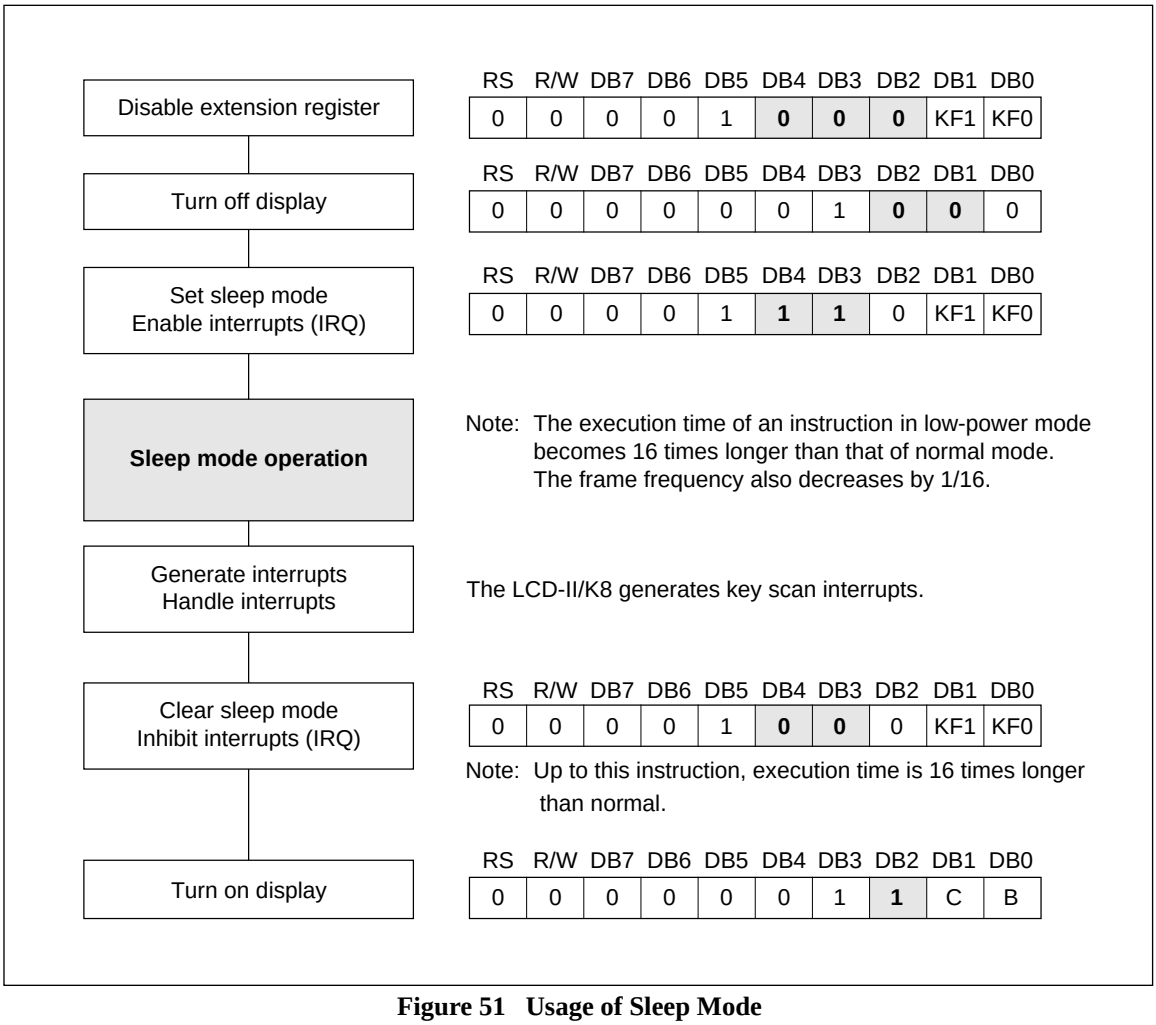


Figure 51 Usage of Sleep Mode

Relationship between Instruction and Display

Table 17 10-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66720 is initialized by the internal reset circuit)											Initialized. No display.
2	Display on/off control	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
3	Entry mode set	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right when writing to the RAM. Display is not shifted.
4	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	H_	Writes H. DD RAM has already been selected by initialization.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	1	HI_	Writes I.
	. . . . .										. . . . .	
6	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
7	Entry mode set	0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
8	Write data to CG RAM/DD RAM	1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 17 10-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CG RAM/DD RAM										ITACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
	. . . . .										. . . . .	
10	Write data to CG RAM/DD RAM										MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
11	Cursor or display shift										MICROCO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	0	0		
12	Cursor or display shift										MICROCO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	0	0		
13	Write data to CG RAM/DD RAM										ICROCO	Writes C. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
14	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	0	0		
15	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	0	0		
16	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
	. . . . .										. . . . .	
17	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 18 8-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66720 is initialized by the internal reset circuit)											Initialized. No display.
2	Display on/off control	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
3	Entry mode set	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
4	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization.
	. . . . .											. . . . .	
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.

Table 18 8-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
6	Set DDRAM address										HITACHI _	Sets the DDRAM address so that the cursor positioned on the head of the second line.
	0	0	1	1	0	0	0	0	0	0		
7	Write data to CG RAM/DD RAM										HITACHI M_	Writes a space.
	1	0	0	1	0	0	1	1	0	1		
	. . .										. . .	
8	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
9	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
10	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
11	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary. Note that instructions are not accepted for 80 ms in 3-V operation or for 40 ms in 5-V operation after power is on since the HD66720 is in an internal reset state. Send an instruction after waiting for an appropriate amount of time after power-on.

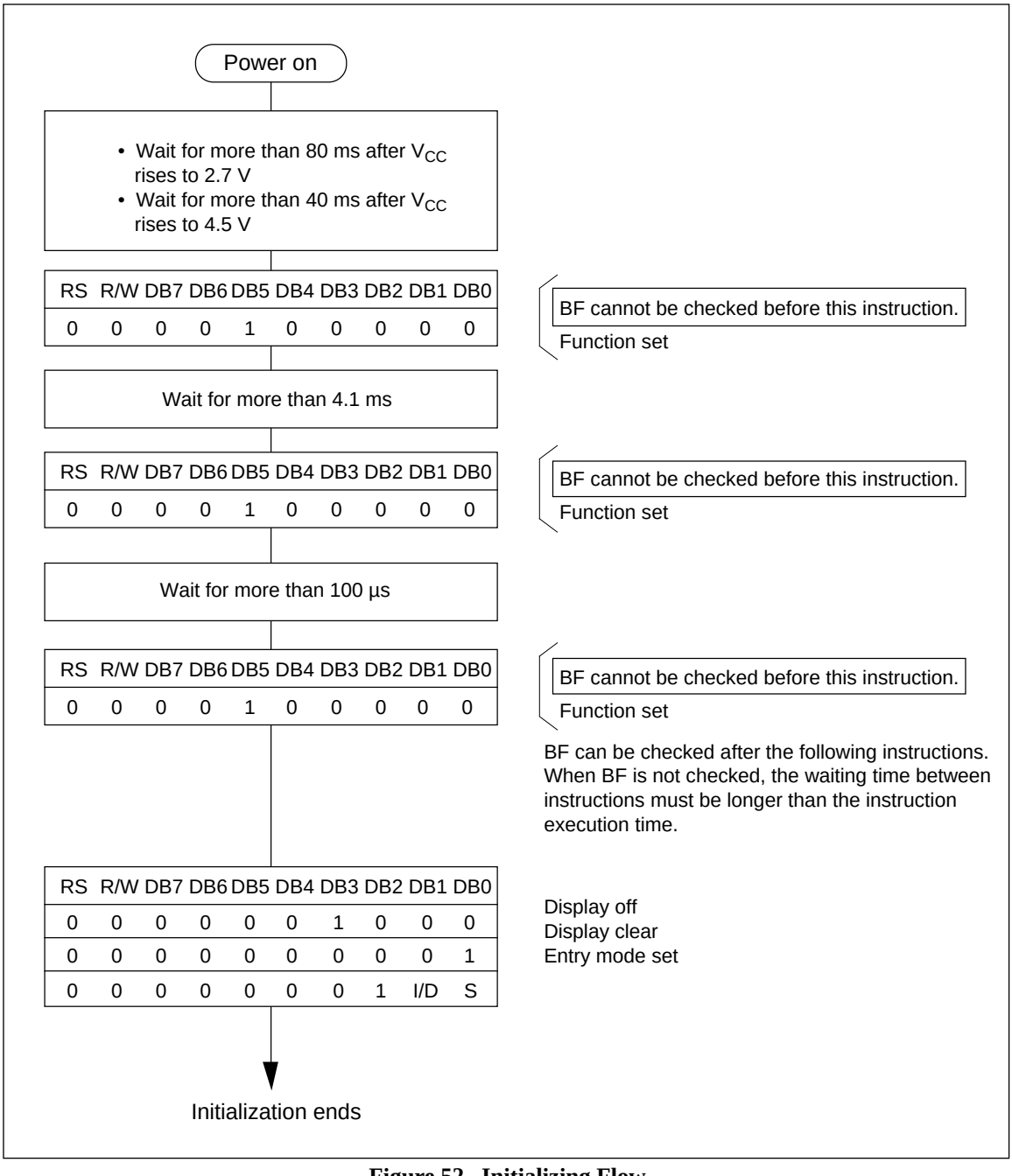


Figure 52 Initializing Flow

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +13.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (1) (except OSC1)	V_{IH1}	0.7V_{CC}	—	V_{CC}	V		5, 6
Input low voltage (1) (except OSC1)	V_{IL1}	–0.3	—	0.2V_{CC}	V	V_{CC} = 2.7 to 3.0 V	5, 6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC1)	V_{IH2}	0.7V_{CC}	—	V_{CC}	V		7
Input low voltage (2) (OSC1)	V_{IL2}	—	—	0.2V_{CC}	V		7
Output high voltage (1) (except KST, IRQ*)	V_{OH1}	0.75V_{CC}	—	—	V	$-I_{OH}$ = 0.1 mA	5, 8
Output high voltage (2) (KST, IRQ*)	V_{OH2}	0.7V_{CC}	—	—	V	$-I_{OH}$ = 1 µA	5, 10
Output low voltage (1) (except KST, LED, IRQ*)	V_{OL1}	—	—	0.2V_{CC}	V	I_{OL} = 0.1 mA	5, 9
Output low voltage (2) (KST, IRQ*)	V_{OL2}	—	—	0.2V_{CC}	V	I_{OL} = 0.5 mA	5, 10
Output low voltage (3) (LED 0/1)	V_{OL3}	—	—	1.2	V	I_{OL} = 10 mA, V_{CC} = 3 V	5, 11
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	12
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	12
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	13
Pull-up MOS current (KIN0-KIN4)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	5, 14
Current consumption — Normal display	I_{CC1}	—	85	170	µA	Rf oscillation, external clock V_{CC} = 3V, f_{OSC} = 160 kHz	15, 16
Current consumption — Sleep mode	I_{CC2}	—	40	100	µA		
LCD voltage	V_{LCD1}	3.0	—	11.0	V	V_{CC}–V5, 1/5 bias	17

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	V_{ci} = 4.5 V, I_O = 0.25 mA, T_a = 25°C	20
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.8	—	V	V_{ci} = 3 V, I_O = 0.25 mA, T_a = 25°C	20
Input voltage	V_{Ci}	2.0	—	4.5	V		20

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	100	150	400	kHz		18
	External clock duty cycle	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{rcp}	—	—	0.2	µs		
Rf oscillation	Clock oscillation frequency	f_{OSC}	120	160	210	kHz	R_f = 160 kΩ, V_{CC} = 3 V	19

Serial Interface Timing (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 53
Serial clock high level width	t_{SCH}	400	—	—	ns	
Serial clock low level width	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	0	—	—		

Serial Interface Timing (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 53
Serial clock high level width	t_{SCH}	200	—	—	ns	
Serial clock low level width	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100	—	—		
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	0	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 54
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Key Scan Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Key strobe low level width	5-dot font width	t_{KLW}	—	200Tc	—	ms	Figure 55
	6-dot font width	t_{KLW}	—	240Tc	—		
Key strobe frequency	5-dot font width	t_{KC}	—	1200Tc	—		
	6-dot font width	t_{KC}	—	1440Tc	—		

Note: Tc = $1/f_{osc}$

Reset Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 56

Power Supply Conditions Using Internal Reset Circuit

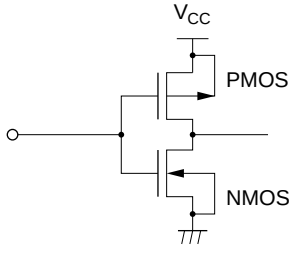
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 57
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

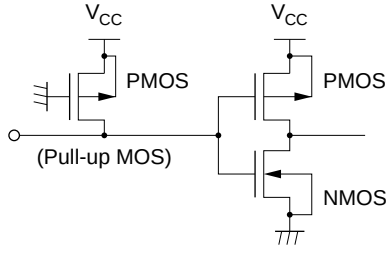
1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic conditions are exceeded, the LSI may malfunction or cause poor reliability.
2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

Input pin

Applies to pins SCLK, CS*, SID, and TEST1/2

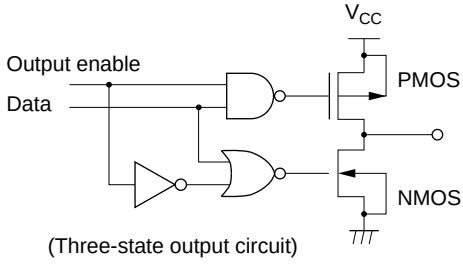


Applies to pins KIN0 to KIN4 and RESET*



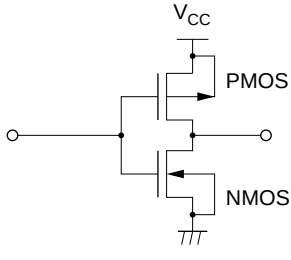
Output pin

Applies to pin SOD



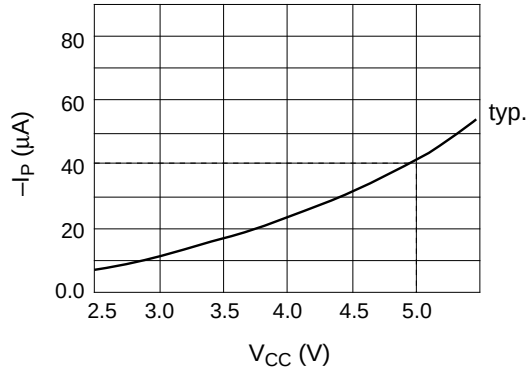
(Three-state output circuit)

Applies to pins CL1, CL2, M, D, KST0 to KST5, IRQ*, and LED0/1

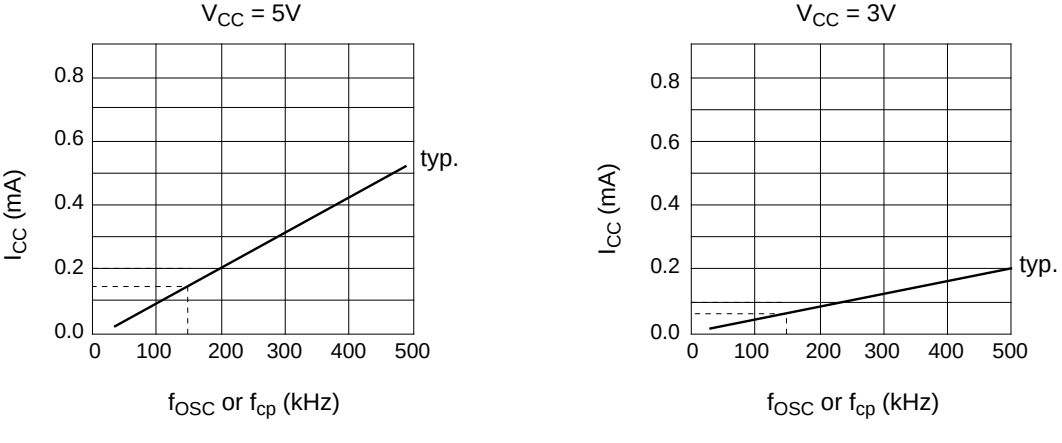


6. Applies to input pins, excluding the OSC_1 pin. However, the TEST1/2 pins must be grounded (GND).
7. Applies to the OSC_1 pin.
8. Applies to output pins, excluding pins KST0 to KST5 and LCD output pins.
9. Applies to output pins, excluding pins KST0 to KST5, pins LED0/1, and LCD output pins.
10. Applies to pins KST0 to KST5.

11. Applies to LED0/1 output pins.
12. Applies to resistor values (RCOM) between power supply pins V_{CC}, V1, V4, V5 and common signal pins (COM1 to COM16 and COMS), and resistor values (RSEG) between power supply pins V_{CC}, V2, V3, V5, and segment signal pins (SEG1 to SEG42).
13. Current that flows through pull-up MOS and output drive MOS is excluded.
14. Applies to the pull-up MOS of pins KIN0 to KIN4. The following shows the relationship between the power supply voltage (V_{CC}) and pull-up MOS current ($-I_p$) (referential data).

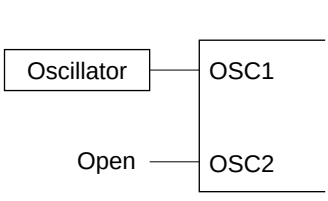


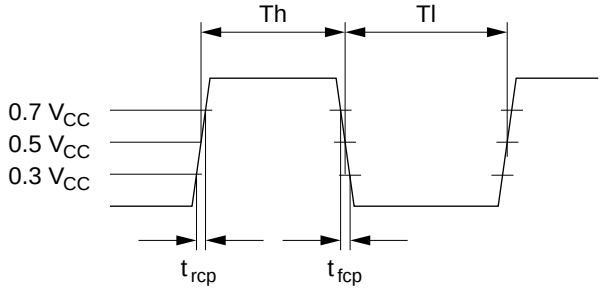
15. This excludes the current flowing through the I/O section. The input level must always be at a specified high or low level because through current increases if the CMOS input is left floating.
16. The following shows the relationship between the operation frequency (f_{OCS} or f_{cp}) and current consumption (I_{CC}).



17. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

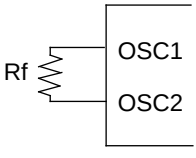
18. Applies to the external clock input.





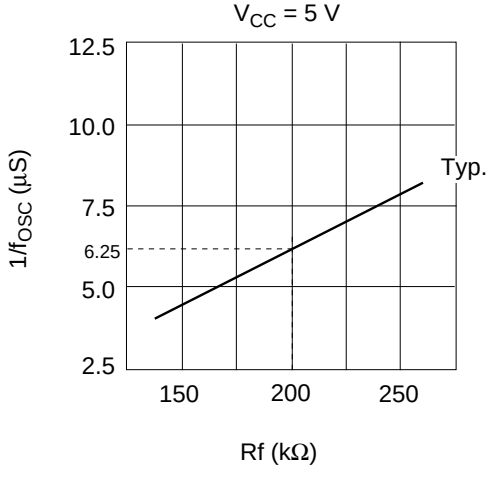
$$\text{Duty cycle} = \frac{Th}{Th + Tl} \times 100\%$$

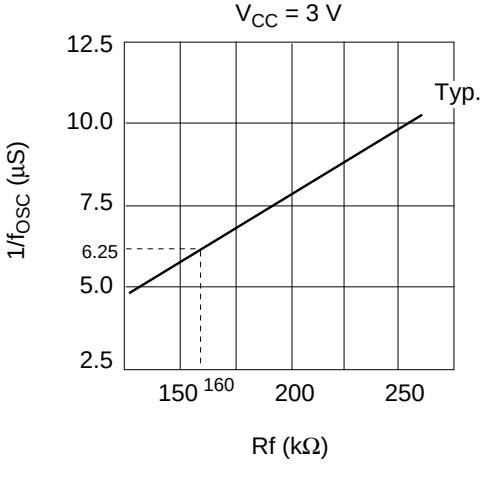
19. Applies to internal oscillator operations when oscillator Rf is used.



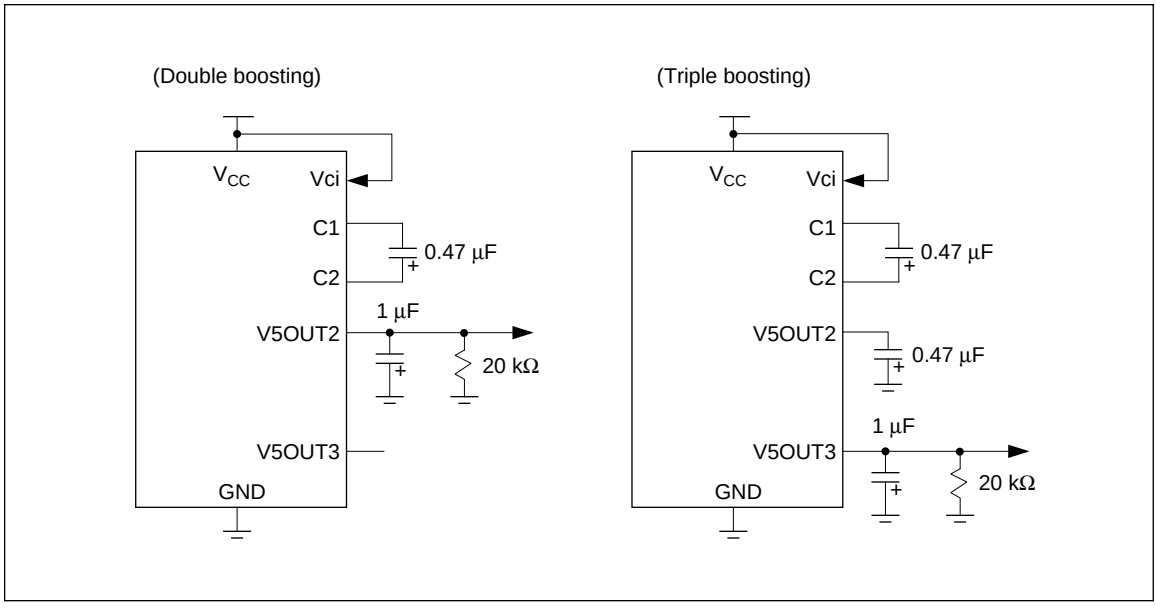
Rf: 160 kΩ ± 2% (when V_{CC} = 3 V to 4 V)
Rf: 200 kΩ ± 2% (when V_{CC} = 4 V to 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

The following shows the relationship between the Rf oscillator resistor value and oscillator frequency (referential data).



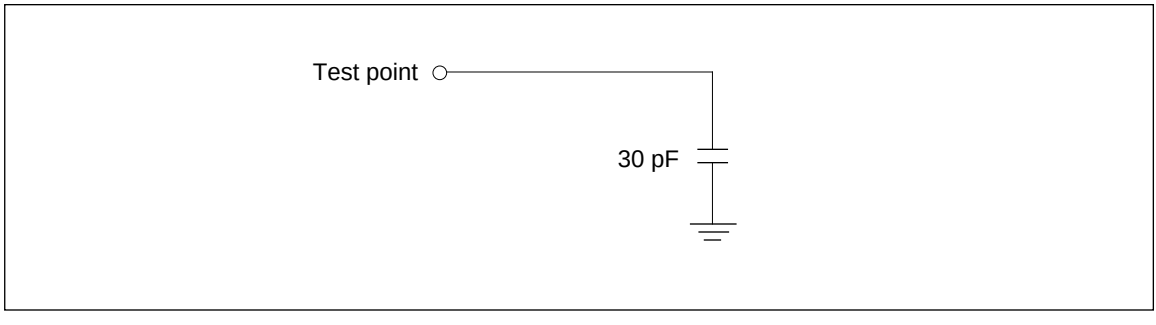


20. Booster characteristics test circuits are shown below.



Load Circuits

AC Characteristics Test Load Circuits



Timing Characteristics

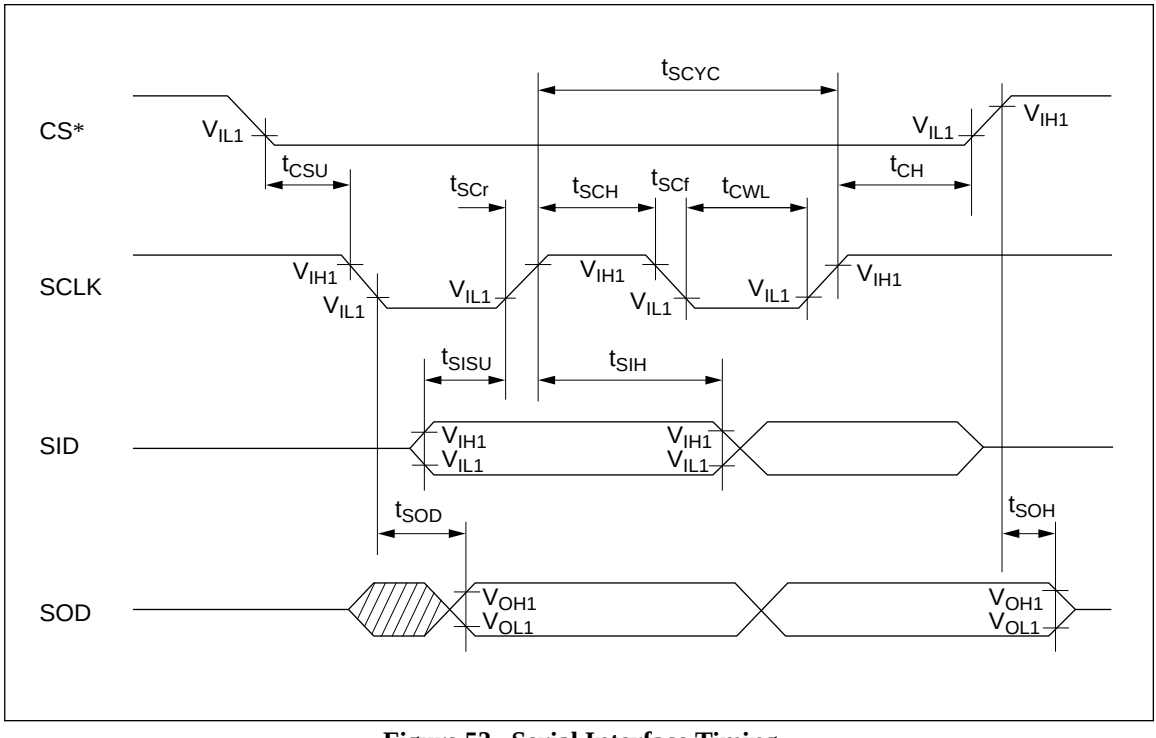


Figure 53 Serial Interface Timing

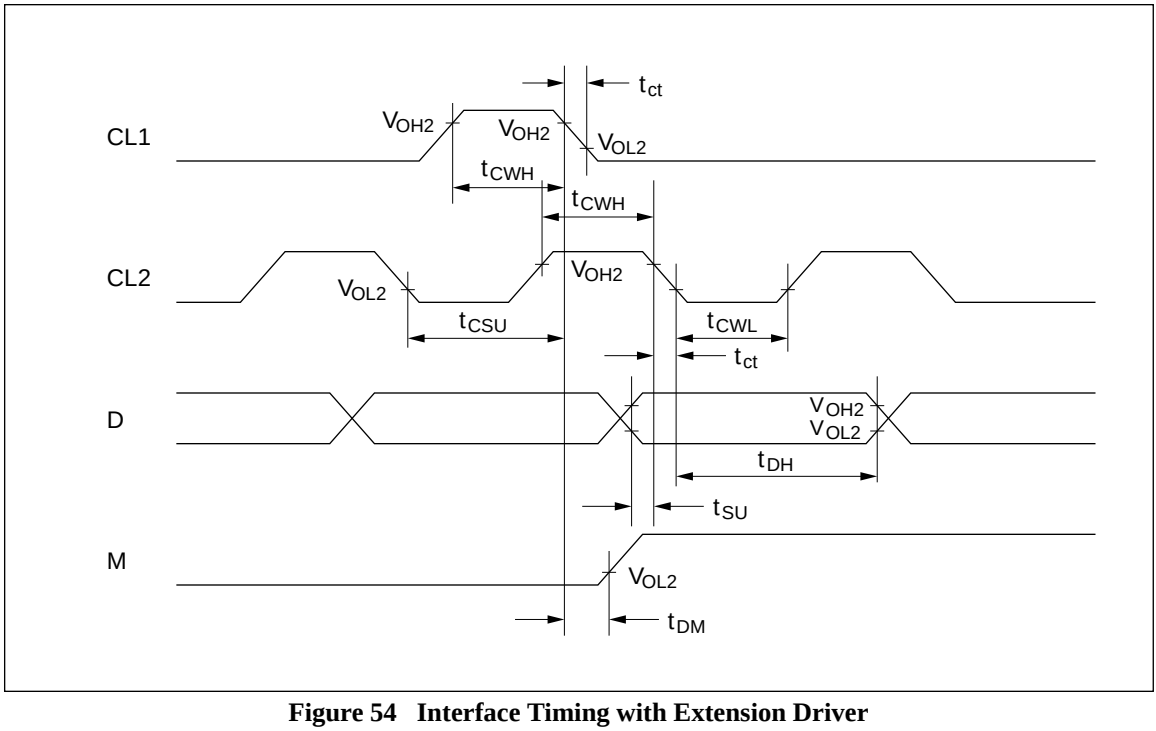


Figure 54 Interface Timing with Extension Driver

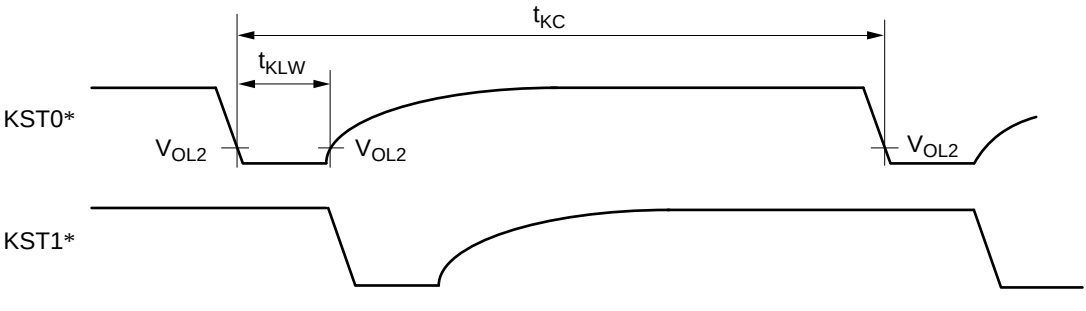
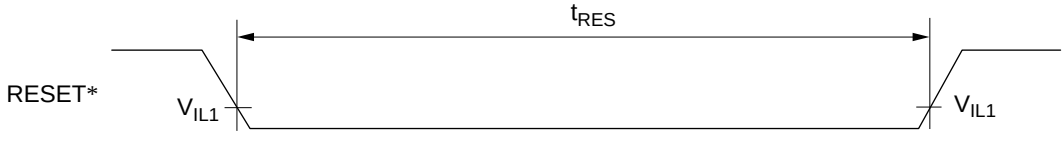
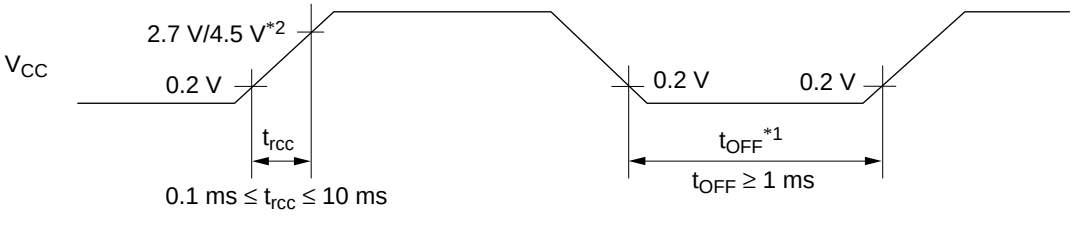


Figure 55 Key Strobe Timing



Note: When power is supplied, initializing by the internal reset circuit has priority. Accordingly, the above RESET* input is ignored during internal reset period.

Figure 56 Reset Timing



Notes:
1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, initialize by instruction. (Refer to Initializing by Instruction.)

Figure 57 Power Supply Sequence

HD66730 (LCD-II/J6)

(Dot-Matrix Liquid Crystal Display Controller/Driver Supporting Japanese Kanji Display)

Preliminary

HITACHI

Description

The HD66730 is a dot-matrix liquid crystal display controller (LCD) and driver LSI that displays Japanese characters consisting of kanji, hiragana and katakana according to the Japanese Industrial Standard (JIS) Level-1 Kanji Set. The HD66730 incorporates the following five functions on a single chip: (1) display control function for the dot matrix LCD, (2) a display RAM to store character codes, (3) ROM fonts to support kanji, (4) liquid crystal driver, and (5) a booster to drive the LCD. A 2-line 6-character kanji display can easily be achieved by receiving character codes (2 bytes/character) from the MPU.

The font ROM includes 2,965 kanji from the JIS Level-1 Kanji Set, 524 JIS non-kanji characters, and 128 half-size alphanumeric characters and symbols. Full-size fonts such as Japanese kanji and half-size of fonts such as alphanumeric characters can be displayed together.

In addition, display control equivalent to full bit mapping can be performed through horizontal and vertical dot-by-dot smooth scroll functions for each display line. To help make systems more compact, a three-line clock synchronous serial transfer method is adopted in addition to an 8-bit bus for interfacing with a microcomputer.

Features

- Dot-matrix liquid crystal display controller/driver supporting the display of kanji according to JIS Level-1 Kanji Set
- Large character generator ROM: 510 kbits
  - — Kanji according to JIS Level-1 Kanji Set (11 × 12 dots): 2,965-character font
  - — JIS non-kanji (11 × 12 dots): 524-character font
  - — Half-size alphanumeric characters and symbols (5 × 12 dots): 128-character font
- Display of 11 × 12 dots for full-size fonts consisting of kanji and kana, 5 × 12 dots for half-size fonts of alphanumeric characters and symbols in the same display
- 2-line 6-character full-size font display with a single chip (1/27 duty)
- Expansion driver interface: maximum 2-line 20-character (or 4-line 10-character) display
- Dot matrix font and 71 marks and icons (96 at extension)
- Various display control functions: horizontal smooth scroll (in dot units), vertical smooth scroll, white black inversion/blinking/white black inversion blinking character display, cursor display, display on/off
- Display data RAM: 40 × 2 bytes (stores codes to support 40 characters in a full-size font)
- Character generator RAM: 8 × 26 bytes (displays 8 characters of a 12 × 13 dot user font)
- 16-byte 96-segment RAM
- Three-line clock synchronous serial bus, 8-bit bus interface
- Built-in double/triple liquid-crystal voltage booster circuit and built-in oscillator (operating frequency can be adjusted through external resistors)
- Operating power supply voltage: 2.7 V to 5.5 V; liquid crystal display voltage: 3.0 V to 13.0 V
- QFP 1420-128 (0.5-mm pitch), bare-chip

Hitachi semiconductor

List 1 Programmable Duty Cycles

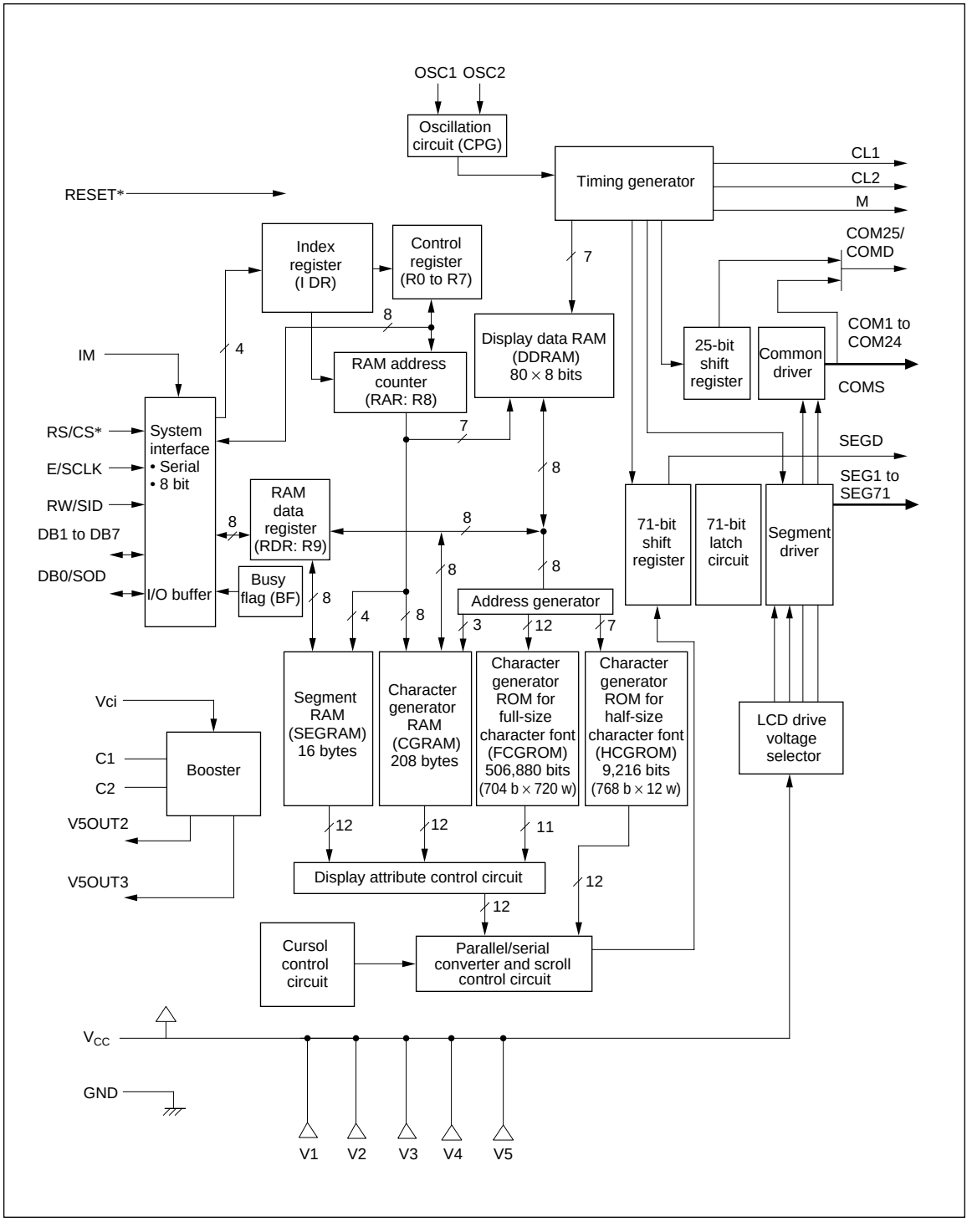
Duty Drive Setting	Number of Display Characters in Full-Size Font (Number of Segments/Marks)			Display Line Setting
	1-Chip Operation	Extension Display	Extension Drivers*	
1/14	1-line 6 characters (71)	1-line 40 characters (96)	10 drivers	1line, 2 lines
1/27	2-line 6 characters (71)	2-line 20 characters (96)	5 drivers	2 lines, 4 lines
1/40	—	3-line 10 characters (96)	3 drivers	4 lines
1/53	—	4-line 10 characters (96)	3 drivers	4 lines

Note: Number of extension driver with 40 outputs (HD44100R)

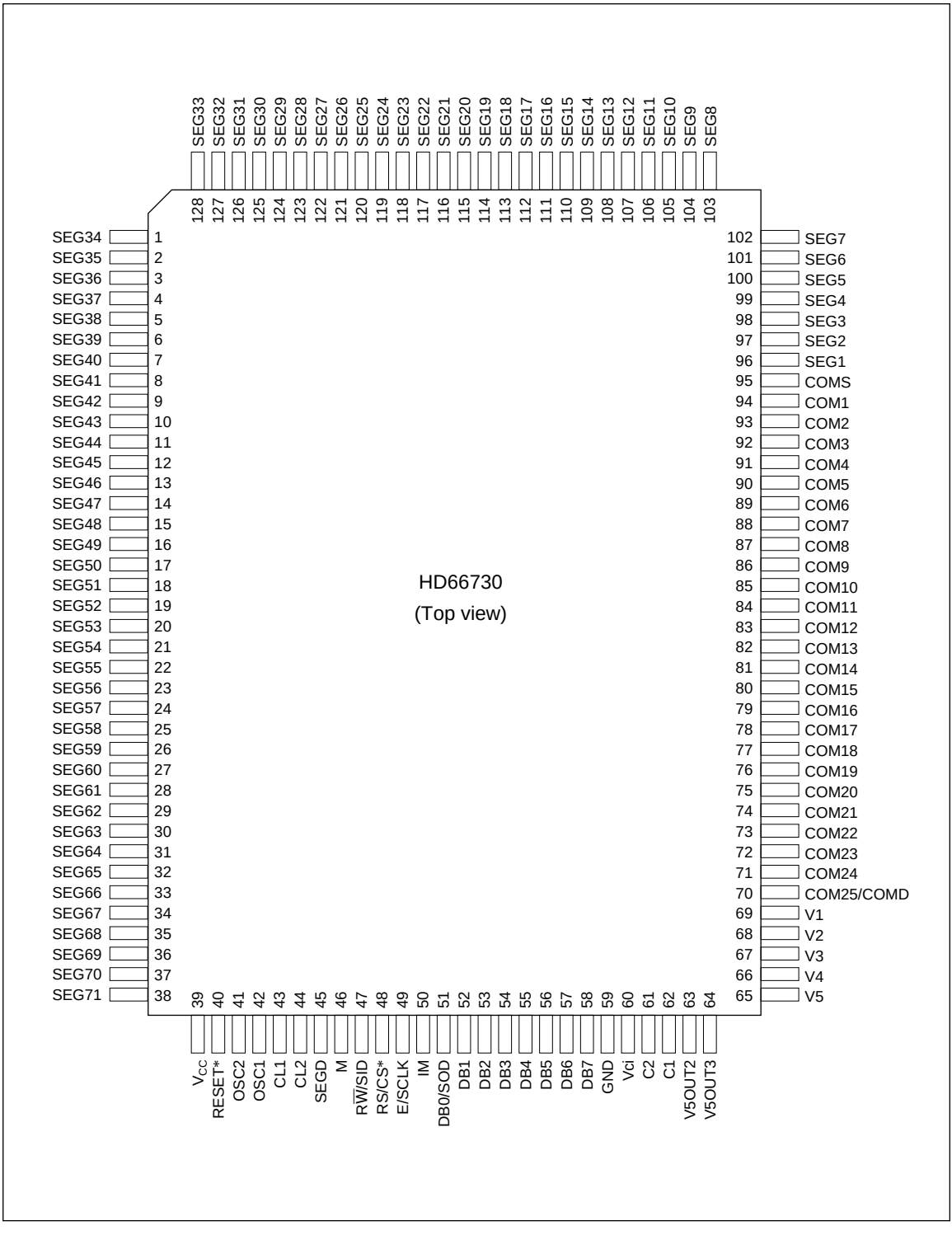
Ordering Information

Type No.	Package	CGROM
HD66730A00FS	FP-128	Japanese Kanji standard
HCD66730A00	Chip	

Block Diagram

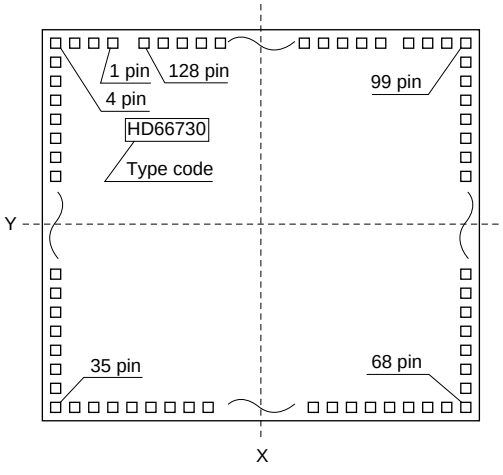


Pin Arrangement



The Location of Bonding Pads

HCD66730



Chip size (X × Y): 7.48 × 6.46 mm^2
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 × 100 µm^2

(unit: µm)

Pin No.	Function	Coordinate X	Coordinate Y
1	SEG34	–2602	3012
2	SEG35	–2984	3012
3	SEG36	–3263	3012
4	SEG37	–3522	3012
5	SEG38	–3522	2782
6	SEG39	–3522	2582
7	SEG40	–3522	2341
8	SEG41	–3522	2161
9	SEG42	–3522	1981
10	SEG43	–3522	1801
11	SEG44	–3522	1621
12	SEG45	–3522	1440
13	SEG46	–3522	1260
14	SEG47	–3522	1030
15	SEG48	–3522	800
16	SEG49	–3522	620
17	SEG50	–3522	439
18	SEG51	–3522	259
19	SEG52	–3522	79
20	SEG53	–3522	–101
21	SEG54	–3522	–281
22	SEG55	–3522	–462
23	SEG56	–3522	–642
24	SEG57	–3522	–822
25	SEG58	–3522	–1002
26	SEG59	–3522	–1182
27	SEG60	–3522	–1363
28	SEG61	–3522	–1543
29	SEG62	–3522	–1723
30	SEG63	–3522	–1939
31	SEG64	–3522	–2183
32	SEG65	–3522	–2364
33	SEG66	–3522	–2544
34	SEG67	–3522	–2774
35	SEG68	–3522	–2984
36	SEG69	–3160	–2984
37	SEG70	–2860	–2984
38	SEG71	–2660	–2984
39	V_{CC}	–2435	–2984
40	RESET*	–2233	–2984
41	OSC2	–2063	–2984
42	OSC1	–1859	–2984
43	CL1	–1689	–2984
44	CL2	–1519	–2984
45	SEGD	–1349	–2984
46	M	–1179	–2984
47	RW/SID	–975	–2984
48	RS/CS*	–771	–2984
49	E/SCLK	–567	–2984
50	IM	–363	–2984
51	DB0/SOD	–146	–2984
52	DB1	71	–2984
53	DB2	287	–2984
54	DB3	504	–2984
55	DB4	721	–2984
56	DB5	938	–2984
57	DB6	1154	–2984
58	DB7	1371	–2984
59	GND	1533	–2984
60	Vci	1730	–2959
61	C2	1896	–2959
62	C1	2057	–2959
63	V5OUT2	2219	–2959
64	V5OUT3	2478	–2959
65	V5	2782	–2984
66	V4	3016	–2984
67	V3	3253	–2984
68	V2	3522	–2984
69	V1	3522	–2806
70	COM25/D	3522	–2626
71	COM24	3522	–2445
72	COM23	3522	–2265
73	COM22	3522	–2085
74	COM21	3522	–1855
75	COM20	3522	–1625
76	COM19	3522	–1444
77	COM18	3522	–1264
78	COM17	3522	–1084
79	COM16	3522	–854
80	COM15	3522	–624
81	COM14	3522	–443
82	COM13	3522	–263
83	COM12	3522	–83
84	COM11	3522	97
85	COM10	3522	277
86	COM9	3522	458
87	COM8	3522	638
88	COM7	3522	818
89	COM6	3522	998
90	COM5	3522	1178

Pin No.	Function	Coordinate X	Coordinate Y
91	COM4	3522	1409
92	COM3	3522	1639
93	COM2	3522	1819
94	COM1	3522	1999
95	COMS	3522	2179
96	SEG1	3522	2410
97	SEG2	3522	2590
98	SEG3	3522	2819
99	SEG4	3522	3012
100	SEG5	3222	3012
101	SEG6	2942	3012
102	SEG7	2662	3012
103	SEG8	2332	3012
104	SEG9	2152	3012
105	SEG10	1972	3012
106	SEG11	1791	3012
107	SEG12	1611	3012
108	SEG13	1431	3012
109	SEG14	1251	3012
110	SEG15	1071	3012
111	SEG16	890	3012
112	SEG17	710	3012
113	SEG18	530	3012
114	SEG19	350	3012
115	SEG20	170	3012
116	SEG21	–11	3012
117	SEG22	–191	3012
118	SEG23	–371	3012
119	SEG24	–551	3012
120	SEG25	–731	3012
121	SEG26	–912	3012
122	SEG27	–1092	3012
123	SEG28	–1272	3012
124	SEG29	–1452	3012
125	SEG30	–1632	3012
126	SEG31	–1813	3012
127	SEG32	–1993	3012
128	SEG33	–2173	3012

Pin Function

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
RESET*	1	I	—	Acts as a reset input pin. The LSI is initialized during low level. Refer to Reset Function.
IM	1	I	—	Selects interface mode with the MPU; Low: Serial mode High: 8-bit bus mode
RS/CS*	1	I	MPU	Selects registers during bus mode: Low: Index register (write); Status register (read) High: Control register (write); RAM data (read/write) Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
R$\overline{W}$/SID	1	I	MPU	Selects read/write during bus mode; Low: Write High: Read Inputs serial data during serial mode.
E/SCLK	1	I	MPU	Starts data read/write during bus mode; Inputs (Receives) serial clock during serial mode.
DB_1 to DB_7	7	I/O	MPU	Seven high-order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66730. DB7 can be used as a busy flag. Open these pins during serial mode since these signals are not used.
DB0/ SOD	1	I/O /O	MPU	The lowest bidirectional data bit (DB0) during bus mode. Outputs (transmits) serial data during serial mode. Open this pin if reading (transmission) is not performed.
SEG_1 to SEG_{71}	71	O	LCD	Display data output signals for the segment extension driver.
COMS	1	O	LCD	Acts as a common output signal for segment display. Used to display icon and marks beside the character display.
COM_1 to COM_{24}	24	O	LCD	Acts as common output signals for character display. COM_{15} toCOM_{24} become non-selective waveforms when the duty ratio is 1/14.
COM_{25}/ COMD	1	O	LCD/ extension driver	Acts as common output signal (COM25) for character display when EXT2 bit is 0. Acts as a common extension pulse signal (COMD) when EXT2 bit is 1. The pin is grounded after RESET input is cleared.

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
CL1	1	O	Extension driver	Outputs the latch pulse of segment extension driver. Can also be used as a shift clock of common extension driver. Enters tristate when both EXT1 and EXT2 are 0.
CL2	1	O	Extension driver	Outputs shift clock of segment extension driver. Can also be used as a common extension driver latch clock. Enters tristate when both EXT1 and EXT2 are 0.
SEGD	1	O	Extension driver	Outputs data of extension driver. Data after the 72nd dot is output. Enters tristate when EXT1 bit is 0.
M	1	O	Extension driver	Acts as an alternating current signal of extension driver. Enters tristate when both EXT1 and EXT2 bits are 0.
V1 to V5	5	—	Power supply	Power supply for LCD drive V_{CC} – V5 = 15 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +2.7 V to +5.5 V, GND: 0 V
OSC1/ OSC2	2	—	Oscillation resistor/ clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC1.
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Vci is reference voltage and power supply for the booster. Vci: 2.0 V to 5.0 V ≤ V_{CC}.
V5OUT2	1	O	V5 pin/ booster capacitor	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, a capacitor with the same capacitance as that of C1–C2 should be connected here.
V5OUT3	1	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitor	External capacitor should be connected here when using the booster.

Function Description

System Interface

The HD66730 has two system interfaces: a synchronized serial one and an 8-bit bus. Both are selected by the IM pin.

The HD66730 has five types of 8-bit registers: an index register (IDR), status register (STR), various control registers, RAM address register (RAR), and RAM data register (RDR).

The index register (IDR) selects control registers, the RAM address register (RAR) or the RAM data register (RDR) for performing data transfer.

The status register (STR) indicates the internal state of the system. Various control registers store display control data here.

The RAM address register (RAR) stores the address data of display data RAM (DD RAM), character generator RAM (CG RAM), and segment RAM (SEG RAM).

The RAM data register (RDR) temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the RDR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by internal operations. The RDR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. Here, when address information is written into the RAR, data is read and then stored into the RDR from DD RAM, CG RAM, or SEG RAM by internal operations.

Data transfer between the MPU is then completed when the MPU reads the RDR. After this read, data in DD RAM, CG RAM, or SEG RAM stored at the next address is sent to the RDR at the next data read from the MPU.

These registers can be selected by the register select signal (RS) and the read/write signal (R/W) in the 8-bit bus interface, and by the RS bit and R/W bit of start-byte data in the synchronized serial interface.

Busy Flag

When the busy flag is 1, the HD66730 is in internal operation mode, and only the status register (STR) can be accessed. The busy flag (BF) is output from bit 7 (DB7). Access of other registers can be performed only after confirming that the busy flag is 0.

RAM Address Counter (RAR)

The RAM address counter (RAR) provides addresses for accessing DD RAM, CG RAM, or SEG RAM. When an initial address value is written into the RAM counter (RAR), the RAR is automatically incremented or decremented by 1. Note that a control register specifies which RAM (DD RAM, CG RAM, SEG RAM) to select.

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IDR write
0	1	STR read
1	0	Control register write, RAM address register (RAR) write, and RAM data register (RDR) write
1	1	RAM data register (RDR) read

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores character codes and display attribute codes for displaying data.

A full-size font is displayed using two bytes, and a half-size font is displayed using one byte. Since the RAM capacity is 80 bytes, 40 full-size characters or 80 half-size characters can be stored.

DD RAM displays only that data stored within the range corresponding to the number of display columns. Data stored outside the range is ignored. Refer to Combined Display of Full-Size and Half-Size characters for details on character codes stored in DD RAM. The relationship between DD RAM addresses and LCD display position depends on the number of display lines (1 line/2 lines/4 lines).

Execution of the display-clear instruction writes H'A0 corresponding to the half-size character for “space” throughout DD RAM.

Note: The HD66730 performs display by reading character codes from the DD RAM according to the number of display columns set by the control register. In particular, reading from the DD RAM begins at the position corresponding to the rightmost character as set by the maximum number of display columns. This means that one byte of a two-byte full-size character code should not be set in a position exceeding the maximum number of display columns. For example, do not write a full-size code (2 bytes) in the 12th and 13th byte when the display is set for six characters.

- 1-line display (NL1/0 = 00)

  80 bytes of consecutive addresses from H'00 to H'4F are allocated for DD RAM addresses. When there are fewer than 40 display characters (at full size), only the number of display characters specified by NC1/0 are displayed starting from H'00 in the DD RAM. For example, 12 bytes of addresses from H'00 to H'0B are used when a 6-character display (NC1/0 = 00) is performed using one HD66730; addresses from H'0C on are ignored. In this case, do not write a full-size code into bytes H'0B and H'0C because a half-size character may be displayed. See figure 1 for a 1-line display.

- 2-line display (NL1/0 = 01)

  The first line in the DD RAM address is displayed for the 40 bytes of addresses from H'00 to H'27, and the second line is displayed for the 40 bytes of addresses from H'40 to H'67. When there are fewer than 20 display characters (at full size), only the number of display characters specified by NC1/0 will be displayed starting from the leftmost address of the DD RAM. For example, 24 bytes of addresses from H'00 to H'0B and H'40 to H'4B are used when a 6-character display (NC1/0 = 00) is performed using one HD66730. Addresses from H'0C and H'4C on are ignored. See figure 2 for a 2-line display.

- 4-line display (NL1/0 = 11)

  The first line in the DD RAM address is displayed from H'00 to H'13, the second line from H'20 to H'33, the third line from H'40 to H'53, and the fourth line from H'60 to H'73. For a 6-character display (NC1/0 = 00) (at full-size), only 12 bytes from the leftmost address of DD RAM are displayed. See figure 3 for a 4-line display.

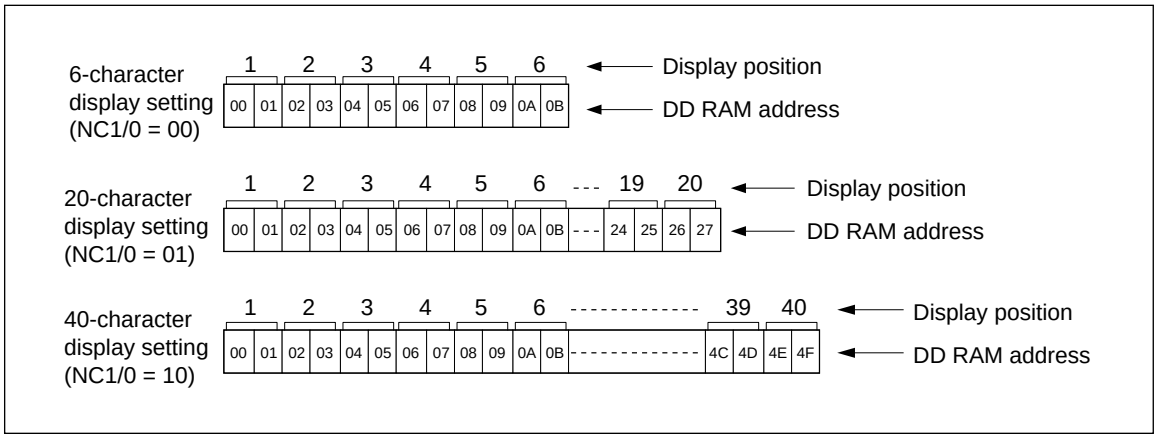


Figure 1 1-Line Display (NL1/0 = 00)

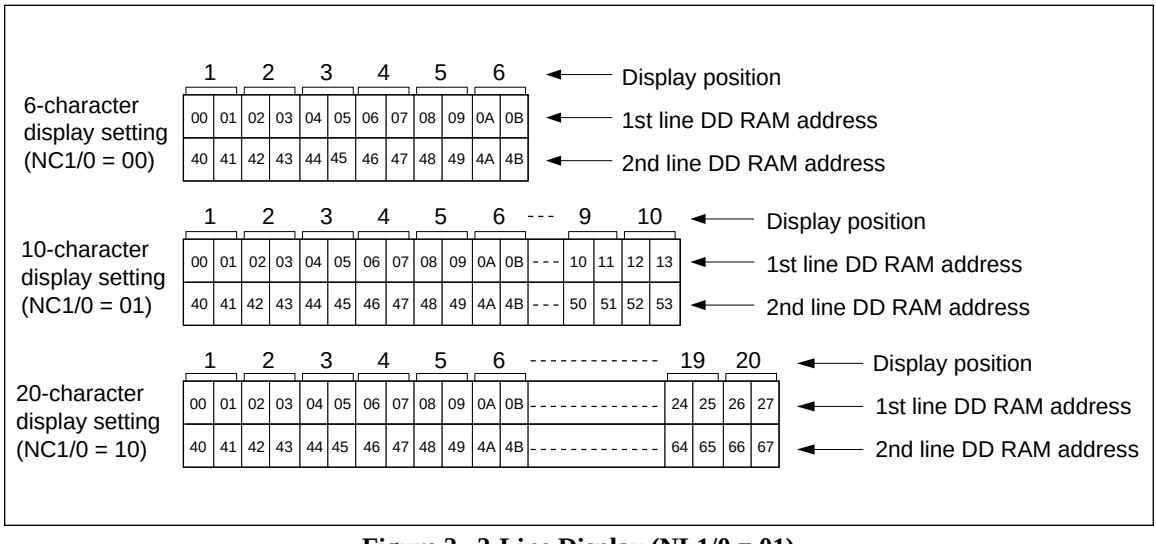


Figure 2 2-Line Display (NL1/0 = 01)

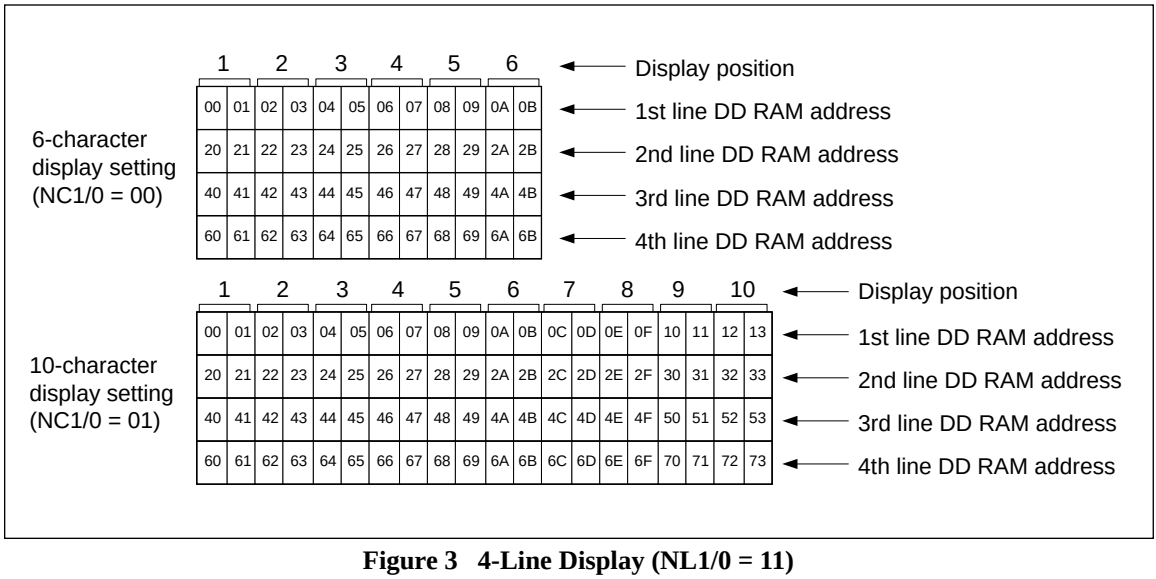


Figure 3 4-Line Display (NL1/0 = 11)

Character Generator ROM for a Full-Size Font (FCG ROM)

The character generator ROM for a full-size font (FCG ROM) generates 3,840 11 × 12 dot full-size character patterns from a 12-bit character code. This includes 2,965 kanji according to the JIS Level-1 Kanji Set and 524 JIS non-kanji. Table 3 shows the relationship between character codes set in DD RAM and full-size font patterns. Refer to Combined Display of Full-Size and Half-Size Characters for the relationship between JIS codes and the character codes to be set in the DD RAM.

Character Generator ROM for a Half-Size Font (HCG ROM)

The character generator ROM for a half-size font (HCG ROM) generates 128 5 × 12 dot character patterns from 7-bit character codes. A half-size font (alphanumeric characters and symbols) can be displayed together with a full-size font. Refer to Combined Display of Full-Size and Half-Size Characters for details.

Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) allows the user to display arbitrary full-size font patterns. It can display 8 12 × 13 dot fonts.

This RAM can also display double-size characters and figures by combining multiple CG RAM fonts. Specify character codes from H'000 to H'007 in a full size of character code when displaying font patterns stored in the CG RAM.

Segment RAM (SEG RAM)

The segment RAM (SEG RAM) is used to control icons and marks in segment units by the user program. Bits in SEG RAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DD RAM and CG RAM. The SEG RAM is read and displayed when the COMS output pin is selected.

Up to 71 icons can be displayed using a single HD66730. Up to 96 icons can be displayed by expanding the drivers on the segment side. SEG RAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DD RAM, FCG ROM, HCG ROM, CG RAM, and SEG RAM. RAM read timing for display and internal operation timing for MPU access are generated separately to avoid interference. This prevents undesirable interferences, such as flickering, in areas other than the display area when writing data to DD RAM, for example.

The timing generator generates interface control signals CL1, CL2, M, and COMD-output of extension drivers for a extension configuration.

Display Attribute Controller

The display attribute controller displays white/black inverse, blinking, and white/black inverse blinking for a full size font in FCG ROM according to the attribute code set in the DD RAM. Refer to Display Attribute Designation for details.

Fonts in CG RAM and bit patterns in SEG RAM control display attributes using the upper two bits (bits 7 and 6) in each display-pattern data.

Cursor Control Circuit

The cursor control circuit is used to produce a cursor on a displayed character corresponding to the DD RAM address set in the RAM address counter (RAR). Cursors can be chosen from three types: 12th raster-row cursor that is displayed only on the 12th raster-row of each font; blink cursor that periodically displays the whole font in black and white and black inverted cursor that periodically displays the font in white and black (see

figure 9). Note that when the RAM address counter (RAR) is selecting CG RAM or SEG RAM, a cursor would be generated at that address, however, it does not have any meaning.

Note: One display line consists of 13 raster-rows.

Smooth Scroll Control Circuit

The smooth scroll control circuit is used to perform a smooth-scroll in units of dots.

When the number of characters to be displayed is greater than that possible at one time in the liquid crystal module, this horizontal smooth scroll can be used to display characters in an easy-to-read manner for each line. Refer to Horizontal Smooth Scroll for details for each line.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 26 common signal drivers and 71 segment signal drivers. When the liquid crystal driver duty ratio is set by a program, the necessary common signal drivers output drive waveforms and the remaining common drivers output non-selected waveforms. In addition, drivers can be expanded on the common and segment sides through register settings.

Display pattern data is sent serially through a 71-bit shift register and latched when all needed data has arrived. The latched data then enables the LCD driver to generate drive waveform outputs. This serial data is sent from the display pattern that corresponds to the last address of the DD RAM and is latched when the character pattern of the display data corresponding to the first address enters the internal shift register.

Booster

The booster outputs a voltage that is two or three times higher than the reference voltage input from pin Vci. Since the LCD voltage can be generated from the LSI operation power supply, this circuit can operate with a single power supply. Refer to Power Supply for Liquid Crystal Display Drive for details.

Oscillator

The HD66730 performs R-C oscillation by adding a single external oscillation resistor. The oscillation frequency corresponding to display size and frame frequency can be adjusted by changing the oscillation resistor. Refer to Oscillator for details.

Table 3 Relationship between Full-Size Character Code and Kanji

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 2		亜	唖	娃	阿	哀	愛	挨	姶	逢	葵	茜	穐	悪	握	渥
0 3	旭	葦	芦	鯵	梓	圧	斡	扱	宛	姐	虻	飴	絢	綾	鮎	或
0 4	粟	袷	安	庵	按	暗	案	闇	鞍	杏	以	伊	位	依	偉	囲
0 5	夷	委	威	尉	惟	意	慰	易	椅	為	畏	異	移	維	緯	胃
0 6	萎	衣	謂	違	遺	医	井	亥	域	育	郁	磯	一	壱	溢	逸
0 7	稲	茨	芋	鰯	允	印	咽	員	因	姻	引	飲	淫	胤	蔭	
0 A		院	陰	隠	韻	吋	右	宇	烏	羽	迂	雨	卯	鵜	窺	丑
0 B	碓	臼	渦	嘘	唄	鬱	蔚	鰻	姥	厩	浦	瓜	閏	噂	云	運
0 C	雲	荏	餌	叡	営	嬰	影	映	曳	栄	永	泳	洩	瑛	盈	穎
0 D	頴	英	衛	詠	鋭	液	疫	益	駅	悦	謁	越	閲	榎	厭	円
0 E	園	堰	奄	宴	延	怨	掩	援	沿	演	炎	焔	煙	燕	猿	縁
0 F	艶	苑	薗	遠	鉛	鴛	塩	於	汚	甥	凹	央	奥	往	応	
1 2		押	旺	横	欧	殴	王	翁	襖	鴬	鴎	黄	岡	沖	荻	億
1 3	屋	憶	臆	桶	牡	乙	俺	卸	恩	温	穏	音	下	化	仮	何
1 4	伽	価	佳	加	可	嘉	夏	嫁	家	寡	科	暇	果	架	歌	河
1 5	火	珂	禍	禾	稼	箇	花	苛	茄	荷	華	菓	蝦	課	嘩	貨
1 6	迦	過	霞	蚊	俄	峨	我	牙	画	臥	芽	蛾	賀	雅	餓	駕
1 7	介	会	解	回	塊	壊	廻	快	怪	悔	恢	懐	戒	拐	改	
1 A		魁	晦	械	海	灰	界	皆	絵	芥	蟹	開	階	貝	凱	劾
1 B	外	咳	害	崖	慨	概	涯	碍	蓋	街	該	鎧	骸	浬	馨	蛙
1 C	垣	柿	蛎	鈎	劃	嚇	各	廓	拡	撹	格	核	殻	獲	確	穫
1 D	覚	角	赫	較	郭	閣	隔	革	学	岳	楽	額	顎	掛	笠	樫
1 E	橿	梶	鰍	潟	割	喝	恰	括	活	渇	滑	葛	褐	轄	且	鰹
1 F	叶	椛	樺	鞄	株	兜	竃	蒲	釜	鎌	噛	鴨	栢	茅	萱	
2 2		粥	刈	苅	瓦	乾	侃	冠	寒	刊	勘	勧	巻	喚	堪	姦
2 3	完	官	寛	干	幹	患	感	慣	憾	換	敢	柑	桓	棺	款	歓
2 4	汗	漢	澗	潅	環	甘	監	看	竿	管	簡	緩	缶	翰	肝	艦
2 5	莞	観	諌	貫	還	鑑	間	閑	関	陥	韓	館	舘	丸	含	岸
2 6	厳	玩	癌	眼	岩	翫	贋	雁	頑	顔	願	企	伎	危	喜	器
2 7	基	奇	嬉	寄	岐	希	幾	忌	揮	机	旗	既	期	棋	棄	
2 A		機	帰	毅	気	汽	畿	祈	季	稀	紀	徽	規	記	貴	起
2 B	軌	輝	飢	騎	鬼	亀	偽	儀	妓	宜	戯	技	擬	欺	犠	疑
2 C	祇	義	蟻	誼	議	掬	菊	鞠	吉	吃	喫	桔	橘	詰	砧	杵
2 D	黍	却	客	脚	虐	逆	丘	久	仇	休	及	吸	宮	弓	急	救
2 E	朽	求	汲	泣	灸	球	究	窮	笈	級	糾	給	旧	牛	去	居
2 F	巨	拒	拠	挙	渠	虚	許	距	鋸	漁	禦	魚	亨	享	京	
3 2		供	侠	僑	兇	競	共	凶	協	匡	卿	叫	喬	境	峡	強
3 3	彊	怯	恐	恭	挟	教	橋	況	狂	狭	矯	胸	脅	興	蕎	郷
3 4	鏡	響	饗	驚	仰	凝	尭	暁	業	局	曲	極	玉	桐	粁	僅
3 5	勤	均	巾	錦	斤	欣	欽	琴	禁	禽	筋	緊	芹	菌	衿	襟
3 6	謹	近	金	吟	銀	九	倶	句	区	狗	玖	矩	苦	躯	駆	駈
3 7	駒	具	愚	虞	喰	空	偶	寓	遇	隅	串	櫛	釧	屑	屈	
3 A		掘	窟	沓	靴	轡	窪	熊	隈	粂	栗	繰	桑	鍬	勲	君
3 B	薫	訓	群	軍	郡	卦	袈	祁	係	傾	刑	兄	啓	圭	珪	型
3 C	契	形	径	恵	慶	慧	憩	掲	携	敬	景	桂	渓	畦	稽	系
3 D	経	継	繋	罫	茎	荊	蛍	計	詣	警	軽	頚	鶏	芸	迎	鯨
3 E	劇	戟	撃	激	隙	桁	傑	欠	決	潔	穴	結	血	訣	月	件
3 F	倹	倦	健	兼	券	剣	喧	圏	堅	嫌	建	憲	懸	拳	捲	

Table 3 Relationship between Full-Size Character Code and Kanji (cont)

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4 2		検	権	牽	犬	献	研	硯	絹	県	肩	見	謙	賢	軒	遣
4 3	鍵	険	顕	験	鹸	元	原	厳	幻	弦	減	源	玄	現	絃	舷
4 4	言	諺	限	乎	個	古	呼	固	姑	孤	己	庫	弧	戸	故	枯
4 5	湖	狐	糊	袴	股	胡	菰	虎	誇	跨	鈷	雇	顧	鼓	五	互
4 6	伍	午	呉	吾	娯	後	御	悟	梧	檎	瑚	碁	語	誤	護	醐
4 7	乞	鯉	交	佼	侯	候	倖	光	公	功	効	勾	厚	口	向	
4 A		后	喉	坑	垢	好	孔	孝	宏	工	巧	巷	幸	広	庚	康
4 B	弘	恒	慌	抗	拘	控	攻	昂	晃	更	杭	校	梗	構	江	洪
4 C	浩	港	溝	甲	皇	硬	稿	糠	紅	紘	絞	綱	耕	考	肯	肱
4 D	腔	膏	航	荒	行	衡	講	貢	購	郊	酵	鉱	砿	鋼	閤	降
4 E	項	香	高	鴻	剛	劫	号	合	壕	拷	濠	豪	轟	麹	克	刻
4 F	告	国	穀	酷	鵠	黒	獄	漉	腰	甑	忽	惚	骨	狛	込	
5 2		此	頃	今	困	坤	墾	婚	恨	懇	昏	昆	根	梱	混	痕
5 3	紺	艮	魂	些	佐	叉	唆	嵯	左	差	査	沙	瑳	砂	詐	鎖
5 4	裟	坐	座	挫	債	催	再	最	哉	塞	妻	宰	彩	才	採	栽
5 5	歳	済	災	采	犀	砕	砦	祭	斎	細	菜	裁	載	際	剤	在
5 6	材	罪	財	冴	坂	阪	堺	榊	肴	咲	崎	埼	碕	鷺	作	削
5 7	詐	搾	昨	朔	柵	窄	策	索	錯	桜	鮭	笹	匙	冊	刷	
5 A		察	拶	撮	擦	札	殺	薩	雑	皐	鯖	捌	錆	鮫	皿	晒
5 B	三	傘	参	山	惨	撒	散	桟	燦	珊	産	算	纂	蚕	讃	賛
5 C	酸	餐	斬	暫	残	仕	仔	伺	使	刺	司	史	嗣	四	士	始
5 D	姉	姿	子	屍	市	師	志	思	指	支	孜	斯	施	旨	枝	止
5 E	死	氏	獅	祉	私	糸	紙	紫	肢	脂	至	視	詞	詩	試	誌
5 F	諮	資	賜	雌	飼	歯	事	似	侍	児	字	寺	慈	持	時	
6 2		次	滋	治	爾	璽	痔	磁	示	而	耳	自	蒔	辞	汐	鹿
6 3	式	識	鴫	竺	軸	宍	雫	七	叱	執	失	嫉	室	悉	湿	漆
6 4	疾	質	実	蔀	篠	偲	柴	芝	屡	蕊	縞	舎	写	射	捨	赦
6 5	斜	煮	社	紗	者	謝	車	遮	蛇	邪	借	勺	尺	杓	灼	爵
6 6	酌	釈	錫	若	寂	弱	惹	主	取	守	手	朱	殊	狩	珠	種
6 7	腫	趣	酒	首	儒	受	呪	寿	授	樹	綬	需	囚	収	周	
6 A		宗	就	州	修	愁	拾	洲	秀	秋	終	繍	習	臭	舟	蒐
6 B	衆	襲	讐	蹴	輯	週	酋	酬	集	醜	什	住	充	十	従	戎
6 C	柔	汁	渋	獣	縦	重	銃	叔	夙	宿	淑	祝	縮	粛	塾	熟
6 D	出	術	述	俊	峻	春	瞬	竣	舜	駿	准	循	旬	楯	殉	淳
6 E	準	潤	盾	純	巡	遵	醇	順	処	初	所	暑	曙	渚	庶	緒
6 F	署	書	薯	藷	諸	助	叙	女	序	徐	恕	鋤	除	傷	償	
7 2		勝	匠	升	召	哨	商	唱	嘗	奨	妾	娼	宵	将	小	少
7 3	尚	庄	床	廠	彰	承	抄	招	掌	捷	昇	昌	昭	晶	松	梢
7 4	樟	樵	沼	消	渉	湘	焼	焦	照	症	省	硝	礁	祥	称	章
7 5	笑	粧	紹	肖	菖	蒋	蕉	衝	裳	訟	証	詔	詳	象	賞	醤
7 6	鉦	鍾	鐘	障	鞘	上	丈	丞	乗	冗	剰	城	場	壌	嬢	常
7 7	情	擾	条	杖	浄	状	畳	穣	蒸	譲	醸	錠	嘱	埴	飾	
7 A		拭	植	殖	燭	織	職	色	触	食	蝕	辱	尻	伸	信	侵
7 B	唇	娠	寝	審	心	慎	振	新	晋	森	榛	浸	深	申	疹	真
7 C	神	秦	紳	臣	芯	薪	親	診	身	辛	進	針	震	人	仁	刃
7 D	塵	壬	尋	甚	尽	腎	訊	迅	陣	靱	笥	諏	須	酢	図	厨
7 E	逗	吹	垂	帥	推	水	炊	睡	粋	翠	衰	遂	酔	錐	錘	随
7 F	瑞	髄	崇	嵩	数	枢	趨	雛	据	杉	椙	菅	頗	雀	裾	

Table 3 Relationship between Full-Size Character Code and Kanji (cont)

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8 2		澄	摺	寸	世	瀬	畝	是	凄	制	勢	姓	征	性	成	政
8 3	整	星	晴	棲	栖	正	清	牲	生	盛	精	聖	声	製	西	誠
8 4	誓	請	逝	醒	青	静	斉	税	脆	隻	席	惜	戚	斥	昔	析
8 5	石	積	籍	績	脊	責	赤	跡	蹟	碩	切	拙	接	摂	折	設
8 6	窃	節	説	雪	絶	舌	蝉	仙	先	千	占	宣	専	尖	川	戦
8 7	扇	撰	栓	梅	泉	浅	洗	染	潜	煎	煽	旋	穿	箭	線	
8 A		繊	羨	腺	舛	船	薦	詮	賤	践	選	遷	銭	銑	閃	鮮
8 B	前	善	漸	然	全	禅	繕	膳	糎	噌	塑	岨	措	曾	曽	楚
8 C	狙	疏	踈	礎	祖	租	粗	素	組	蘇	訴	阻	遡	鼠	僧	創
8 D	双	叢	倉	喪	壮	奏	爽	宋	層	匝	惣	想	捜	掃	挿	掻
8 E	操	早	曹	巣	槍	槽	漕	燥	争	痩	相	窓	糟	総	綜	聡
8 F	草	荘	葬	蒼	藻	装	走	送	遭	鎗	霜	騒	像	増	憎	
9 2		臓	蔵	贈	造	促	側	則	即	息	捉	束	測	足	速	俗
9 3	属	賊	族	続	卒	袖	其	揃	存	孫	尊	損	村	遜	他	多
9 4	太	汰	詑	唾	堕	妥	惰	打	柁	舵	楕	陀	駄	騨	体	堆
9 5	対	耐	岱	帯	待	怠	態	戴	替	泰	滞	胎	腿	苔	袋	貸
9 6	退	逮	隊	黛	鯛	代	台	大	第	醍	題	鷹	滝	瀧	卓	啄
9 7	宅	托	択	拓	沢	濯	琢	託	鐸	濁	諾	茸	凧	蛸	只	
9 A		叩	但	達	辰	奪	脱	巽	竪	辿	棚	谷	狸	鱈	樽	誰
9 B	丹	単	嘆	坦	担	探	旦	歎	淡	湛	炭	短	端	箪	綻	耽
9 C	胆	蛋	誕	鍛	団	壇	弾	断	暖	檀	段	男	談	値	知	地
9 D	弛	恥	智	池	痴	稚	置	致	蜘	遅	馳	築	畜	竹	筑	蓄
9 E	逐	秩	窒	茶	嫡	着	中	仲	宙	忠	抽	昼	柱	注	虫	衷
9 F	註	酎	鋳	駐	樗	瀦	猪	苧	著	貯	丁	兆	凋	喋	寵	
A 2		帖	帳	庁	弔	張	彫	徴	懲	挑	暢	朝	潮	牒	町	眺
A 3	聴	脹	腸	蝶	調	諜	超	跳	銚	長	頂	鳥	勅	捗	直	朕
A 4	沈	珍	賃	鎮	陳	津	墜	椎	槌	追	鎚	痛	通	塚	栂	掴
A 5	槻	佃	漬	柘	辻	蔦	綴	鍔	椿	潰	坪	壺	嬬	紬	爪	吊
A 6	釣	鶴	亭	低	停	偵	剃	貞	呈	堤	定	帝	底	庭	廷	弟
A 7	悌	抵	挺	提	梯	汀	碇	禎	程	締	艇	訂	諦	蹄	逓	
A A		邸	鄭	釘	鼎	泥	摘	擢	敵	滴	的	笛	適	鏑	溺	哲
A B	徹	撤	轍	迭	鉄	典	填	天	展	店	添	纏	甜	貼	転	顛
A C	点	伝	殿	澱	田	電	兎	吐	堵	塗	妬	屠	徒	斗	杜	渡
A D	登	菟	賭	途	都	鍍	砥	砺	努	度	土	奴	怒	倒	党	冬
A E	凍	刀	唐	塔	塘	套	宕	島	嶋	悼	投	搭	東	桃	梼	棟
A F	盗	淘	湯	涛	灯	燈	当	痘	祷	等	答	筒	糖	統	到	
B 2		董	蕩	藤	討	謄	豆	踏	逃	透	鐙	陶	頭	騰	闘	働
B 3	動	同	堂	導	憧	撞	洞	瞳	童	胴	萄	道	銅	峠	鴇	匿
B 4	得	徳	涜	特	督	禿	篤	毒	独	読	栃	橡	凸	突	椴	届
B 5	鳶	苫	寅	酉	瀞	噸	屯	惇	敦	沌	豚	遁	頓	呑	曇	鈍
B 6	奈	那	内	乍	凪	薙	謎	灘	捺	鍋	楢	馴	縄	畷	南	楠
B 7	軟	難	汝	二	尼	弐	迩	匂	賑	肉	虹	廿	日	乳	入	
B A		如	尿	韮	任	妊	忍	認	濡	禰	祢	寧	葱	猫	熱	年
B B	念	捻	撚	燃	粘	乃	廼	之	埜	嚢	悩	濃	納	能	脳	膿
B C	農	覗	蚤	巴	把	播	覇	杷	波	派	琶	破	婆	罵	芭	馬
B D	俳	廃	拝	排	敗	杯	盃	牌	背	肺	輩	配	倍	培	媒	梅
B E	楳	煤	狽	買	売	賠	陪	這	蝿	秤	矧	萩	伯	剥	博	拍
B F	柏	泊	白	箔	粕	舶	薄	迫	曝	漠	爆	縛	莫	駁	麦	

Table 3 Relationship between Full-Size Character Code and Kanji (cont)

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C 2		函	箱	硲	箸	肇	筈	櫨	幡	肌	畑	畠	八	鉢	溌	発
C 3	醗	髪	伐	罰	抜	筏	閥	鳩	噺	塙	蛤	隼	伴	判	半	反
C 4	叛	帆	搬	斑	板	氾	汎	版	犯	班	畔	繁	般	藩	販	範
C 5	釆	煩	頒	飯	挽	晩	番	盤	磐	蕃	蛮	匪	卑	否	妃	庇
C 6	彼	悲	扉	批	披	斐	比	泌	疲	皮	碑	秘	緋	罷	肥	被
C 7	誹	費	避	非	飛	樋	簸	備	尾	微	枇	毘	琵	眉	美	
C A		鼻	柊	稗	匹	疋	髭	彦	膝	菱	肘	弼	必	畢	筆	逼
C B	桧	姫	媛	紐	百	謬	俵	彪	標	氷	漂	瓢	票	表	評	豹
C C	廟	描	病	秒	苗	錨	鋲	蒜	蛭	鰭	品	彬	斌	浜	瀕	貧
C D	賓	頻	敏	瓶	不	付	埠	夫	婦	富	冨	布	府	怖	扶	敷
C E	斧	普	浮	父	符	腐	膚	芙	譜	負	賦	赴	阜	附	侮	撫
C F	武	舞	葡	蕪	部	封	楓	風	葺	蕗	伏	副	復	幅	服	
D 2		福	腹	複	覆	淵	弗	払	沸	仏	物	鮒	分	吻	噴	墳
D 3	憤	扮	焚	奮	粉	糞	紛	雰	文	聞	丙	併	兵	塀	幣	平
D 4	弊	柄	並	蔽	閉	陛	米	頁	僻	壁	癖	碧	別	瞥	蔑	箆
D 5	偏	変	片	篇	編	辺	返	遍	便	勉	娩	弁	鞭	保	舗	鋪
D 6	圃	捕	歩	甫	補	輔	穂	募	墓	慕	戊	暮	母	簿	菩	倣
D 7	俸	包	呆	報	奉	宝	峰	峯	崩	庖	抱	捧	放	方	朋	
D A		法	泡	烹	砲	縫	胞	芳	萌	蓬	蜂	褒	訪	豊	邦	鋒
D B	飽	鳳	鵬	乏	亡	傍	剖	坊	妨	帽	忘	忙	房	暴	望	某
D C	棒	冒	紡	肪	膨	謀	貌	貿	鉾	防	吠	頬	北	僕	卜	墨
D D	撲	朴	牧	睦	穆	釦	勃	没	殆	堀	幌	奔	本	翻	凡	盆
D E	摩	磨	魔	麻	埋	妹	昧	枚	毎	哩	槙	幕	膜	枕	鮪	柾
D F	鱒	桝	亦	俣	又	抹	末	沫	迄	侭	繭	麿	万	慢	満	
E 2		漫	蔓	味	未	魅	巳	箕	岬	密	蜜	湊	蓑	稔	脈	妙
E 3	粍	民	眠	務	夢	無	牟	矛	霧	鵡	椋	婿	娘	冥	名	命
E 4	明	盟	迷	銘	鳴	姪	牝	滅	免	棉	綿	緬	面	麺	摸	模
E 5	茂	妄	孟	毛	猛	盲	網	耗	蒙	儲	木	黙	目	杢	勿	餅
E 6	尤	戻	籾	貰	問	悶	紋	門	匁	也	冶	夜	爺	耶	野	弥
E 7	矢	厄	役	約	薬	訳	躍	靖	柳	薮	鑓	愉	愈	油	癒	
E A		諭	輸	唯	佑	優	勇	友	宥	幽	悠	憂	揖	有	柚	湧
E B	涌	猶	猷	由	祐	裕	誘	遊	邑	郵	雄	融	夕	予	余	与
E C	誉	輿	預	傭	幼	妖	容	庸	揚	揺	擁	曜	楊	様	洋	溶
E D	熔	用	窯	羊	耀	葉	蓉	要	謡	踊	遥	陽	養	慾	抑	欲
E E	沃	浴	翌	翼	淀	羅	螺	裸	来	莱	頼	雷	洛	絡	落	酪
E F	乱	卵	嵐	欄	濫	藍	蘭	覧	利	吏	履	李	梨	理	璃	
F 2		痢	裏	裡	里	離	陸	律	率	立	葎	掠	略	劉	流	溜
F 3	琉	留	硫	粒	隆	竜	龍	侶	慮	旅	虜	了	亮	僚	両	凌
F 4	寮	料	梁	涼	猟	療	瞭	稜	糧	良	諒	遼	量	陵	領	力
F 5	緑	倫	厘	林	淋	燐	琳	臨	輪	隣	鱗	麟	瑠	塁	涙	累
F 6	類	令	伶	例	冷	励	嶺	怜	玲	礼	苓	鈴	隷	零	霊	麗
F 7	齢	暦	歴	列	劣	烈	裂	廉	恋	憐	漣	煉	簾	練	聯	
F A		蓮	連	錬	呂	魯	櫓	炉	賂	路	露	労	婁	廊	弄	朗
F B	楼	榔	浪	漏	牢	狼	篭	老	聾	蝋	郎	六	麓	禄	肋	録
F C	論	倭	和	話	歪	賄	脇	惑	枠	鷲	亙	亘	鰐	詫	藁	蕨
F D	椀	湾	碗	腕												
F E																
F F																

Table 4 Relationship between Full-Size Character Code and Non-Kanji

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4 8			、	。	,	.	・	:	;	?	!	゛	゜	´	`	¨
4 9	^	―	_	ヽ	ヾ	ゝ	ゞ	〃	仝	々	〆	〇	―	―	-	／
8 8	＼	～	∥	｜	…	‥	‘	’	“	”	(	)	〔	〕	[	]
8 9	｜	｜	〈	〉	《	》	「	」	『	』	【	】	＋	－	±	×
C 8	÷	＝	≠	＜	＞	≦	≧	∞	∴	♂	♀	°	′	″	℃	¥
C 9	$	¢	£	%	#	&	*	@	§	☆	★	○	●	◎	◇	
5 0		◆	□	■	△	▲	▽	▼	※	〒	→	←	↑	↓	＝	
5 1											∈	∋	⊆	⊇	⊂	⊃
9 0	∪	∩									∧	∨	¬	⇒	⇔	∀
9 1	∃												∠	⊥	⌒	∂
D 0	∇	≡	≒	≪	≫	√	∽	∝	∵	∫	∬					
D 1			Å	‰	♯	♭	♪	†	‡	¶					◯	
5 8																
5 9	0	1	2	3	4	5	6	7	8	9						
9 8		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
9 9	P	Q	R	S	T	U	V	W	X	Y	Z					
D 8		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
D 9	p	q	r	s	t	u	v	w	x	y	z					
6 0		ぁ	あ	ぃ	い	ぅ	う	ぇ	え	ぉ	お	か	が	き	ぎ	く
6 1	ぐ	け	げ	こ	ご	さ	ざ	し	じ	す	ず	せ	ぜ	そ	ぞ	た
A 0	だ	ち	ぢ	っ	つ	づ	て	で	と	ど	な	に	ぬ	ね	の	は
A 1	ば	ぱ	ひ	び	ぴ	ふ	ぶ	ぷ	へ	べ	ぺ	ほ	ぼ	ぽ	ま	み
E 0	む	め	も	ゃ	や	ゅ	ゆ	ょ	よ	ら	り	る	れ	ろ	ゎ	わ
E 1	ゐ	ゑ	を	ん												
6 8		ァ	ア	ィ	イ	ゥ	ウ	ェ	エ	ォ	オ	カ	ガ	キ	ギ	ク
6 9	グ	ケ	ゲ	コ	ゴ	サ	ザ	シ	ジ	ス	ズ	セ	ゼ	ソ	ゾ	タ
A 8	ダ	チ	ヂ	ッ	ツ	ヅ	テ	デ	ト	ド	ナ	ニ	ヌ	ネ	ノ	ハ
A 9	バ	パ	ヒ	ビ	ピ	フ	ブ	プ	ヘ	ベ	ペ	ホ	ボ	ポ	マ	ミ
E 8	ム	メ	モ	ャ	ヤ	ュ	ユ	ョ	ヨ	ラ	リ	ル	レ	ロ	ヮ	ワ
E 9	ヰ	ヱ	ヲ	ン	ヴ	ヵ	ヶ									
7 0		A	B	Γ	Δ	E	Z	H	Θ	I	K	Λ	M	N	Ξ	O
7 1	Π	P	Σ	T	ϒ	Φ	X	Ψ	Ω							
B 0		α	β	γ	δ	ε	ζ	η	θ	ι	κ	λ	μ	ν	ξ	ο
B 1	π	ρ	σ	τ	υ	φ	χ	ψ	ω							
F 0																
F 1																
7 8		А	Б	В	Г	Д	Е	Ё	Ж	З	И	Й	К	Л	М	Н
7 9	О	П	Р	С	Т	У	Ф	Х	Ц	Ч	Ш	Щ	Ъ	Ы	Ь	Э
B 8	Ю	Я														
B 9		а	б	в	г	д	е	ё	ж	з	и	й	к	л	м	н
F 8	о	п	р	с	т	у	ф	х	ц	ч	ш	щ	ъ	ы	ь	э
F 9	ю	я														
4 0		─	│	┌	┐	┘	└	├	┬	┤	┴	┼	━	┃	┏	┓
4 1	┛	┗	┣	┳	┫	┻	╋	┠	┯	┨	┷	┿	┝	┰	┥	┸
8 0	╂															
8 1																
C 0																
C 1																

Table 5 Relationship between Half-Size Character Code and Character Pattern (ROM Code: A00)

Lower (3 bits) \ Upper (4 bits)	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 000					(Space)											
xxxx 001																
xxxx 010																
xxxx 011																
xxxx 100																
xxxx 101																
xxxx 110																
xxxx 111																

Relationship between Character Codes (DD RAM), CG RAM Addresses, and Display Characters

Full size character codes H'000 to H'007 can be used to access 8 character patterns in the CG RAM. Since each character pattern can be displayed up to 12 × 13 dots, CG RAM patterns can be displayed immediately next to each other (to the right, left, top, or bottom) without any character spaces between them. Table 6 shows the correspondence between CG RAM addresses and full-size character codes for access of the CG RAM by the MPU.

Table 6 Relationship between Character Codes (DD RAM), CG RAM Addresses, and Display Characters

Character Code				CGRAM Address							CGRAM Data														
											$A_0 = 0$								$A_0 = 1$						
C_{11} ---------- C_3	C_2	C_1	C_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
							0	0	0	1	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							0	0	1	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	0	1	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	1	0	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	1	0	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	1	1	0	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							0	1	1	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	0	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	0	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	1	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	1	1	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							1	1	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
0 0 0 0 0 0 0 0 0 1	0	0	1	0	0	1	0	0	0	0	A	A	0	0	0	0	0	1	A	A	0	0	0	0	0	0
							0	0	0	1	A	A	0	0	0	0	0	0	A	A	1	0	0	0	0	0
							0	0	1	0	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							0	0	1	1	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
							0	1	0	0	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	1	0	1	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	1	1	0	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	1	1	1	A	A	0	0	0	1	0	0	A	A	0	1	0	0	0	0
							1	0	0	0	A	A	0	0	0	1	0	0	A	A	0	1	0	0	0	0
							1	0	0	1	A	A	0	0	0	1	0	0	A	A	0	1	0	0	0	0
							1	0	1	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
							1	0	1	1	A	A	1	1	1	1	1	1	A	A	1	1	1	1	1	0
							1	1	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
0 0 0 0 0 0 0 0 0 0	1	1	1	1	1	1	0	0	0	0	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	0	0	1	A	A	0	1	0	0	0	1	A	A	0	0	0	1	0	0
							0	0	1	0	A	A	0	1	0	0	1	1	A	A	0	0	0	1	0	0
							0	0	1	1	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	0	0	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	0	1	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	1	0	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	1	1	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							1	0	0	0	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							1	0	0	1	A	A	0	1	0	0	0	1	A	A	0	0	0	1	0	0
							1	0	1	0	A	A	0	1	0	0	0	1	A	A	0	0	0	1	0	0
							1	0	1	1	A	A	0	0	1	0	1	1	A	A	1	0	1	0	0	0
							1	1	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0

Character pattern (1)

Character pattern (2)

Character pattern (8)

Notes:
1. CG RAM is selected when the upper 9 bits (C3 to C11) of the full size character codes are 0. In this case, the lower 3 bits (C0 to C2) of the character code correspond to bits 5 to 7 (A5 to A7) (3 bits: 8 types) in the CG RAM address.
2. CG RAM address bits 1 to 4 (A1 to A4) designate the character pattern line position. The 12th line is the cursor position and its display is formed by a logical OR with the cursor.
3. CG RAM address 0 (A0) corresponds to the left-half and right-half of a full-size character pattern.
4. The character data is stored with the rightmost character element in bit 0 (LSB), as shown in the table above. Pattern produced by bits 0 to 5 is displayed and 13 raster-rows are displayed together. Thus, an arbitrary character pattern consisting of 12×13 dots can be displayed.
5. A set bit in the CG RAM data corresponds to display selection, and 0 to non-selection.
6. The upper two bits (AA) of CG RAM data indicate the display attribute for the lower 6-bit pattern. In this case, display attributes specified for the DD RAM during full-size character display is disabled. When these upper two bits are 00, the CG RAM pattern is simply displayed as set; when 01, the pattern reverses (black/white), when 10, the pattern blinks; and when 11, the pattern reverses and blinks.

Relationship between SEG RAM Addresses and Display Patterns

SEG RAM data is displayed when the select level of the COMS pin is output. Since SEG RAM data does not depend on character code data in DD RAM, and does not undergo horizontal smooth scroll, it can be used to display icon and marks. The following shows the relationship between SEG RAM addresses and segment output pins.

Table 7 Relationship between SEG RAM Addresses and Display Patterns

SEGRAM Address				SEGRAM Data							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B1	B0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6
0	0	0	1	B1	B0	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12
0	0	1	0	B1	B0	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18
0	0	1	1	B1	B0	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
0	1	0	0	B1	B0	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30
0	1	0	1	B1	B0	SEG31	SEG32	SEG33	SEG34	SEG35	SEG36
0	1	1	0	B1	B0	SEG37	SEG38	SEG39	SEG40	SEG41	SEG42
0	1	1	1	B1	B0	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
1	0	0	0	B1	B0	SEG49	SEG50	SEG51	SEG52	SEG53	SEG54
1	0	0	1	B1	B0	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60
1	0	1	0	B1	B0	SEG61	SEG62	SEG63	SEG64	SEG65	SEG66
1	0	1	1	B1	B0	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
1	1	0	0	B1	B0	SEG73	SEG74	SEG75	SEG76	SEG77	SEG78
1	1	0	1	B1	B0	SEG79	SEG80	SEG81	SEG82	SEG83	SEG84
1	1	1	0	B1	B0	SEG85	SEG86	SEG87	SEG88	SEG89	SEG90
1	1	1	1	B1	B0	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96

Blinking control — Pattern on/off

Notes:
1. SEG1 to SEG71 are pin numbers of the segment output driver of the HD66730. Pin SEG1 is positioned on the left edge of the display. Segments from SEG72 on are displayed by extension drivers. After SEG 96, display is performed from SEG1 again.
2. The lower six bits (D0 to D5) indicate display on/off for of each segment. A bit setting of 1 selects display while 0 selects no display.
3. Pattern blinking of the lower six bits is controlled by the upper two bits (D6 and D7) of SEG RAM data. When the upper two bits (B0 and B1) are 10, segments whose corresponding bits in the lower 6 bits are set to 1 will blink on the display. When the upper two bits (B0 and B1) are 01, only the bit-5 pattern can blink. Do not attempt to set the upper two bits (B0 and B1) to 11 (setting is prohibited).

Register Functions

Outline

Data can be written from the MPU to the internal control registers and internal RAM of the HD66730 via an 8-bit bus interface or a serial interface. There are five types of internal control registers, as follows (details are described later):

- Index register: Selects and designates which control register the MPU is to access
- Status register: Indicates the internal state
- Control registers: Designates display control
- RAM address register: Sets an address for accessing the various RAMs
- RAM data register: Receives and transmits data to and from the various RAMs

Table 17 shows the instruction list and the number of execution cycles of each instruction after performing register setting. Instructions that perform data transfer with the RAM data register tend to be used the most. However, auto-incrementation by 1 (or auto decrementation by 1) of internal HD66730 RAM addresses after each data write can lighten the program load on the MPU. Note that when an instruction is being executed (internal operations are being performed), only the busy flag in the status register can be read.

Since the busy flag is 1 during execution, the MPU should check this value before accessing a register. When accessing a register without checking the busy flag, an interval longer than the instruction execution time is needed before the next access. Refer to table 17 Instruction Registers, for instruction execution times.

When rewriting DD RAM, character display will momentarily breakdown if the data (character codes) that is being rewritten is also being read by the system for display. For this reason, check the display read line position (NF) and the display read raster-row position (LF) in the status register (SR), and rewrite a DD RAM line that is not being read and displayed.

Functional Description

Index Register (IR)

The index register (figure 4) designates control registers (R0 to R7), RAM address register (RAR: R8), and RAM data register (RDR: R9). The register number must be set between addresses 0000 to 1001 in binary digits. Note that if address 1111 is set, the test register will be selected. Addresses 1010 to 1110 are ignored.

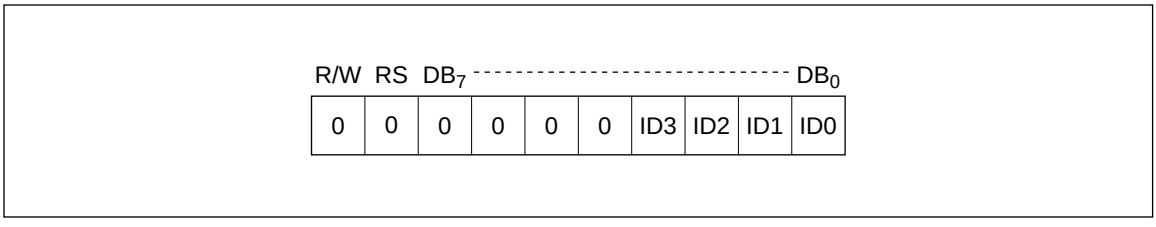


Figure 4 Index Register

Status Register (ST)

The status register (figure 5) includes the busy flag (BF), display line bits (NF1/0), and display raster-row bits (LF0 to LF3). If BF is 1, an instruction is being executed, and another instruction will not be accepted during this time. Any attempt to write data to a register at this time is ignored.

Rasters-rows are driven one at a time according to specific timing to perform liquid crystal display. Bits NF1 and NF0 indicate display lines, and bits LF3 to LF0 indicate the raster-row in a line. If character display degenerates when rewriting DD RAM, rewrite only those display lines that are not currently being read out by the system for display. During segment display, the next state of the last raster-row in the character display is read out.

Table 8 Display State According to NF1 and NF0

NF1	NF0	Display State
00	0	Displaying the first line
0	1	Displaying the second line
1	0	Displaying the third line
1	1	Displaying the fourth line

Table 9 Display State According to LF3 to LF0

LF3	LF2	LF1	LF0	Display State
0	0	0	0	Displaying the first raster-row
0	0	0	1	Displaying the second raster-row
0	0	1	0	Displaying the third raster-row
0	0	1	1	Displaying the fourth raster-row
•				•
•				•
•				•
1	1	0	0	Displaying the 13th raster-row

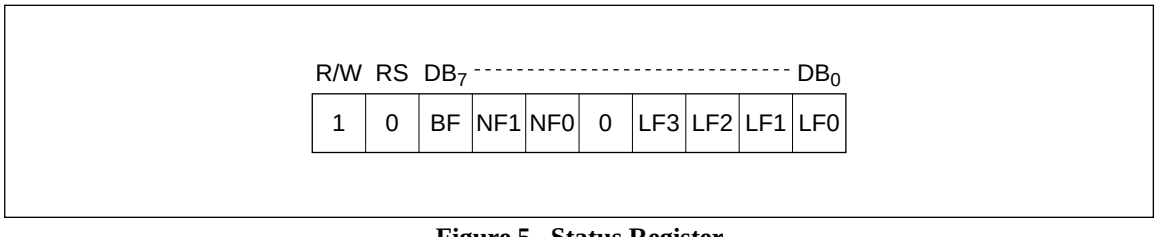


Figure 5 Status Register

Entry Mode Register (R0)

The entry mode register (figure 6) includes bits I/D, RM1, and RM0.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read out from the DD RAM. When the DD RAM address is incremented by 1, the cursor or blinking will also shift to the right. This applies to both CG RAM and SEG RAM.

RM1/0: Selects DD RAM, CG RAM, or SEG RAM for access (table 10).

Table 10 RAM Selection by RM1 and RM0

RM1	RM0	Selected RAM
0	0/1	Display data RAM (DD RAM)
1	0	Character generator RAM (CG RAM)
1	1	Segment RAM (SEG RAM)

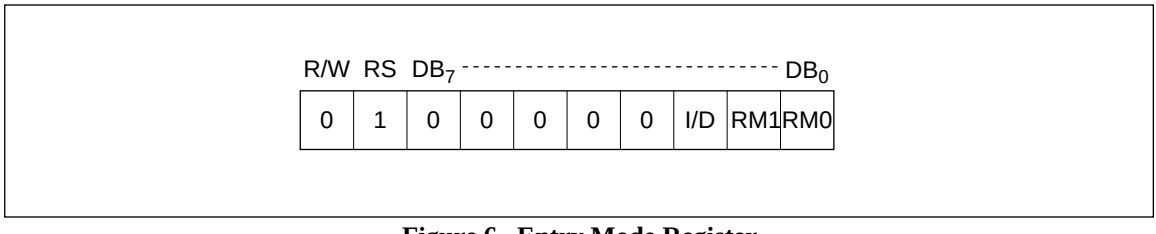


Figure 6 Entry Mode Register

Function Set Register (R1)

The function set register (figure 7) includes bits BST, EXT2, EXT1, DT1, DT0, and DCL.

BST: When BST is 1, the booster starts to operate. When the LCD voltage is external, set BST to 0 to stop operation of the internal booster. In addition, the consumption current can be suppressed by stopping the booster when entering standby mode without display.

EXT2/1: Extends the common driver and segment driver. Set EXT2 to 1 to extend the driver to the common side if the duty ratio is 1/40 or 1/53. Extend the driver to the segment side by setting EXT1 to 1 when displaying 7 or more digits (of full size) in the horizontal direction. DD RAM capacity is 80 bytes.

DT1/0: Selects the duty ratio of the LCD (table 11). Although this bit can be set separately from the display line designation (NL1/0), the duty ratio must be selected so that it will be smaller than the number of display lines.

DCL: When DCL is 1, the display is cleared by writing the code for half-size space (H'A0) into all DD RAM addresses. Then H'00 is written into the RAM address counter (RAR) and the DD RAM is selected. The character code for character code H'A0 must be a blank pattern when rewriting HCG ROM used for half-size characters.

Cursor Control Register (R2)

The cursor control register includes bits CHM, C, CM1, and CM0.

CHM: When CHM is set to 1, DD RAM is selected, the RAM address counter (RAR) is set to 0, and the cursor home instruction is executed. The contents of DD RAM do not change. The cursor or blinking moves to the left edge of the display (the left edge of the first line if two lines are displayed).

C: When C = 1, cursor display is turned on. The cursor is displayed at the position corresponding to the count value of the RAM address counter (RAR). To set data in the RAR, set the index register (IDR) to 1000 to select it, and modify the data in the RAR. Note that the RAM address counter (RAR) automatically increments (decrements) when the RAM is accessed, and the cursor will move accordingly.

CM1/0: Selects cursor display mode (table 12 and figure 9). The blinking frequency (cycle) of the blink cursor and the white/black inverted cursor has 64 frames.

Table 11 Duty Drive Ratio

DT1	DT0	Duty Drive Ratio
0	0	1/14 duty drive
0	1	1/27 duty drive
1	0	1/40 duty drive
1	1	1/53 duty drive

Table 12 Cursor Mode Selection

CM1	CM0	Selected Cursor Mode
0	0	12th raster-row cursor
0	1	Blink cursor
1	0/1	White/black inverted cursor

R/W	RS	DB_7						DB_0
0	1	0	BST	EXT2	EXT1	DT1	DT0	0	DCL

Figure 7 Function Set Register

R/W	RS	DB_7						DB_0
0	1	0	0	0	0	CHM	C	CM1	CM0

Figure 8 Cursor Control Register

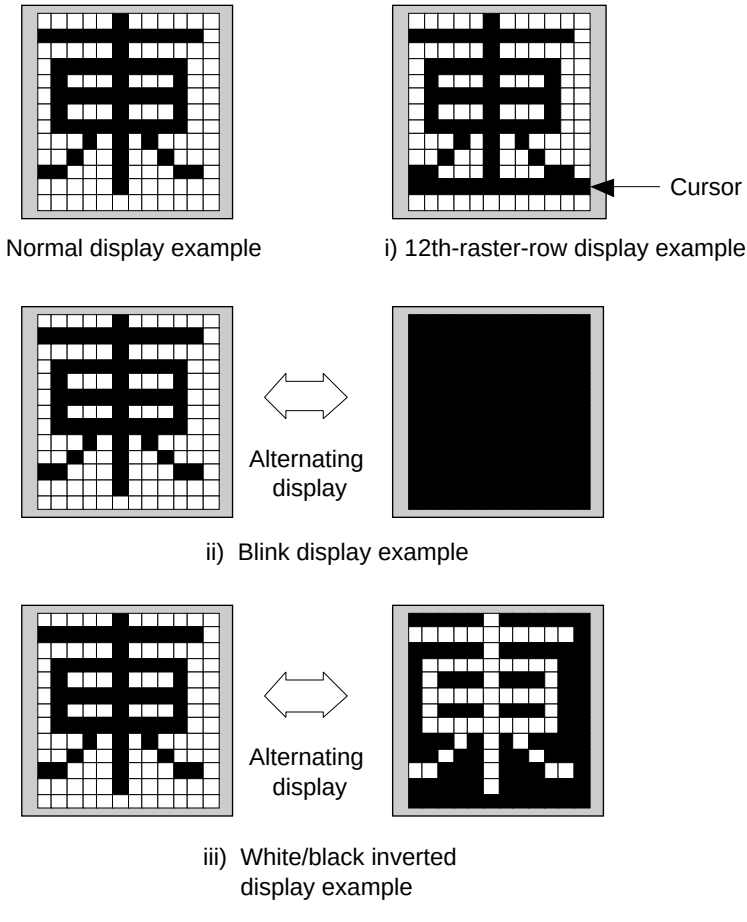


Figure 9 Cursor Display Examples

Display Control Register 1 (R3)

The display control register 1 (figure 10) includes bits ST, DC, and DS.

ST: When ST is 1, the display control register 1 enters the standby mode. The internal operation clock is divided into 32. Data cannot be displayed on the LCD panel, however, the consumption current can be suppressed during the standby mode. Note that the register setting value and the data inside the RAM are maintained.

DC: When DC is 1, the character display is turned on.

DS: When DS is 1, the segment display is turned on. Bit DS can selectively display marks.

Display Control Register 2 (R4)

NC1/0: Selects the display character in the horizontal direction. When performing a horizontal smooth scroll, set the number of display characters larger than the actual number of liquid crystal drive characters. When the frame frequency (cycle) is stable, the operation frequency is proportional to the display characters. Operation frequency must be suppressed by setting the number of display character as small as possible because the consumption current is proportional to the operation frequency. Refer to Oscillator for details.

N/L1/0: Sets the number of display lines. Set the number of display lines larger than the duty drive ratio (DT1/0). Do not set 10 to these bits. Table 13 indicates the settings of the display lines.

Table 13 Display Control Register 2 Setting

Display Lines NL1/0	Display Characters: NC1/0		
	00	**01**	**10**
00	1-line 6 characters	1-line 20 characters	1-line 40 characters
01	2-line 6 characters	2-line 10 characters	2-line 20 characters
10	Setting is inhibited.		
11	4-line 6 characters	4-line 10 characters	4-line 10 characters

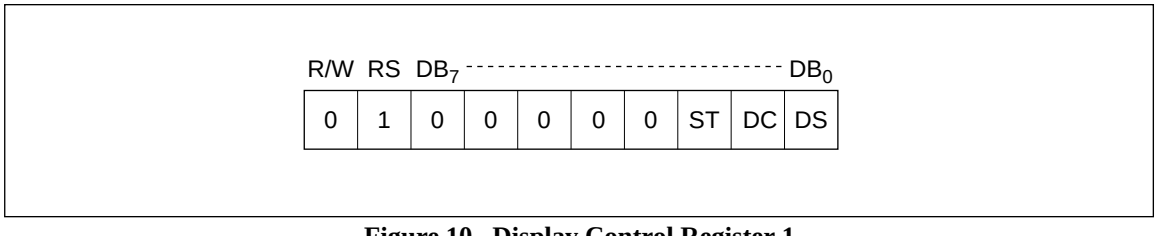


Figure 10 Display Control Register 1

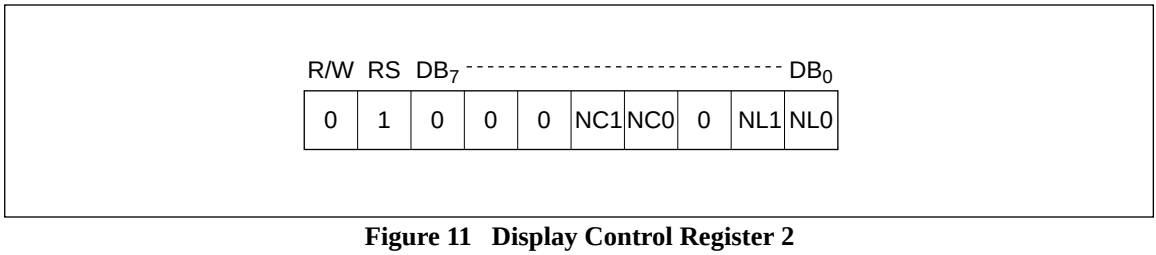


Figure 11 Display Control Register 2

Scroll Control Register 1 (R5)

The scroll control register 1 (figure 12) includes bits SN1, SN0, SL3, SL2, SL1, and SL0.

SN1/0: Selects the starting line to be displayed. When SN1/0 shows 00, display begins from the first line. When SN1/0 shows 01, 10, 11, display begins from the second, third, or fourth line, respectively. Use these bits within the display line setting (NL1/0). SN can be used to display a smooth scroll and DD RAM memory bank switching.

SL0 to SL3: Selects the scroll starting raster-row of the line set by the start display line (SL1/0). When these bits show 0000, a display line starting from the head raster-row (first raster-row) is displayed and can be set to 1100 (13th raster-row) showing the last raster-row. A vertical smooth scroll can be performed by sequentially incrementing the first raster-row. Refer to Vertical Smooth Scroll for details. Note that bits SL0 to SL3 that are set to a value above 1100 will not operate correctly.

Scroll Control Register 2 (R6)

The scroll control register 2 (figure 13) includes bits PS1, PS0, SE4, SE3, SE2, and SE1.

PS1/0: Selects the partial smooth scroll mode. When PS1/0 bits are 00, all characters scroll horizontally across the display. When bits PS1/0 are 01, only the leftmost character is fixed and the remaining characters perform horizontal smooth scroll display. When bits PS1/0 are 10, the two leftmost bits, and when 11, the three leftmost characters are fixed and the remaining characters perform horizontal smooth scroll Refer to Partial Smooth Scroll for details.

SE1 to SE4: These bits enable a dot scroll in display lines designated by scroll control register 3 (R7). When bit SE is 1, the first line is scrolled according to scroll control register 3 (R7). When SE2 is 1, the second line scrolls independently, when SE3 is 1, the third line scrolls independently, when SE4 is 1, the fourth line scrolls independently. Scrolling multiple lines at the same time is also possible.

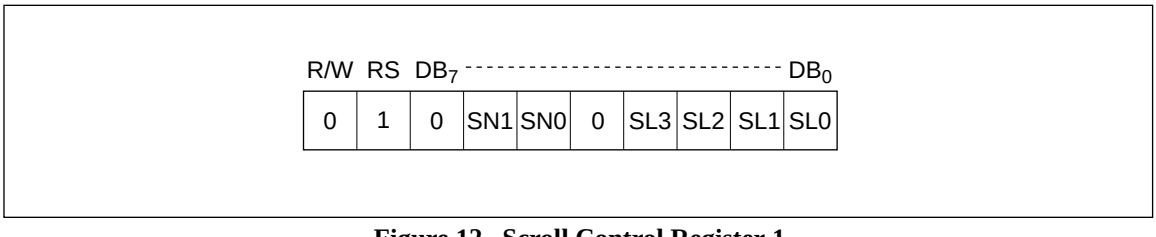


Figure 12 Scroll Control Register 1

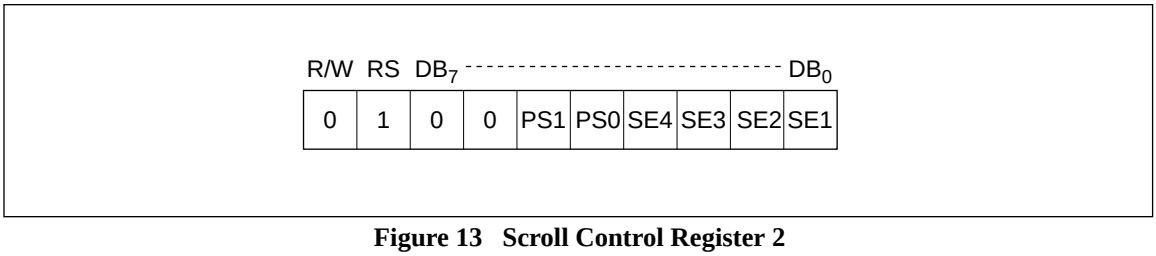


Figure 13 Scroll Control Register 2

Scroll Control Register 3 (R7)

The scroll control register 3 (figure 14) includes bits SQ5, SQ4, SQ3, SQ2, SQ1, and SQ0.

SQ0 to SQ5: These bits designate the number of dots to be horizontally scrolled to the left on the panel. Horizontal smooth scroll can be performed for any number of dots between 1 and 48 inclusive by using the non-display DD RAM area. When these bits are 000000, scrolling is not performed. When these bits are 110000, 48 dots are scrolled to the left. If these bits are set to a value above 110000, 48 dots are still scrolled. Refer to Horizontal Smooth Scroll for details.

RAM Address Register (R8)

The RAM address register (figure15) initially contains the RAM address at which incrementation (decrementation) starts. RAM selection bits (RM1/0) in the entry mode register (R0) select which RAM to access (DD RAM/CG RAM/SEG RAM). When DD RAM (RM1/0 = 00) is selected, address allocation differs according to the number of display lines, but in all cases the most significant bit (RA7) is ignored. During a 1-line display (NL1/0 = 00), addresses H'00 to H'4F are allocated to that line. During a 2-line display, addresses H'00 to H'27 are allocated to the first line, and addresses H'40 to H'67 are allocated to the second line. During a 4-line display, addresses H'00 to H'13 are allocated to the first line, H'20 to H'33 to the second , H'40 to H'53 to the third, and H'60 to H'73 to the fourth. See table 14.

When CG RAM (RM1/0 = 10) is selected, addresses H'00 to H'19 are allocated to the first character and addresses H'20 to H'39 are allocated to the second character, and so on (table 15). The setting of addresses between characters (example: H'1A to H'1F) is ignored here. When SEG RAM is selected (RM1/0 = 11), addresses H'0 to H'F are allocated to the RAM and the upper four bits (R4 to R7) are ignored (table 16).

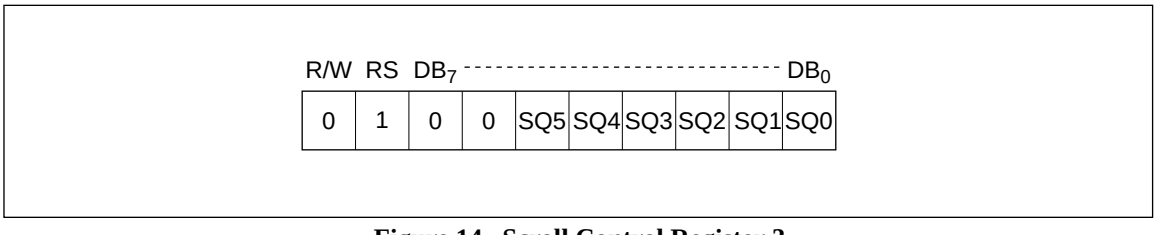


Figure 14 Scroll Control Register 3

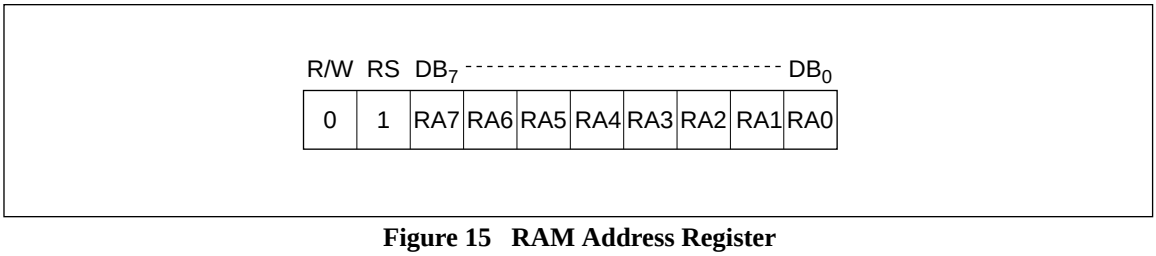


Figure 15 RAM Address Register

Table 14 DD RAM Address Allocation

Displayed Lines	1-Line Display (NL1/0 = 00)	2-Line Display (NL1/0 = 01)	4-Line Display (NL1/0 = 00)
First line	H'00 to H'4F	H'00 to H'27	H'00 to H'13
Second line	—	H'40 to H'67	H'20 to H'33
Third line	—	—	H'40 to H'53
Fourth line	—	—	H'60 to H'73

Table 15 CG RAM Address Allocation

Displayed Character	CG RAM Address
First character	H'00 to H'19
Second character	H'20 to H'39
Third character	H'40 to H'59
Fourth character	H'60 to H'79
Fifth character	H'80 to H'99
Sixth character	H'A0 to H'B9
Seventh character	H'C0 to H'D9
Eighth character	H'E0 to H'F9

Table 16 SEG RAM Address Allocation

Displayed Segment	SEG RAM Address	Displayed Segment	SEG RAM Address
SEG1 to SEG6	H'0	SEG49 to SEG54	H'8
SEG7 to SEG12	H'1	SEG55 to SEG60	H'9
SEG13 to SEG18	H'2	SEG61 to SEG66	H'A
SEG19 to SEG24	H'3	SEG67 to SEG72	H'B
SEG25 to SEG30	H'4	SEG73 to SEG78	H'C
SEG31 to SEG36	H'5	SEG79 to SEG84	H'D
SEG37 to SEG42	H'6	SEG85 to SEG90	H'E
SEG43 to SEG48	H'7	SEG91 to SEG96	H'F

Note: SEG72 to SEG96 are driven by extension drivers.

RAM Data Register (R9)

This register (figure 16) stores 8-bit data that is written to or read from the DD RAM, CG RAM, or SEG RAM at the address indicated by the RAM address counter (RAC). The RAM selection bit (RM1/0) selects the RAM (DD RAM, CG RAM, SEG RAM). After the said RAM is accessed, RAM address is automatically incremented (decremented) by 1 according to the I/D bit.

Note that RAM selection bits (RM1/0) and RAM address register (R8) must be set before reading. If not, the first data read is invalid. If read instructions continue to be executed, however, data will be read correctly from the second read.

Test Register (RF)

This is a test register (figure 17) and must be set to H'00 at all times. This register is automatically cleared (H'00) by reset input; however, it must be cleared by software after power-on if the reset pin is not used.

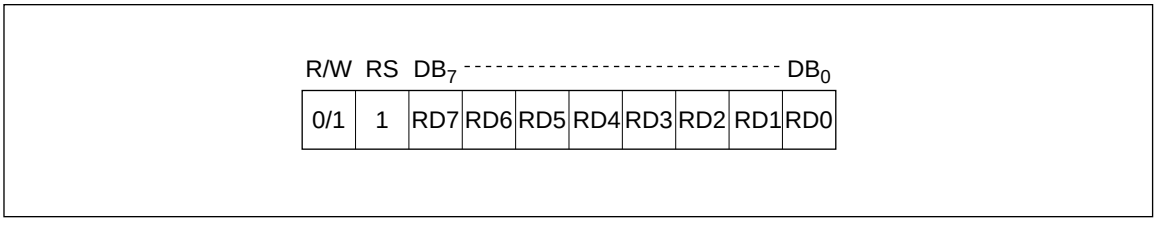


Figure 16 RAM Data Register

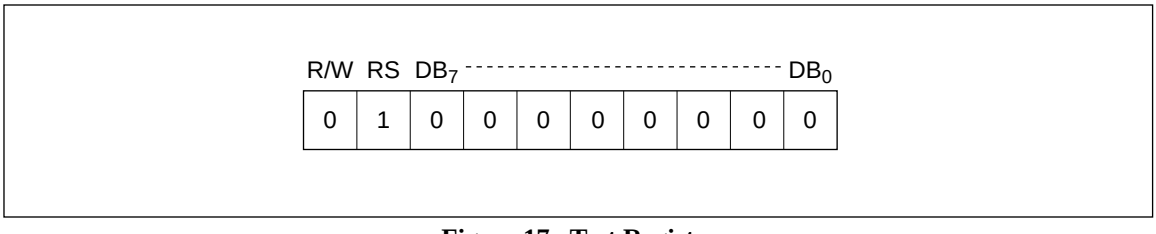


Figure 17 Test Register

Table 17 Instruction Registers

Reg. No.	Index (Hex)	Register	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Clock Cycle
IR	—	Index (IDR)	0	0	—	—	—	—	ID3	ID2	ID1	ID0	Designates the register number of the instruction register to access. ID = 0000: R0 to 1001: R9	12
SR	—	Status (STR)	1	0	BF	NF1	NF0	—	LF3	LF2	LF1	LF0	Indicates the busy flag (BF), display read line position (NF1/0), display read raster-row position (NL0 to NL3).	0
R0	0	Entry mode (EMR)	0	1	0	0	0	0	0	I/D	RM1	RM0	Designates RAM address incrementation or decrementation (I/D) and RAM selection (RM1/0).	12
R1	1	Function set (FSR)	0	1	0	BST	EXT2	EXT1	DT1	DT0	0	DCL	Clears display (DCL) and initializes the DDRAM address. Selects duty drive ratio (DT1/0), enables extension driver (EXT2/1) and sets the booster operation on.	DCL = 1: 492 Other: 12
R2	2	Cursor control (CCR)	0	1	0	0	0	0	CHM	C	CM1	CM0	Designates cursor-on (C) and cursor display mode (CM1/0). Executes cursor home (CHM) instruction.	12
R3	3	Display control 1 (DCR1)	0	1	0	0	0	0	0	ST	DC	DS	Designates standby mode (ST), character display on (DC), and segment display on (DS).	12
R4	4	Display control 2 (DCR2)	0	1	0	0	NC1	NC0	0	0	NL1	NL0	Sets the number of display characters (NC1/0) and display lines (NL1/0).	12
R5	5	Scroll control 1 (SCR1)	0	1	0	SN1	SN0	0	SL3	SL2	SL1	SL0	Sets the display start line (SN1/0) and start raster-row (ST0 to ST3).	12
R6	6	Scroll control 2 (SCR2)	0	1	0	0	PS1	PS0	SE4	SE3	SE2	SE1	Designates partial scroll columns (PS1/0) and scroll display line enable (SE1 to SE4).	12
R7	7	Scroll control 3 (SCR3)	0	1	0	0	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Sets the number of dots to be scrolled (SQR0 to SQR5).	12

Table 17 Instruction Registers (cont)

Reg. No.	Index (Hex)	Register	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Clock Cycle
R8	8	RAM address (RAR)	0	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Resets the address counter for DD RAM/CG RAM/SEG RAM. RAM is selected by RM1/0.	12
R9	9	RAM data (RDR)	0/1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Writes or reads data to and from DD RAM/CG RAM/SEG RAM. RAM is selected by RM1/0.	12
RF	F	Test (TSR)	0	1	0	0	0	0	0	0	0	0	This is a test register. Set 00 in this register.	12

Note: The execution time depends on the input or oscillation frequency.

BF = 1: Internal processing being performed
NF1/0: Position of display read line
LF0 to LF3: Position of display read raster-row
ID = 1: Address increment
= 0: Address decrement
RM1/0: RAM selection (00/01: DD RAM. (10: GG RAM, 11: SEG RAM)
BST = 1: Booster on
EXT2 = 1: Common driver extension enable
EXT1 = 1: Segment driver extension enable
DT1/0: Duty ratio (00: 1/14, 01: 1/27, 10: 1/40, 11: 1/53)
DCL = 1: Executes display-clear instruction
CHM = 1: Executes cursor-home instruction
C = 1: Cursor on
CM1/0: Designates cursor mode (00: 12th raster-row, 01: blinking, 10: white/black inverse)
ST = 1: Standby mode
DC = 1: Character display on
DS = 1: Segment display on

NC1/0: Sets the number of display characters (6 to 40 characters)
NL1/0: Sets the number of display lines (00: 1 line, 01: 2 lines, 11: 4 lines)
SN1/0: Designates the line to start displaying (00: first line, 01: second line, 10: third line, 11: fourth line)
SL0 to SL3: Designates scroll starting raster-row (0000: first raster-row, 1100: 13th raster-row)
PS1/0: Designates partial scroll (00: all columns scroll. 01: the leftmost column fixed, 10: the two leftmost columns fixed, 11: the three leftmost columns fixed)
SE1 to SE4: Designates which line to scroll (SE = 1: enables the first line to be scrolled, etc.)
SQ0 to SQ5: Number of dots to scroll (0 to 48 dots)
RA0 to RA7: RAM address
RD0 to RD7: RAM data

Reset Function

The HD66730 is reset by setting the RESET pin to low level. During reset, the system performs next-control-register setting and executes instructions. The busy flag (BF) therefore indicates a busy state (BF = 1) at this time, which means that only the index register and status register can be accessed.

Display clear (DD RAM reset) is performed automatically by reset input. Since more than 500 clocks of execution cycles are needed to initialize the DD RAM, the reset period must be set to more than this number. Note that if the reset input conditions specified in Electrical Characteristics are not satisfied, the HD66730 will not operate correctly, and reset should be performed by software.

Initialization of Instruction Register Function

1. Index Register: IR

   The index register cannot be initialized by reset. After reset release, the index register must be set to access a control register.

2. Status register: SR

   BF = 1: Busy state

3. Entry mode register: R0

   I/D = 1: +1 (incrementation)
   RM1/0 = 00: DD RAM selection

4. Function set register: R1

   BST = 0: Booster off
   EXT2/1 = 11: Driver extension enable
   DT1/0 = 11: 1/53 duty drive
   DCL = 1: Display-clear execution

Note: At least 500 clock cycles of execution time is needed to clear the DD RAM.

5. Cursor control register: R2

   CHM = 1: Cursor home execution
   C = 0: Cursor display off
   CM1/0 = 00: 12th raster-row cursor display mode

6. Display control register 1: R3

   ST = 0: Standby mode clear
   DC = 0: Character display off
   DS = 0: Segment display off

7. Display control register 2: R4

   NC1/0 = 00: 6-column display mode
   NL1/0 = 00: 1-line display mode

8. Scroll control register 1: R5

   SN1/0 = 00: Starts displaying from the first line.
   SL3 to SL0 = 0000: Starts displaying from the first raster-row.

9. Scroll control register 2: R6

   PS1/0 = 00: Partial scroll release
   SE4 to SE1 = 0000: Disables dot scrolling for all lines.

10. Scroll control register 3: R7

    SQ5 to SQ0 = 000000: Number of dots to be scrolled = 0

11. RAM address register: R8

    RAM address register is automatically incremented during reset when display-clear is executed. Note that after reset is released, this register must be reset by software before accessing RAM.

Initial Setting of Pin Functions

1. Bus/serial interface

   The input level of pin IM selects the 8-bit bus or serial interface. For an 8-bit bus interface, data is written into the index register or read from the status register according to the level of pin R/W. Note that pin RS must be held low during this time. For serial interface, data is written into the index register according to bit R/W. Note that bit RS must be 0 during this time. During reset, only the index register and status register can be set and RAM cannot be accessed.

2. LCD driver output

   Since segment drivers (pins SEG1 to SEG71) are in a display-off state during reset, they output non-selective levels (V2/V3 level) during reset. At this time, a 4-line 6-character display alternates its current. Common drivers (pins COM1 to COM24 and COMS) output non-selective levels (V1/V4 level) during reset, and alternate its current for a 4-line 6-character display.

Note: Pins COM25/COMD are grounded (0V) during reset. When pin COM25 is used without expanding drivers to the common side, display may be performed using the liquid crystal drive voltage. In this case, adjust the liquid crystal voltage during reset.

3. Extension driver interface output

   Since bits EXT2/1 are 11 during reset, extension is performed to both segment side and common side. Pin CL2 outputs the oscillation (operation) frequency clock. Pins CL1 and M output signals in a cycle corresponding to a 4-line 6-character display size. In addition, pins SEGD and COM25/COMD output low (ground level) since the display is turned off.

4. Booster output

   The operation of the internal booster stops because bit BST becomes 0 during reset.

Note: The potential of pins V5OUT2 and V5OUT3 increases by about +0.7 V with respect to GND level when the booster stops. When using external polarized capacitors, make sure that no reverse bias occurs.

Interfacing to the MPU

The HD66730 enters 8-bit bus interface mode when the IM pin is set high. The HD66730 can interface with the MPU via an I/O port. Use the serial interface when there are restraints in the bus wiring width.

Instruction is executed when data is written into the control register. In this case, only the status register can be read (busy check, etc.). In this case, check the busy flag when accessing (polling), or insert an interval considering the execution time and perform the next access when the internal process has completely finished. The instruction execution time depends on the HD66730 operation frequency. When using the internal oscillation circuit of the HD66730, the instruction time will change as the oscillation frequency does. Figure 18 shows an example of an 8-bit data transfer timing sequence. Figure 19 shows an example of interface between HD66730 and 8-bit microcomputers.

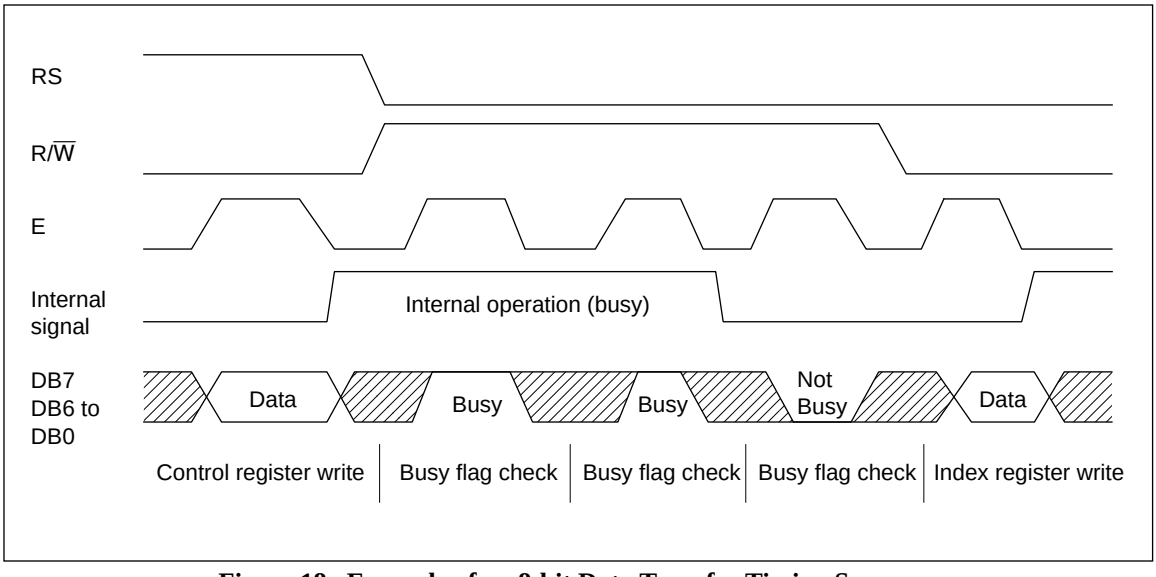
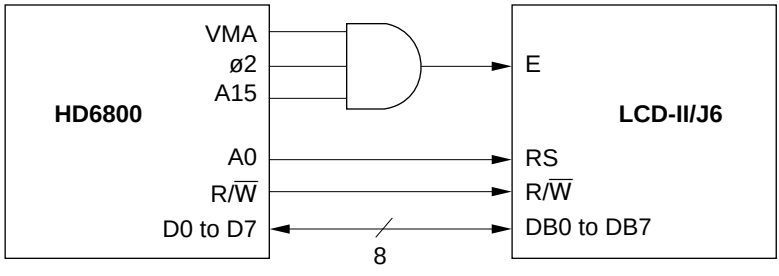
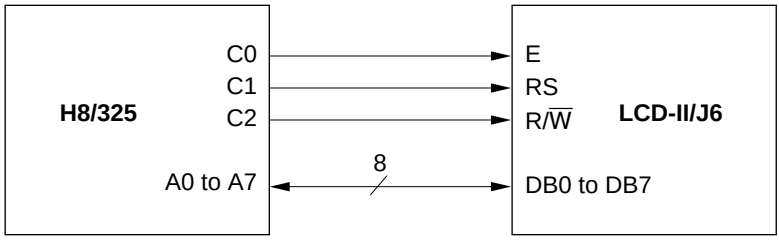


Figure 18 Example of an 8-bit Data Transfer Timing Sequence



a) Bus line interface



b) I/O port interface

Figure 19 Example of Interfacing with 8-Bit Microcomputers

Transferring Serial Data

The HD66730 enters serial interface mode when the IM pin is set low. A three-line clock-synchronous transfer method is used. The HD66730 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66730 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the HD66730 can be reset and serial transfer synchronized by making chip select (CS*) high. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single HD66730 interfaces to a single MPU, an interface can be constructed from the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS*) should be fixed to low.

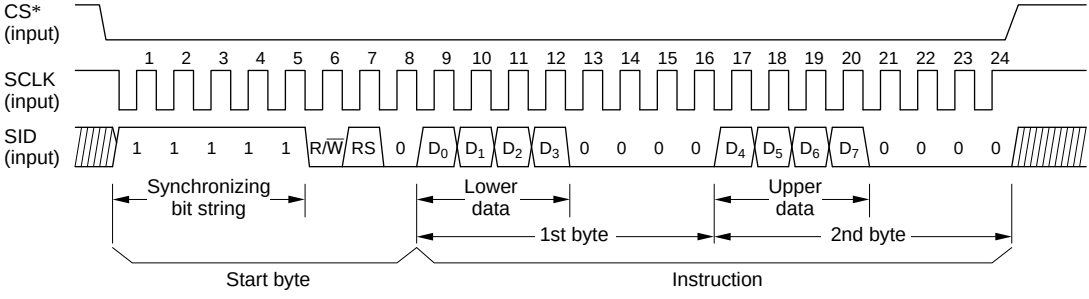
The transfer clock (SCLK) is independent of operational clock (CLK) of the HD66730. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see Continuous Transfer) must be considered since the HD66730 does not have an internal transmit/receive buffer.

Figure 20 shows the basic procedure for transferring serial data. To begin with, transfer the start byte. By receiving five consecutive bits of 1 (synchronizing bit string) at the beginning of the start byte, the transfer counter of the HD66730 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction (R/$\overline{W}$ bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail in the following.

a) Serial data input (receiving)



b) Serial data output (transmitting)

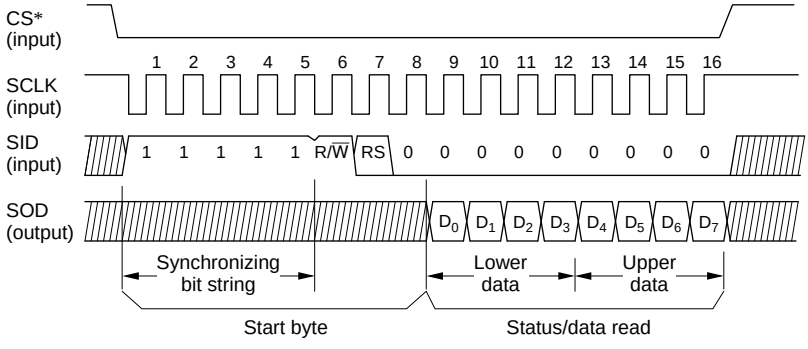


Figure 20 Basic Procedure for Transferring Serial Data

- Receiving (write)

  After receiving the start synchronizing bit string, the R/W bit (= 0), and the RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are received with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

- Transmitting (read)

  After receiving the synchronizing bit string, the R/W bit (= 0), and the RS bit in the start byte, 8-bit read data is transmitted from pin SOD in the same way as receiving. When read data is transmitted with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

  The status register (SR) is read when the RS bit is 0. RAM data is read out when the RS bit is set to 1 after designating RAM data register (R9) with the index register (IR). Bits RM1/0 of entry mode register (R0) select the RAM. When reading RAM data, an interval longer than the RAM reading time must be taken after the start byte has been accepted and before the first data has been read out. During transmission (data output), the SID input is continuously monitored for a start synchronizing bit string (11111). Once this has been detected, the R/$\overline{W}$ and RS bits are received. Accordingly, 0 must always be input to SID when transmitting data continuously.

- Continuous Transfer

  When instructions are received with the R/W bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.

  After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it. To execute the next instruction, the instruction execution time of the HD66730 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.

  In addition, if the next unit of data is read before read execution of previous data is completed for RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, if the amount of wiring used for transmission needs to be reduced, or if the burden of polling on the CPU needs to be lightened, transfer can be performed without reading the busy flag. In this case, insert a transfer wait between instructions so that the current instruction has time to complete execution. Figure 21 shows the procedure for continuous data transfer.

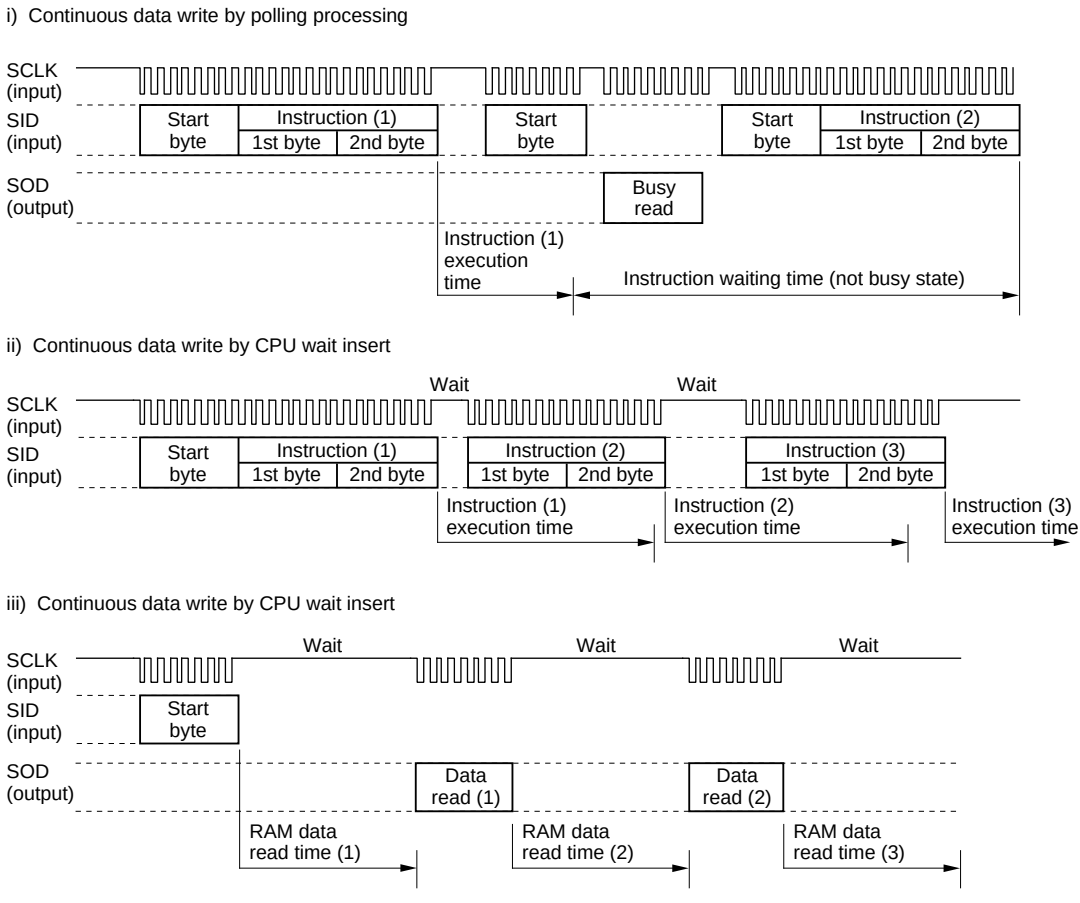


Figure 21 Procedure for Continuous Data Transfer

Combined Display of Full-Size and Half-Size Characters

The HD66730 performs display from the left edge of the display combining 12-dot full-size (character size: 11 × 12 dots) and 6-dot half-size characters (character size: 5 × 12 dots). There will be a one-dot space between these fonts.

The most significant bit in the data (8 bits) in DD RAM is allocated to the designation bit indicating a full-size or half-size character. When this MSB is 0, the full-size character is selected, and when 1, the half-size character is selected.

When the full-size character is selected, 2 bytes of DD RAM are linked and used as a 16-bit code (figure 22). In this case, the lower byte is written into the smaller DD RAM address. 12 bits of this 16-bit code are used as character codes. Up to 4096 character codes can be specified. In addition, two of the remaining four bits can be allocated to a display-attribute code and can designate white/black inverted display for individual characters (refer to Display Attribute Designation). Table 18 shows the relationship between the 16-bit designated JIS code and the HD66730 12-bit character code. 8-bit data designating half-size characters are used as an 8-bit code (figure 23). Specifically, 7 bits of the 8-bit half-size characters become the character codes, so that a total of 128 characters can be displayed (alphanumeric characters and symbols can be displayed as half-size characters).

User fonts can be displayed using the CG RAM. Special symbols not included in the internal CG ROM or the JIS Level-2 Kanji Set can be displayed as needed. Since the display font size of the CG RAM is 12 × 13 dots, CG RAM fonts can be displayed to the right, left, top or bottom, in order to be used to display double-size characters or graphics. Note that the display-attribute code (A1/A0) designation that is to be written into the DD RAM is ignored when the CG RAM is used. In this case, bits 6 and 7 in the CG RAM are used for display-attribute-code designation. Refer to CG RAM for details.

Table 18 Relationship between JIS Codes and HD66730 Character Codes

- JIS first byte code: b1 to b7 (7 bits)
- JIS second byte code: a1 to a7 (7 bits)
- CG RAM address for user fonts: u0 to u2 (3 bits)

				Character Code Arrangement of HD66730											
JIS	**b7**	**b6**	**b5**	**C11**	**C10**	**C9**	**C8**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
Non-kanji	0	1	0	a7	a6	b3	b2	b1	0	0	a5	a4	a3	a2	a1
Level 1 kanji	0	1	1	b7	b6	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
Level 1 kanji	1	0	0	b7	b6	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
User font	—	—	—	0	0	0	0	0	0	0	0	0	u2	u1	u0
				Upper byte				Lower byte							

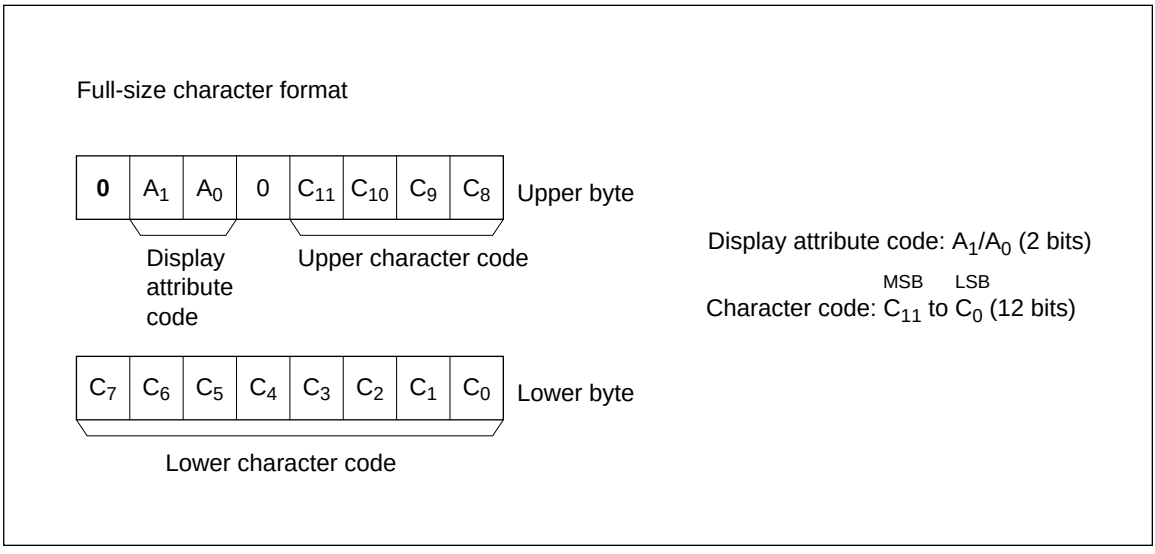


Figure 22 Full-Size Character Codes

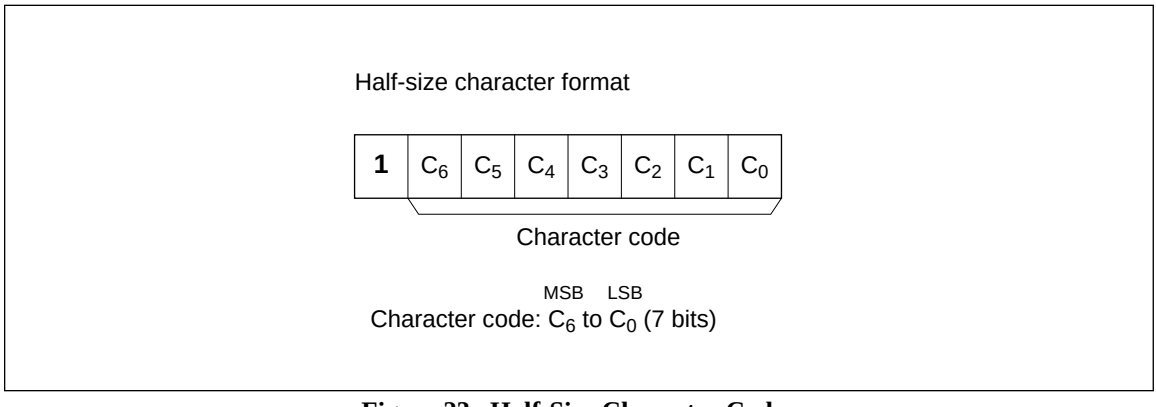


Figure 23 Half-Size Character Codes

An example of displaying full-size and half-size characters together is described here.

Full-size character display conforms to JIS (16 bits). Perform code conversion (16 bits → 12 bits) according to the relationship between the 16-bit JIS code and the HD66730 12-bit character code and write two-byte character data to the DD RAM (write the lower byte to the smaller DD RAM address). The example is shown in table 19. When displaying a half-size character, refer to table 5 the HD66730 Half-size Font List and write one-byte character data into the DD RAM. The example is shown in table 20.

Figure 24 shows how to set data to the DD RAM when performing a 2-line display and figure 25 shows the resulting liquid crystal display.

Table 19 Example of Full-Size Font Conversion

Displayed Character	JIS Code (First/Second Byte)	Character Code (C11 to C0)
東	45/6C (Hex)	AEC (Hex)
京	35/7E (Hex)	2FE (Hex)
都	45/54 (Hex)	AD4 (Hex)
小	3E/2E (Hex)	72E (Hex)
平	4A/3F (Hex)	D3F (Hex)
市	3B/54 (Hex)	5D4 (Hex)
本	4B/5C (Hex)	DDC (Hex)
町	44/2E (Hex)	A2C (Hex)
の	24/4E (Hex)	A0E (Hex)

Table 20 Example of Half-Size Font Code

Display Character	Character Code (C0 to C11)
1	31 (Hex)
2	32 (Hex)
0	30 (Hex)
,	2C (Hex)
M	4D (Hex)
C	43 (Hex)

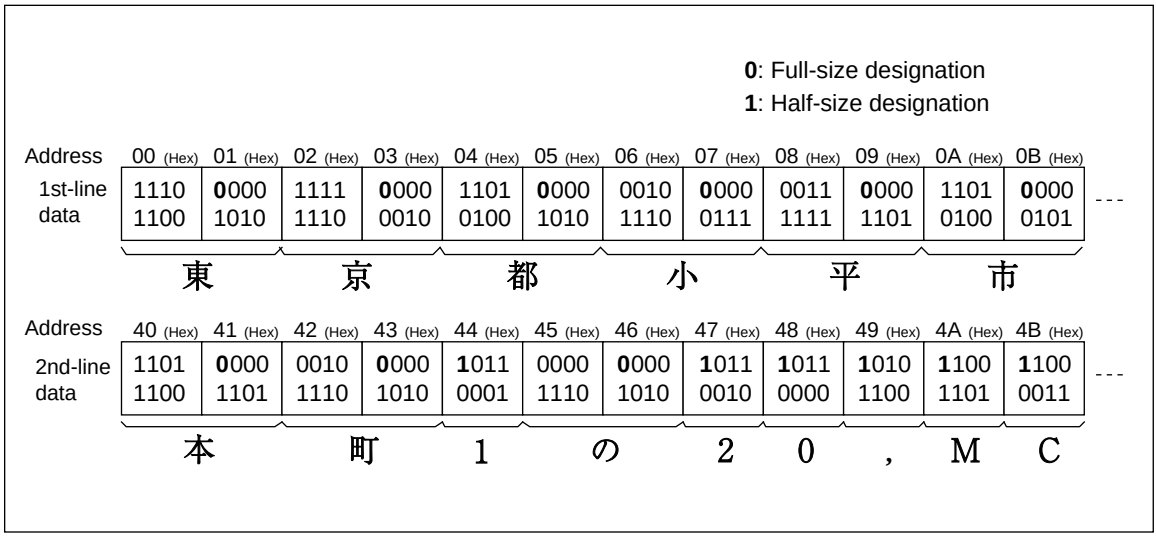


Figure 24 Example of DD RAM Character Code (2-Line Display Mode)

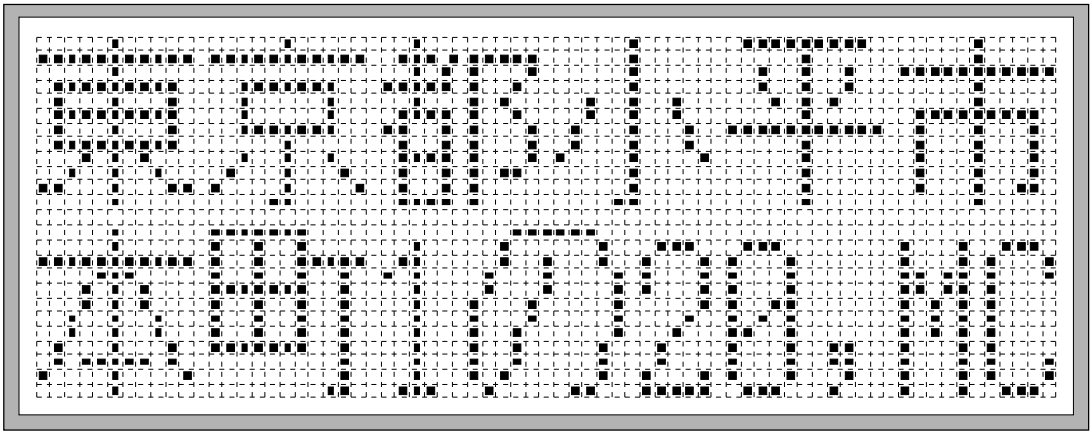


Figure 25 Example of Liquid Crystal Display

Display Attribute Designation

The HD66730 allocates 12 bits of the full-size 16-bit code character to an abbreviated character code and 2 bits to a display-attribute code (figure 26). White/black inverted display, blinking display, and white/black inverted blinking display can be designated for each full-size character (table 21). Display attribute control is performed for a 12×13 dot matrix unit that includes a 11×12 dot full-size character and a column of dots to the right and a row of dots to the bottom (figure 27). The blinking cycle for blinking display and white/black inverted blinking display is 64 frames. Blinking display is performed by changing the display pattern every 32 frames. Since the 8-bit code designated for half-size characters cannot accommodate a display attribute, they will always be displayed normally.

Table 21 Display Attribute Designation

A1	A0	Display State
0	0	Normal display
0	1	White/black inverted display
1	0	Blinking display
1	1	White/black inverted blinking display

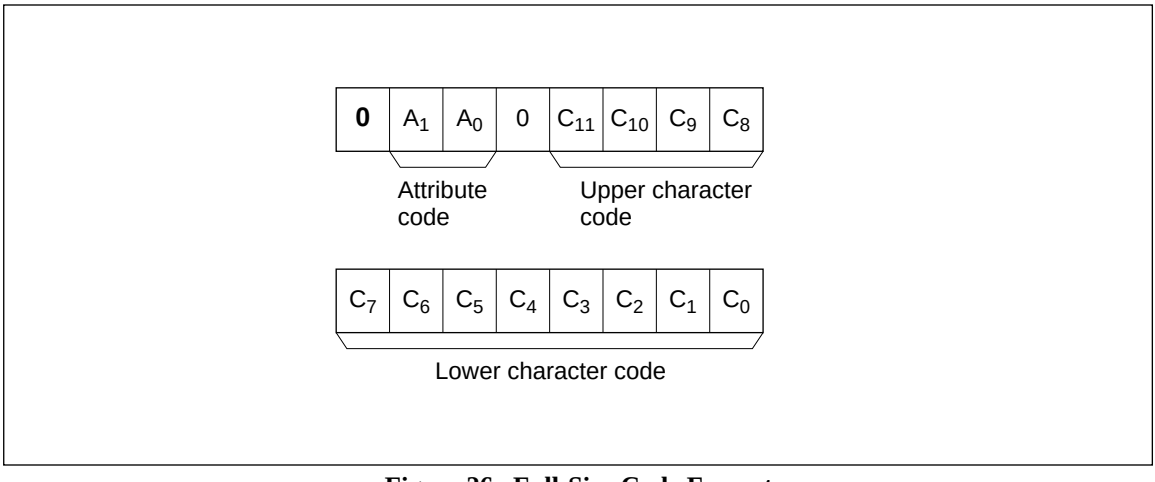
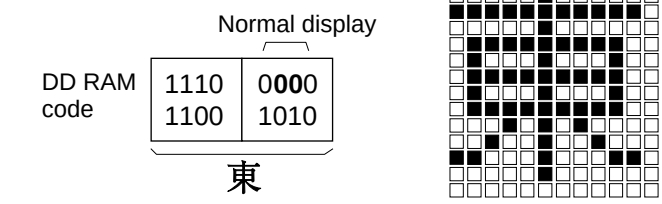
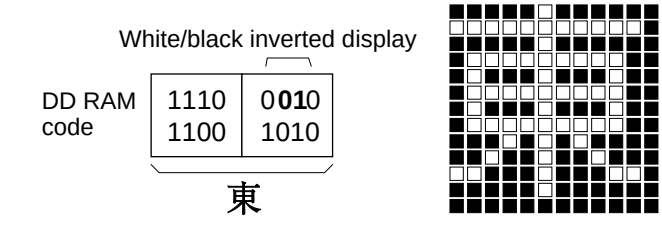


Figure 26 Full-Size Code Format

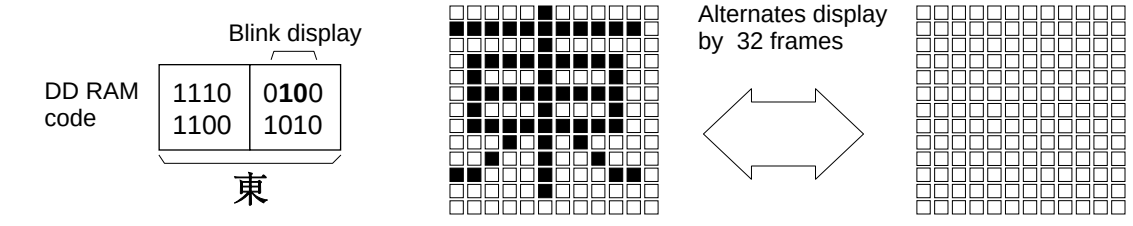
a) Example of normal display



b) Example of white/black inverted display



c) Example of blinking display



d) Example of white/black inverted blinking display

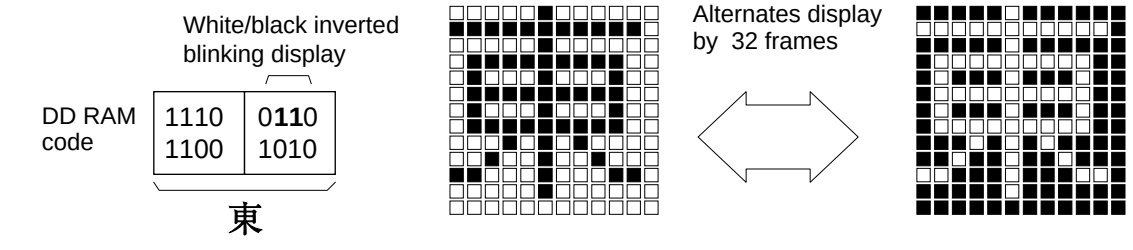


Figure 27 Setting Codes in the DD RAM and Display Examples

Horizontal Smooth Scroll

Data shown on the display can be scrolled horizontally to the left for a specified number of dots (figure 28). The number of dots are set in scroll control register 3 (SCR3: R7), and the display lines to be scrolled are designated by the display line enable bits (SE1/SE2/SE3/SE4) in scroll control register 2 (SCR2: R6). Because the number of dots that can be set for scrolling here is 48, scrolling for more than this number can be achieved by shifting to the left by four characters of character code data in DD RAM for the scroll display line in question, rewriting the characters, and then scrolling again. When rewriting DD RAM while displaying characters, however, character output will momentarily breakdown, and the display may flicker. In this case, first check which display lines are currently being displayed by referring to NF1/0 (line 1 to the line 4) and display raster-rows LF0 to LF3 (raster-row 1 to raster-row 13) in the status register, and then rewrite a DD RAM line that is not being displayed. Keep in mind that scroll display line enable bits (SE1 to SE4) can be used to designate those display lines for which horizontal smooth scroll is desired.

In partial scroll, one to three leftmost characters on the display as specified by the partial scroll bits (PS1/0) of the scroll control register 2 (SCR: R6) are fixed and the remaining characters undergo a smooth scroll to perform partial smooth scroll.

When performing horizontal smooth scroll, the number of characters to be displayed (NC1/0: R4) must be at least 4 characters more than the number of characters actually displayed on the liquid crystal display. For example, set 10 or more display characters (NC1/0) for a single-chip 6-character display.

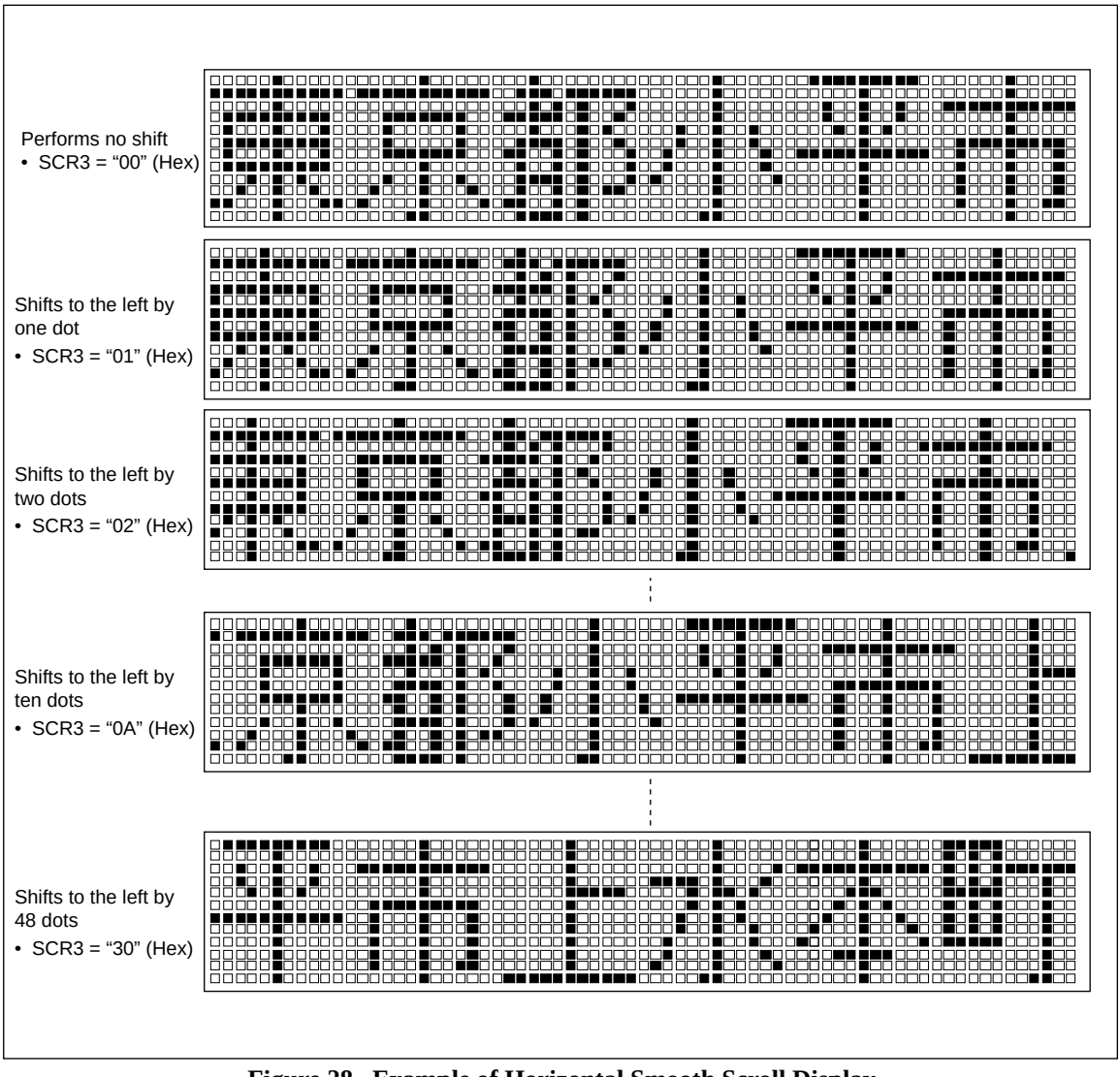
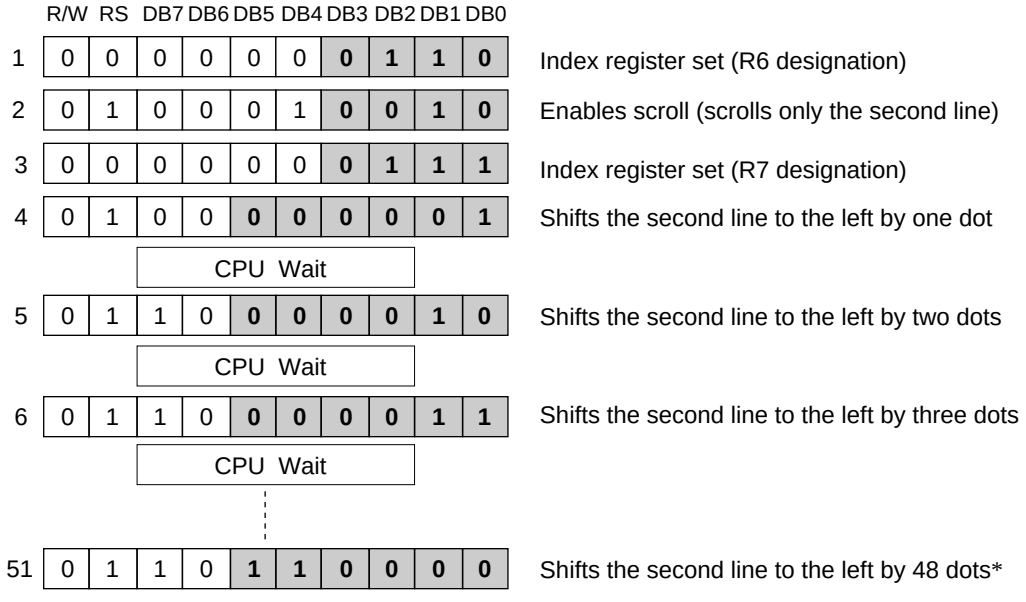


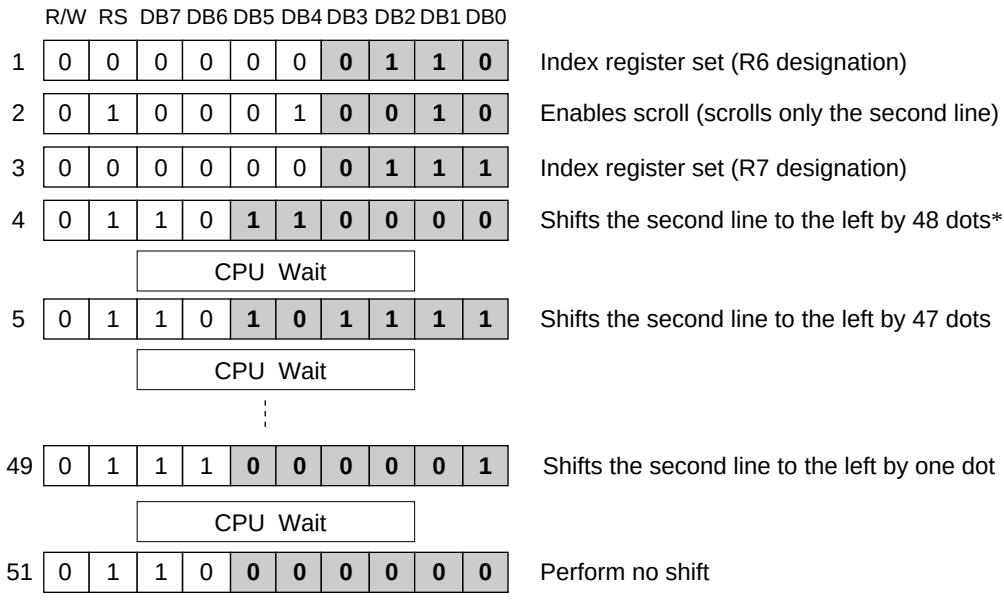
Figure 28 Example of Horizontal Smooth Scroll Display

Examples of Register Setting



Note: The number of dots that can be specified for scrolling is 48. Scrolling for more than this number can be achieved by rewriting DD RAM data and scrolling again from dot 0. Note that the number of characters shown on the LCD and the number of scroll characters must be less than the number of maximum display characters (1-line display mode: 40 characters, 2-line display mode: 20 characters, 4-line display mode: 10 characters).

Figure 29 Example of Executing Smooth Scroll to the Left



Note: The number of dots that can be specified for scrolling is 48. Rewrite 48 dots (4 characters) of data inside the DD RAM and shift them to the right before scrolling. Scrolling for more than this number can be achieved by rewriting the data of DD RAM and begin scrolling from dot 48 again. Note that the number of characters shown on the LCD and the number of scroll characters must be less than the number of maximum display characters (1-line display mode: 40 characters, 2-line display mode: 20 characters, 4-line display mode: 10 characters).

Figure 30 Example of Executing Smooth Scroll to the Right

Partial Smooth Scroll

Partial smooth scroll displays one to three leftmost characters as fixed while the remaining ones undergo a horizontal smooth scroll in the left and right direction. Specifically, the number of leftmost characters to be fixed is specified by the partial scroll bits (PS1/0) in the scroll control register 2 (SCR2: R6). For example, when bits PS1/0 are 10, the two leftmost characters are fixed; when 11, the three leftmost characters are fixed.

Although half-size characters can be displayed in a fixed display area, they must be displayed in even-numbered groups of two, four or six characters. Figure 31 shows an example of smooth scroll performed in a display when bits PS1/0 are set to 10. The two leftmost characters (住所) are displayed as fixed, and the remaining four characters undergo a smooth scroll.

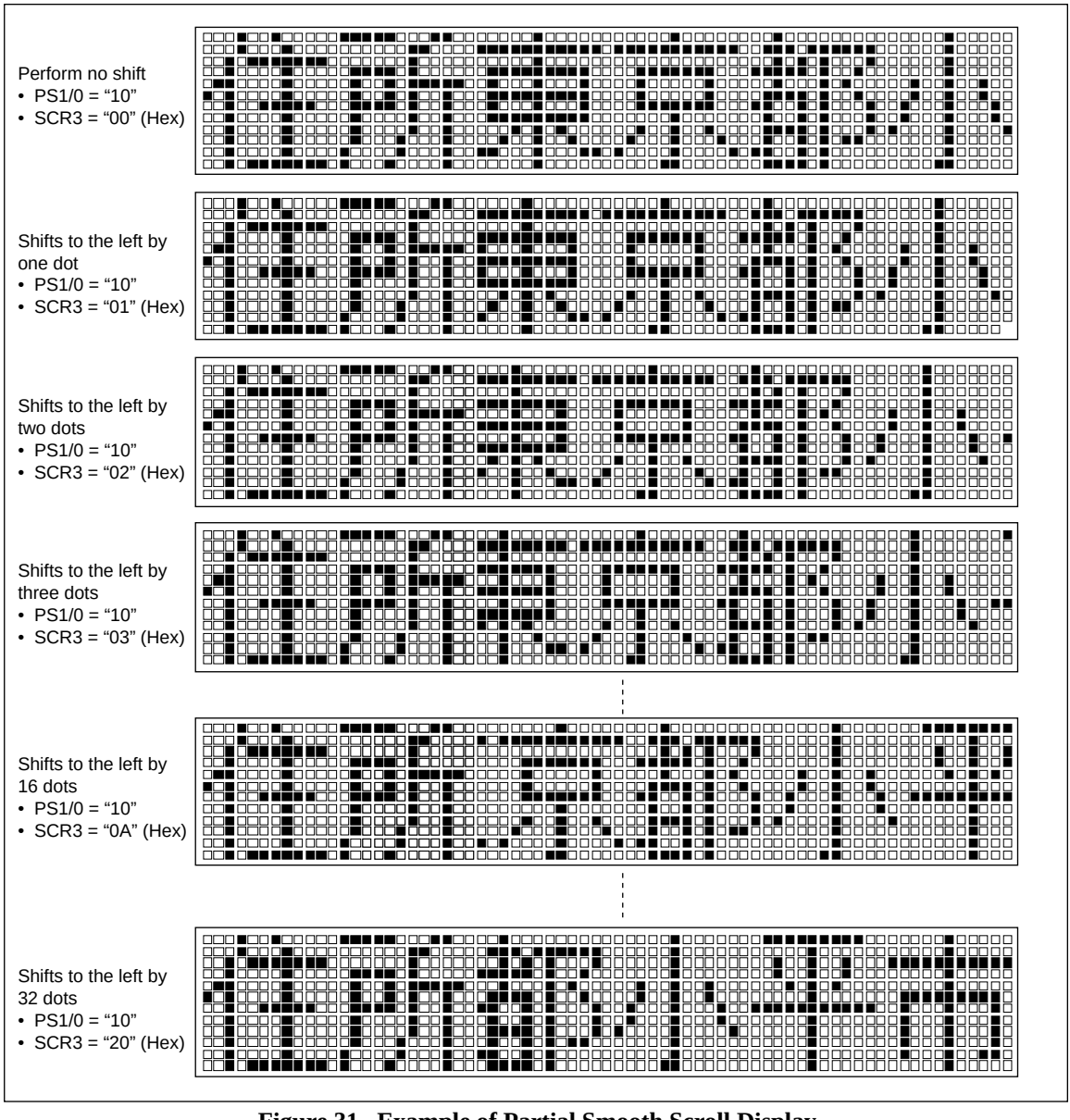


Figure 31 Example of Partial Smooth Scroll Display

Vertical Smooth Scroll

Vertical smooth scroll up and down can be performed by setting the number of display lines (NL1/0: R4) to a value greater than the actual number of liquid crystal display lines, which can be set by the duty drive ratio (DT1/0: R1) to 1/14 (1-line display), 1/27 (2-line display), 1/40 (3-line display), or 1/53 (4-line display). The display line setting (NL1/0: R4), which controls the display, can select 1-line display mode, 2-line display mode, or 4-line display mode.

For example, to perform normal vertical smooth scroll for a 3-line liquid crystal display with a duty ratio of 1/40, set the number of display lines (NL1/0: R4) to 4 lines. Note that if vertical smooth scroll is performed when the number of actual liquid display lines is the same as the number of set display lines, the display line that has scrolled out of the display will appear again from the bottom (or the top) (this function is called lap-around). In a 4-line crystal liquid display, only the lap-around function can be performed. Vertical smooth scroll is controlled by incrementing or decrementing the display line (SN1/0), which indicates which line to start from, and the display raster-row (SL0 to SL3). For example, when performing smooth scroll up, the display raster-row (SL0 to SL3) is incremented from 0000 to 1100 in order to scroll 12 raster-rows. Moreover, by incrementing the display line (SN1/0) and then incrementing the display raster-row from 0000 to 1100 again, a total of 25 raster-rows can be scrolled. Since the DD RAM is only 80 bytes, its data must be rewritten when performing continuous scroll exceeding this capacity.

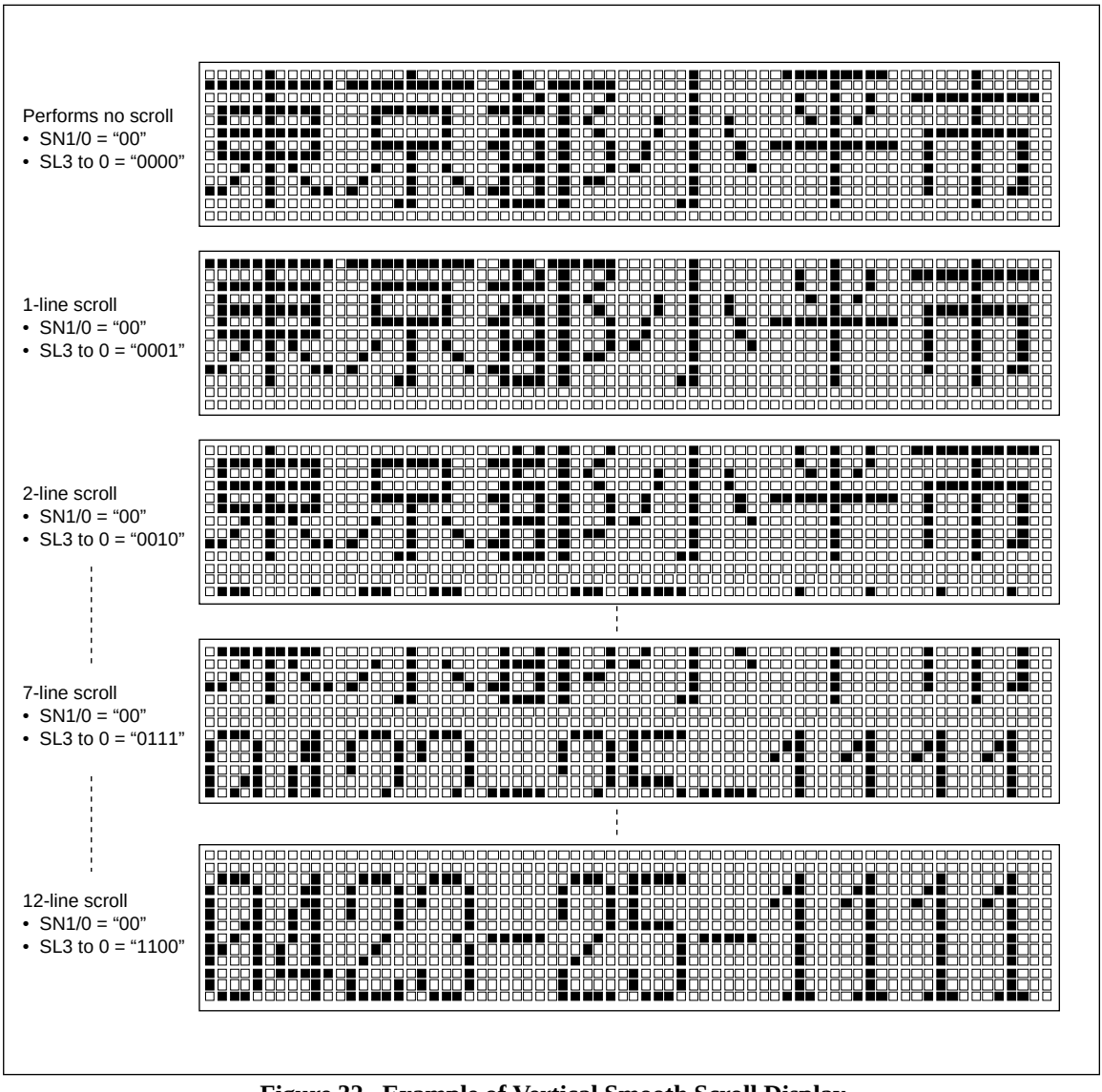
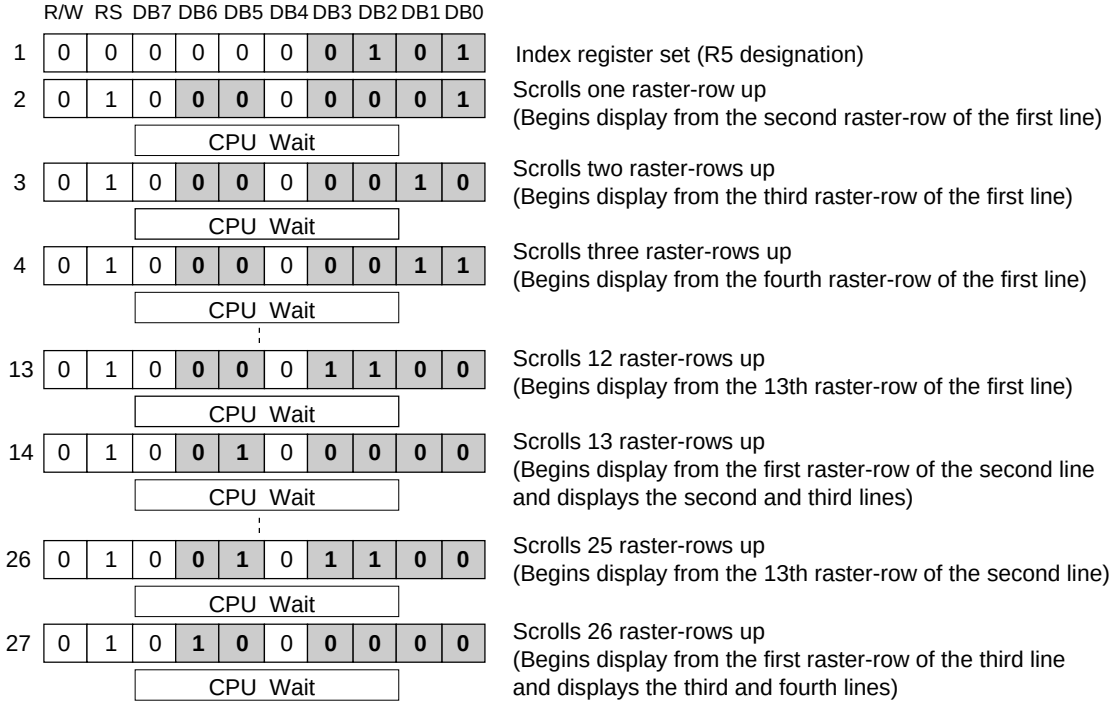


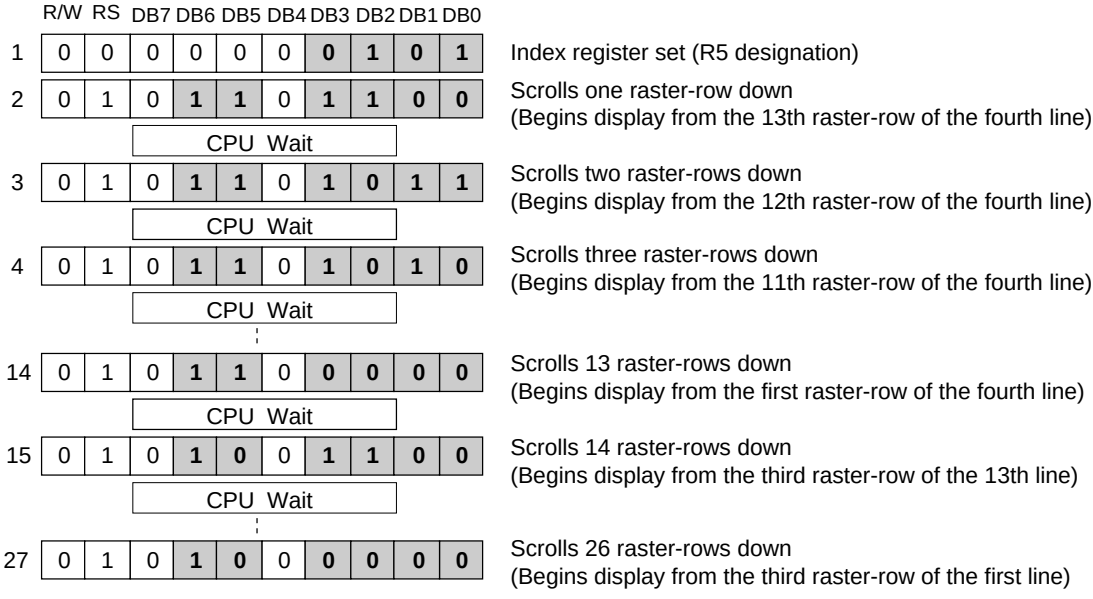
Figure 32 Example of Vertical Smooth Scroll Display

Examples of Register Setting (2-Line Liquid Crystal Drive: DT1/0 = 01, 4-Line Display Mode: NL1/0 = 11)



Note: The DD RAM has 80 bytes. For a 4-line display mode, a 4-line 10-character/line display can therefore be performed. Although the line and raster-row for scrolling can be designated as desired, the first raster-row of the first line will be displayed after displaying raster-row 13 of line 4.

Figure 33 Example of Performing Smooth Scroll Up



Note: The DD RAM has 80 bytes. For a 4-line display mode, a 4-line 10-character/line display can therefore be performed. Although the line and raster-row for scrolling can be designated as desired, the first raster-row of the first line will be displayed after displaying raster-row 13 of line 4.

Figure 34 Example of Performing Smooth Scroll Down

Extension Driver LSI Interface

The HD66730 can interface with extension drivers using extension driver interface signals CL1, CL2, D, and M output from the HD66730, increasing the number of display characters (figure 35). Although the liquid crystal driver voltage that drives the booster of the HD66730 can also be used as the driver power supply of extension drivers, the output voltage drop of the booster increases as the load of the booster increases.

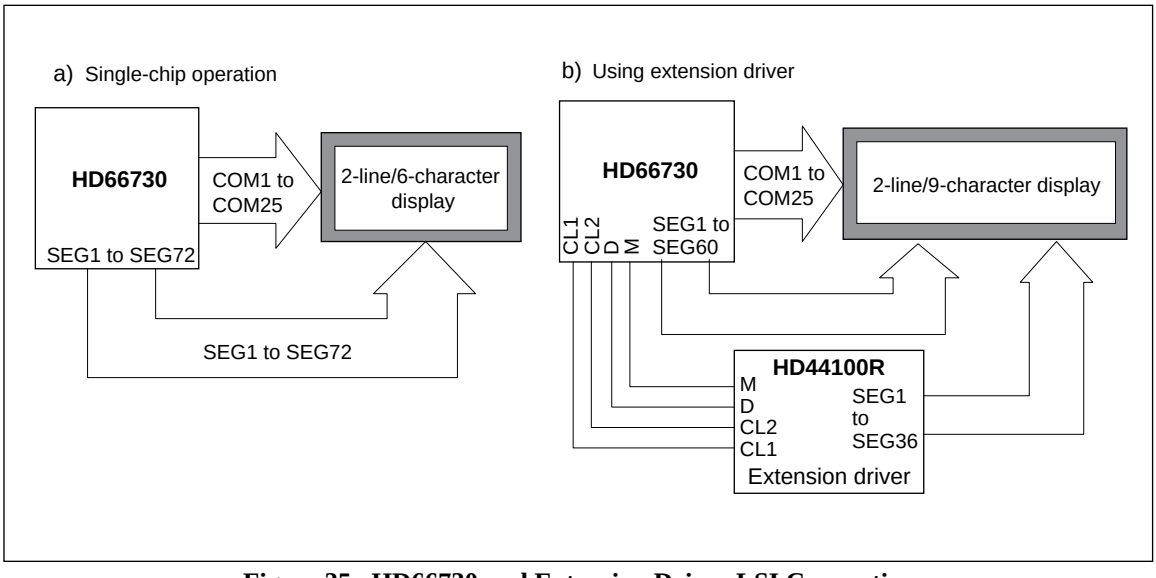


Figure 35 HD66730 and Extension Driver LSI Connection

Relationship between the Display Position at Extension Display and the Display Data RAM (DD RAM) Address

During 1-line display mode, up to 40 characters can be displayed by using extension drivers. In this case, DD RAM addresses H'00 to H'4F are allocated to each display position. During 2-line display, up to 20 characters can be displayed by using extension drivers. DD RAM addresses H'00 to H'27 are allocated to the first line and H'40 to H'67 to the second. See figure 36.

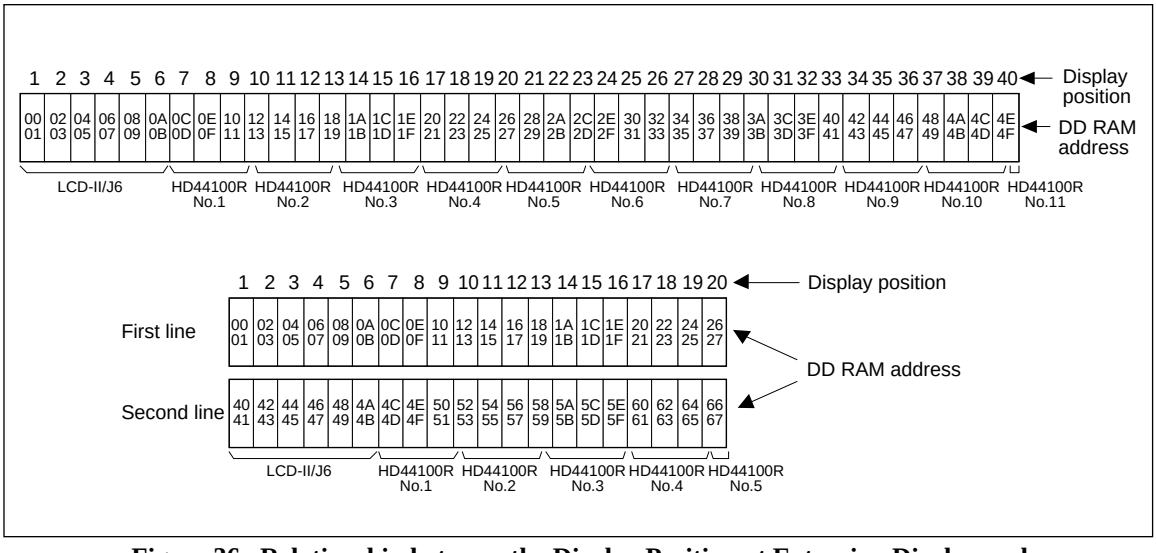


Figure 36 Relationship between the Display Position at Extension Display and the Display Data RAM (DD RAM) Address

Interfacing with the Liquid Crystal Panel

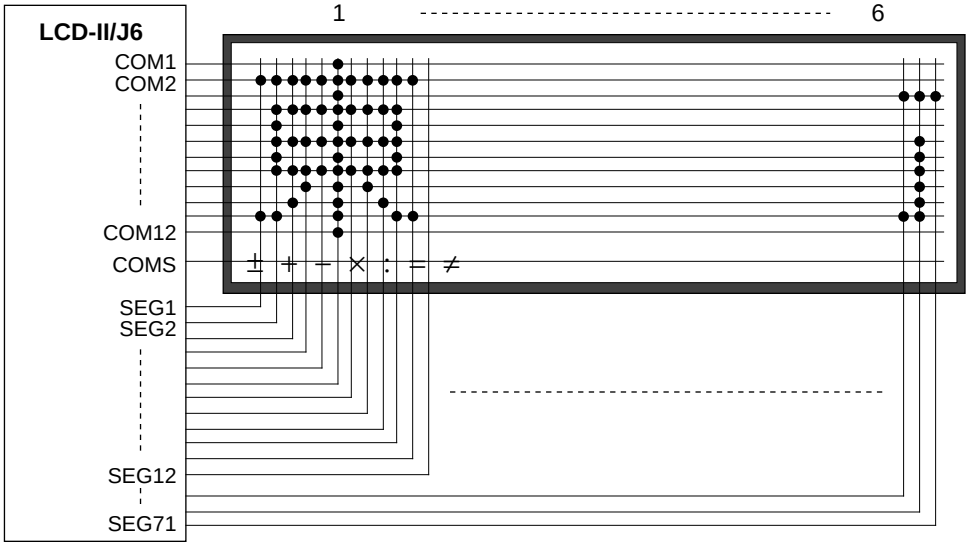
By connecting the HD66730 to extension drivers, the display can be expanded up to a 1-line/40-character, 2-line/20-character, or a 4-line/10-character display configuration. Bits DT1/0 set the duty drive ratio and bits NC1/0 set the number of characters per line. In addition, bits NL1/0 sets the number of display lines during display read control. Table 22 shows the relationship between the number of characters actually displayed on the liquid crystal panel and the corresponding number of extension drivers needed.

Table 22 Relationship between the Number of Liquid Crystal Display Characters and Extension Drivers

	Number of Display Characters per Line						
Display Lines	**6 Characters**	**10 Characters**	**12 Characters**	**16 Characters**	**20 Characters**	**40 Characters**	**Duty Drive**
1 line	(0/0)	(2/0)	(2/0)	(3/0)	(5/0)	(11/0)	1/14
2 lines	(0/0)	(2/0)	(2/0)	(3/0)	(5/0)	Display disabled	1/27
3 lines	(0/1)	(2/1)	Display disabled	Display disabled	Display disabled	Display disabled	1/40
4 lines	(0/1)	(2/1)	Display disabled	Display disabled	Display disabled	Display disabled	1/53

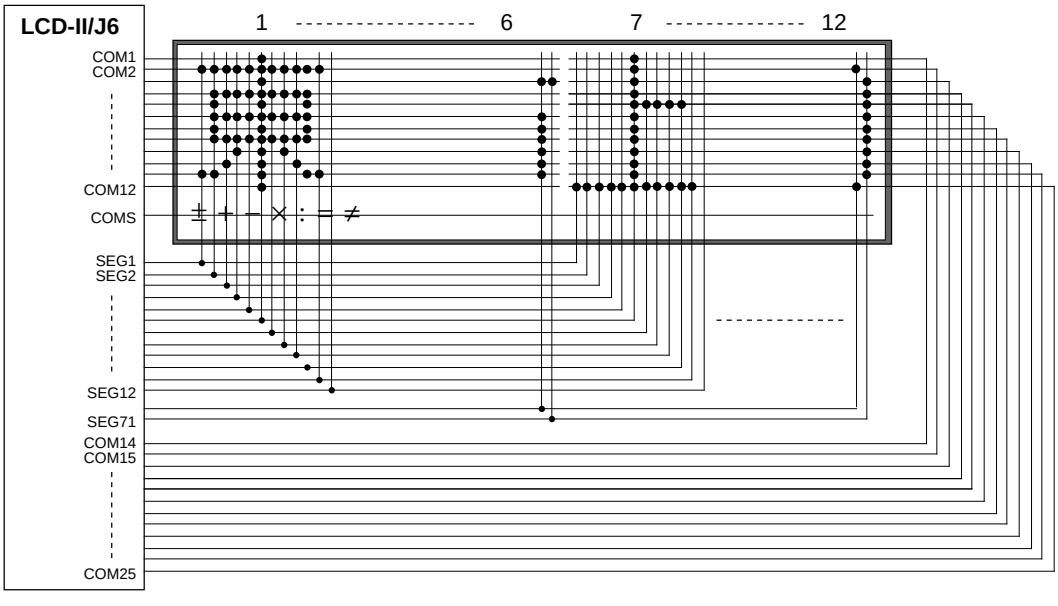
Notes:
1. Numbers in parentheses = (number of extension segment drivers/number of common drivers)
2. This is an example when using the HD44100R (40 output extension drivers), and when Nh represents display characters and Nd extension driver outputs, the number of extension drivers needed can generally be calculated as follows:
   [Number of extension drivers] = (12 * Nh – 71 – 1)/Nd] ↑
3. The right-edge segment (space between characters) is not displayed in 6-character or 16-character display.
4. Horizontal smooth scroll cannot be performed during an 1-line/40-character, 2-line/20-character, 3-line/10-character, or 4-line/10-character display.

Example of Interfacing with a 1-Line Display Panel



Note: The rightmost dot-column space of the 6th character cannot be displayed.

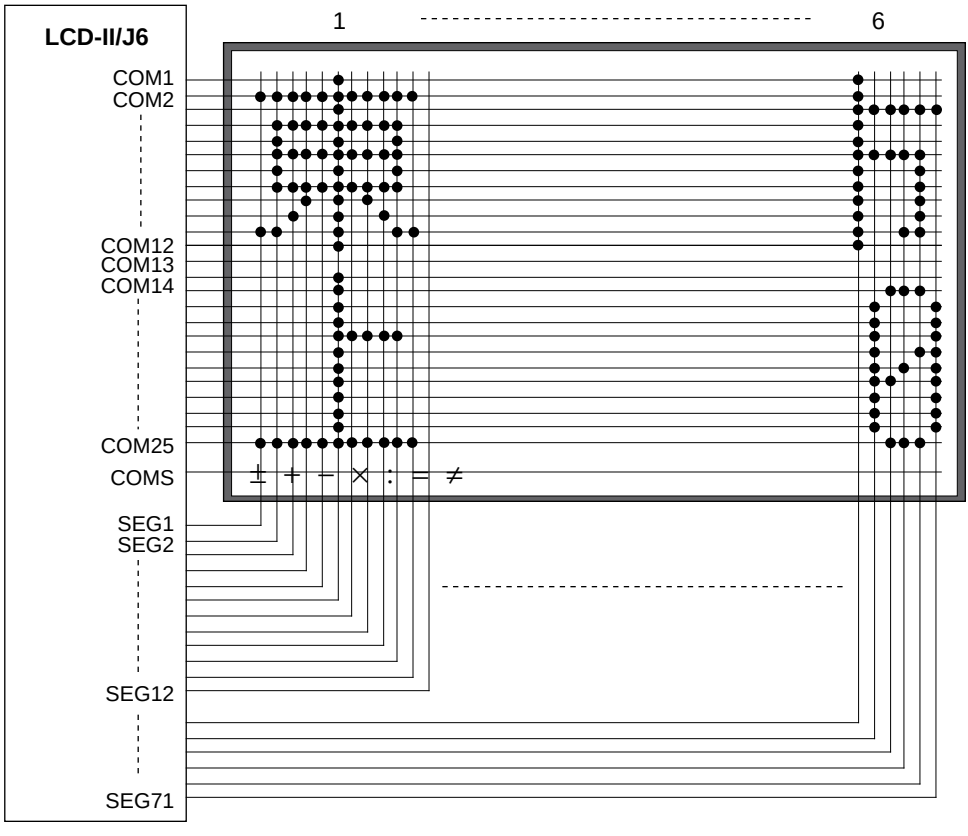
Figure 37 Example of 1-Line/6-Character + 71-Segment Display (Using 1/14 Duty)



Notes: 1. The rightmost dot-column space of the 6th character cannot be displayed.
2. The above figure shows how a liquid crystal panel can be arranged into a 1-line/12-character display while operating the HD66730 in 2-line/6-character display mode. Although the duty ratio becomes high, extension drivers will not be needed. COM13 for spaces between display lines will not be needed.

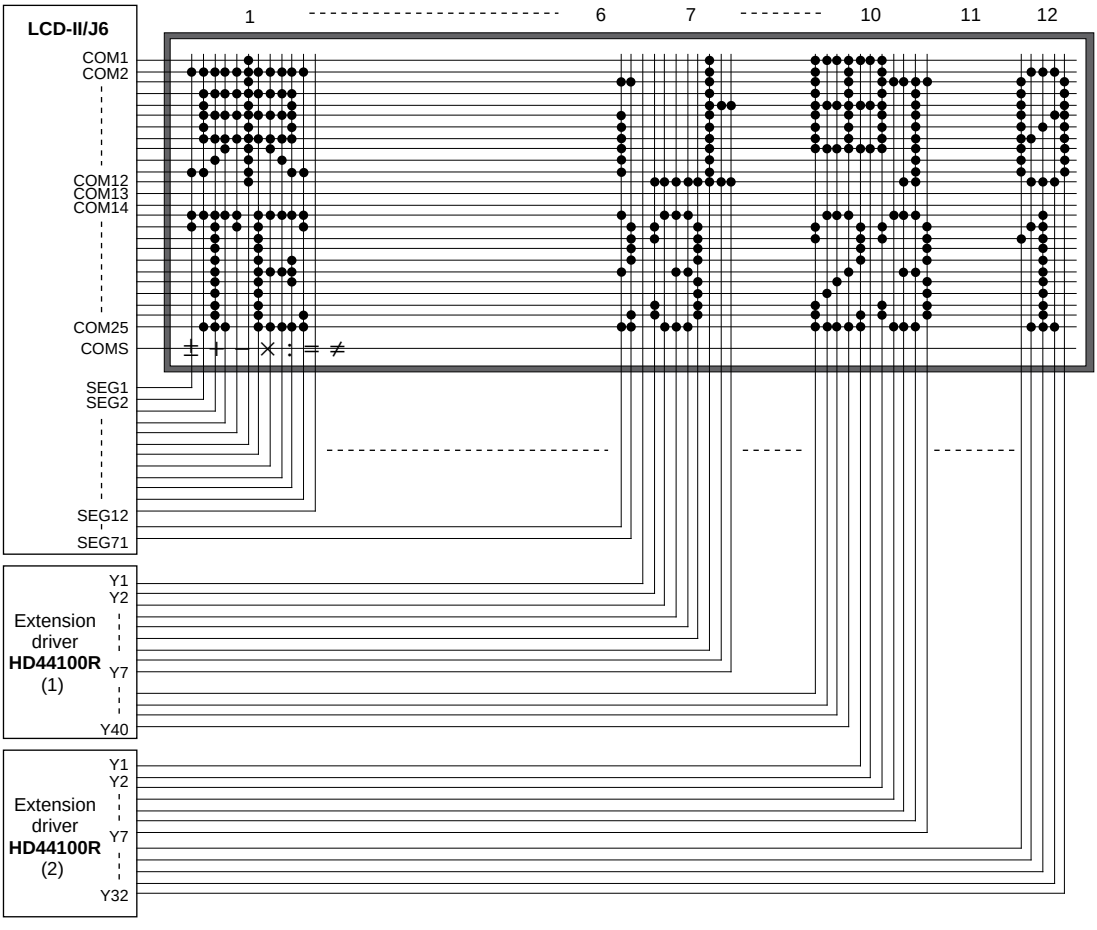
Figure 38 Example of 1-Line/12-Character + 71-Segment Display (Using 1/27 Duty)

Example of Interfacing with a 2-Line Display Panel



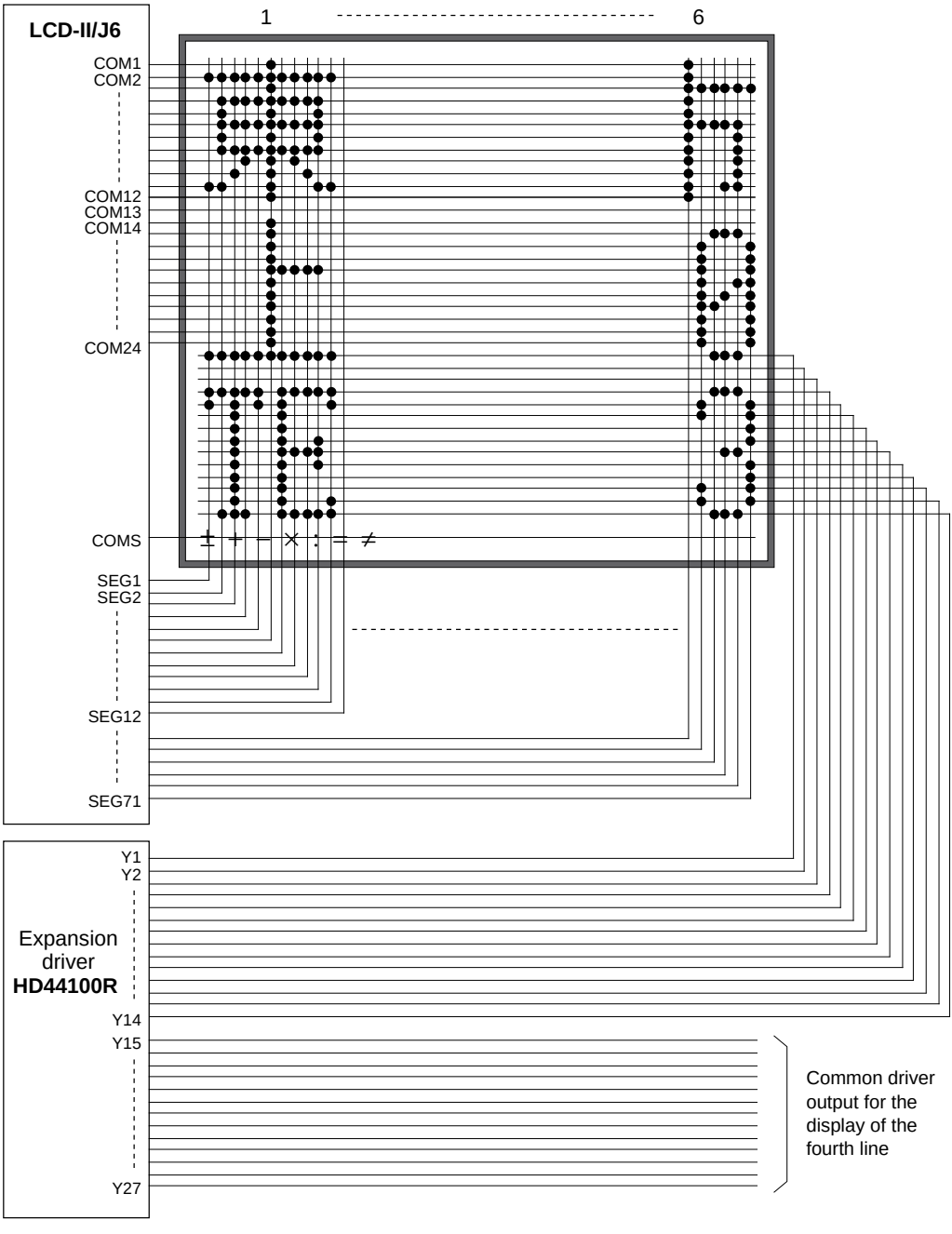
Notes: 1. The rightmost dot-column space of the 6th character cannot be displayed.
2. When performing vertical smooth scroll, or displaying double-size characters or graphic figures by the CG RAM, COM13 can be used for spaces between lines. Display can be performed continuously vertically.

Figure 39 Example of 2-Line/6-Character + 71-Segment Display (Using 1/27 Duty)



Note: COM13 is used for the space between the first line and the second line.

Figure 40 Example of 2-Line/12-Character + 96-Segment Display (Using 1/27 Duty)



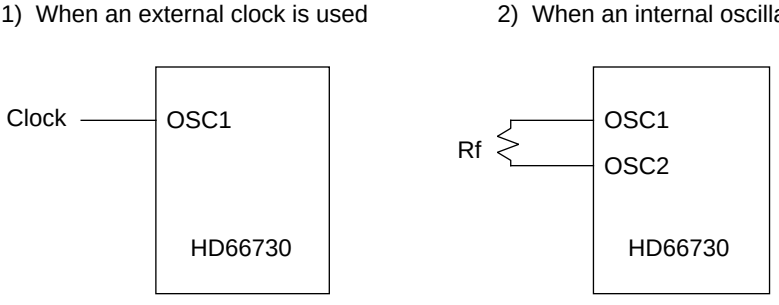
Notes: 1. The rightmost dot-column space of the 6th character cannot be displayed.

2. When performing vertical smooth scroll, or displaying double-size characters or graphic figures by the CG RAM, COM13 is used for spaces between lines. Display can be performed continuously vertically.
3. HD44100 output usage: Y1 = 12th raster-row of the second line, Y2 = space between lines, Y3 to Y4 = third-line characters, Y15 = space between lines, Y16 to Y27 = fourth-line characters

Figure 41 Example of 3-Line/6-Character + 71-Segment Display (Using 1/40 Duty) (Example of 4-Line/6-Character + 71-Segment Display (Using 1/53 Duty))

Oscillator

Figure 42 shows the optimal value of the oscillation frequency or the external clock frequency depends on the duty drive ratio setting (DT1/0), number of display lines (NL1/0), and the number of display characters (NC1/0) in the HD66730. The oscillation frequency or the external clock frequency must be adjusted according to the frame frequency of the liquid crystal drive.



Note: The oscillator frequency can be adjusted by an oscillator resistor (Rf). Refer to Electrical Characteristics for the relationship between the oscillator resistor (Rf) and the oscillator frequency. If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases.

Figure 42 Oscillator Connections

Relationship between the Oscillation Frequency and the Liquid Crystal Display Frame Frequency

Figures 43 to 46 and tables 23 to 26 show the oscillation frequency and the external clock frequency for various registor settings when the frame frequency is 80 Hz.

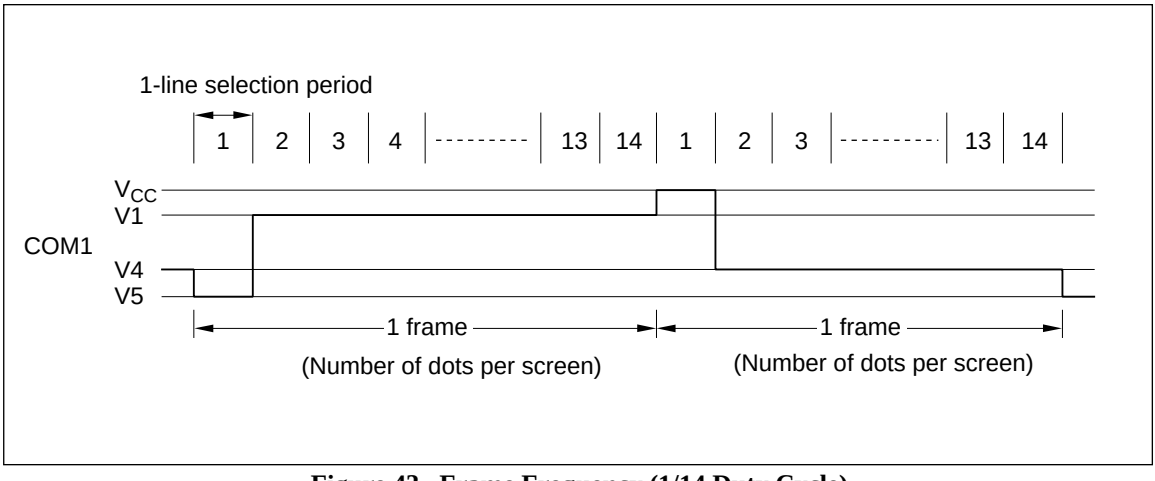


Figure 43 Frame Frequency (1/14 Duty Cycle)

Table 23 1/14 Duty Drive

Number of Display Lines:	**1-Line Display**		
(NL1/0 Set Value):	**(00)**		
Number of display characters	6 characters	20 characters	40 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	240 dots	480 dots
Number of dots per screen (kHz)	1008 dots	3360 dots	6720 dots
Oscillation frequency (kHz)*	80	270	540

Number of Display Lines:	**2-line Display**		
(NL1/0 Set Value):	**(01)**		
Number of display characters	6 characters	20 characters	40 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	120 dots	240 dots
Number of dots per screen (kHz)	1008 dots	1680 dots	3360 dots
Oscillation frequency (kHz)*	80	270	540

Number of Display Lines:	**4-Line Display**	
(NL1/0 Set Value):	**(11)**	
Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	1008 dots	1680 dots
Oscillation frequency (kHz)*	80	270

Note: * The frequencies in table 23 are examples when the frame frequency is set to 80 Hz. Adjust the oscillation frequency so that a optimum frame frequency can be obtained.

1/27 Duty Cycle (DT1/0 = 01: 2-Line Drive)

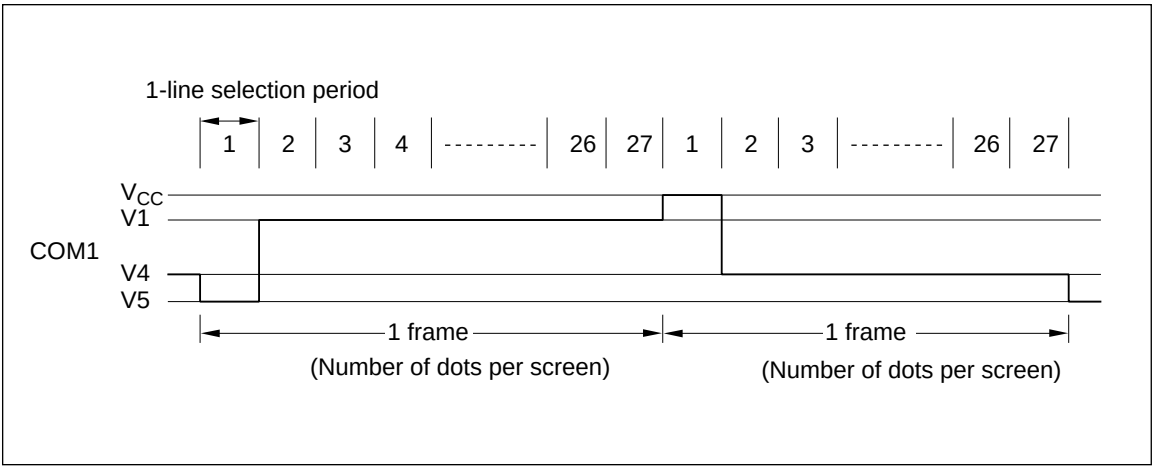


Figure 44 Frame Frequency (1/27 Duty Cycle)

Table 24 1/27 Duty Drive

Number of Display Lines:	**2-Line Display**		
(NL1/0 Set Value):	**(01)**		
Number of display characters	6 characters	10 characters	20 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	120 dots	240 dots
Number of dots per screen (kHz)	1944 dots	3240 dots	6480 dots
Oscillation frequency (kHz)*	155	260	520

Number of Display Lines:	**4-Line Display**	
(NL1/0 Set Value):	**(11)**	
Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	1944 dots	3240 dots
Oscillation frequency (kHz)*	155	260

Note: * The frequencies in table 24 are examples when the frame frequency is set to 80 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

1/40 Duty Cycle (DT1/0 = 10: 3-Line Drive)

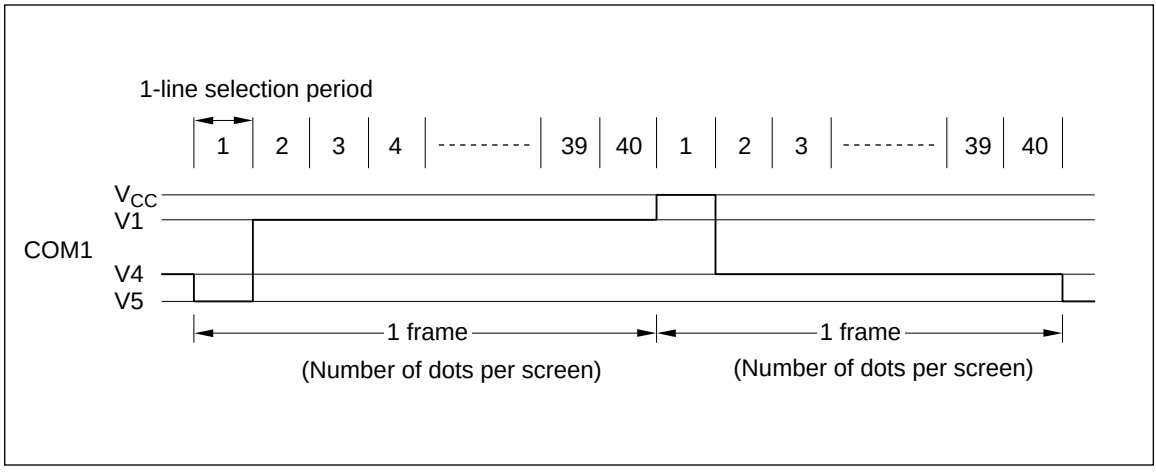


Figure 45 Frame Frequency (1/40 Duty Cycle)

Table 25 1/40 Duty Drive

Number of Display Lines:	**4-Line Display**	
(NL1/0 set value):	**(11)**	
Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	2880 dots	4800 dots
Oscillation frequency (kHz)*	230	385

Note: * The frequencies in table 25 are examples when the frame frequency is set to 80 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

1/53 Duty Cycle (DT1/0 = 11: 4-Line Drive)

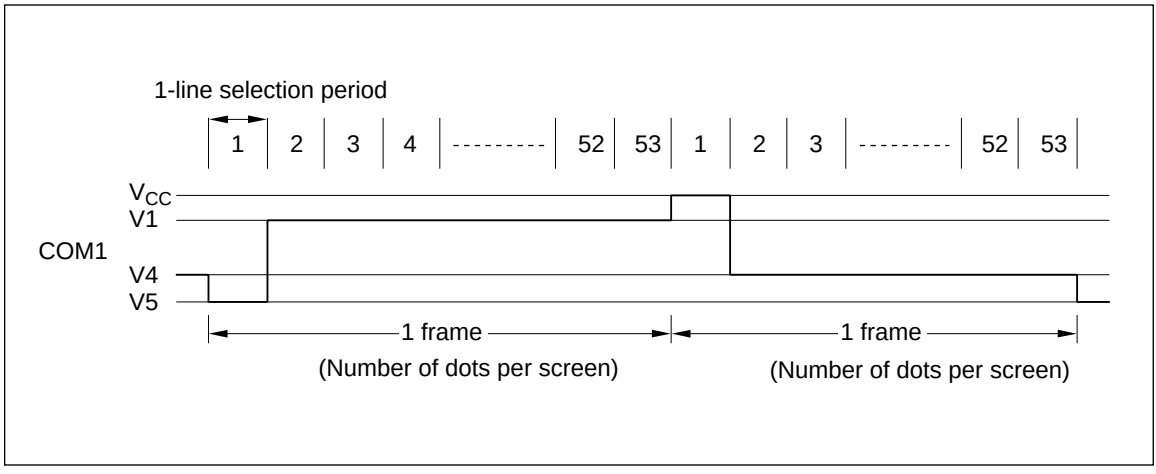


Figure 46 Frame Frequency (1/53 Duty Cycle)

Table 26 1/53 Duty Drive

Number of Display Lines:	**4-line Display (11)**	
(NL1/0 Setting Value):	**(00)**	**(01)**
Number of display characters	6 characters	10 characters
(NC1/0 setting value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	3816 dots	6360 dots
Oscillation frequency (kHz)*	305	510

Note: * The frequencies in table 26 are examples when the frame frequency was is to 80 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

Power Supply for Liquid Crystal Display Drive

The HD66730 incorporates a booster for raising the LCD voltage two or three times that of the reference voltage input below V_{CC} (figure 47). A two or three times boosted voltage can be obtained by externally attaching two or three 1-µF capacitors.

If the LCD panel is large and needs a large amount of drive current, the values of bleeder resistors that generate the V1 to V5 potential are made smaller. However, the load current in the booster and the voltage drop increases in this case.

We recommend setting the resistance value of each bleeder larger than 4.7 kW and to hold down the DC load current to 0.4 mA if using a booster circuit. An external power supply should supply LCD voltage if the DC load current exceeds 0.7 mA (figure 48). Refer to Electrical Characteristics showing the relationship between the load current and booster voltage output. Table 27 shows the duty factor and bleeder resistor value for power supply for liquid crystal display drive.

Table 27 Duty Factor and Bleeder Resistor Value for Power Supply for Liquid Crystal Display Drive

Item		Data			
Drive lines (DT1/0 setting value)		1	2	3	4
Duty factor		1/14	1/27	1/40	1/53
Bias		1/4.7	1/6.2	1/7.3	1/8.3
Bleeder resistance value	R1	R	R	R	R
	R0	R*0.7	R*2.2	R*3.3	R*4.3

Note: * R changes depending on the size of a liquid crystal panel. Normally, R must be 5 kΩ to 10 kΩ. Adjust R to the optimum value with the consumption current and display picture quality.

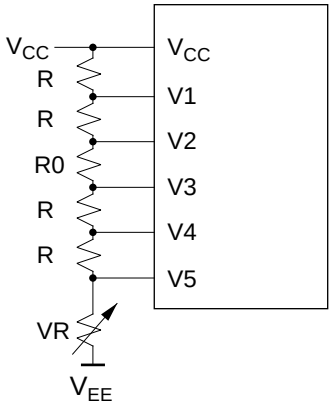
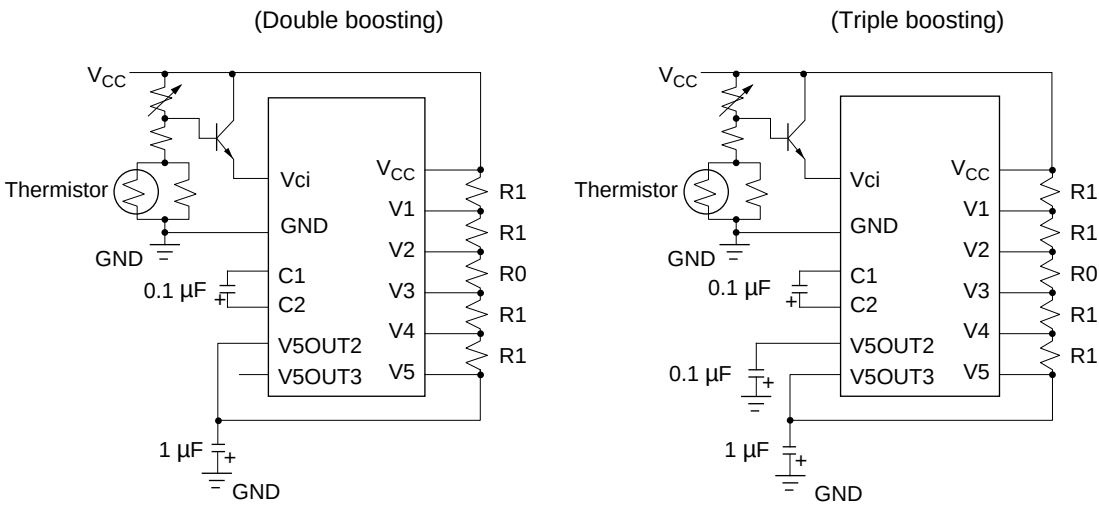


Figure 47 Example of Power Supply for Liquid Crystal Display Drive (with External Power Supply)



Notes:
1. The reference voltage input (Vci) must be set below the power supply (V_{CC}).
2. Current that flows into reference voltage input (Vci) is 2-3 times larger than the load current flowing through bleeder resistors. Note that a reference voltage drop occurs due to the current flowing into the Vci input when a reference voltage (Vci) is generated by resistor division.
3. The amount of output voltage (V5OUT2/V5OUT3) drop of a booster circuit also increases as the load current flowing through bleeder resistors increases. Thus, set the bleeder resistance as large as possible (4.7 kW or greater) without affecting display picture quality.
4. Adjust the reference voltage input (Vci) according to the fluctuation of booster characteristics because the output voltage (V5OUT2/V5OUT3) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors, and manufacturing tolerance. Refer to Electrical Characteristics for details.
5. Adjust the reference voltage input (Vci) so that the output voltage (V5OUT2/V5OUT3) after boosting will not exceed the absolute maximum rating of liquid crystal power supply voltage (15 V).
6. Make sure that you connect polarized capacitors correctly.

Figure 48 Example of Power Supply for Liquid Crystal Display Drive (with Internal Booster)

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +17.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} + 0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (1) (except OSC1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		5, 6
Input low voltage (1) (except OSC1)	V_{IL1}	–0.3	—	$0.2V_{CC}$	V	V_{CC} = 2.7 to 3.0 V	5, 6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D0–D7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D0–D7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D0–D7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D0–D7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RESET* pin)	$–I_p$	5	50	120	µA	V_{CC} = 3 V Vin = 0 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD}	3.0	—	15.0	V	V_{CC}–V5, 1/4.7 bias	16

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	$V_{CC} = V_{ci} = 4.5$ V, $I_o = 0.25$ mA, C = 1 µF, $f_{OSC} = 270$ kHz, $T_a = 25°C$	18
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.7	—	V	$V_{CC} = V_{ci} = 2.7$ V, $I_o = 0.25$ mA, C = 1 µF, $f_{OSC} = 270$ kHz, $T_a = 25°C$	18
Input voltage	V_{Ci}	2.0	—	5.0	V		18, 19

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	80	270	700	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{rcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	180	240	300	kHz	$R_f = 75$ kΩ, $V_{CC} = 3$ V	12

System Interface Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C*3)

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	1000	—	—	ns	Figure 49
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	0 (T.B.D.)	—	—		
Address hold time	t_{AH}	0 (T.B.D.)	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	1000	—	—	ns	Figure 50
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	0 (T.B.D.)	—	—		
Address hold time	t_{AH}	0 (T.B.D.)	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 51
Serial clock (high level width)	t_{SCH}	400	—	—	ns	
Serial clock (low level width)	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{scr}, t_{scf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	5	—	—		

System Interface Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C[*3])

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figure 49
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figure 50
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Sequence

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 51
Serial clock (high level width)	t_{SCH}	200	—	—	ns	
Serial clock (low level width)	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{scr}, t_{scf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100	—	—		
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	5	—	—		

Segment Extension Signal Timing Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 52
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
COMD set-up time		t_{DSU}	300				
Clock rise/fall time	COMD	t_{ct1}	—	—	700		
	Pins except COMD	t_{ct2}	—	—	200		

Reset Timing Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 53

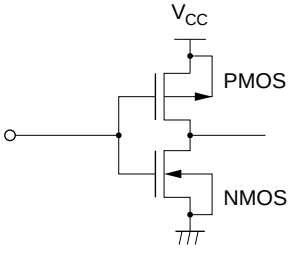
Power Supply Conditions (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rcc}	0.1	—	10	ms	Figure 54
Power supply off time	t_{OFF}	1	—	—		

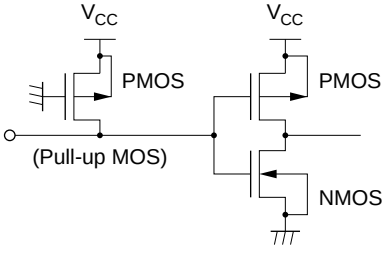
Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic are exceeded, the LSI may malfunction or exhibit poor reliability.
2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

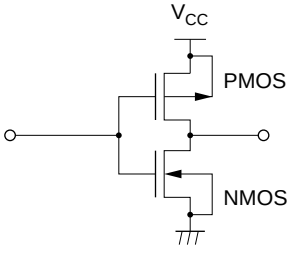
Input pin
Pin: E/SCLK, RS/CS*, RW/SID, IM,



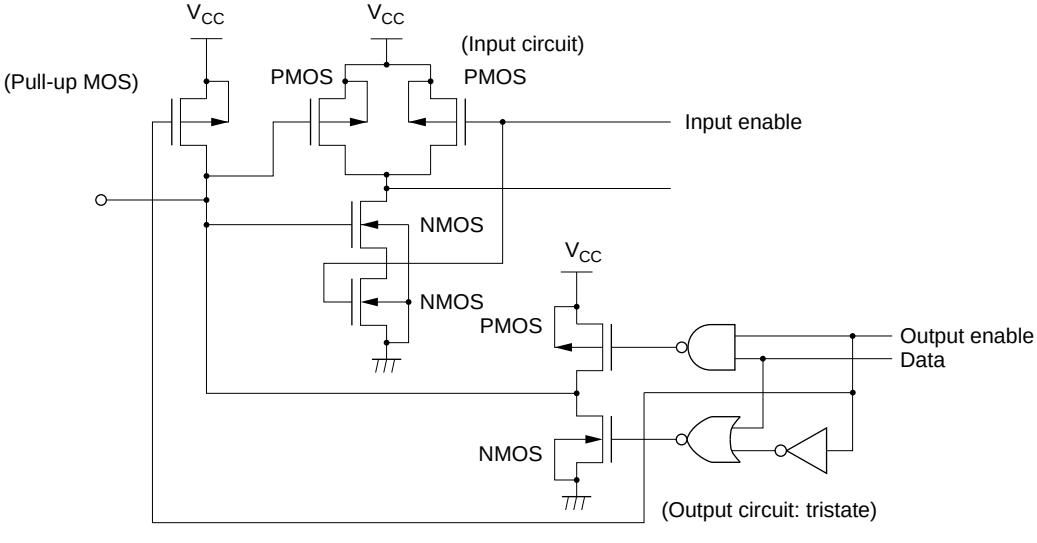
Input pin
Pins: RESET*



Output pin
Pins: CL1, CL2, M, SEGD



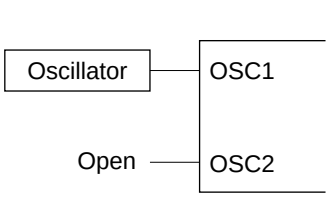
I/O Pin
Pins: DB0/SOD to DB7

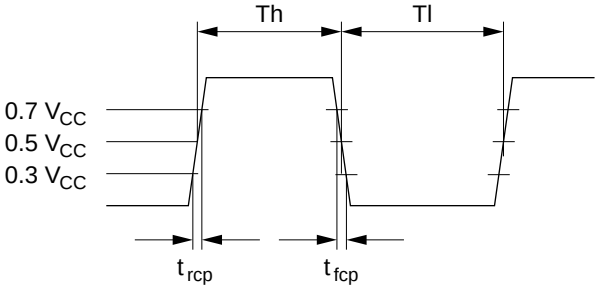


6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.

10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

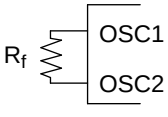
11. Applies only to external clock operation.





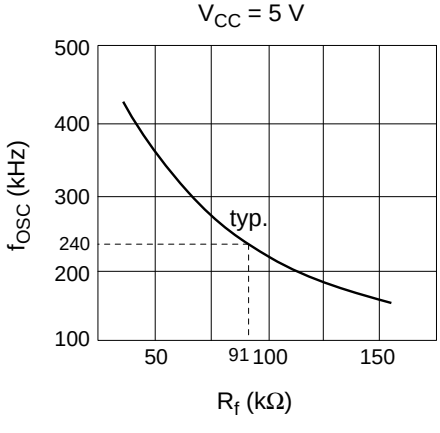
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

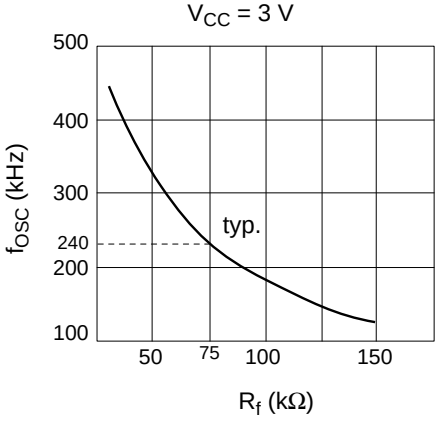
12. Applies only to the internal oscillator operation using oscillation resistor R_f.



Since the oscillation frequency varies depending on the I = OSC2 pin capacitance, the wiring length to these pins should be minimized.

Referential data

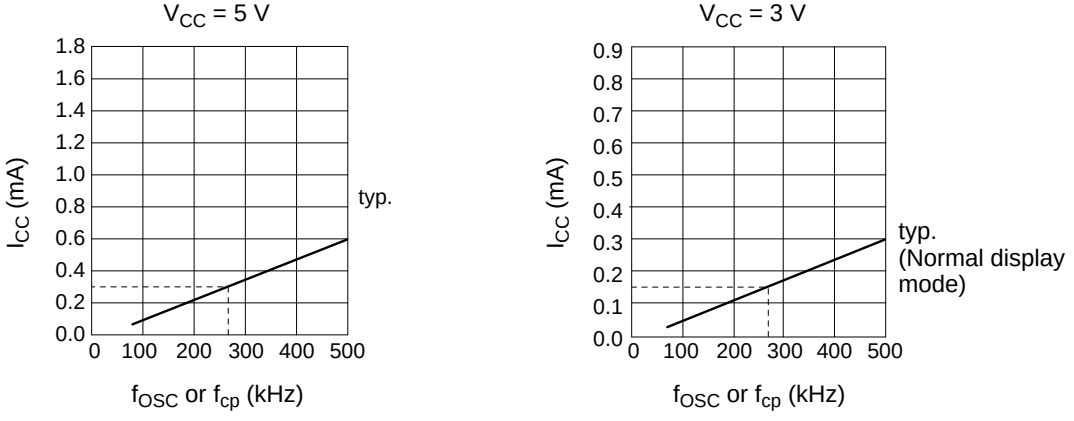




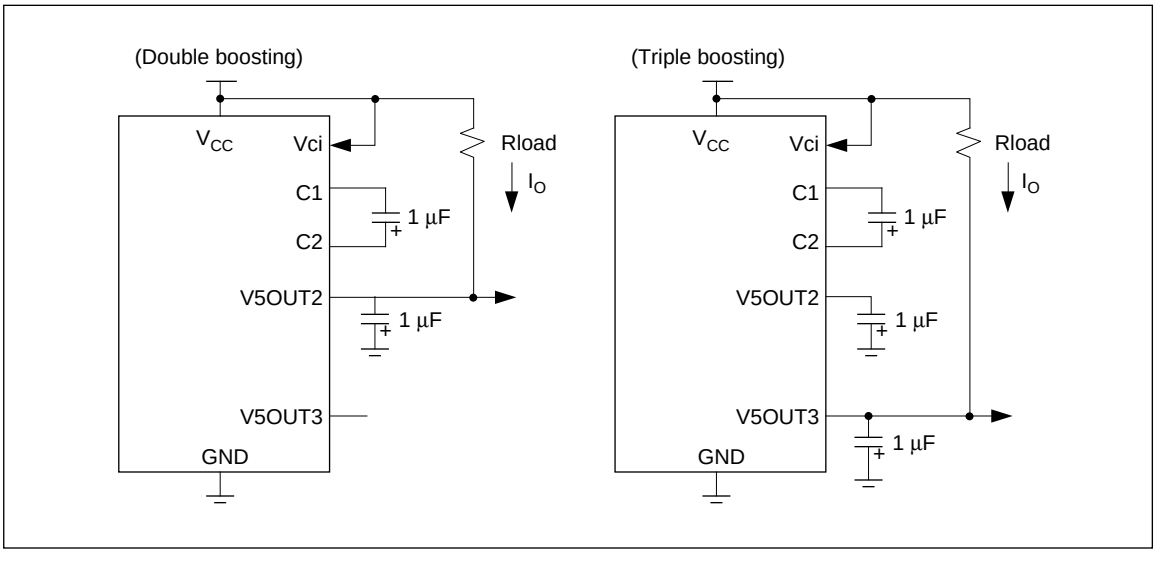
13. RCOM is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM0 to COM25).

    RSEG is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG71).

14. The following graphs show the relationship between operation frequency and current consumption (referential data).



15. Applies to the OSC1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.
17. The TEST pin must be fixed to ground, and the IM pin must also be connected to V_{CC} or ground.
18. Booster characteristics test circuits are shown below.

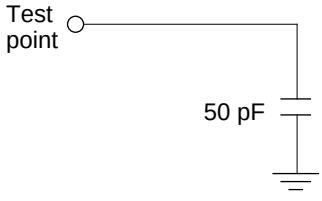


19. Vci ≤ V_{CC} must be maintained.

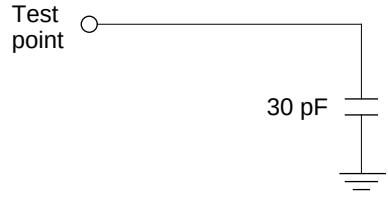
Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB0 to DB7, SOD



Segment extension signals: CL1, CL2, SEGD, M, COM



Timing Characteristics

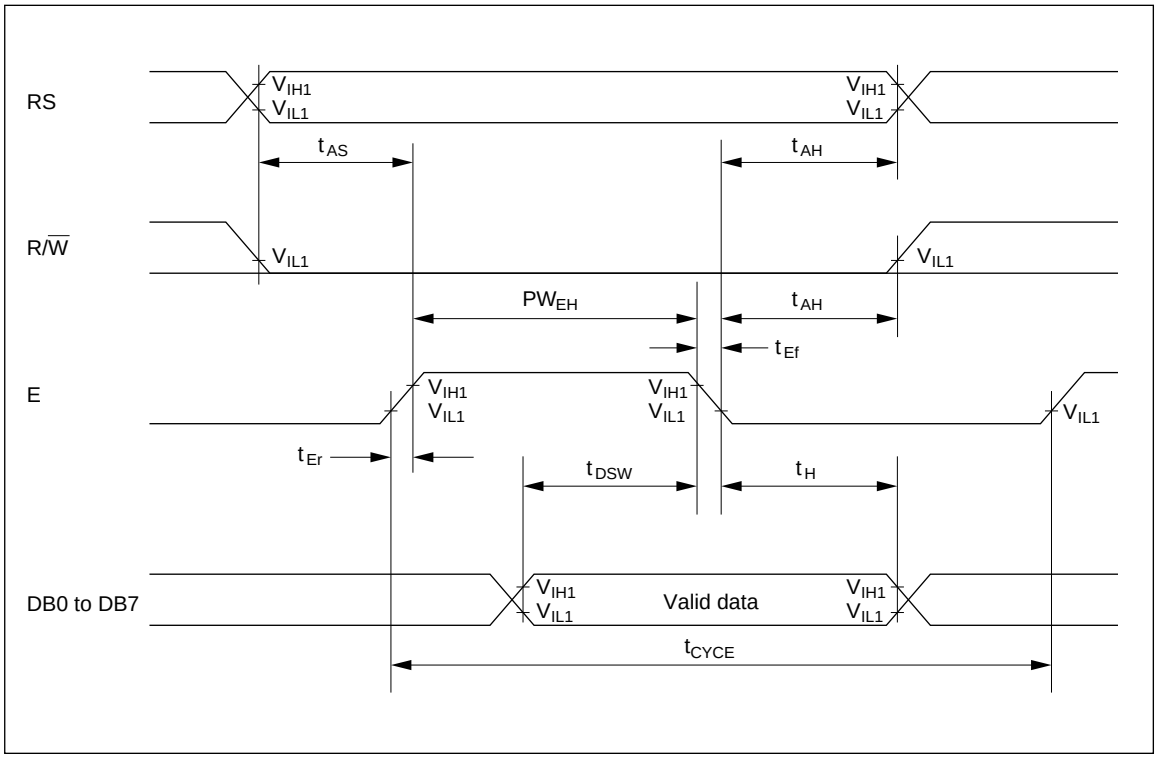


Figure 49 Bus Write Operation

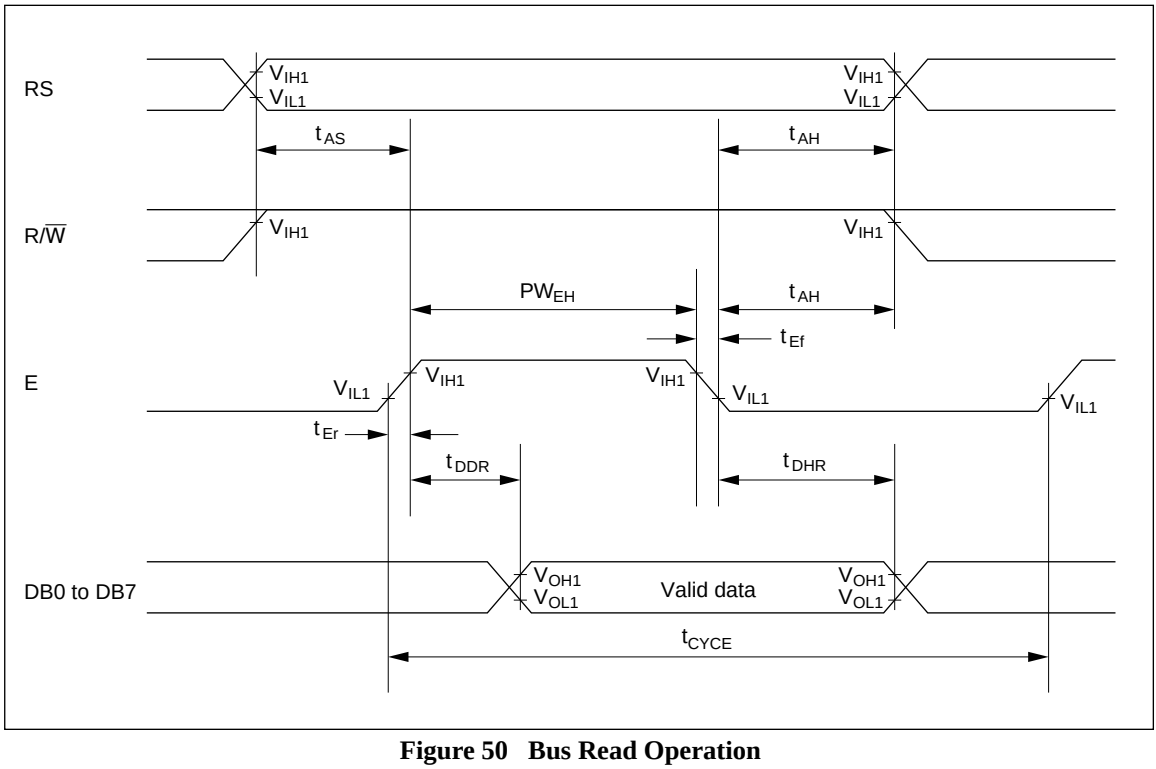


Figure 50 Bus Read Operation

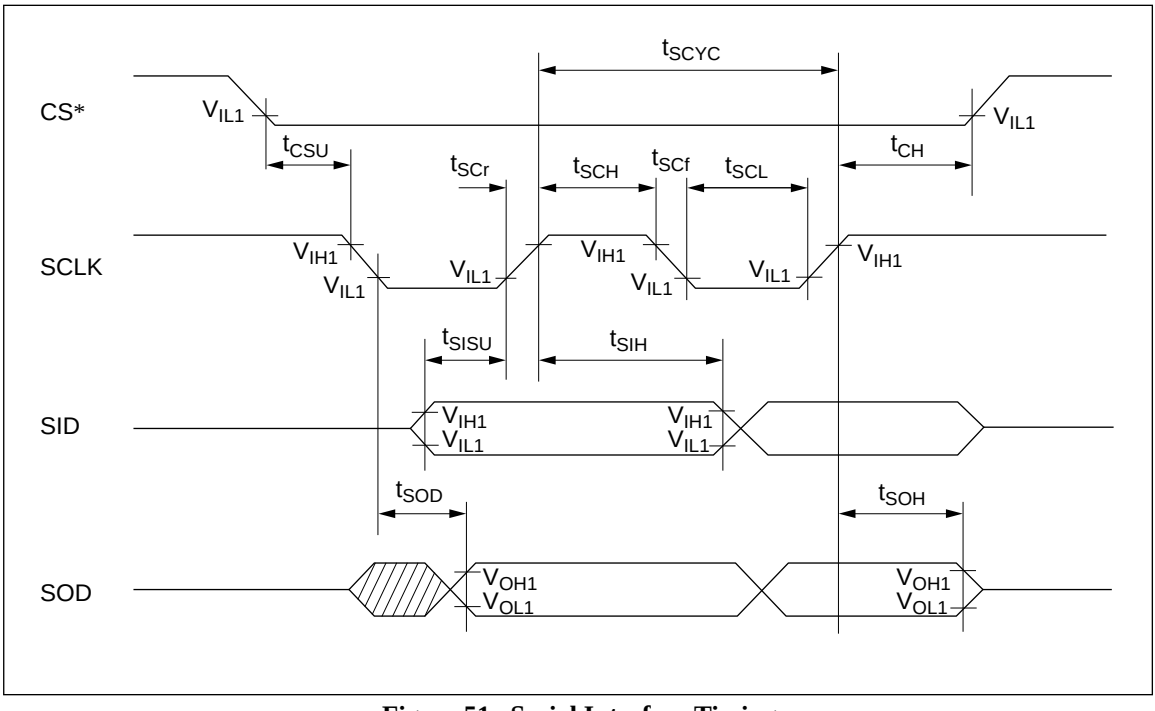


Figure 51 Serial Interface Timing

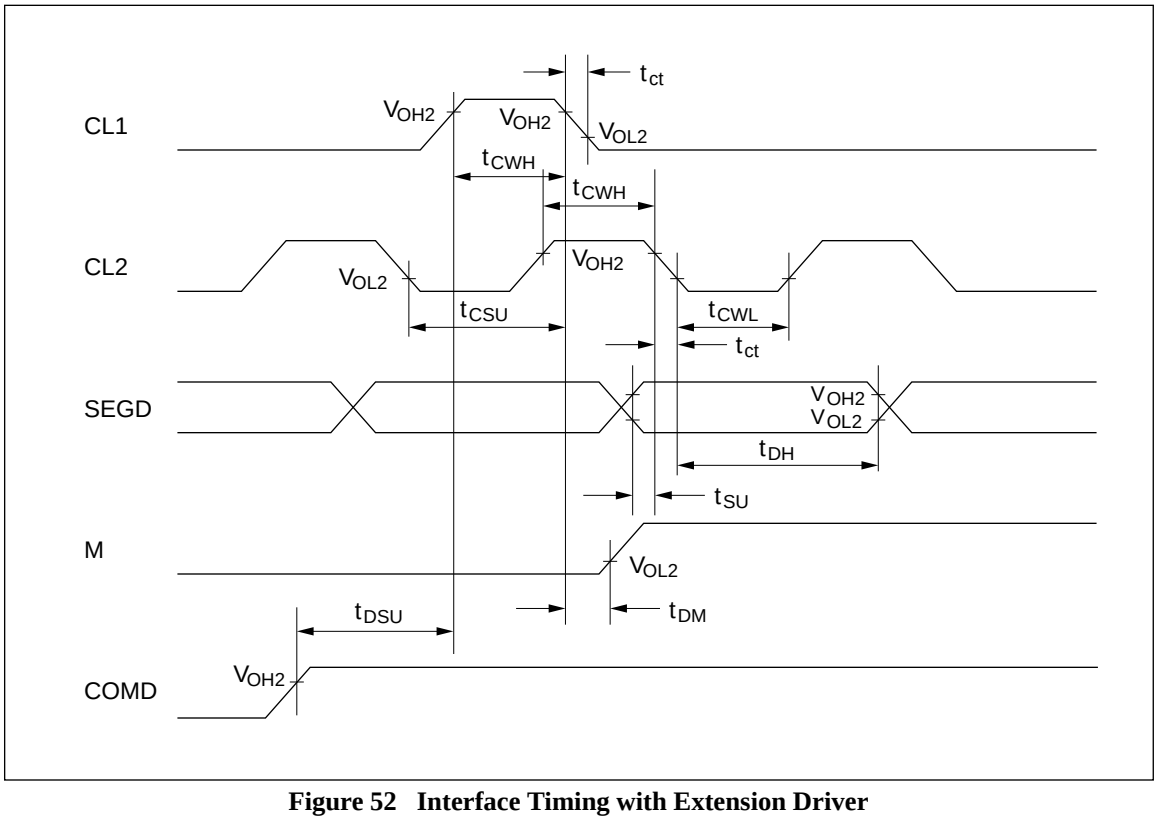
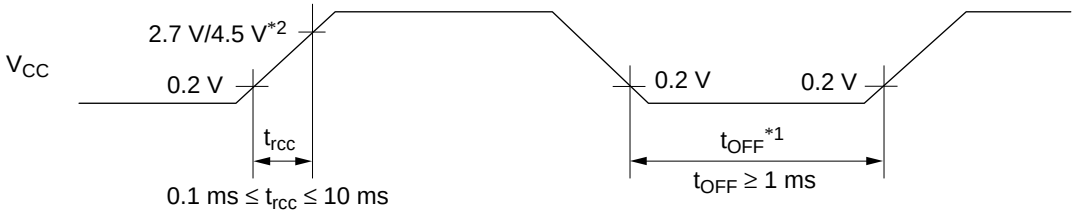


Figure 52 Interface Timing with Extension Driver

Figure 53 Reset Timing



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.

Figure 54 Power Supply Sequemce

HD44102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

HITACHI

Description

The HD44102 is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit microcomputer in the internal display RAM and generating dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of each dot of a liquid crystal display to provide more flexible than character display.

The HD44102 is produced by the CMOS process. Therefore, the combination of HD44102 with a CMOS microcontroller can complete portable battery-driven unit utilizing the liquid crystal display's low power dissipation.

The combination of HD44102 with the row (common) driver HD44103 facilitates dot matrix liquid crystal graphic display system configuration.

Features

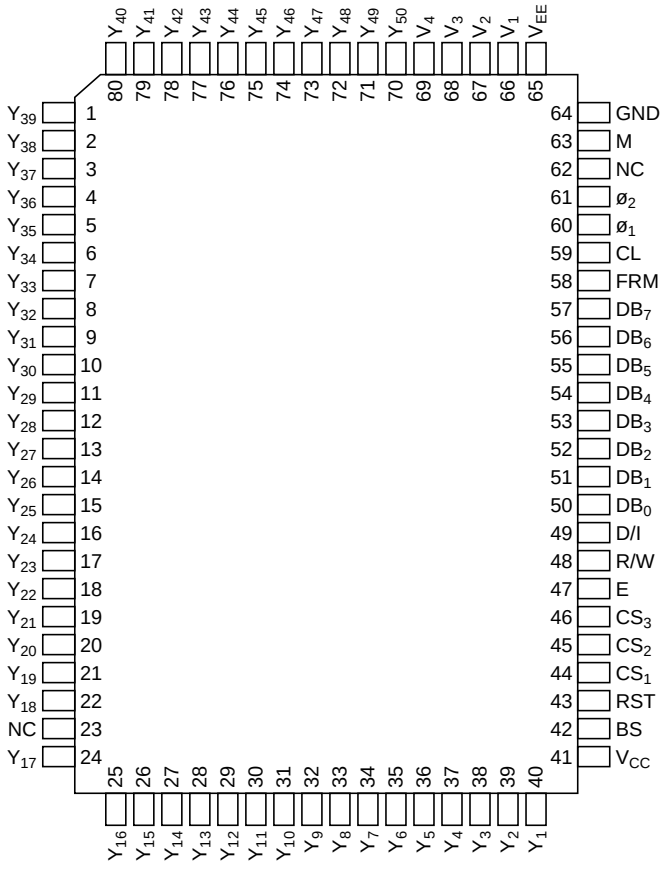
- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- Interfaces with 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  - — RAM bit data 1: On
  - — RAM bit data 0: Off
- Display RAM capacity: $50 \times 8 \times 4$ (1600 bits)
- Internal liquid crystal display driver circuit (segment output): 50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  - — Selectable duty factors: 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  - — Display data read/write, display on/off, set address, set display
  - — Start page, set up/down, read status
- Low power dissipation
- Power supplies:
  - — V_{CC} = 5V ± 10%
  - — V_{EE} = 0 to –5 V
- CMOS process

Ordering Information

Type No.	Package
HD44102CH	80-pin plastic QFP (FP-80)
HD44102D	Chip

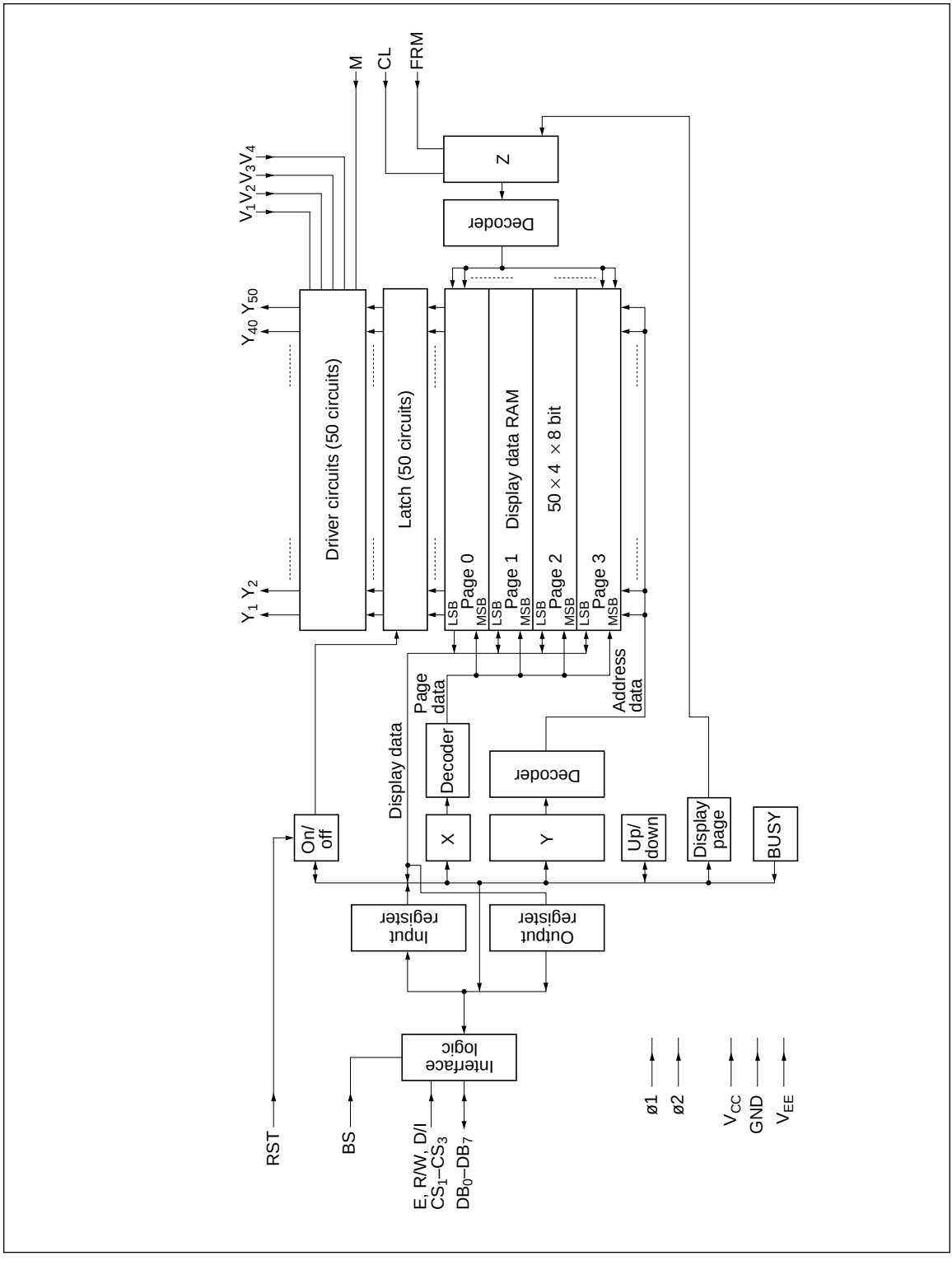
Hitachi semiconductor

Pin Arrangement

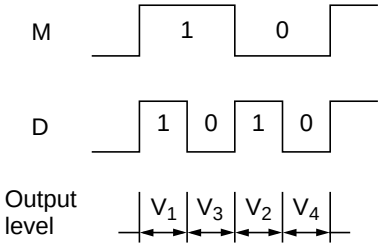


(Top view)

Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Function
Y1–Y50	50	O	Liquid crystal display drive output. Relationship among output level, M and display data (D): 
CS1–CS3	3	I	Chip select CS1 CS2 CS3 State L L L Non-selected L L H Non-selected L H L Non-selected L H H Selected read/write enable H L L Selected write enable only H L H Selected write enable only H H L Selected write enable only H H H Selected read/write enable
E	1	I	Enable • At write (R/W = Low) Data of DB0 to DB7 is latched at the fall of E. • At read (R/W = High) Data appears at DB0 to DB7 while E is at high level.
R/W	1	1	Read/write • R/W = High Data appears at DB0 to DB7 and can be read by the CPU when E = high and CS2, CS3 = high. • R/W = Low DB0 to DB7 can accept input when CS2, CS3 = high or CS1 = high.
D/I	1	I	Data/instruction • D/I = High Indicates that the data of DB0 to DB7 is display data. • D/I = Low Indicates that the data of DB0 to DB7 is display control data.

<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>I/O</th><th>Function</th></tr>
<tr><td>DB0–DB7</td><td>8</td><td>I/O</td><td>Data bus, three-state I/O common terminal
<table>
<tr><th>E</th><th>R/W</th><th>CS1</th><th>CS2</th><th>CS3</th><th>State of DB0 to DB7</th></tr>
<tr><td>H</td><td>H</td><td>*</td><td>H</td><td>H</td><td>Output state</td></tr>
<tr><td>*</td><td>L</td><td>H</td><td>*</td><td>*</td><td rowspan="2">Input state, high impedance</td></tr>
<tr><td>*</td><td>L</td><td>*</td><td>H</td><td>H</td></tr>
<tr><td colspan="5">Others</td><td>High impedance</td></tr>
</table></td></tr>
<tr><td>M</td><td>1</td><td>I</td><td>Signal to convert liquid crystal display drive output to AC.</td></tr>
<tr><td>CL</td><td>1</td><td>I</td><td>Display synchronous signal
At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.</td></tr>
<tr><td>FRM</td><td>1</td><td>I</td><td>Display synchronous signal (frame signal)
This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.</td></tr>
<tr><td>ø1, ø2</td><td>2</td><td>I</td><td>2-phase clock signal for internal operation
The ø1 and ø2 clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.</td></tr>
<tr><td>RST</td><td>1</td><td>I</td><td>Reset signal
The display disappears and Y address counter is set in the up counter state by setting the RST signal to low level. After releasing reset, the display off state and up mode is held until the state is changed by the instruction.</td></tr>
<tr><td>BS</td><td>1</td><td>I</td><td>Bus select signal
• BS = Low
DB0 to DB7 operate for 8-bit length.
• BS = High
DB4 to DB7 are valid for 4-bit length only.
8-bit data is accessed twice in the high and low order.</td></tr>
<tr><td>V1, V2, V3, V4</td><td>4</td><td></td><td>Power supply for liquid crystal display drive
V1 and V2: Selected level
V3 and V4: Non-selected level</td></tr>
<tr><td>V_{CC}
GND
V_{EE}</td><td>3</td><td></td><td>Power supply
V_{CC}–GND: Power supply for internal logic
V_{CC}–V_{EE}: Power supply for liquid crystal display drive circuit logic</td></tr>
</table>

Function of Each Block

Interface Logic

The HD44102 can use the data bus in 4-bit or 8-bit word length to enable interface to a 4-bit or 8-bit CPU.

1. 4 bit mode (BS = High)

   8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high.

   The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) are transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).

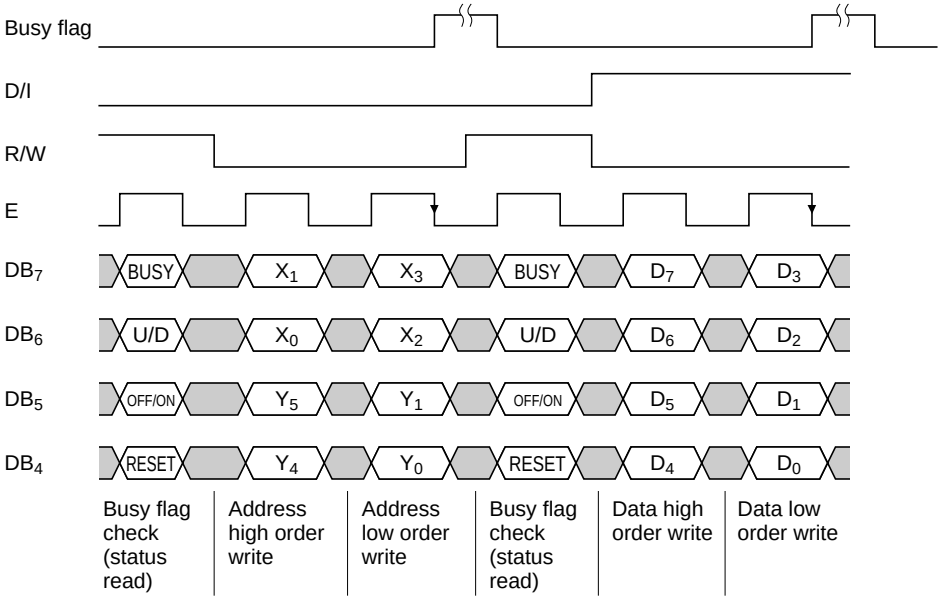
2. 8-bit mode (BS= Low)

   If the BS signal is low, the 8 data bus lines (DB0 to DB7) are used for data transfer.

   DB7: MSB (most significant bit)

   DB0: LSB (least significant bit)

For AC timing, refer to note 12 to note 15 of "Electrical Characteristics."



Note: Execute instructions other than status read in 4-bit length each. The busy flag is set at the fall of the second E signal. The status read is executed once. After the execution of the status read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

Figure 1 4-Bit Mode Timing

Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of the E signal when the CS is in the select state and R/W is in write state.

Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data (figure 2).

X, Y Address Counter

The X, Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit up/down counter. The address is increased or decreased by 1 by the read/write operation of display data. The up/down mode can be determined by the instruction or RST signal. The Y address register counts by looping the values of 0 to 49. The X address register has no count function.

Display On/Off Flip/Flop

This flip/flop is set to on/off state by the instruction or RST signal. In the off state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the on state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display on/off.

Up/Down Flip/Flop

This flip/flop determines the count mode of the Y address counter. In the up mode, the Y address register is increased by 1. 0 follows 49. In the down mode, the register is decreased by 1. 0 is followed by 49.

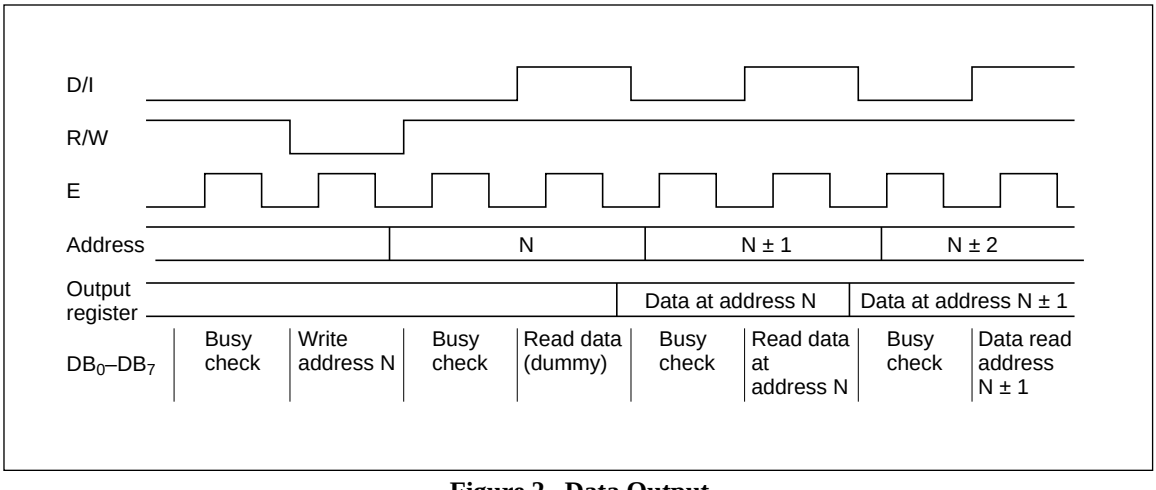


Figure 2 Data Output

Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

Busy Flag

After an instruction other than status read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective (figure 3). The value can be read out on DB7 by the status read instruction.

The HD44102 cannot accept any other instructions than the status read in the busy state. Make sure the busy flag is reset before issuing an instruction.

Z Address Counter

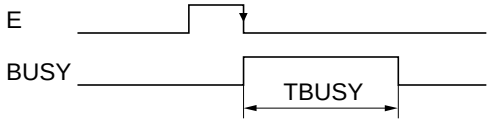
The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputting the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

Latch

The display data from the display data RAM is latched at the rise of CL signal.

Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of display data from latches and the M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.



$$\frac{1}{F\phi} \leq TBUSY \leq \frac{3}{F\phi}$$

Fø is ø1, ø2 frequency (half of HD44103 oscillation frequency)

Figure 3 Busy Flag

Display RAM

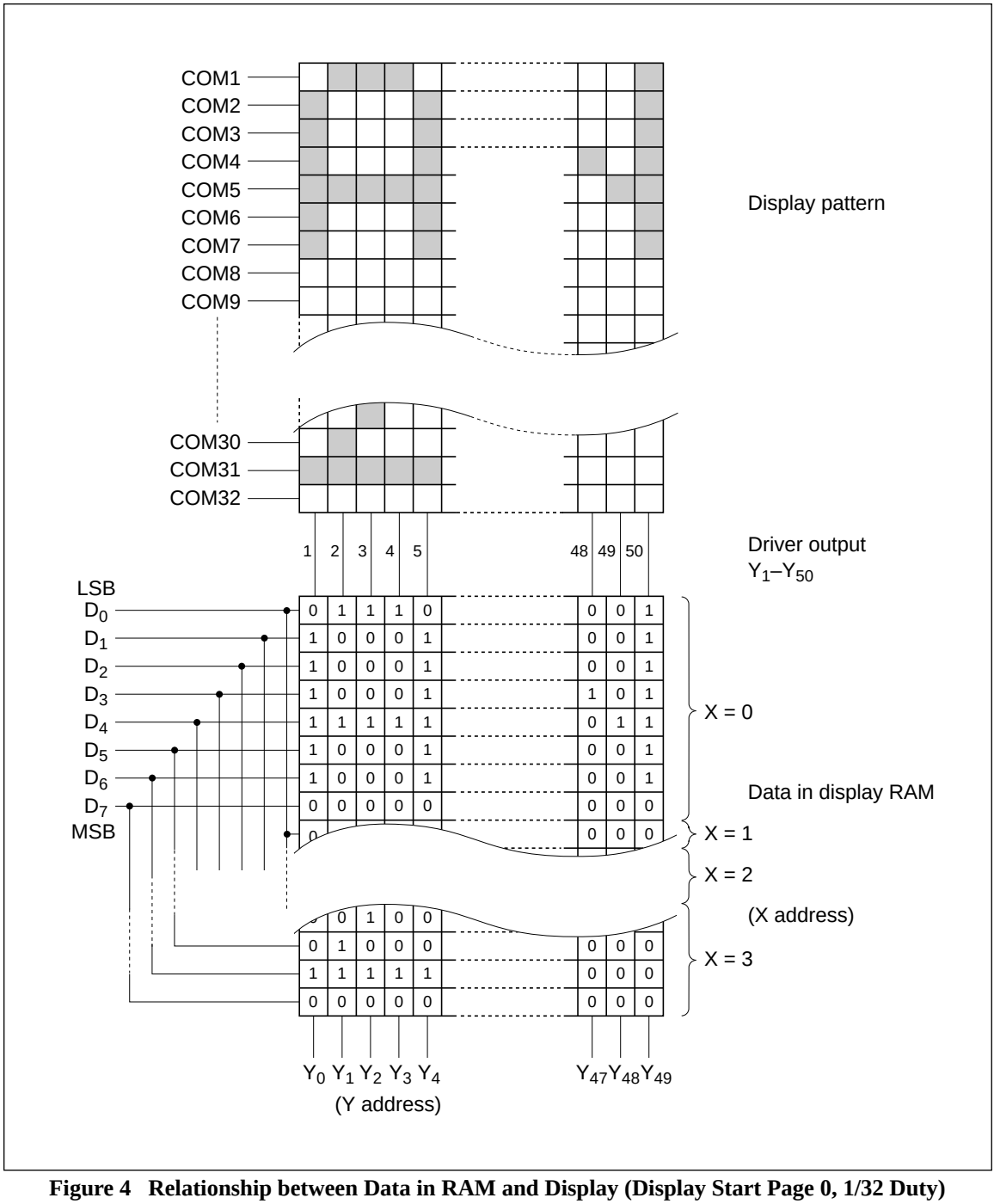


Figure 4 Relationship between Data in RAM and Display (Display Start Page 0, 1/32 Duty)

Display Control Instructions

Read/Write Display Data

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
1	1				(Display data)					
					Read (CPU ← HD44102)					
0	1				(Display data)					
					Write (CPU → HD44102)					

Sends or receives data to or from the address of the display RAM specified in advance. However, a dummy read may be required for reading display data. Refer to the description of the output register in Function of Each Block.

Display On/Off

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	0	1	Display on
0	0	0	0	1	1	1	0	0	0	Display off

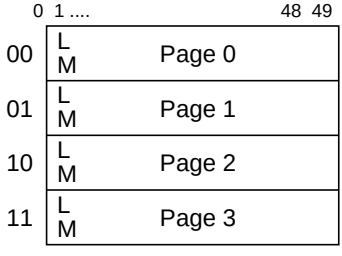
Turns the display on/off. RAM data is not affected.

Set X/Y Address

		MSB		DB					LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0							
0	0	0	1							Binary numbers of 0–49
0	0	1	0							
0	0	1	1							

X address (page) — Y address (address)

Y address



Display Data RAM

Display Start Page

		MSB		DB					LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	1	1	0	
		.....								Refer to figure 5 (a)
0	0	0	1	1	1	1	1	1	0	
		.....								Refer to figure 5 (b)
0	0	1	0	1	1	1	1	1	0	
		.....								Refer to figure 5 (c)
0	0	1	1	1	1	1	1	1	0	

Display start page

..... Refer to figure 5 (d)

Specifies the RAM page displayed at the top of the screen. Display is as shown in figure 4. When the display duty factor is more than 1/32 (for example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

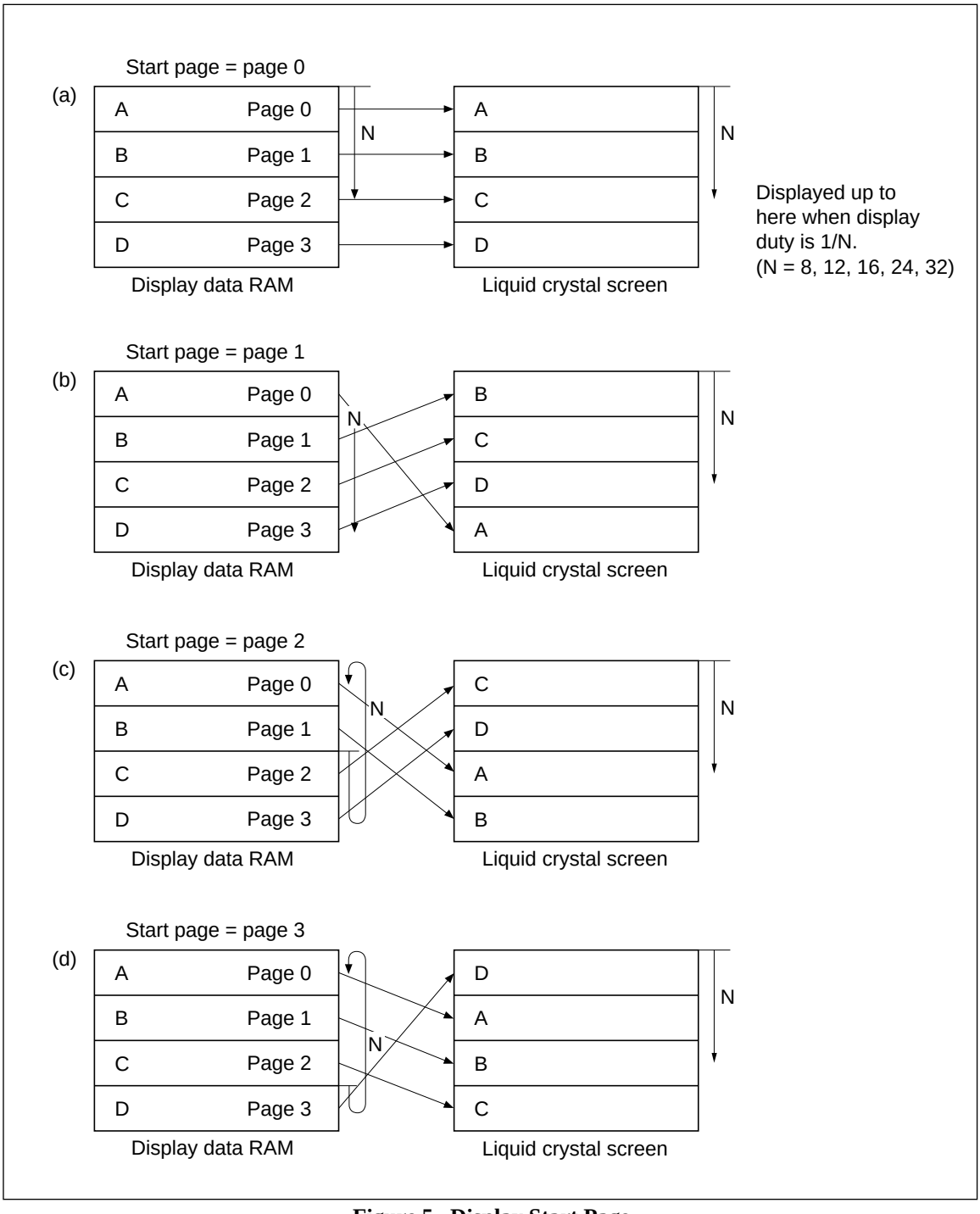


Figure 5 Display Start Page

Up/Down Set

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	1	1	Up mode
0	0	0	0	1	1	1	0	1	0	Down mode

Sets Y address register in the up/down counter mode.

Status Read

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0

- RESET: Goes to 1 when RST is in the reset state (busy also goes to 1).
  Goes to 0 when RST is in the operating state.
- OFF/ON: Goes to 1 in the display off state.
  Goes to 0 on the display on state.
- UP/DOWN: Goes to 1 when address counter is in the up mode.
  Goes to 0 when address counter is in the down mode.
- BUSY: Goes to 1 while all other instructions are being executed.
  While 1, none of the other instructions are accepted.

Connection between LCD Drivers (Example of 1/32 Duty Factor)

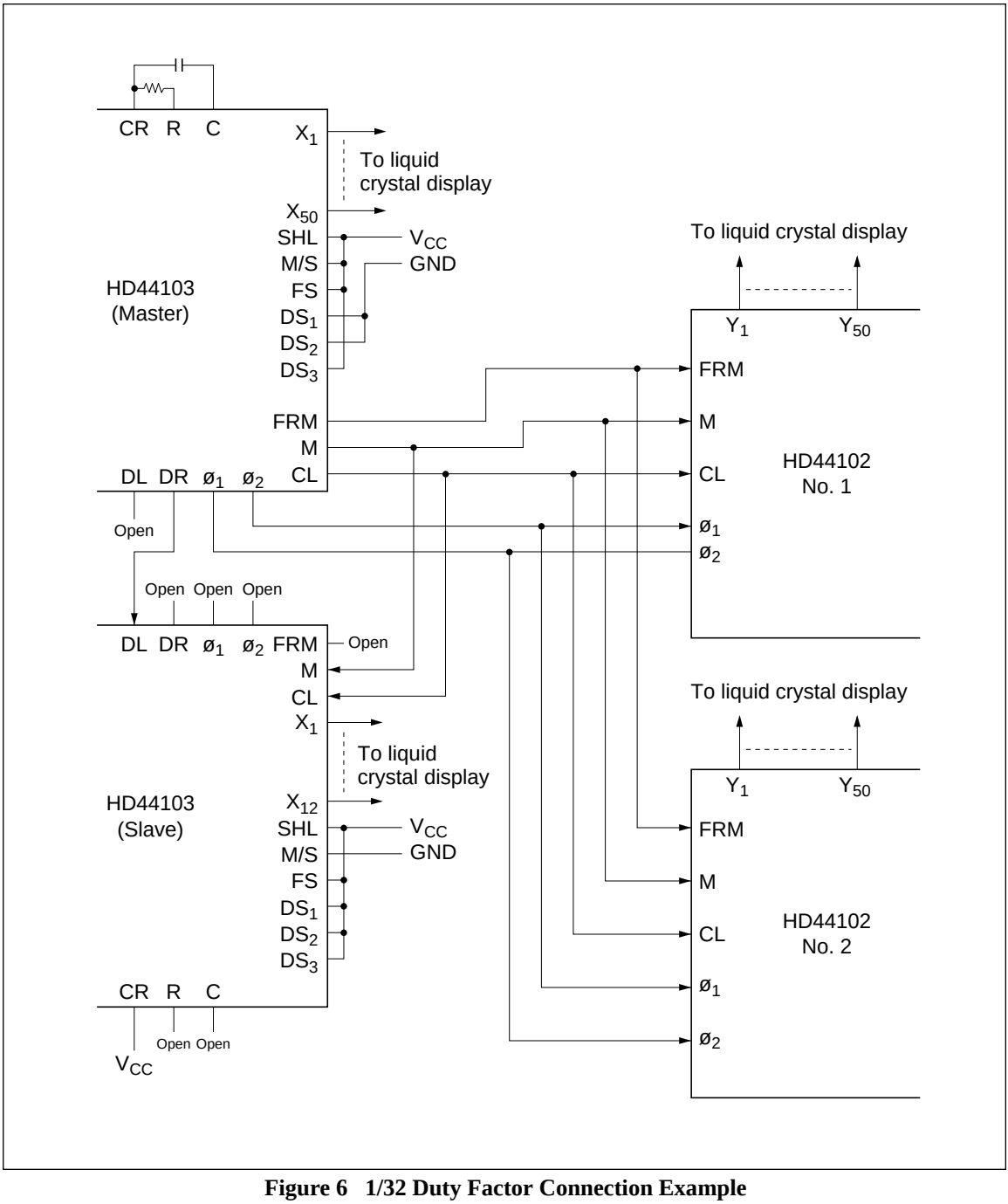


Figure 6 1/32 Duty Factor Connection Example

Interface to MPU

1. Example of Connection to HD6800

In the decoder given in this example, the addresses of HD44102 in the address space of HD6800 are:

Read/write of display data: $'FFFF'
Write of display instruction: $'FFFE'
Read of status: $'FFFE'

Thus, the HD44102 can be controlled by reading/ writing data at these addresses.

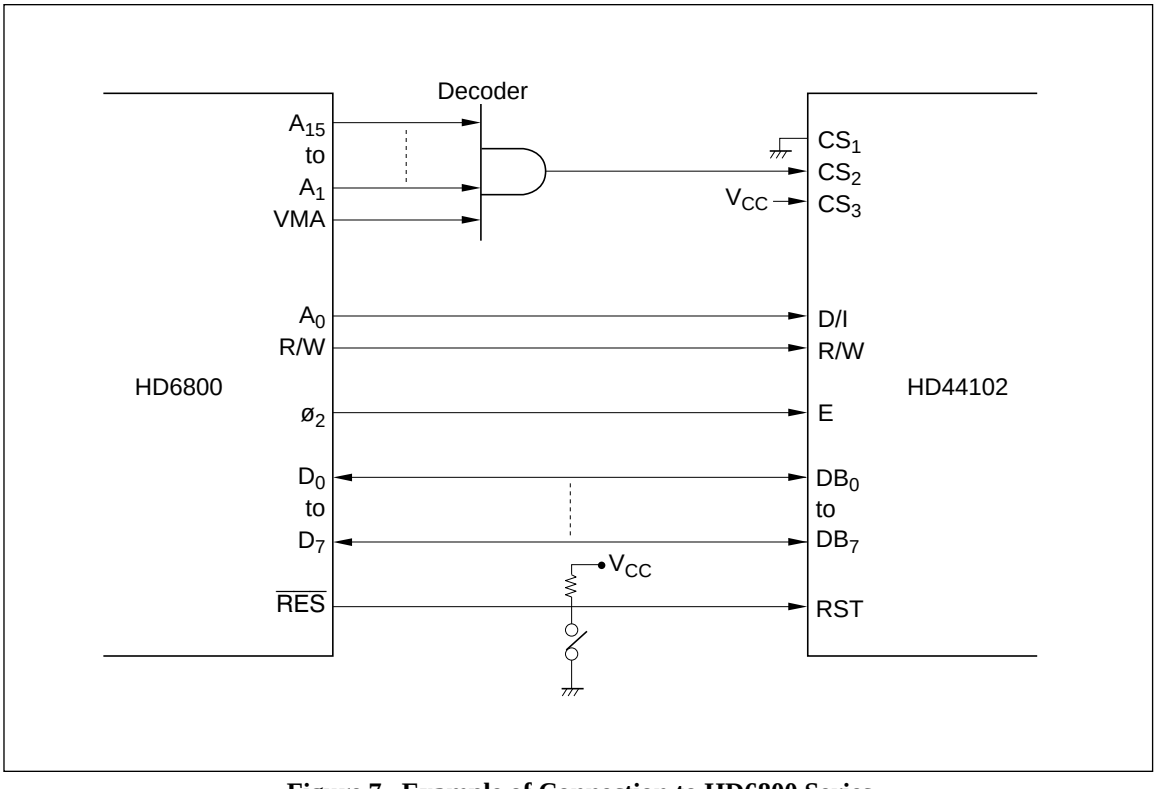


Figure 7 Example of Connection to HD6800 Series

2. Example of Connection to HD6801

- The HD6801 is set to mode 5. P10–P14 are used as output ports, and P30–P37 are used as the data bus.
- The 74LS154 is a 4-to-16 decoder that decodes 4 bits of P10–P13 to select the chips.
- Therefore, the HD44102 can be controlled by selecting the chips through P10–P13 and specifying the D/I signal through P14 in advance, and later conducting memory read or write for external memory space $0100 to $01FF of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to their manuals.

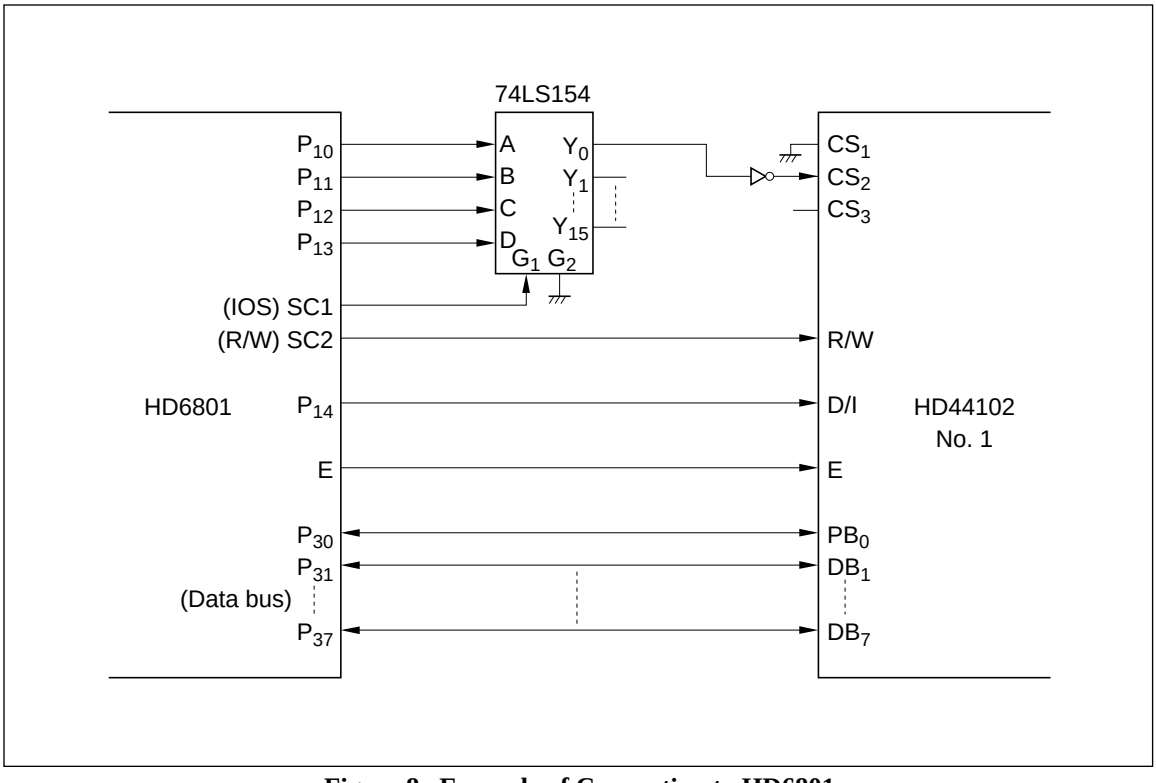


Figure 8 Example of Connection to HD6801

Connection to Liquid Crystal Display

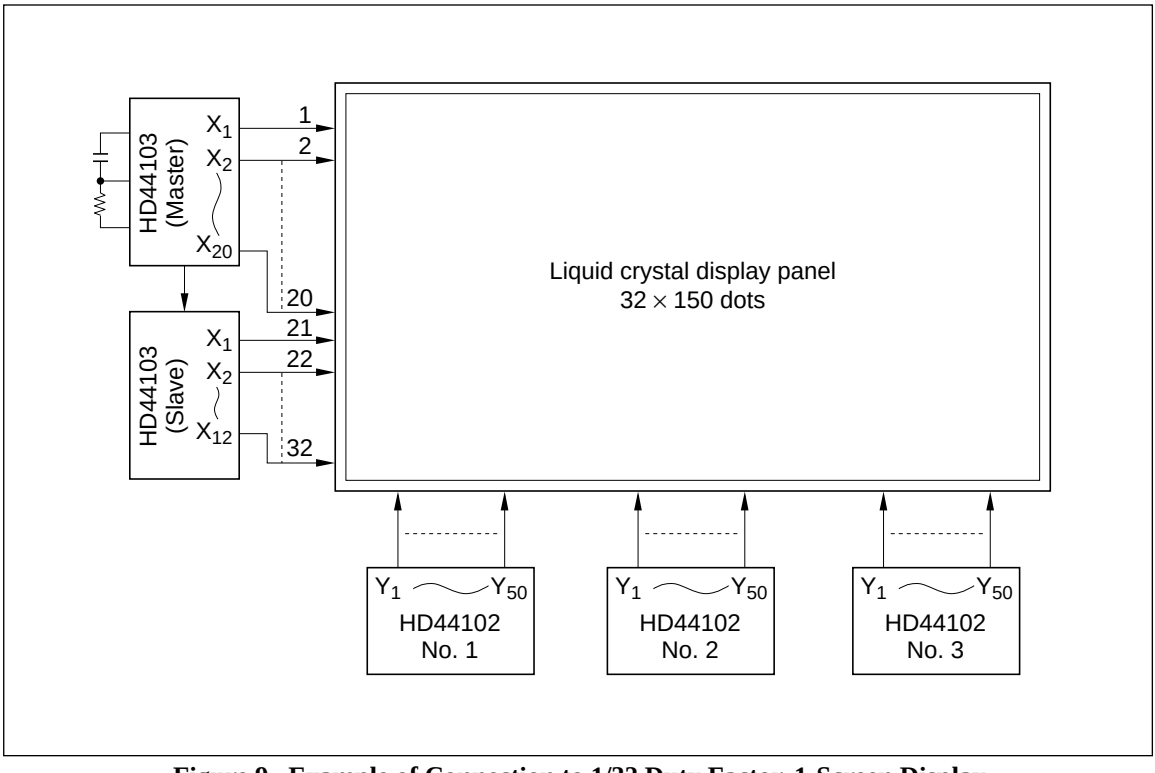


Figure 9 Example of Connection to 1/32 Duty Factor, 1-Screen Display

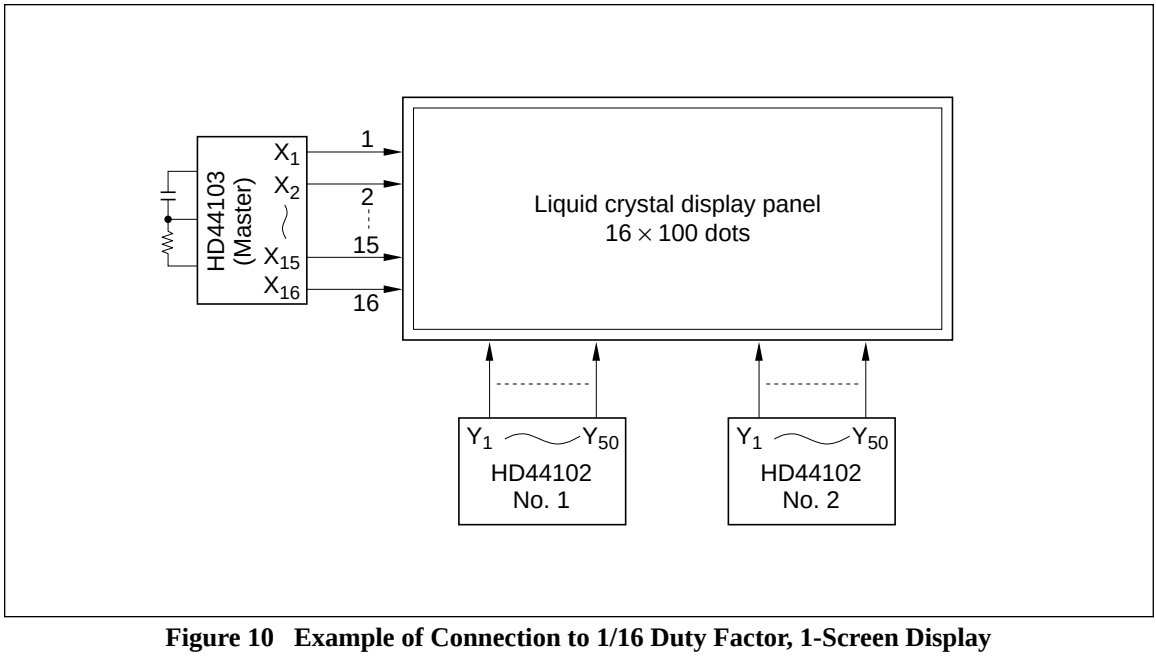


Figure 10 Example of Connection to 1/16 Duty Factor, 1-Screen Display

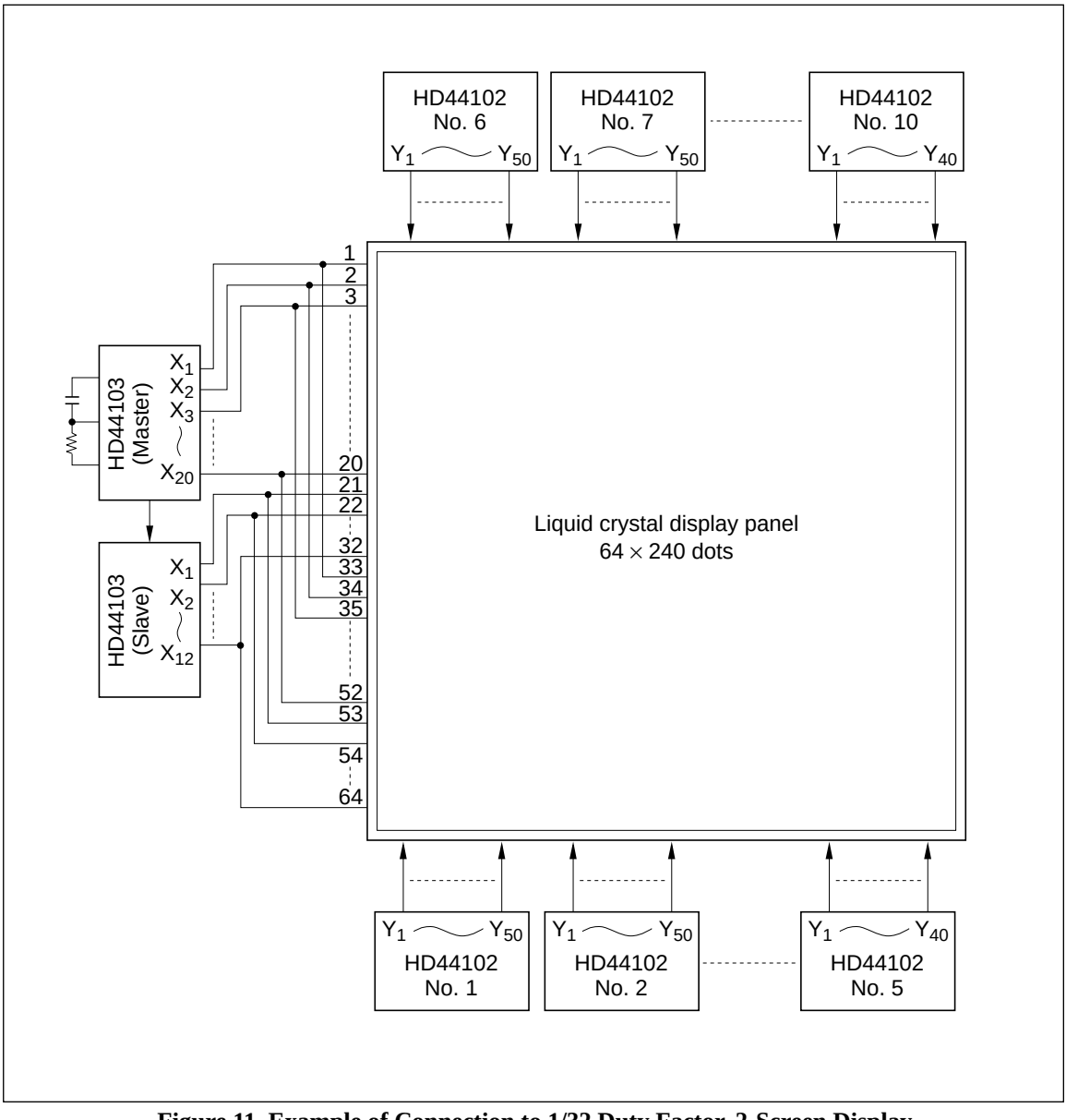


Figure 11 Example of Connection to 1/32 Duty Factor, 2-Screen Display

Limitations on Using 4-Bit Interface Function

The HD44102 usually transfers display control data and display data via 8-bit data bus. It also has the 4-bit interface function in which the HD44102 transfers 8-bit data by dividing it into the high-order 4 bits and the low-order 4-bits in order to reduce the number of wires to be connected. You should take an extra care in using the application with the 4-bit interface function since it has the following limitations.

Limitations

The HD44102 is designed to transfer the high-order 4-bits and the low-order 4-bits of data in that order after busy check. The LSI does not work normally if the signals are in the following state for the time period (indicated with (*) in figure 11) from when the high-order 4 bits are written (or read) to when the low-order 4 bits are written (or read); R/W = high and D/I = low while the chip is being selected (CS1 = high and CS2 = CS3 = don't care, or CS1 = low and CS2 = CS3 = high).

If the signals are in the limited state mentioned before for the time period indicated with (*) the LSI does not work normally. Please do not make the signals indicated with dotted lines simultaneously. As far as the time period indicated with (**), there is no problem.

The following explains how the malfunction is caused and gives the measures in application.

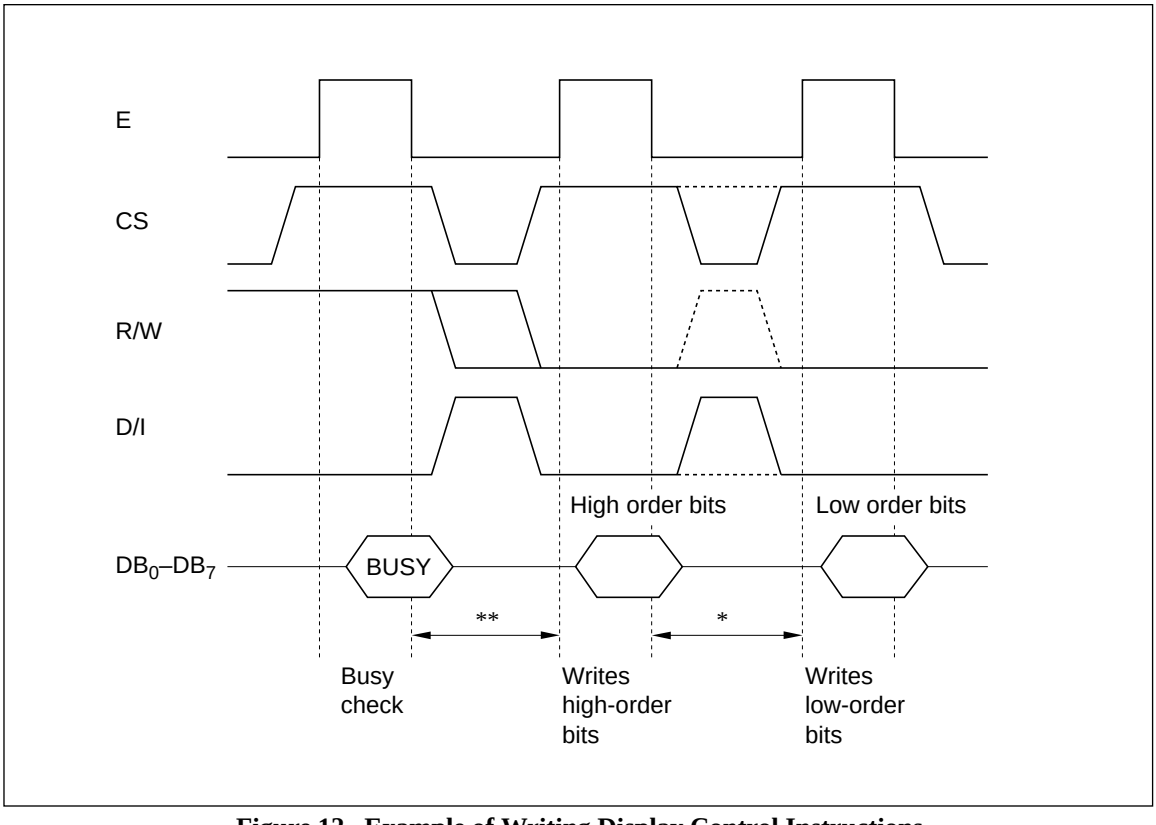


Figure 12 Example of Writing Display Control Instructions

Cause

Busy check checks if the LSI is ready to accept the next instruction or display data by reading the status register to the HD44102. And at the same time, it resets the internal counter counting the order of high-order data and low-order data. This function makes the LSI ready to accept only the high-order data after busy check. Strictly speaking, if R/W = high and D/I = low while the chip is being selected, the internal counter is reset and the LSI gets ready to accept high-order bits. Therefore, the LSI takes low-order data for high-order data if the state mentioned above exist in the interval between transferring high-order data and transferring low-order data.

Measures in Application

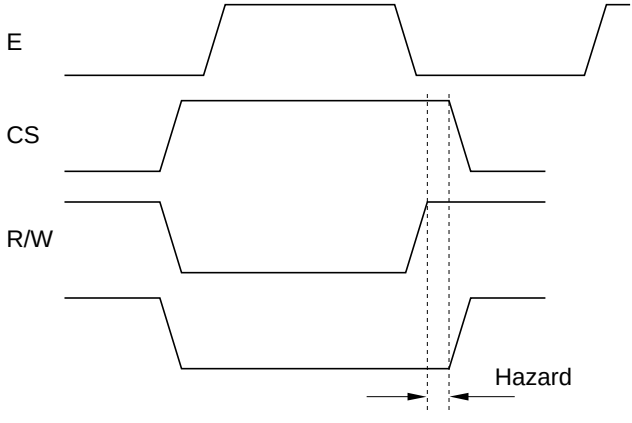
1. HD44102 controlled via port

   When you control the HD44102 with the port of a single-chip microcomputer, you should take care of the software and observe the limitations strictly.

2. HD44102 controlled via bus

   a. Malfunction caused by hazard

   Hazard of input signals may also cause the phenomenon mentioned before. The phase shift at transition of the input signals may cause the malfunction and so the AC characteristics must be carefully studied.

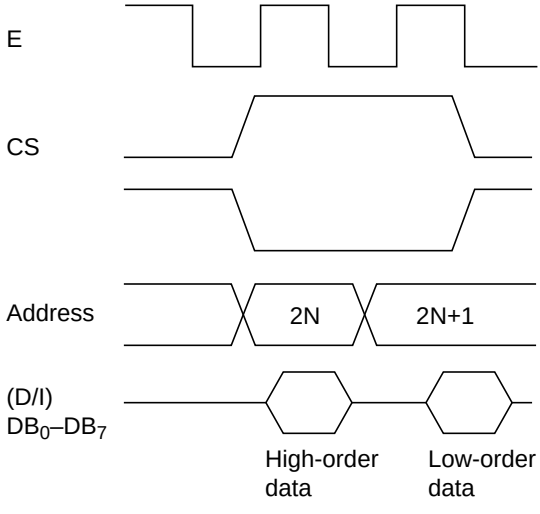


Example
Writing high-order data

Figure 13 Input Hazard

b. Using 2-byte instruction

In an application with the HD6303, you can prevent malfunction by using 2-byte instructions such as STD and STX. This is because the high-order and low-order data are accessed in that order without a break in the last machine cycle of the instruction and R/W and D/I do not change in the meantime. However, you cannot use the least significant bit of the address signals as the D/I signal since the address for the second byte has an added 1. Design the CS decoder so that the addresses for the HD44102 should be 2N and 2N + 1, and that those addresses should be accessed when using 2-byte instructions. For example, in figure 15 the address signal A_1 is used as D/I signal and A_2–A_{15} are used for the CS decoder. Addresses 4N and 4N+1 are for instruction access and addresses 4N + 2 and 4N + 3 are for display data access.



Last 2 machine cycles of 2-byte instruction

Figure 14 2-Byte Instruction

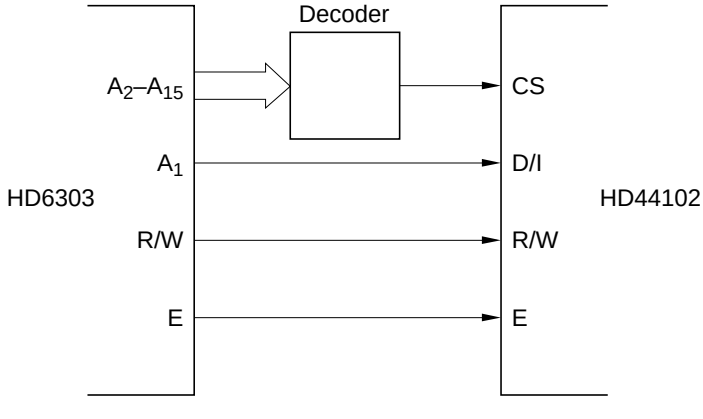


Figure 15 HD6303 Interface

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V3, and V4), and I/O common terminals.
3. Applied to terminals V1, V2, V3, and V4.

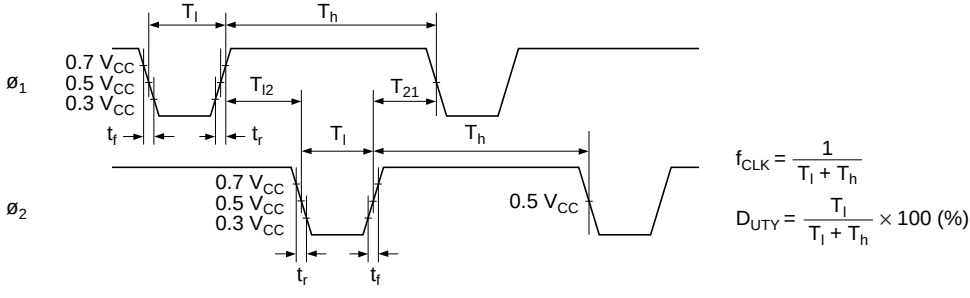
Electrical Characteristics (V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –6 V, Ta = –20 to 75°C)(Note 4)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage (CMOS)	V_{IHC}	0.7 × V_{CC}	—	V_{CC}	V		5
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 × V_{CC}	V		5
Input high voltage (TTL)	V_{IHT}	+2.0	—	V_{CC}	V		6
Input low voltage (TTL)	V_{ILT}	0	—	+0.8	V		6
Output high voltage	V_{OH}	+3.5	—	—	V	I_{OH} = –250 µA	7
Output low voltage	V_{OL}	—	—	+0.4	V	I_{OL} = +1.6 mA	7
Vi-Xj ON resistance	R_{ON}	—	—	7.5	kΩ	V_{EE} = –5 V ± 10%, load current 100 µA	
Input leakage current (1)	I_{IL1}	–1	—	+1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	–2	—	+2	µA	V_{IN} = V_{CC} to V_{EE}	9
Operating frequency	f_{CLK}	25	—	350	kHz	ø1, ø2 frequency	10
Dissipation current (1)	I_{CC1}	—	—	100	µA	f_{clk} = 200 kHz frame = 65 Hz during display	11
Dissipation current (2)	I_{CC2}	—	—	500	µA	Access cycle 1 MHz at access	12

Notes: 4. Specified within this range unless otherwise noted.
5. Applied to M, FRM, CL, BS, RST, ø1, ø2.
6. Applied to CS1 to CS3, E, D/I, R/W and DB0 to DB7.
7. Applied to DB0 to DB7.
8. Applied to input terminals, M, FRM, CL, BS, RST, ø1, ø2, CS1 to CS3, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.
9. Applied to V1, V2, V3, and V4.

10. ø1 and ø2 AC characteristics.

	Symbol	Min	Typ	Max	Unit
Duty factor	Duty	20	25	30	%
Fall time	t_f	—	—	100	ns
Rise time	t_r	—	—	100	ns
Phase difference time	t_{l2}	0.8	—	—	µs
Phase difference time	t_{21}	0.8	—	—	µs
$T_l + T_h$		—	—	40	µs

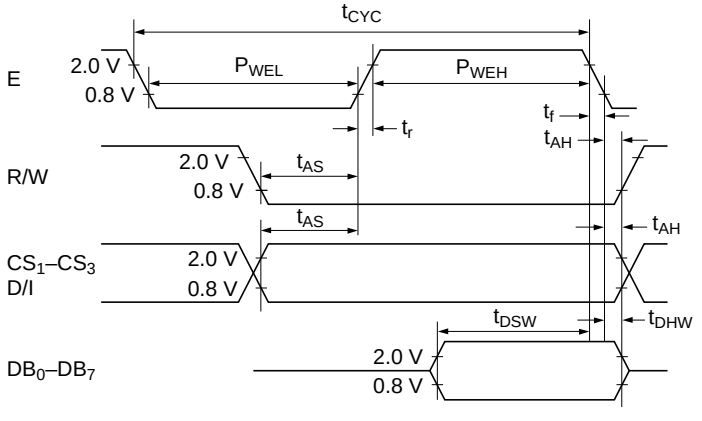


11. Measured by V_{CC} terminal at no output load, at 1/32 duty factor, an frame frequency of 65 Hz, in checker pattern display. Access from the CPU is stopped.
12. Measured by V_{CC} terminal at no output load, 1/32 duty factor and frame frequency of 65 Hz.

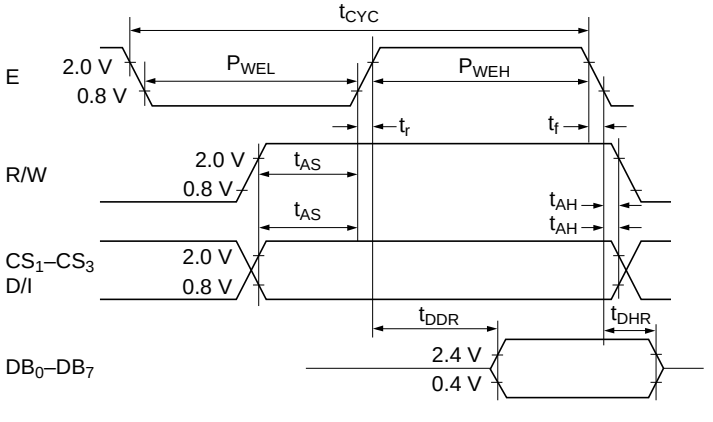
Interface AC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
C cycle time	t_{CYC}	1000	—	—	ns	13, 14
E high level width	P_{WEH}	450	—	—	ns	13, 14
E low level width	P_{WEL}	450	—	—	ns	13, 14
E rise time	t_r	—	—	25	ns	13, 14
E fall time	t_f	—	—	25	ns	13, 14
Address setup time	t_{AS}	140	—	—	ns	13, 14
Address hold time	t_{AH}	10	—	—	ns	13, 14
Data setup time	t_{DSW}	200	—	—	ns	13
Data delay time	t_{DDR}	—	—	320	ns	14, 15
Data hold time at write	t_{DHW}	10	—	—	ns	13
Data hold time at read	t_{DHR}	20	—	—	ns	14

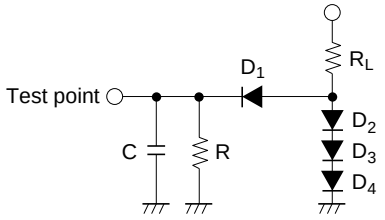
Notes: 13. At CPU write



14. At CPU read



15. DB0 to DB7 load circuits



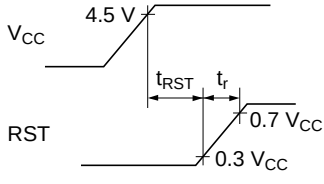
R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (including jig capacitance)
Diodes D_1 to D_4 are all 1S2074Ⓗ

16. Display off at initial power up.

The HD44102 can be placed in the display off state by setting terminal RST to low at initial power up.

No instruction other than the read status can be accepted while the RST is at the low level.

	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns



HD44103

(Dot Matrix Liquid Crystal Graphic Display
20-Channel Common Driver)

HITACHI

Description

The HD44103 is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duty ratio: 1/8, 1/12, 1/16, 1/24, and 1/32. 20 driver output lines are provided, and the impedance is low (500 Ω max.) to enable a large screen to be driven.

Features

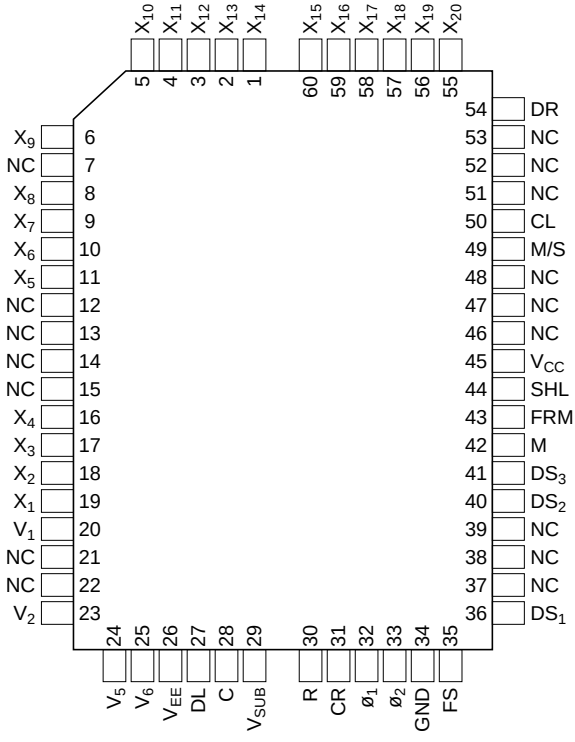
- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit
- Internal oscillator (oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies
  - — V_{CC}: 5 V ±10%
  - — V_{EE}: 0 to –5.5 V
- CMOS process

Ordering Information

Type No.	Package
HD44103CH	60-pin plastic QFP (FP-60)

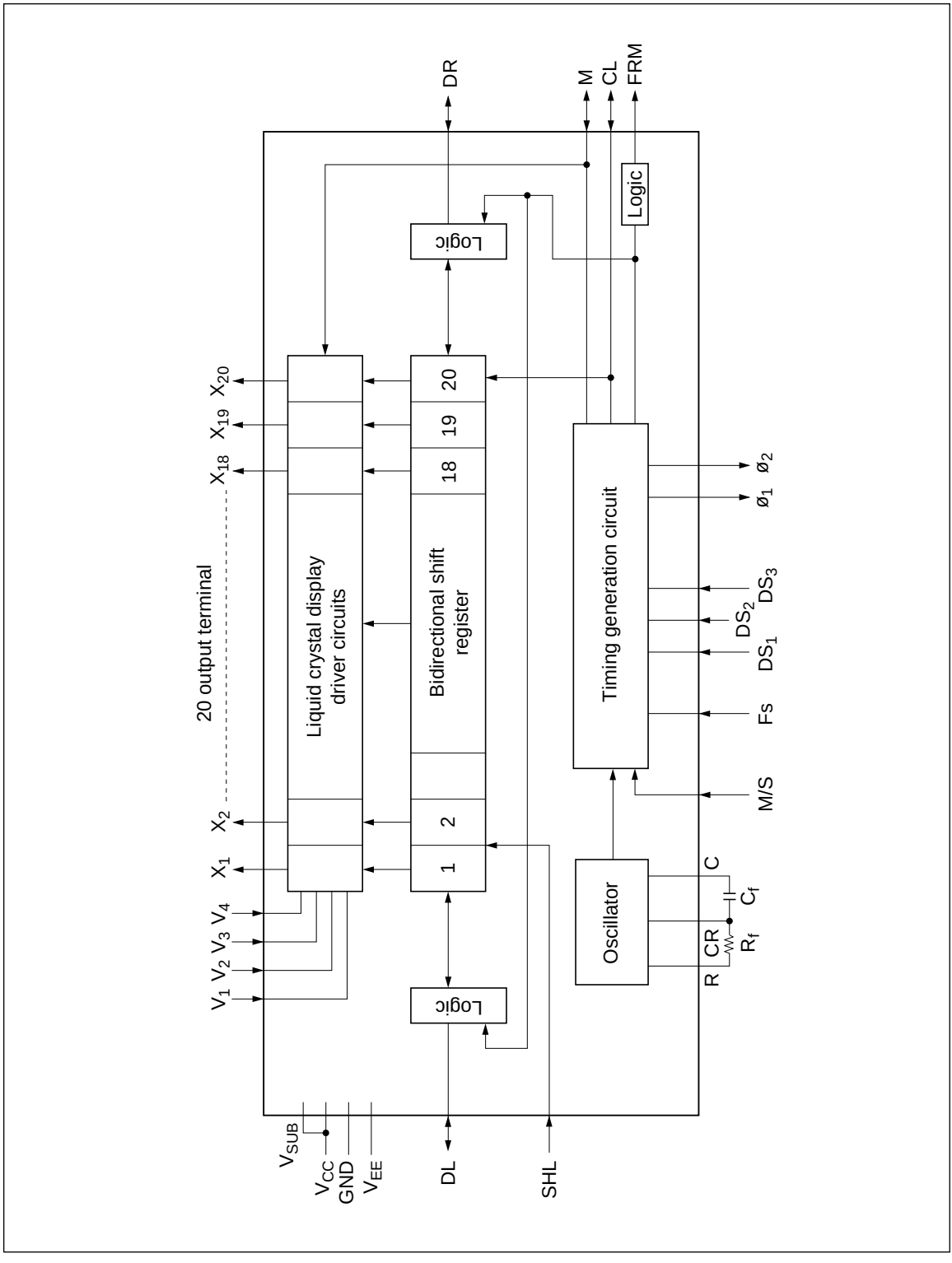
Hitachi semiconductor

Pin Arrangement

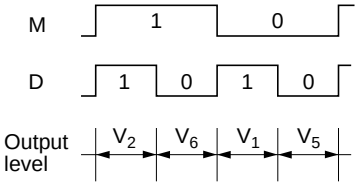
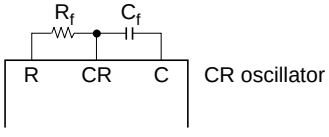


(Top view)

Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Function
X1–X20	20	O	Liquid crystal display driver output. Relationship among output level, M, and data (D) in shift register: 
CR, R, C	3		Oscillator 
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, display synchronous signal.
DS1–DS3	3	I	Display duty ratio select.

Display Duty Ratio	1/24	1/12		X	1/32	1/16		1/8
DS1	L	H	L	H	L	H	L	H
DS2	L	L	H	H	L	L	H	H
DS3	L	L	L	L	H	H	H	H

Pin Name	Pin Number	I/O	Function
FS	1	I	Frequency select. The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows: FS = High: $f_{OSC} = 6144 \times f_{FRM}$ (1) FS = Low: $f_{OSC} = 3072 \times f_{FRM}$ (2) Example (1) When FS = high, adjust Rf and Cf so that the oscillation frequency is approx. 430 kHz if the frame frequency is 70 Hz. Example (2) When FS = low, adjust Rf and Cf so that the oscillation is approx. 215 kHz, in order to obtain the same display waveforms as example 1. When compared with example 1, the power dissipation is reduced because of operation at lower frequency. However, the operating clocks ø1 and ø2 supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102 becomes longer.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Shift direction select of bidirectional shift register. **SHL** — **Shift Direction** H — DL → DR L — DL ← DR
M/S	1	I	Master/slave select. • M/S = High: Master mode The oscillator and timing generation circuit supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is placed in the output state. • M/S = Low: Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CI are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS, DS1, DS2, and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12, or 1/16, one HD44103 is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103s are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).

Pin Name	Pin Number	I/O	Function
ø1, ø2	2	O	Operating clock output terminals for HD44102. The frequencies of ø1 and ø2 become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for driver circuit logic

Block Functions

Oscillator

The oscillator is a CR oscillator attached to an oscillation resistor Rf and oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to Electrical Characteristics (note 11) to make proper adjustment.

Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ø1 and ø2) for HD44102 according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

20-bit bidirectional shift register. The shift direction is determined by SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 20 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Applications

Refer to the applications of the HD44102.

Absolute Maximum Ratings

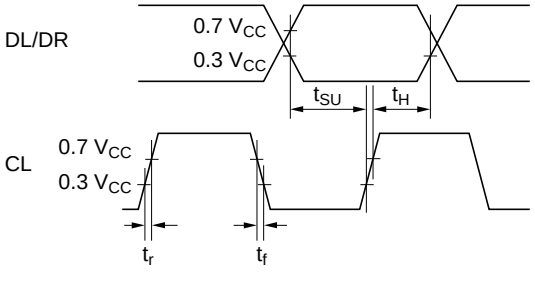
Item	Symbol	Rated Value	Unit	Notes
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} – 13.5 to V_{CC} + 0.3	V	4
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6.
4. Connect a protection resistor of 220 Ω ± 5% to V_{EE} power supply in series.

Electrical Characteristics (V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to +75°C)*5

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		2
Input low voltage	V_{IL}	0	—	0.3 × V_{CC}	V		2
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = +400 µA	3
Vi-Xj on resistance	R_{ON}	—	—	500	Ω	V_{EE} = –5 ± 10%, load current ±150 µA	
Input leakage current (1)	I_{IL1}	–1	—	1	µA	V_{IN} = V_{CC} to GND	4
Input leakage current (2)	I_{IL2}	–2	—	2	µA	V_{IN} = V_{CC} to V_{EE}	5
Shift frequency	f_{SFT}	—	—	50	kHz	In slave mode	6
Oscillation frequency	f_{OSC}	350	430	480	kHz	R_f = 68 kΩ ± 2% C_f = 10 pF ± 5%	7
External clock operating frequency	f_{cp}	50	—	500	kHz		
External clock duty	Duty	45	50	55	%		8
External clock rise time	t_{rcp}	—	—	50	ns		8
External clock fall time	t_{fcp}	—	—	50	ns		8
Dissipation power (master)	P_{w1}	—	—	5.5	mW	CR oscillation = 430 kHz	9
Dissipation power (slave)	P_{w2}	—	—	2.75	mW	Frame frequency = 70 Hz	10

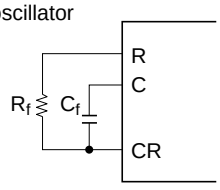
Notes: 1. Specified within this range unless otherwise noted.
2. Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR, and DL.
3. Applied to DL, DR, M, FRM, CL, ø1, and ø2.
4. Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M, and CL at high impedance.
5. Applied to V1, V2, V5, and V6.
6. Shift operation timing



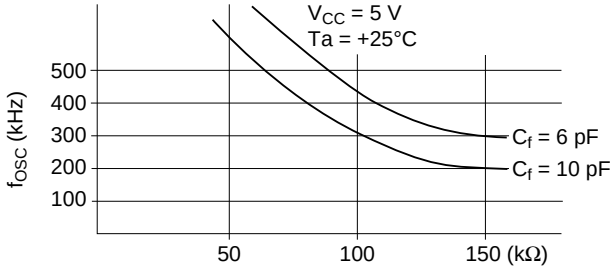
	Min	Typ	Max	Unit
t_{SU}	5	—	—	µs
t_H	5	—	—	µs
t_r	—	—	100	ns
t_f	—	—	100	ns

7. Relationship between oscillation frequency and R_f/C_f

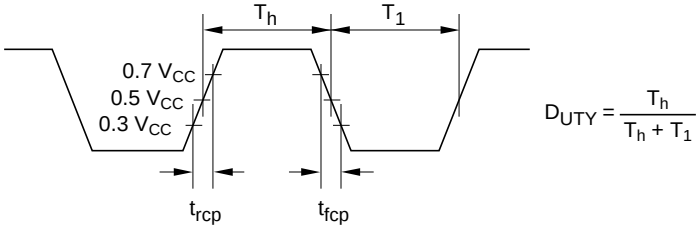
CR oscillator

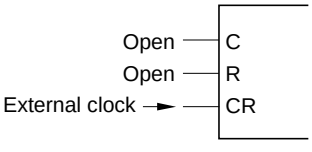


The values of R_f and C_f are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to the required value.



8.





9. Measured by V_{CC} terminal at output non-load of R_f = 68 kΩ ± 2% and C_f = 10 pF ± 5%, 1/32 duty factor in the master mode. Input terminals must be fixed at V_{CC} or GND while measuring.
10. Measured by V_{CC} terminal at output non-load, 1/32 duty factor, frame frequency of 70 Hz in the slave mode. Input terminals must be fixed at V_{CC} or GND while measuring.

HD44105

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

HITACHI

Description

The HD44105 is a common signal driver for LCD dot matrix graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty cycle.

It can select 7 types of display duty cycle 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, and 1/64. It provides 32 driver output lines and the impedance is low (1 kΩ max) enough to drive a large screen.

Features

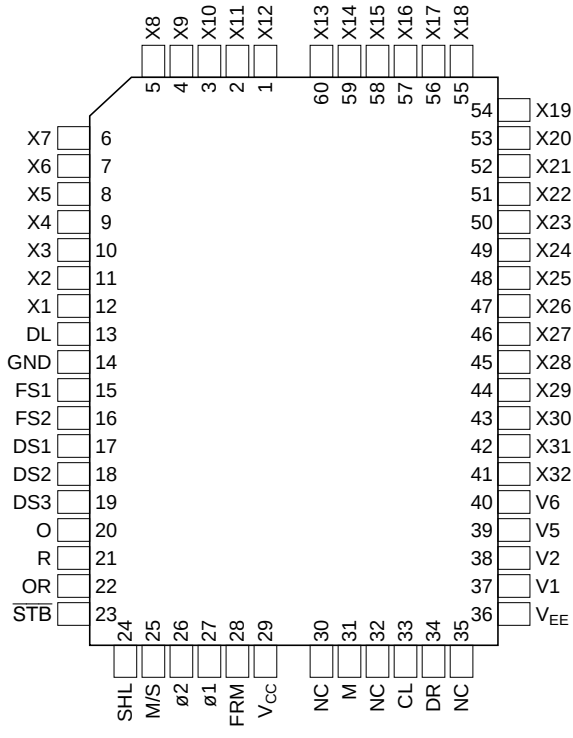
- Dot matrix graphic display common driver including the timing generation circuit
- Internal oscillator (oscillation frequency is selectable by attaching an oscillation resistor and an oscillation capacitor)
- Generates display timing signals
- 32-bit bidirectional shift register for generating common signals
- 32 liquid crystal driver circuits with low impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64
- Low power dissipation
- Power supplies:
  - — V_{CC} = +5 V ±10%
  - — V_{EE} = 0 to –5.5 V
- CMOS process

Ordering Information

Type No.	Package
HD44105H	60-pin plastic QFP (FP-60)
HD44105D	Chip

Hitachi semiconductor

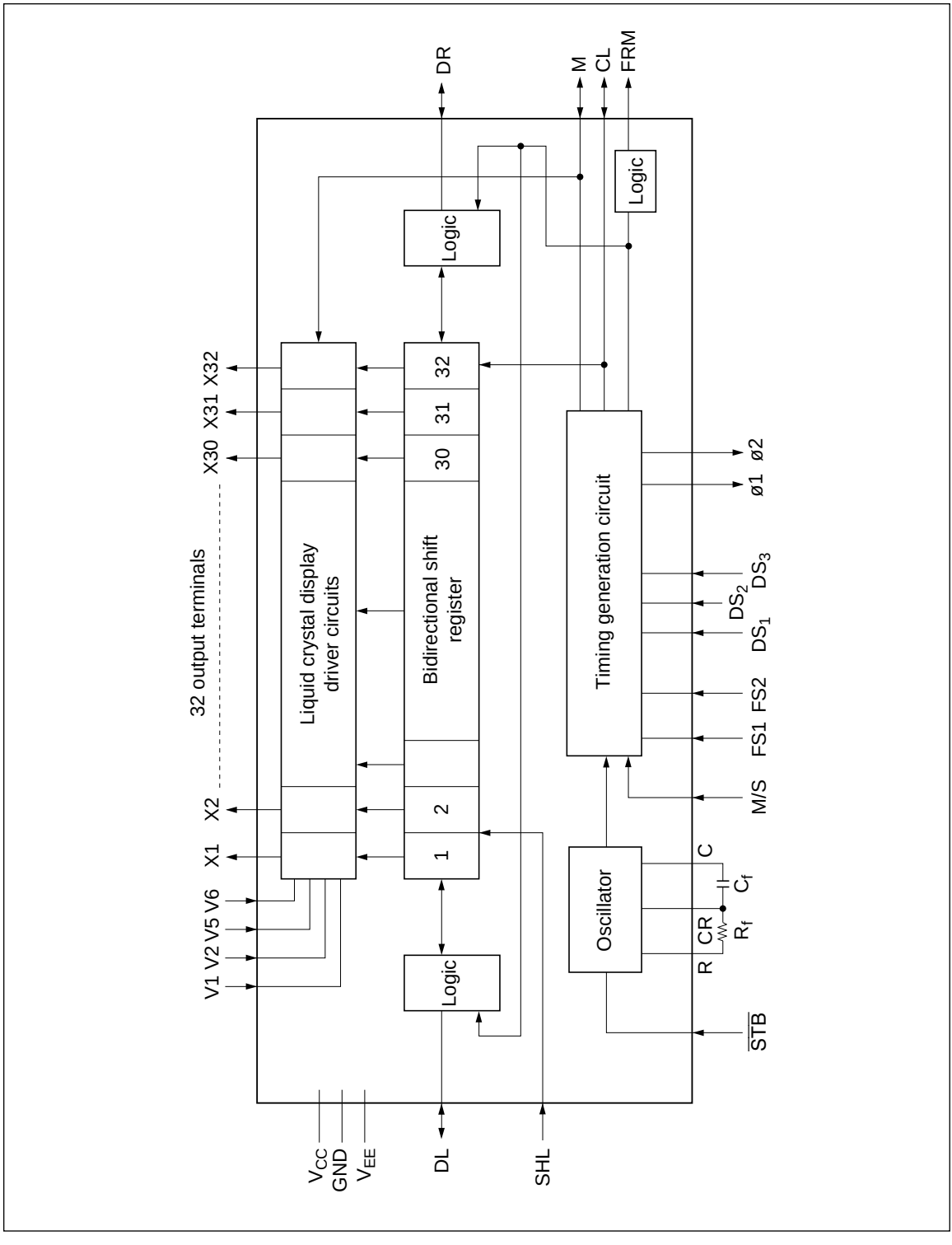
Pin Arrangement



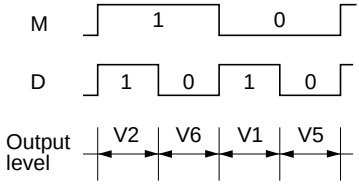
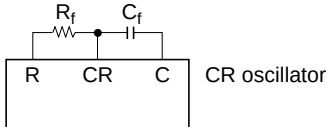
(Top view)

Note: NCs show unused terminals.
Don't connect any lines to them in using this LSI.

Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Function
X1–X32	32	O	Liquid crystal display driver output. Relation among output level, M, and data (d) in shift register. 
CR, R, C	3		Oscillator. 
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, display synchronous signal.
DS1–DS3	3	I	Display duty ratio select.

Display Duty Ratio	1/8	1/16	1/32	1/64	–	1/12	1/24	1/48
DS1	L	L	H	H	L	L	H	H
DS2	L	H	L	H	L	H	L	H
DS3	L	L	L	L	H	H	H	H

FS1–FS2 — 2 — 1

Selects frequency.

The relation between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:

FS1	FS2	f_{OSC} (kHz)	f_{FRM} (Hz)	f_M (Hz)	f_{CP} (kHz)
L	L	107.5	70	35	53.8
H	L	107.5	70	35	53.8
L	H	215.0	70	35	107.5
H	H	430.0	70	35	215.0

f_{OSC}: Oscillation frequency
f_{FRM}: Frame frequency
f_M: M signal frequency
f_{CP}: Frequencies of ø1 and ø2

Pin Name	Pin Number	I/O	Function
$\overline{STB}$	1	1	Input terminal for testing. Connect this terminal to V_{CC}.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Selects shift direction of bidirectional shift register. SHL — Shift Direction H — DL → DR L — DL ← DR
M/S	1	I	Selects Master/Slave. • M/S = High: Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is in the output state. • M/S = Low: Slave mode The timing generation circuit stop operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS1, FS2, DS1, DS2, DS3, $\overline{STB}$ to V_{CC}. When display duty ratio is 1/8, 1/12, 1/16, 1/24, 1/32, one HD44105 is required. Use it in the master mode. When display duty ratio is 1/48, 1/64, two HD44105s are required. Use one in the master mode to drive common signals 1 to 32, and another in the slave mode to drive common signals 33 to 48 (64).
ø1, ø2	2	O	Operating clock output terminals for HD44102. The frequencies of ø1 and ø2 are half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC}, GND V_{EE}	3		Power supply. V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for liquid crystal display drive circuit logic

Block Functions

Oscillator

The oscillator is a CR oscillator attached to an oscillation resistor Rf and an oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to electrical characteristics (note 10) to make proper adjustment.

Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ø1 and ø2) for HD44102 according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS1, FS2 and DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

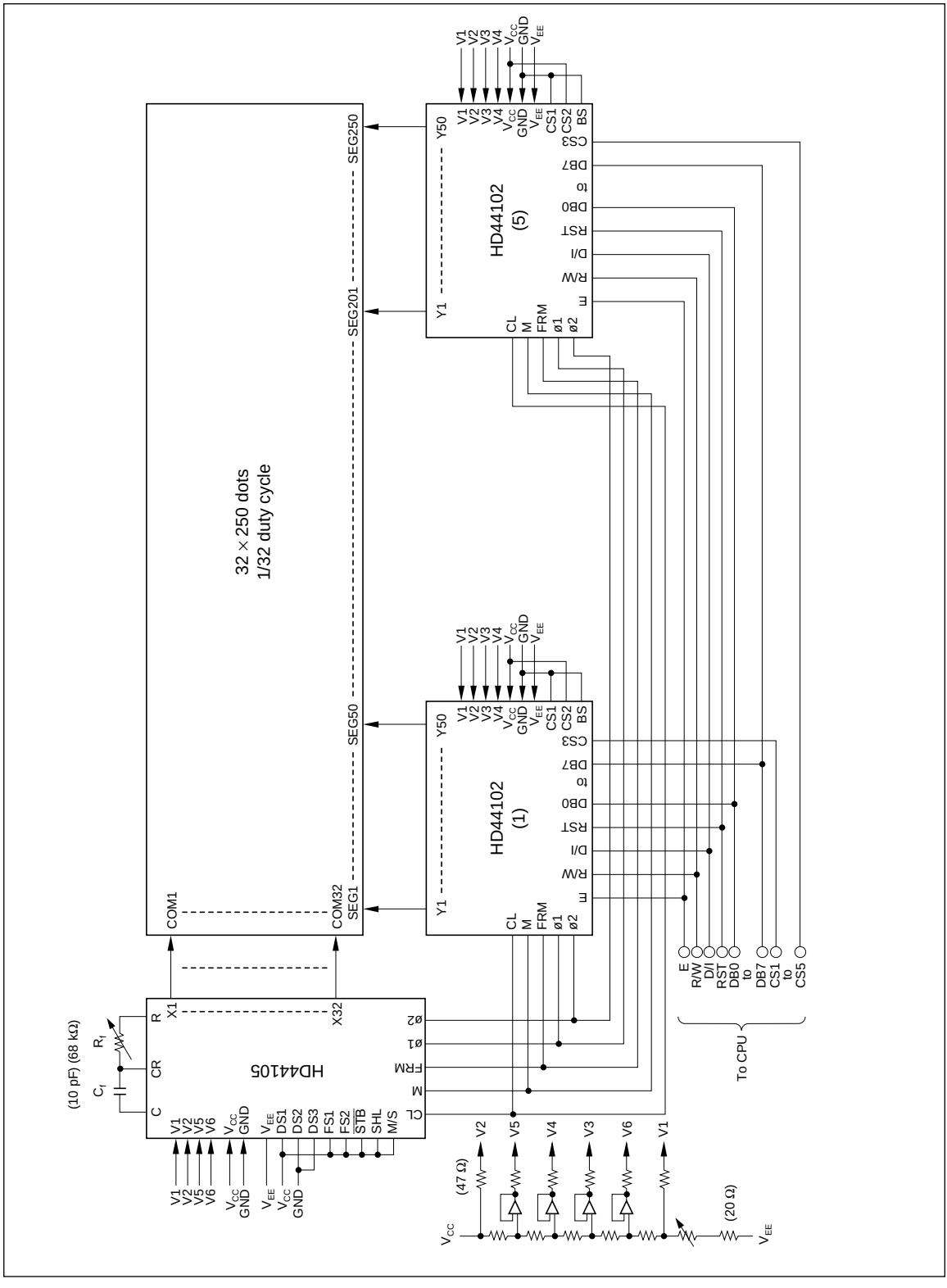
Bidirectional Shift Register

A 32-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 32 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Connection between HD44105 and HD44102



Absolute Maximum Ratings (Ta = 25°C)

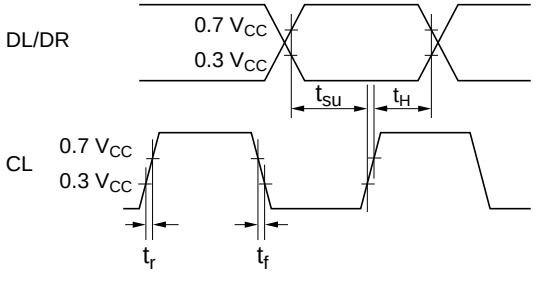
Item	Symbol	Ratings	Unit	Notes
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} – 13.5 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Referred to GND = 0 V.
2. Applied to input terminals (except for V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6. Connect a protection resistor of 47 Ω ± 10% to each terminal in series.

Electrical Characteristics (V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to –5.5 V, Ta = –20 to +75°C)(Note 4)

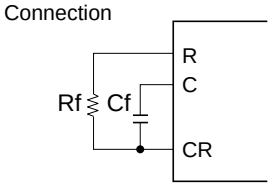
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		5
Input low voltage	V_{IL}	0	—	0.3 × V_{CC}	V		5
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA	6
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	6
Vi-Xj on resistance	R_{ON}	—	—	1000	Ω	V_{EE} = –5 V ± 10%, load current ±15 µA	
Input leakage current (1)	I_{IL1}	–1	—	1	µA	V_{IN} = V_{CC} to GND	7
Input leakage current (2)	I_{IL2}	–5	—	5	µA	V_{IN} = V_{CC} to V_{EE}	8
Shift frequency	F_{SFT}	—	—	50	kHz	In slave mode	9
Oscillation frequency	f_{OSC}	300	430	560	kHz	Rf = 68 kΩ ±2%, Cf = 10 pF ± 5%	10
External clock operating frequency	f_{CP}	50	—	560	kHz		11
External clock duty cycle	Duty	45	50	55	%		11
External clock rise time	t_{rCP}	—	—	50	ns		11
External clock fall time	t_{fCP}	—	—	50	ns		11
Dissipation power (master)	P_{W1}	—	—	4.4	mW	CR oscillation, 430 kHz	12
Dissipation power (slave)	P_{W2}	—	—	1.1	mW	Frame 70 Hz	13

Notes: 4. Specified within this range unless otherwise noted.
5. Applied to CR, FS1, FS2, DS1 to DS3, M, SHL, M/S, CL, DR, DL, and $\overline{STB}$.
6. Applied to DL, DR, M, FRM, CL, ø1, and ø2.
7. Applied to input terminals CR, FS1, FS2, DS1 to DS3, SHL, M/S, and $\overline{STB}$ and I/O common terminals DL, DR, M, and CL at high impedance.
8. Applied to V1, V2, V5, and V6.
9. Shift operation timing.

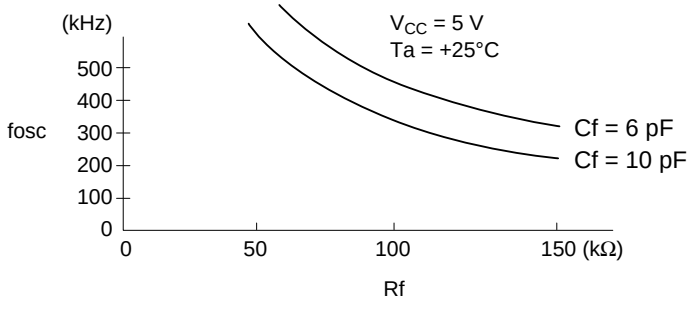


	Min	Typ	Max	Unit
t_{su}	5	—	—	µs
t_H	5	—	—	µs
t_r	—	—	100	ns
t_f	—	—	100	ns

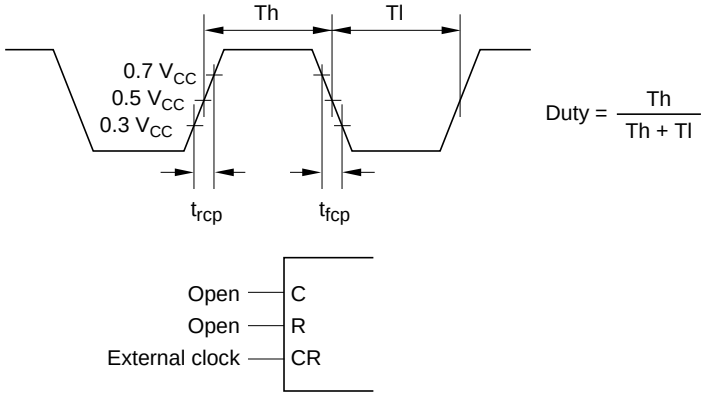
10. Relation between oscillation frequency and Rf, Cf.



The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



11.



12. Measured by V_{CC} terminal at output non-load of Rf = 68 kΩ ± 2% and Cf = 10 pF ± 5%, and 1/32 duty cycle in the master mode.
    Input terminals are connected to V_{CC} or GND.
13. Measured by V_{CC} terminal at output non-load, 1/32 duty cycle, and frame frequency of 70 Hz in the slave mode.
    Input terminals are connected to V_{CC} or GND.

HD61102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

HITACHI

Description

HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-controller in internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of each dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

The HD61102, which is produced by the CMOS process, can complete a portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61103A.

Features

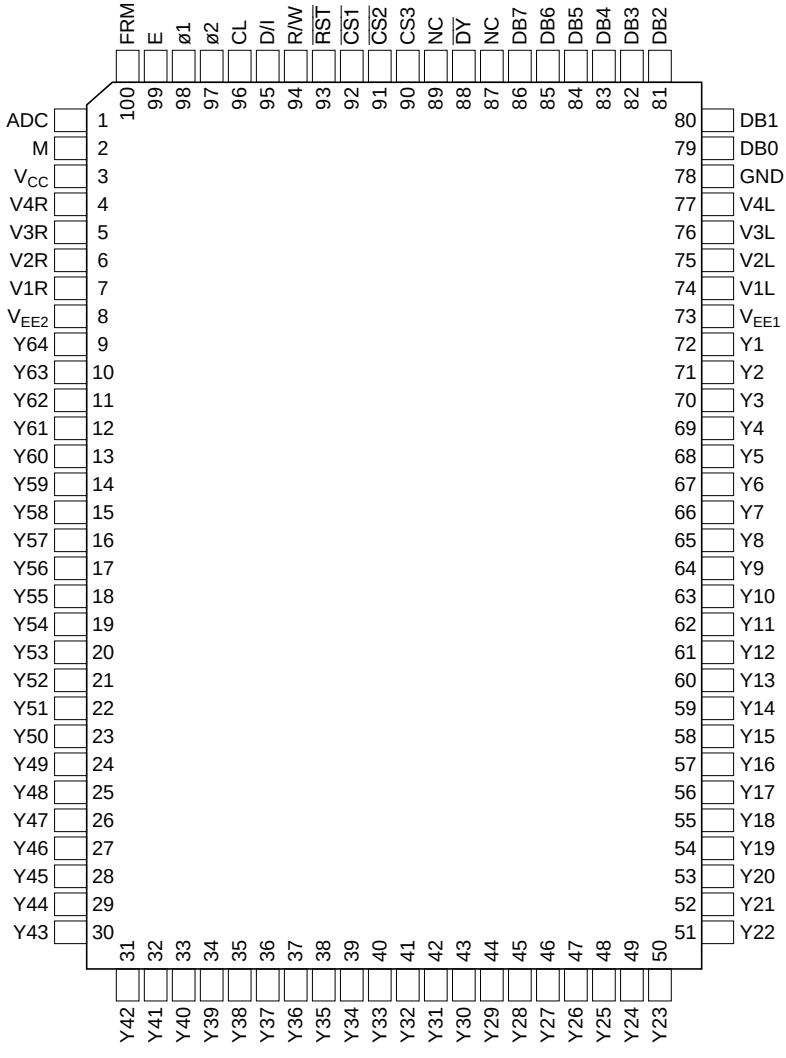
- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 0: Off
- Internal display RAM address counter: Preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty:
  - Combination of frame control signal and data latch synchronization signal make it possible to select static or optional duty cycle
- Wide range of instruction function:
  - Display data read/write, display on/off, set address, set display start line, read status
- Lower power dissipation: during display 2 mW max
- Power supply
  - V_{CC}: +5 V ± 10%
  - V_{EE}: 0 V to –10 V
- Liquid crystal display driving level: 15.5 V max
- CMOS process

Ordering Information

Type No.	Package
HD61102RH	100-pin plastic QFP (FP-100)

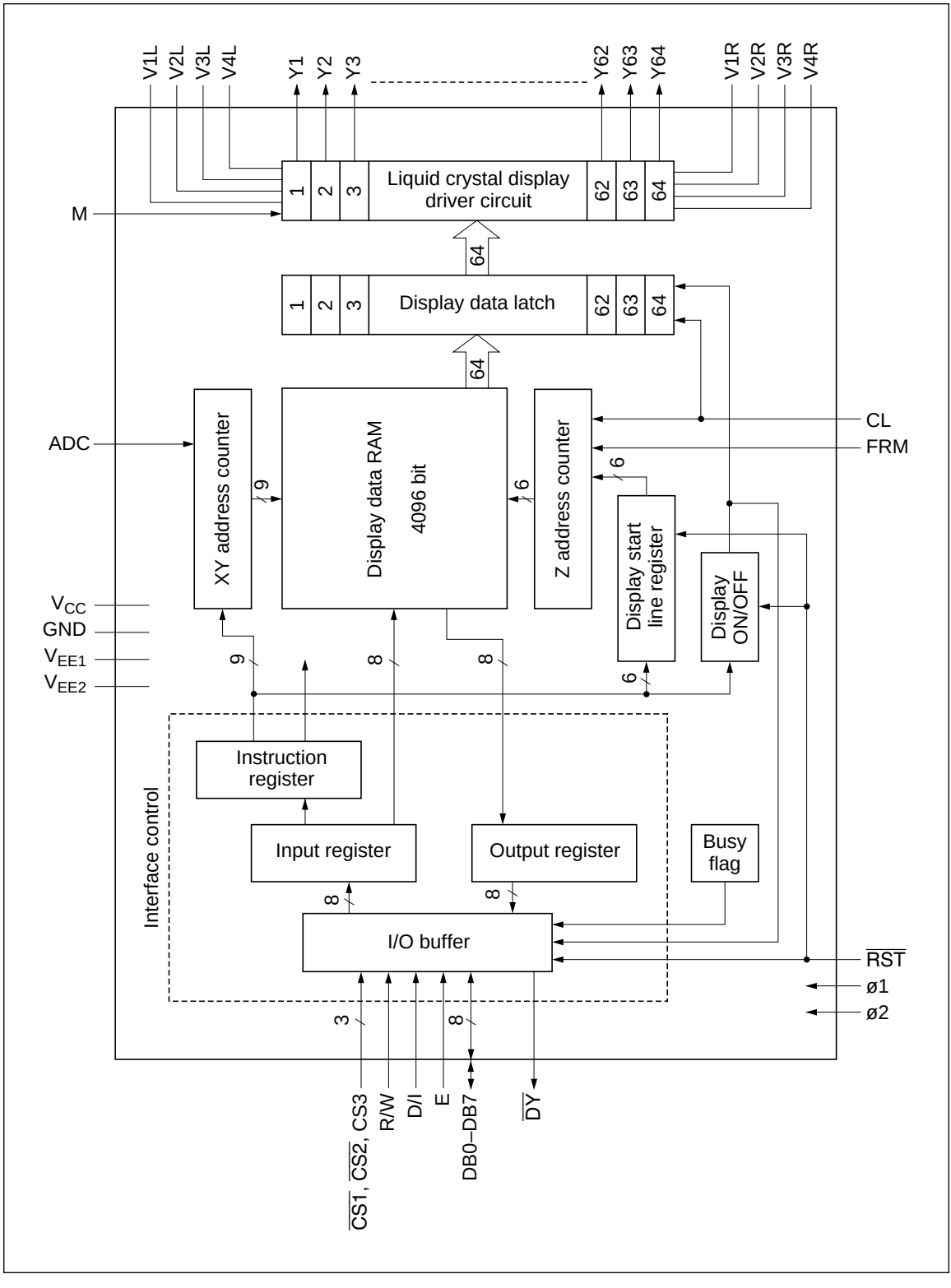
Hitachi semiconductor

Pin Arrangement



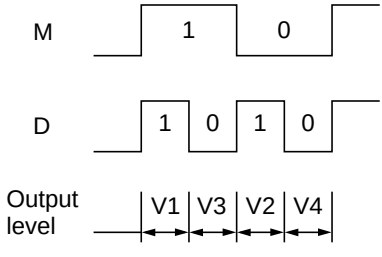
(Top view)

Block Diagram



Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is: GND = 0 V V_{CC} = +5 V ± 10%
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V_{CC} –15 to GND. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected to each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified for the liquid crystals within the limit of V_{EE} through V_{CC}. V1L (V1R), V2L (V2R): Selected level V3L (V3R), V4L (V4R): Non-selected level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection Data can be input or output when the terminals are in the following conditions: Terminal name: $\overline{CS1}$ $\overline{CS2}$ CS3 Condition: L L H
E	1	I	MPU	Enable At write (R/W = low): Data of DB0 to DB7 is latched at the fall of E. At read (R/W = high): Data appears at DB0 to DB7 while E is high.
R/W	1	I	MPU	Read/write R/W = High: Data appears at DB0 to DB7 and can be read by the MPU when E = high, $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high. R/W = Low: DB0 to DB7 accepted at fall of E when $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.
D/I	1	I	MPU	Data/instruction D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1–$0, Y64–$63 ADC = Low: Y64–$0, Y1–$63
DB0–DB7	8	I/O	MPU	Data bus, three-state I/O common terminals.
M	1	I	HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61103A	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61103A	Synchronous signal to latch display data. The rising edge of the CL signal increments the display output address counter and latches the display data.
ø1, ø2	1	I	HD61103A	2-phase clock signal for internal operation. The ø1 and ø2 clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1–Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins output light on level when 1 is in the display RAM, and light off level when 0 is in it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	MPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level: 1. On/off register set to 0 (display off) 2. Display start line register set to line 0 (displays from line 0) After releasing reset, this condition can be changed only by instruction.
$\overline{DY}$	1	O	Open	Output terminal for test. Normally, don't connect any lines to this terminal.
NC	2		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

I/O Buffer: Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (most significant bit)
DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, that is namely, the internal state is maintained and no instruction executes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

Register: Both input register and output register are provided to interface to MPU whose the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

1. Input Register

   The input register is used to store data temporarily before writing it into display data RAM. The data from MPU is written into input register, then into display data RAM automatically by internal operation.

   When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of E signal.

2. Output Register

   The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. The read display data instruction outputs data stored in the output register while E is high. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

   Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 1 shows the MPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register).
1	0	Writes data into input register as internal operation (input register → display data RAM).
0	1	Busy check. Read of status data.
0	0	Instruction.

Busy Flag

Busy flag = 1 indicates that HD61102 is operating and no instructions except status read can be accepted (figure 2). The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing an instruction.

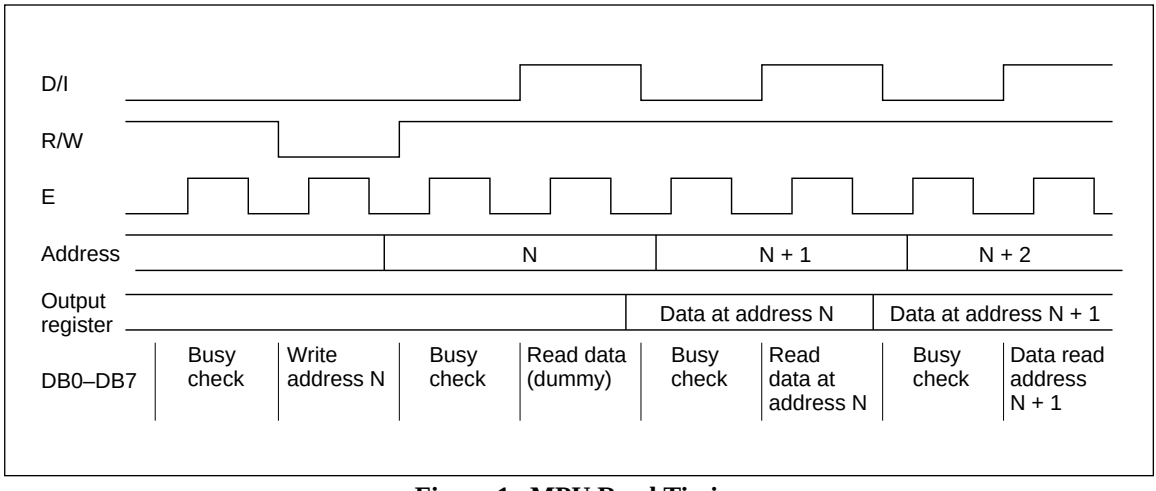


Figure 1 MPU Read Timing

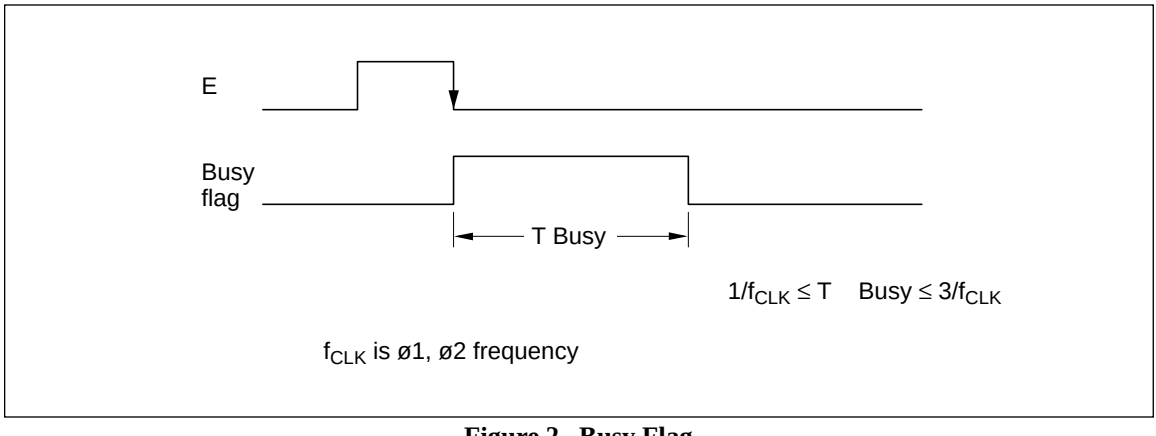


Figure 2 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by the display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by the status read instruction. The display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, C1 signal (display synchronous signal) should be input correctly.

Display Start Line Register

The register specifies a line in RAM that corresponds to the top line of the LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling the screen.

6-bit display start line information is written into this register by the display start line set instruction, with high level of FRM signal signalling the start of the display, the information in this register is transferred to the Z address counter, which controls the display address, and the Z address counter is preset.

X, Y Address Counter

A 9-bit counter that designates addresses of internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set by the respective instructions.

1. X Address Counter

   Ordinary register with no count functions. An address is set by instruction.

2. Y Address Counter

   An Address is set by instruction and it is increased by 1 automatically by display data R/W operations. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

As the ADC signal controls the Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, always connect ADC pin to V_{CC} or GND when using.

Figure 3 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

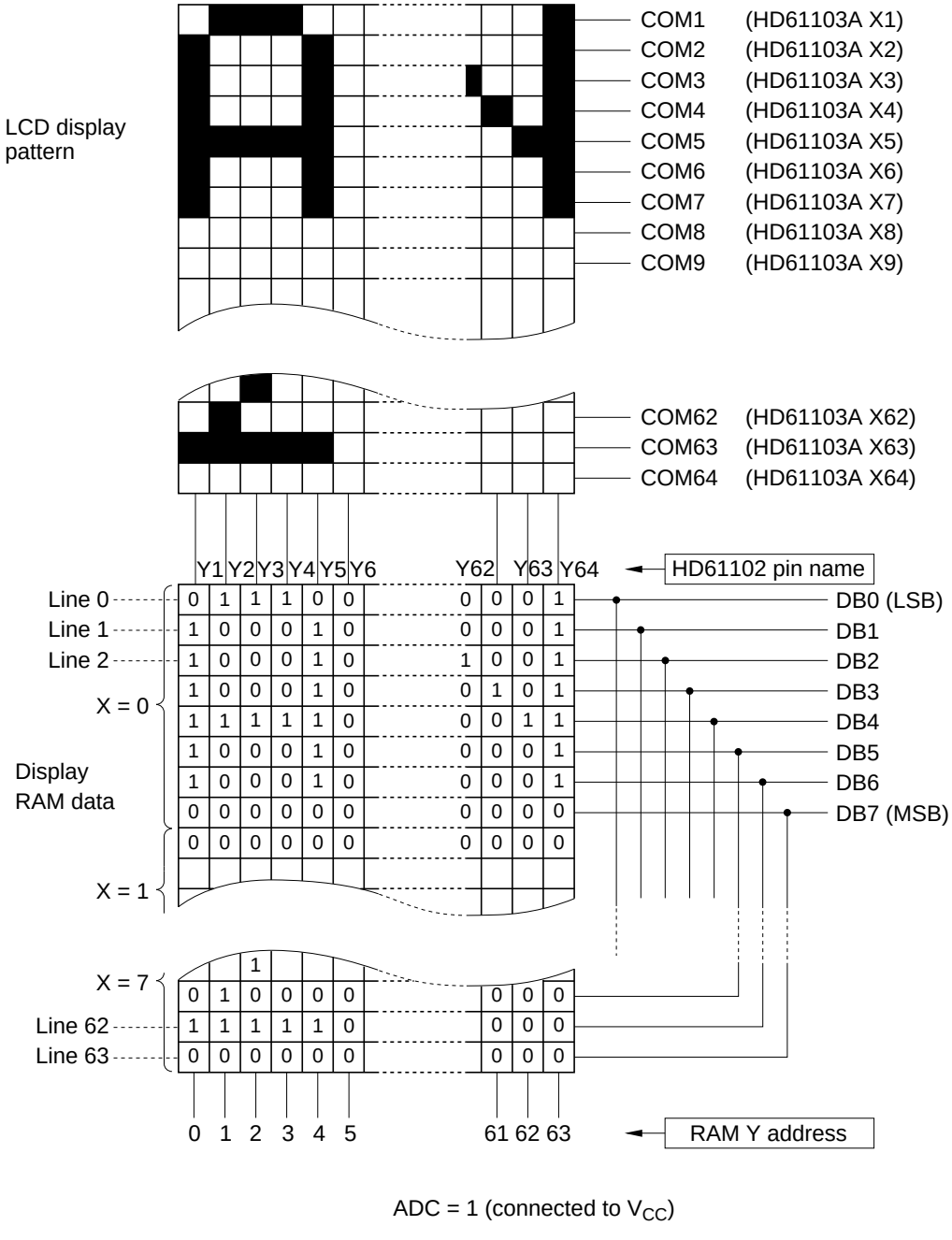


Figure 3 Relation between RAM Data and Display

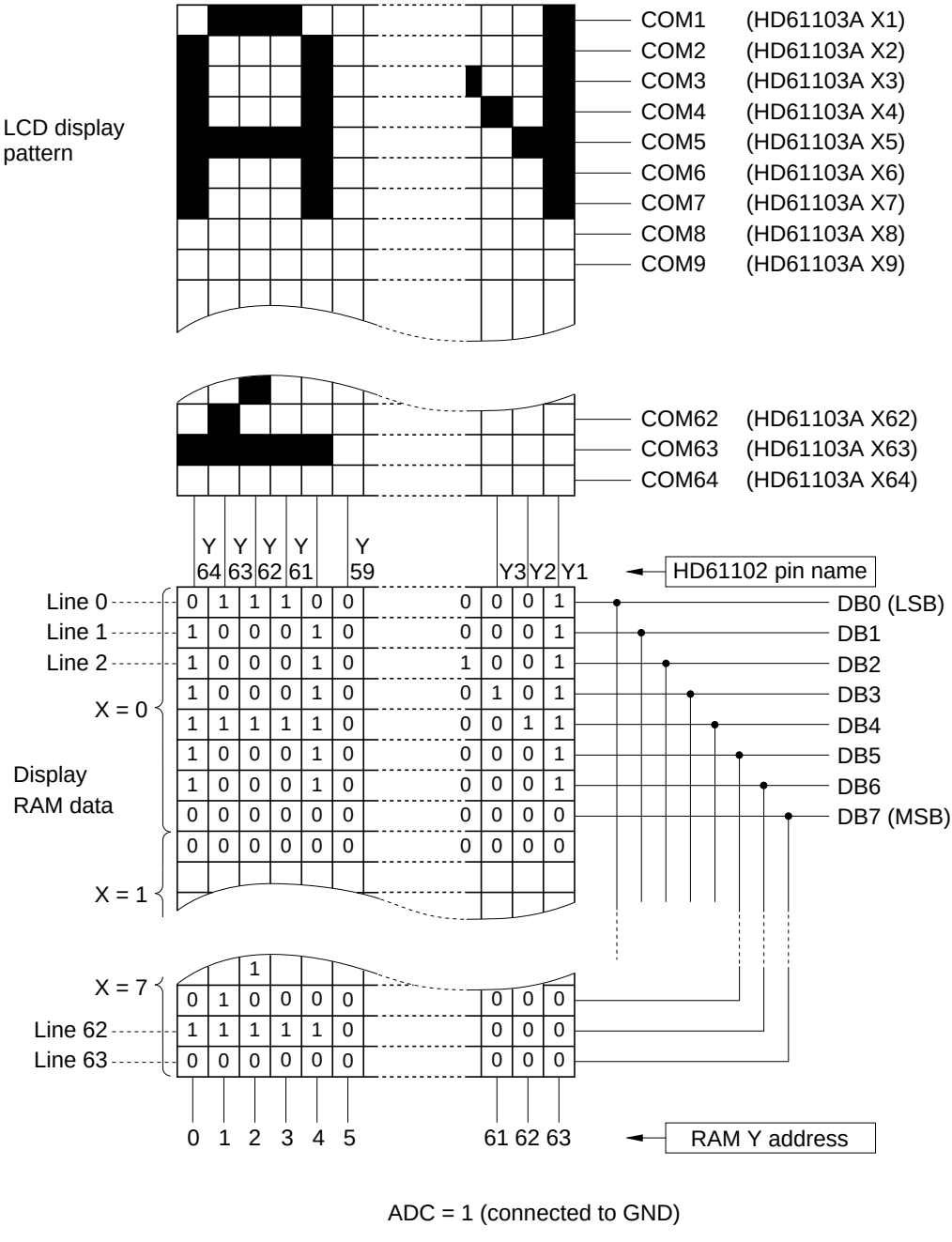


Figure 3 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At FRM high, the contents of the display start line register are preset in the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit.

Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal to low when turning power on.

1. Display off
2. Set display start line register line 0

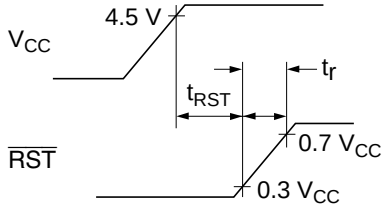
While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, carry out other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction.

The conditions of the power supply at initial power up are as in table 2.

Table 2 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 3 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.

These explanations are detailed in the following pages. Generally, there are the following three kinds of instructions.

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction are used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than the status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is the proof that an instruction is not being executed.

Table 3 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.	
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.	
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM in the page (X address) register.	
Set Y address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.	
Status read	1	0	Busy	0	ON/ OFF	RE- SET	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Executing internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note: 1. Busy time varies with the frequency (f_{CLK}) of ø1, and ø2.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

Display On/Off

	R/W	D/I	DB7	·····	DB0
Code	0	0	0	0	1	1	1	1	1	D
			MSB							LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen when D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display Start Line

	R/W	D/I	DB7	·····	DB0
Code	0	0	1	1	A	A	A	A	A	A
			MSB							LSB

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen.

Figure 4 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Set Page (X Address)

	R/W	D/I	DB7	·····	DB0
Code	0	0	1	0	1	1	1	A	A	A
			MSB							LSB

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 5.

Set Y Address

	R/W	D/I	DB7	·····	DB0
Code	0	0	0	1	A	A	A	A	A	A
			MSB							LSB

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7	·····	DB0
Code	1	0	Busy	0	ON/OFF	RESET	0	0	0	0
			MSB							LSB

- Busy

  When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

- ON/OFF

  Shows the liquid crystal display conditions: on condition or off condition.

  When ON/OFF is 1, the display is in off condition.
  When ON/OFF is 0, the display is in on condition.

- RESET

  RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

  RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

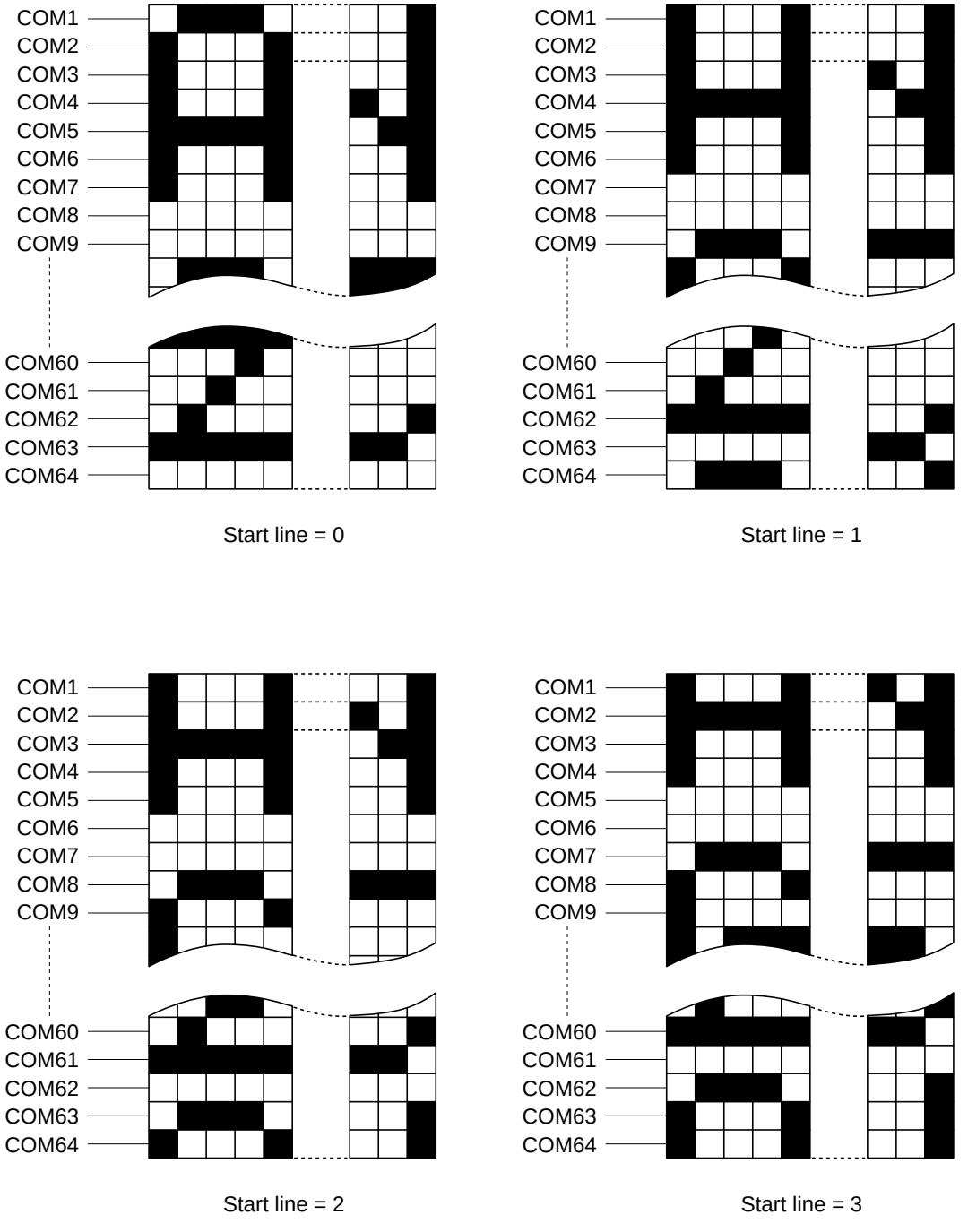


Figure 4 Relation between Start Line and Display

Write Display Data

	R/W	D/I	DB7	·····	DB0
Code	0	1	D	·····	D
			MSB		LSB

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W	D/I	DB7	·····	DB0
Code	1	1	D	·····	D
			MSB		LSB

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in “Function of Each Block”.

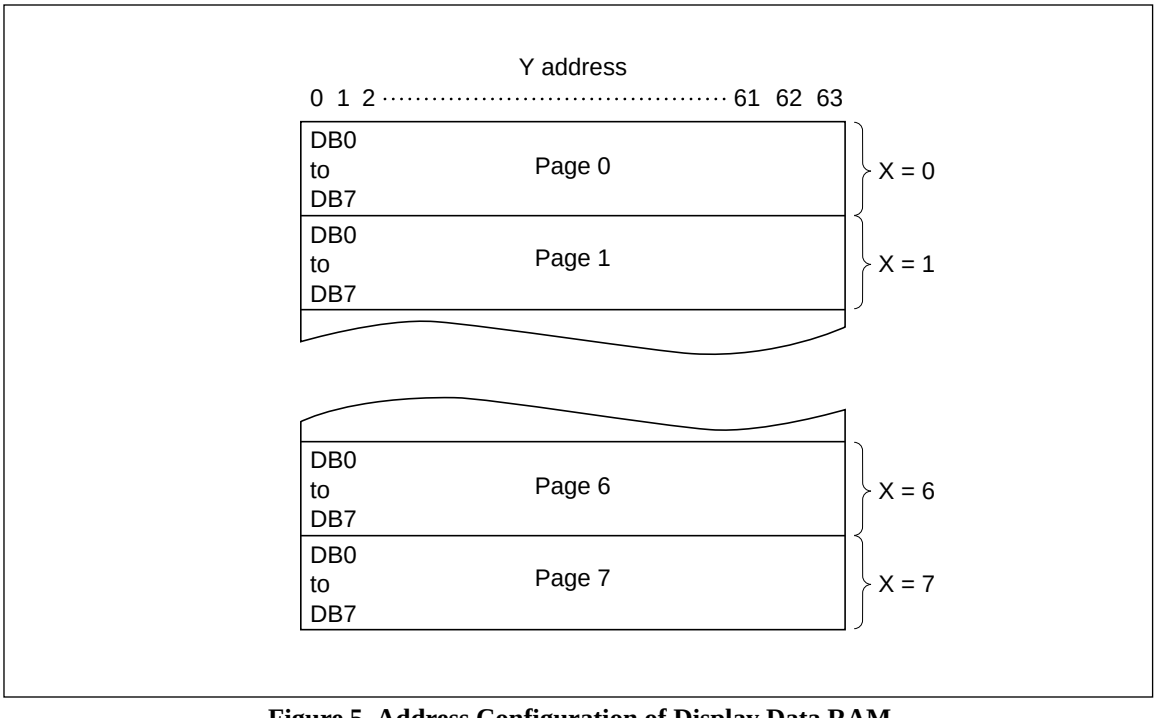
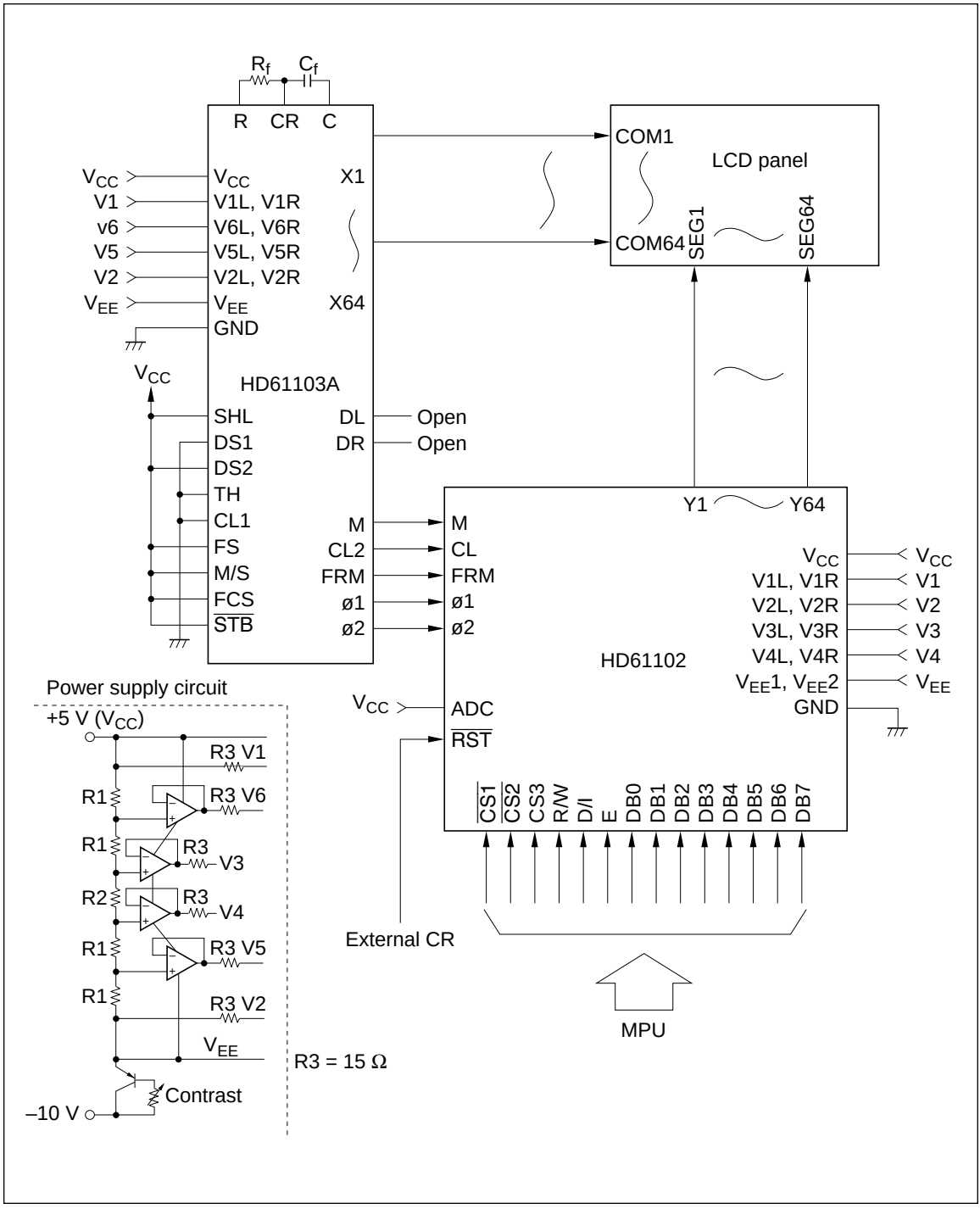
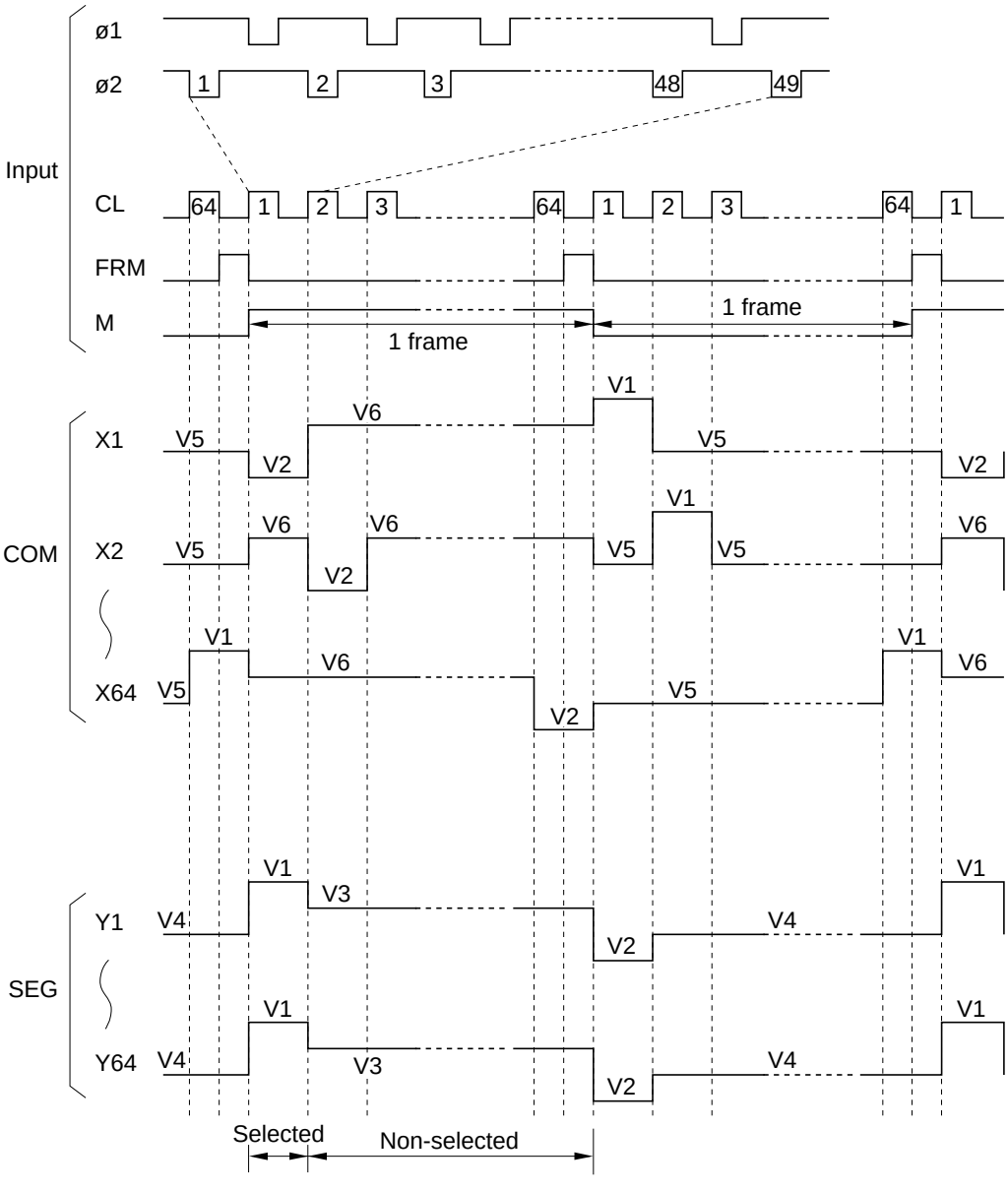


Figure 5 Address Configuration of Display Data RAM

Use of HD61102

Interface with HD61103A (1/64 Duty Cycle)





The waveforms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Figure 6 LCD Driver Timing Chart (1/64 Duty Cycle)

Interface with CPU

Example of Connection with HD6800

In this decoder (figure 7), addresses of HD61102 in the address area of HD6800 are:

Read/write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61102 by reading/ writing the data at these addresses.

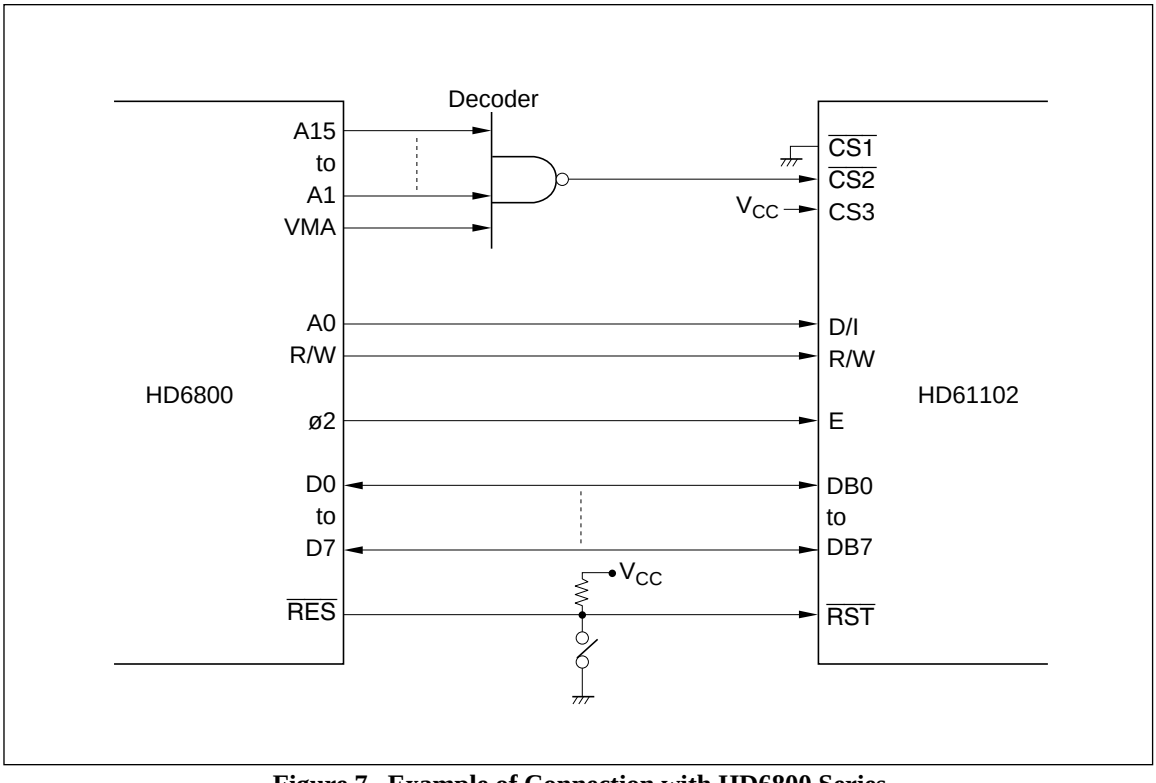


Figure 7 Example of Connection with HD6800 Series

Example of Connection with HD6801

- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus (figure 8).
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61102. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

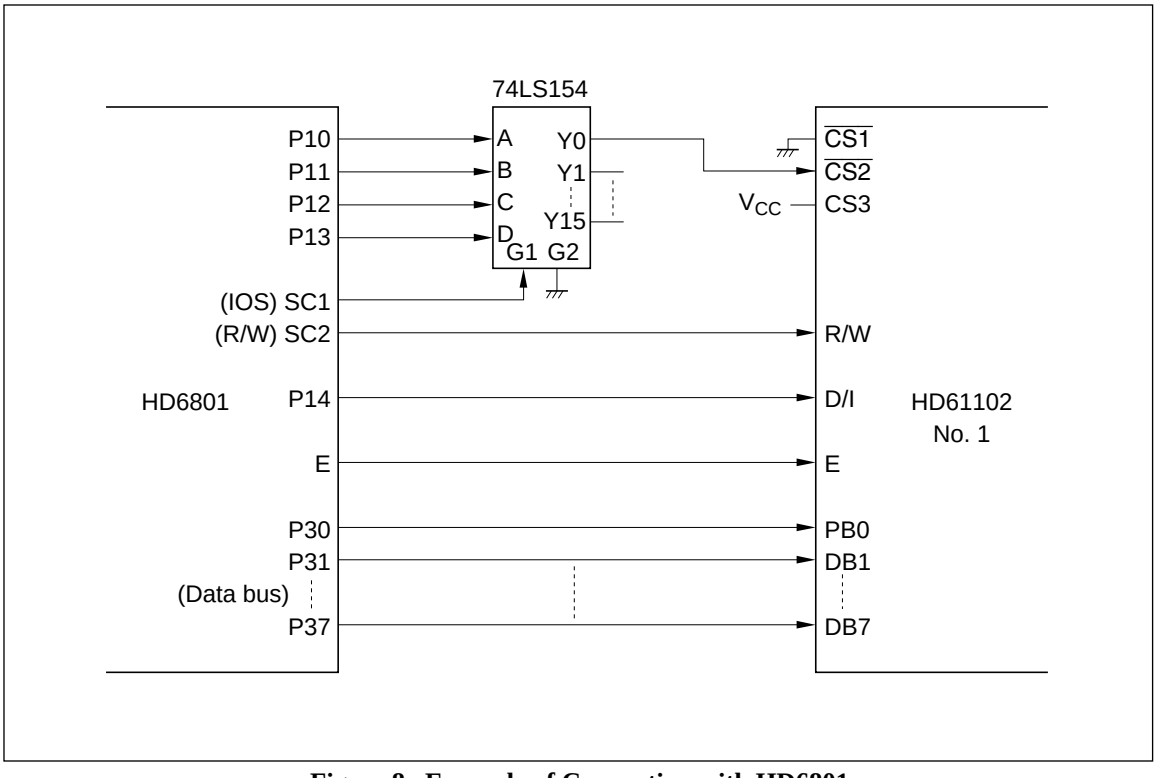


Figure 8 Example of Connection with HD6801

Example of Application

In this example (figure 9), two HD61103As output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

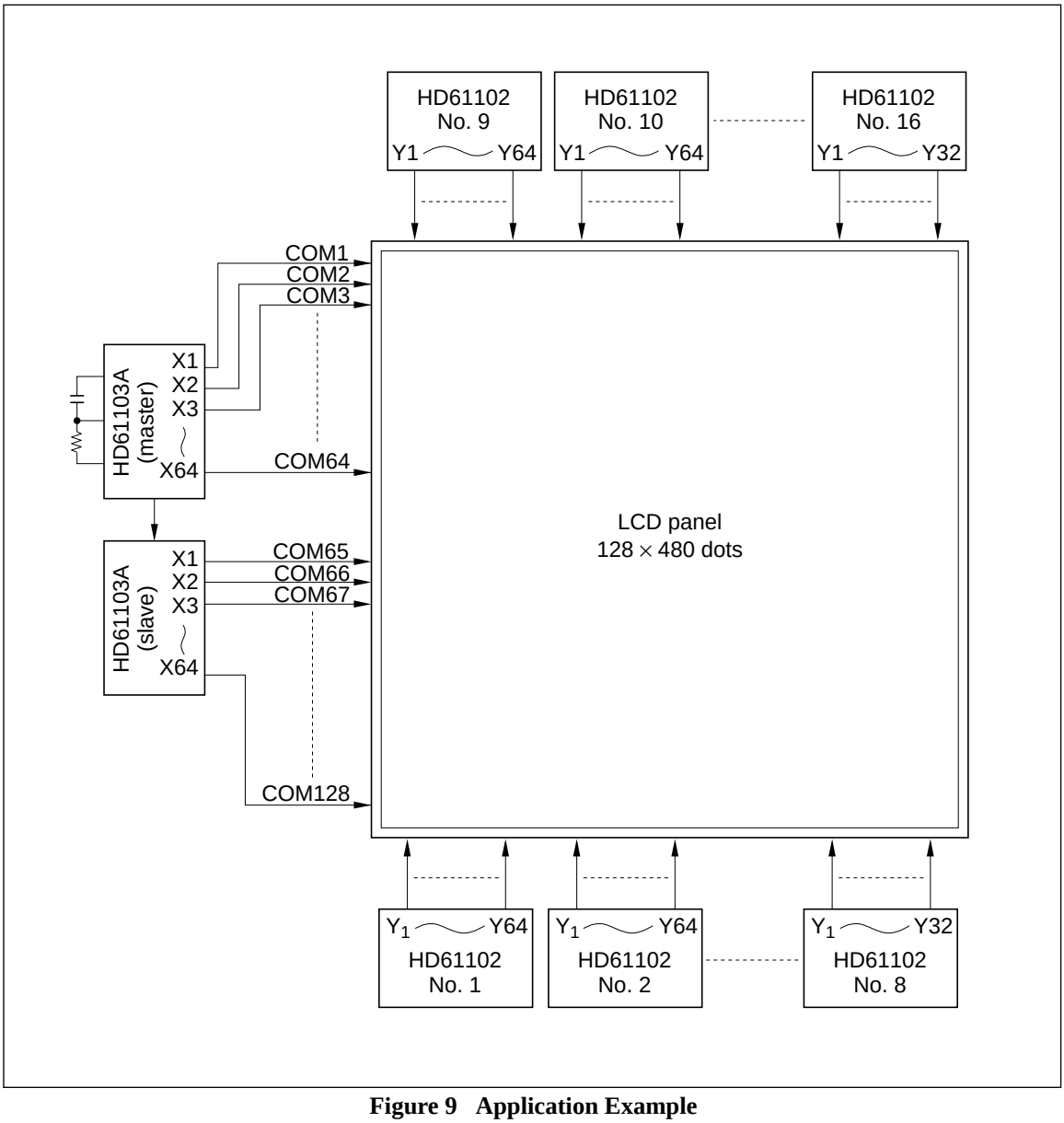


Figure 9 Application Example

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
supply voltage	V_{CC}	–0.3 to +7.0	V	2
	V_{EE1}, V_{EE2}	V_{CC} – 16.5 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminal voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them within the recommended operating conditions.
Use beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
Maintain
$V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, ø1, ø2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC, and DB0–DB7.

Electrical Characteristics (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition	Notes
Input high voltage	V_{IHC}	0.7 × V_{CC}	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	0.3 × V_{CC}	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND – V_{CC}	4
High impedance off input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND – V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE} – V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	V_{CC} – V_{EE} = 15 V ±I_{LOAD} = 0.1 mA	7
Dissipation current	I_{CC}(1)	—	—	100	µA	During display	8
	I_{CC}(2)	—	—	500	µA	During access Access cycle = 1 MHz	8

Notes: 1. Applies to M, FRM, CL, $\overline{RST}$, ø1, ADC, and ø2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to input terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Applies to Y1–Y64.
7. Specified when liquid crystal display is in 1/64 duty.

   Operation frequency: f_{CLK} = 250 kHz (ø1 and ø2 frequency)
   Frame frequency: f_M = 70 Hz (FRM frequency)

   Specified in the state of

   Output terminal: Not loaded
   Input level: V_{IH} = V_{CC} (V)
   V_{IL} = GND (V)

   Measured at V_{CC} terminal

Interface AC Characteristics

MPU Interface (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
E cycle time	t_{CYC}	1000	—	—	ns	Fig. 10, Fig. 11
E high level width	P_{WEH}	450	—	—	ns	
E low level width	P_{WEL}	450	—	—	ns	
E rise time	t_r	—	—	25	ns	
E fall time	t_f	—	—	25	ns	
Address setup time	t_{AS}	140	—	—	ns	
Address hold time	t_{AH}	10	—	—	ns	
Data setup time	t_{DSW}	200	—	—	ns	Fig. 10
Data delay time	t_{DDR}	—	—	320	ns	Fig. 11, Fig. 12
Data hold time (write)	t_{DHW}	10	—	—	ns	Fig. 10
Data hold time (read)	t_{DHR}	20	—	—	ns	Fig. 11

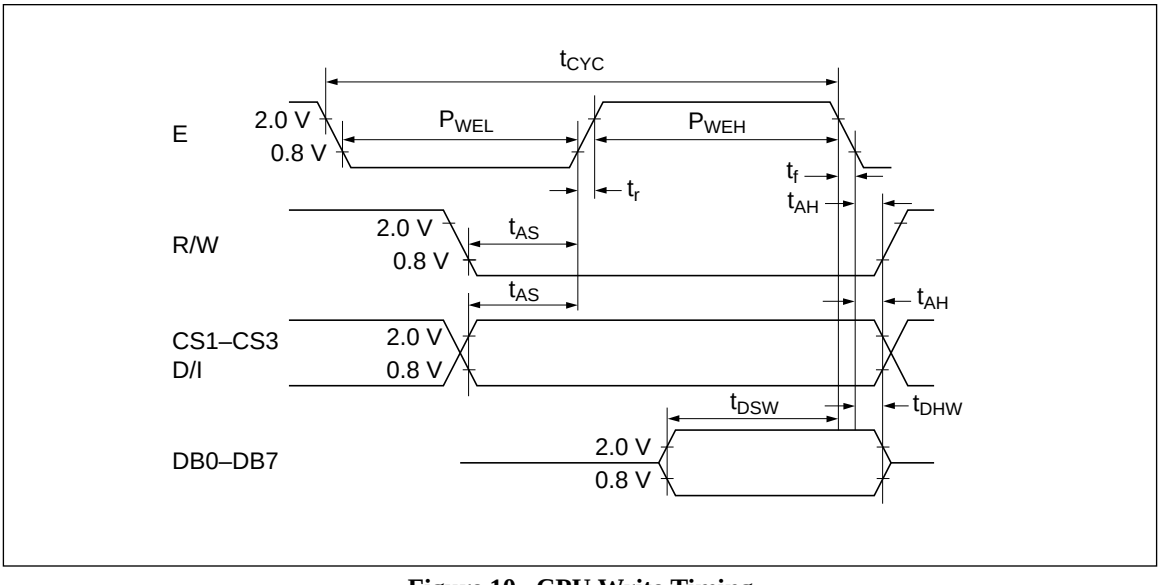


Figure 10 CPU Write Timing

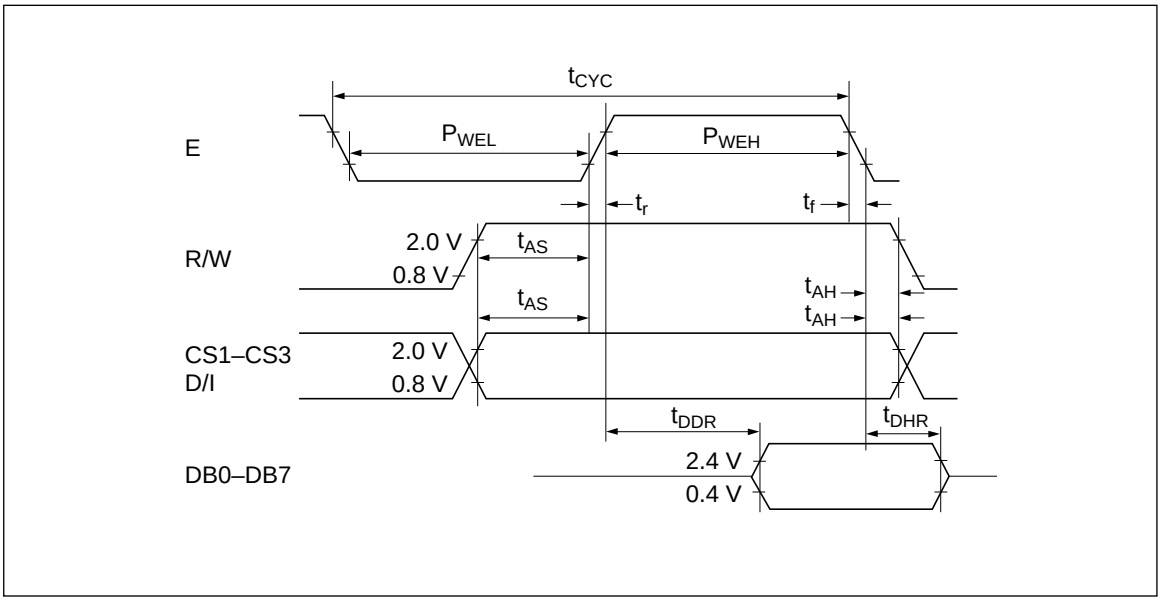


Figure 11 CPU Read Timing

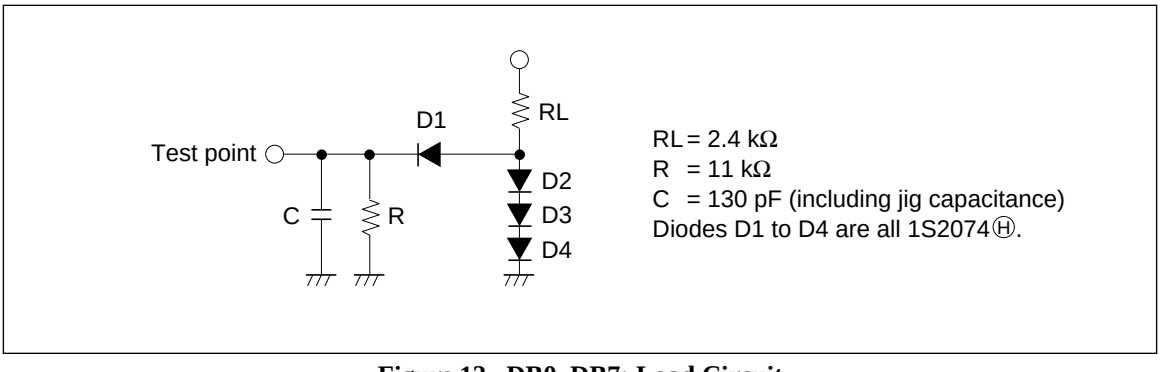


Figure 12 DB0–DB7: Load Circuit

Clock Timing (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
ø1, ø2 cycle time	t_{cyc}	2.5	—	20	µs	Fig. 13
ø1 low level width	$t_{WLø1}$	625	—	—	ns	
ø2 low level width	$t_{WLø2}$	625	—	—	ns	
ø1 high level width	$t_{WHø1}$	1875	—	—	ns	
ø2 high level width	$t_{WHø2}$	1875	—	—	ns	
ø1—ø2 phase difference	t_{D12}	625	—	—	ns	
ø2—ø1 phase difference	t_{D21}	625	—	—	ns	
ø1, ø2 rise time	t_r	—	—	150	ns	
ø1, ø2 fall time	t_f	—	—	150	ns	

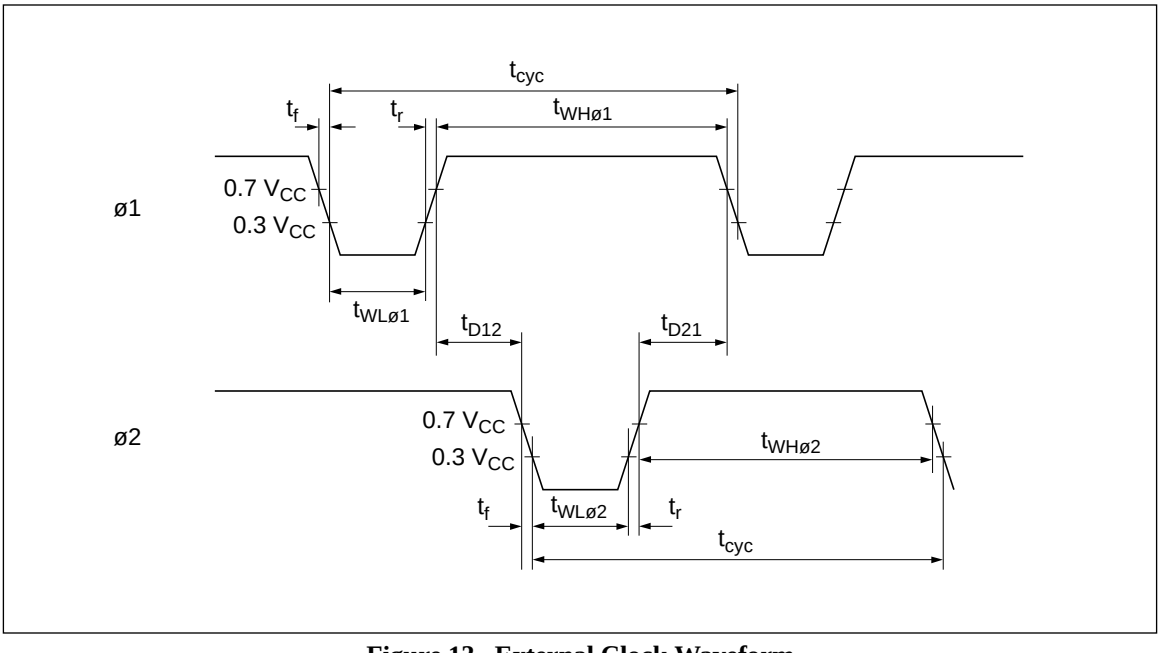


Figure 13 External Clock Waveform

Display Control Timing (GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{EE} = 0 to –10 V, Ta = –20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 14
M delay time	t_{DM}	–2	—	+2	µs	
CL low level width	t_{WLCL}	35	—	—	µs	
CL high level width	t_{WHCL}	35	—	—	µs	

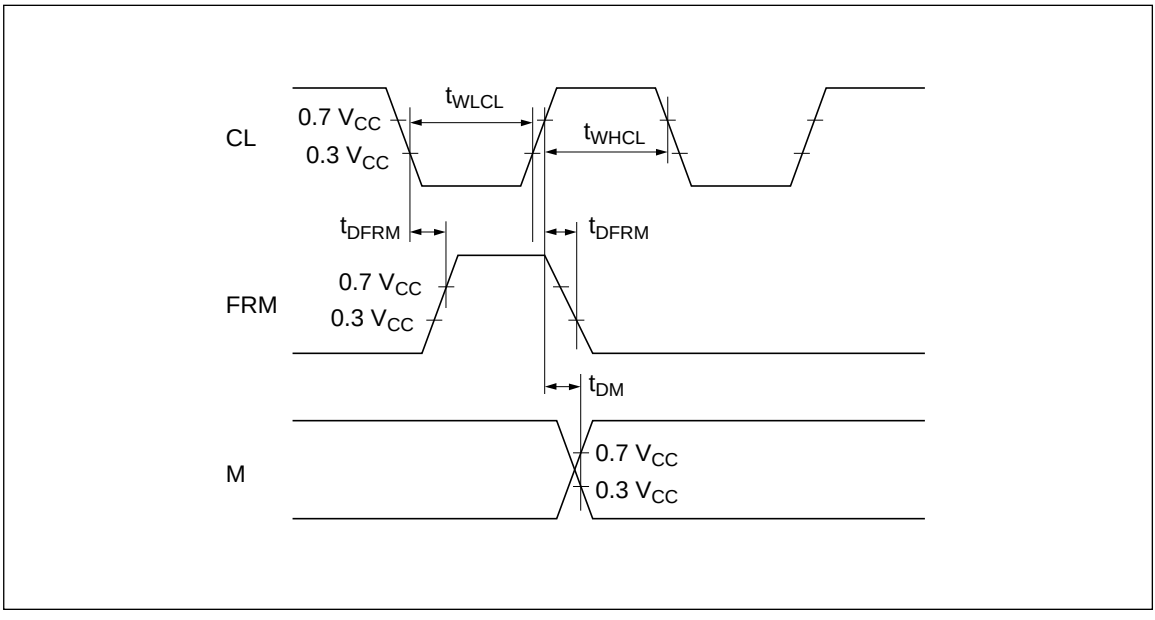


Figure 14 Display Control Signal Waveform

HD61103A

(Dot Matrix Liquid Crystal Graphic Display
64-Channel Common Driver)

HITACHI

Description

The HD61103A is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61103A is produced by a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61103A and the column (segment) driver HD61102.

Features

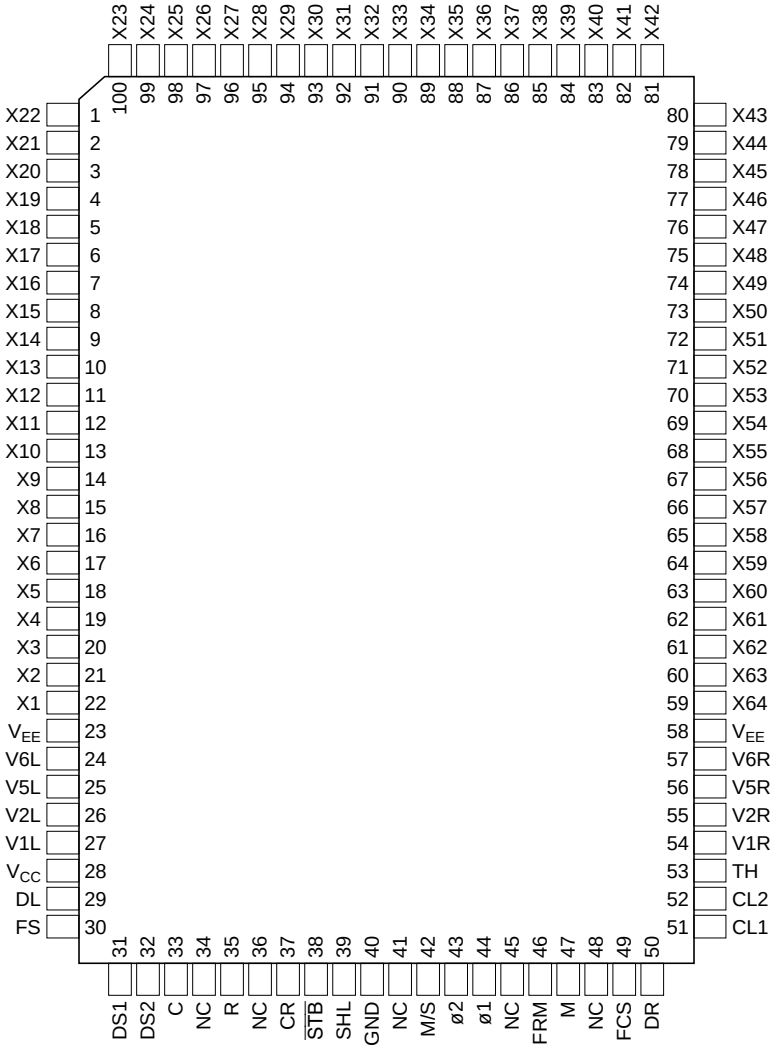
- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Selectable display duty ratio factor 1/48, 1/64, 1/96, 1/128
- Can be used as a column driver transferring data serially
- Low power dissipation: During display: 5 mW
- Power supplies:
  - V_{CC}: +5 V ± 10%
  - V_{EE}: 0 to –11.5 V
- LCD driver level: 17.0 V max
- CMOS process

Ordering Information

Type No.	Package
HD61103A	100-pin plastic QFP (FP-100)

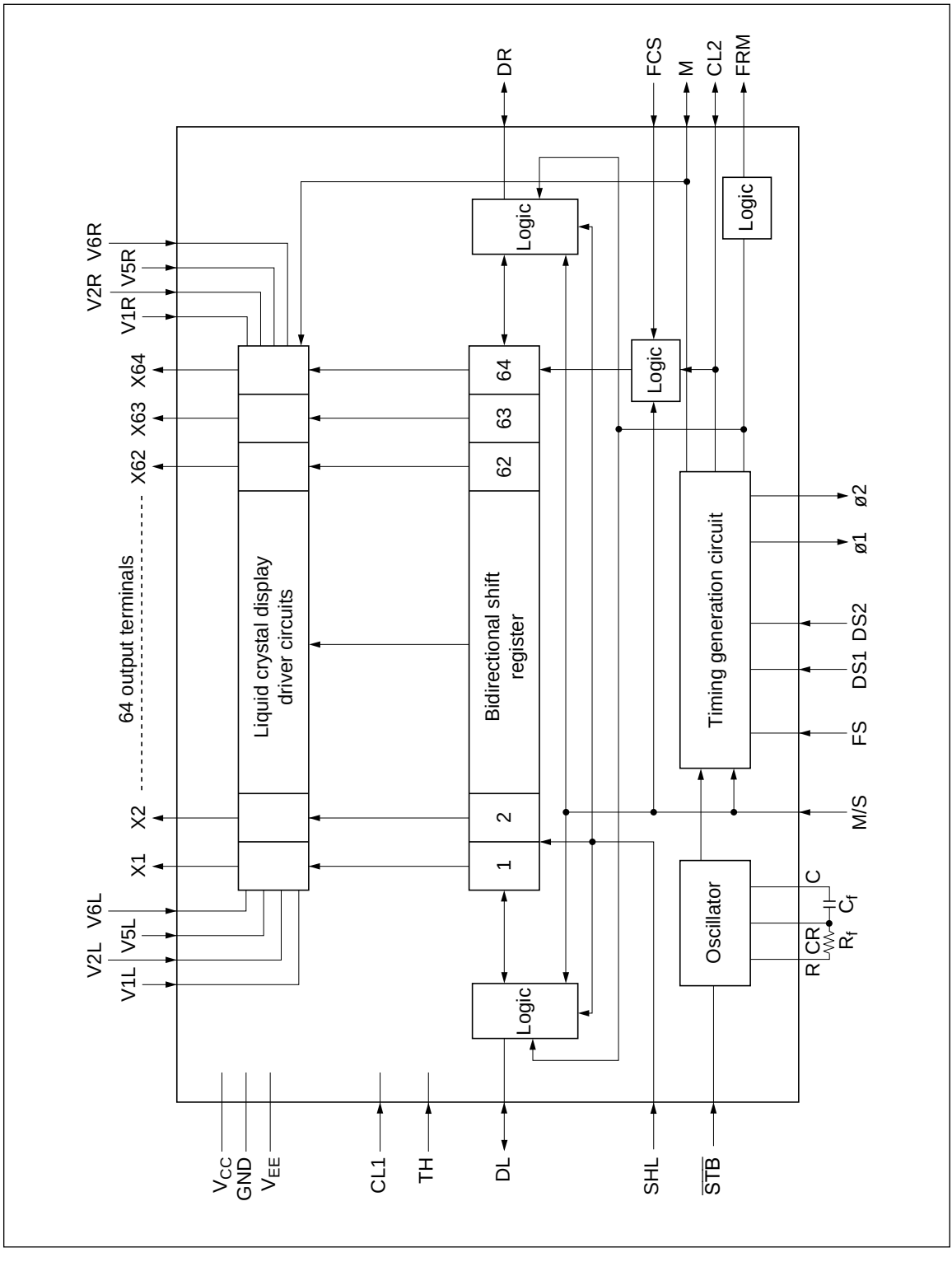
Hitachi semiconductor

Pin Arrangement



(Top view)

Block Diagram



Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61202. It is required when the HD61103A is used with the HD61102. An oscillation resistor Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{STB}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminals R and C.

The oscillator is not required when the HD61103A is used with the HD61830. Connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

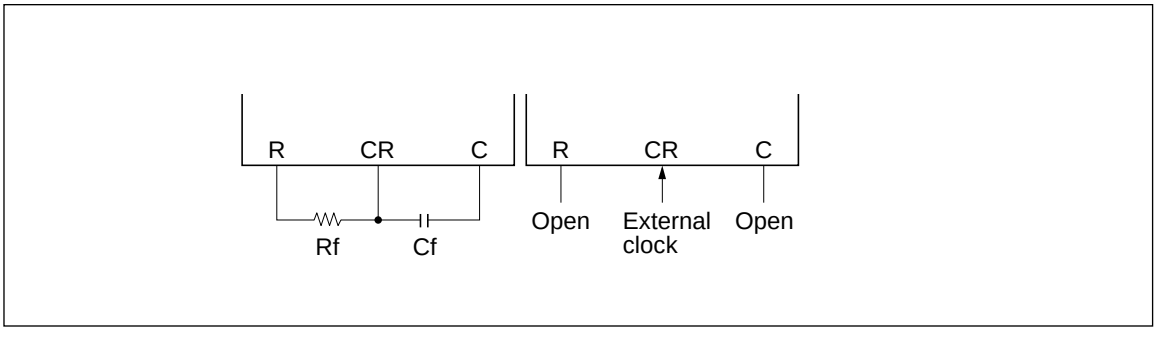


Figure 1 Oscillator Connection with HD61102

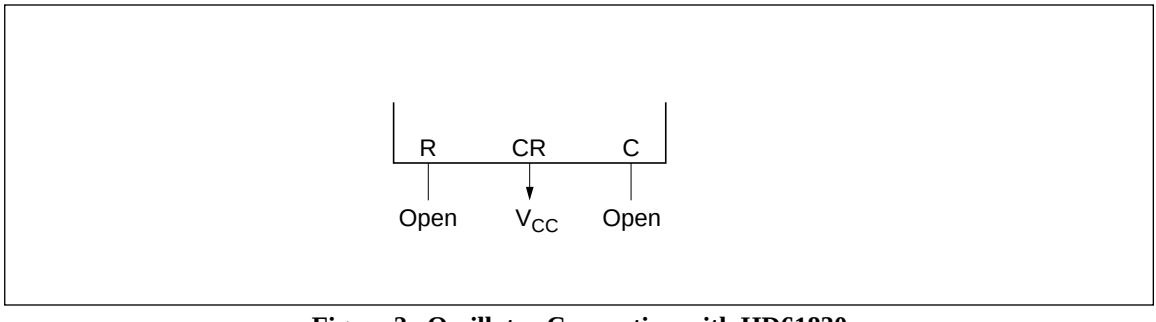


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61102. This circuit is required when the HD61103A is used with the HD61102. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals Fs, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

Table 1 Output Levels

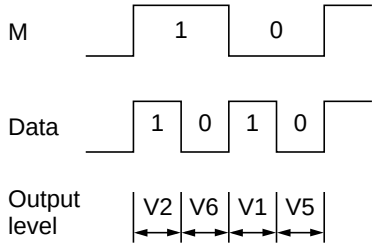
Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

HD61103A Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC}–GND: Power supply for internal logic. V_{CC}–V_{EE}: Power supply for driver circuit logic.
V1L, V2L V5L, V6L V1R, V2R V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects master/slave. • M/S = V_{CC}: Master mode When the HD61103A is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61102. Each of I/O common terminals DL, DR, CL2, and M is in the output state. • M/S = GND: Slave mode The timing operation circuit stops operating. The HD61103A is used in this mode when combined with the HD61830. Even if combined with the HD61102, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61103A in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. • FCS = V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61103A is used with HD61102 or when MA of the HD61830 connects to CL2 in combination with the HD61830. • FCS = GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.

Terminal Name	Number of Terminals	I/O	Connected to	Functions
FS	1	I	V_{CC} or GND	Selects frequency. When the frame frequency is 70 Hz, the oscillation frequency should be: f_{OSC} = 430 kHz at FCS = V_{CC} f_{OSC} = 215 kHz at FCS = GND This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.
DS1, DS2	2	I	V_{CC} or GND	Selects display duty factor. Display Duty Factor: 1/48 / 1/64 / 1/96 / 1/128 DS1: GND / GND / V_{CC} / V_{CC} DS2: GND / V_{CC} / GND / V_{CC} These terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.
$\overline{STB}$ TH CL1	1 1 1	I	V_{CC} or GND	Input terminal for testing. Connect to $\overline{STB}$ V_{CC}. Connect TH and CL1 to GND.
CR, R, C	3			Oscillator. In the master mode, use these terminals as shown below. Usage of these terminals in the master mode: Internal oscillation: Rf, Cf; R, CR, C External clock: Open, External clock, Open; R, CR, C In the slave mode, stop the oscillator as shown below: Open, V_{CC}, Open; R, CR, C
ø1, ø2	2	O	HD61102	Operating clock output terminals for the HD61102. • Master mode Connect these terminals to terminals ø1 and ø2 of the HD61102 respectively. • Slave mode Don't connect any lines to these terminals.

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>HD61102</td><td>Frame signal
• Master mode
Connect this terminal to terminal FRM of the HD61102.
• Slave mode
Don’t connect any lines to this terminal.</td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61102</td><td>Signal to convert LCD driver signal into AC
• Master mode: Output terminal
Connect this terminal to terminal M of the HD61102.
• Slave mode: Input terminal
Connect this terminal to terminal MB of the HD61830.</td></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61102</td><td>Shift clock
• Master mode: Output terminal
Connect this terminal to terminal CL of the HD61102.
• Slave mode: Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register
DL corresponds to X1’s side and DR to X64’s side.
• Master mode
Output common scanning signal. Don’t connect any lines to these terminals normally.
• Slave mode
Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don’t connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><td>SHL</td><td>Shift Direction</td><td>Common Scanning Direction</td></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
</table>

Terminal Name	Number of Terminals	I/O	Connected to	Functions
X1–X64	64	O	Liquid crystal display	Liquid crystal display driver output Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the data from the shift register and M signal.  Data 1: Selected level 0: Non-selected level When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

Example of Application

HD61103A Connection List

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	ø1	ø2	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From CL1 of HD61830	H	From FLM of HD61830	—	COM1–COM64
																	L	—	From FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From MA of HD61830	H	From FLM of HD61830	To DL/DR of HD61103A No. 2	COM1–COM64
																	L	To DL/DR of HD61103A No. 2	From FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From MA of HD61830	H	From DL/DR of HD61103A No. 1	—	COM65–COM128
																	L	—	From DL/DR of HD61103A No. 1	COM128–COM65
D	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	To ø1 of HD61102	To ø2 of HD61102	To FRM of HD61102	To M of HD61102	To CL of HD61102	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	To ø1 of HD61102	To ø2 of HD61102	To FRM of HD61102	To M of HD61102 HD61103A	To CL of HD61102 To CL2 of HD61103A	H	—	To DL/DR of HD61103A No. 2	COM1–COM64
																	L	To DL/DR of HD61103A No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From M of HD61103A No. 1	From CL2 of HD61103A No. 1	H	From DL/DR of HD61103A No. 1	—	COM1–COM64
																	L	—	From DL/DR of HD61103A No. 1	COM64–COM1

Notes: H: V_{CC} } Fixed
L: GND }

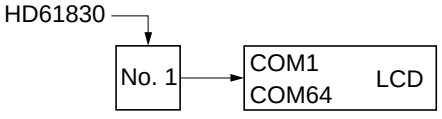
"—" means "open".

Rf: Oscillation resister
Cf: Oscillation capacitor

Outline of HD61103A System Configuration

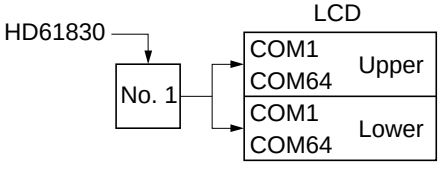
Use with HD61830

1. When display duty ratio of LCD is more than 1/64



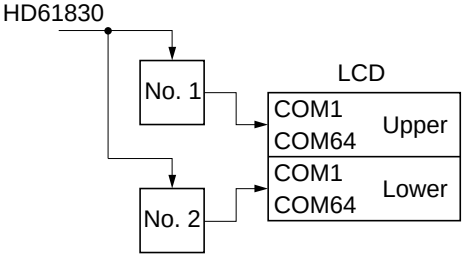
One HD61103A drives common signals.

Refer to Connection List A.



One HD61103A drives common signals for upper and lower panels.

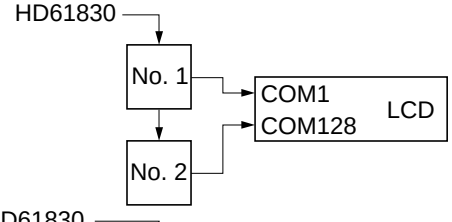
Refer to Connection List A.



Two HD61103As drive upper and lower panels separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

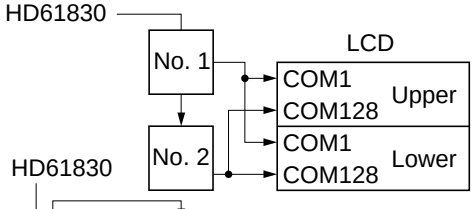
For both of No. 1 and No. 2, refer to Connection List A.

2. When display duty ratio of LCD is from 1/65 to 1/128



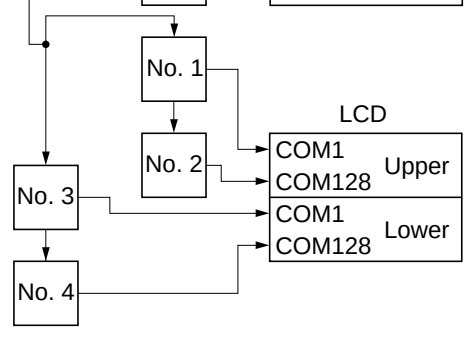
Two HD61103As connected serially drive common signals.

Refer to Connection List B for No. 1.
Refer to Connection List C for No. 2.



Two HD61103As connected serially drive upper and lower panels in parallel.

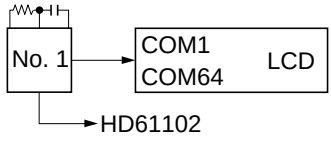
Refer to Connection List B for No. 1.
Refer to Connection List C for No. 2.



Two sets of HD61103As connected serially drive upper and lower panels in parallel to ensure the quality of display.

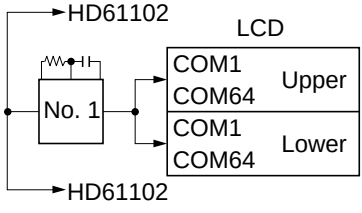
Refer to Connection List B for No. 1 and 3.
Refer to Connection List C for No. 2 and 4.

Use with HD61102 (1/64 Duty Ratio)



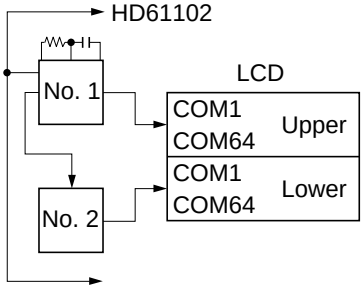
One HD61103A drives common signals and supplies timing signals to the HD61102s.

Refer to Connection List D.



One HD61103A drives upper and lower panels and supplies timing signals to the HD61102s.

Refer to Connection List D.



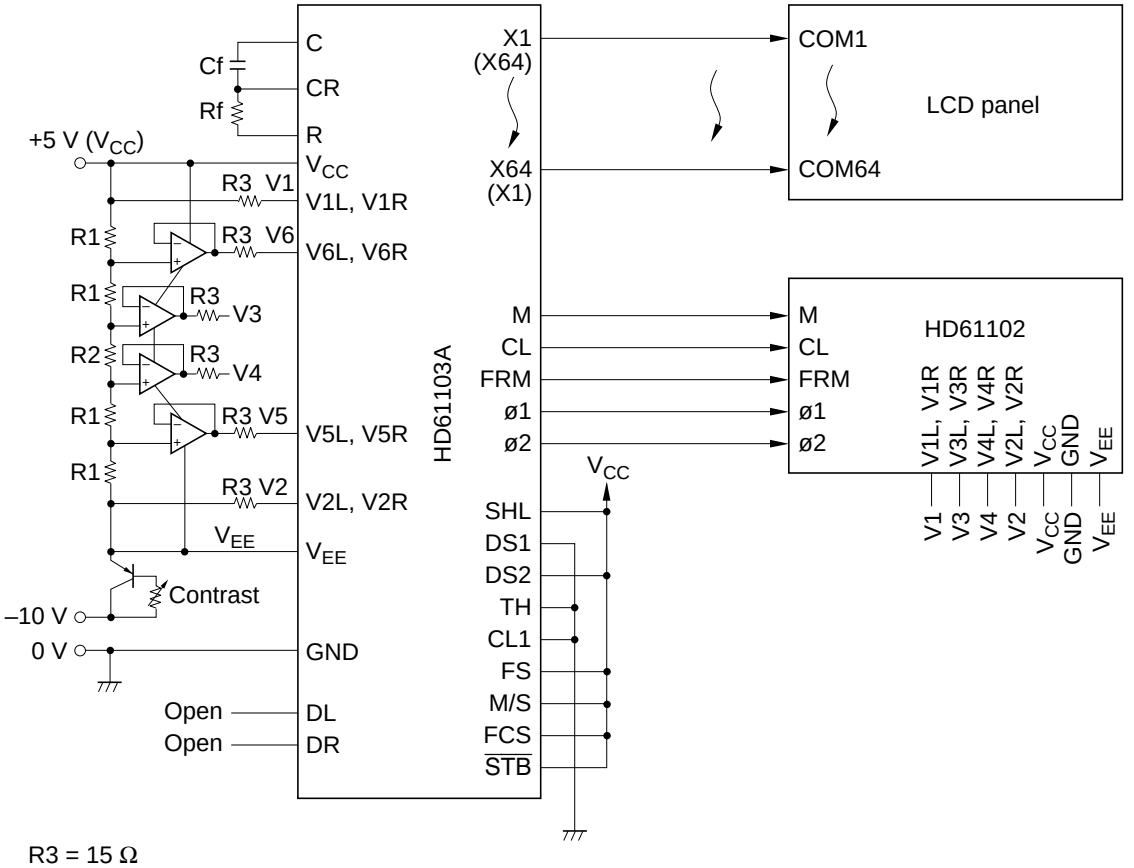
Two HD61103As drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61102s.

Refer to Connection List E for No. 1.
Refer to Connection List F for No. 2.

Connection Example 1

Use with HD61102 (RAM Type Segment Driver)

1. 1/64 duty ratio (see Connection List D)



R3 = 15 Ω

( ) is at SHL = Low

Note: The values of R1 and R2 vary with the LCD panel used. When bias factor is 1/9, the values of R1 and R2 should satisfy.

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1 = 3 kΩ, R2 = 15 kΩ

Figure 3 Example 1

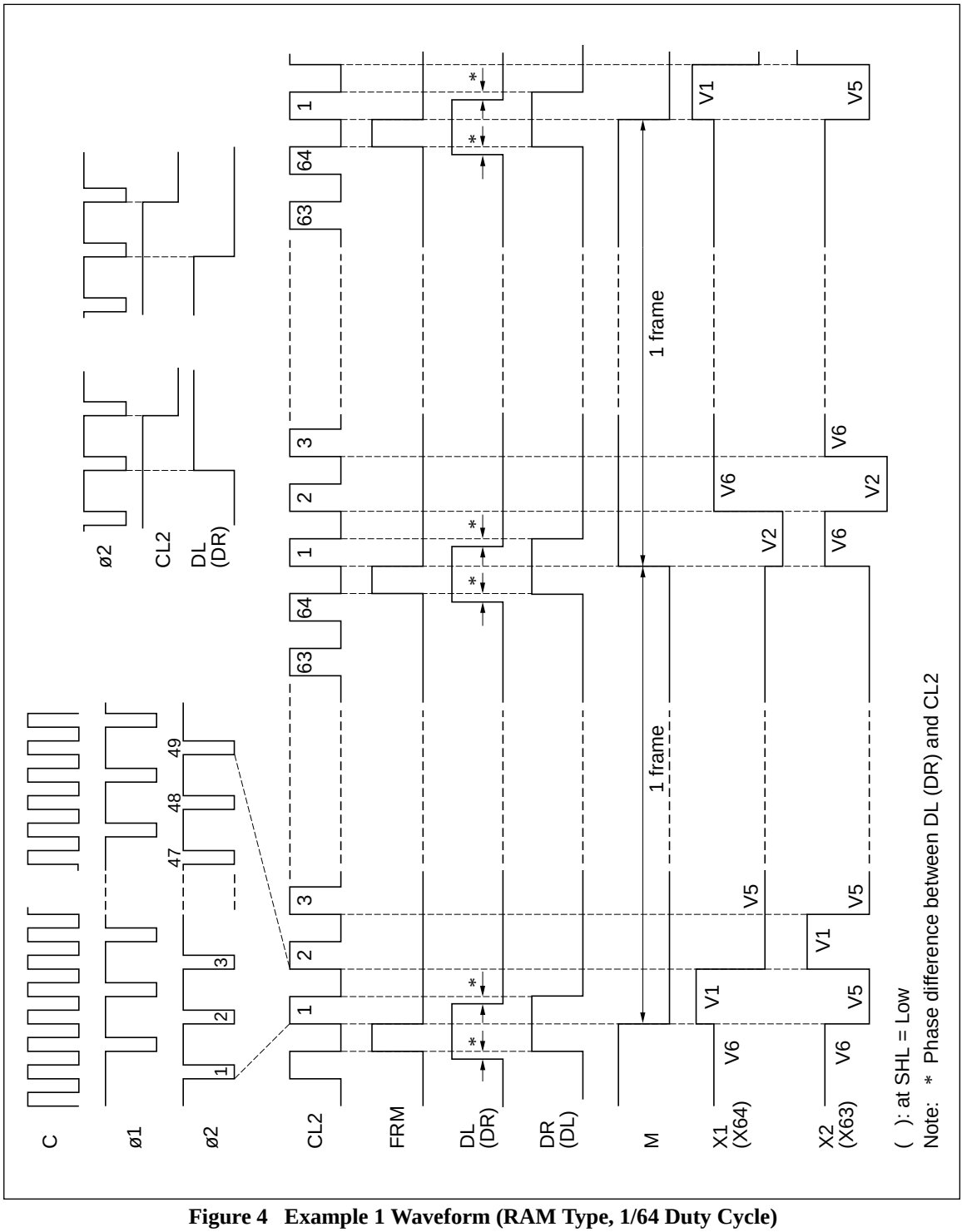


Figure 4 Example 1 Waveform (RAM Type, 1/64 Duty Cycle)

Connection Example 2

Use with HD61830 (Display Controller)

1. 1/64 duty ratio (see Connection List A)

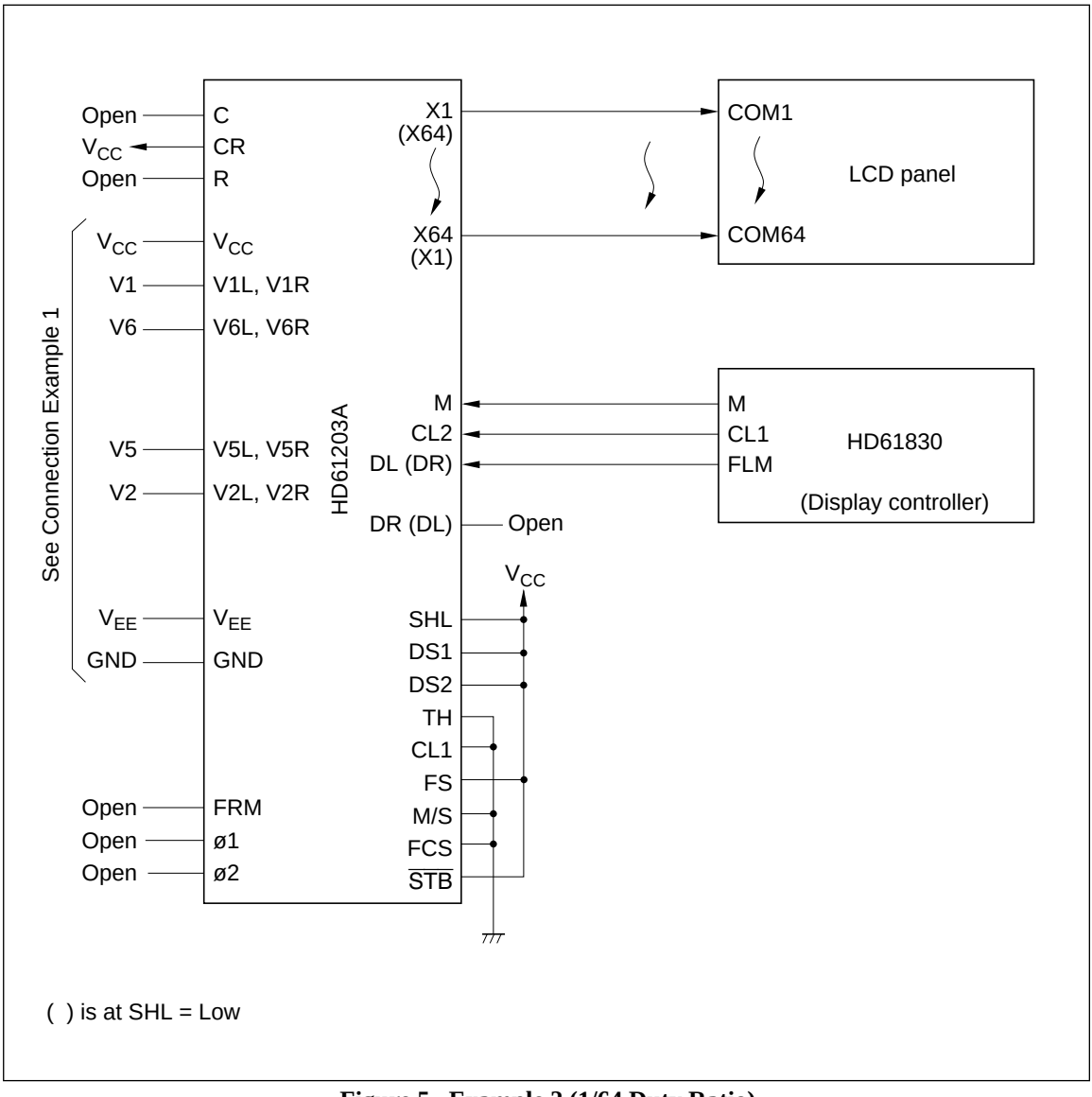


Figure 5 Example 2 (1/64 Duty Ratio)

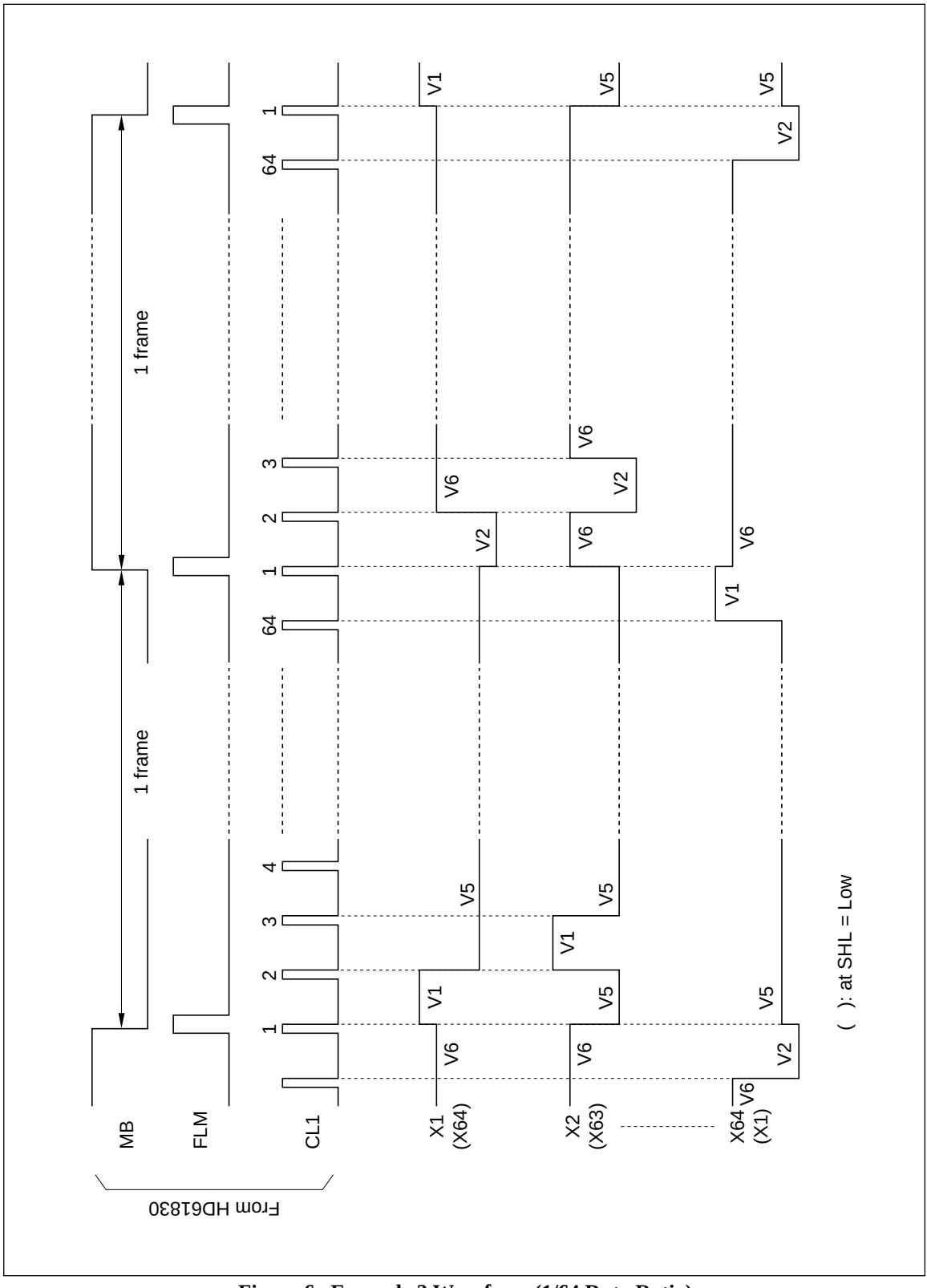


Figure 6 Example 2 Waveform (1/64 Duty Ratio)

2. 1/100 duty ratio (see Connection List B, C)

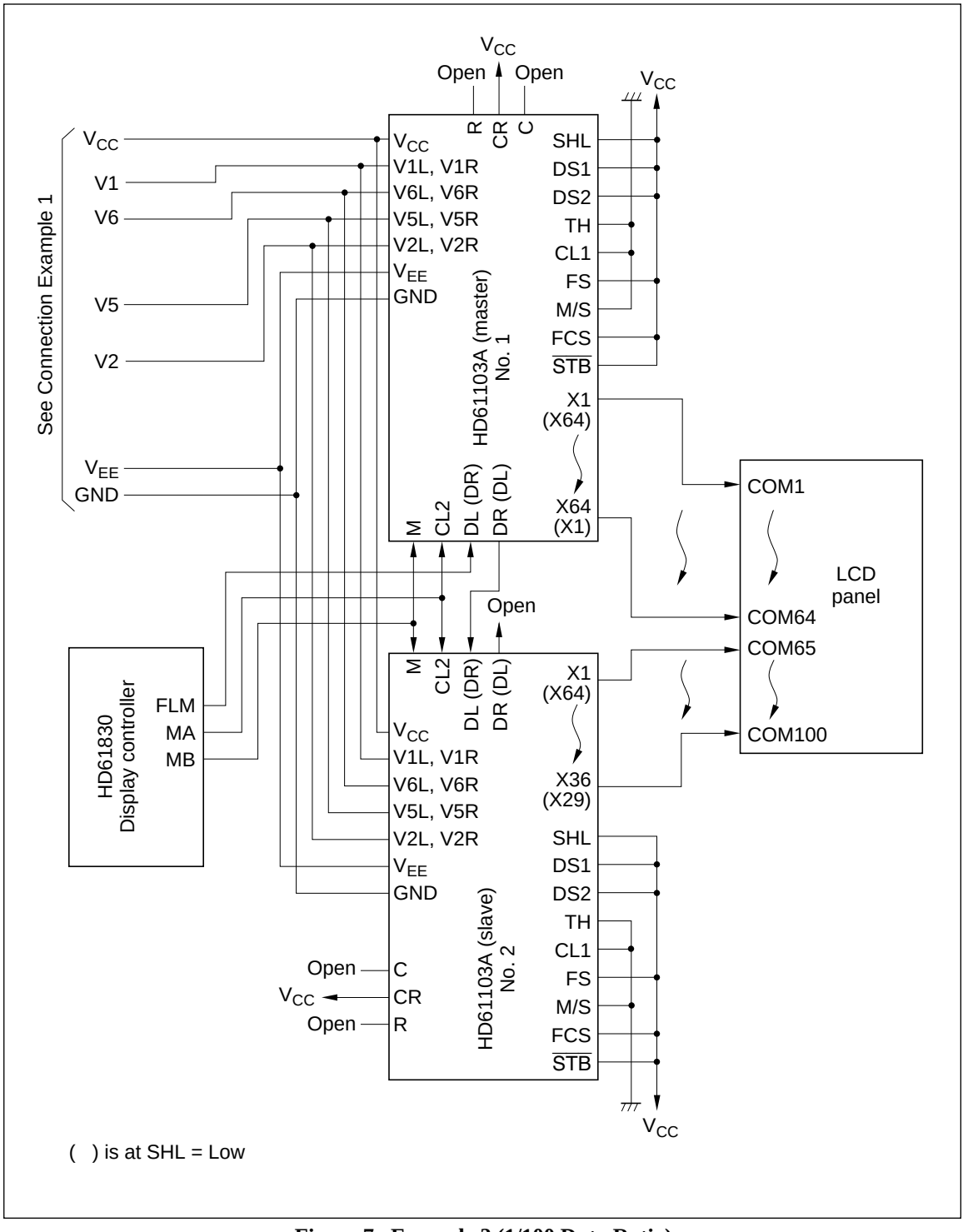


Figure 7 Example 2 (1/100 Duty Ratio)

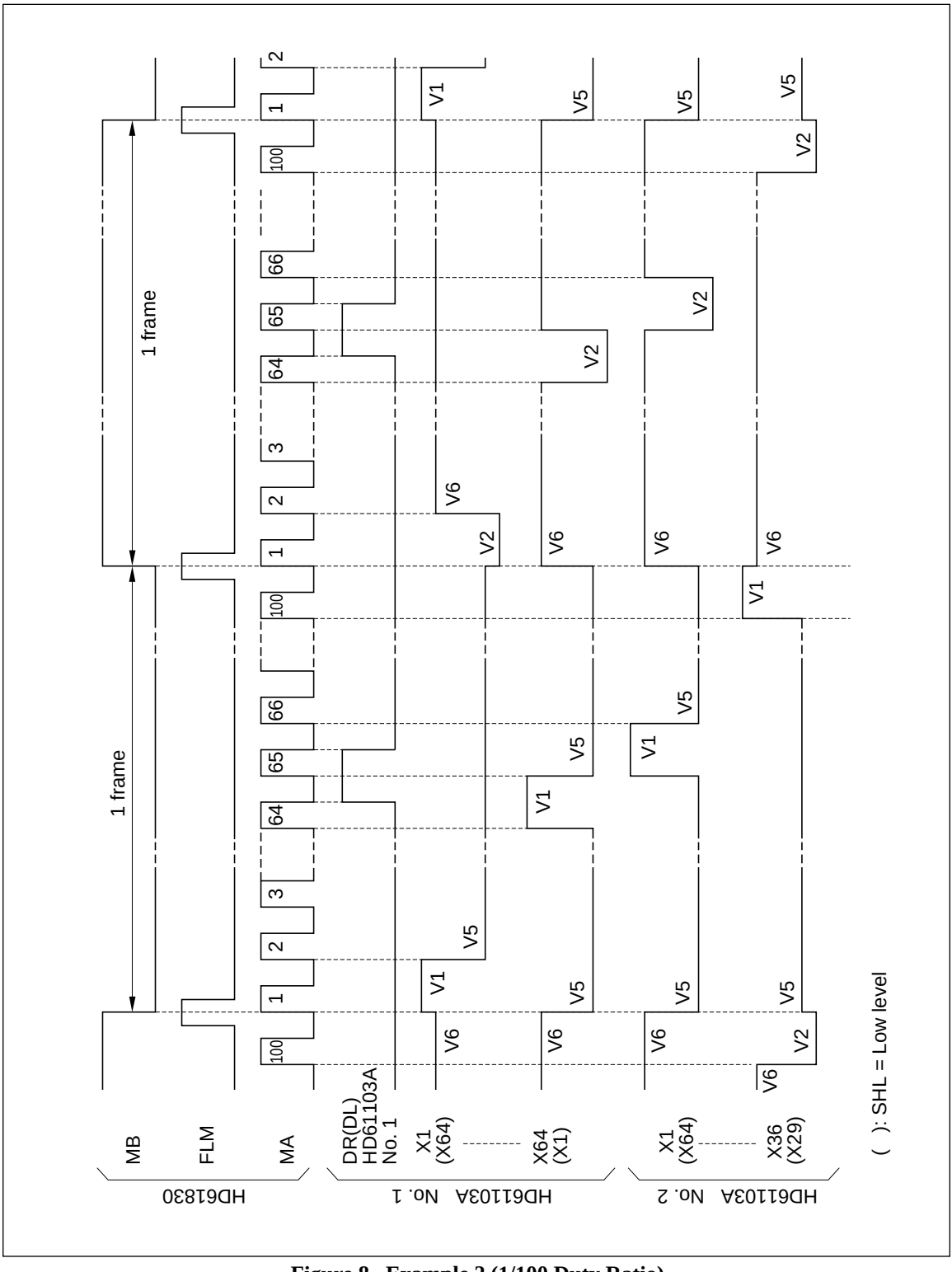


Figure 8 Example 2 (1/100 Duty Ratio)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O common terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.

   Maintain $V_{CC} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EE}$

Electrical Characteristics

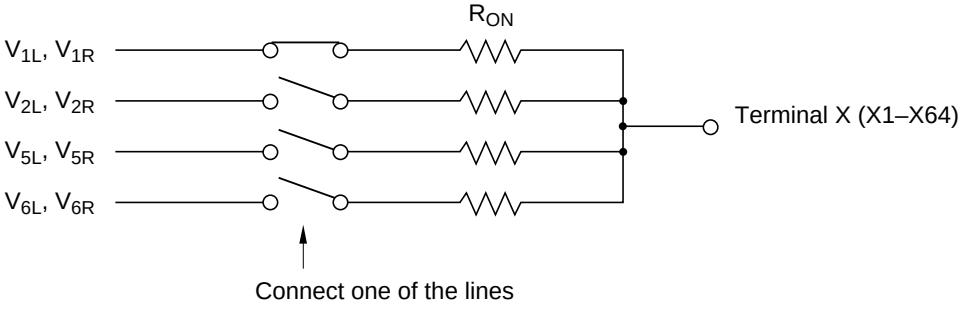
DC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –11.5 V, Ta = –20 to +75°C)

		Specifications					
Test Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Notes**
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low voltage	V_{OL}	—	—	+0.4	V	I_{OL} = +0.4 mA	2
Vi–Xj on resistance	R_{ON}	—	—	1.5	kΩ	$V_{CC} – V_{EE}$ = 10 V Load current ±150 µA	3
Input leakage current	I_{IL1}	–1.0	—	+1.0	µA	Vin = 0 to V_{CC}	4
Input leakage current	I_{IL2}	–2.0	—	+2.0	µA	Vin = V_{EE} to V_{CC}	5
Operating frequency	f_{opr1}	50	—	600	kHz	In master mode external clock operation	6
Operating frequency	f_{opr2}	50	—	1500	kHz	In slave mode shift register	7
Oscillation frequency	f_{osc}	315	450	585	kHz	Cf = 20 pF ± 5% Rf = 47 kΩ ± 2%	8, 13
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	9, 10
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	9, 11
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	9, 12

Notes: 1. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH and I/O terminals DL, M, DR and CL2 in the input state.

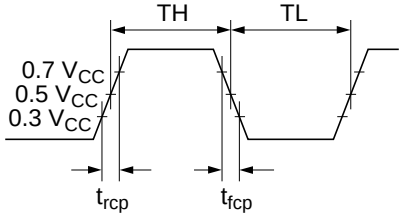
2. Applies to output terminals, ø1, ø2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output status.

3. Resistance value between terminal X (one of X1 to X64) and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) when load current is applied to each terminal X.
Equivalent circuit between terminal X and terminal V.

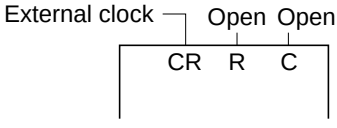


4. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH, I/O common terminals DL, M, DR and CL2 in the input status and NC terminals.
5. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R. Don't connect any lines to X1 to X64.
6. External clock is as follows.

External clock waveform

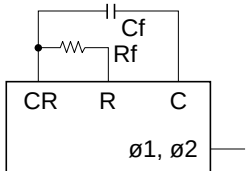


$$\text{Duty cycle} = \frac{TH}{TH + TL} \times 100\%$$



	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
t_{rcp}	—	—	50	ns
t_{fcp}	—	—	50	ns

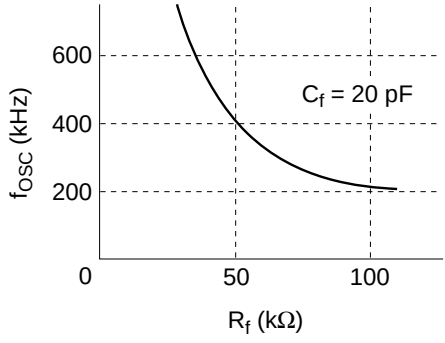
7. Applies to the shift register in the slave mode. For details, refer to AC characteristics.
8. Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency (fø) at ø1 or ø2.



Cf = 20 pF
Rf = 47 kΩ $\quad f_{OSC} = 2 \times f\text{ø}$

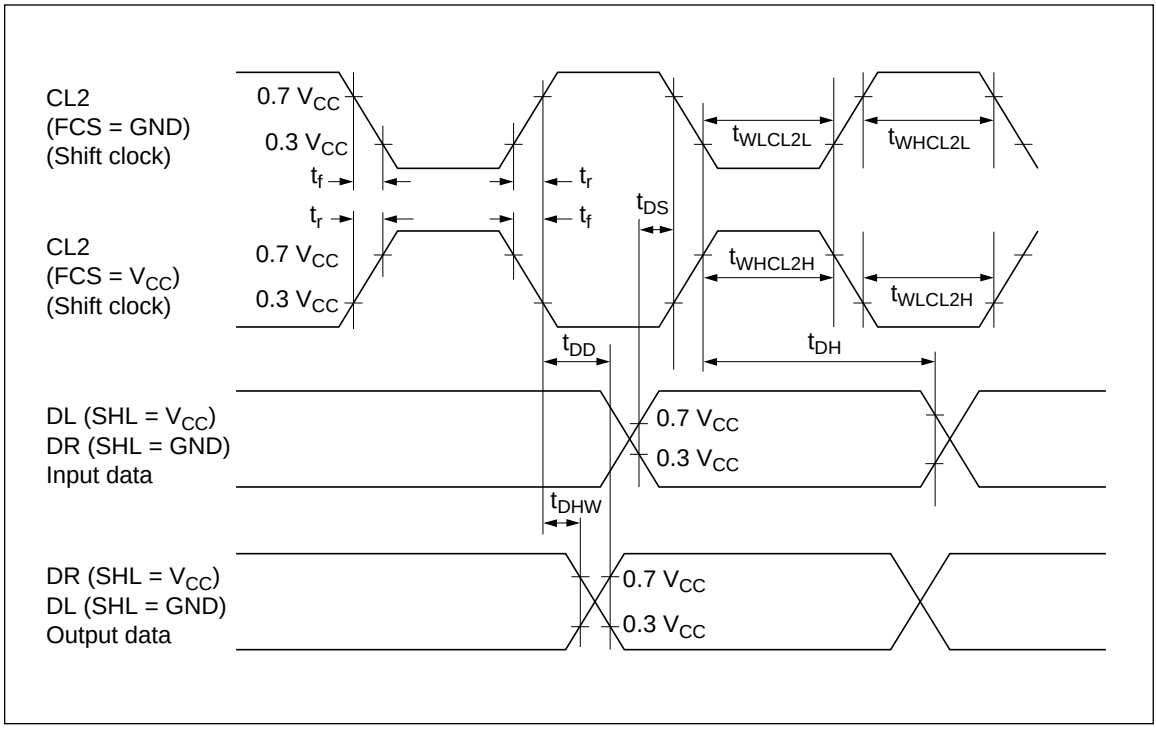
9. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and V_{IL} = GND.
10. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 8.
11. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61103A under the conditions described in note 10.
12. This value is specified for current flowing through V_{EE} under the condition described in note 10. Don't connect any lines to terminal V.

13. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.



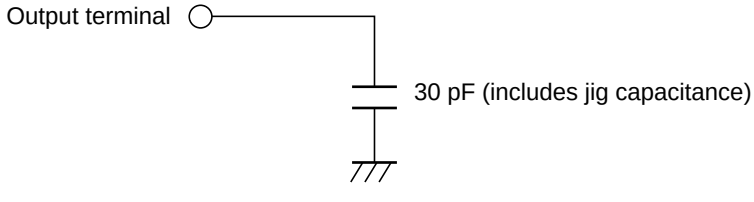
AC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –11.5 V, Ta = –20 to +75°C)

Slave Mode (M/S = GND)

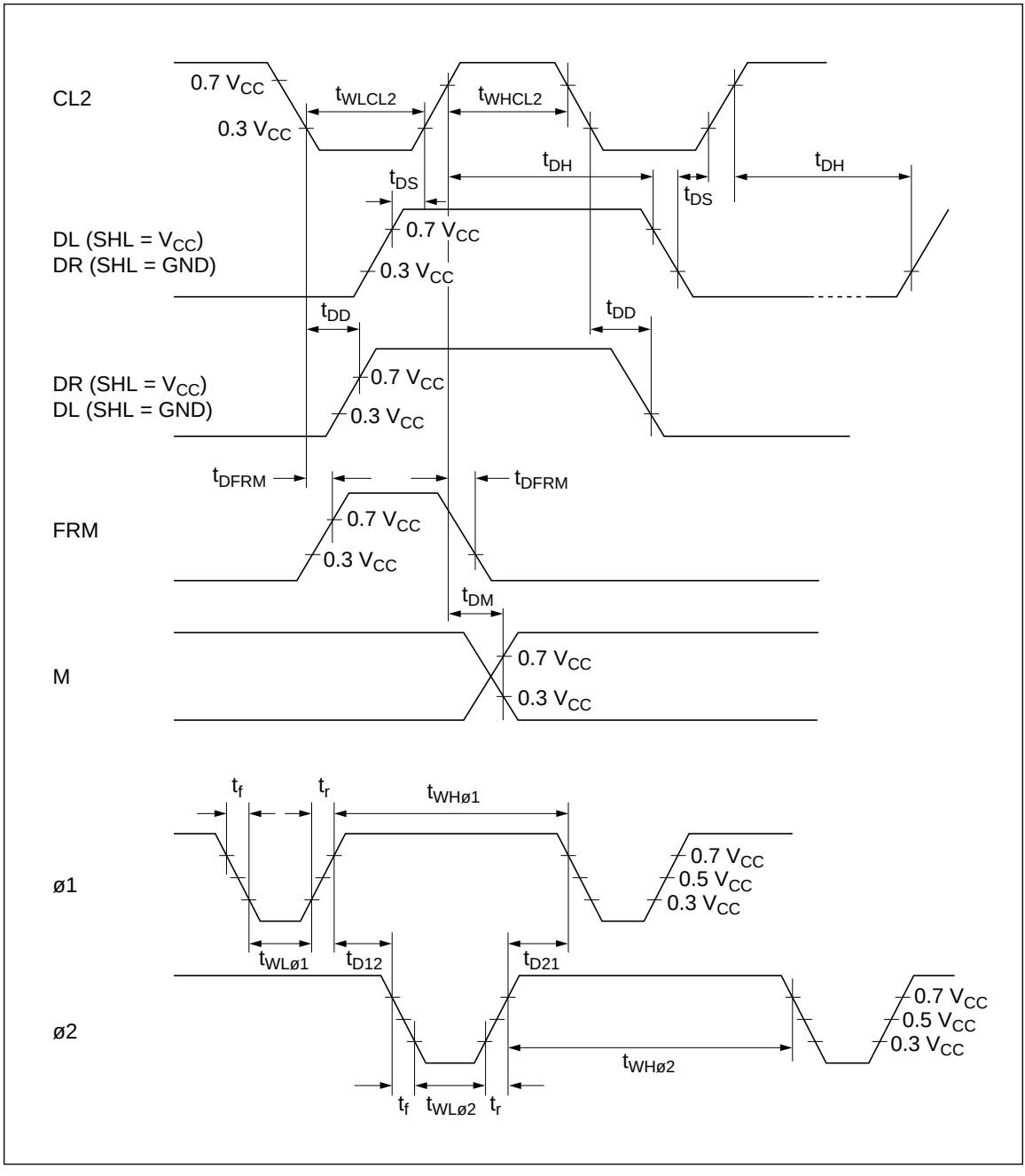


Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS = GND)	t_{WLCL2L}	450	—	—	ns	
CL2 high level width (FCS = GND)	t_{WHCL2L}	150	—	—	ns	
CL2 low level width (FCS = V_{CC})	t_{WLCL2H}	150	—	—	ns	
CL2 high level width (FCS = V_{CC})	t_{WHCL2H}	450	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	100	—	—	ns	
Data delay time	t_{DD}	—	—	200	ns	1
Data hold time	t_{DHW}	10	—	—	ns	
CL2 rise time	t_r	—	—	30	ns	
CL2 fall time	t_f	—	—	30	ns	

Note: 1. The following load circuit is connected for specification.



Master Mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)



Item	Symbol	Min	Typ	Max	Unit
Data setup time	t_{DS}	20	—	—	µs
Data hold time	t_{DH}	40	—	—	µs
Data delay time	t_{DD}	5	—	—	µs
FRM delay time	t_{DFRM}	–2	—	+2	µs
M delay time	t_{DM}	–2	—	+2	µs
CL_2 low level width	t_{WLCL2}	35	—	—	µs
CL_2 high level width	t_{WHCL2}	35	—	—	µs
ø1 low level width	$t_{WLø1}$	700	—	—	ns
ø2 low level width	$t_{WLø2}$	700	—	—	ns
ø1 high level width	$t_{WHø1}$	2100	—	—	ns
ø2 high level width	$t_{WHø2}$	2100	—	—	ns
ø1–ø2 phase difference	t_{D12}	700	—	—	ns
ø2–ø1 phase difference	t_{D21}	700	—	—	ns
ø1, ø2 rise time	t_r	—	—	150	ns
ø1, ø2 fall time	t_f	—	—	150	ns

HD61202

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

HITACHI

Description

HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro controller in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of a dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

The HD61202, which is produced in the CMOS process, can complete portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61203.

Features

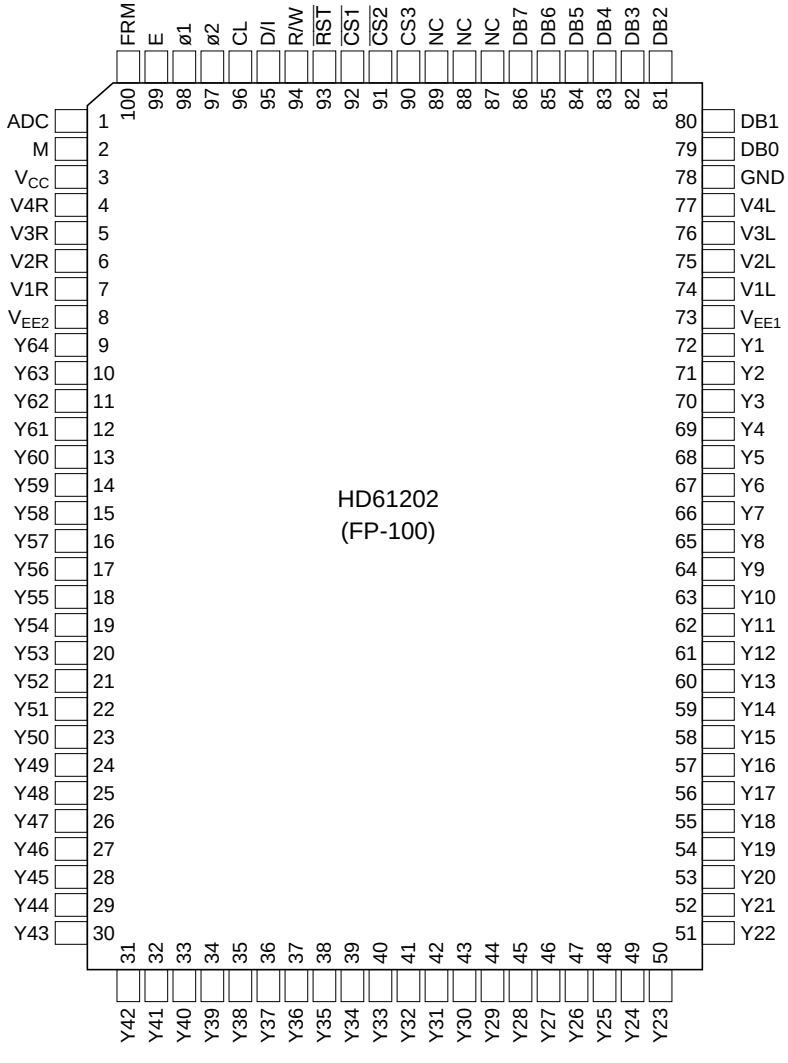
- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  - — RAM bit data 1: On
  - — RAM bit data 0: Off
- Internal display RAM address counter preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty cycle
  Drives liquid crystal panels with 1/32–1/64 duty cycle multiplexing
- Wide range of instruction function
  Display data read/write, display on/off, set address, set display start line, read status
- Lower power dissipation: during display 2 mW max
- Power supply: V_{CC}: 5 V ± 10%
- Liquid crystal display driving voltage: 8 V to 17 V
- CMOS process

Ordering Information

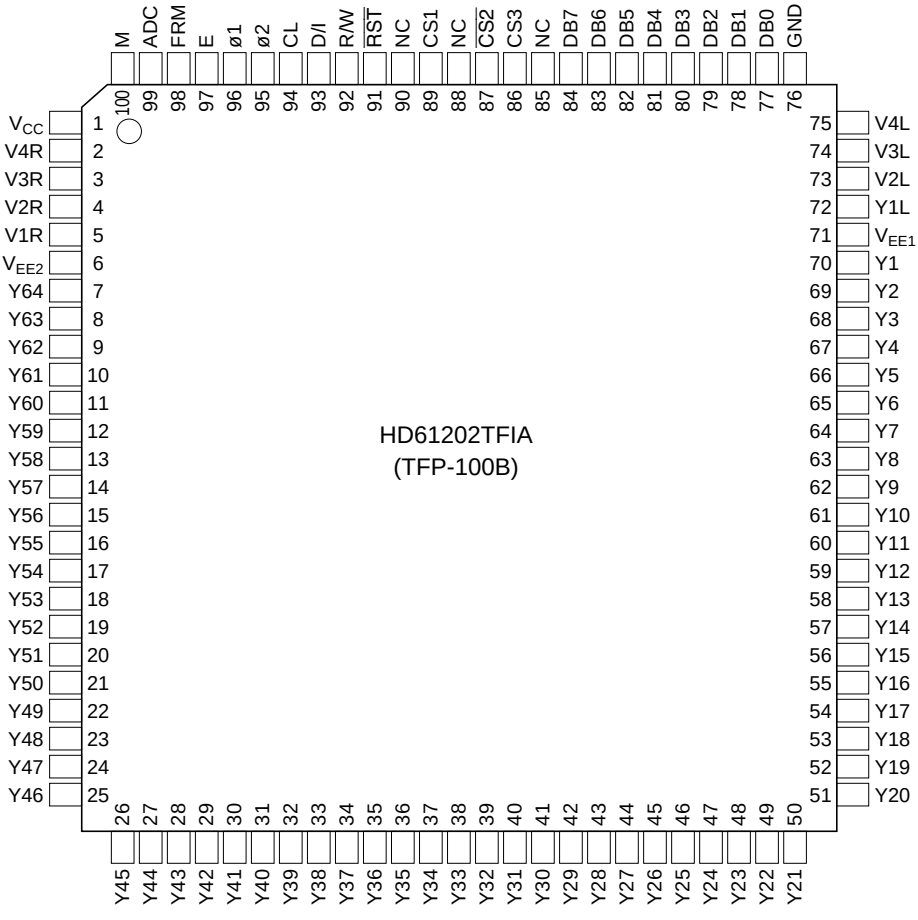
Type No.	Package
HD61202	100-pin plastic QFP (FP-100)
HD61202TFIA	100-pin thin plastic QFP (TFP-100B)
HD61202D	Chip

Hitachi semiconductor

Pin Arrangement

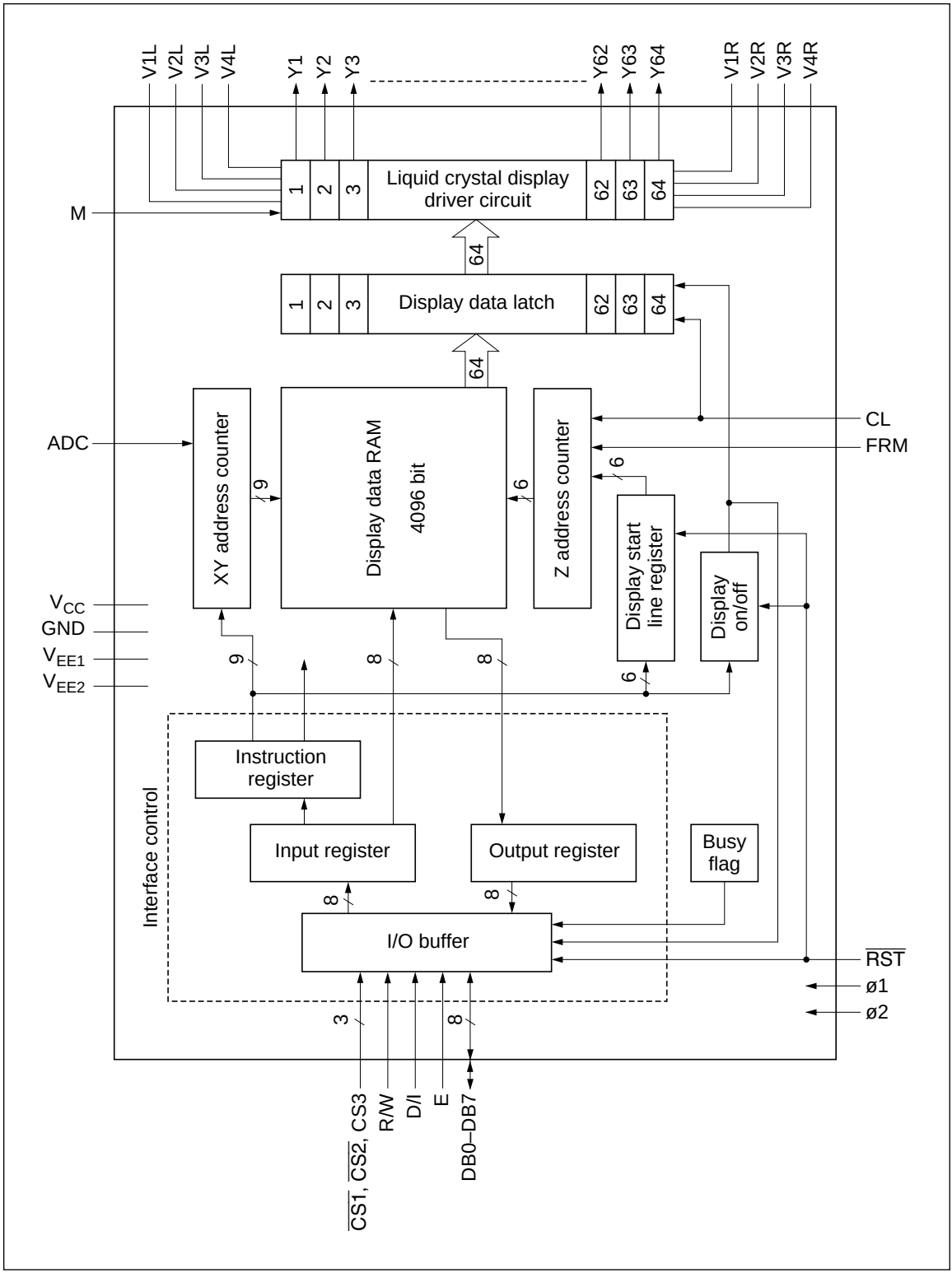


(Top view)


M
ADC
FRM
E
ø1
ø2
CL
D/I
R/W
RST
NC
CS1
NC
CS2
CS3
NC
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
GND
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
V_{CC} 1
V4R 2
V3R 3
V2R 4
V1R 5
V_{EE2} 6
Y64 7
Y63 8
Y62 9
Y61 10
Y60 11
Y59 12
Y58 13
Y57 14
Y56 15
Y55 16
Y54 17
Y53 18
Y52 19
Y51 20
Y50 21
Y49 22
Y48 23
Y47 24
Y46 25
75 V4L
74 V3L
73 V2L
72 Y1L
71 V_{EE1}
70 Y1
69 Y2
68 Y3
67 Y4
66 Y5
65 Y6
64 Y7
63 Y8
62 Y9
61 Y10
60 Y11
59 Y12
58 Y13
57 Y14
56 Y15
55 Y16
54 Y17
53 Y18
52 Y19
51 Y20
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
Y45 Y44 Y43 Y42 Y41 Y40 Y39 Y38 Y37 Y36 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 Y25 Y24 Y23 Y22 Y21
HD61202TFIA
(TFP-100B)

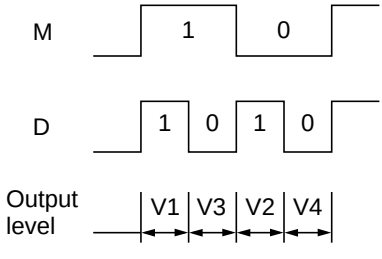
(Top view)

Block Diagram



Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is: GND = 0 V V_{CC} = 5 V ± 10%
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is $V_{CC} - V_{EE}$ = 8 to 17 V. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal name: $\overline{CS1}$ $\overline{CS2}$ CS3 Condition: L L H
E	1	I	MPU	Enable. At write (R/W = low): Data of DB0 to DB7 is latched at the fall of E. At read (R/W = high): Data appears at DB0 to DB7 while E is at high level.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the MPU. When E = high, CS1, CS2 = low and CS3 = high. R/W = Low: DB0 to DB7 can accept at fall of E when CS1, CS2 = low and CS3 = high.
D/I	1	I	MPU	Data/instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1: $0, Y64: $63 ACD = Low: Y64: $0, Y1: $63
DB1–DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61203	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes the common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203	Synchronous signal to latch display data. The rising CL signal increments the display output address counter and latches the display data.
ø1, ø2	2	I	HD61203	2-phase clock signal for internal operation. The ø1 and ø2 clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1–Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. The outputs at these pins are at the light-on level when the display RAM data is 1, and at the light-off level when the display RAM data is 0. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	MPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level. 1. On/off register 0 set (display off) 2. Display start line register line 0 set (displays from line 0) After releasing reset, this condition can be changed only by instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

I/O Buffer: Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (most significant bit)
DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC; that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively of $\overline{CS1}$ to CS3.

Register: Both input register and output register are provided to interface to an MPU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

1. Input register

   The input register is used to store data temporarily before writing it into display data RAM.

   The data from MPU is written into input register, then into display data RAM automatically by internal operation. When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of the E signal.

2. Output register

   The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With the read display data instruction, data stored in the output register is output while E is high level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.

   The contents in the output register are rewritten by the read display data instruction, but are held by address set instruction, etc.

   Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 1 shows the MPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

Busy Flag

Busy flag = 1 indicates that HD61202 is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing instructions.

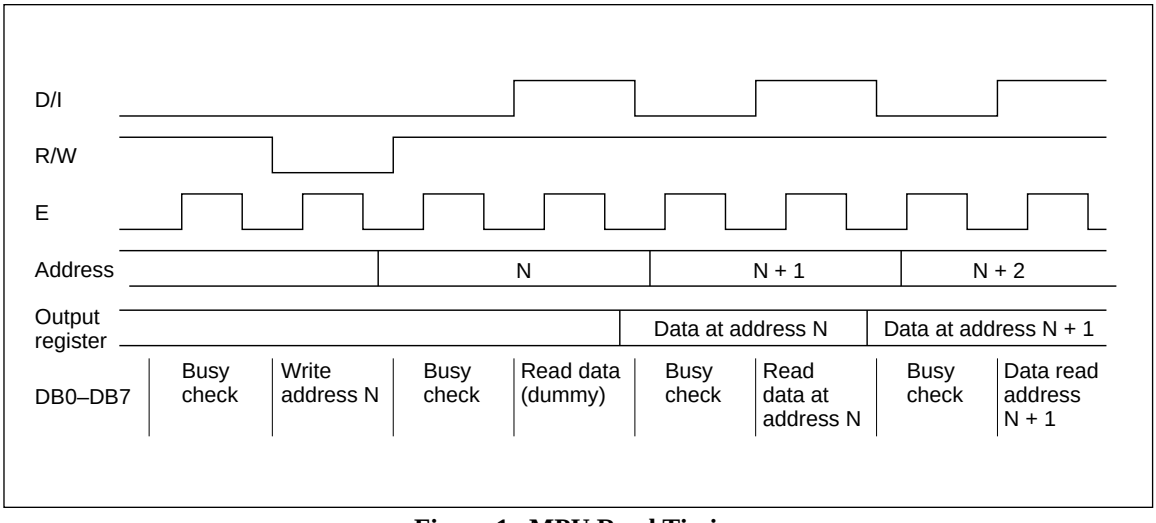


Figure 1 MPU Read Timing

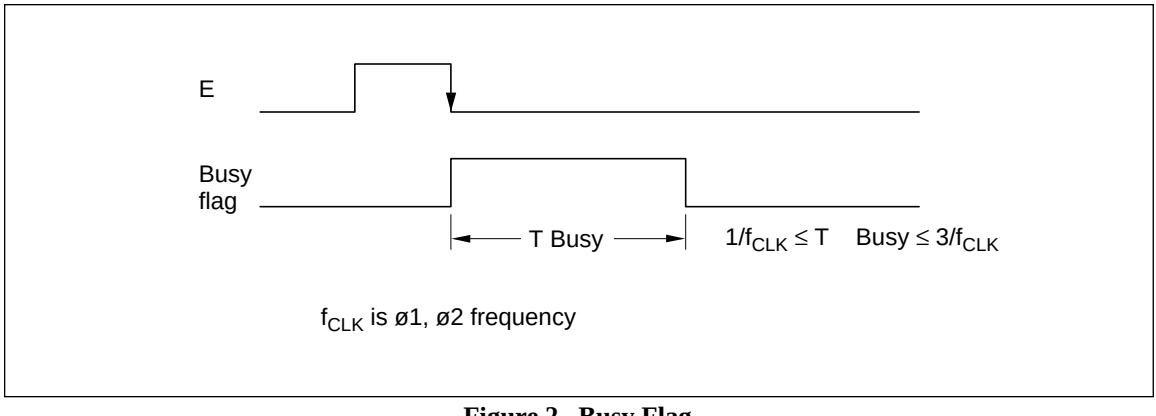


Figure 2 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by status read instruction. Display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CL signal (display synchronous signal) should be input correctly.

Display Start Line Register

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction. When high level of the FRM signal starts the display, the information in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. X address counter

   Ordinary register with no count functions. An address is set by instruction.

2. Y address counter

   An Address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

As the ADC signal controls the Y address counter, reversing of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Figure 3 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

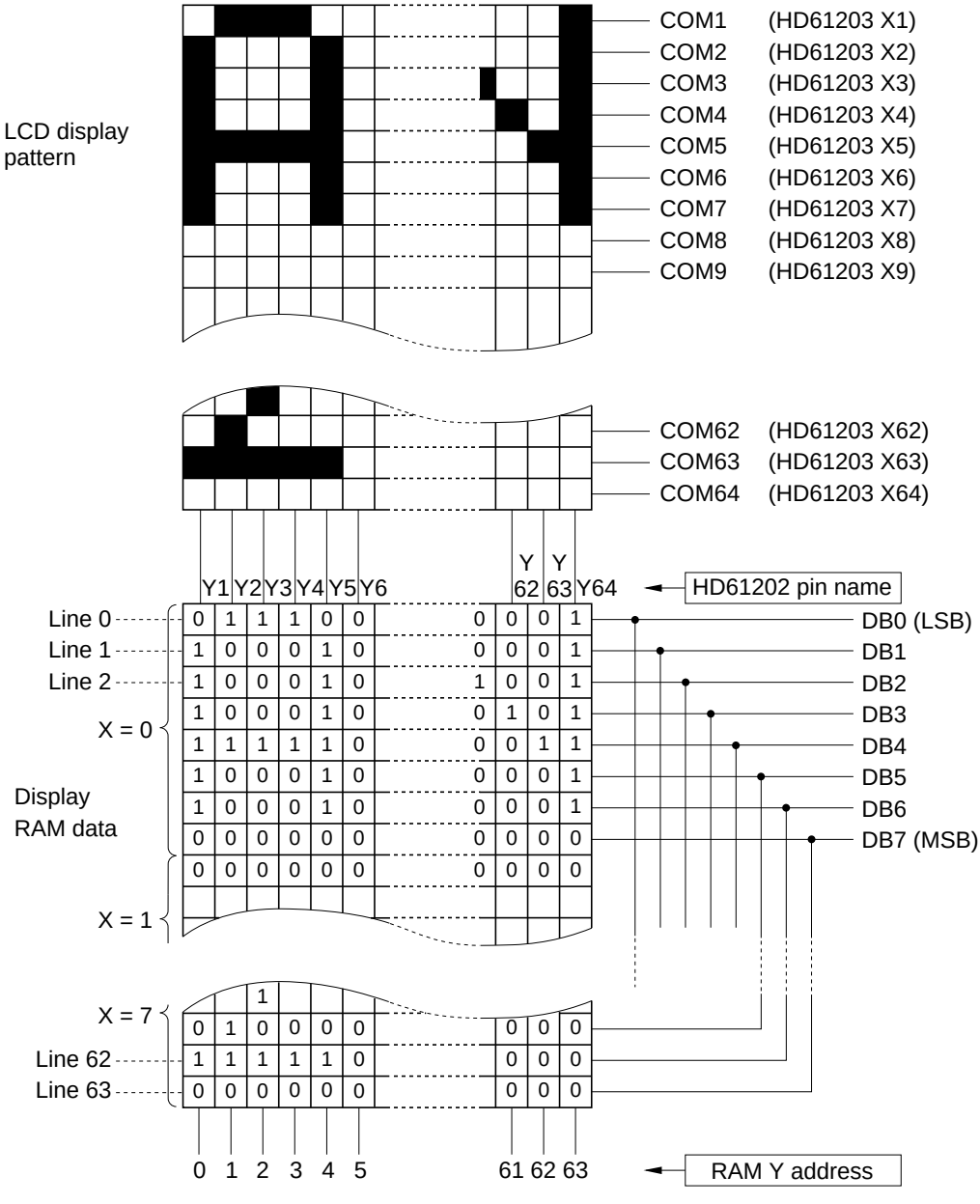


Figure 3 Relation between RAM Data and Display

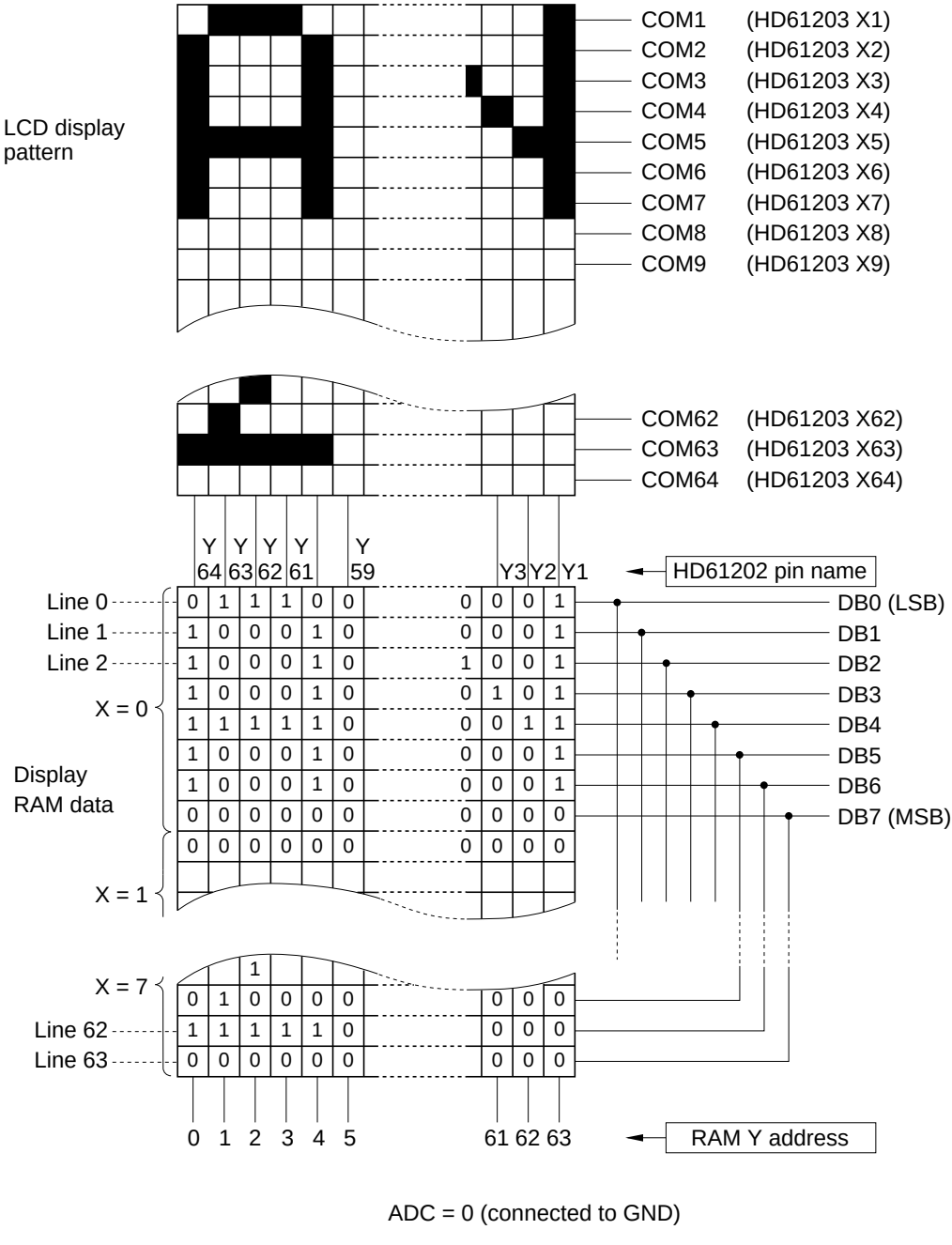


Figure 3 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is present at the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal at low level when turning power on.

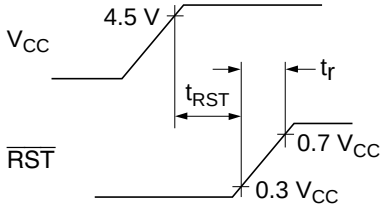
1. Display off
2. Set display start line register line 0.

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction. The conditions of power supply at initial power up are shown in table 2.

Table 2 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 3 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MPU.

These explanations are detailed in the following pages. Generally, there are following three kinds of instructions:

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is proof that an instruction is not being executed.

Table 3 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.	
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.	
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register.	
Set Y address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.	
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note: Busy time varies with the frequency (f_{CLK}) of ø1, and ø2.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

Display On/Off

	R/W	D/I	DB7	·····	DB0
Code	0	0	0	0	1	1	1	1	1	D
			MSB							LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display Start Line

	R/W	D/I	DB7	·····	DB0
Code	0	0	1	1	A	A	A	A	A	A
			MSB							LSB

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 4 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Set Page (X Address)

	R/W	D/I	DB7	·····	DB0
Code	0	0	1	0	1	1	1	A	A	A
			MSB							LSB

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 5.

Set Y Address

	R/W	D/I	DB7	·····	DB0
Code	0	0	0	1	A	A	A	A	A	A
			MSB							LSB

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7	·····	DB0
Code	1	0	Busy	0	ON/OFF	RESET	0	0	0	0
			MSB							LSB

- Busy

  When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instruction.

- ON/OFF

  Shows the liquid crystal display conditions: on condition or off condition.

  When on/off is 1, the display is in off condition. When on/off is 0, the display is in on condition.

- RESET

  RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

  RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

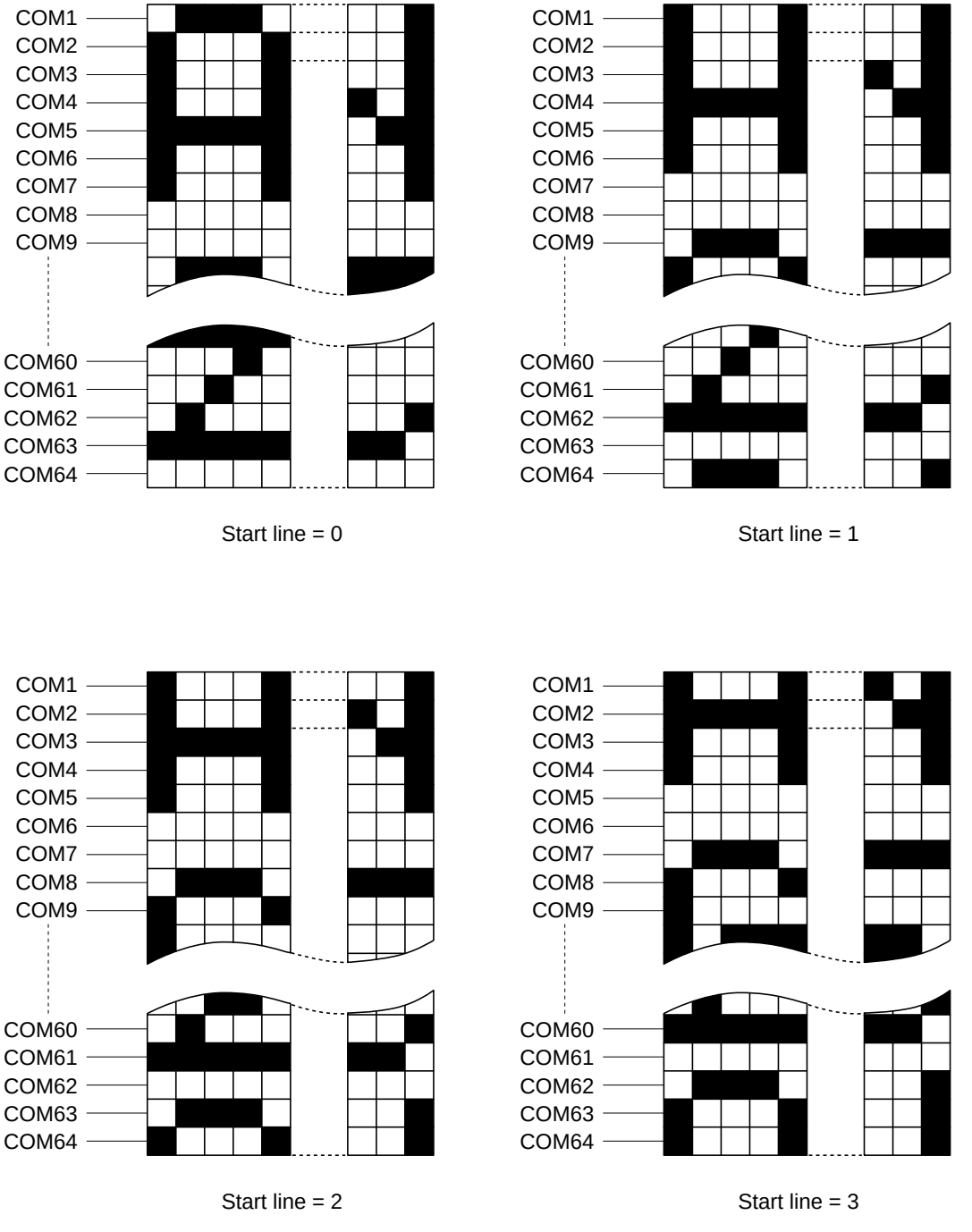


Figure 4 Relation between Start Line and Display

Write Display Data

	R/W	D/I	DB7	·····	DB0
Code	0	1	D	·····	D
			MSB		LSB

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W	D/I	DB7	·····	DB0
Code	1	1	D	·····	D
			MSB		LSB

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in “Function of Each Block”.

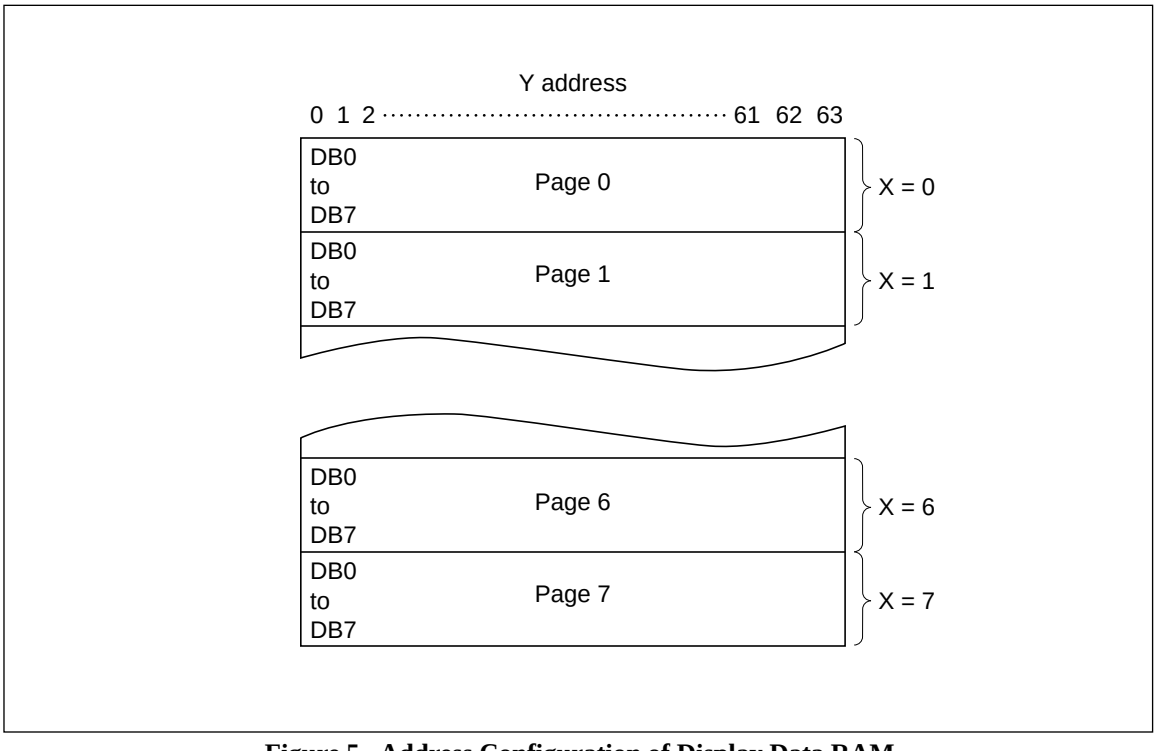
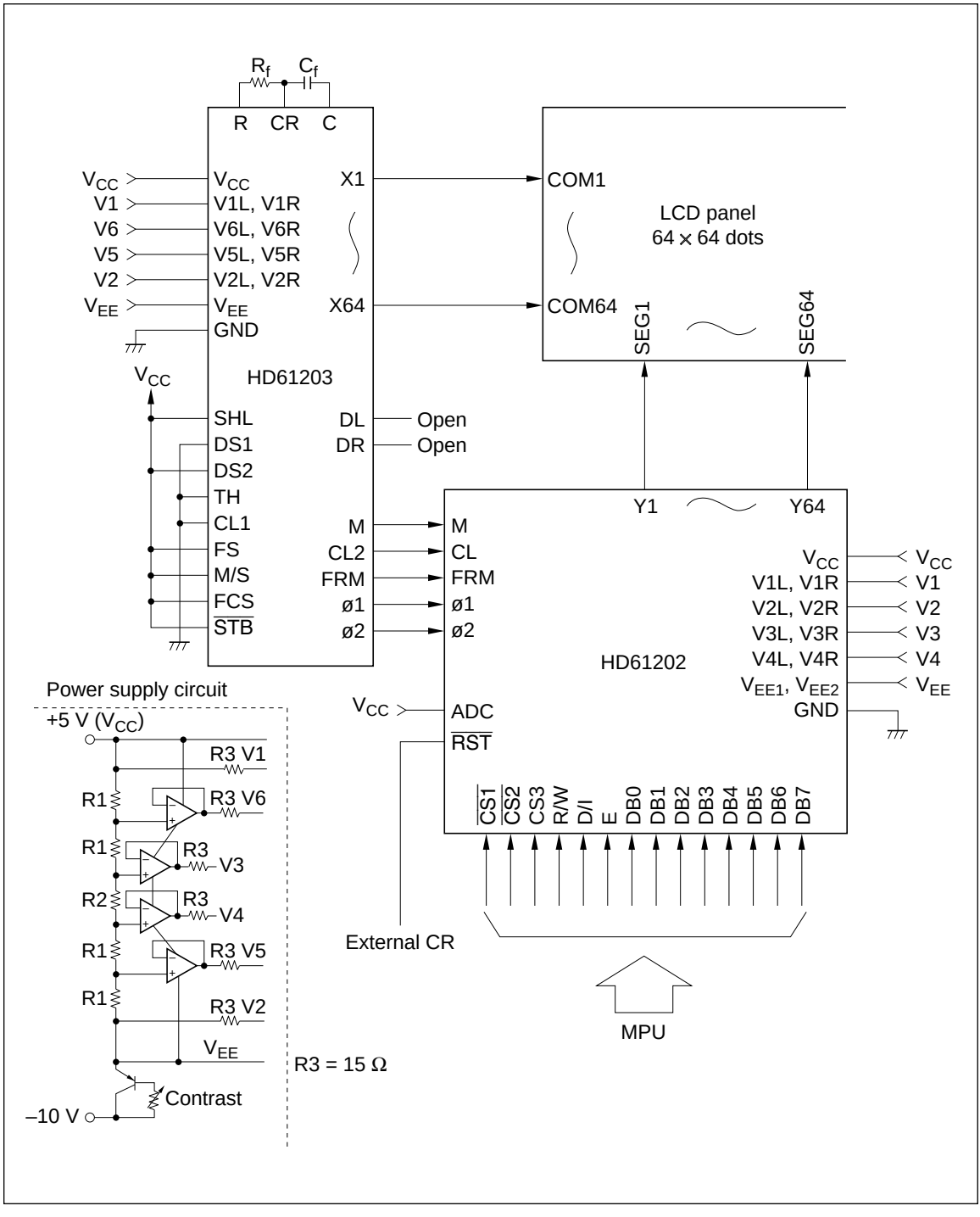
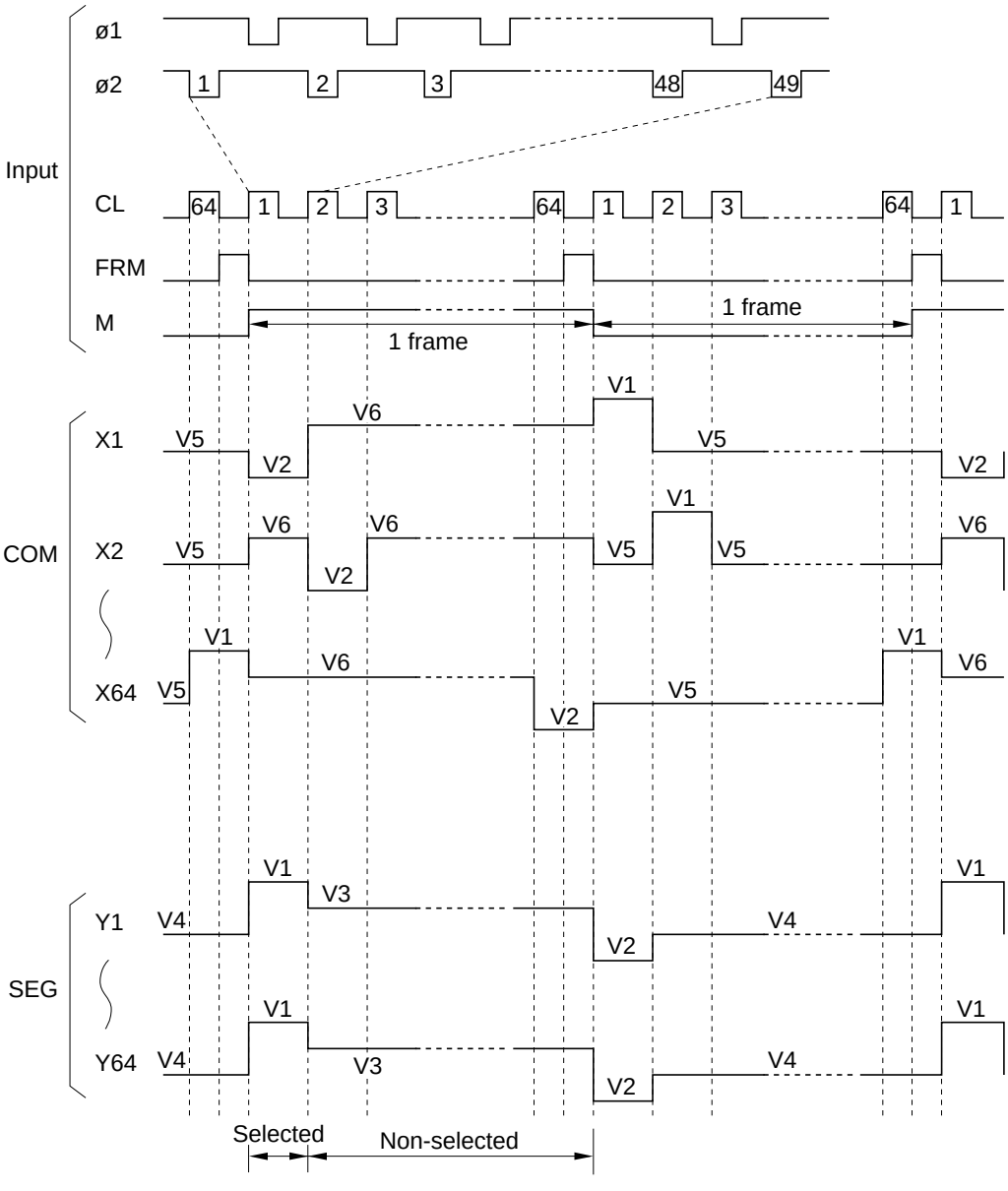


Figure 5 Address Configuration of Display Data RAM

Use of HD61202

Interface with HD61203 (1/64 Duty Cycle)





The waveforms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Figure 6 LCD Driver Timing Chart (1/64 Duty Cycle)

Interface with CPU

1. Example of Connection with HD6800

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61202 by reading/ writing the data at these addresses.

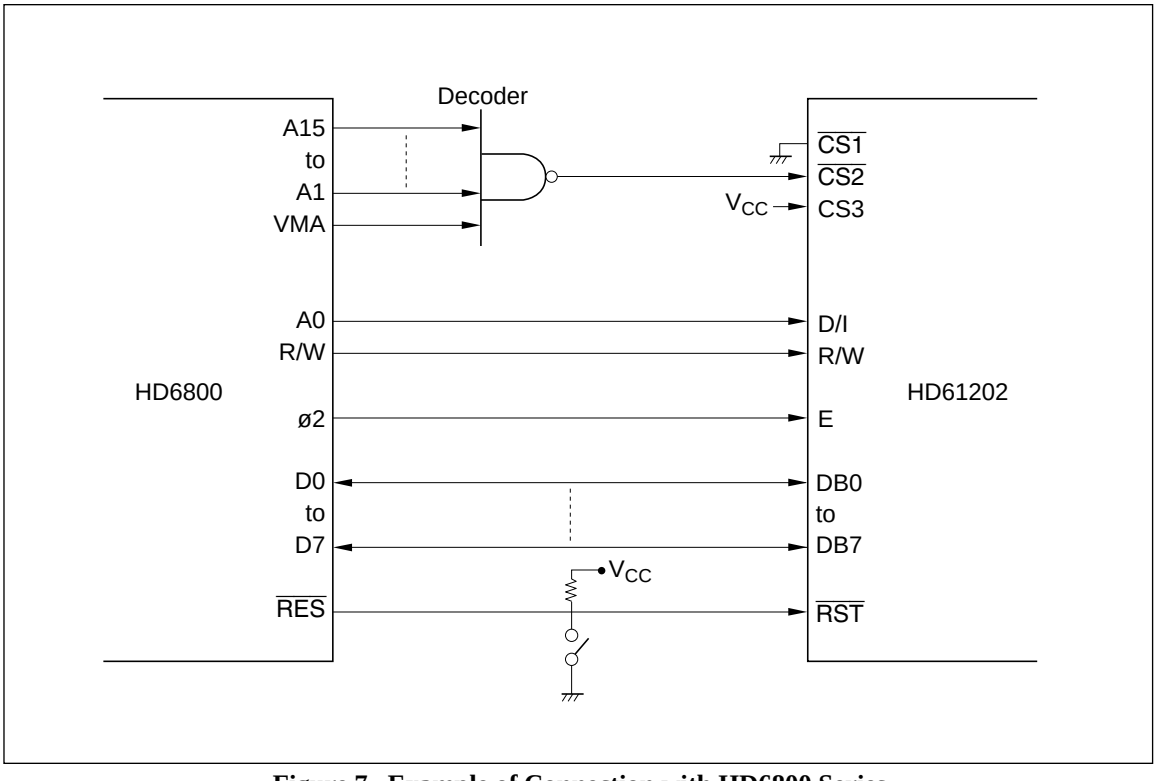


Figure 7 Example of Connection with HD6800 Series

2. Example of Connection with HD6801

- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

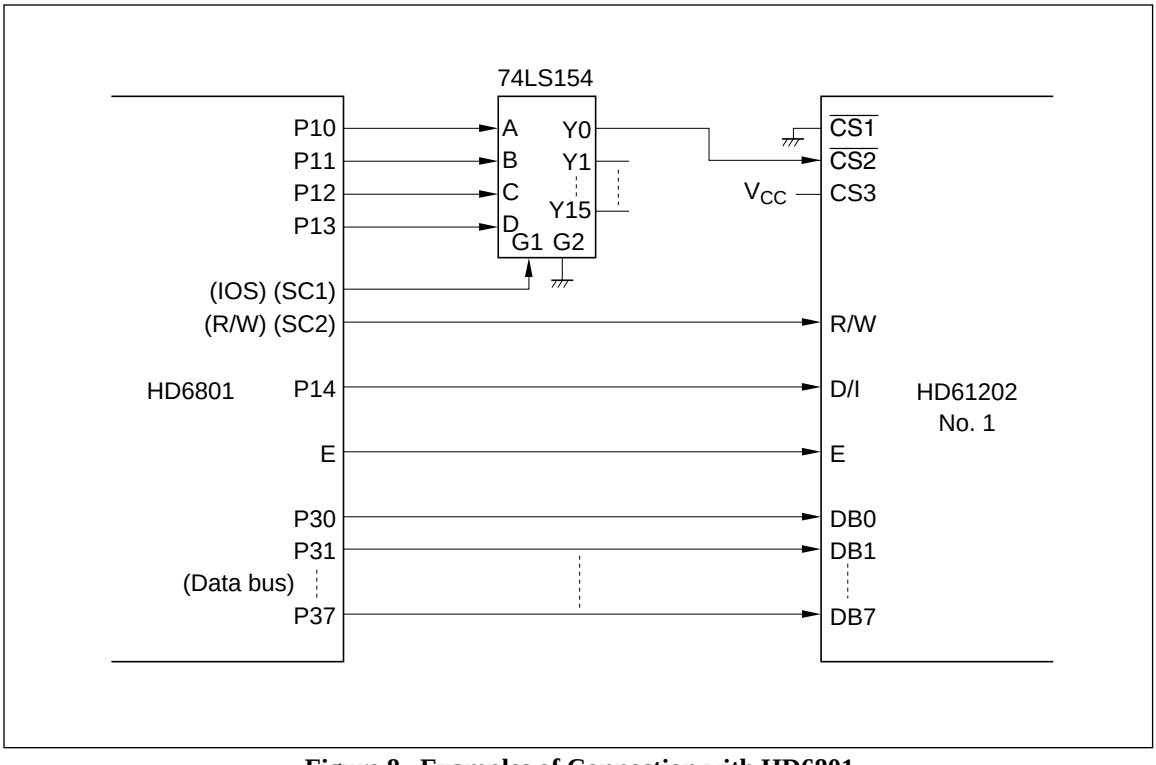


Figure 8 Examples of Connection with HD6801

Example of Application

In this example, two HD61203s output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

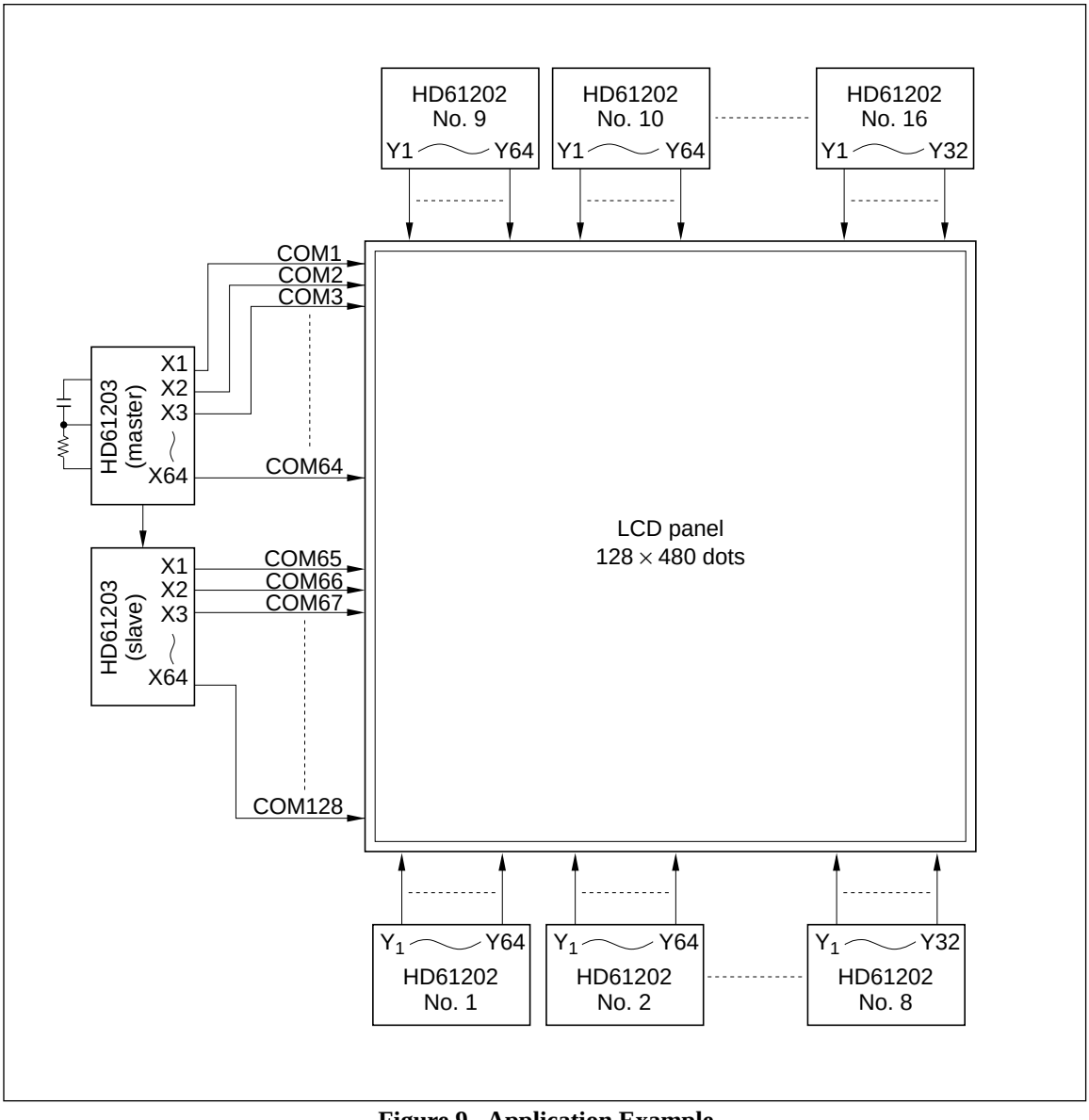


Figure 9 Application Example

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} – 19.0 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminal voltage (2)	V_{T2}	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them within the recommended operation conditions.
Useing them beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
Maintain
$V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, ø1, ø2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.

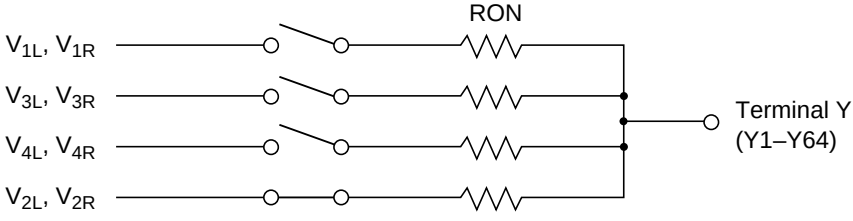
Electrical Characteristics (GND = 0 V, V_{CC} = 4.5 to 5.5 V, $V_{CC} - V_{EE}$ = 8 to 17.0 V, Ta = –20 to +75°C)

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IHC}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	$0.3 \times V_{CC}$	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND – V_{CC}	4
Three-state (off) input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND – V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE} – V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	$V_{CC} - V_{EE}$ = 15 V $\pm I_{LOAD}$ = 0.1 mA	8
Dissipation current	$I_{CC}(1)$	—	—	100	µA	During display	7
	$I_{CC}(2)$	—	—	500	µA	During access access cycle = 1 MHz	7

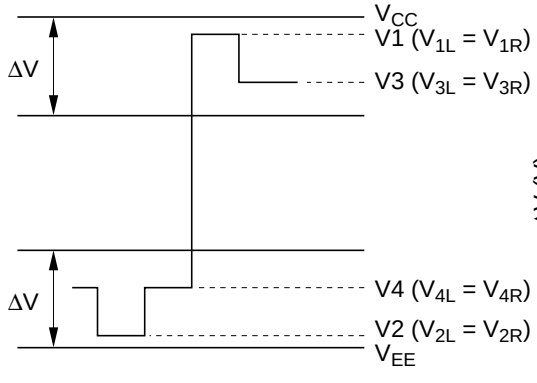
Notes: 1. Applies to M, FRM, CL, $\overline{RST}$, ø1, and ø2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Specified when liquid crystal display is in 1/64 duty cycle mode.
   Operation frequency: f_{CLK} = 250 kHz (ø1 and ø2 frequency)
   Frame frequency: f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: Not loaded
   Input level: $V_{IH} = V_{CC}$ (V)
   V_{IL} = GND (V)
   Measured at V_{CC} terminal

8. Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition:

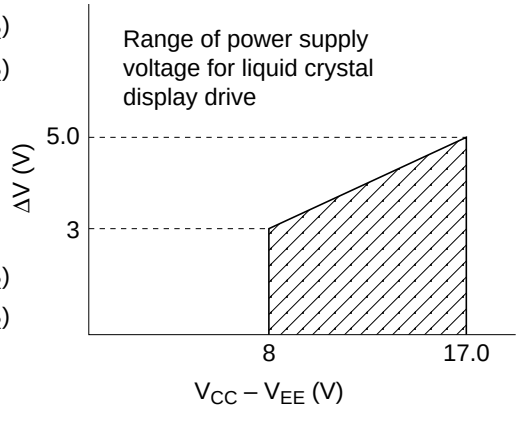
$$V_{CC} - V_{EE} = 15.0\ V$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{CC} + 2/7\ (V_{CC} - V_{EE})$$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



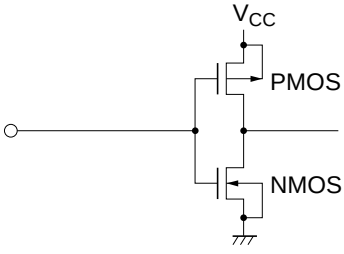
Correlation between driver output waveform and power supply voltages for liquid crystal display drive



Correlation between power supply voltage $V_{CC} - V_{EE}$ and ΔV

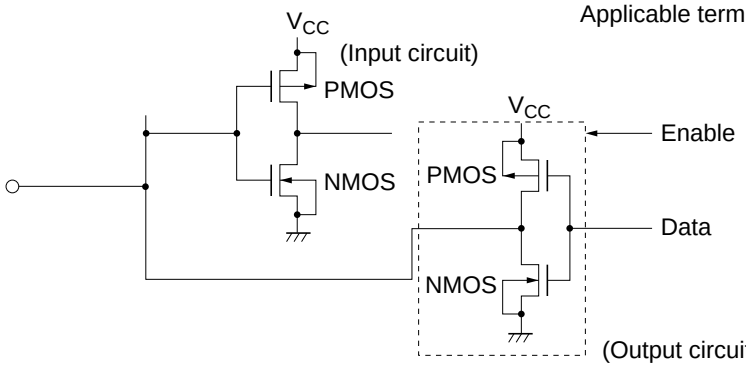
Terminal Configuration

Input Terminal



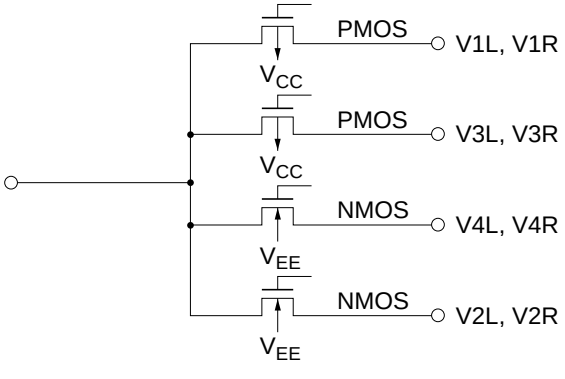
Applicable terminals:
M, FRM, CL, $\overline{RST}$, ø1, ø2, $\overline{CS1}$, $\overline{CS2}$, CS3,
E, R/W, D/I, ADC

Input/Output Terminal



Applicable terminals: DB0–DB7

Output Terminal



Applicable terminals:
Y1–Y64

Interface AC Characteristics

MPU Interface (GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	Fig. 10, Fig. 11
E high level width	P_{WEH}	450	—	—	ns	
E low level width	P_{WEL}	450	—	—	ns	
E rise time	t_r	—	—	25	ns	
E fall time	t_f	—	—	25	ns	
Address setup time	t_{AS}	140	—	—	ns	
Address hold time	t_{AH}	10	—	—	ns	
Data setup time	t_{DSW}	200	—	—	ns	Fig. 10
Data delay time	t_{DDR}	—	—	320	ns	Fig. 11, Fig. 12
Data hold time (write)	t_{DHW}	10	—	—	ns	Fig. 10
Data hold time (read)	t_{DHR}	20	—	—	ns	Fig. 11

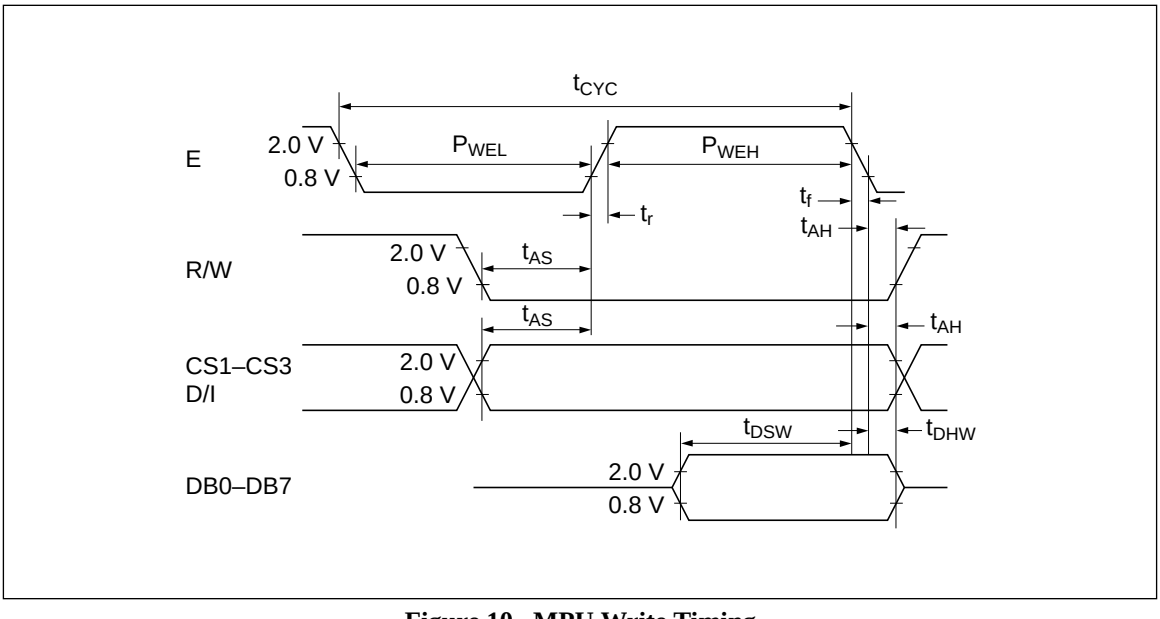


Figure 10 MPU Write Timing

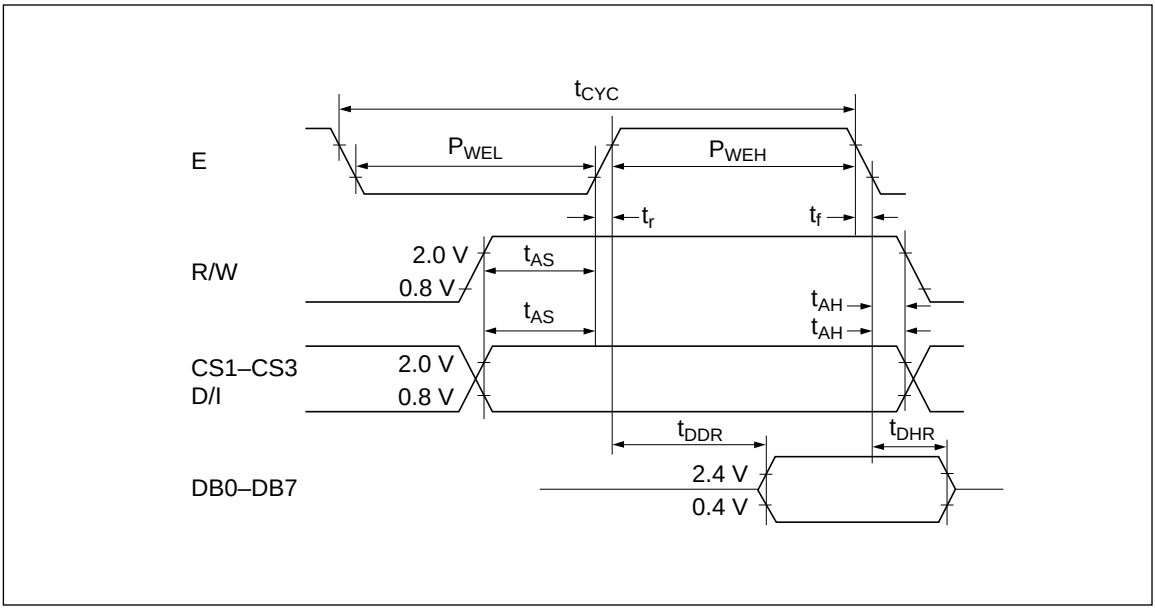
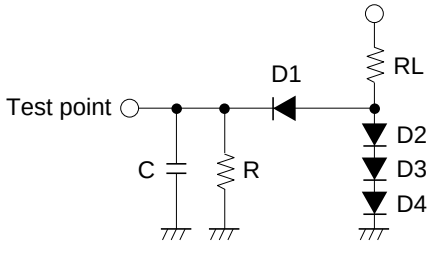


Figure 11 MPU Read Timing



RL = 2.4 kΩ
R = 11 kΩ
C = 130 pF (including jig capacitance)
Diodes D1–D4 are all 1S2074Ⓗ.

Figure 12 DB0–DB7: Load Circuit

Clock Timing (GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
ø1, ø2 cycle time	t_{cyc}	2.5	—	20	µs	Fig. 13
ø1 low level width	$t_{WLø1}$	625	—	—	ns	
ø2 low level width	$t_{WLø2}$	625	—	—	ns	
ø1 high level width	$t_{WHø1}$	1875	—	—	ns	
ø2 high level width	$t_{WHø2}$	1875	—	—	ns	
ø1—ø2 phase difference	t_{D12}	625	—	—	ns	
ø2—ø1 phase difference	t_{D21}	625	—	—	ns	
ø1, ø2 rise time	t_r	—	—	150	ns	
ø1, ø2 fall time	t_f	—	—	150	ns	

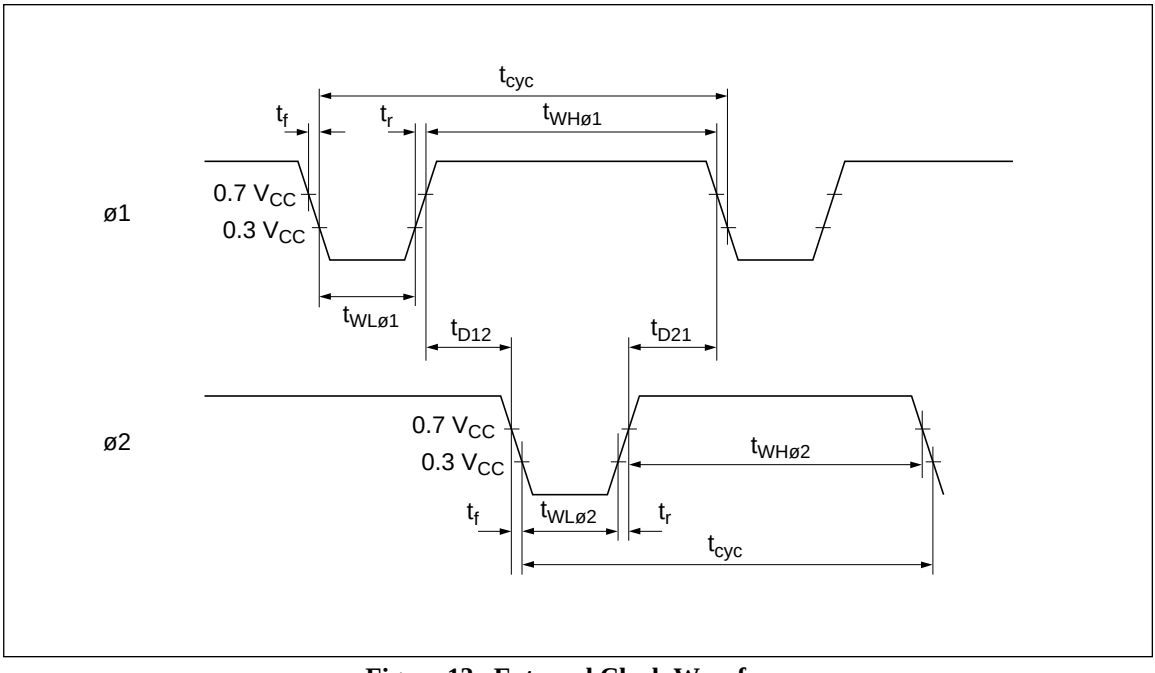


Figure 13 External Clock Waveform

Display Control Timing (GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 14
M delay time	t_{DM}	–2	—	+2	µs	
CL low level width	t_{WLCL}	35	—	—	µs	
CL high level width	t_{WHCL}	35	—	—	µs	

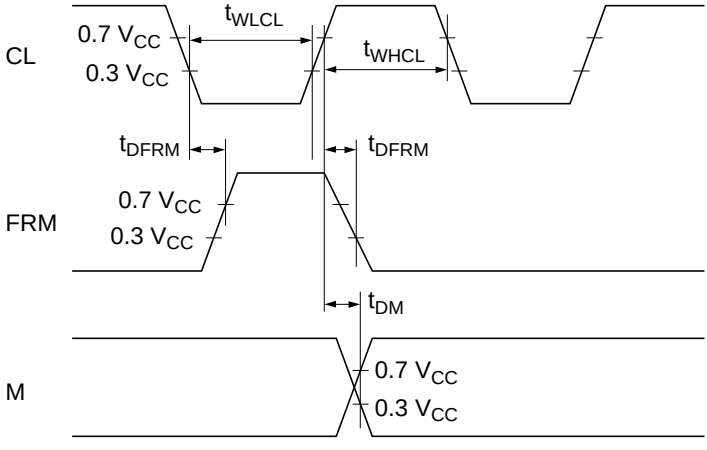


Figure 14 Display Control Signal Waveform

HD61203

(Dot Matrix Liquid Crystal Graphic Display
64-Channel Common Driver)

HITACHI

Description

The HD61203 is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61203 is produced by a CMOS process, it is fit for use in portable battery-driven equipment utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61203 and the column (segment) driver HD61202.

Features

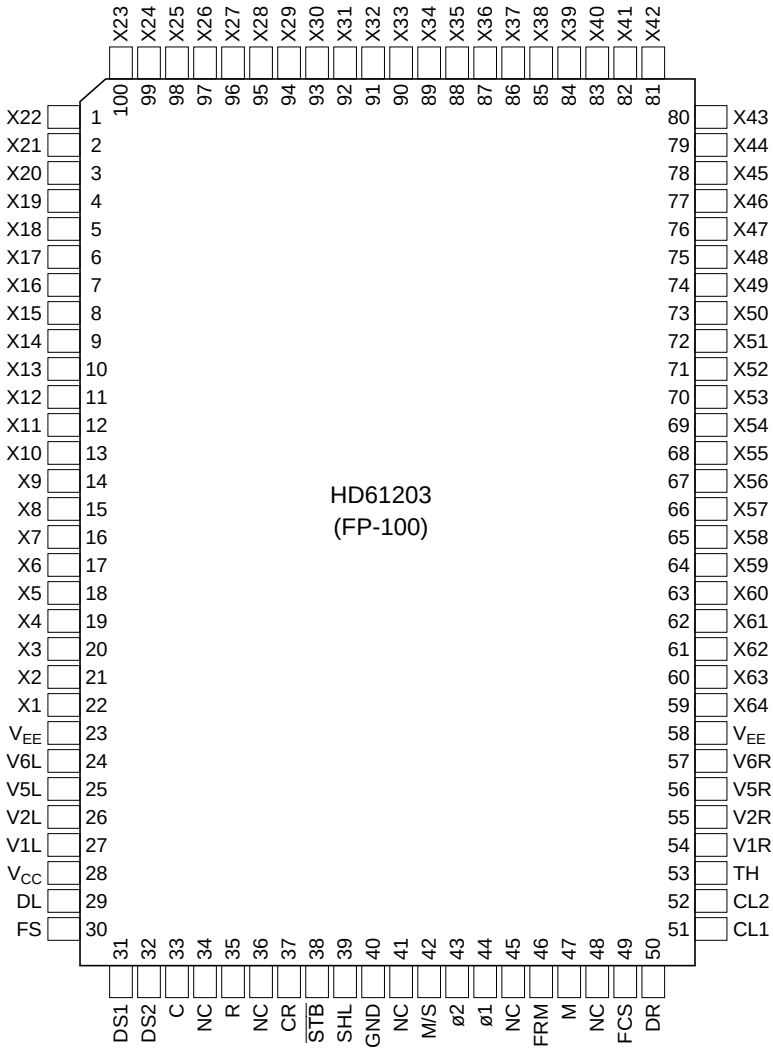
- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Display duty cycle
  - — When used with the column driver HD61202: 1/48, 1/64, 1/96, 1/128
  - — When used with the column driver HD61200: Selectable out of 1/32 to 1/128
- Low power dissipation: During displays: 5 mW
- Power supplies: V_{CC}: 5 V ± 10%
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process

Ordering Information

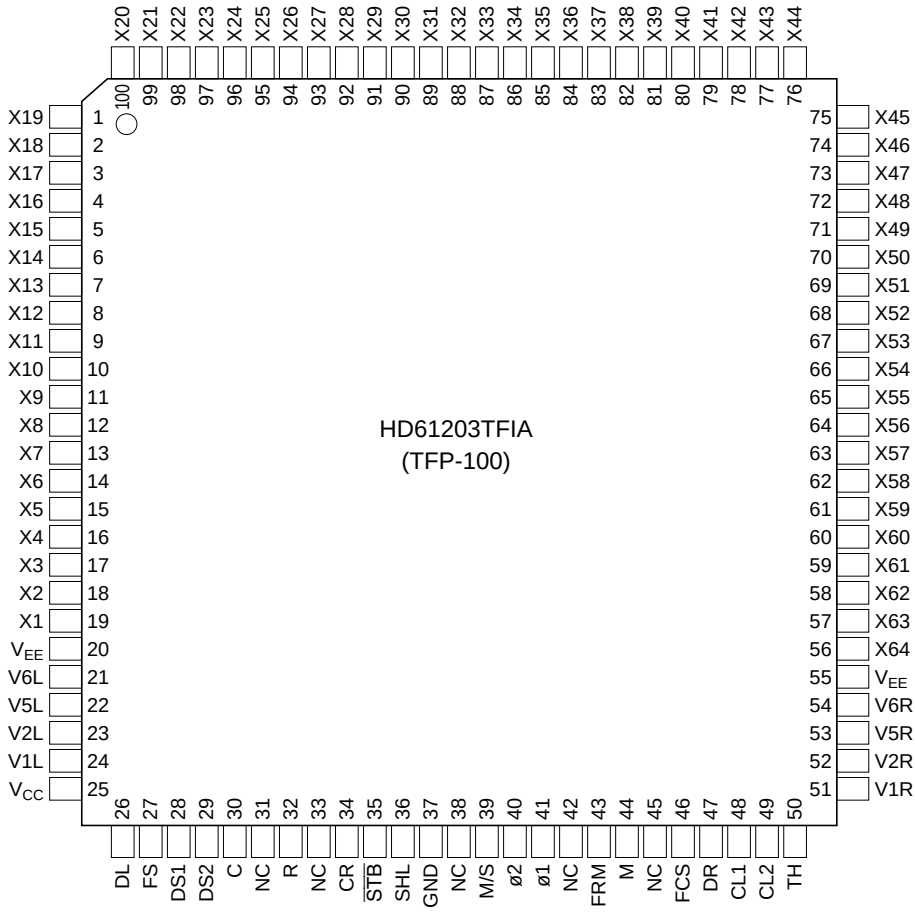
Type No.	Package
HD61203	100-pin plastic QFP (FP-100)
HD61203TFIA	100-pin thin plastic QFP (TFP-100)
HD61203D	Chip

Hitachi semiconductor

Pin Arrangement

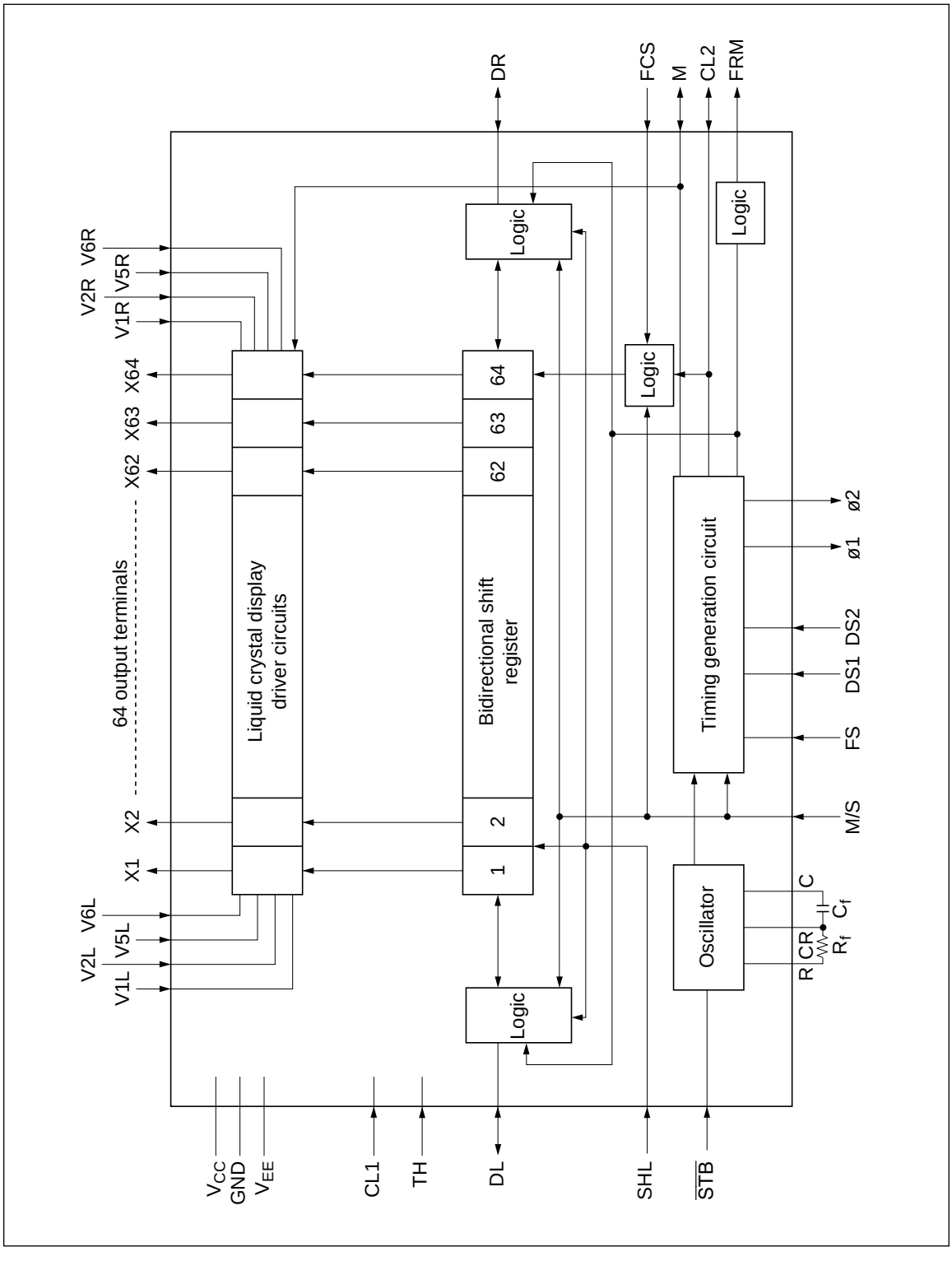


(Top view)


X20 X21 X22 X23 X24 X25 X26 X27 X28 X29 X30 X31 X32 X33 X34 X35 X36 X37 X38 X39 X40 X41 X42 X43 X44
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
X19 1
X18 2
X17 3
X16 4
X15 5
X14 6
X13 7
X12 8
X11 9
X10 10
X9 11
X8 12
X7 13
X6 14
X5 15
X4 16
X3 17
X2 18
X1 19
VEE 20
V6L 21
V5L 22
V2L 23
V1L 24
VCC 25
75 X45
74 X46
73 X47
72 X48
71 X49
70 X50
69 X51
68 X52
67 X53
66 X54
65 X55
64 X56
63 X57
62 X58
61 X59
60 X60
59 X61
58 X62
57 X63
56 X64
55 VEE
54 V6R
53 V5R
52 V2R
51 V1R
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
DL FS DS1 DS2 C NC R NC CR STB SHL GND NC M/S ø2 ø1 NC FRM M NC FCS DR CL1 CL2 TH
HD61203TFIA
(TFP-100)

(Top view)

Block Diagram



Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61202. It is required when the HD61203 is used with the HD61202. An oscillation resister Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{STB}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminals R and C.

The oscillator is not required when the HD61203 is used with the HD61830. Then, connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

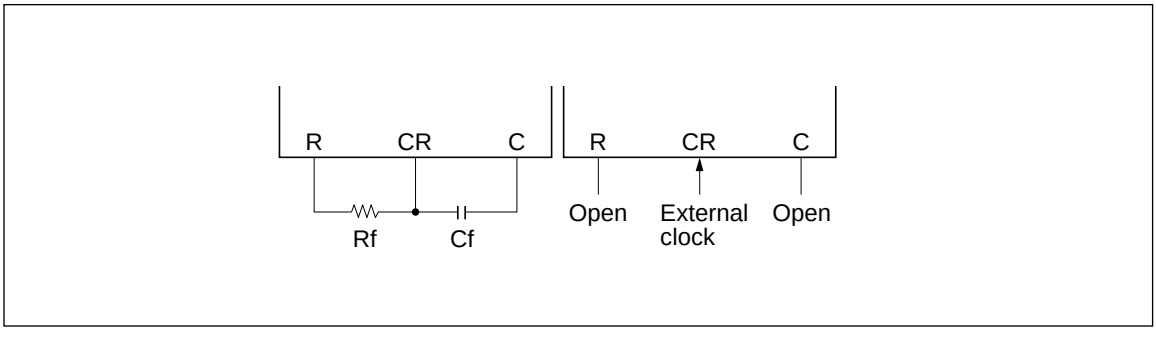


Figure 1 Oscillator Connection with HD61202

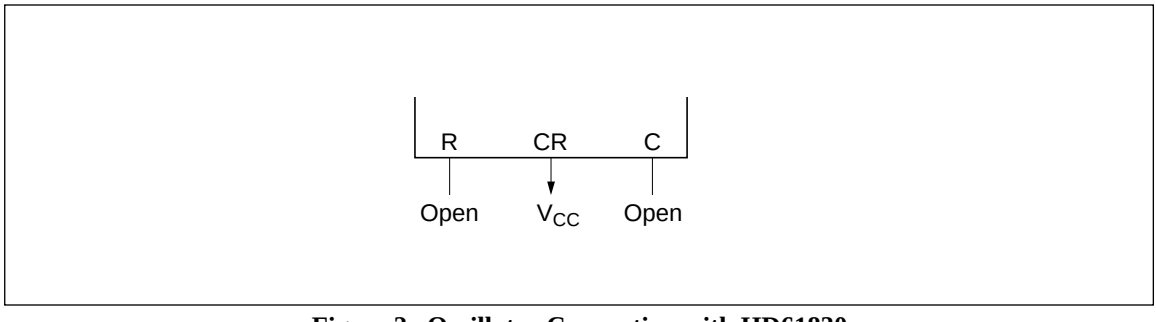


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61202. This circuit is required when the HD61203 is used with the HD61202. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals Fs, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

Table 1 Output Levels

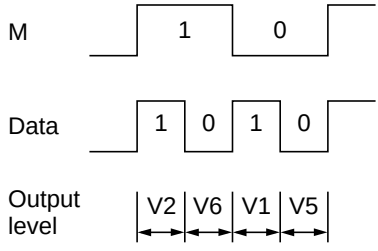
Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

HD61203 Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC}–GND: Power supply for internal logic. V_{CC}–V_{EE}: Power supply for driver circuit logic.
V1L, V2L V5L, V6L V1R, V2R V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively.)
M/S	1	I	V_{CC} or GND	Selects master/slave. • M/S = V_{CC}: Master mode When the HD61203 is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61202. Each of I/O common terminals DL, DR, CL2, and M is in the output state. • M/S = GND: Slave mode The timing operation circuit stops operating. The HD61203 is used in this mode when combined with the HD61830. Even if combined with the HD61202, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61203 in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. • FCS = V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61203 is used with HD61202 or when MA of the HD61830 connects to CL2 in combination with the HD61830. • FCS = GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.

Terminal Name	Number of Terminals	I/O	Connected to	Functions
FS	1	I	V_{CC} or GND	Selects frequency. When the frame frequency is 70 Hz, the oscillation frequency should be: f_{OSC} = 430 kHz at FCS = V_{CC} f_{OSC} = 215 kHz at FCS = GND This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.
DS1, DS2	2	I	V_{CC} or GND	Selects display duty factor. Display Duty Factor: 1/48 / 1/64 / 1/96 / 1/128 DS1: GND / GND / V_{CC} / V_{CC} DS2: GND / V_{CC} / GND / V_{CC} These terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.
$\overline{STB}$ TH CL1	1 1 1	I	V_{CC} or GND	Input terminal for testing Connect to $\overline{STB}$ V_{CC}. Connect TH and CL1 to GND.
CR, R, C	3			Oscillator In the master mode, use these terminals as shown below: Internal oscillation: Rf, Cf; R, CR, C External clock: Open, External clock, Open; R, CR, C In the slave mode, stop the oscillator as shown below: Open, V_{CC}, Open; R, CR, C
ø1, ø2	2	O	HD61202	Operating clock output terminals for the HD61202 • Master mode Connect these terminals to terminals ø1 and ø2 of the HD61202 respectively. • Slave mode Don't connect any lines to these terminals.

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>HD61202</td><td>Frame signal
• Master mode
Connect this terminal to terminal FRM of the HD61202.
• Slave mode
Don’t connect any lines to this terminal.</td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61202</td><td>Signal to convert LCD driver signal into AC
• Master mode: Output terminal
Connect this terminal to terminal M of the HD61202.
• Slave mode: Input terminal
Connect this terminal to terminal MB of the HD61830.</td></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61202</td><td>Shift clock
• Master mode: Output terminal
Connect this terminal to terminal CL of the HD61202.
• Slave mode: Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register
DL corresponds to X1’s side and DR to X64’s side.
• Master mode
Output common scanning signal. Don’t connect any lines to these terminals normally.
• Slave mode
Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don’t connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><td>SHL</td><td>Shift Direction</td><td>Common Scanning Direction</td></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
</table>

Terminal Name	Number of Terminals	I/O	Connected to	Functions
X1–X64	64	O	Liquid crystal display	Liquid crystal display driver output Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the data from the shift register and M signal.  When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

Example of Application

HD61203 Connection List

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	ø1	ø2	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From CL1 of HD61830	H	From FLM of HD61830	—	COM1–COM64
																	L	—	From FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From MA of HD61830	H	From FLM of HD61830	To DL/DR of HD61203 No. 2	COM1–COM64
																	L	To DL/DR of HD61203 No. 2	From FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From MA of HD61830	H	From DL/DR of HD61203 No. 1	—	COM65–COM128
																	L	—	From DL/DR of HD61203 No. 1	COM128–COM65
D	H	L	L	H	H	L or L	L or H	H	Rf Cf	Rf	Cf	To ø1 of HD61202	To ø2 of HD61202	To FRM of HD61202	To M of HD61202	To CL of HD61202	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	L or L	L or H	H	Rf Cf	Rf	Cf	To ø1 of HD61202	To ø2 of HD61202	To FRM of HD61202	To M of HD61202 HD61203	To CL of HD61202 To CL2 of HD61203	H	—	To DL/DR of HD61203 No. 2	COM1–COM64
																	L	To DL/DR of HD61203 No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From M of HD61203 No. 1	From CL2 of HD61203 No. 1	H	From DL/DR of HD61203 No. 1	—	COM1–COM64
																	L	—	From DL/DR of HD61203 No. 1	COM64–COM1

Notes: H: V_{CC} } Fixed
L: GND }

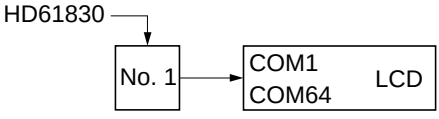
"—" means "open".

Rf: Oscillation resister
Cf: Oscillation capacitor

Outline of HD61203 System Configuration

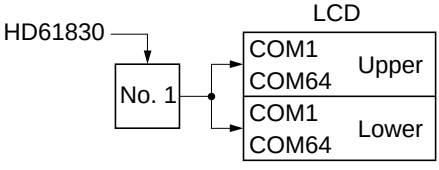
Use with HD61830

1. When display duty ratio of LCD is 1/64



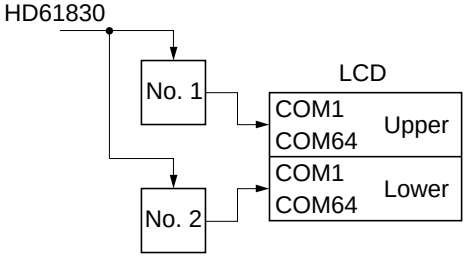
One HD61203 drives common signals.

Refer to Connection List A.



One HD61203 drives common signals for upper and lower panels.

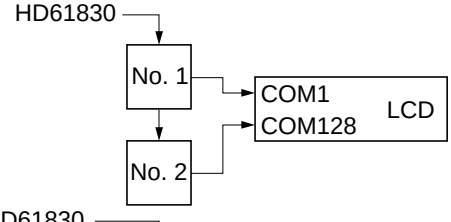
Refer to Connection List A.



Two HD61203s drive upper and lower panels separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

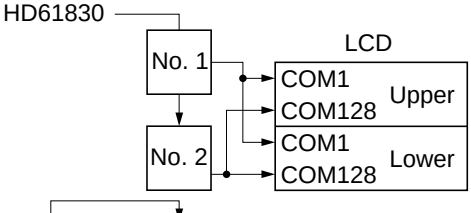
For both of No. 1 and No. 2, refer to Connection List A.

2. When display duty ratio of LCD is from 1/65 to 1/128



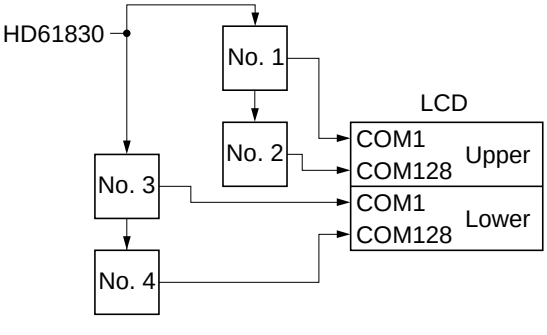
Two HD61203s connected serially drive common signals.

Refer to Connection List B for No. 1.
Refer to Connection List C for No. 2.



Two HD61203s connected serially drive upper and lower panels in parallel.

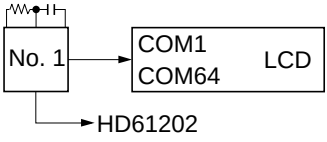
Refer to Connection List B for No. 1.
Refer to Connection List C for No. 2.



Two sets of HD61203s connected serially drive upper and lower panels in parallel to ensure the quality of display.

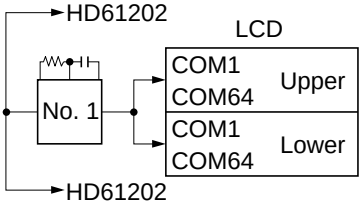
Refer to Connection List B for No. 1 and 3.
Refer to Connection List C for No. 2 and 4.

Use with HD61202 (1/64 Duty Ratio)



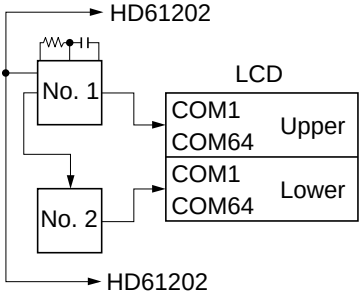
One HD61203 drives common signals and supplies timing signals to the HD61202s.

Refer to Connection List D.



One HD61203 drives upper and lower panels and supplies timing signals to the HD61202s.

Refer to Connection List D.



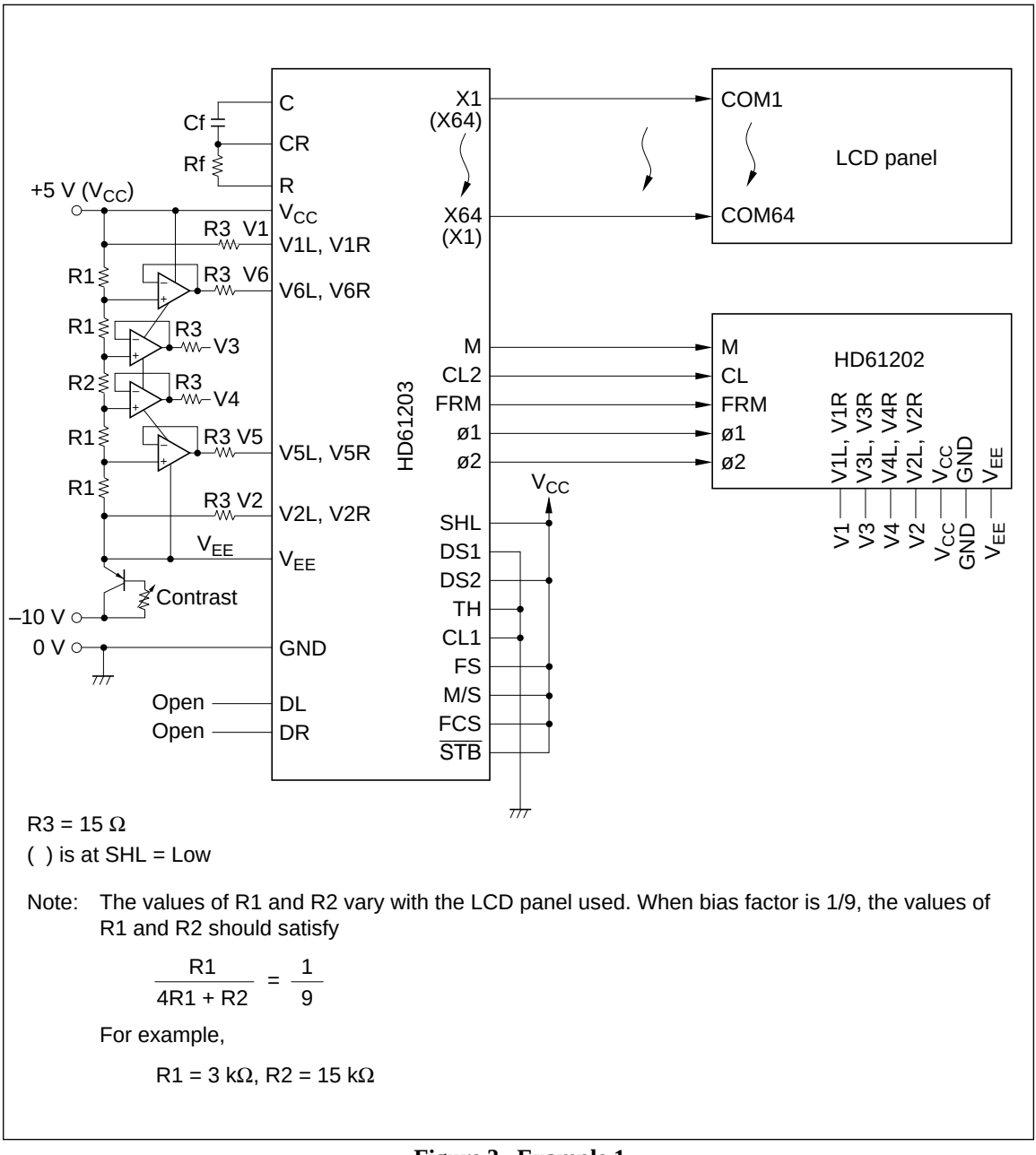
Two HD61203s drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61202s.

Refer to Connection List E for No. 1.
Refer to Connection List F for No. 2.

Connection Example 1

Use with HD61202 (RAM Type Segment Driver)

1. 1/64 duty ratio (see Connection List D)



R3 = 15 Ω

( ) is at SHL = Low

Note: The values of R1 and R2 vary with the LCD panel used. When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1 = 3 kΩ, R2 = 15 kΩ

Figure 3 Example 1

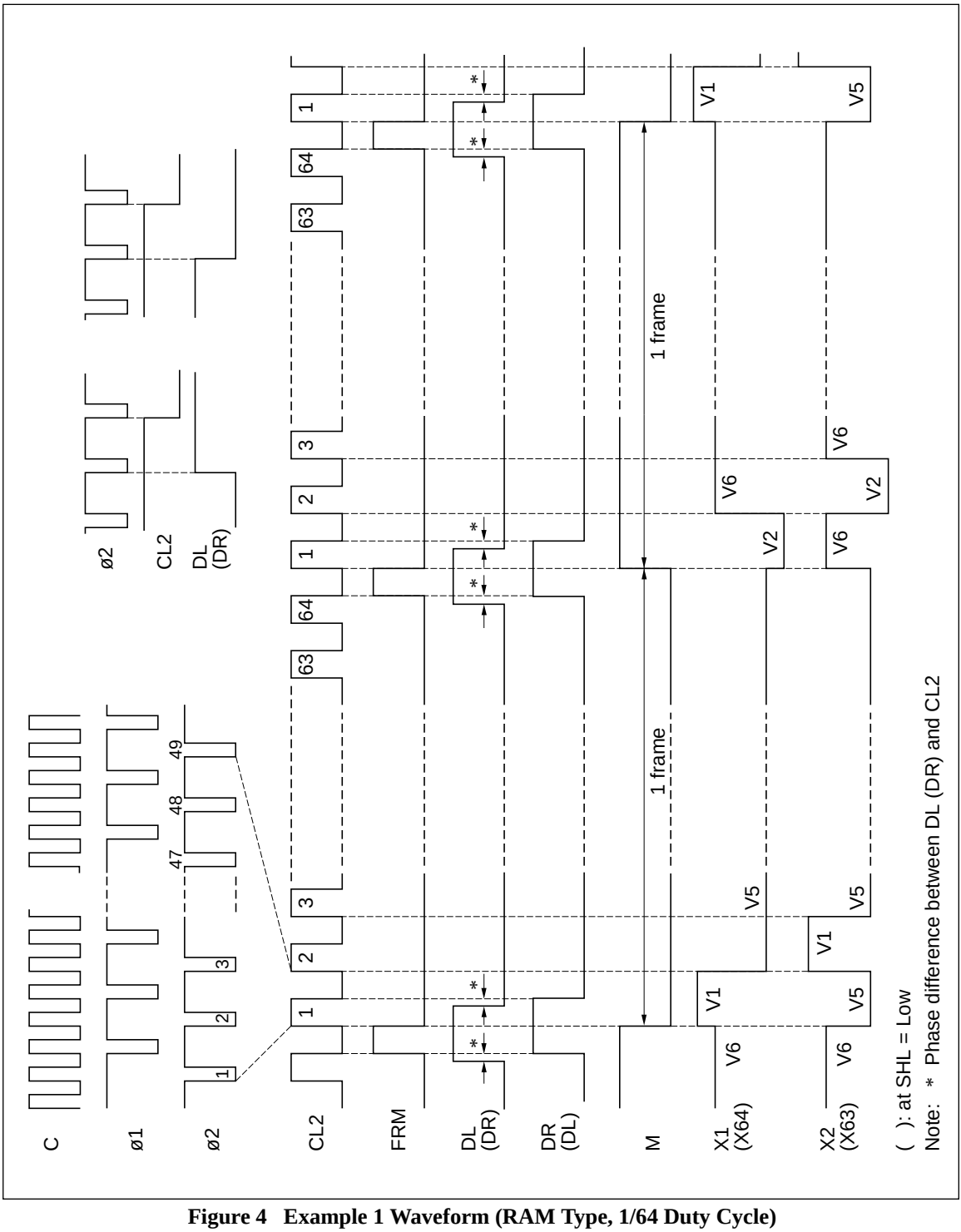


Figure 4 Example 1 Waveform (RAM Type, 1/64 Duty Cycle)

Connection Example 2

Use with HD61830 (Display Controller)

1. 1/64 duty ratio (see Connection List A)

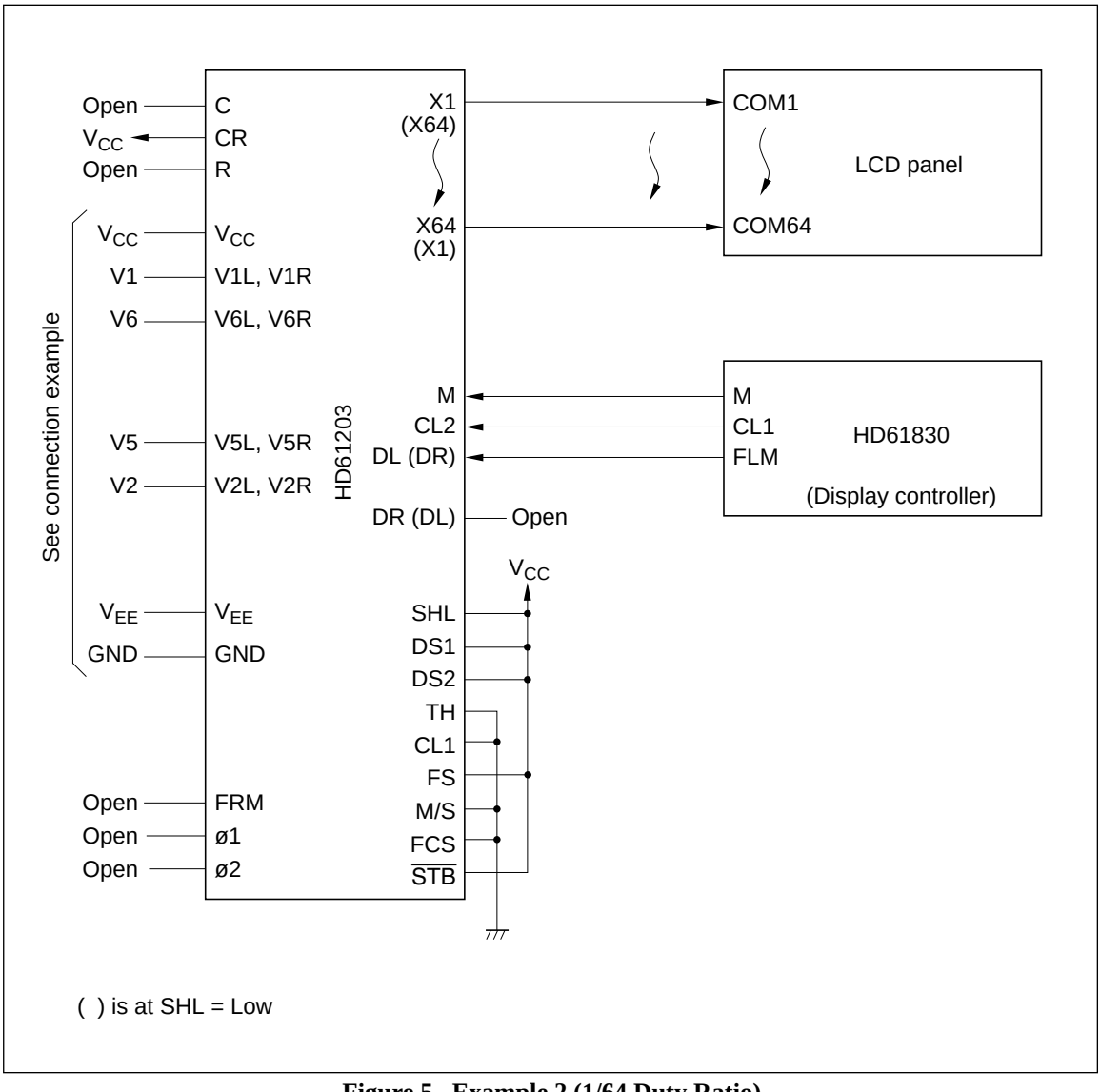


Figure 5 Example 2 (1/64 Duty Ratio)

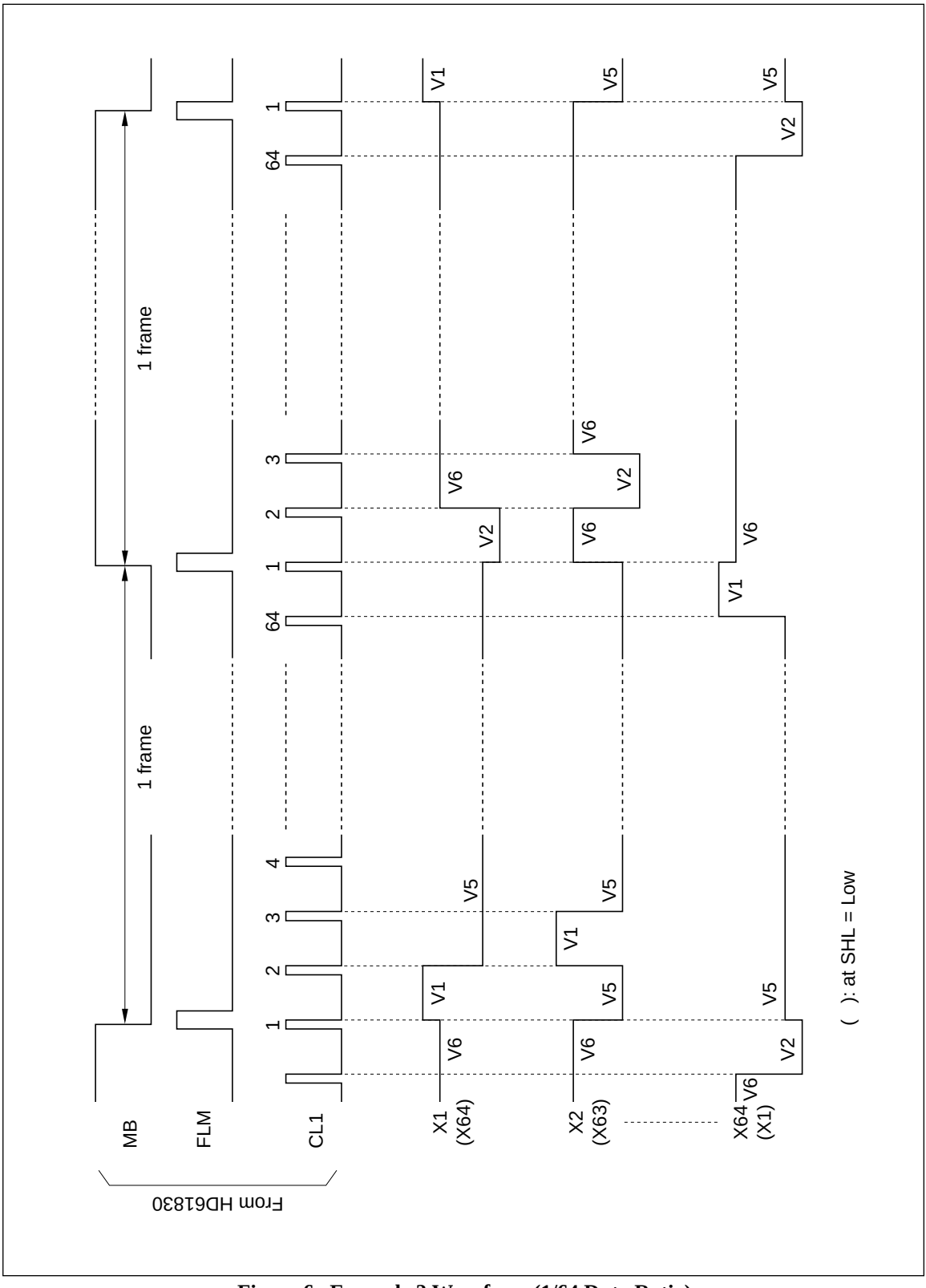


Figure 6 Example 2 Waveform (1/64 Duty Ratio)

2. 1/100 duty ratio (see Connection List B, C)

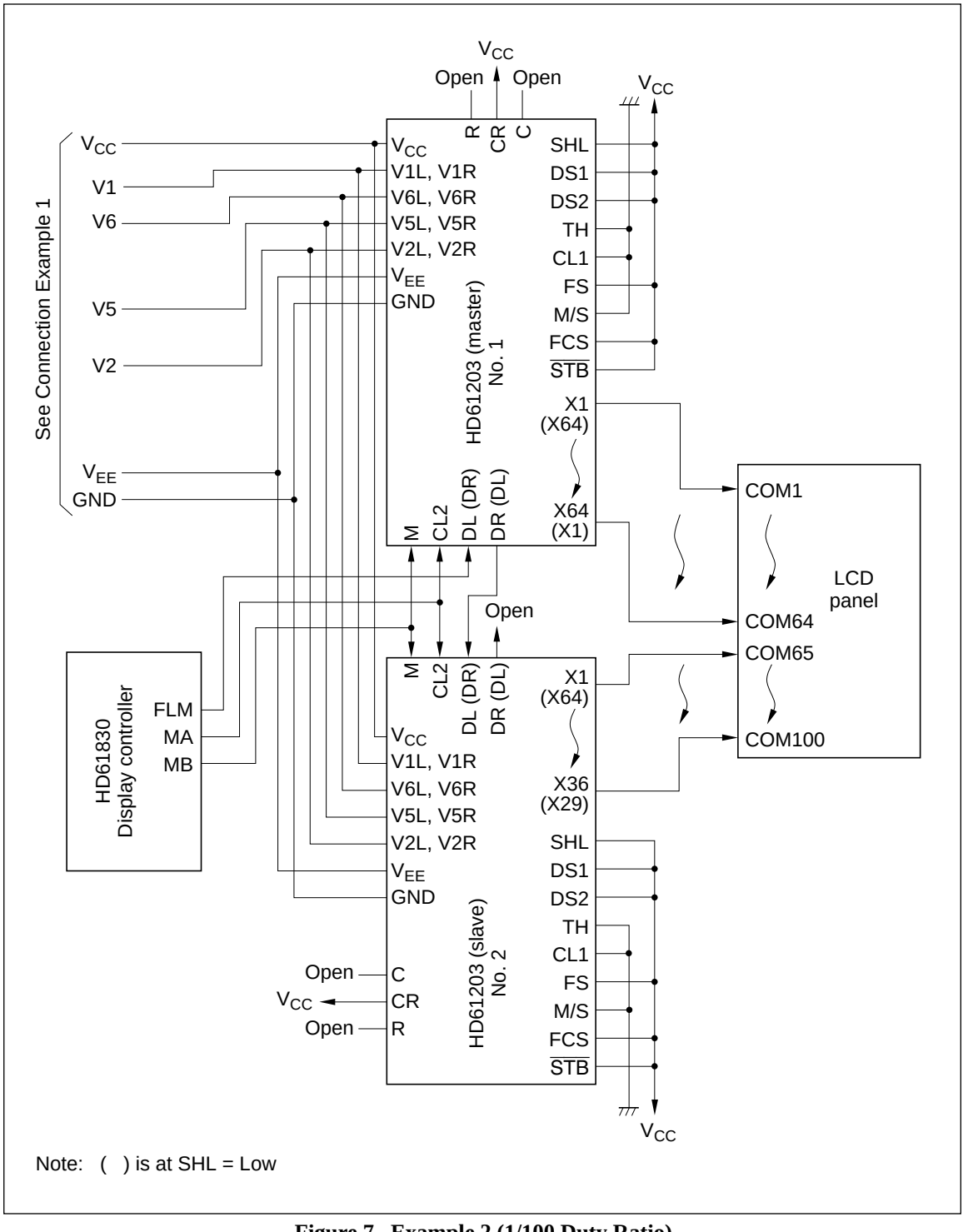


Figure 7 Example 2 (1/100 Duty Ratio)

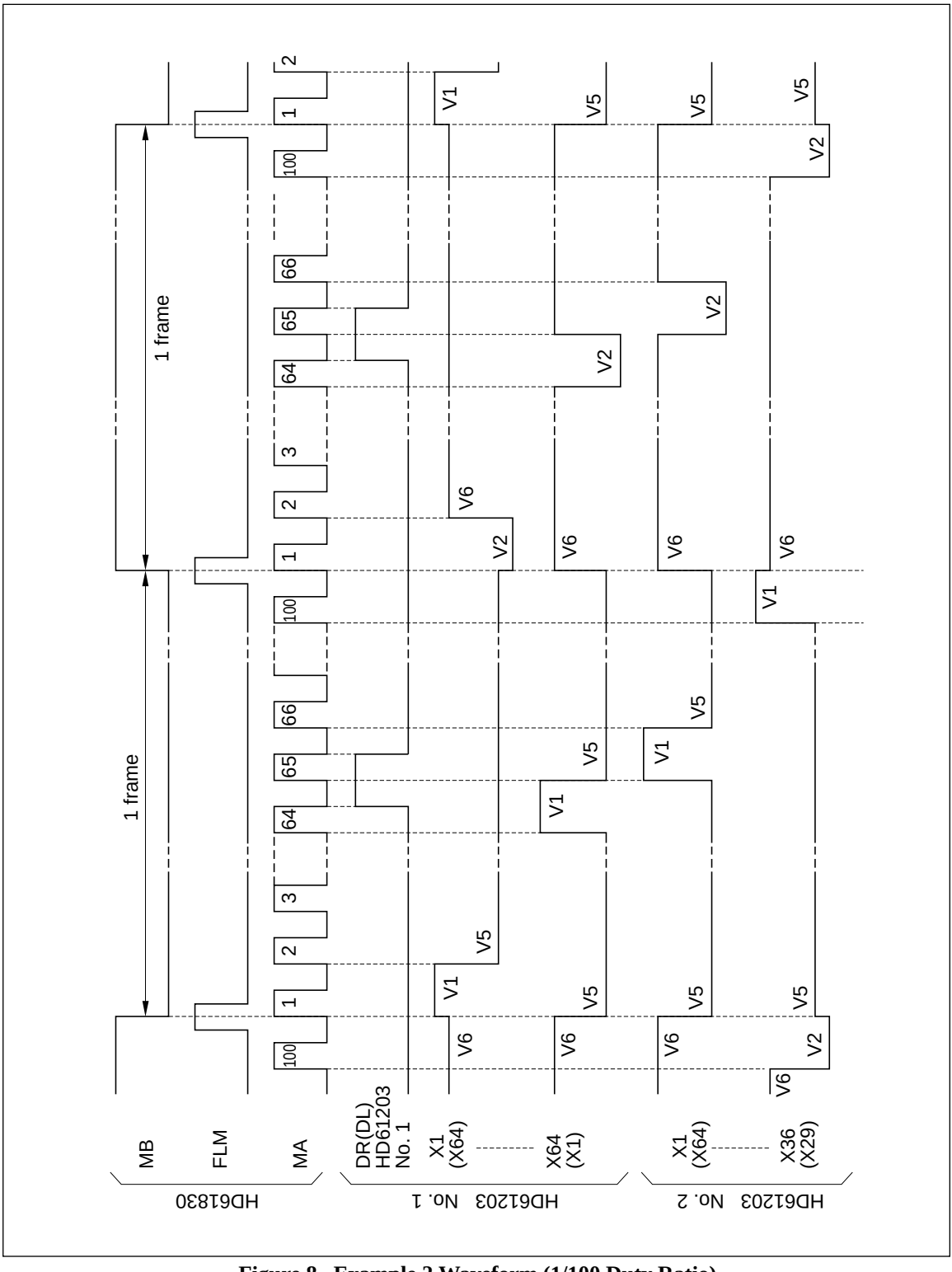


Figure 8 Example 2 Waveform (1/100 Duty Ratio)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.

   Maintain $V_{CC} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EE}$

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, $V_{CC} - V_{EE}$ = 8.0 to 17.0 V, Ta = –20 to +75°C)

		Specifications					
Test Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Notes**
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA	2
Vi–Xj on resistance	R_{ON}	—	—	1.5	kΩ	$V_{CC} - V_{EE}$ = 10 V Load current ±150 µA	13
Input leakage current	I_{IL1}	–1.0	—	1.0	µA	Vin = 0 to V_{CC}	3
Input leakage current	I_{IL2}	–2.0	—	2.0	µA	Vin = V_{EE} to V_{CC}	4
Operating frequency	f_{opr1}	50	—	600	kHz	In master mode external clock operation	5
Operating frequency	f_{opr2}	0.5	—	1500	kHz	In slave mode shift register	6
Oscillation frequency	f_{osc}	315	450	585	kHz	Cf = 20 pF ± 5% Rf = 47 kΩ ± 2%	7, 12
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	8, 9
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	8, 10
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	8, 11

Notes: 1. Applies to input terminals FS, DS1, DS2, CR, SHL, M/S, and FCS and I/O terminals DL, M, DR and CL2 in the input state.

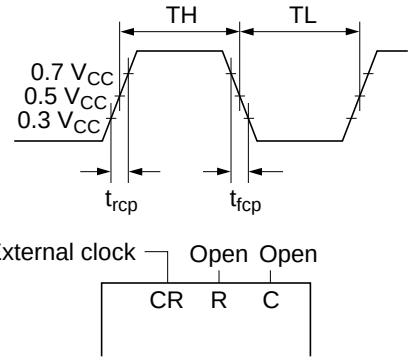
2. Applies to output terminals, ø1, ø2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output status.

3. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH, I/O terminals DL, M, DR, and CL2 in the input state and NC terminals.

4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R. Don't connect any lines to X1 to X64.

5. External clock is as follows.

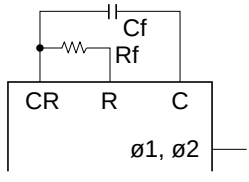
External clock waveform



$$\text{Duty cycle} = \frac{TH}{TH + TL} \times 100\%$$

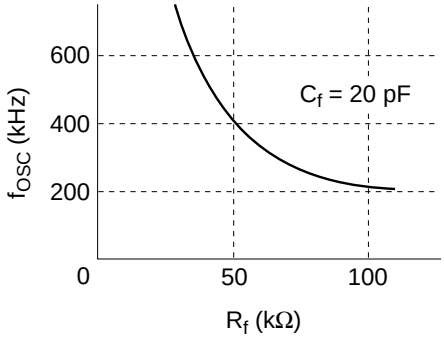
	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
t_{rcp}	—	—	50	ns
t_{fcp}	—	—	50	ns

6. Applies to the shift register in the slave mode. For details, refer to AC characteristics.
7. Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency (fø) at ø1 or ø2.



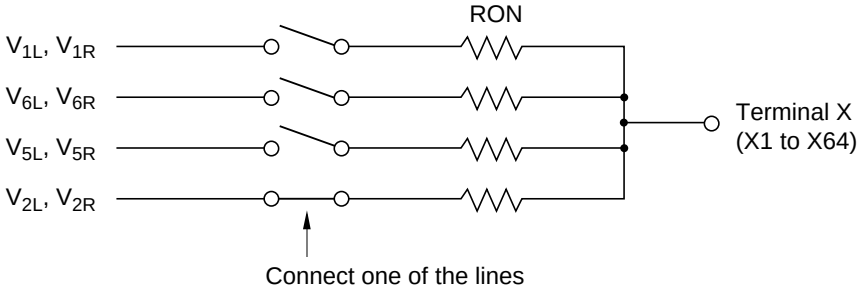
Cf = 20 pF
Rf = 47 kΩ $\quad f_{OSC} = 2 \times f\text{ø}$

8. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and V_{IL} = GND.
9. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 7.
10. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61203 under the condition described in note 9.
11. This value is specified for current flowing through V_{EE} under the condition described in note 9. Don't connect any lines to terminal V.
12. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.

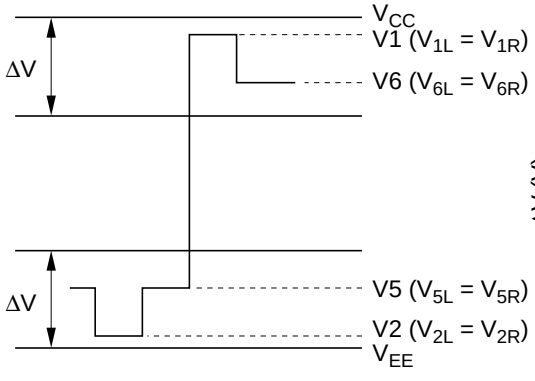


13. Resistance between terminal X and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

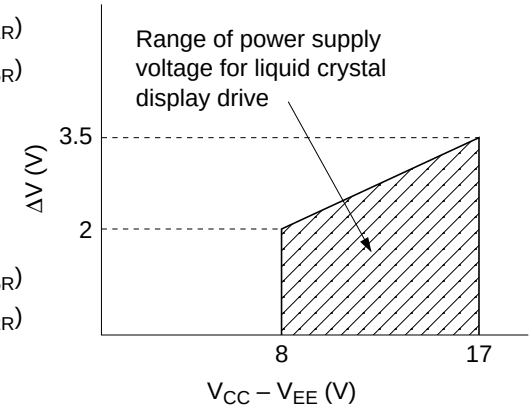
$$V_{CC} - V_{EE} = 17\ V$$
$$V_{1L} = V_{1R},\ V_{6L} = V_{6R} = V_{CC} - 1/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{5L} = V_{5R} = V_{EE} + 1/7\ (V_{CC} - V_{EE})$$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V6L = V6R and negative voltage to V2L = V2R and V5L = V5R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



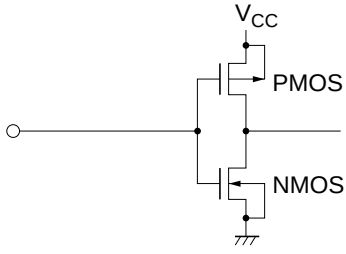
Correlation between driver output waveform and power supply voltage for liquid crystal display drive



Correlation between power supply voltage $V_{CC} - V_{EE}$ and ΔV

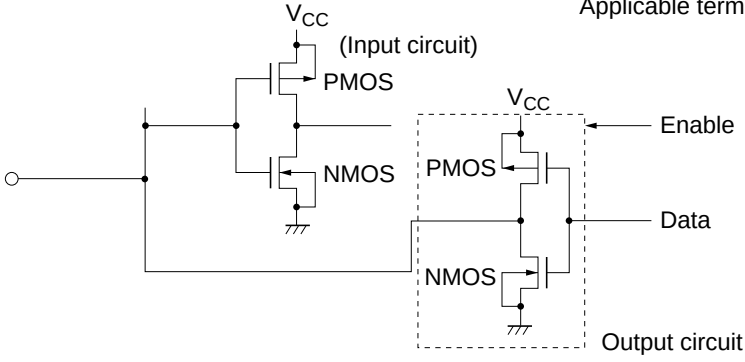
Terminal Configuration

Input Terminal



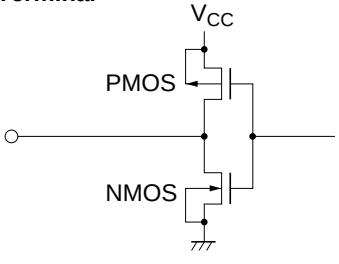
Applicable terminals:
CR, M/S, SHL, FCS, DS1, DS2, FS

I/O Terminal



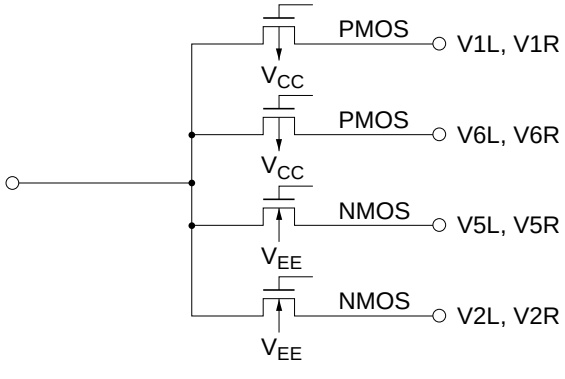
Applicable terminals: DL, DR, CL2, M

Output Terminal



Applicable terminals: ø1, ø2, FRM

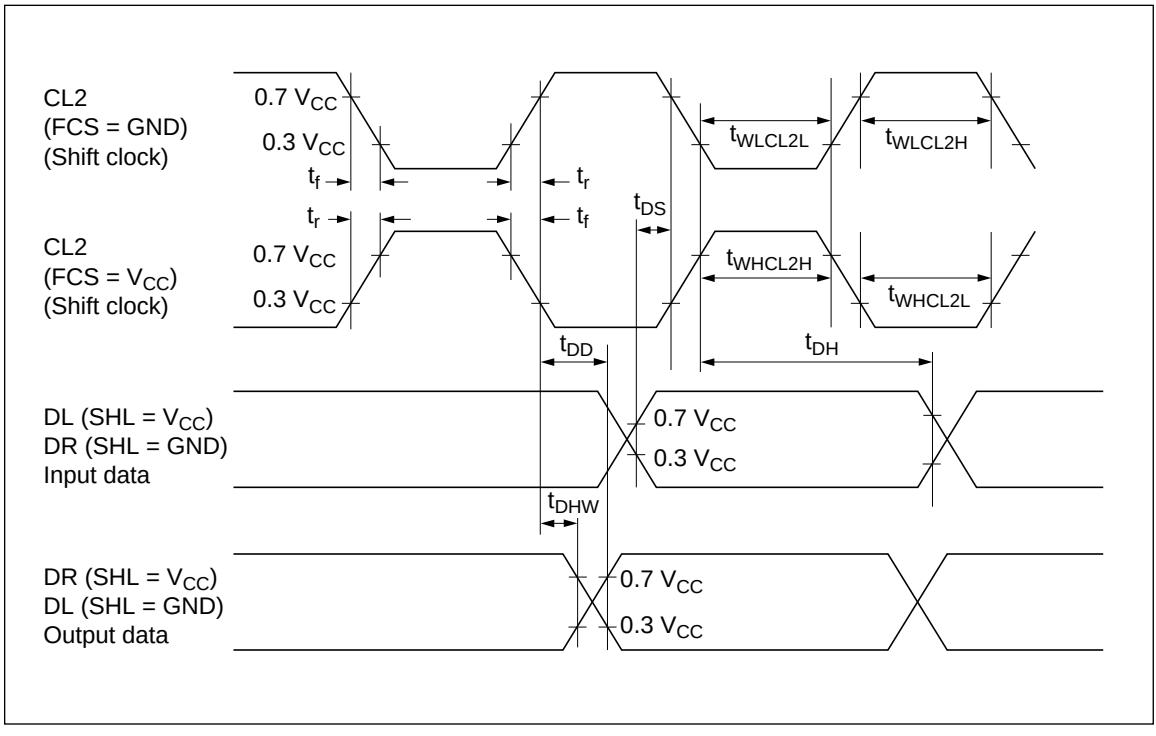
Output Terminal



Applicable terminals:
X1 to X64

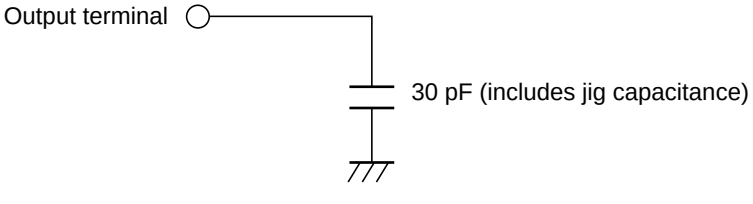
AC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

In the Slave Mode (M/S = GND)

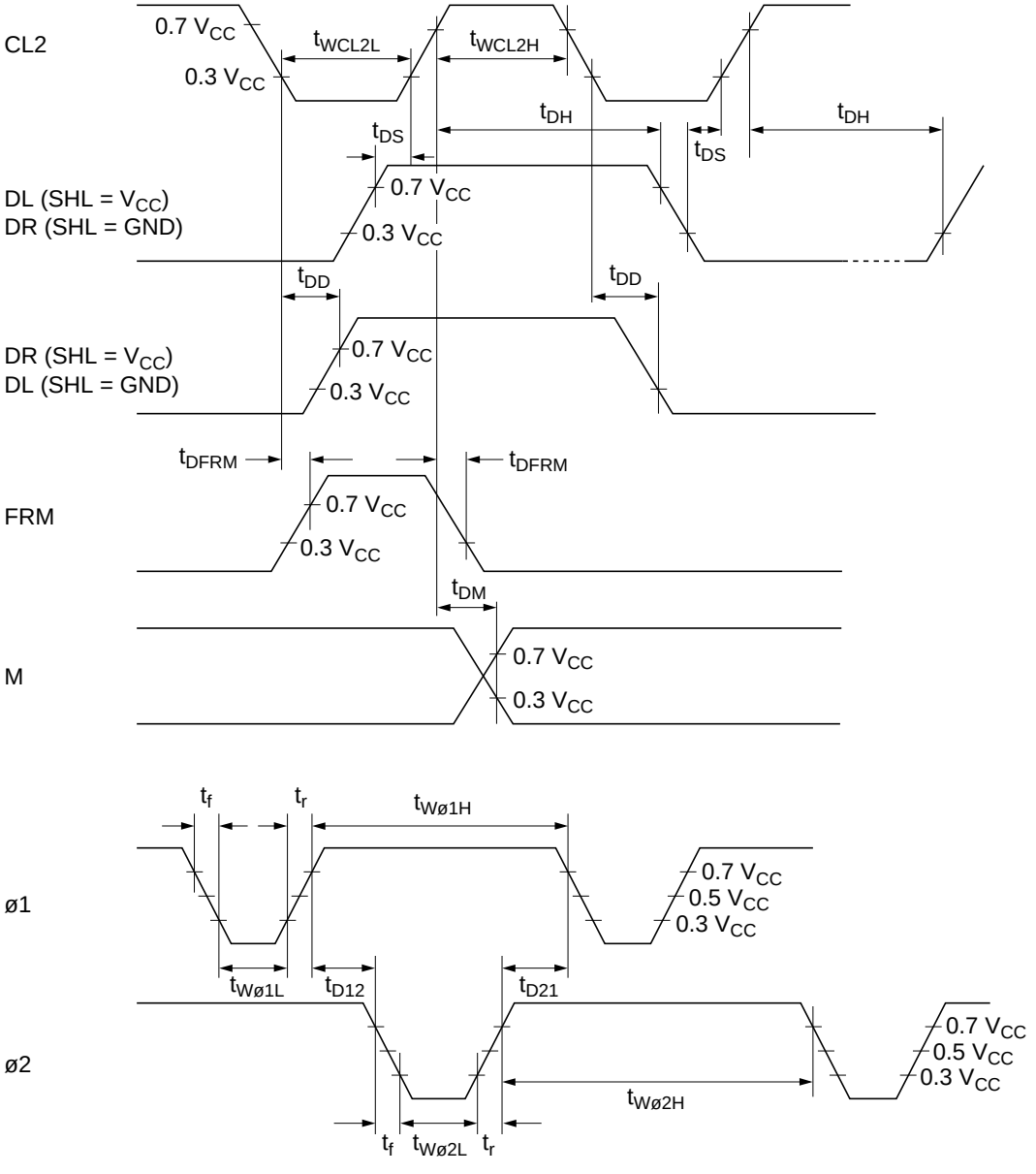


Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS = GND)	t_{WLCL2L}	450	—	—	ns	
CL2 high level width (FCS = GND)	t_{WLCL2H}	150	—	—	ns	
CL2 low level width (FCS = V_{CC})	t_{WHCL2L}	150	—	—	ns	
CL2 high level width (FCS = V_{CC})	t_{WHCL2H}	450	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	100	—	—	ns	
Data delay time	t_{DD}	—	—	200	ns	1
Data hold time	t_{DHW}	10	—	—	ns	
CL2 rise time	t_r	—	—	30	ns	
CL2 fall time	t_f	—	—	30	ns	

Notes: 1. The following load circuit is connected for specification.



2. In the master mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)



Item	Symbol	Min	Typ	Max	Unit
Data setup time	t_{DS}	20	—	—	µs
Data hold time	t_{DH}	40	—	—	µs
Data delay time	t_{DD}	5	—	—	µs
FRM delay time	t_{DFRM}	–2	—	+2	µs
M delay time	t_{DM}	–2	—	+2	µs
C_{L2} low level width	t_{WCL2L}	35	—	—	µs
C_{L2} high level width	t_{WCL2H}	35	—	—	µs
ø1 low level width	$t_{Wø1L}$	700	—	—	ns
ø2 low level width	$t_{Wø2L}$	700	—	—	ns
ø1 high level width	$t_{Wø1H}$	2100	—	—	ns
ø2 high level width	$t_{Wø2H}$	2100	—	—	ns
ø1–ø2 phase difference	t_{D12}	700	—	—	ns
ø2–ø1 phase difference	t_{D21}	700	—	—	ns
ø1, ø2 rise time	t_r	—	—	150	ns
ø1, ø2 fall time	t_f	—	—	150	ns

HD66410

(RAM-Provided 128-Channel Driver for Dot-Matrix Graphic LCD)

Preliminary

HITACHI

Description

The HD66410 drives and controls a dot-matrix graphic LCD using a bit-mapped display method. It provides a highly flexible display through its on-chip display RAM, in which each bit of data can be used to turn on or off one dot on the LCD panel.

A single HD66410 can display a maximum of 128 × 33 dots using its powerful display control functions. It features 24-channel annunciator output operating with 1/3 duty cycle that is available even during standby modes, which makes it suitable for time and other mark indications.

An MPU can access the HD66410 at any time because the MPU operations are asynchronous with the HD66410's system clock and display operations.

Its low-voltage operation at 2.2 to 3.6 V and the standby function provides low power-dissipation, making the HD66410 suitable for small portable device applications.

Features

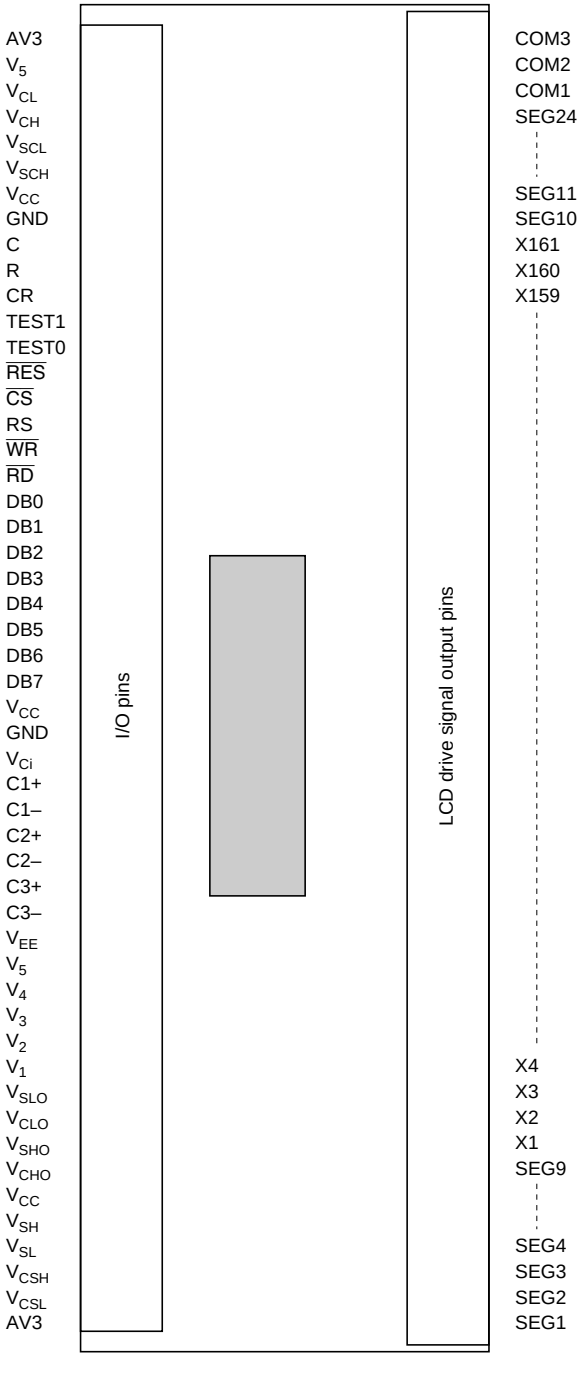
- 4.2-kbit (128 × 33-bit) bit-mapped display RAM
- 128 × 33 dots displayed using a single HD66410
  - 8 characters × 2 lines (16 × 16-dot character)
  - 21 characters × 4 lines (6 × 8-dot character)
- Annunciator display using dedicated output channels
  - Maximum of 72 segments displayed with 1/3 duty cycle
  - Available even during standby modes
- Flexible LCD driver configuration
  - Row output from both sides of an LCD panel
  - Row output from one side of an LCD panel
- Low power-dissipation suitable for long battery-based operation
  - Low-voltage operation: 2.2 to 3.6 V
  - Two standby modes: modes with and without annunciator display
- On-chip double to quadruple booster
- Versatile display control functions
  - Display data read/write
  - Display on/off
  - Column address inversion according to column driver layout
  - Vertical display scroll
  - Blink area select
  - Read-modify-write
- 80-system CPU interface through 8-bit asynchronous data bus
- On-chip oscillator combined with external resistors and capacitors
- Tape carrier package (TCP)

Ordering Information

Type No.	Package
HD66410Txx	TCP

Hitachi semiconductor

Pin Arrangement



Note: This figure is not drawn to a scale.

Pin Description

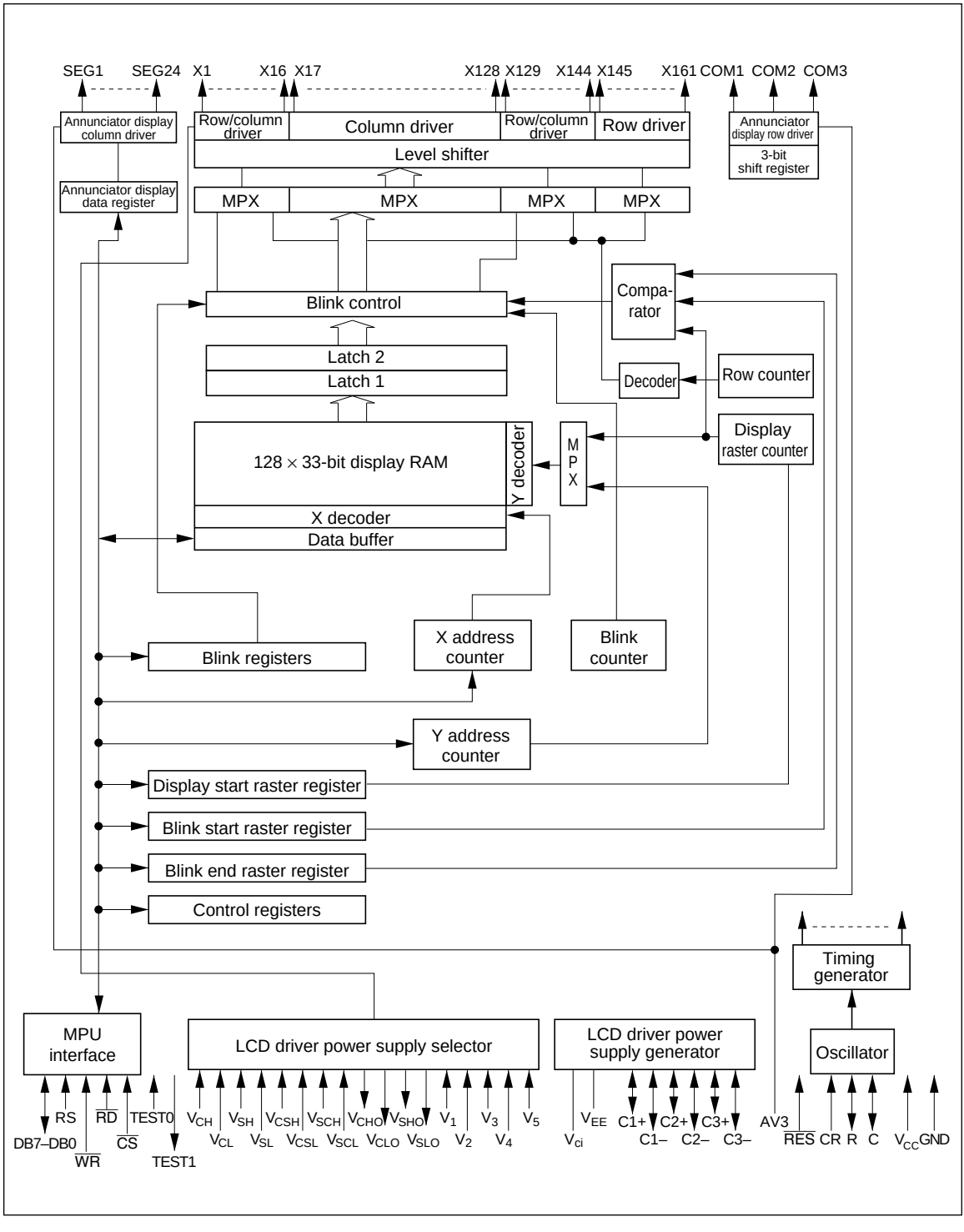
Pin Name	Number of Pins	I/O	Connected to	Description
V_{CC}, GND	5	—	Power supply	V_{CC}: +2.2 to +3.6 V, GND: 0 V
Vci	1	—	Power supply	Inputs voltage to the booster to generate the base of the LCD drive voltages (V_{EEC} and V_{EEL}); must be below V_{CC}. Vci: 0 to +3.6 V.
AV3	1	—	Power supply	Supplies power to the internal annunciator drivers to generate the annunciator drive voltages using AV3 and V_{CC}. V_{CC}–AV3: 0 to 3.6 V; must be above GND.
V_{EE}	1	I/O	Booster capacitors and V5	Boosts and outputs the voltage input to the Vci pin; must be connected to the booster capacitors and V5 pin.
V1, V2, V3, V4, V5	5	—	Resistive divider	Supplies several levels of power to the internal LCD drivers for dot-matrix display; must be applied with the appropriate level of bias for the LCD panel used.
C1+ to C3+, C1– to C3–	6	—	Booster capacitor	Must be connected to external capacitors according to the boosting ratio.
V_{SHO}, V_{SLO}	2	O	VSH, VSL, VCSH, VCSL, VSCH, VSCL	Output voltage to be supplied to the internal column drivers.
V_{CHO}, V_{CLO}	2	O	VCH, VCL, VCSH, VCSL, VSCH, VSCL	Output voltage to be supplied to the internal row drivers.
V_{SH}, V_{SL}	2	I	VSHO, VSLO	Input voltage to be supplied to internal drivers X17 to X128.
V_{CH}, V_{CL}	2	I	VCHO, VCLO	Input voltage to be supplied to internal drivers X145 to X160.
V_{CSH}, V_{CSL}	2	I	VCHO, VCLO, VSHO, VSLO	Input voltage to be supplied to internal drivers X1 to X16.
V_{SCH}, V_{SCL}	2	I	VCHO, VCLO, VSHO, VSLO	Input voltage to be supplied to internal drivers X129 to X144.
C, R, CR	3	I, I/O	Oscillator resistor and capacitor	Must be connected to external capacitors and resistors when using R-C oscillation. When using an external clock, it must be input to the CR pin.
$\overline{RES}$	1	I	—	Resets the LSI internally when driven low.
$\overline{CS}$	1	I	MPU	Selects the LSI, specifically internal registers (index and data registers) when driven low.
RS	1	I	MPU	Selects one of the internal registers; selects the index register when driven low and data registers when driven high.
$\overline{WR}$	1	I	MPU	Inputs write strobe; allows a write access when driven low.

Pin Name	Number of Pins	I/O	Connected to	Description
$\overline{RD}$	1	I	MPU	Inputs read strobe; allows a read access when driven low.
DB7 to DB0	8	I/O	MPU	8-bit three-state bidirectional data bus; transfers data between the HD66410 and MPU through this bus.
X1 to X16, X129 to X144	32	O	Liquid crystal display	Output column or row drive signals; either column or row can be selected by programming.
X17 to X128	112	O	Liquid crystal display	Output column drive signals.
X145 to X161	17	O	Liquid crystal display	Output row drive signals.
COM1 to COM3	3	O	Liquid crystal display	Output row drive signals for annunciator display; available even during standby modes. Can operate statically or with 1/3 duty cycle.
SEG1 to SEG24	24	O	Liquid crystal display	Output column drive signals for annunciator display; available even during standby modes.
TEST0	1	I	GND	Tests the LSI; must be grounded.
TEST1	1	O	—	Tests the LSI; must be left unconnected.

Register List

CS	RS	Index Register Bits					Register Symbol	Register Name	R/W	Data Bits							
		4	3	2	1	0				7	6	5	4	3	2	1	0
1	—	—	—	—	—	—											
0	0	—	—	—	—	—	IR	Index register	W				IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	R0	Control register 1	W		DISP	STBY	PWR	OSC	IDTY	CNF	ADC
0	1	0	0	0	0	1	R1	Control register 2	W					RMW	DDTY	INC	BLK
0	1	0	0	0	1	0	R2	X address register	W					XA3	XA2	XA1	XA0
0	1	0	0	0	1	1	R3	Y address register	W			YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	1	0	0	R4	Display memory access register	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	R5	Display start raster register	W			ST5	ST4	ST3	ST2	ST1	ST0
0	1	0	0	1	1	0	R6	Blink register 1	W	BK0	BK1	BK2	BK3	BK4	BK5	BK6	BK7
0	1	0	0	1	1	1	R7	Blink register 2	W	BK8	BK9	BK10	BK11	BK12	BK13	BK14	BK15
0	1	0	1	0	0	0	R8	Blink start raster register	W			BSL5	BSL4	BSL3	BSL2	BSL1	BSL0
0	1	0	1	0	0	1	R9	Blink end raster register	W			BEL5	BEL4	BEL3	BEL2	BEL1	BEL0
0	1	0	1	0	1	0		Reserved									
0	1	0	1	0	1	1		Reserved									
0	1	0	1	1	0	0		Reserved									
0	1	0	1	1	0	1		Reserved									
0	1	0	1	1	1	0		Reserved									
0	1	0	1	1	1	1		Reserved									
0	1	1	0	0	0	0	A0	Annunciator display data register 1	W	IC1A	IC1B	IC1C	IC1D	IC1E	IC1F	IC1G	IC1H
0	1	1	0	0	0	1	A1	Annunciator display data register 2	W	IC2A	IC2B	IC2C	IC2D	IC2E	IC2F	IC2G	IC2H
0	1	1	0	0	1	0	A2	Annunciator display data register 3	W	IC3A	IC3B	IC3C	IC3D	IC3E	IC3F	IC3G	IC3H
0	1	1	0	0	1	1	A3	Annunciator display data register 4	W	IC1I	IC1J	IC1K	IC1L	IC1M	IC1N	IC1O	IC1P
0	1	1	0	1	0	0	A4	Annunciator display data register 5	W	IC2I	IC2J	IC2K	IC2L	IC2M	IC2N	IC2O	IC2P
0	1	1	0	1	0	1	A5	Annunciator display data register 6	W	IC3I	IC3J	IC3K	IC3L	IC3M	IC3N	IC3O	IC3P
0	1	1	0	1	1	0	A6	Annunciator display data register 7	W	IC1Q	IC1R	IC1S	IC1T	IC1U	IC1V	IC1W	IC1X
0	1	1	0	1	1	1	A7	Annunciator display data register 8	W	IC2Q	IC2R	IC2S	IC2T	IC2U	IC2V	IC2W	IC2X
0	1	1	1	0	0	0	A8	Annunciator display data register 9	W	IC3Q	IC3R	IC3S	IC3T	IC3U	IC3V	IC3W	IC3X
0	1	1	1	0	0	1	A9	Annunciator blink register 1	W	IP11	IP10	IB15	IB14	IB13	IB12	IB11	IB10
0	1	1	1	0	1	0	A10	Annunciator blink register 2	W	IP21	IP20	IB25	IB24	IB23	IB22	IB21	IB20
0	1	1	1	0	1	1	A11	Annunciator blink register 3	W	IP31	IP30	IB35	IB34	IB33	IB32	IB31	IB30
0	1	1	1	1	0	0		Reserved									
0	1	1	1	1	0	1		Reserved									
0	1	1	1	1	1	0		Reserved									
0	1	1	1	1	1	1		Reserved									

Block Diagram



System Description

The HD66410 comprises two kinds of independent LCD drivers: one operating with 1/33 or 1/17 duty cycle for dot-matrix displays and the other operating statically or with 1/3 duty cycle for annunciator displays. These drivers can display a maximum of 128 × 33 dots (eight 16 × 16-dot characters × 2 lines) on an LCD panel together with a 72-segment annunciator. Annunciator display is available even during standby modes, thus enabling constant display such as for a time function. The HD66410 can reduce power dissipation without affecting display because data is retained in the display RAM even during standby modes. An LCD system can be configured simply by attaching external capacitors and resistors (figure 1) since the HD66410 incorporates booster circuits.

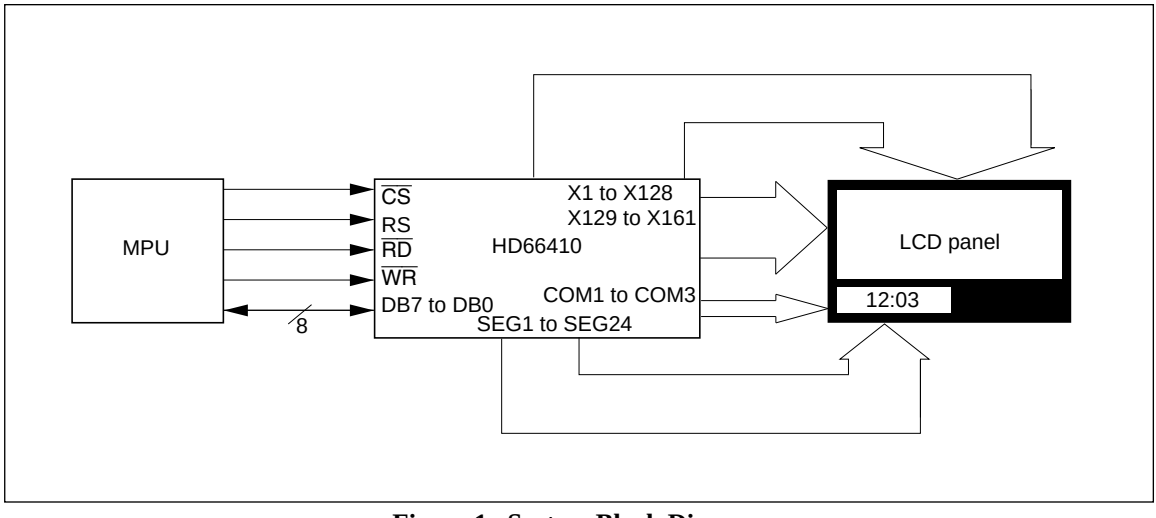


Figure 1 System Block Diagram

MPU Interface

The HD66410 can interface directly to an MPU through an 8-bit data bus or through an I/O port (figure 2). The MPU can access the HD66410 internal registers independent of internal clock timing.

The index register can be directly accessed but the other registers (data registers) cannot. Before accessing a data register, its register number must be written to the index register. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. An example of a register access sequence is shown in figure 3.

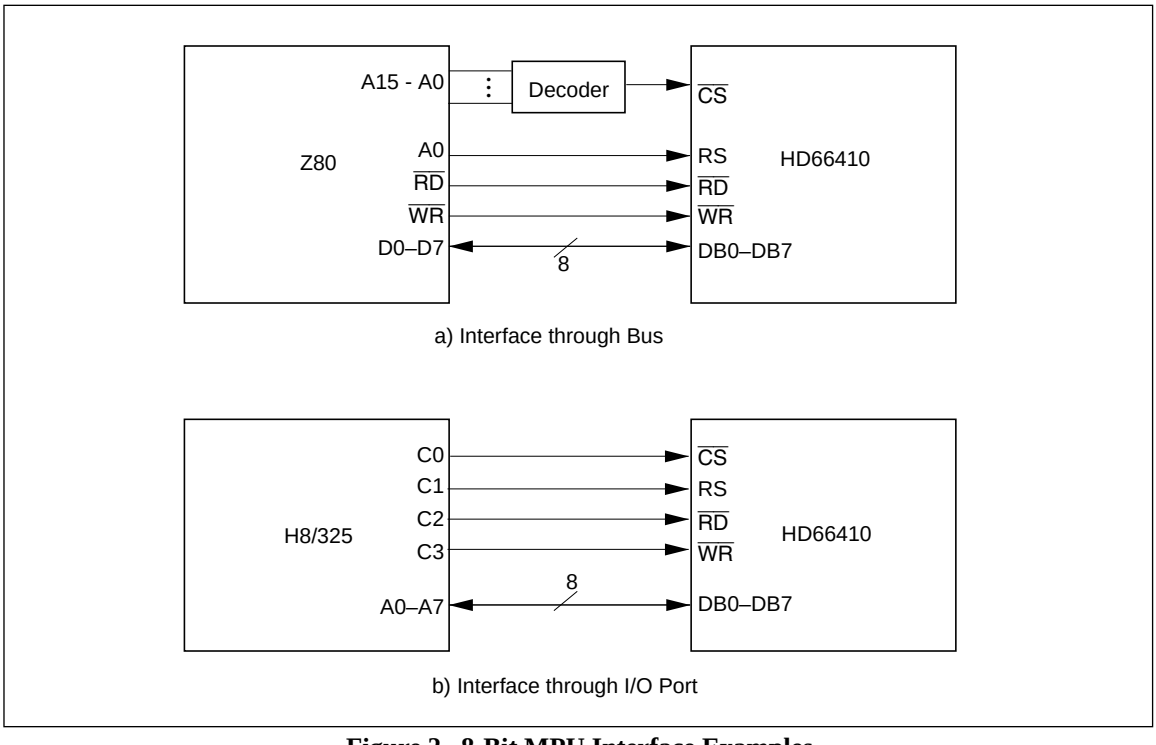


Figure 2 8-Bit MPU Interface Examples

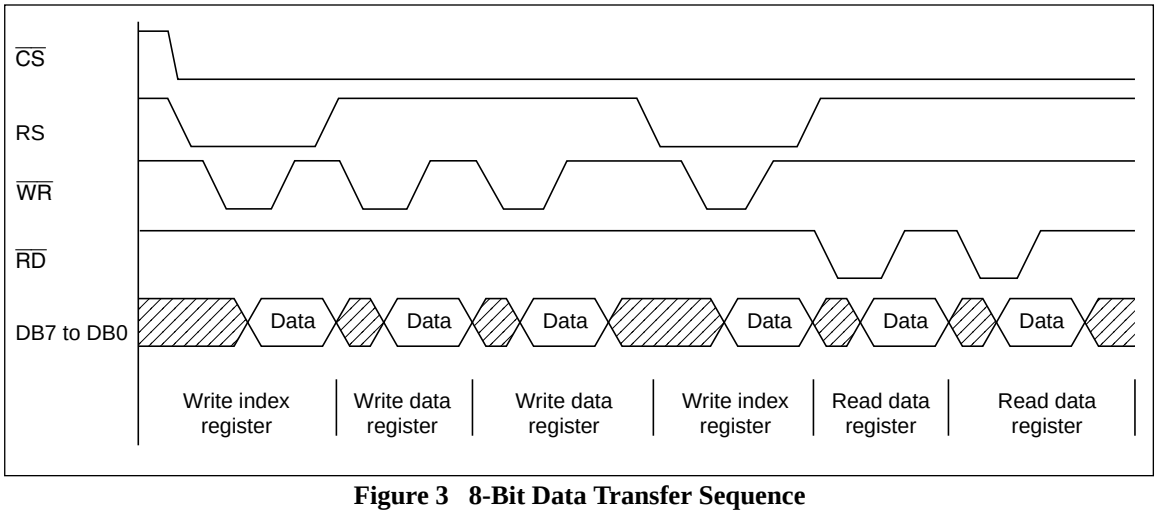


Figure 3 8-Bit Data Transfer Sequence

LCD Driver Configuration

Row/Column Output Assignment: The HD66410 can assign LCD driver output pins X1 to X16 and X129 to X144 to either row or column output depending on the CNF bit value in control register 1, while X17 to X128 and X145 to X161 are fixed to column output and row output, respectively. With this function, row output can be positioned on either one side or two sides of an LCD panel. Figure 4 shows an example where 33-channel row output is positioned to the right of an LCD panel, with X129 to X144 assigned to row output and X1 to X16 assigned to column output. Figure 5 shows an example where 33-channel row output is divided into two and positioned to the right and left of the LCD panel, with X129 to X144 assigned to column output and X1 to X16 assigned to row output.

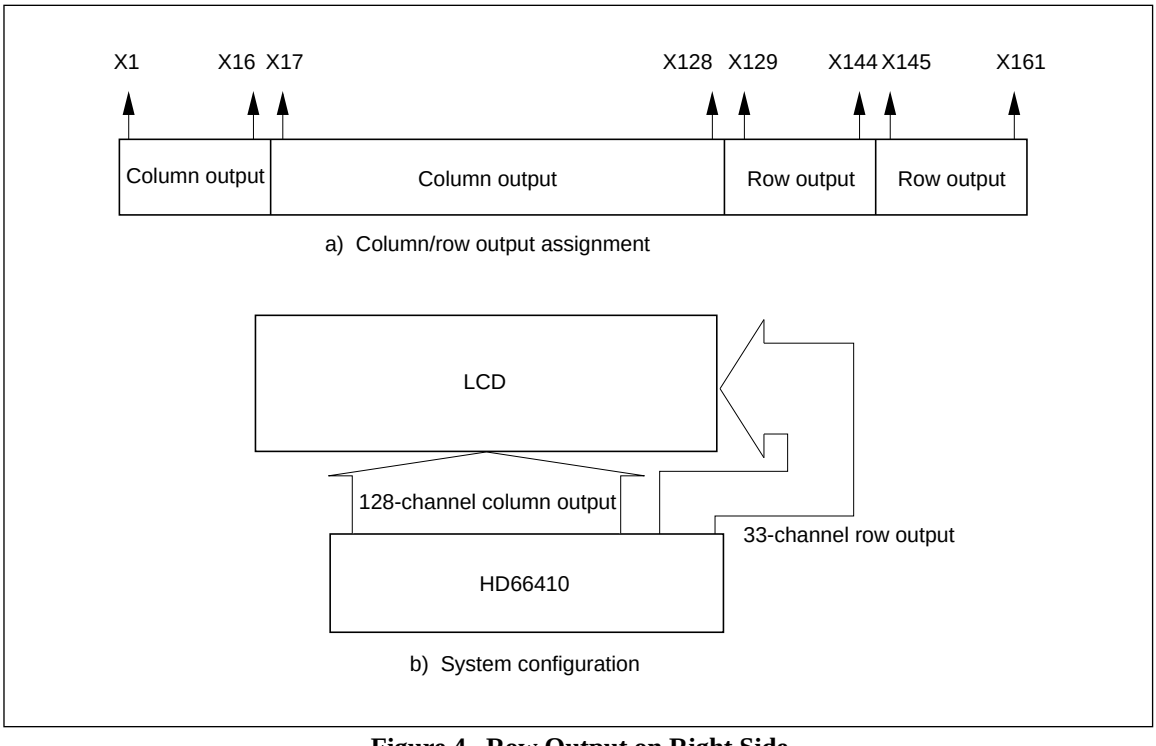
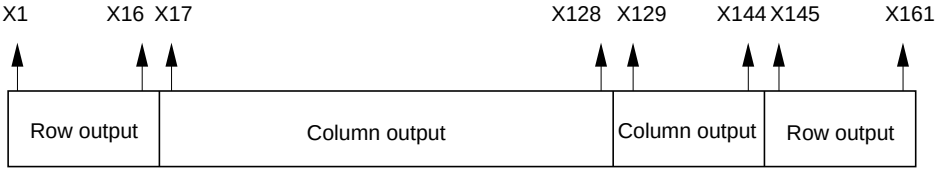
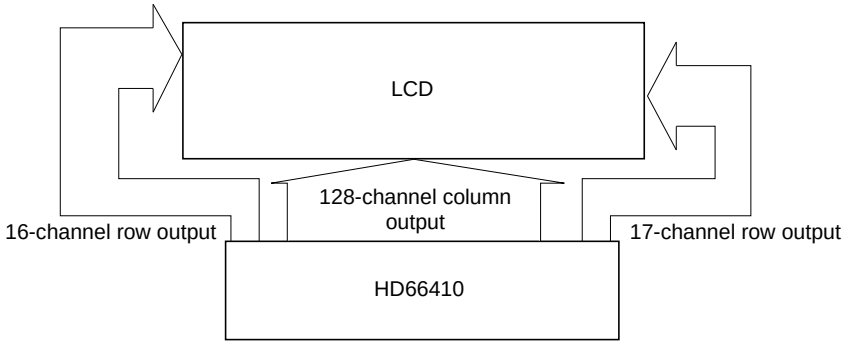


Figure 4 Row Output on Right Side



a) Column/row output assignment



b) System configuration

Figure 5 Row Output on Right and Left Sides

Column Address Inversion According to LCD Driver Layout: The HD66410 can always display data in address $0 on the top left of an LCD panel regardless of where it is positioned with respect to the panel. This is because the HD66410 can invert the positional relationship between display RAM addresses and LCD driver output pins by inverting RAM addresses. Specifically, the HD66410 outputs data in address $0 from X1 (X17) when the ADC bit in control register 1 is 0, and from X128 (X144) otherwise. Here, the scan direction of row output is also inverted according to the situation, as shown in figure 6. Note that addresses and scan direction are inverted when data is written to the display RAM, and thus changing the ADC bit after data has been written has no effect. Therefore, hardware control bits such as CNF and ADC must be set immediately after reset is canceled, and must not be set while data is being displayed.

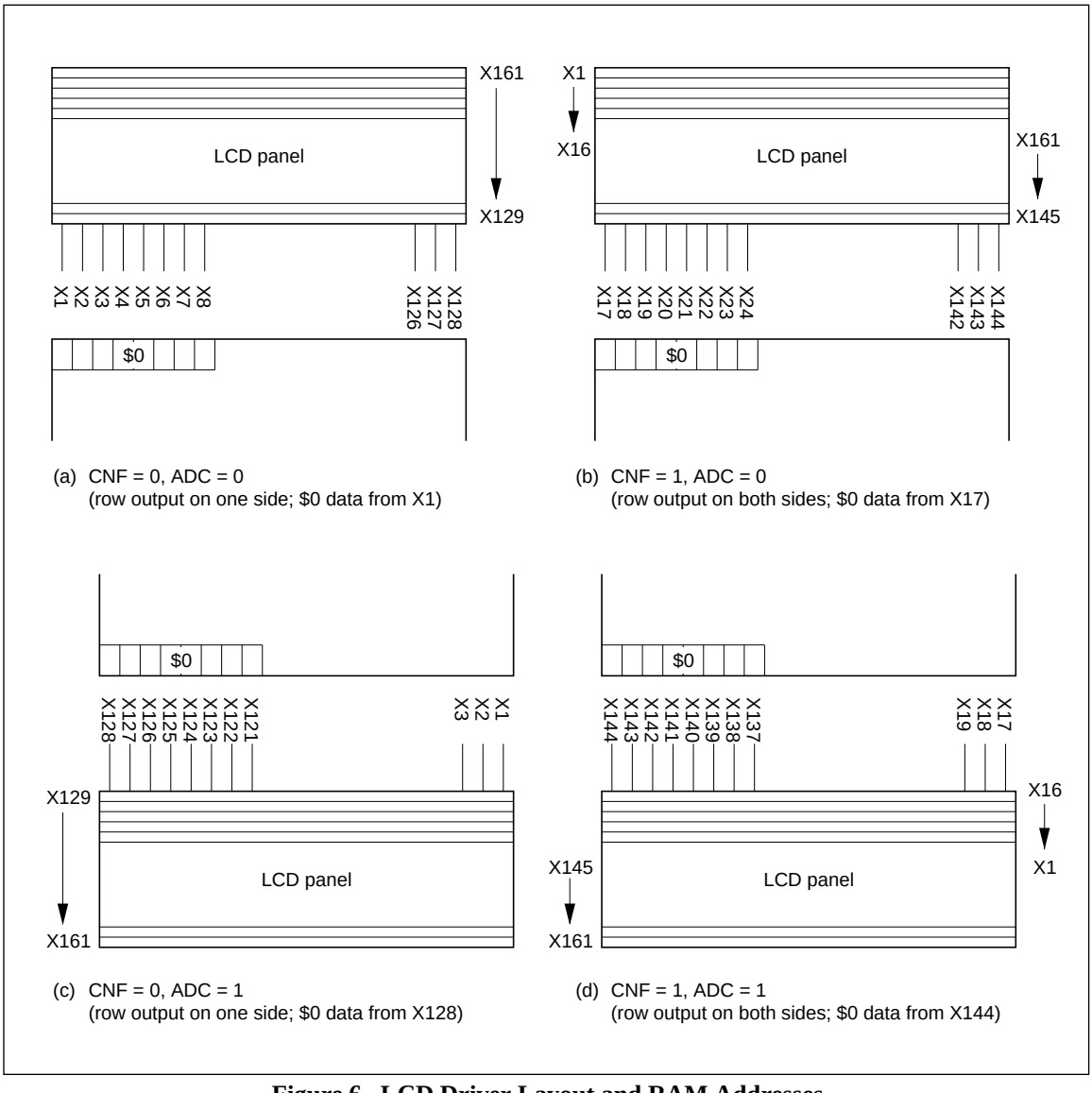


Figure 6 LCD Driver Layout and RAM Addresses

Display RAM Configuration and Display

The HD66410 incorporates a bit-mapped display RAM. It has 128 bits in the X direction and 33 bits in the Y direction. The 128 bits are divided into sixteen 8-bit groups. As shown in figure 7, data written by the MPU is stored horizontally with the MSB at the far left and the LSB at the far right. A display data of 1 turns on (black) the corresponding dot of an LCD panel and 0 turns it off (transparent).

The ADC bit of control register 1 can control the positional relationship between X addresses of the RAM and LCD driver output (figure 8). Specifically, the data in address $0 is output from X1 (X17) when the ADC bit in control register 1 is 0, and from X128 (X144) otherwise. Here, data in each 8-bit group is also inverted. Because of this function, the data in X address $0 can be always displayed on the top left of an LCD panel with the MSB at the far left regardless of the LSI is positioned with respect to the panel.

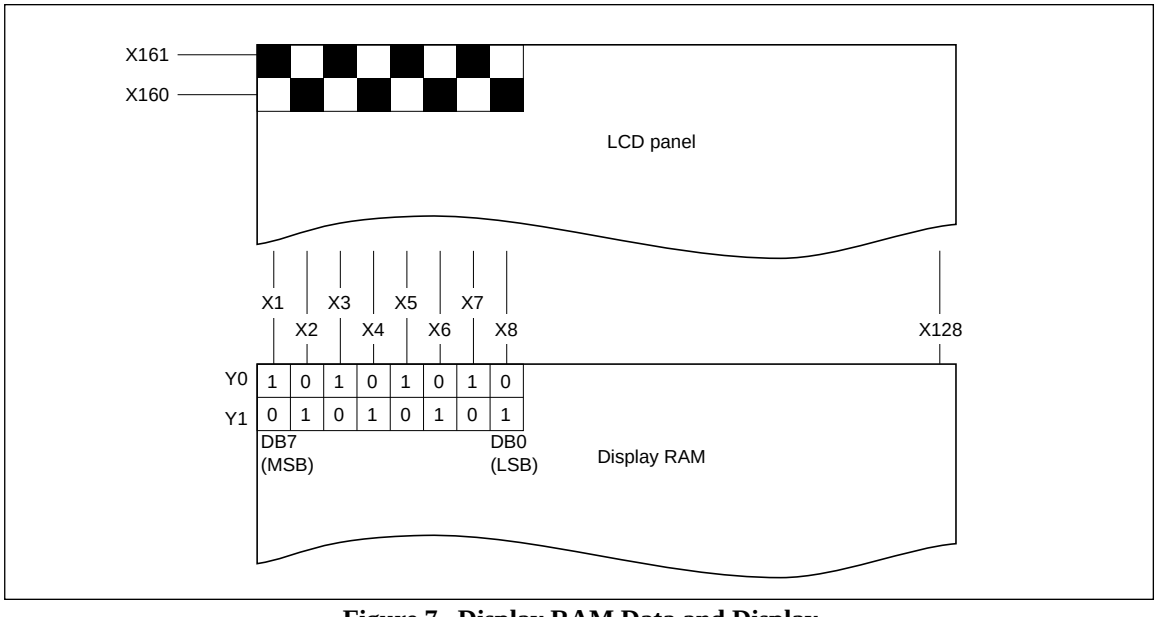


Figure 7 Display RAM Data and Display

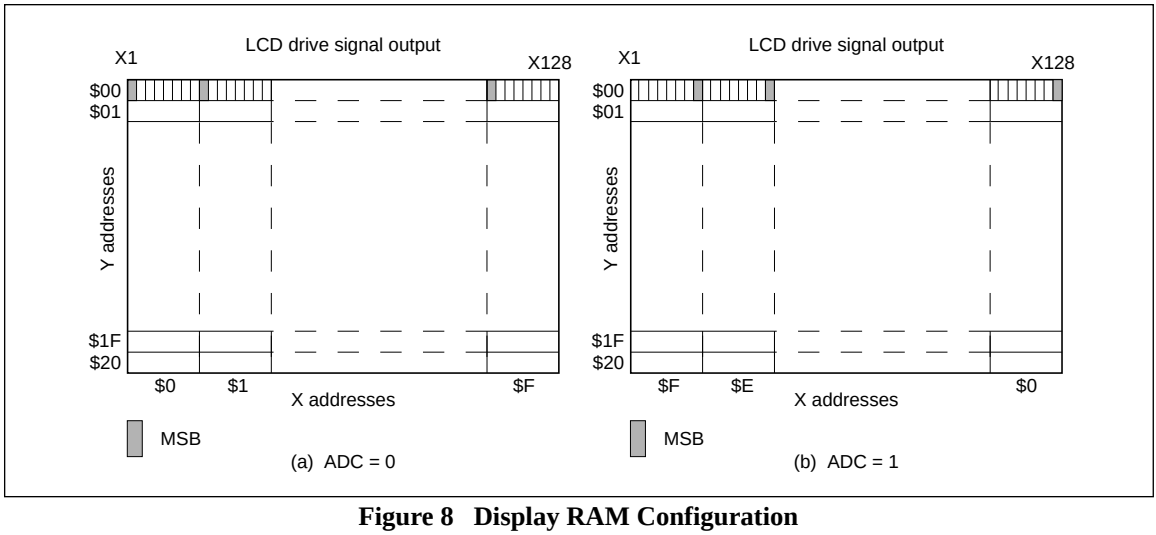


Figure 8 Display RAM Configuration

Access to Internal Registers and Display RAM

Access to Internal Registers by the MPU: The internal registers includes the index register and data registers. The index register can be accessed by driving both the $\overline{CS}$ and RS signals low. To access a data register, first write its register number to the index register with RS set to 0, and then access the data register with RS set to 1. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. Some data registers contain unused bits; they should be set to 0. Note that all data registers except the display memory access register can only be written to.

Access to Display RAM by the MPU: To access the display RAM, first write the RAM address desired to the X address register (R2) and the Y address register (R3). Then read/write the display memory access register (R4). Memory access by the MPU is independent of memory read by the HD66410 and is also asynchronous with the system clock, thus enabling an interface independent of HD66410's internal operations. However, when reading, data is temporarily latched into a HD66410's buffer and then output next time a read is performed in a subsequent cycle. This means that a dummy read is necessary after setting X and Y addresses. The memory read sequence is shown in figure 9.

X and Y addresses are automatically incremented after each memory access according to the INC bit value in control register 2; therefore, it is not necessary to update the addresses for each access. Figure 10 shows two cases of incrementing display RAM address. When the INC bit is 0, the Y address will be incremented up to $3F with the X address unchanged. However, actual memory is valid only within $00 to $20; accessing an invalid address is ignored. When the INC bit is 1, the X address will be incremented up to $F with the Y address unchanged. After address $F, the X address will return to $0; if more than 16 bytes of data are consecutively written, data will be overwritten at the same address.

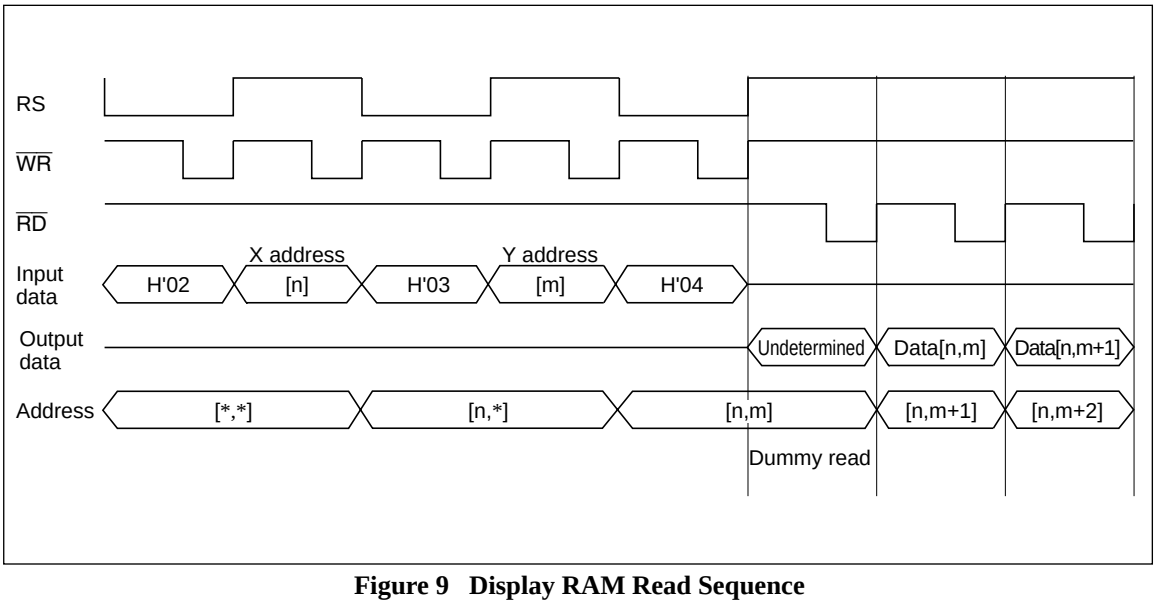


Figure 9 Display RAM Read Sequence

Display RAM Reading by LCD Controller: Data is read by the HD66410 to be displayed asynchronously with accesses by the MPU. However, because simultaneous access could damaging data in the display RAM, the HD66410 internally arbitrates access timing; access by the MPU usually has priority and so access by the HD66410 is placed between accesses by the MPU. Accordingly, an appropriate time must be secured (see the given electrical characteristics between two accesses by the MPU).

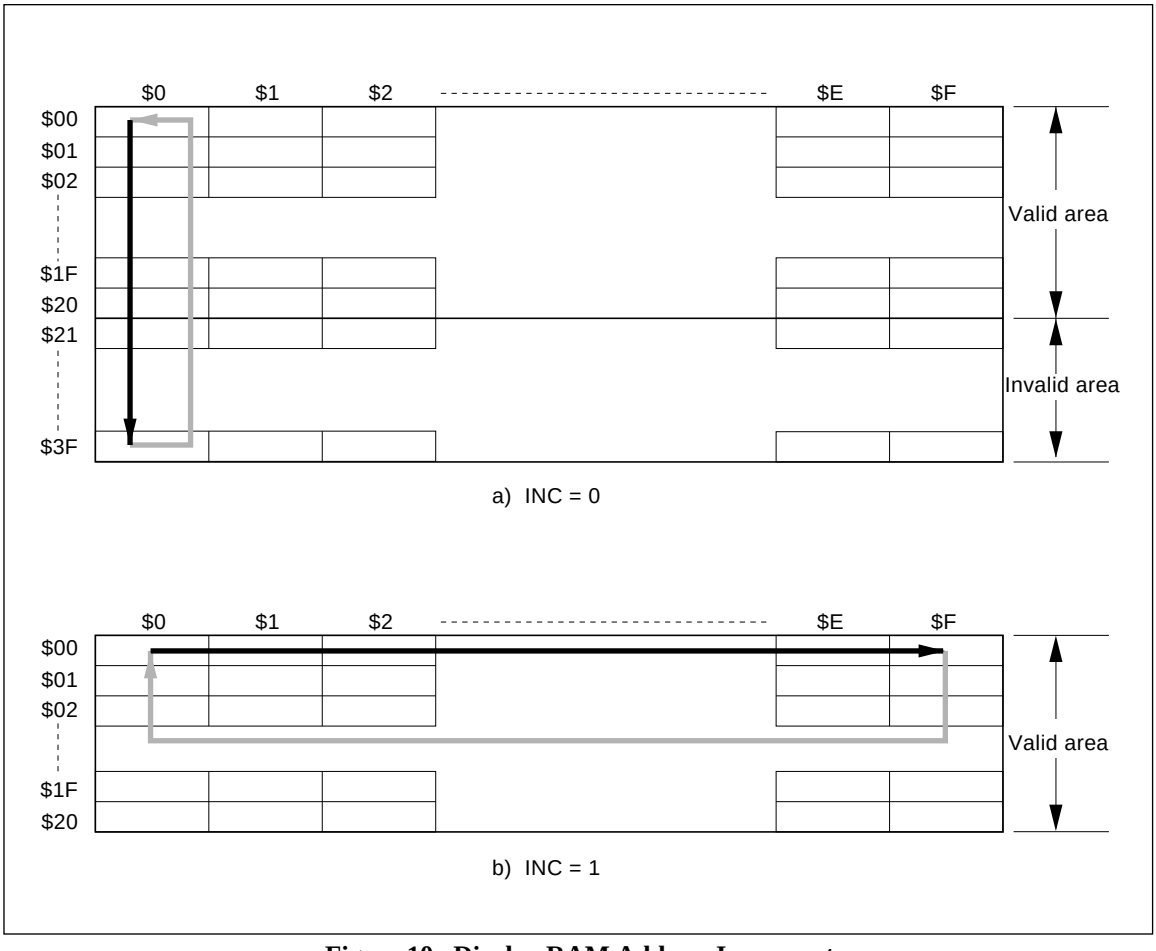


Figure 10 Display RAM Address Increment

Vertical Scroll Function

The HD66410 can vertically scroll a display by varying the top raster to be displayed, which is specified by the display start raster register. Figure 11 shows a vertical scroll example. As shown, when the top raster to be displayed is set to 1, data in Y address $00 is displayed on the 33rd raster. To display another frame on the 33rd raster, therefore, data in Y address $00 must be modified after setting the top raster.

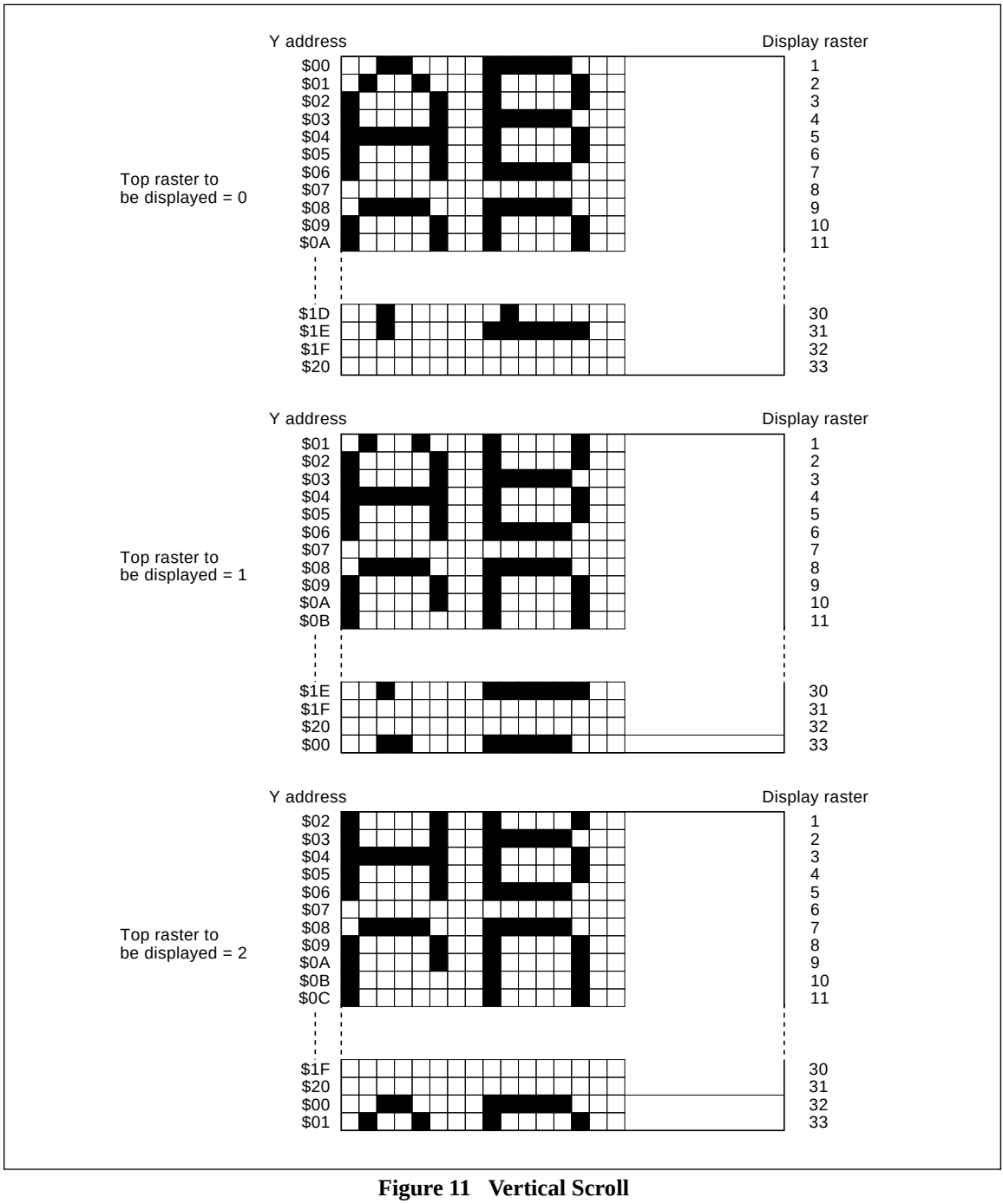


Figure 11 Vertical Scroll

Blink Function

Blinking Dot-Matrix Display Area: The HD66410 can blink a specified area on the dot-matrix display. Blinking is achieved by repeatedly turning on and off the specified area at a frequency of one sixty-fourth the frame frequency. For example, when the frame frequency is 80 Hz, the area is turned on and off every 0.8 seconds.

The area to be blinked can be designated by specifying vertical and horizontal positions of the area. The vertical position, or the rasters to be blinked, are specified by the blink start raster register (R8) and blink end raster register (R9). The horizontal position, or the dots to be blinked in the specified rasters, are specified by the blink registers (R6 and R7) in an 8-dot group; each data bit in the blink registers controls its corresponding 8-dot group. The relationship between the registers and blink area is shown in figure 12. Setting the BLK bit to 1 in control register 2 after setting the above registers starts blinking the designated area. Note that since the area to be blinked is designated absolutely with respect to the display RAM, it will move along with a scrolling display (figure 13).

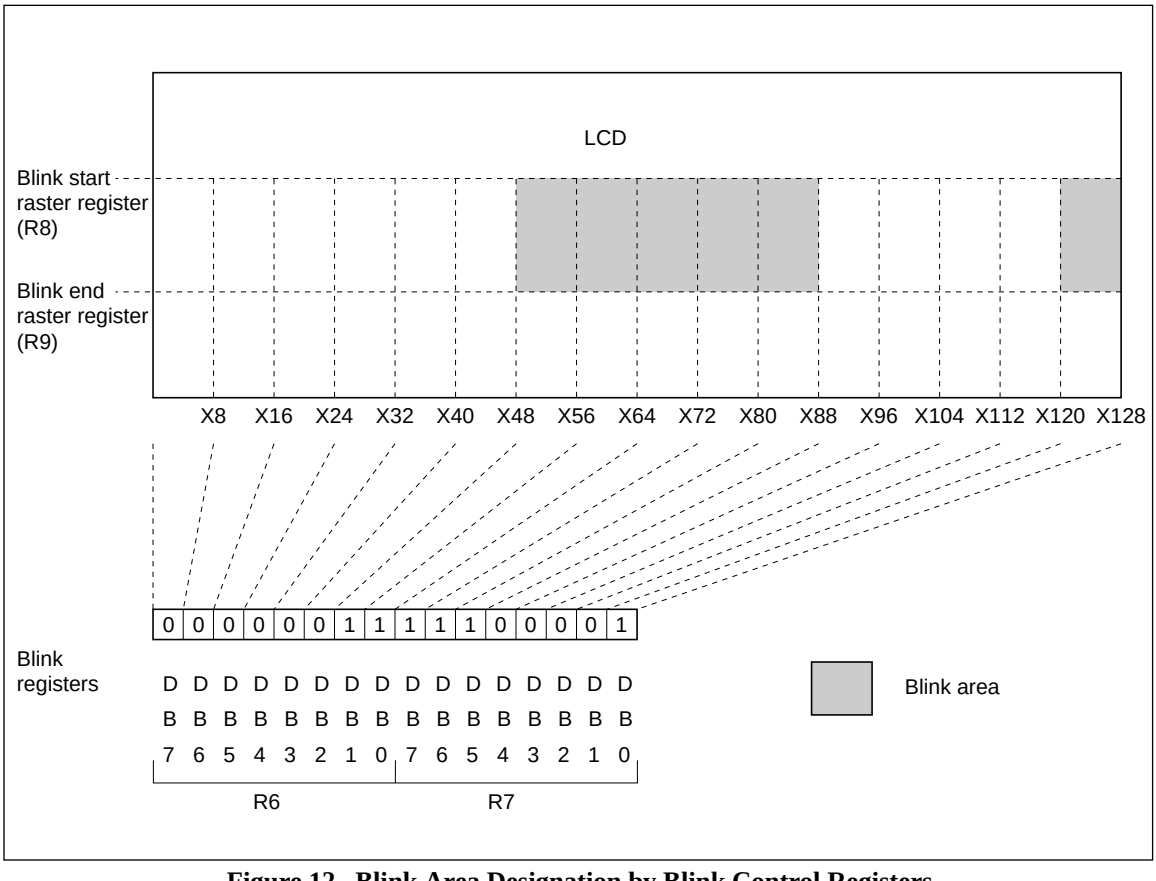
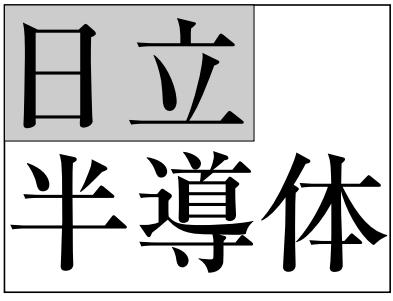
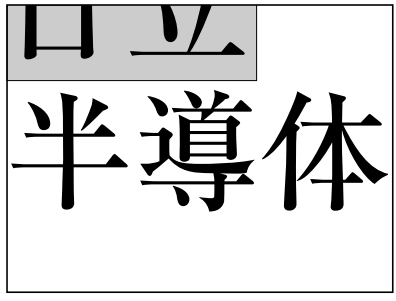


Figure 12 Blink Area Designation by Blink Control Registers



Display start raster = 0
Blink start raster = 0
Blink end raster = H'F



Display start raster = H'5
Blink start raster = H'5
Blink end raster = H'F

Figure 13 Scrolling Blink Area

Blinking Annunciator Display Area: The HD66410 can blink up to 18 dots among a maximum of 72 dots on the annunciator display. This function is controlled by a blink controller independent of that for the main dot-matrix display part. The dots to be blinked can be designated by annunciator blink registers 1, 2, and 3, each of which contains two bits to specify a block and six bits to specify dots to be blinked in the specified block (figures 14 and 15).

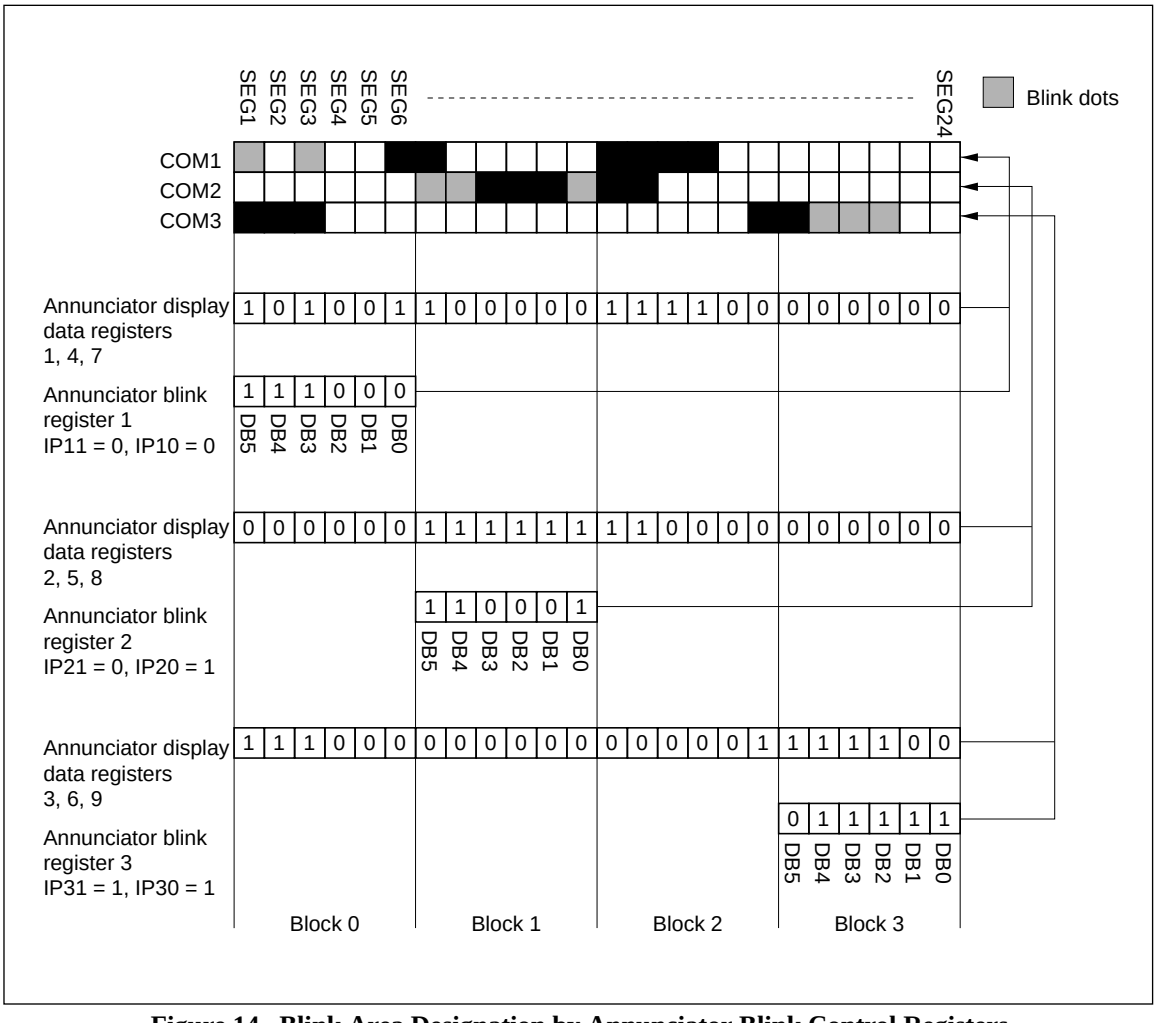
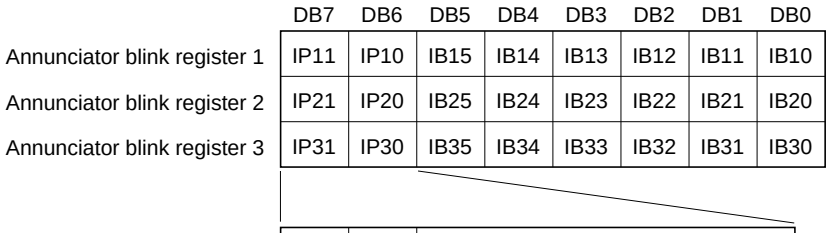


Figure 14 Blink Area Designation by Annunciator Blink Control Registers



IPn1	IPn0	Blink Block
0	0	Block 0 (SEG1–SEG6)
0	1	Block 1 (SEG7–SEG12)
1	0	Block 2 (SEG13–SEG18)
1	1	Block 3 (SEG19–SEG24)

IPn1, IPn0: Block select bits (n = 1, 2, 3)

Figure 15 Annunciator Blink Registers

Power Down Modes

The HD66410 has a standby function providing low power-dissipation, which is initiated by internal register settings. There are two standby modes: in one, all the HD66410 functions are inactive, and in the other, only the annunciator display function is active. In both modes, the internal booster halts but data in the display RAM and internal registers except the DISP bit is retained. However, only control registers can be accessed during standby modes. In the standby mode with annunciator display, the oscillator does not halt, thus dissipating more power than in the other standby mode. Table 1 lists the LCD driver output pin status during standby modes. Figure 16 shows the procedure for initiating and canceling a standby mode. Note that the cancelation procedure must be strictly followed to protect data in the display RAM.

Table 1 Output Pin Status during Standby Modes

X1 to X161	Output V_{CC} (display off)	
COM1 to COM3	OSC = 0	Output V_{CC} (display off)
	OSC = 1	Output common signals (display on)
SEG1 to SEG24	OSC = 0	Output V_{CC} (display off)
	OSC = 1	Output segment signals (display on)

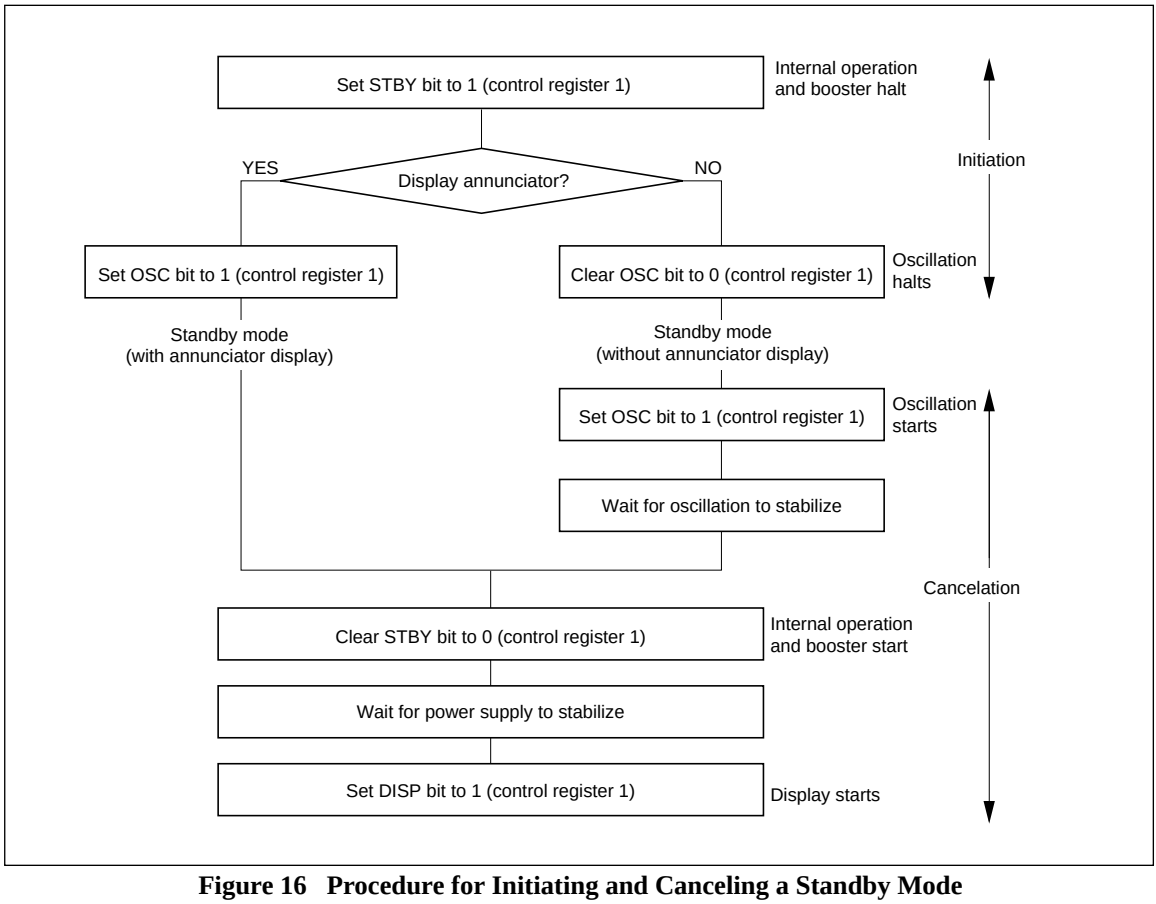


Figure 16 Procedure for Initiating and Canceling a Standby Mode

Power On/Off Procedure

Figure 17 shows the procedure for turning the power supply on and off. This procedure must be strictly followed to prevent incorrect display because the HD66410 incorporates all power supply circuits .

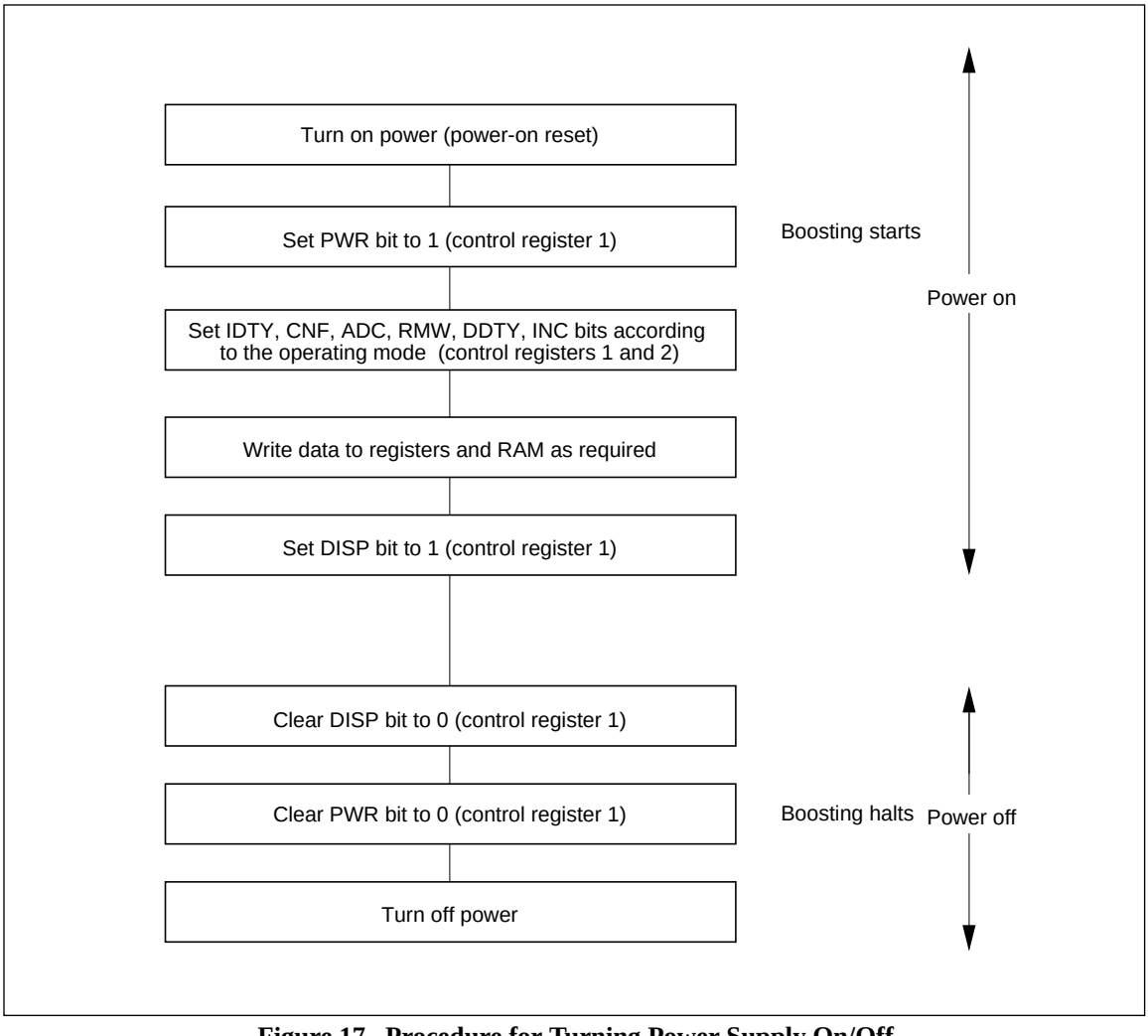


Figure 17 Procedure for Turning Power Supply On/Off

Annunciator Display Function

The HD66410 can display up to 72 dots of annunciator using 24 segment (column) drivers (SEG1 to SEG24) and three common (row) drivers (COM1 to COM3). These drivers, independent of the display RAM, operate statically or with a 1/3 duty cycle. They are available even during standby modes, where dot-matrix display and the internal booster is turned off, making them suitable for time and other mark indications with reduced power dissipation.

The dots to be displayed are designated by annunciator display data registers 1 to 9. For static drive, only display data registers 1, 4, and 7 and row driver COM1 are used. A maximum of 18 turned-on dots can be blinked. For details on blinking, see the Blink Function section. Figure 18 shows the relationship between annunciator display data register bits and display positions. In the figure, alphanumerics in the ovals indicate the bit names of annunciator display data registers. Data value 1 turns on the corresponding dot on the panel, and data value 0 turns off the corresponding dot. Table 2 lists the annunciator display data registers.

Table 2 Annunciator Display Data Register Bits

Register		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Annunciator display data register 1	A0	IC1A	IC1B	IC1C	IC1D	IC1E	IC1F	IC1G	IC1H
Annunciator display data register 2	A1	IC2A	IC2B	IC2C	IC2D	IC2E	IC2F	IC2G	IC2H
Annunciator display data register 3	A2	IC3A	IC3B	IC3C	IC3D	IC3E	IC3F	IC3G	IC3H
Annunciator display data register 4	A3	IC1I	IC1J	IC1K	IC1L	IC1M	IC1N	IC1O	IC1P
Annunciator display data register 5	A4	IC2I	IC2J	IC2K	IC2L	IC2M	IC2N	IC2O	IC2P
Annunciator display data register 6	A5	IC3I	IC3J	IC3K	IC3L	IC3M	IC3N	IC3O	IC3P
Annunciator display data register 7	A6	IC1Q	IC1R	IC1S	IC1T	IC1U	IC1V	IC1W	IC1X
Annunciator display data register 8	A7	IC2Q	IC2R	IC2S	IC2T	IC2U	IC2V	IC2W	IC2X
Annunciator display data register 9	A8	IC3Q	IC3R	IC3S	IC3T	IC3U	IC3V	IC3W	IC3X

Note: Only annunciator display data registers 1, 4, and 7 are used for static display.

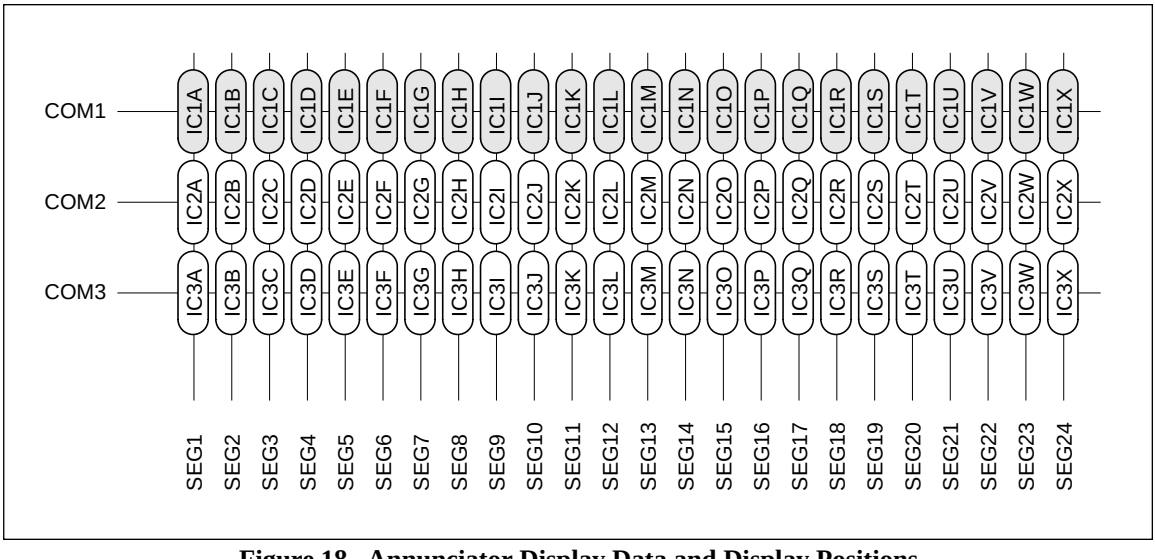


Figure 18 Annunciator Display Data and Display Positions

Oscillator

The HD66410 incorporates an R-C oscillator with low power-dissipation, in which the oscillation frequency can be adjusted by appropriate selection of oscillator resistor Rf and capacitor Cf. The adjusted clock signal is used for system internal circuits; thus, if this oscillator is not used, an appropriate clock signal must be externally input through the CR pin. In this case, the C and R pins must be left unconnected. Figure 19 shows oscillator connections.

Clock and Frame Frequency

The HD66410 generates the frame frequency (LCD drive frequency) by dividing the input clock frequency by 132. The division ratio is the same for all LCD duty cycles.

The frame frequency is usually 70 to 90 Hz; when the frame frequency is 80 Hz, for example, the input clock frequency must be 10.56 kHz.

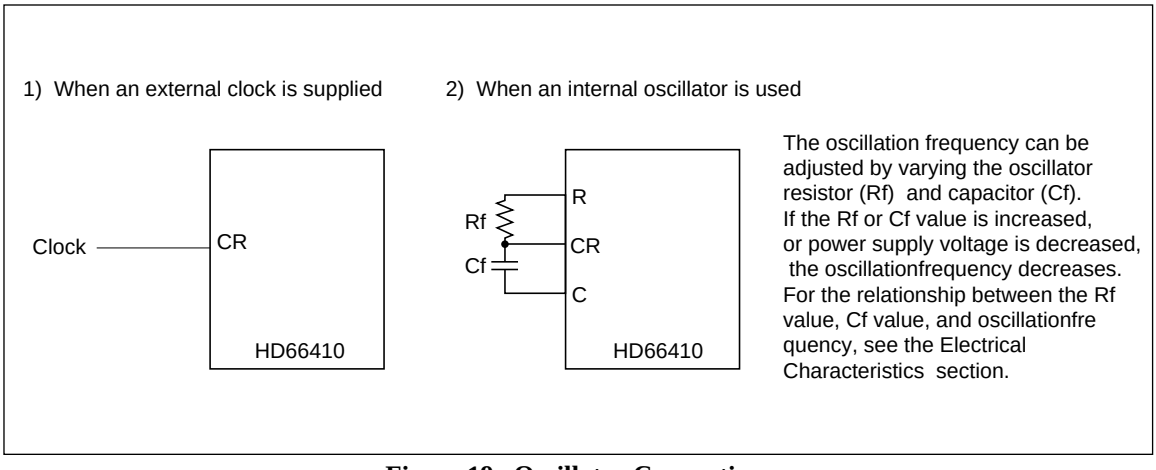
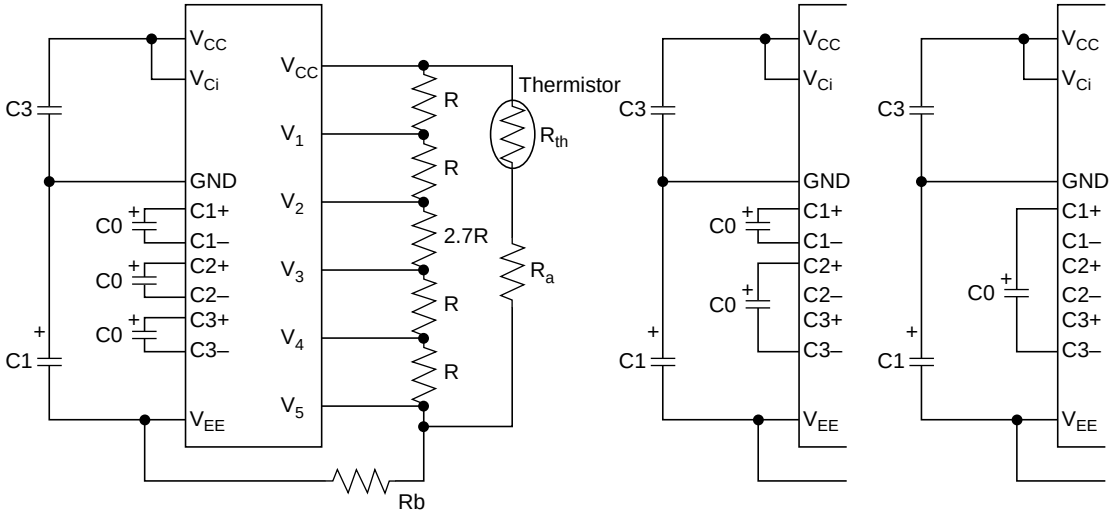


Figure 19 Oscillator Connections

Power Supply Circuits

The HD66410 incorporates a double to quadruple booster to supply power to LCD drivers. The booster is automatically turned off during standby mode, dissipating no power. If the current capacity provided is insufficient for the user system, external power supply circuits are necessary. In this case, the internal power supply can be turned off by register settings. Figure 20 shows examples of power supply circuits for different boosting ratios.

Booster: The internal booster raises the input voltage between V_{CC} and GND two to four times every raster by turning on the internal power supply with capacitors attached between C1+ and C1-, C2+ and C2-, C3+ and C3-, and to V_{EE}. The booster uses the system clock, and thus the internal oscillator must be operating to activate the booster (if the internal oscillator has been selected to generate the system clock).



C0 ≥ 1.0 µF
C0 ≥ 2.2 µF

a) Quadruple boosting

C2–, C3+: open

b) Triple boosting

C1–, C2+, C2–, C3+: open

c) Double boosting

Notes: 1. Adjust the power supply voltage and capacitance of external capacitors according to the characteristics of the LCD used because the output voltage (V_{EE}) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors, and manufacturing tolerance. Refer to the Electrical Characteristics section for details.

2. Adjust the power supply voltage so that the output voltage (V_{EE}) after boosting will not exceed the absolute maximum rating of the LCD power supply voltage (13 V).

3. Vci is both a reference voltage and power supply for the booster; it needs to be supplied with at least three times the current consumed by the LCD drivers including the current flowing in the resistive divider. Make sure that Vci is below V_{CC}.

4. Be sure to connect polarized capacitors correctly.

Figure 20 Power Supply Circuit Examples

LCD Drive Voltage Power Supply Levels: To drive the LCD, a 6-level power supply is necessary. These levels can be usually generated by dividing the V_{CC}–V5 power supply using resistive dividers. If the total resistance is small, current consumption increases, and if the total resistance is large, display quality degrades. Appropriate resistance should be selected for the user system.

Brightness Adjust: The booster drives liquid crystals with a voltage after raising the voltage supplied to the Vci pin two to four times. Accordingly, brightness can be adjusted by varying the Vci level. Attaching a thermister is recommended to vary the voltage according to the thermal characteristics of liquid crystals.

Row/Column Output Switchover: LCD column drivers use V_{CC}, V2, V3, and V5, while row drivers use V_{CC}, V1, V4, and V5. These voltage levels are switched to AC and are output to an LCD panel. Since the HD66410 can assign X1 to X16 and X129 to X144 to either row or column output, the power supply connection must be externally changed according to the assignment, which is determined by the CNF bit value in control register 1. The select and deselect levels for row output are temporarily output from the V_{CHO} and V_{CLO} pins, and the two levels for column output are output from the V_{SHO} and V_{SLO} pins; these outputs must be connected according to row and column output assignment as shown in figure 21.

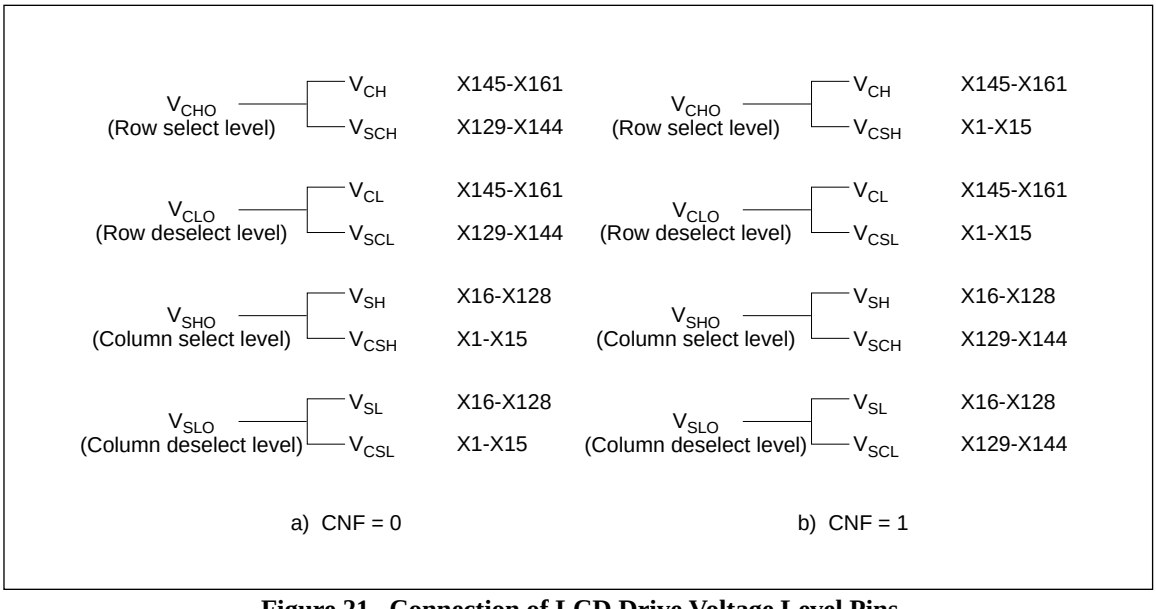


Figure 21 Connection of LCD Drive Voltage Level Pins

Reset

The low $\overline{\text{RESET}}$ signal initializes the HD66410, clearing all the bits in the internal registers. During reset, the internal registers cannot be accessed.

Note that if the reset conditions specified in the Electric Characteristics section are not satisfied, the HD66410 will not be correctly initialized. In this case, the internal registers of the HD66410 must be initialized by software.

Initial Setting of Internal Registers: All the internal register bits are cleared to 0. Details are listed below.

- Data registers (DR: R0 to R9, A0 to A11)
  - — Normal operation
  - — Oscillator is active
  - — Display is off (including annunciator display)
  - — Booster is not used
  - — Y address of display RAM is incremented
  - — 1/33 duty cycle
  - — X and Y addresses are 0
  - — Data in address $0 is output from the X1 pin
  - — Blink function is inactive

Initial Setting of Pins:

- Bus interface pins
  During reset, the bus interface pins do not accept signals to access internal registers; data is undefined when read.

- LCD driver output pins
  During reset, all the LCD driver output pins (X1 to X161, SEG1 to SEG33, COM1 to COM3) output V_{CC}-level voltage, regardless of data value in the display RAM, turning off the LCD. Here, the output voltage is not alternated. Note that the same voltage (V_{CC}) is applied to both column and row output pins to prevent liquid crystals from degrading.

- Booster output pins
  Since the PWR bit in control register 1 is 0 during reset, the booster halts. Accordingly, the output state of the V_{EE} pin depends on the value of the booster's external capacitor.

Internal Registers

The HD66410 has one index register and 22 data registers, all of which can be accessed asynchronously with the internal clock. All the registers except the display memory access register are write-only. Accessing unused bits or addresses affects nothing; unused bits should be set to 0 when written to.

Index Register (IR): The index register (figure 22) selects one of 22 data registers. The index register itself is selected when both the $\overline{CS}$ and RS signals are low. Data bits 7 to 5 are unused; they should be set to 0 when written to.

Control Register 1 (R0): Control register 1 (figure 23) controls general operations of the HD66410. Each bit has its own function as described below. Data bit 7 bit is unused; it should be set to 0 when written to.

- DSP bit
  DSP = 1: Display on
  DSP = 0: Display off (all LCD driver output pins output V_{CC} level)

- STBY bit
  STBY = 1: Internal operation and booster halt; display off
  STBY = 0: Normal operation
  The STBY bit does not affect the state of PWR and DISP bit.

- PWR bit
  PWR = 1: Booster active
  PWR = 0: Booster inactive

- OSC bit
  OSC = 1: Internal operation and booster halt; oscillator does not halt to provide annunciator display
  OSC = 0: Internal operation, booster, and oscillator halt
  The OSC bit is valid only when the STBY bit is 1.

- IDTY bit
  IDTY = 1: Annunciator display signals are operating statically
  IDTY = 0: Annunciator display signals are operating with 1/3 duty cycle

- CNF bit
  CNF = 1: Row output on both sides of the LCD panel
  CNF = 0: Row output on one side of the LCD panel

- ADC bit
  ADC = 1: Data in X address $0 is output from X128 or X144; row signals are scanned from X129 to X161.
  ADC = 0: Data in X address $0 is output from X1 or X17; row signals are scanned from X161 to X129.

	Data bit	7	6	5	4	3	2	1	0
IR	Set value				Register number				

Figure 22 Index Register (IR)

	Data bit	7	6	5	4	3	2	1	0
R0	Set value		DISP	STBY	PWR	OSC	IDTY	CNF	ADC

Figure 23 Control Register 1 (R0)

Control Register 2 (R1): Control register 2 (figure 24) controls general operations of the HD66410. Each bit has its own function as described below. Data bits 7 to 4 are unused; they should be set to 0 when written to.

- RMW bit
  RMW = 1: Read-modify-write mode
  Address is incremented only after write access
  RMW = 0: Address is incremented after both write and read accesses

- DDTY bit
  DDTY = 1: 1/17 display duty cycle
  DDTY = 0: 1/33 display duty cycle

- INC bit
  INC = 1: X address is incremented for each access
  INC = 0: Y address is incremented for each access

- BLK bit
  BLK = 1: Blink function is used
  BLK = 0: Blink function is not used
  The blink counter is reset when the BLK bit is set to 0. It starts counting and at the same time initiates blinking when the BLK bit is set to 1.

X Address Register (R2): The X address register (figure 25) designates the X address of the display RAM to be accessed by the MPU. The set value must range from $0 to $F; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bits 7 to 3 are unused; they should be set to 0 when written to.

Y Address Register (R3): The Y address register (figure 26) designates the Y address of the display RAM to be accessed by the MPU. The set value must range from $00 to $20; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bit 7 is unused; it should be set to 0 when written to.

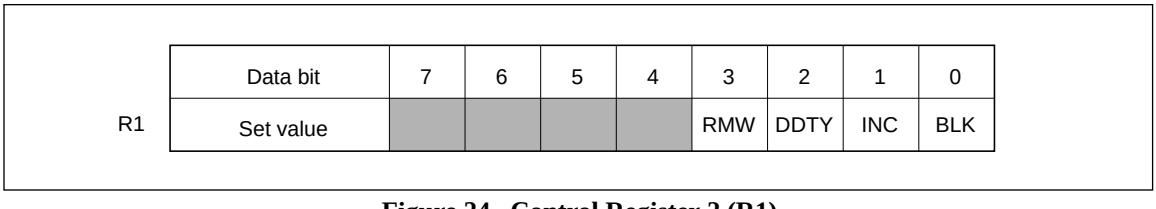


Figure 24 Control Register 2 (R1)

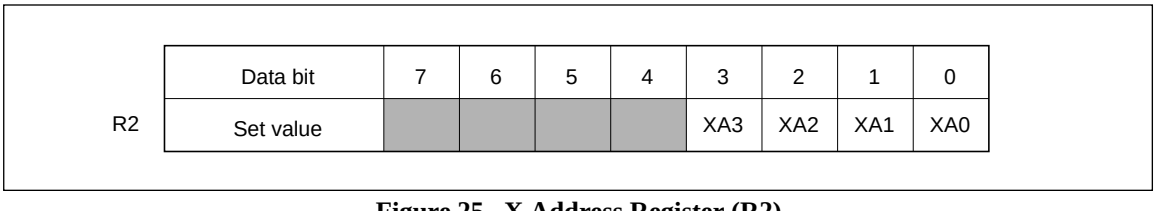


Figure 25 X Address Register (R2)

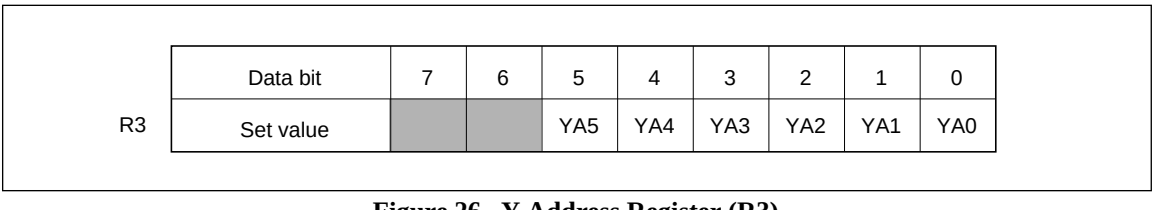


Figure 26 Y Address Register (R3)

Display Memory Access Register (R4): The display memory access register (figure 27) is used to access the display RAM. If this register is write-accessed, data is directly written to the display RAM. If this register is read-accessed, data is first latched to this register from the display RAM and sent out to the data bus on the next read; therefore, a dummy read access is necessary after setting the display RAM address.

Display Start Raster Register (R5): The display start raster register (figure 28) designates the raster to be displayed at the top of the LCD panel. Varying the set value scrolls the display vertically. The set value must be one less than the actual top raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. If the value is set outside these ranges, data may not be displayed correctly. Data bits 7 and 6 are unused; they should be set to 0 when written to.

Blink Registers (R6, R7): The blink bit registers (figure 29) designate the 8-bit groups to be blinked. Setting a bit to 1 blinks the corresponding 8-bit group. Any number of groups can be blinked; setting all the bits to 1 will blink the entire LCD panel. These bits are valid only when the BLK bit of control register 2 is 1.

	Data bit	7	6	5	4	3	2	1	0
R4	Set value	D7	D6	D5	D4	D3	D2	D1	D0

Figure 27 Display Memory Access Register (R4)

	Data bit	7	6	5	4	3	2	1	0
R5	Set value			ST5	ST4	ST3	ST2	ST1	ST0

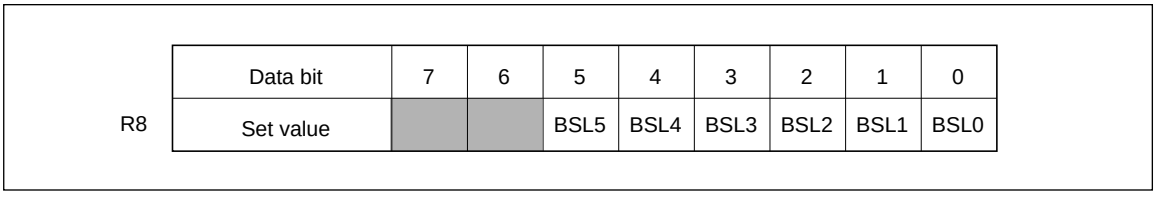
Figure 28 Display Start Raster Register (R5)

	Data bit	7	6	5	4	3	2	1	0
R6	Set value	BK0	BK1	BK2	BK3	BK4	BK5	BK6	BK7
R7	Set value	BK8	BK9	BK10	BK11	BK12	BK13	BK14	BK15

Figure 29 Blink Registers (R6, R7)

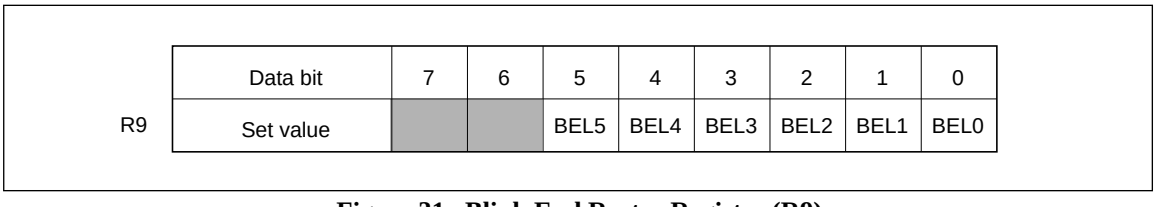
Blink Start Raster Register (R8): The blink start raster register (figure 30) designates the top raster in the area to be blinked. The set value must be one less than the actual top raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. If the value is set outside these ranges, operations may not be correct. Data bits 7 and 6 are unused; they should be set to 0 when written to.

Blink End Raster Register (R9): The blink end raster register (figure 31) designates the bottom raster in the area to be blinked. The area to be blinked is designated by the blink registers, blink start raster register, and blink end raster register. The set value must be one less than the actual bottom raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. It must also be greater than the value set in the blink start raster register. If an inappropriate value is set, operations may not be correct. Data bits 7 and 6 are unused; they should be set to 0 when written to.



	Data bit	7	6	5	4	3	2	1	0
R8	Set value			BSL5	BSL4	BSL3	BSL2	BSL1	BSL0

Figure 30 Blink Start Raster Register (R8)



	Data bit	7	6	5	4	3	2	1	0
R9	Set value			BEL5	BEL4	BEL3	BEL2	BEL1	BEL0

Figure 31 Blink End Raster Register (R9)

Annunciator Display Data Registers (A0 to A8): The annunciator display data registers (figure 32) store data for annunciator (icon) display. Setting a data bit to 1 turns on the corresponding dot on the LCD panel.

Annunciator Blink Registers (A9 to A11): The annunciator blink registers (figure 33) designate bits to be blinked on the annunciator display. For details, see the Blink Function section.

- IPn1, IPn0 bits (n = 1, 2, 3)
  These bits select annunciator blocks to be blinked.
  IPn1, IPn0 = 0, 0: Block 0 is selected (SEG1 to SEG6)
  IPn1, IPn0 = 0, 1: Block 1 is selected (SEG7 to SEG12)
  IPn1, IPn0 = 1, 0: Block 2 is selected (SEG13 to SEG18)
  IPn1, IPn0 = 1, 1: Block 3 is selected (SEG19 to SEG24)
- IBn5, IBn0 bits (n = 1, 2, 3)
  These bits select bits to be blinked in the selected blocks.

	Data bit	7	6	5	4	3	2	1	0
A0	Set value	IC1A	IC1B	IC1C	IC1D	IC1E	IC1F	IC1G	IC1H
A1	Set value	IC2A	IC2B	IC2C	IC2D	IC2E	IC2F	IC2G	IC2H
A2	Set value	IC3A	IC3B	IC3C	IC3D	IC3E	IC3F	IC3G	IC3H
A3	Set value	IC1I	IC1J	IC1K	IC1L	IC1M	IC1N	IC1O	IC1P
A4	Set value	IC2I	IC2J	IC2K	IC2L	IC2M	C2N	IC2O	IC2P
A5	Set value	IC3I	IC3J	IC3K	IC3L	IC3M	C3N	IC3O	IC3P
A6	Set value	IC1Q	IC1R	IIC1S	IC1T	IC1U	IIC1V	IIC1W	IC1X
A7	Set value	IC2Q	IC2R	IC2S	IC2T	IC2U	IC2V	IC2W	IC2X
A8	Set value	IC3Q	IC3R	IC3S	IC3T	IC3U	IC3V	IC3W	IC3X

Figure 32 Annunciator Display Data Registers (A0 to A8)

	Data bit	7	6	5	4	3	2	1	0
A9	Set value	IP11	IP10	IB15	IB14	IB13	IB12	IB11	IB10
A10	Set value	IP21	IP20	IB25	IB24	IB23	IB22	IB21	IB20
A11	Set value	IP31	IP30	IB35	IB34	IB33	IB32	IB31	IB30

Figure 33 Annunciator Blink Registers (A9 to A11)

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuits	V_{EE}	V_{CC} – 18.0 to V_{CC} + 0.3	V	
Input voltage 1		V_{T1}	–0.3 to VCC + 0.3	V	1, 2
Input voltage 2		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. Measured relative to GND.

2. Applies to pins CR, DB7 to DB0, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, RS, $\overline{RES}$, TEST0, AV3.
3. Applies to pins V1, V2, V3, V4, V5, C1+, C1–, C2+, C2–, C3+, C3–, V_{SH}, V_{SL}, V_{CH}, V_{CL}, V_{SCH}, V_{SCL}, V_{CSH}, V_{CSL}.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics to prevent malfunction or unreliability.

Electrical Characteristics

Table 3 DC Characteristics (V_{CC} = 2.2 to 3.6 V, GND = 0 V, V_{CC}–V5 = 6 to 15 V, Ta = –20 to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input leakage current (1)	I_{IL1}	Except for DB0 to DB7	–1.0	—	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current (2)	I_{IL1}	DB7 to DB0	–2.5	—	2.5	µA	$V_{IN} = V_{CC}$ to GND	
Driver “on” resistance (1)	R_{COM}	X1 to X16, X129 to X161	—	—	20	kΩ	I_{ON} = 100 µA V_{CC} – V5 = 8 V	
Driver “on” resistance (2)	R_{SEG}	X17 to X128	—	—	30	kΩ	I_{ON} = 100 µA V_{CC} – V5 = 8 V	
Driver “on” resistance (3)	R_{ICON}	COM_1 to COM_3, SEG_1 to SEG_{24}	—	—	50	kΩ	I_{ON} = 100 µA	
Input high voltage	V_{IH1}		$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	V_{IL1}		0	—	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}		$0.8 \times V_{CC}$	—	—	V	I_{OH} = –50 µA	
Output low voltage	V_{OL}		—	—	$0.2 \times V_{CC}$	V	I_{OL} = 50 µA	
Current consumption during display	I_{DISP}				T.B.D.	µA		1
Current consumption during standby (1)	I_{STB1}				T.B.D.	µA	Annunciator displayed	2
Current consumption during standby (2)	I_{STB2}				T.B.D.	µA	Annunciator not displayed	3
Current consumption during RAM access	I_{CC}				T.B.D.	µA		

Notes: 1. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

2. Measured when STBY bit = 1 and OSC (ICON) bit = 1

3. Measured when STBY bit = 1 and OSC (ICON) bit = 0

Table 4 Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions	Notes
Output voltage	V_{FF}	10.0	11.0	—	V		1
Input voltage	V_{ci}	—	—	3.6	V		2

Notes: 1. Measured when V_{CC} = 3.0 V, Io (load current) = 0.25 mA, C = 1 µF, f_{OSC} (oscillation frequency) = 10 kHz, and the input voltage is boosted four times.
2. Input voltage must be below V_{CC}.

AC Characteristics

Table 5 Clock Characteristics (V_{CC} = 2.2 to 3.6 V, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions	Notes
Oscillation frequency	f_{OSC}	7	10	13	kHz	C = 100 pF, R = 470 kΩ	
External clock frequency	f_{CP}	5	10	20	kHz		
External clock duty cycle	Duty	45	50	55	%		
External clock rise time	t_r	—	—	0.2	µS		
External clock fall time	t_f	—	—	0.2	µS		

Table 6 MPU Interface (V_{CC} = 2.2 to 3.6 V, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Notes
$\overline{RD}$ low-level width	t_{WRDL}	450	—	ns	
$\overline{RD}$ high-level width	t_{WRDH}	450	—	ns	
$\overline{WR}$ low-level width	t_{WWRL}	450	—	ns	
$\overline{WR}$ high-level width	t_{WWRH}	450	—	ns	
Address setup time	t_{AS}	0	—	ns	
Address hold time	t_{AH}	0	—	ns	
Data delay time	t_{DDR}	—	300	ns	
Data output hold time	t_{DHR}	10	—	ns	
Data setup time	t_{DSW}	100	—	ns	
Data hold time	t_{DHW}	0	—	ns	

Table 7 Reset Timing

Item	Symbol	Min	Max	Unit	Notes
$\overline{RES}$ low-level width	t_{RES}	1	—	ms	

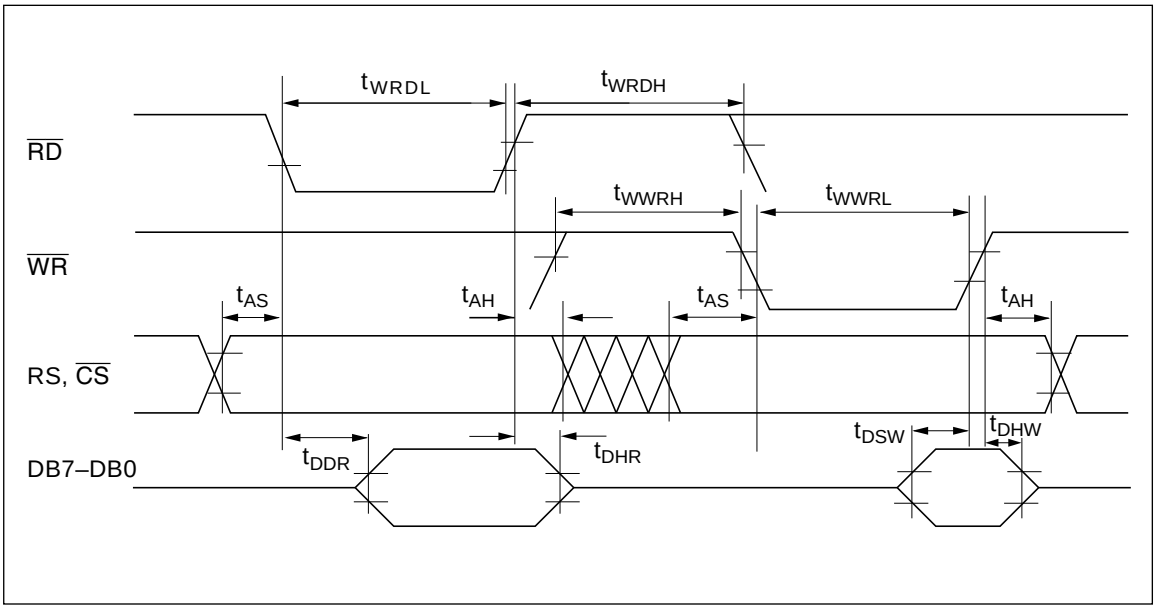


Figure 34 MPU Interface

HD66503

(240-Channel Common Driver with Internal LCD Timing Circuit)

Preliminary

HITACHI

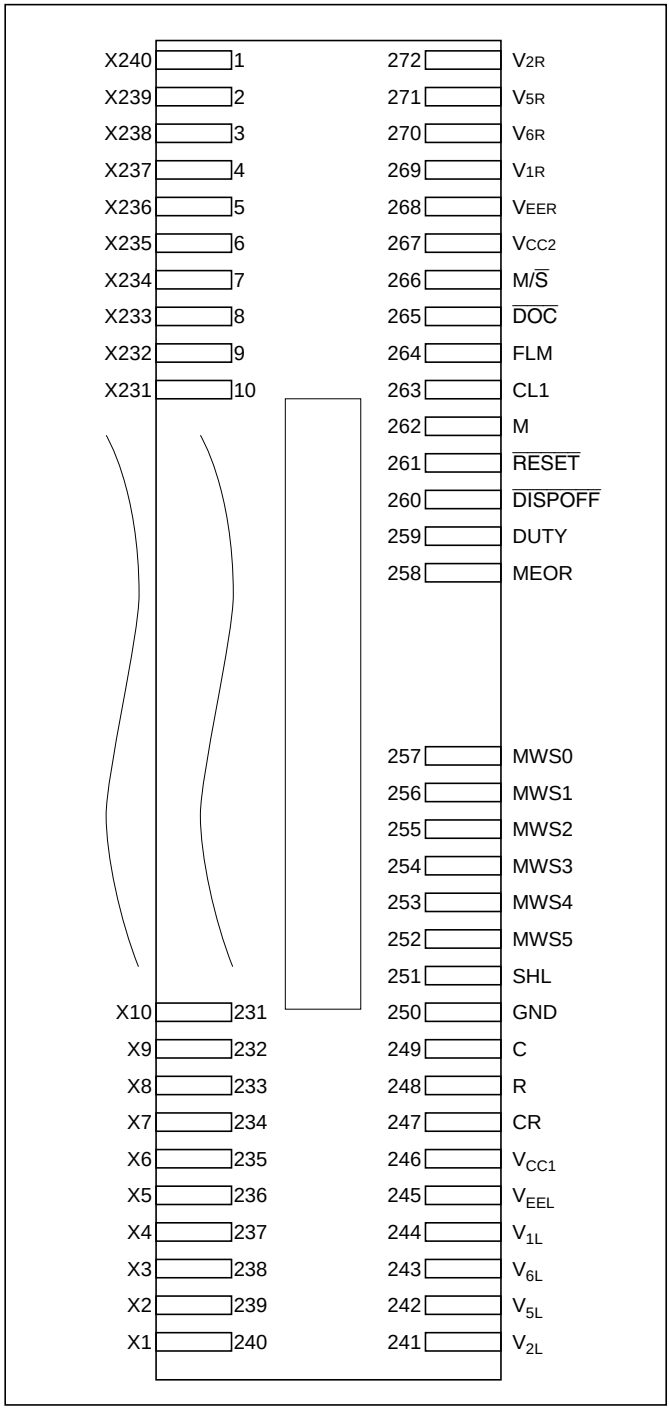
Description

The HD66503 is a common driver for liquid crystal dot-matrix graphic display systems. This device incorporates a 240 liquid crystal driver and an oscillator, and generates timing signals (alternating signals and frame synchronizing signals) required for the liquid crystal display. It also achieves low current consumption of 100 µA through the CMOS process. Combined with the HD66520, a 160-channel column driver with an internal RAM, the HD66503 is optimal for use in displays for portable information tools.

Features

- LCD timing generator: 1/120, 1/240 duty cycle internal generator
- Alternating signal waveform generator: Pin programmable 2 to 63 line inversion
- Recommended display duty cycle: 1/120, 1/240 (master mode): 1/120 to 1/240 (slave mode)
- Number of LCD driver: 240
- Power supply voltage: 2.7 to 5.5 V
- High voltage: 8 to 28-V LCD drive voltage
- Low power consumption: 100 µA (during display)
- Internal display off function
- Oscillator circuit with standby function: 130 kHz (max)
- Display timing operation clock: 65 kHz (max) (operating at 1/2 system clock)
- Package: 272-pin TCP
- CMOS process

Pin Arrangement



Pin Description

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Power supply	V_{CC1}, V_{CC2}	246 267	V_{CC}	Power supply	2	V_{CC}–GND: logic power supply
	GND	250	GND	Power supply	1	
	V_{EE}L, V_{EE}R	245 268	V_{EE}	Power supply	2	V_{CC}–V_{EE}: LCD drive circuits power supply
	V1L, R	244 269	V1	Input	2	LCD drive level power supply See figure 1.
	V2L, R	241 272	V2	Input	2	
	V5L, R	242 271	V5	Input	2	
	V6L, R	243 270	V6	Input	2	
Control signals	M/$\overline{S}$	266	Master/slave	Input	1	Controls the initiation and termination of the LCD timing generator. In addition, the input/output is determined of 4 signal pins: display data transfer clock (CL1); first line marker (FLM); alternating signal (M); and display off control ($\overline{DOC}$). See table 1 for details.
	DUTY	259	Duty	Input	1	Selects the display duty cycle. Low level: 1/120 display duty ratio High level: 1/240 display duty ratio
	MWS0 to MWS5	257 256 255 254 253 252	MWS0 MWS1 MWS2 MWS3 MWS4 MWS5	Input	6	The number of line in the line alternating waveform is set during master mode. The number of lines can be set between 10 and 63. When using the external alternating signal or during slave mode, set the number of lines to 0. See table 2.
	MEOR	258	M Exclusive-OR	Input	1	During master mode, the signals alternating waveform output from pin M is selected. During low level, the line alternating waveform is output from pin M. During high level, pin M outputs an EOR (exclusive OR) waveform between a line alternating waveform and frame alternating waveform. Set the pin to low during slave mode. See table 3.

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Control signals	CR, R, C	247 248 249	CR R C		3	These pins are used as shown in figure 4 in master mode, and as shown in figure 5 in slave mode.
	$\overline{\text{RESET}}$	261	Reset	Input	1	The following initiation will be proceeded by setting to initiation. 1) Stops the internal oscillator or the external oscillator clock input. 2) Initializes the counters of the liquid crystal display timing generator and alternating signal (M) generator. 3) Set display off control output ($\overline{\text{DOC}}$) to low and turns off display. After reset, display off control output ($\overline{\text{DOC}}$) will stay low for four more frame cycles (four clocks of FLM signals) to prevent error display at initiation. The electrical characteristics are shown in table 4. See figure 2. However, when reset is performed during operation, RAM data in the HD66520 which is used together with the HD66503 may be destroyed. Therefore, write data to the RAM again.
LCD timing	CL1	263	Clock 1	I/O	1	The bidirectional shift register shifts data at the falling edge of CL1. During master mode, this pinoutputs a data transfer clock with a two times larger cycle than the internal oscillator (or the cycle of the external clock) with a duty of 50%. During slave mode, this pin inputs the external data transfer clock.
	FLM	264	First line marker	I/O	1	During master mode, pin FLM outputs the first line marker. During slave mode, this pin inputs the external data first line marker. The shift direction of the first line marker is determined by DUTY and SHL signal as follows. Set signal DUTY to high during slave mode. See table 5.
	M	262	M	I/O	1	Pin M inputs and outputs the alternating signal of the LCD output.

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
LCD timing	SHL	251	Shift left	Input	1	Pin SHL switches the shift direction of the shift register. Refer to FLM for details.
	$\overline{\text{DISPOFF}}$	260	Display off	Input	1	Turns off the LCD. During master mode, liquid crystal drive output X1 to X240can be set to level V1 by setting the pin to low. By setting the HD66520 to level V1 in the same way, the data on the display can be erased. During slave mode, set $\overline{\text{DISPOFF}}$ high.
	$\overline{\text{DOC}}$	265	Display off control	I/O	1	Controls the display-off function. During master mode, pin $\overline{\text{DOC}}$ becomes an output pin and controls display off after reset and display off according to signal $\overline{\text{DISPOFF}}$. In this case, connect this signal to the HD66520's pin $\overline{\text{DISPOFF}}$. During slave mode, pin $\overline{\text{DOC}}$ becomes an input pin for display off control signal. In this case, connect this signal to the master HD66503's pin $\overline{\text{DOC}}$.
LCD drive output	X1 to X240	240 to 1	X1 to X240	Output	240	Selects one from among four levels (V1, V2, V5, and V6) depending on the combination of M signal and display data. See figure 3.

Note: 30 input/outputs (excluding driver block)

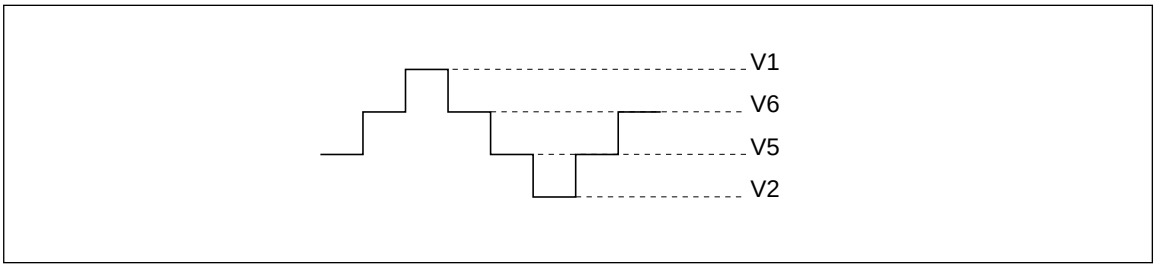


Figure 1 LCD Drive Levels

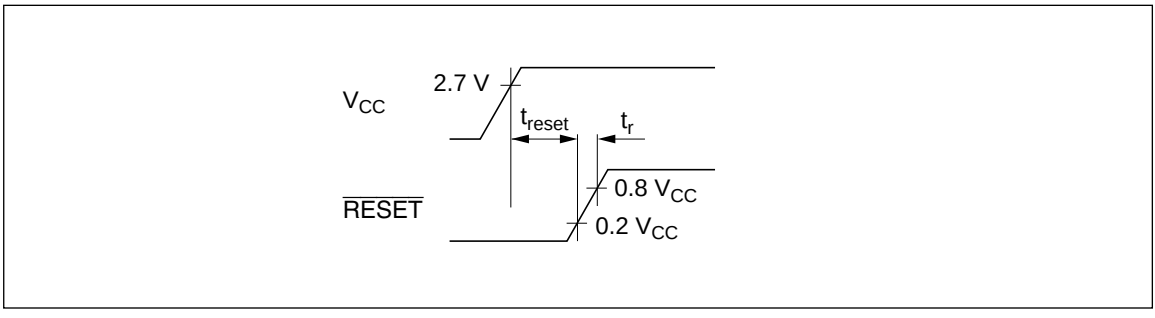


Figure 2 Reset Pin Operation

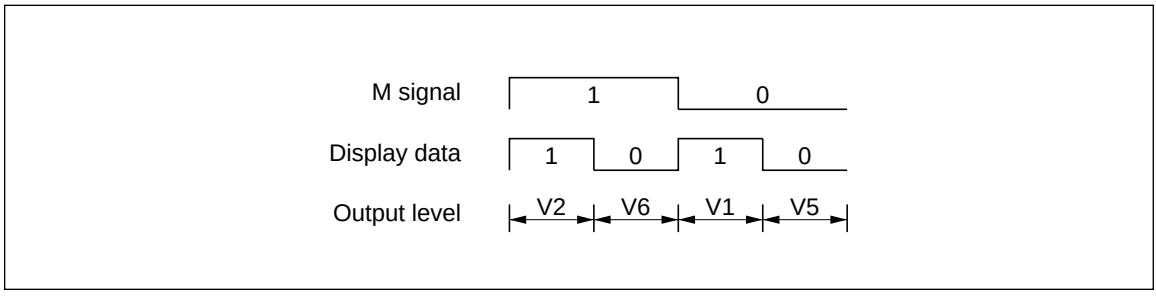


Figure 3 LCD Drive Output

Table 1 M/$\overline{S}$ Signal Status

M/$\overline{S}$	Mode	LCD Timing Generator	CL1, FLM, M, $\overline{DOC}$ Input/Output State
H	Master	1/120 or 1/240 duty cycle control	Output
L	Slave	Stop	Input

Table 2 MSW0 to MSW5 Signals Status

Number of Lines	MWS5	MWS4	MWS3	MWS2	MWS1	MWS0	Line Alternating Waveform	Pin M State
0	0	0	0	0	0	0	—	Input
1	0	0	0	0	0	1	Disable	Output
2	0	0	0	0	1	0	2-line alternation	
3 to 63	0 to 1	0 to 1	0 to 1	0 to 1	1 to 1	1 to 1	3-line alternation to 63-line alternation	

Table 3 MEOR Signal Status

Mode	MEOR	Types of Alternating Waveforms Output by Pin M
Master	H	Line alternating waveform ⊕ frame alternating waveform
	L	Line alternating waveform
Slave	L	—

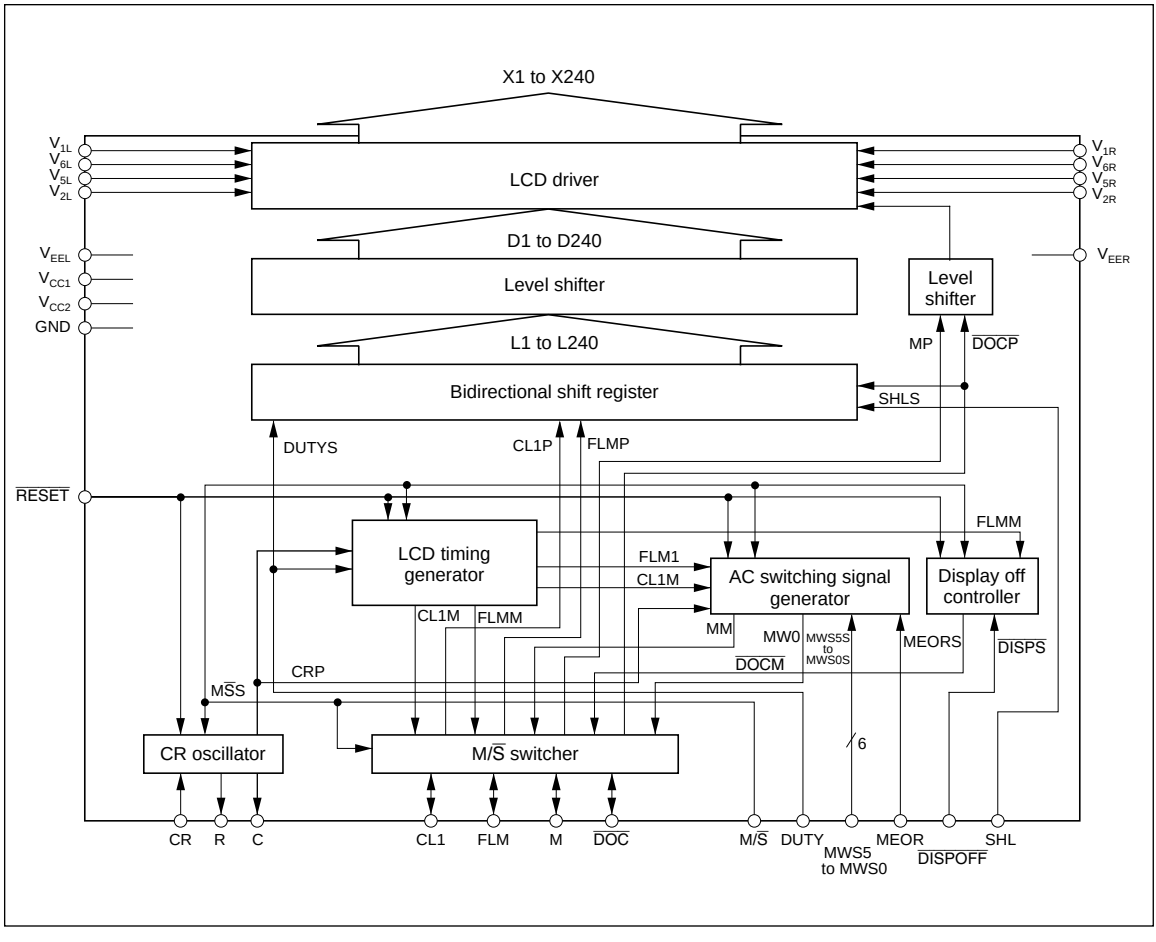
Table 4 Power Supply Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{reset}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Table 5 FLM Status Control

Mode	DUTY	SHL	Shift Direction of First Line Marker
Master	H	H	X240 → X1
		L	X1 → X240
	L	H	X120 → X1, X240 → X121
		L	X1 → X120, X121 → X240
Slave	H	H	X240 → X1
		L	X1 → X240

Internal Block Diagram



1. CR Oscillator: The CR oscillator generates the HD66503 operation clock. During master mode, since the operation clock is needed, connect oscillation resistor Rf with oscillation capacitor Cf as follows. When the external clock is used, input external clock to pin CR and open pins C and R (figure 4).

When using the HD66503 during slave mode, the operation clock will not be needed; therefore, connect pin CR to V_{CC} and open pins C and R (figure 5).

2. Liquid Crystal Timing Generator: The liquid crystal timing generator creates various signals for the LCD. During master mode (M/$\overline{S}$ = V_{CC}), the generator operates the HD66503's internal circuitry as a common internal driver using the generated LCD signals. In addition, signals CL1, M, and $\overline{DOC}$ created by this generator can synchronously display data on a liquid crystal display by inputting them into the RAM-provided segment driver HD66520 used together with HD66503. During slave mode (M/$\overline{S}$ = GND), this generator stops; the slave HD66503 operates based on signals CL1, M, $\overline{DOC}$, and FLM generated by the master HD66503.

3. M/$\overline{S}$ Switcher: Controls the input and output of LCD signals CL1, FLM, M, and $\overline{DOC}$.

This circuit outputs data when M/$\overline{S}$ = V_{CC} (master mode) and inputs data when M/$\overline{S}$ = GND (slave mode).

4. Alternating Signal Generator: Generates the alternating signal for the liquid crystal display. Since the alternating signal decreases cross talk, it can alternate among 2 to 63 lines. The number of lines are specified with pins MWS0 to MWS5 is set to either V_{CC} or GND.

Moreover, the alternating signal can be externally input by grounding pins MWS0 to MWS5. In this case, the alternating signal is input from pin M.

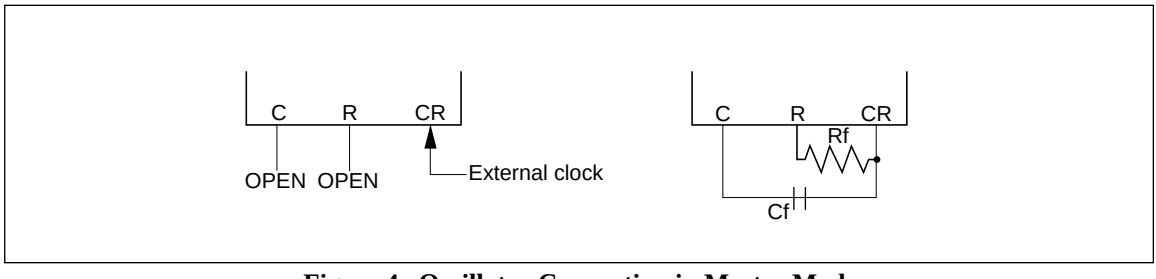


Figure 4 Oscillator Connection in Master Mode

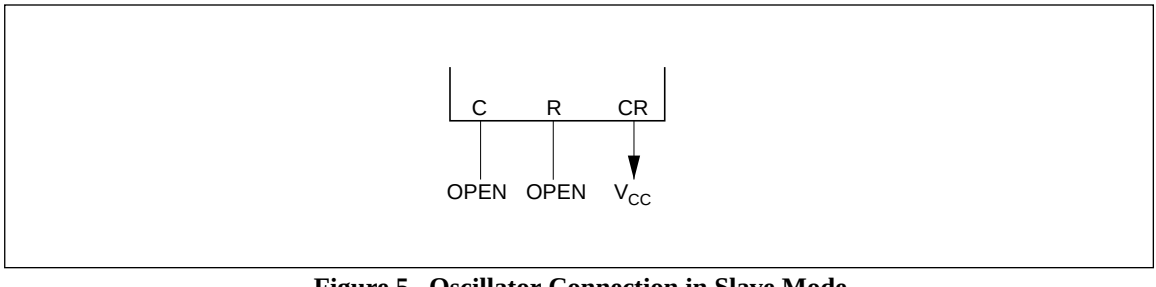


Figure 5 Oscillator Connection in Slave Mode

5. Display Off Control Circuit: Controls display-off function by using external display off signal $\overline{\text{DISPS}}$ and automatic display off signal FLMM generated by the liquid crystal timing generator. Automatic display off signal FLMM is an internal signal that is used to turn off the display in four frames after signal reset is released. As a result, it is possible to turn off display using the display off signal that is sent randomly from an external LSI and automatically prevent incorrect display after reset release.

6. Bidirectional Shift Register: This is a 240-bit bidirectional shift register. This register can change the shift direction using signal SHL. During master mode, the scan signal of the common driver can be generated by sequentially shifting first line marker signal FLM generated internally. During slave mode, a scan signal is generated by sequentially shifting first line marker signal FLM input from pin FLM.

7. Level Shifter: Boosts the logic signal to a high voltage signal for the LCD.

8. LCD Drive Circuit: One of the LCD levels V1, V2, V5, and V6 are selected and output via pin X according to the combination of the data in the bidirectional shift register and signal M.

Table 6 Output Level of LCD Circuit

Data in the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

Internal Function Description

1. Generation of Signals CL1 and FLM: Signal CL1 shifts the scanning signal of the common driver. It is a 50% duty-ratio clock that changes level synchronously with the rising edge of oscillator clock CR.

FLM is a clock signal that is output once every 240 CL1 clock cycles for a duty of 1/240 (DUTY = V_{CC}), and every 120 CL1 clock cycles for a duty of 1/120 (DUTY = GND).

2. Generation of Signal M: Signal M alternates current in the LCD. It alternates the current to decrease cross talk after a certain number of lines ranging from 2 to 63 lines. The number of lines can be specified with pins MWS0 to MWS5 by setting each pin to either V_{CC} or GND (H or L). In addition, when pin MEOR is connected to GND, signal M is a simple line alternating waveform, and when pin MEOR is connected to V_{CC}, signal M is an EOR (exclusive OR) of line alternating waveform and frame alternating waveform.

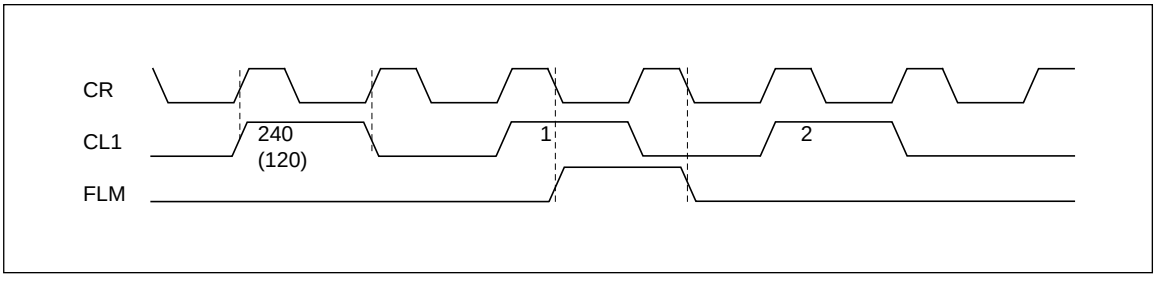


Figure 6 Generation of Signals CL1 and FLM

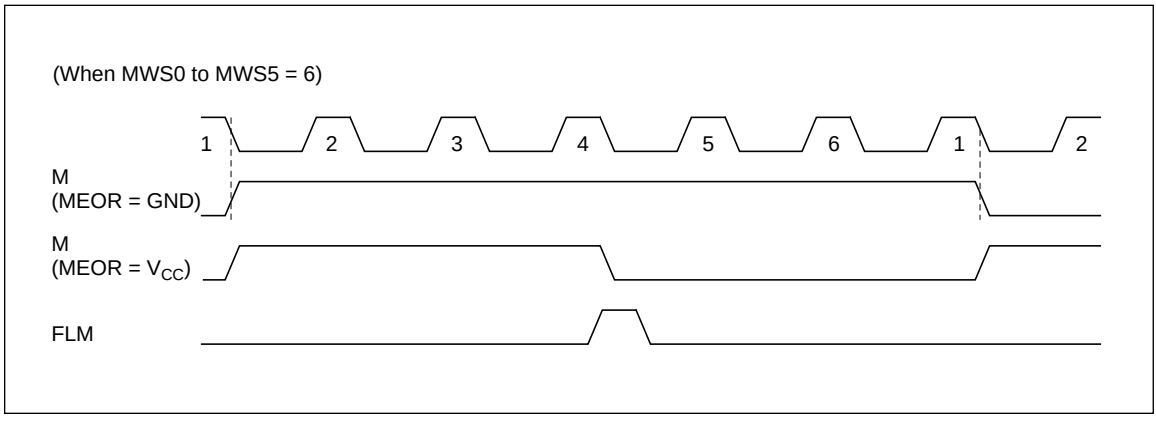
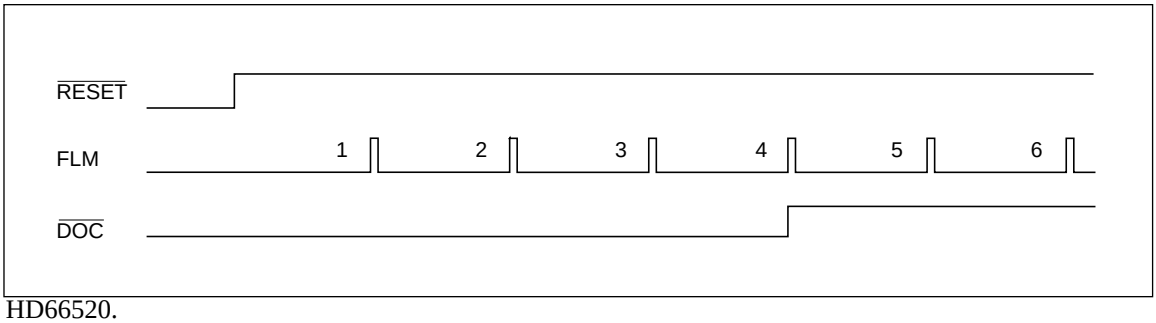


Figure 7 Generation of Signal M

3. Auto Display-Off Control: This functions prevents incorrect display after reset release. The display is turned off four frames following after reset release. In addition, the display off control signal shown in fig.8 is output by pin $\overline{DOC}$. This pin is connected to pin $\overline{DISPOFF}$ of the



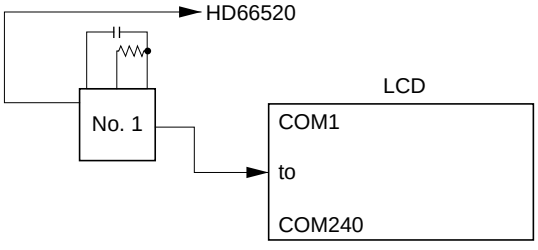
HD66520.

Figure 8 Automatic Display-Off Control Function

Application Example

Outline of HD66503 System Configuration

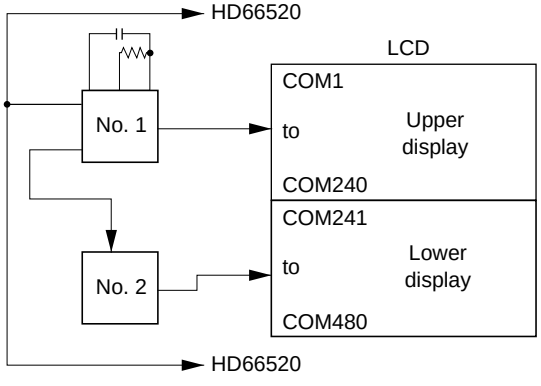
The HD66503 system configuration is outlined in figs. 9 and 10. Refer to the connection list (table 7) for connection details.



	No. 1
When using the internal oscillator	Refer to connection list A
When using an external clock	Refer to connection list D

Note: One HD66503 drives common signals and supplies timing signal to the HD66520.

- When a single HD66503 is used to configure a small display (figure 9)



	No. 1	No. 2
When using the internal oscillator	Refer to connection list B	Refer to connection list C
When using an external clock	Refer to connection list E	Refer to connection list C

Note: Upper and lower displaya are driven by separate HD66503s to ensure display quality. No. 1 operates in master mode, and No. 2 operates in slave mode.

- When two HD66503s are used to configure a large display (figure 10)

Figure 10 When Using Two HD66503s

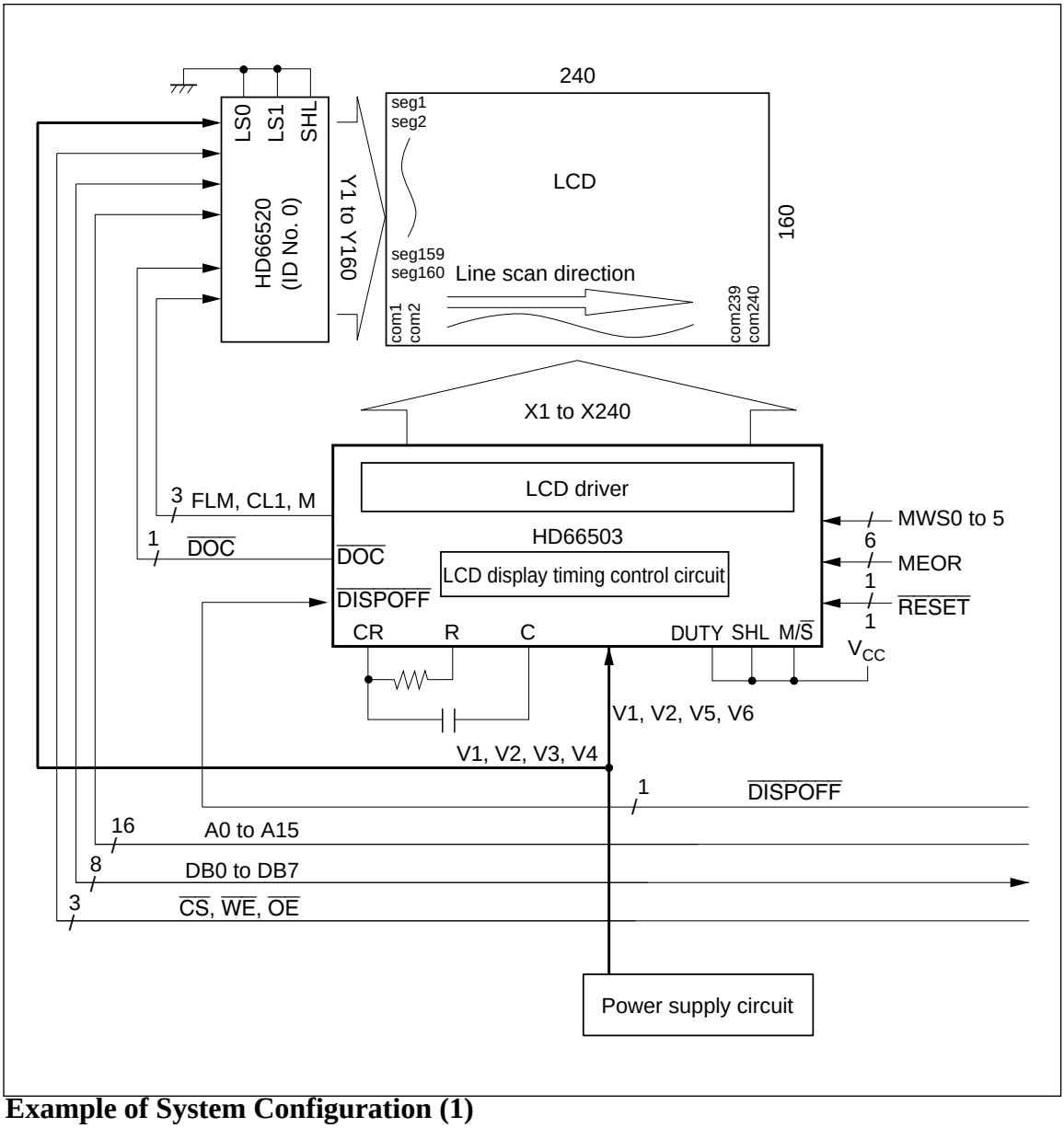
HD66503 Connection List

Table 9 HD66503 Connection List

Connection Example	M/$\overline{S}$	DUTY	MWS0, MWS1, MWS2, MWS3, MWS4, MWS5	MEOR	$\overline{RESET}$	$\overline{DISPOFF}$	CR	R	C	CL1	FLM	M	$\overline{DOC}$	SHL	X1 to X240
A	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	Rf	Rf		To CL1 of HD66520	To FLM of HD66520	To M of HD66520	To $\overline{DISPOFF}$ of HD66520	H	COM1 to COM240
							Cf		Cf					L	COM240 to COM1
B	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	Rf	Rf		To CL1 of HD66520 HD66503	To FLM of HD66520 HD66503	To M of HD66520 HD66503	To $\overline{DOC}$ of HD66503	H	COM1 to COM240
							Cf		Cf				T0 $\overline{DISPOFF}$ of HD66520	L	COM240 to COM1
C	L	H	Set the number of lines for alternating the current	L	From CPU of external reset circuit	H	H	—	—	From CL1 of HD66503	From FLM of HD66503	From M of HD66503	From $\overline{DOC}$ of HD66503	H	COM241 to COM480
														L	COM480 to COM241
D	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	From external oscillator	—	—	To CL1 of HD66520	To FLM of HD66520	To M of HD66520	To $\overline{DISPOFF}$ of HD66520	H	COM1 to COM240
														L	COM240 to COM1
E	H	H	Set the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	From external oscillator	—	—	To CL1 of HD66520 HD66503	To FLM of HD66520 HD66503	To M of HD66520 HD66503	To $\overline{DOC}$ of HD66503	H	COM1 to COM240
													To $\overline{DISPOFF}$ of HD66520	L	COM240 to COM1

Notes: H = V_{CC} (Fixed)
L = GND (Fixed)
"—" means "open"

Rf: Oscillation resistor
Cf: Oscillation capacitor



Example of System Configuration (1)

Figure 11 shows a system configuration for a 240 × 160-dot LCD panel using segment driver HD66520 with internal bit-map RAM. All required functions can be prepared for liquid crystal display with just two chips except for liquid crystal display power supply circuit functions. Refer to Timing

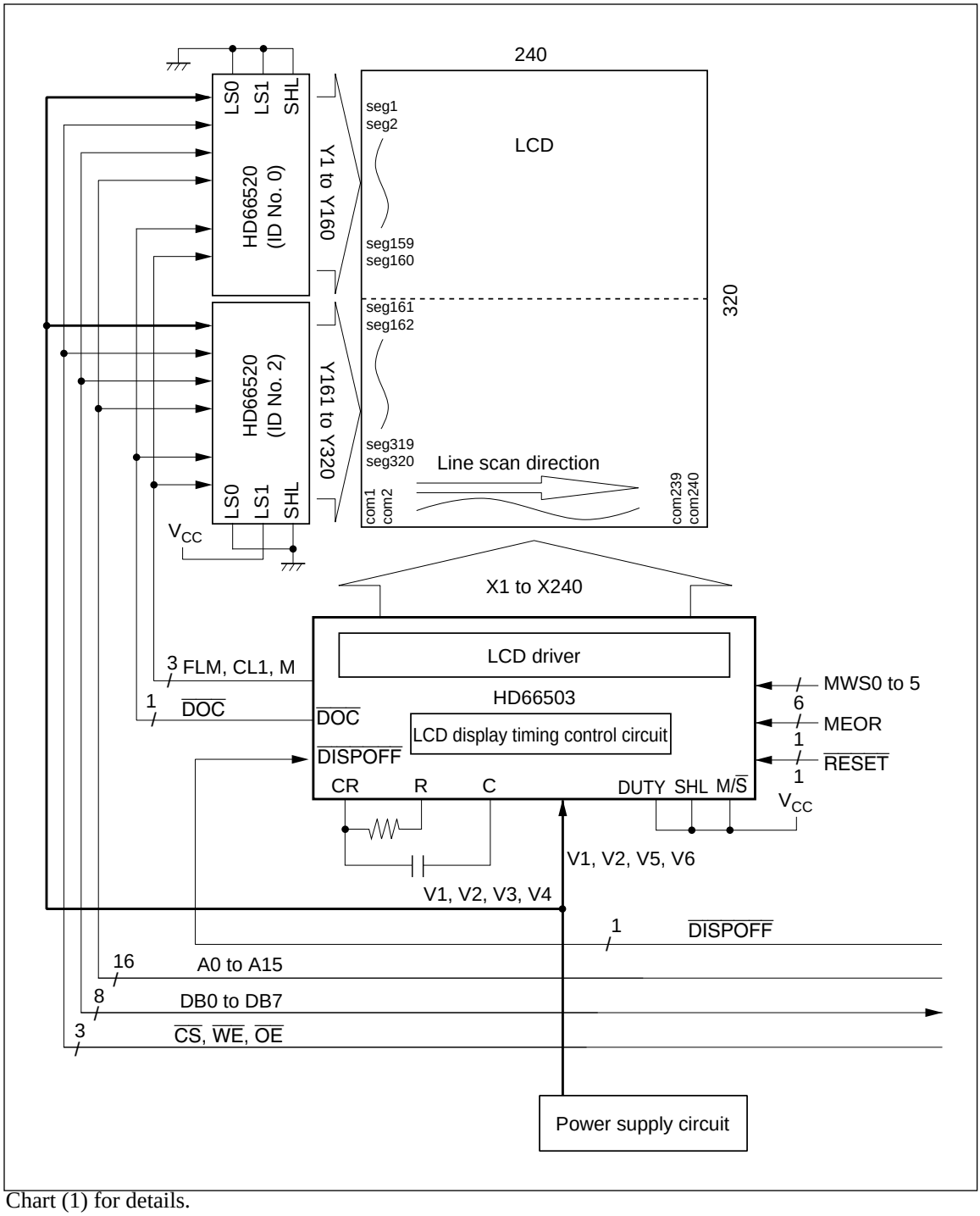
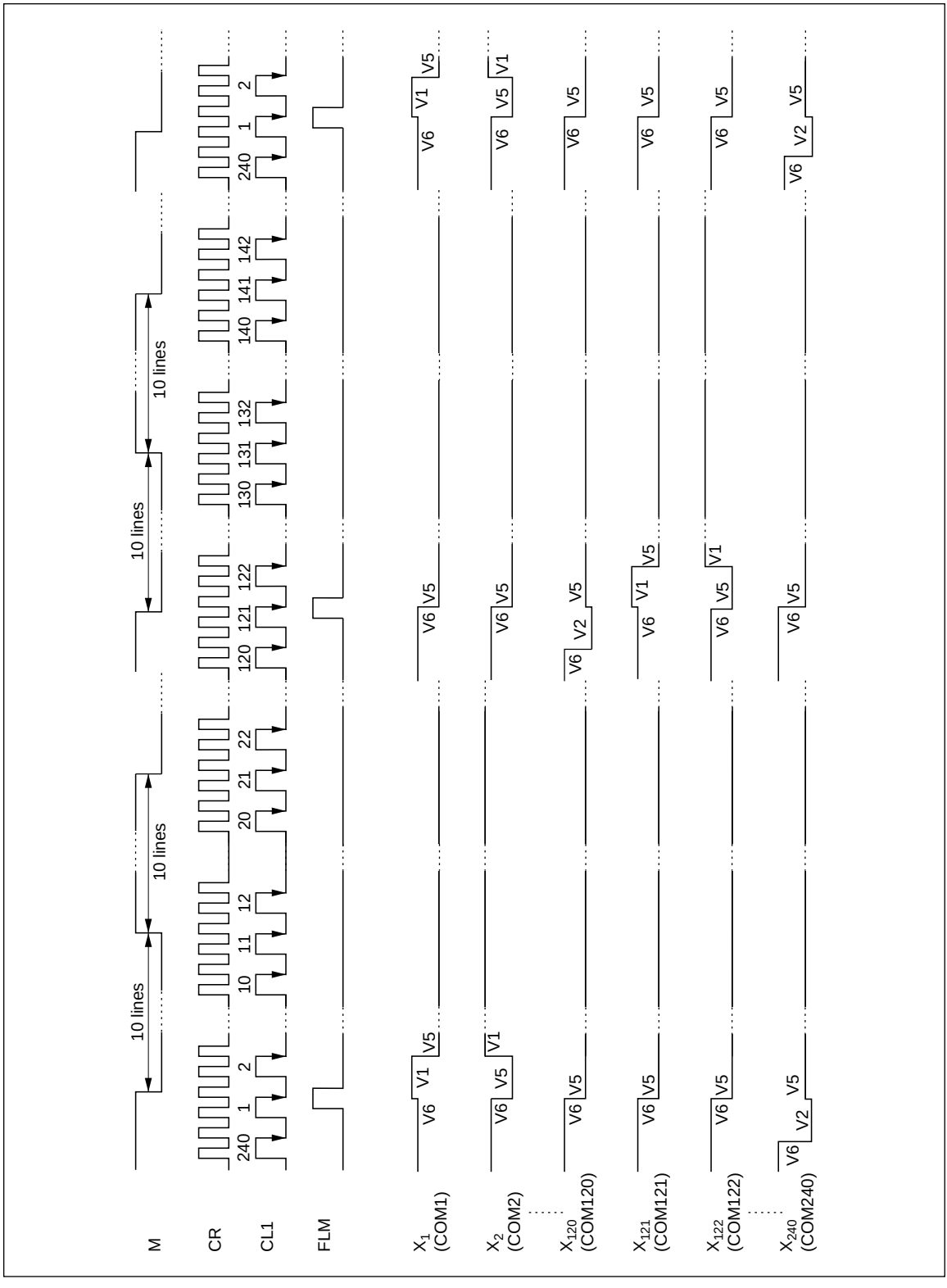


Chart (1) for details.

Figure 11 System Configuration (1)



Example of System Configuration (2)

Figure 12 shows a system configuration for a 240 × 320-dot LCD panel using segment driver HD66520 with internal bit-map RAM. Refer to Timing Chart (1) for details.

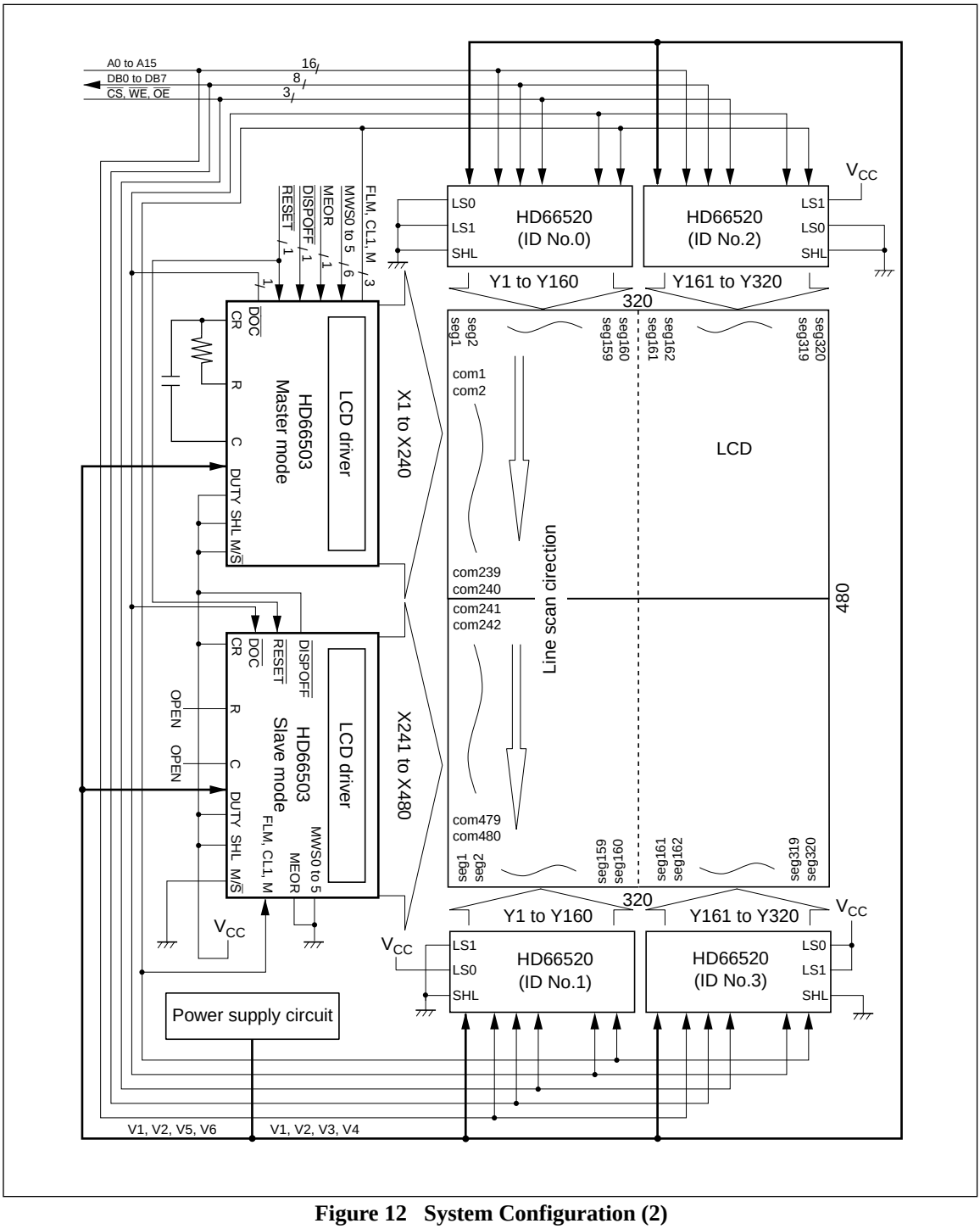


Figure 12 System Configuration (2)

Timing Chart (1)

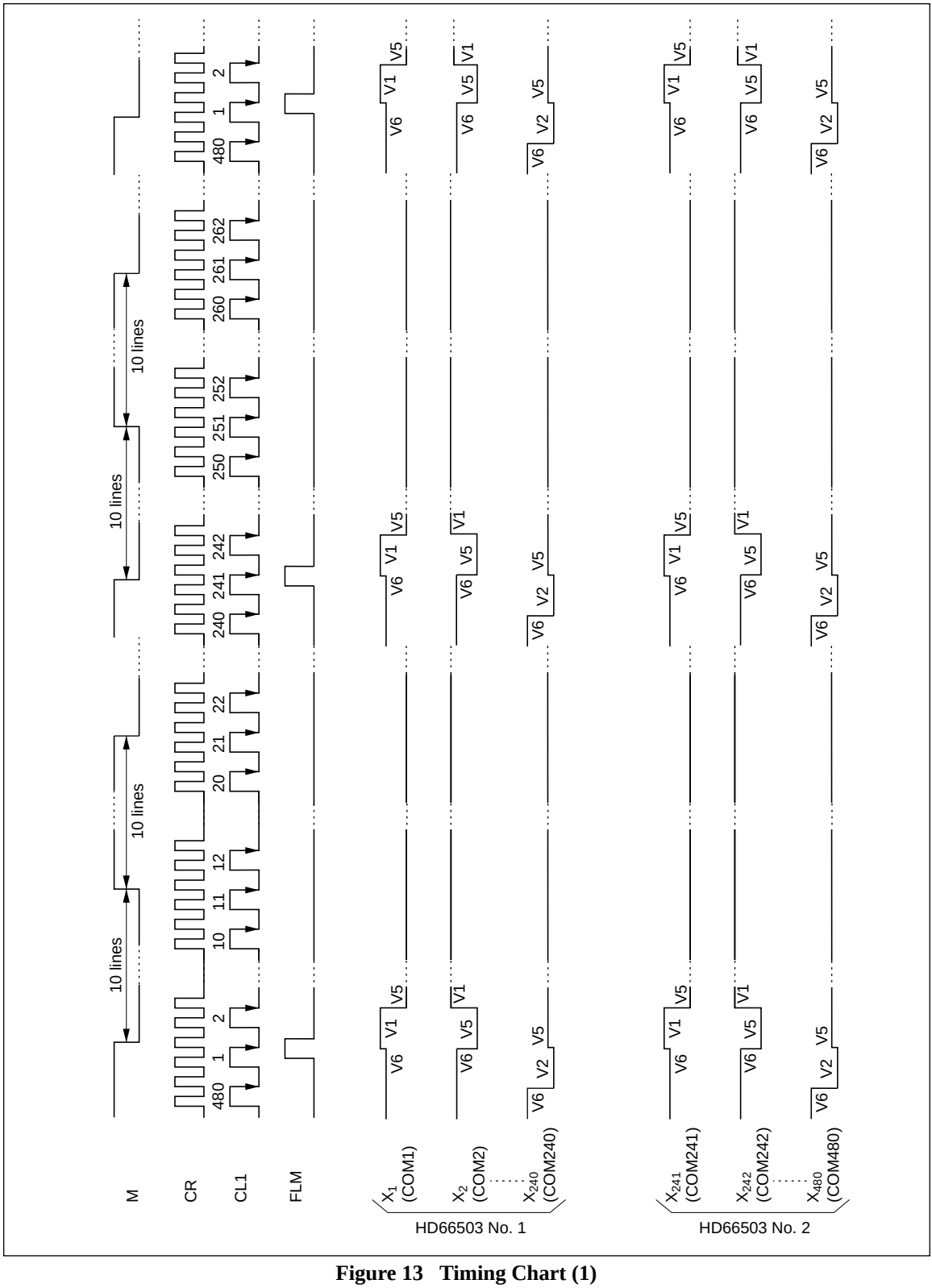
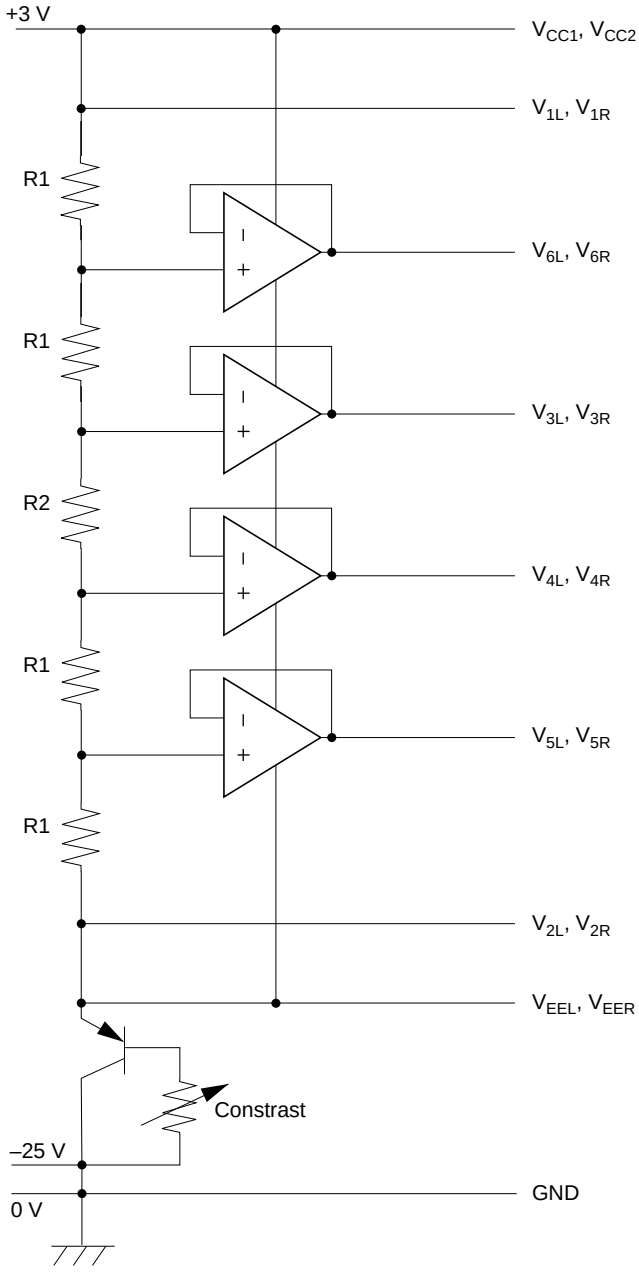


Figure 13 Timing Chart (1)

Example of System Configuration (3)



Note: The values of R1 and R2 vary with the LCD panel used. When the bias factor is 1/15, for example, the values of R1 and R2 can be determined as follows:

$$\frac{R1}{4R1 + R2} = \frac{1}{15}$$

If R1 = 3 kΩ, then R2 = 33 kΩ

Figure 14 shows a system configuration for a 320 × 480-dot LCD panel using segment driver HD66520

with internal bit-map RAM. Refer to Timing Chart (2) for details.

Figure 14 System Configuration (3)

Timing Chart (2)

Figure 15 Timing Chart (2)

Power Supply Circuit

Figure 16 Power Supply Circuit

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	2
	LCD drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	5
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Input voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes:
1. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.
2. Measured relative to GND (0 V).
3. Applies to all input pins except for V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{6L}, and V_{6R}, and to input/output pins in high-impedance state.
4. Applies to pins V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{6L}, and V_{6R}.
5. Apply the same voltage to pairs V_{1L} and V_{1R}, V_{2L} and V_{2R}, V_{5L} and V_{5R}, V_{6L} and V_{6R}, and V_{EEL} and V_{EER}.
   It is important to preserve the relationships $V_{CC1} = V_{CC2} \geq V_{1L} = V_{1R} \geq V_{6L} = V_{6R} \geq V_{5L} = V_{5R} \geq V_{2L} = V_{2R} \geq V_{EEL} = V_{EER}$

Electrical Characteristics

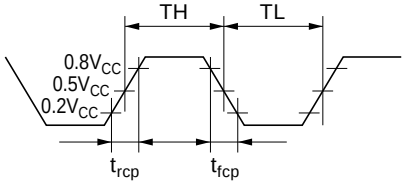
DC Characteristics (V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 8 to 28 V, GND = 0 V, Ta = –20 to +75°C)

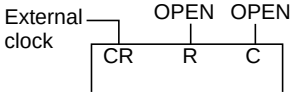
Item	Symbol	Min	Typ	Max	Unit	Measurement Condition	Notes
Input high level voltage	V_{IH}	0.8 V_{CC}	—	V_{CC}	V		1
Input low level voltage	V_{IL}	0	—	0.2 V_{CC}	V		1
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low level voltage	V_{OL}	—	—	0.4	V	I_{OL} = +0.4 mA	2
Driver “on” resistance	R_{ON}	—	—	2.0	kΩ	$V_{CC} - V_{EE}$ = 28 V, load current: ±150 µA	13, 14
Input leakage current (1)	I_{IL1}	–1.0	—	1.0	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current (2)	I_{IL2}	–25	—	25	µA	V_{IN} = V_{EE} to V_{CC}	3
Operating frequency (1)	f_{opr1}	10	—	200	kHz	Master mode (external clock operation)	4
Operating frequency (2)	f_{opr2}	5	—	500	kHz	Slave mode	5
Oscillation frequency (1)	f_{OSC1}	70	100	130	kHz	Cf = 100 pF ±5%, Rf = 51 kΩ ±2%	6, 12
Oscillation frequency (2)	f_{OSC2}	21	30	39	kHz	Cf = 100 pF ±5%, Rf = 180 kΩ ±2%	6, 12
Power consumption (1)	I_{GND1}	—	—	80	µA	Master mode 1/240 duty cycle, Cf = 100 pF, Rf = 180 kΩ V_{CC} – GND = 3 V, $V_{CC} - V_{EE}$ = 28 V	7, 8
Power consumption (2)	I_{GND2}	—	—	20	µA	Master mode 1/240 duty cycle external clock f_{opr1} = 30 kHz V_{CC} – GND = 3 V, $V_{CC} - V_{EE}$ = 28 V	7, 9
Power consumption (3)	I_{GND3}	—	—	10	µA	Slave mode 1/240 duty cycle during operation f_{CL} = 15 kHz V_{CC} – GND = 3 V, $V_{CC} - V_{EE}$ = 28 V	7, 10

Item	Symbol	Min	Typ	Max	Unit	Measurement Condition	Notes
Power consumption	I_{EE}	—	—	20	µA	Master mode 1/240 duty cycle, Cf = 100 pF, Rf = 180 kΩ V_{CC} – GND = 3 V V_{CC} – V_{EE} = 28 V,	7, 11

Notes: 1. Applies to input pins MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISPOFF}}$, M/$\overline{\text{S}}$, $\overline{\text{RESET}}$, and CR, and when inputting to input/output pins CL1, FLM, $\overline{\text{DOC}}$, and M.

2. Applies when outputting from input/output pins CL1, FLM, $\overline{\text{DOC}}$, and M.
3. Applies to V1L/R, V2L/R, V5L/R, and V6L/R. X1 to X240 are open.
4. Figure 17 shows the external clock specifications:





$$\text{Duty} = \frac{TH}{TH + TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty	45	50	55	%
t_{rcp}	—	—	50	ns
t_{fcp}	—	—	50	ns

Figure 17 External Clock

5. Regulates to operation frequency limits of the bidirectional shift register in the slavemode.
6. Connect resistance Rf and capacitance Cf as follows:

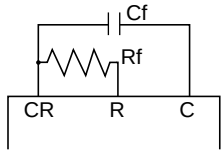


Figure 18 Timing Components

7. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
8. This value is specified for the current flowing through GND under the following conditions: Internal oscillation circuit is used. Each terminal of MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISPOFF}}$, M/$\overline{\text{S}}$, and $\overline{\text{RESET}}$ is connected to V_{CC}. Oscillator is set as described in note 6.
9. This value is specified for the current flowing through GND under the following conditions: Each terminal of MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISPOFF}}$, M/$\overline{\text{S}}$, and $\overline{\text{RESET}}$ is connected to V_{CC}. Oscillator is set as described in note 4.

10. This value is specified for the current flowing through GND under the following conditions: Each terminal of MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{DOC}$, $\overline{DISPOFF}$, $\overline{RESET}$, and CR is connected to V_{CC}, M/$\overline{S}$ to GND, and frequency of CL1, FLM, M is respectively established as follows.

    f_{CL1} = 15 kHz, f_{FLM} = 62.5 Hz, f_M = 120 Hz

11. This value is specified for the current flowing through V_{EE} under the following condition described in note 8. Do not connect any lines to pin X.
12. Figure 18 shows a typical relation among ocsillation frequency Rf and Cf. Oscillation frequency may vary with mounting conditions.

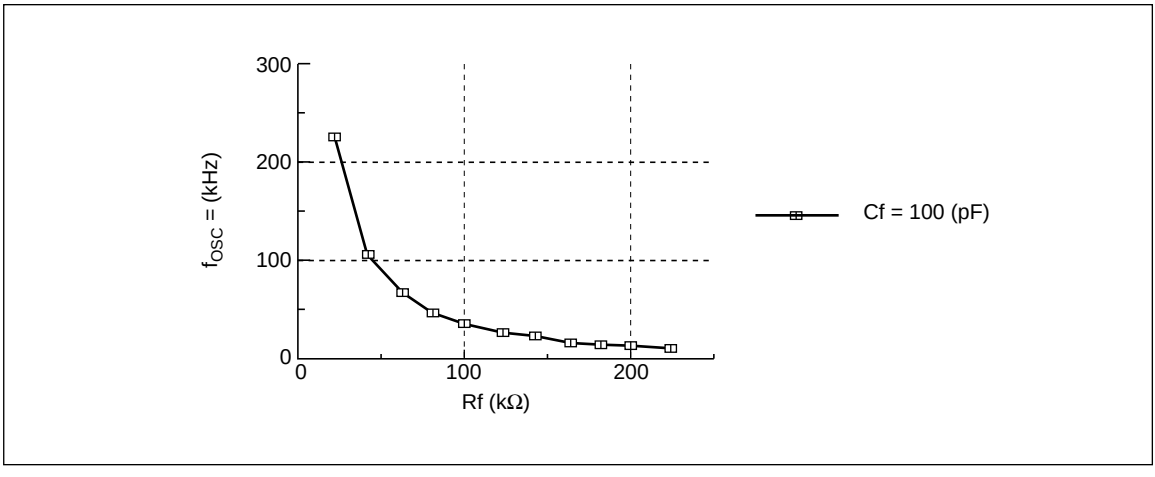


Figure 19 Ocsillation Frequency Characteristics

13. Indicates the resistance between one pin from X1 to X240 and another pin from the V pins V1L/R, V2L/R, V5L/R, and V6L/R, when a load current is applied to the X pin; defined under the following conditions:

    $V_{CC} - V_{EE}$ = 28 (V)
    V1L/R, V6L/R = V_{CC} – 1/10 ($V_{CC} - V_{EE}$)
    V5L/R, V2L/R = V_{EE} + 1/10 ($V_{CC} - V_{EE}$)

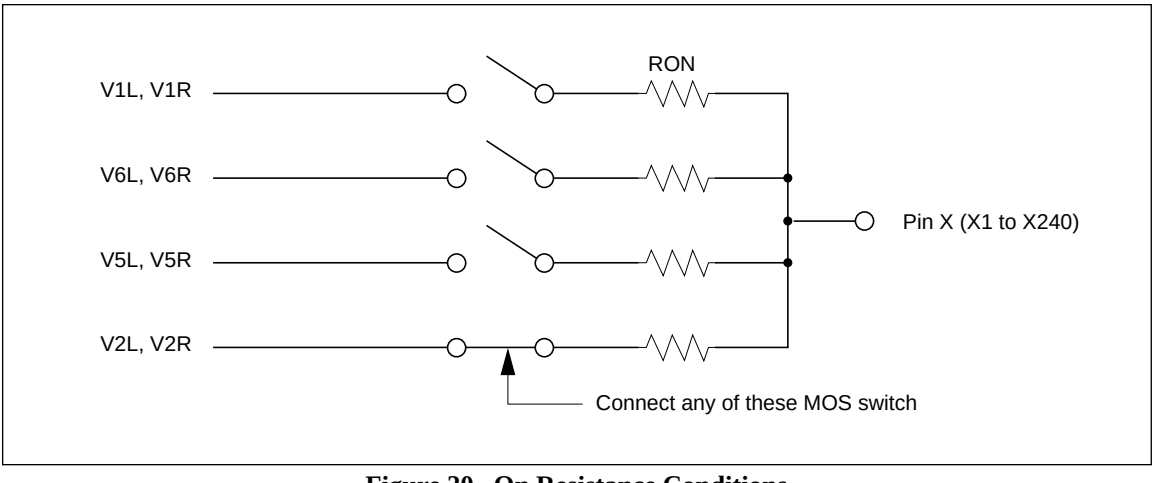


Figure 20 On Resistance Conditions

14. V1L/R and V6L/R should be near the V_{CC} level, and V5L/R and V2L/R should be near the V_{EE} level. All these voltage pairs should be separated by less than ΔV, which is the range within which R_{ON}, the LCD drive circuits' output impedance is stable. Note that ΔV depend on power supply voltages $V_{CC} - V_{EE}$. See figure 21.

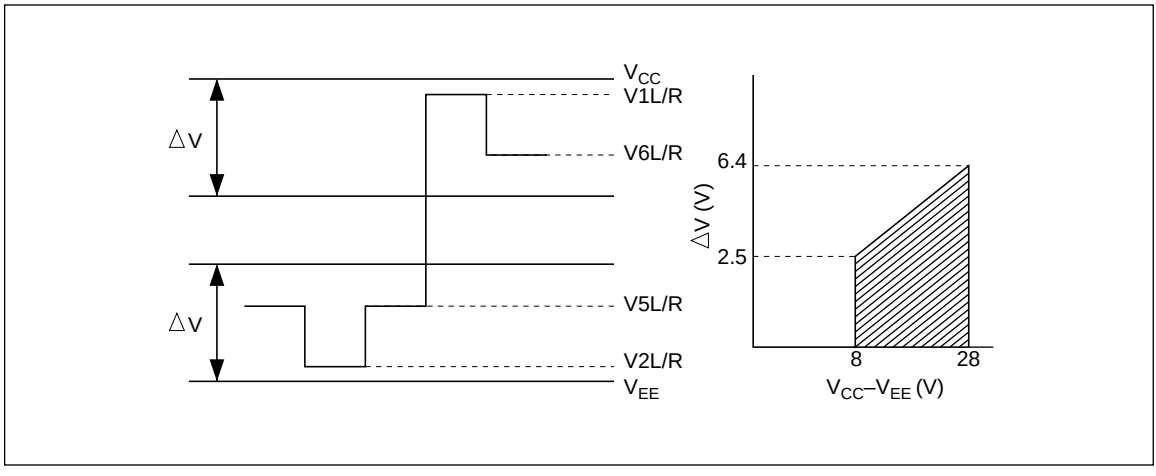


Figure 21 Relationship between Driver Output Waveform

AC Characteristics (V_{CC} = 2.7 to 5.5 V, $V_{CC} - V_{EE}$ = 8 to 28 V, GND = 0 V, Ta = –20 to +75°C)

Slave Mode (M/$\overline{S}$ = GND)

Item	Symbol	Min	Typ	Max	Unit	Notes
CL1 high-level width	t_{CWH}	500	—	—	ns	1
CL1 low-level width	t_{CWL}	500	—	—	ns	1
FLM setup time	t_{FS}	100	—	—	ns	1
FLM hold time	t_{FH}	100	—	—	ns	1
CL1 rise time	t_r	—	—	50	ns	1
CL1 fall time	t_f	—	—	50	ns	1

Note: 1. Based on the load circuit shown in figure 22.

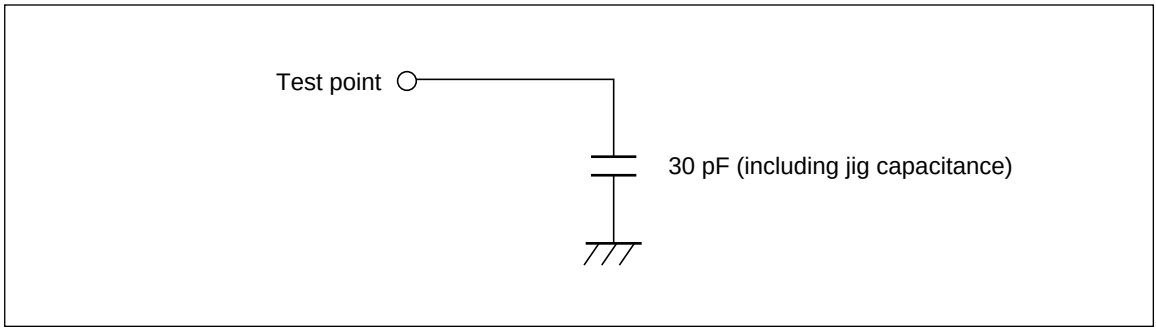


Figure 22 Load Circuit

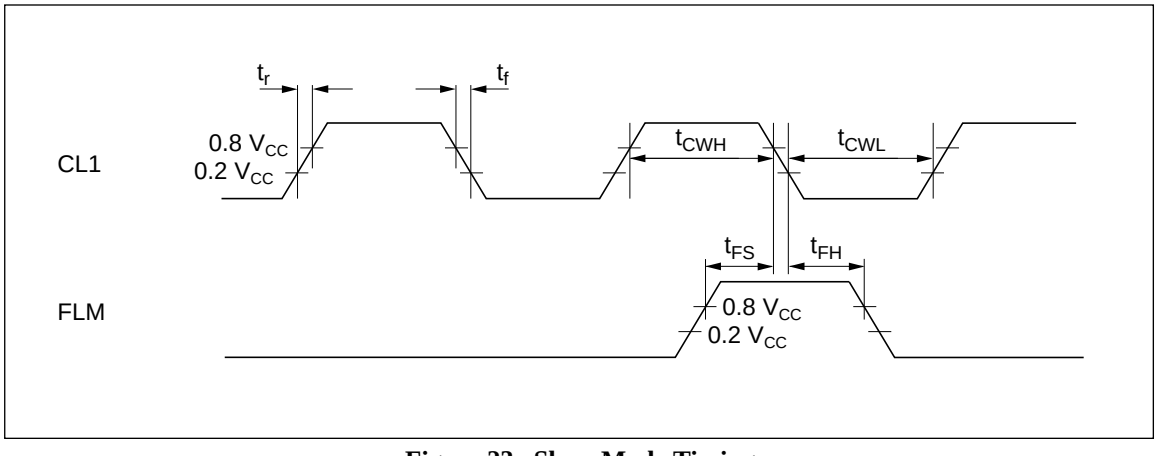


Figure 23 Slave Mode Timing

Master Mode ($M/\overline{S} = V_{CC}$)

Item	Symbol	Min	Typ	Max	Unit	Notes
CL1 delay time	t_{DCL1}	—	—	1	µs	
FLM delay time	t_{DFLM}	—	—	1	µs	
M delay time	t_{DM}	—	—	500	ns	
FLM setup time	t_{FS}	t_{osc}/ 2 – 500	—	—	ns	

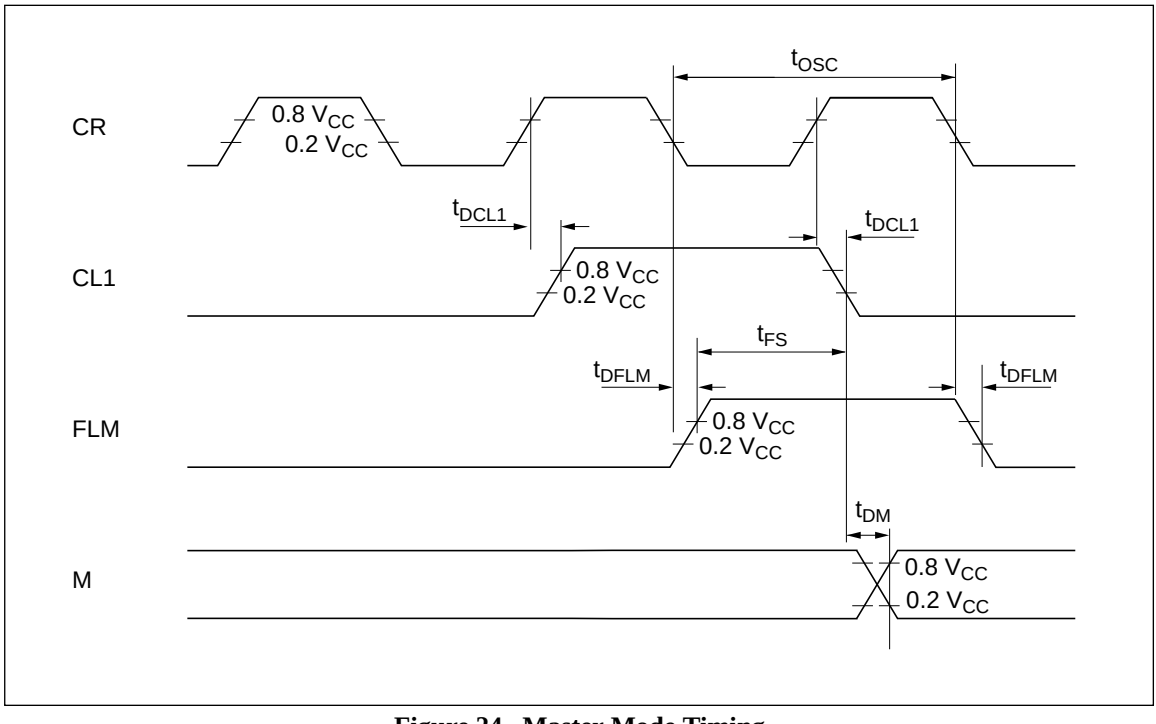


Figure 24 Master Mode Timing

HD66108

(RAM-Provided 165-Channel LCD Driver for Liquid Crystal Dot Matrix Graphics)

HITACHI

Description

The HD66108T under control of an 8-bit MPU can drive a dot matrix graphic LCD (liquid-crystal display) employing bit-mapped display with support of an 8-bit MPU.

Use of the HD66108T enables a simple LCD system to be configured with only a small number of chips, since it has all the functions required for driving the display.

The HD66108T also enables highly-flexible display selection due to the bit-mapped method, in which one bit of data in a display RAM turns one dot of an LCD panel on or off. A single HD66108T can display a maximum of 100 × 65 dots by using its on-chip 165 × 65-bit RAM. Also, by using several HD66108T's, a display can be further expanded.

The HD66108T employs the CMOS process and TCP package. Thus, if used together with an MPU, it can provide the means for a battery-driven pocket-size graphic display device utilizing the low current consumption of LCDs.

Features

- Four types of LCD driving circuit configurations can be selected:

Configuration Type	No. of Column Outputs	No. of Row Outputs
Column outputs only	165	0
Row outputs from the left and right sides	100	65 (from left: 32, from right: 33)
Row outputs from the right side 1	100	65
Row outputs from the right side 2	132	33

- Seven types of multiplexing duty ratios can be selected: 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, 1/66
  Notes: The maximum number of row outputs is 65.
- Built-in bit-mapped display RAM: 10 kbits (165 × 65 bits)
- The word length of display data can be selected according to the character font: 8-bit or 6-bit
- A standby operation is available
- The display can be extended through a multi-chip operation
- A built-in CR oscillator
- An 80-system CPU interface: ø = 4 MHz
- Power supply voltage for operation: 2.7 V to 6.0 V
- LCD driving voltage: 6.0 V to 15.0 V
- Low current consumption: 400 µA max (at f_{OSC} = 500 kHz, f_{OSC} is external clock frequency)

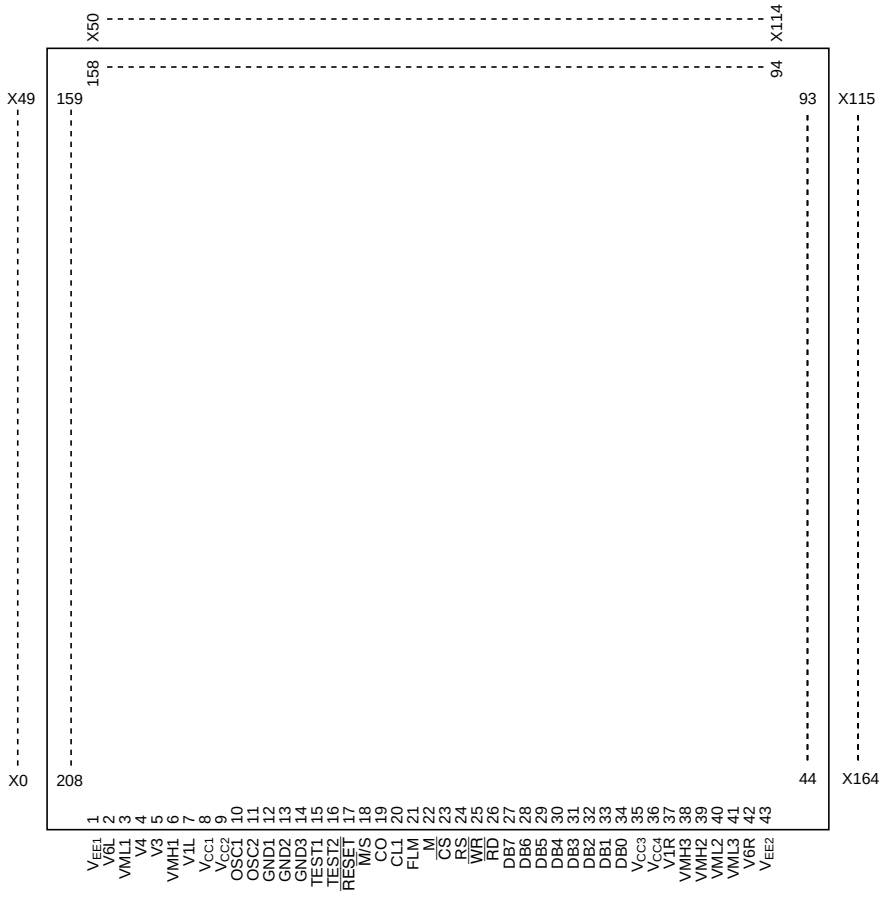
Ordering Information

Type No.	Package
HD66108T00	208 pin TCP

Note: The details of TCP pattern are shown in "The Information of TCP."

Hitachi semiconductor

Chip Terminals



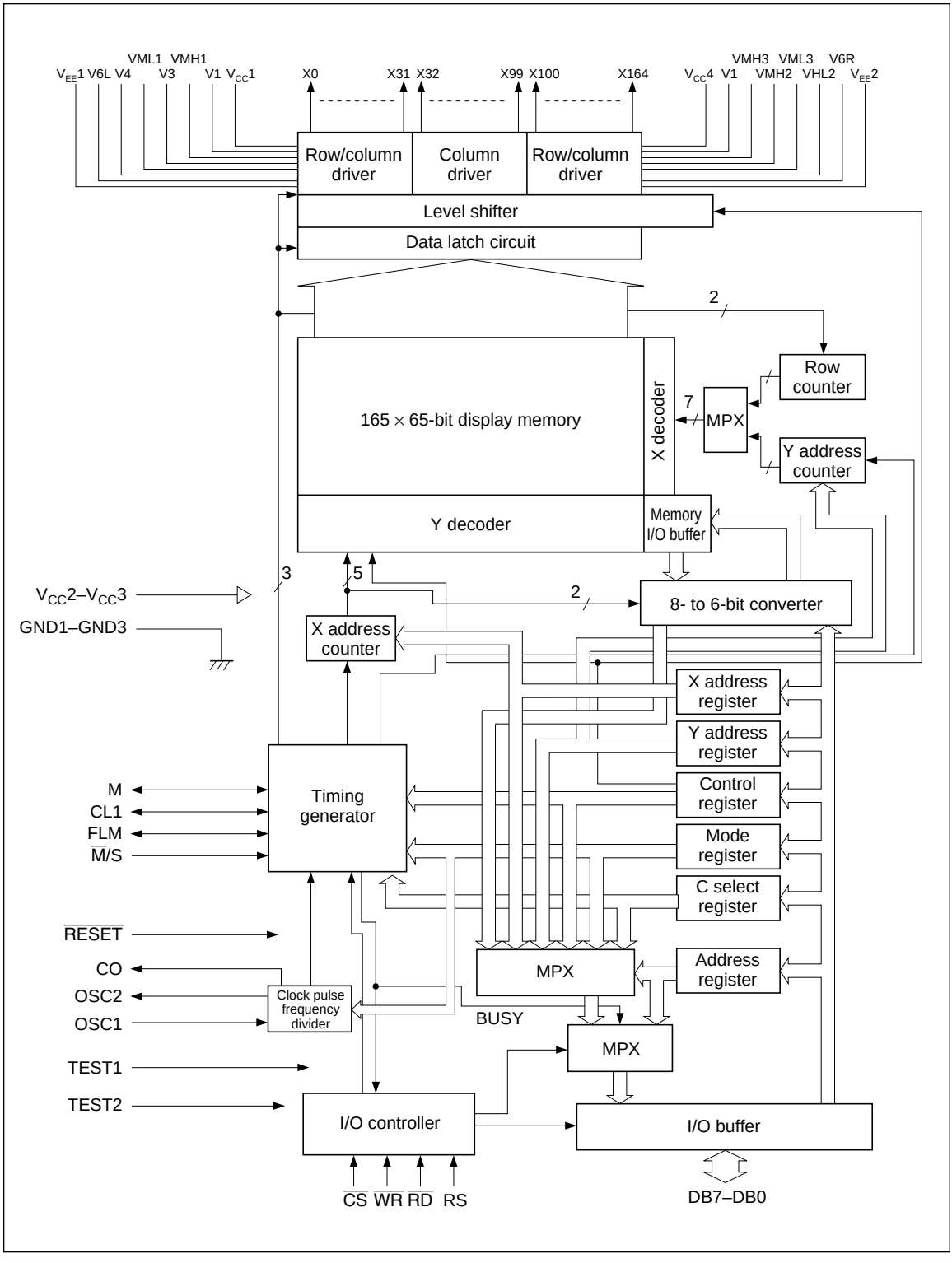
Note: The above view is seen from the back-ground surface of the chip, not TCP.

Pin Description

Classification	No. of Pins	Symbol	I/O	No. of Pins	Function
Power supply	8, 9, 35, 36	$V_{CC}1$–$V_{CC}4$	—	4	Connect these pins to V_{CC}.
	12 to 14	GND1–GND3	—	3	Ground these pins.
	1, 43	$V_{EE}1$, $V_{EE}2$	—	2	These pins supply power to the LCD driving circuits and should usually be set to the V6 level.
	2, 7 37, 42 4, 5 6, 39, 38 3, 40, 41	V6L, V1L, V1R, V6R, V4, V3, VMH1–VMH3, VML1–VML3	—	12	Apply an LCD driving voltage V1 to V6 to these pins.
CPU interface	23	$\overline{CS}$	I	1	Input a chip select signal via this pin. A CPU can access the HD66108T's internal registers only while the $\overline{CS}$ signal is low.
	25	$\overline{WR}$	I	1	Input a write enable signal via this pin.
	26	$\overline{RD}$	I	1	Input a read enable signal via this pin.
	24	RS	I	1	Input a register select signal via this pin.
	27 to 34	DB7–DB0	I/O	8	Data is transferred between the HD66108T and a CPU via these pins.
LCD driving output	44 to 208	X164–X0	O	165	These pins output LCD driving signals. The X0–X31 and X100–X164 pins are column/row common pins and output row driving signals when so programmed. X32–X99 pins are column pins.
LCD interface	21	FLM	I/O	1	This pin outputs a first line marker when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.
	20	CL1	I/O	1	This pin outputs latch clock pulses of display data when the chip is a master chip and inputs clock CL1 pulses when the chip is a slave chip.
	22	M	I/O	1	This pin outputs or inputs an M signal, which converts LCD driving outputs to AC; it outputs the signal when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.

Classification	No. of Pins	Symbol	I/O	No. of Pins	Function
Control signals	10	OSC1	I	1	Input system clock pulses via this pin.
	11	OSC2	O	1	This pin outputs clock pulses generated by the internal CR oscillator.
	19	CO	O	1	This pin outputs the same clock pulses as the system clock pulses, the OSC1 pin of a slave chip. Connect with the OSC1 pin of a slave chip.
	18	$\overline{M}$/S	I	1	This pin specifies master/slave. Set this pin low when the HD66108T is a master chip and set high when the chip is a slave chip; must not be changed after power-on.
	17	$\overline{RESET}$	I	1	Input a reset signal via this pin. Setting this pin low initializes the HD66108T.
	15, 16	TEST1, TEST2	I	2	These pins input a test signal and should usually be set low.

Internal Block Diagram



Register List

$\overline{CS}$	RS	Reg. No. 2	1	0	Reg. Symbol	Register Name	Read/ Write	Data Bit Assignment 7	6	5	4	3	2	1	0	Busy Time	Notes
1	—	—	—	—	—	Invalid	—									—	1
0	0	—	—	—	AR	Address	R	Busy	STBY	DISP			Register No.			None	
							W										
0	1	0	0	0	DRAM	Display memory	R	D7	D6	D5	D4	D3	D2	D1	D0	8 clocks max	2
							W										3
0	1	0	0	1	XAR	X address	R				XAD					None	
							W									1.5 clocks max	
0	1	0	1	0	YAR	Y address	R		YAD							None	
							W									1.5 clocks max	
0	1	0	1	1	FCR	Control	R	INC	WLS	PON	ROS		DUTY			None	
							W										
0	1	1	0	0	MDR	Mode	R				FFS			DWS		None	
							W										
0	1	1	0	1	CSR	C select	R			EOR	CLN					None	
							W										
0	1	1	1	0	—	Invalid	—									—	
0	1	1	1	1	—	Invalid	—									—	

Notes:
1. Shaded bits are invalid. Writing 1 or 0 to invalid bits does not affect LSI operation. Reading these bits returns 0.
2. DRAM is not actually a register but can be handled as one.
3. Setting the WLS bit of control register to 1 invalidates D7 and D6 bits of the display memory register.
4. DRAM must not be written to or read from until a time period of t_{CL1} has elapsed rewriting the DUTY bit of FCR or the FFS bit of MDR. t_{CL1} can be obtained from the following equation; in general, a time period of 1 ms or greater is sufficient if the frame frequency is 60–90 Hz.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}\ (kHz)}\ (ms) \quad \text{..... Equation 1}$$

D2 (duty correction value 2): 192 (duty = 1/32, 1/34, or 1/36)
128 (duty = 1/48 or 1/50)
96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits):
2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8
Refer to "6. Clock and Frame Frequency."

f_{CLK}: Input clock frequency (kHz)

System Description

The HD66108T can assign a maximum of 65 out of 165 channels to row outputs for LCD driving. It also incorporates a timing generator and display memory, which are necessary to drive an LCD.

If connected to an MPU and supplied with LCD driving voltage, one HD66108T chip can be used to configure an LCD system with a 100 × 65 dot panel (figure 1). In this case, clock pulses should be supplied by the internal CR oscillator or the MPU.

Using LCD expansion signals CL1, FLM and M enables the display size to be expanded. In this case, LCD expansion signal pins output corresponding signals when pin $\overline{M}$/S is set low for master mode and conversely input corresponding signals when pin $\overline{M}$/S is set high for slave mode; LCD expansion signal pins of both master chip and slave chips must be mutually connected. Figure 2 shows a basic system configuration using two HD66108T chips.

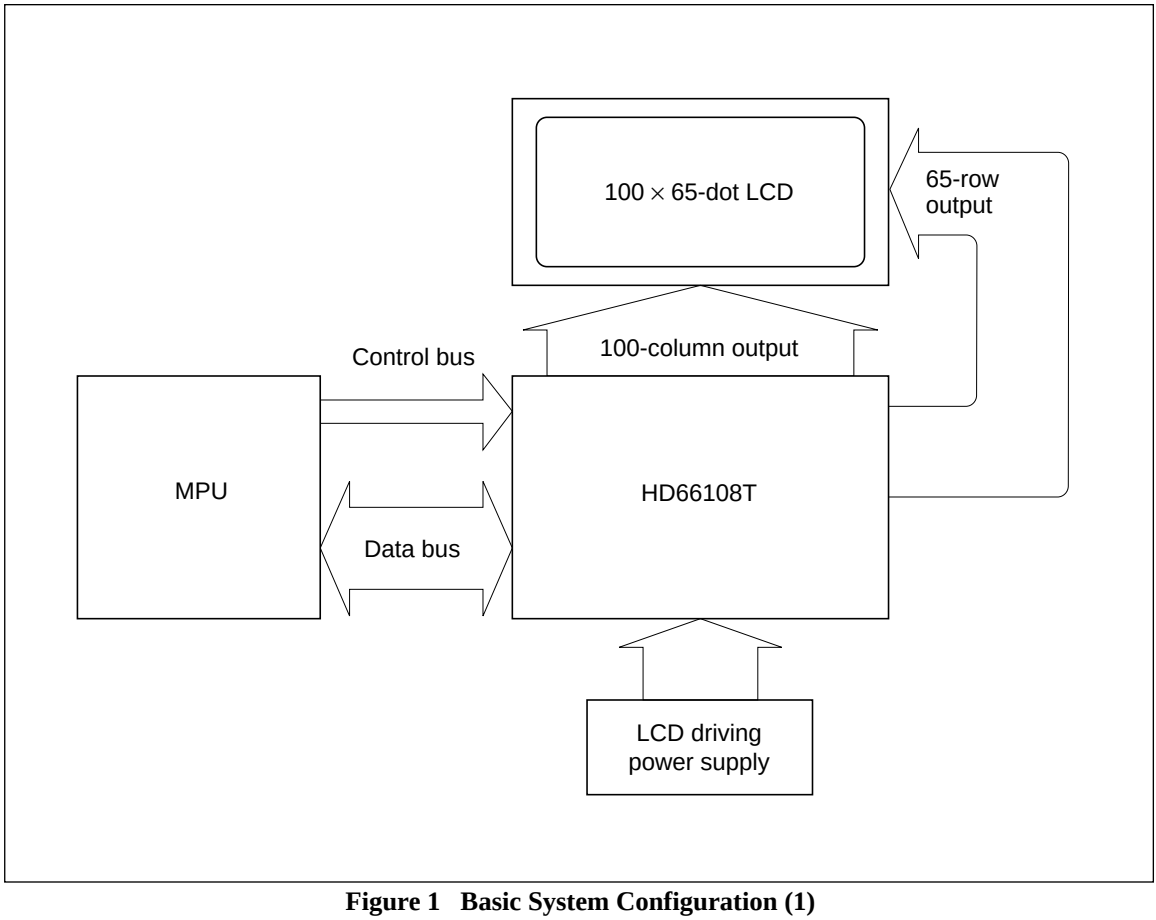


Figure 1 Basic System Configuration (1)

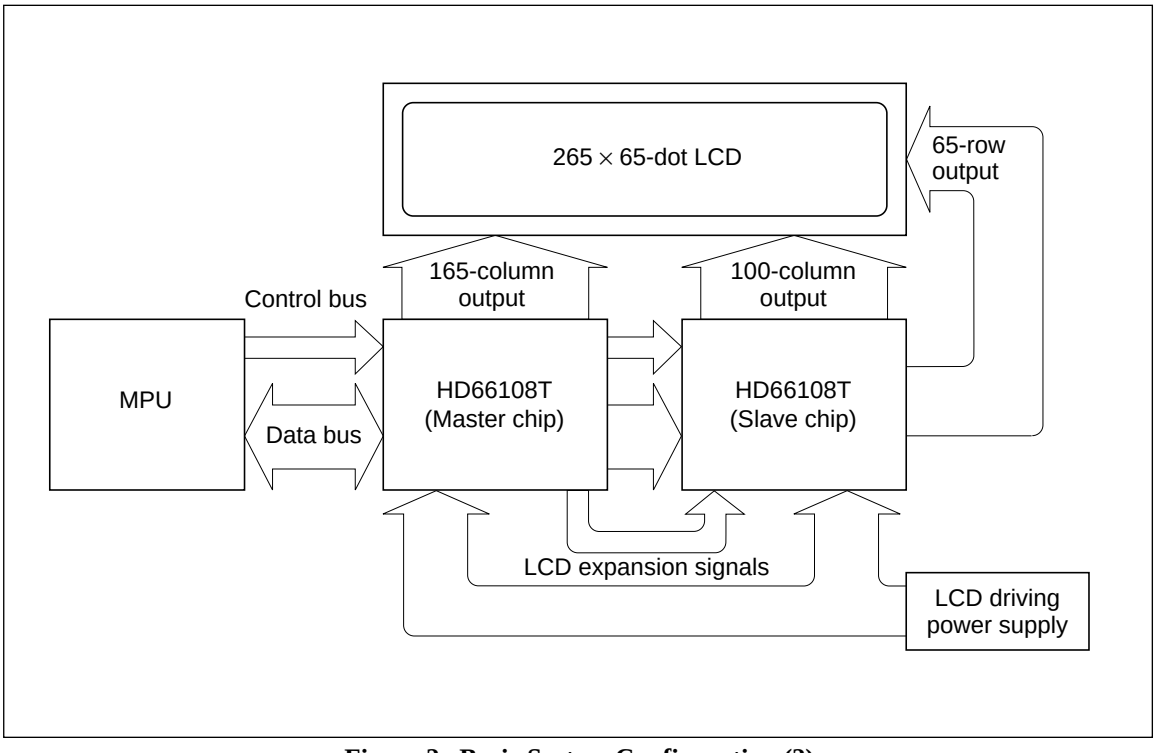


Figure 2 Basic System Configuration (2)

Functional Description

1. Display Size Programming

A variety of display sizes can be programmed by changing the system configuration and internal register settings.

(1) System Configuration Using One HD66108T Chip

When the 65-row-output mode is selected by internal register settings, a maximum of 100 dots in the X direction can be displayed (figure 3 (a)). Display size in the Y direction can be selected from 32, 34, 36, 48, 50, 64, and 65 dots according to display duty setting. Note that Y direction settings does not affect those in the X direction (100 dots).

When the 33-row-output mode is selected by internal register settings, a maximum of 132 dots in the X direction can be displayed (figure 3 (b)).

Table 1 shows the relationship between display sizes and the control register's (FCR) ROS and DUTY bits. ROS and DUTY bit settings determine the function of X pins. For more details, refer to "4.1 Row Output Pin Selection."

(2) System Configuration Using One HD66108T Chip and One HD61203 Chip as Row Driver

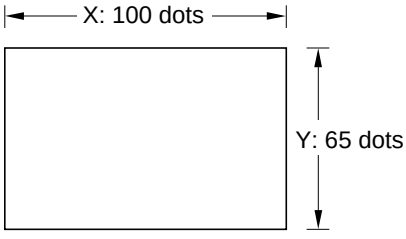
A maximum of 64 dots in the Y direction and 165 dots in the X direction can be displayed. 48 or 64 dots in the Y direction can be selected by HD61203 pin settings (figure 3 (c)).

(3) System Configuration Using Two or more HD66108T Chips

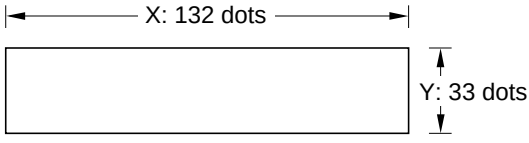
X direction size can be expanded by 165 dots per chip. Figure 3 (d) shows a 265 × 65-dot display. Y direction size can be expanded up to 130 dots with 2 chips; a 100 × 130-dot display provided by 2 chips is shown in figure 3 (e).

Table 1 Relationship between Display Size and Register Settings (No. of Dots)

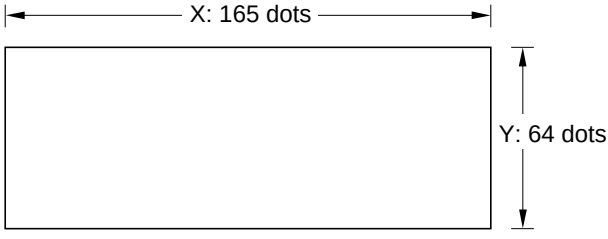
ROS Bit Setting (X0–X164 Pin Function)	Duty Bit Setting (Multiplexing Duty Ratio)						
	1/32	1/34	1/36	1/48	1/50	1/64	1/66
165-column-output	Specified by a row driver						
65-row-output from the right side	X: 100 Y: 32	X: 100 Y: 34	X:100 Y: 36	X: 100 Y: 48	X: 100 Y: 50	X: 100 Y: 64	X:100 Y: 65
65-row-output from the left and right sides	X: 100 Y: 32	X: 100 Y: 34	X:100 Y: 36	X: 100 Y: 48	X: 100 Y: 50	X: 100 Y: 64	X:100 Y: 65
33-row-output from the right side	X: 132 Y: 32	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33



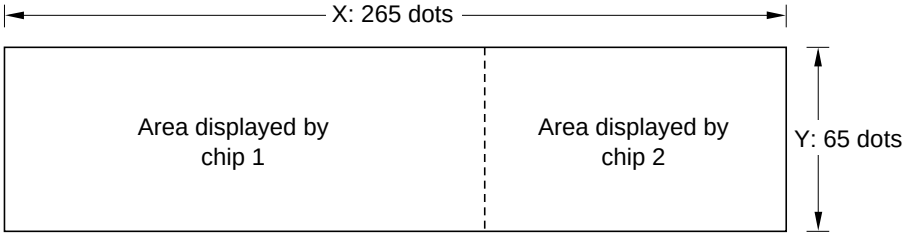
(a) Configuration Using One HD66108T Chip (1)
(65-Row Output from the Right Side)



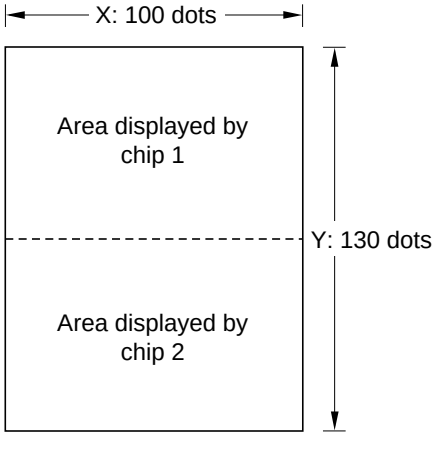
(b) Configuration Using One HD66108T Chip (2)
(33-Row Output from the Right Side)



(c) Configuration Using One HD66108T Chip and One HD61203 as Row Driver
(165-Column Output)



(d) Configuration Using Two HD66108T Chips (1)



(e) Configuration Using Two HD66108T Chips (2)

Figure 3 Relationship between System Configurations and Display Sizes

2. Display Memory Construction and Word Length Setting

The HD66108T has a bit-mapped display memory of 165 × 65 bits. As shown in figure 4, data from the MPU is stored in the display memory, with the MSB (most significant bit) on the left and the LSB (least significant bit) on the right.

The sections on the LCD panel corresponding to the display memory bits in which 1's are written will be displayed as on (black).

Display area size of the internal RAM is determined by control register (FCR) settings (refer to table 1).

The start address in the Y direction for the display area is always Y0, independent of the register setting. In contrast, the start address in the X direction is X0 in the modes for 165-column-output, 65-row-output from the right side, and 33-row-output from the right side, and is X32 in the 65-row-output mode from the left and right sides.

Each display area contains the number of dots shown in table 1, beginning from each start address.

For more detail, refer to "4.2 Row Output Data Setting," figures 15 to 19.

In the display memory, one X address is assigned to each word of 8 or 6 bits long in X direction. (Either 8 or 6 bits can be selected as word length of display data.) Similarly, one Y address is assigned to each row in Y direction.

Accordingly, X address 20 in the case of 8-bit word and X address 27 in the case of 6-bit word have 5 and 3 bits of display data, respectively. Nevertheless, data is also stored here with the MSB on the left (figure 5).

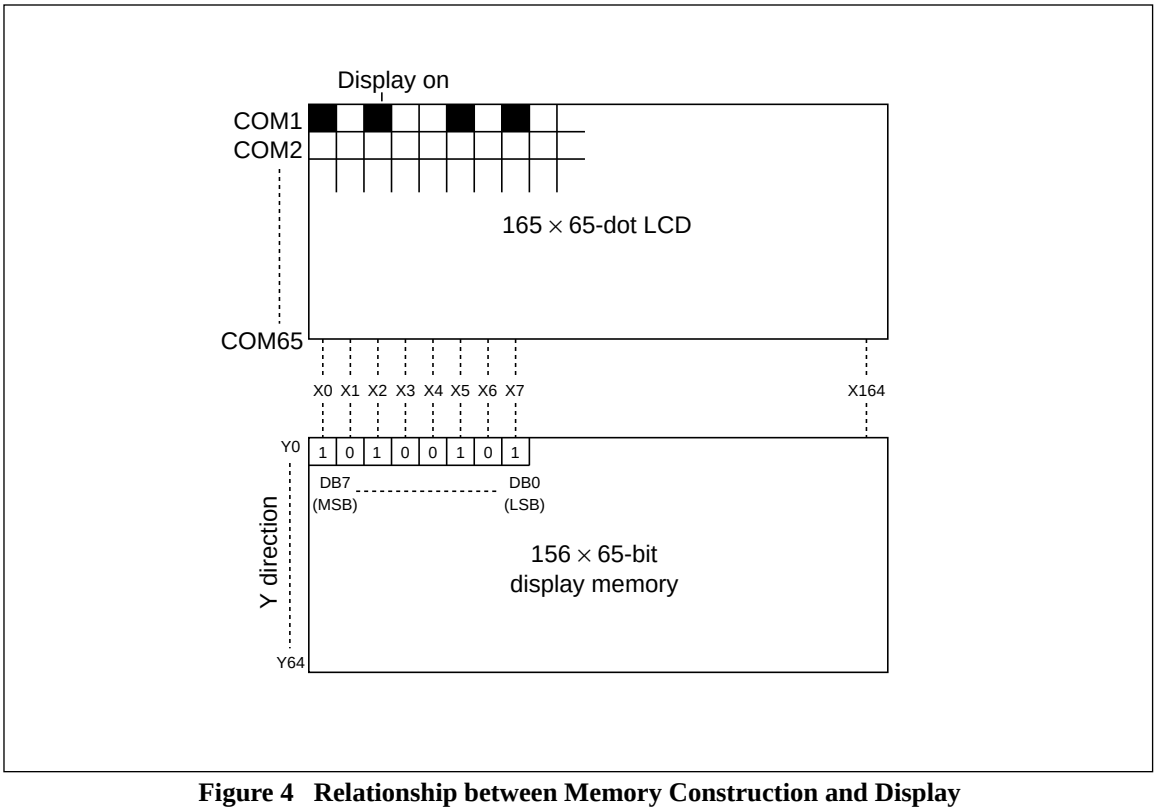
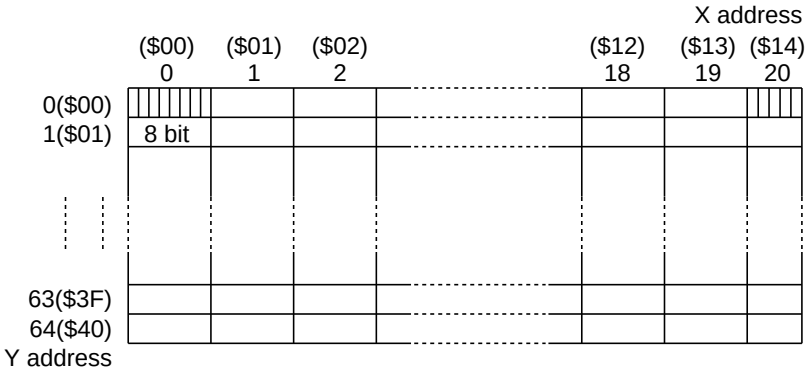
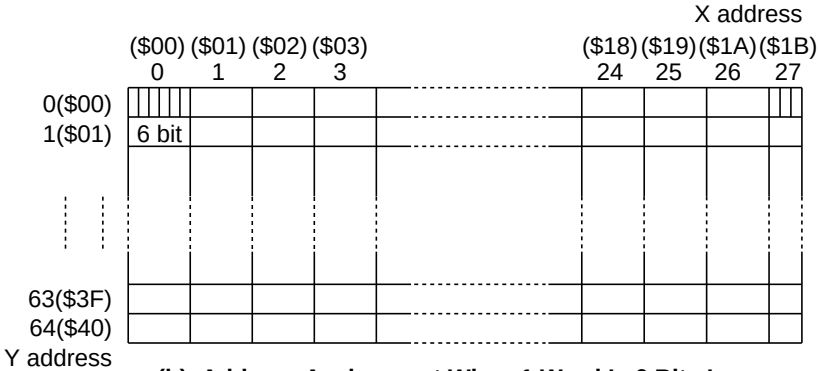


Figure 4 Relationship between Memory Construction and Display



(a) Address Assignment When 1 Word Is 8 Bits Long



(b) Address Assignment When 1 Word Is 6 Bits Long

Figure 5 Display Memory Addresses

3. Display Data Write

3.1 Display Memory and Data Register Accesses

(1) Access

Figure 6 shows the relationship between the address register (AR) and internal registers and display memory in the HD66108T. Display memory shall be referred to as a data register since it can be handled as other registers.

To access a data register, the register address assigned to the desired register must be written into the address register's Register No. bits. The MPU will access only that register until the register address is updated.

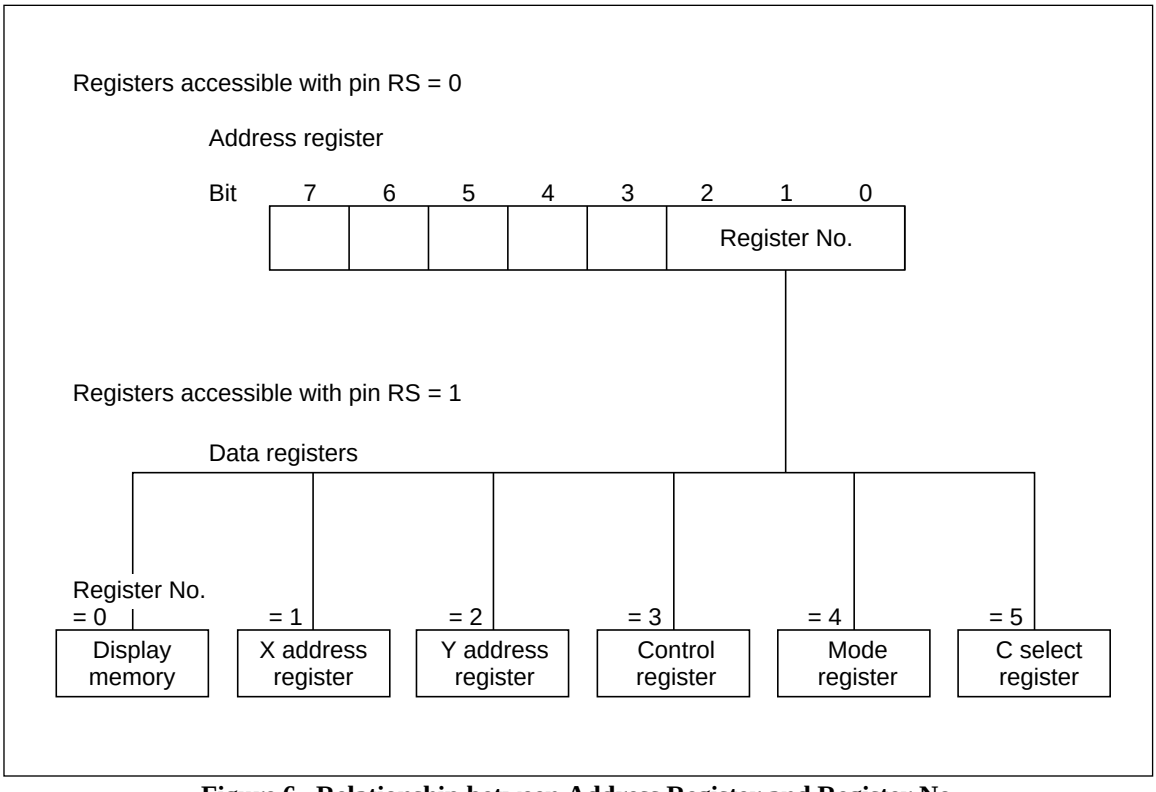


Figure 6 Relationship between Address Register and Register No.

(2) Busy Check

A busy time period appears after display memory read/write or X or Y address register write, since post-access processing is performed synchronously with internal clock pulses. Updating data in registers other than the address register is disabled during this time. Subsequent data must be input after confirming ready mode by reading the address register. The busy time period is a maximum of 8 clock pulses after display memory read/write and a maximum of 1.5 clock pulses after X or Y address register write (figure 7).

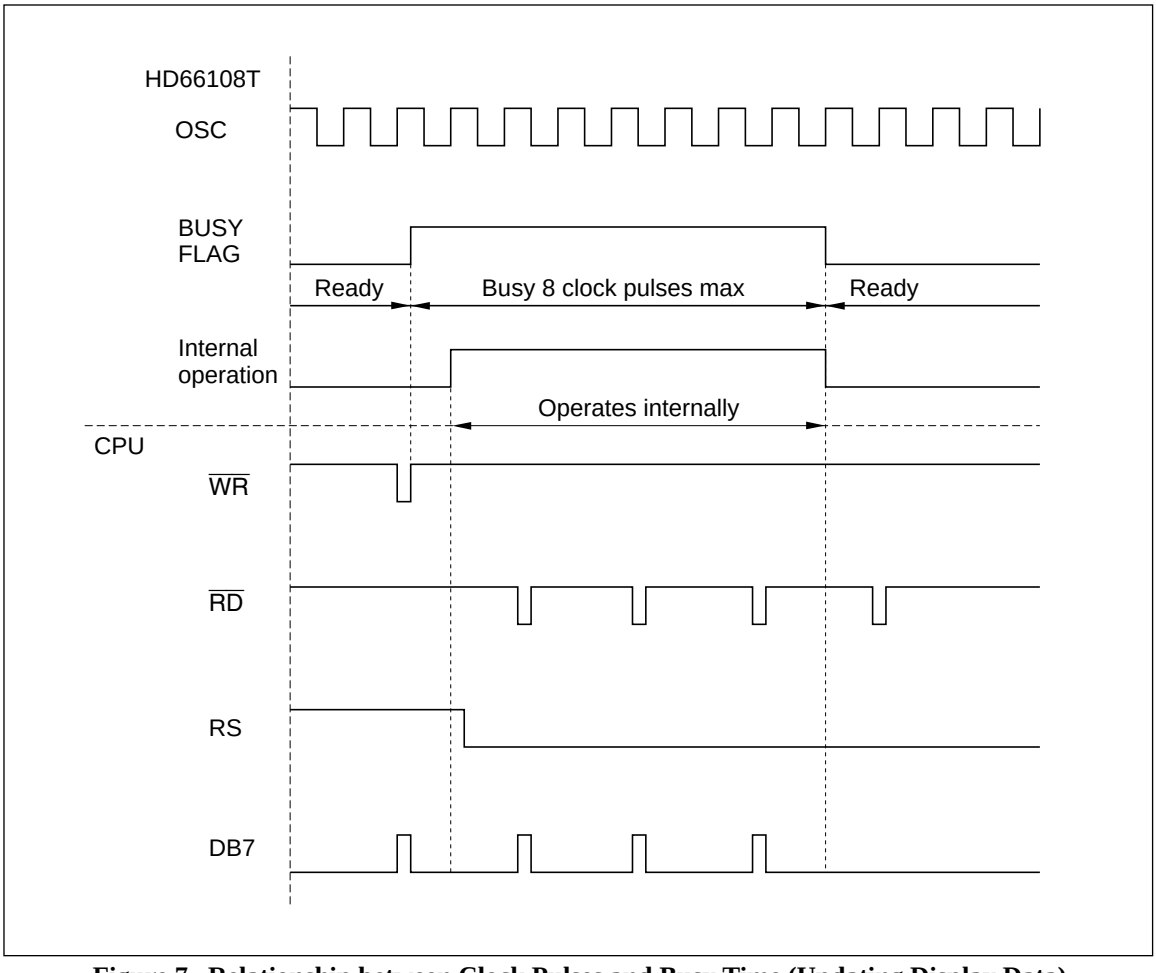


Figure 7 Relationship between Clock Pulses and Busy Time (Updating Display Data)

(3) Dummy Read

When reading out display data, the data which is read out immediately after setting the X and Y addresses is invalid. Valid data can be read out after one dummy read, which is performed after setting the X and Y addresses desired (figure 8).

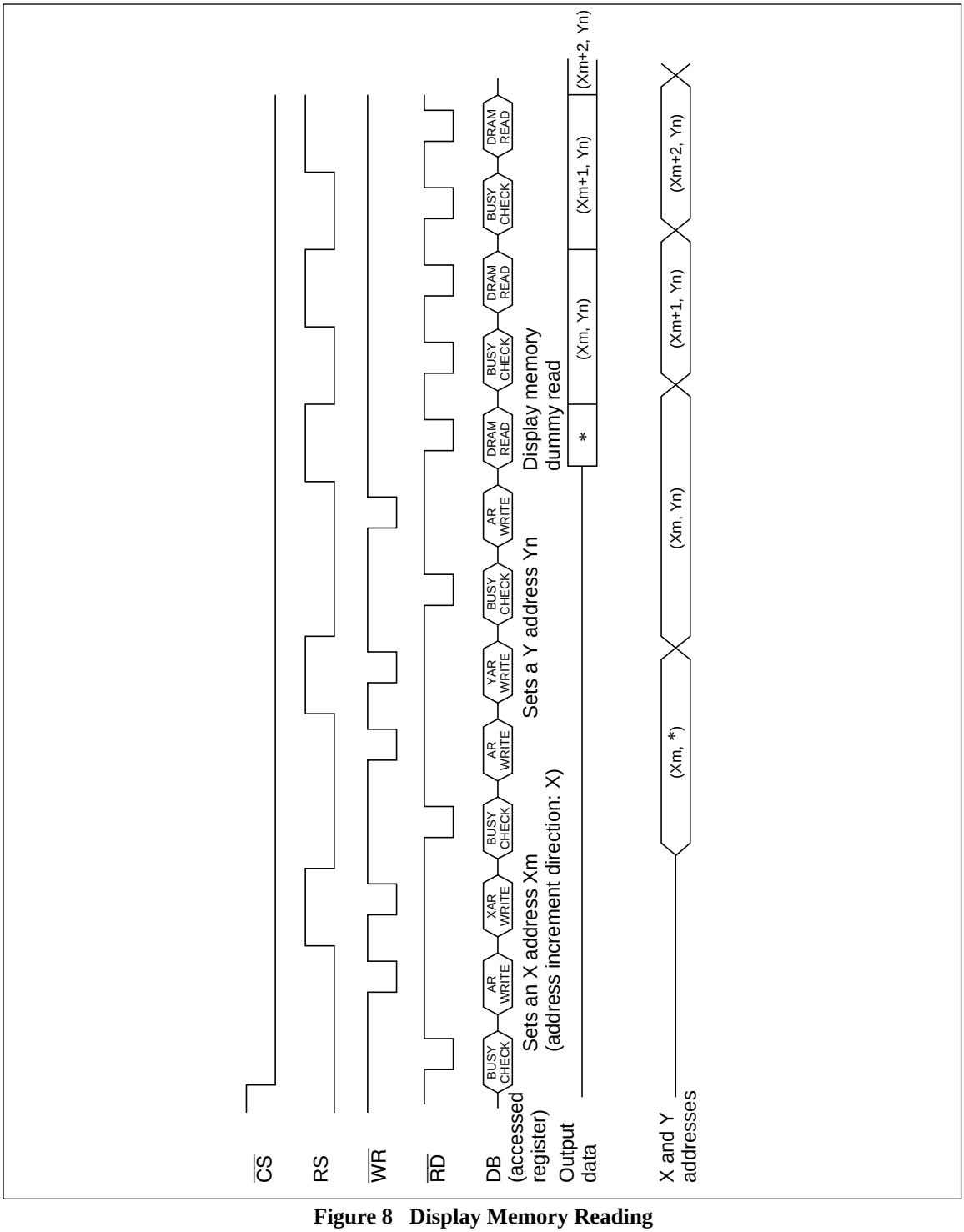


Figure 8 Display Memory Reading

(4) Limitations on Access

As shown in figure 9, the display memory must not be rewritten until a time period of t_{CL1} or longer has elapsed after rewriting the control register's DUTY bits or the mode register's FFS bits. However, display memory and registers other than the control register and mode register can be accessed even during this time period. t_{CL1} can be obtained from the following equation. If using an LSI with a frame frequency of 60 Hz or greater, a time period of 1 ms should be sufficient.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}\ (kHz)}\ (ms) \quad \text{..... Equation 1}$$

D2 (duty correction value 2):

192 (duty = 1/32, 1/34, or 1/36)

128 (duty = 1/48 or 1/50)

96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits):

2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8

f_{CLK}: Input clock frequency (kHz)

3.2 X and Y address Counter Auto-Incrementing Function

As described in "2. Display Memory Construction and Word Length Setting,'' the HD66108T display memory has X and Y addresses. Internal X address counter and Y address counter both employ an auto-incrementing function. After display data is read or written, the X or Y address is incremented according to the address increment direction selected by internal register.

Although X addresses up to 20 are valid when 8 bits make up one word (up to 27 when 6 bits make up one word), the X address counter can count up to 31 since it is a 5-bit free counter. Similarly, although Y addresses up to 64 are valid, the Y address counter can count up to 127. Consequently, X or Y address must be reset at an appropriate point as shown in figure 10.

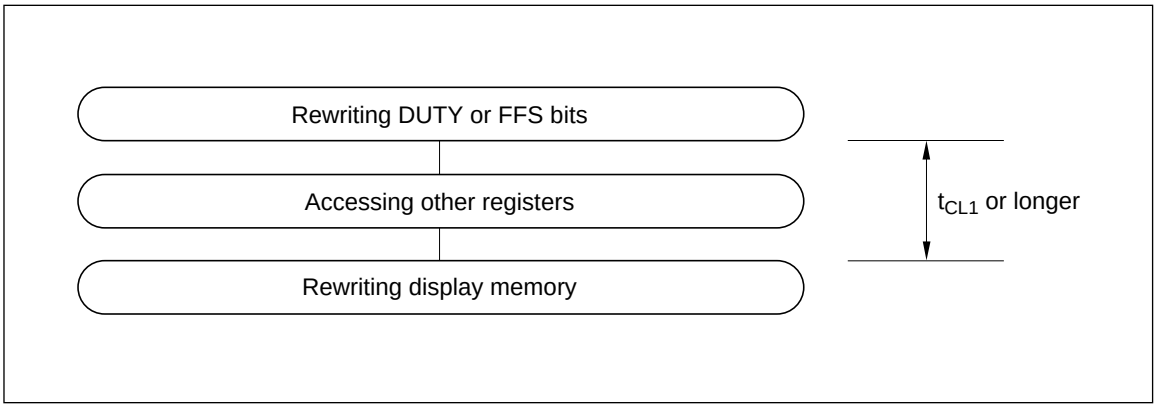
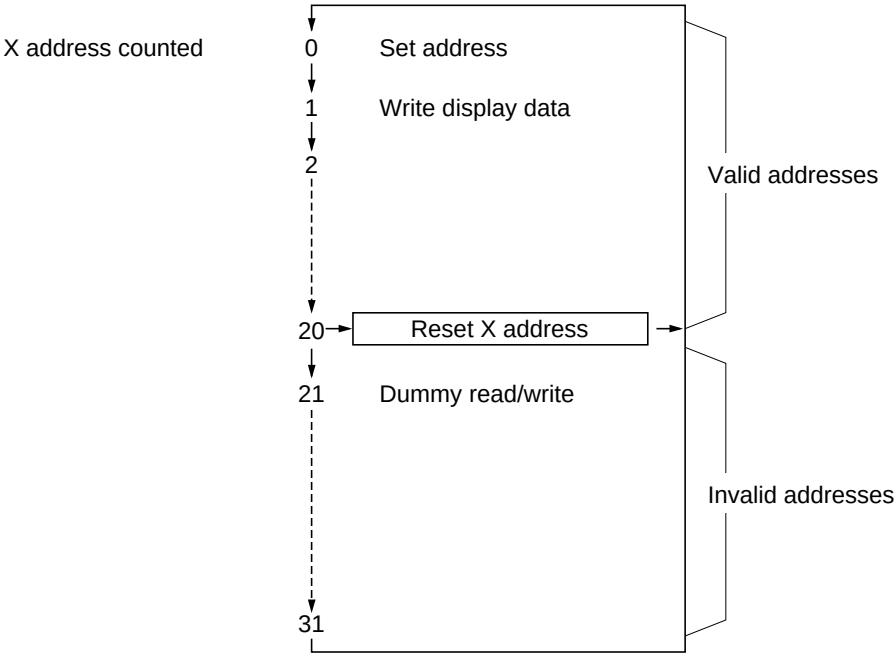
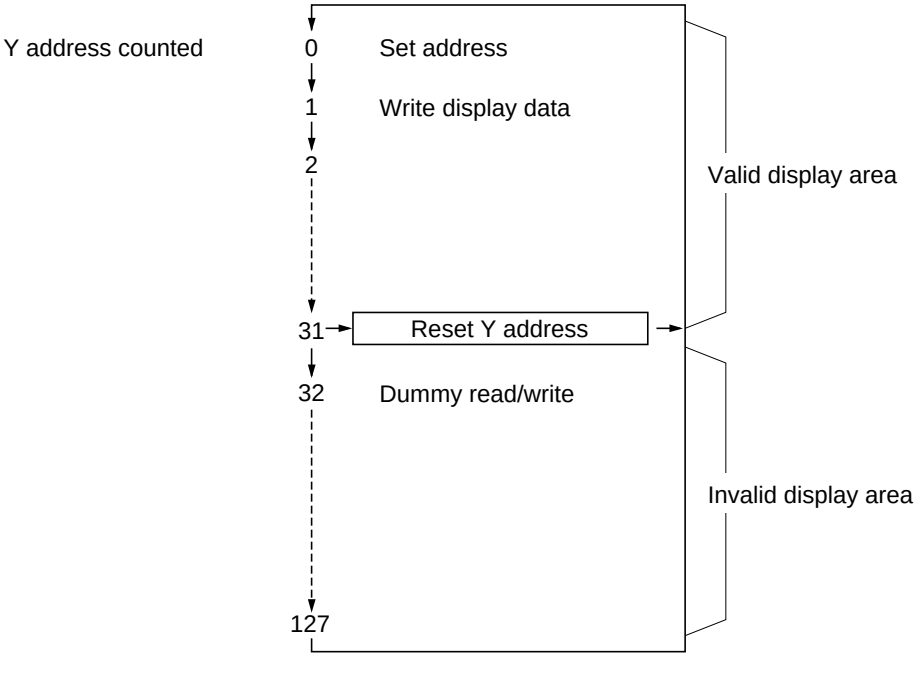


Figure 9 Rewriting Display Memory after Rewriting Registers



(1) Example of X Address Counter Increment (Word Length: 8 Bits)



(2) Example of Y Address Counter Increment (Multiplexing Duty Ratio: 1/32)

Figure 10 X/Y Address Counter Increment

4. Selection for LCD Driving Circuit Configuration

4.1 Row Output Pin Selection

The HD66108T can assign a maximum of 65 pins for row outputs among the 165 pins named X0–X164. The X0–X164 pins can be classified into four blocks labelled A, B, C, and D (figure 11 (a)). Blocks A, C, and D consist of row/column common pins and block B consists of column pins only. The output function of the LCD driving pins and the combination of blocks can be selected by internal registers.

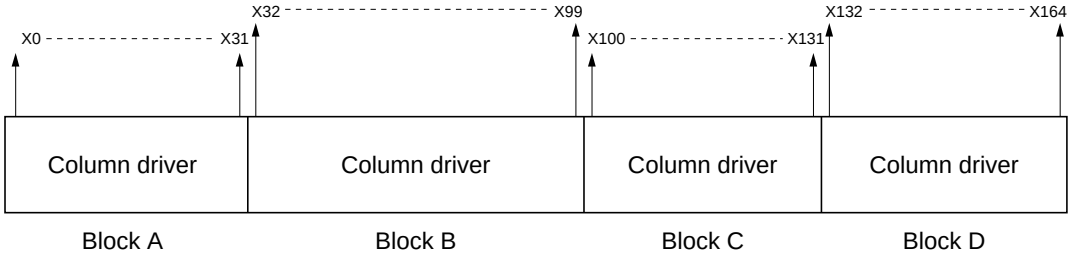
Figure 11 shows an example of 165-column-output mode. This configuration is useful when using more than one HD66108T chip or using the HD66108T as a slave chip of the HD61203.

Figure 12 shows an example of 65-row-output mode from the right side. Blocks A and B are used for column output and blocks C and D (X100–X164 pins) for row output. This configuration offers an easy way of connecting row output lines in the case of using one or more HD66108T chips.

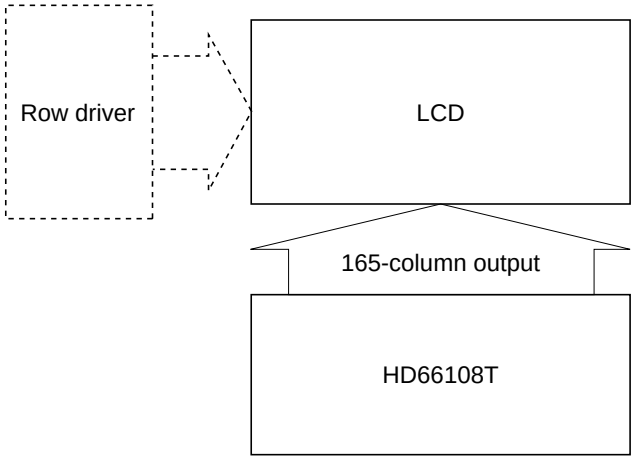
Figure 13 shows an example of 65-row-output mode from the left and right sides. 32 pins of X0–X31 and 33 pins of X132-X164 are used for row output here. This configuration offers an easy way of connecting row output lines in the case of using only one HD66108T chip.

Figure 14 shows an example of 33-row-output mode from the right side. Block D, i.e., X132–X164 pins, is used for row outputs. This configuration provides a means for assigning many pins to column outputs when 1/32 or 1/34 multiplexing duty ratio is desired.

In all modes, it is row data and multiplexing duty ratio that determine which pins are actually used among the pins assigned to row output. Y values shown in table 1 indicate the numbers of pins that are actually used. Pins not used must be left disconnected.

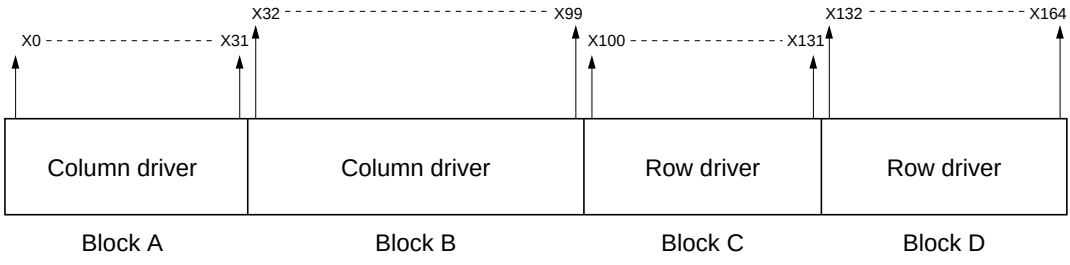


(a) LCD Driving Circuit Configuration

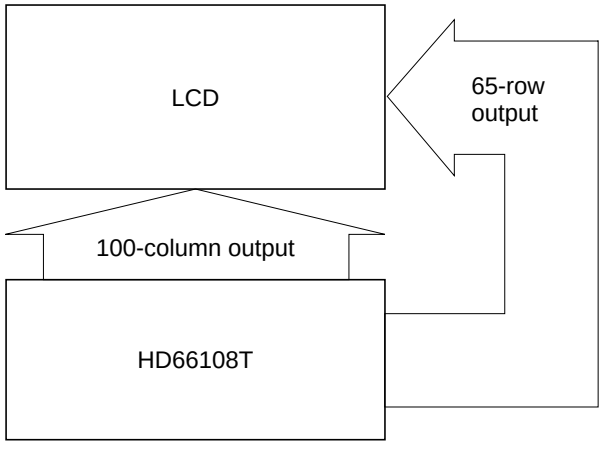


(b) System Configuration

Figure 11 165-Column-Output Mode

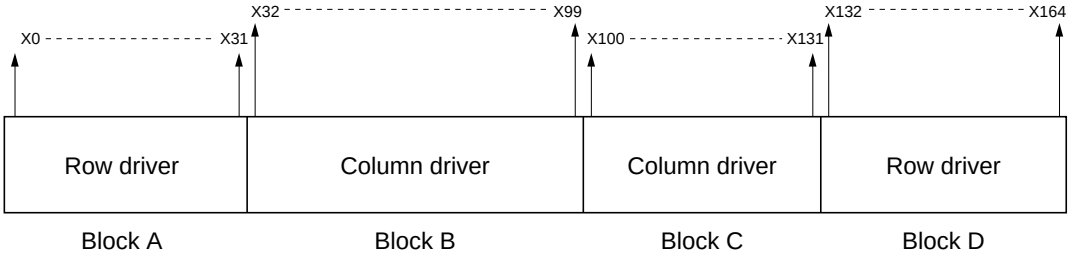


(a) LCD Driving Circuit Configuration

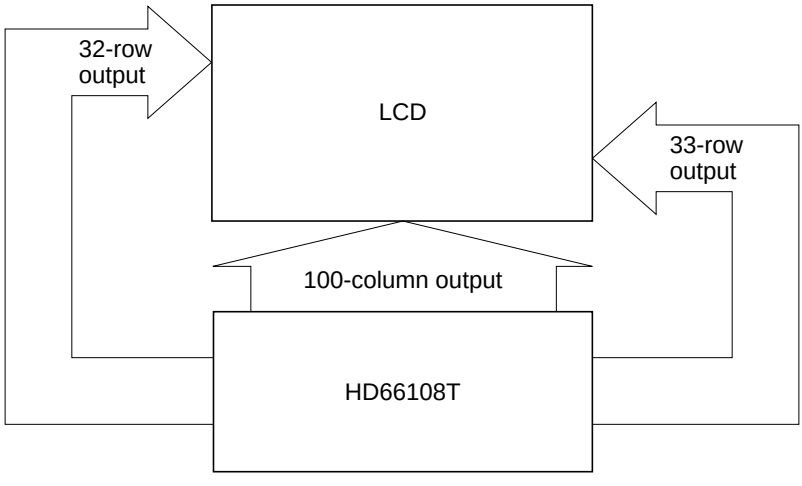


(b) System Configuration

Figure 12 65-Row-Output Mode from the Right Side

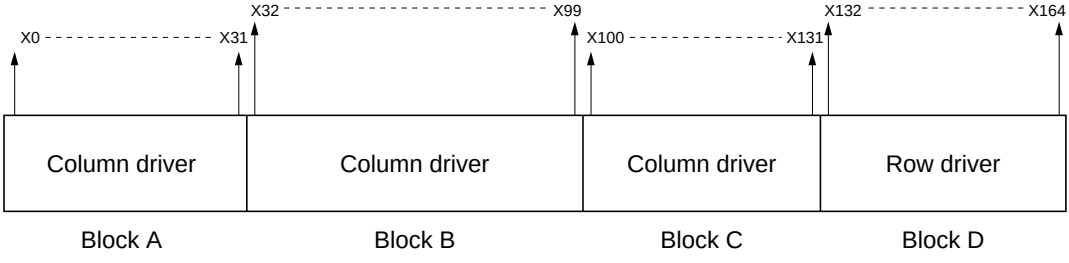


(a) LCD Driving Circuit Configuration

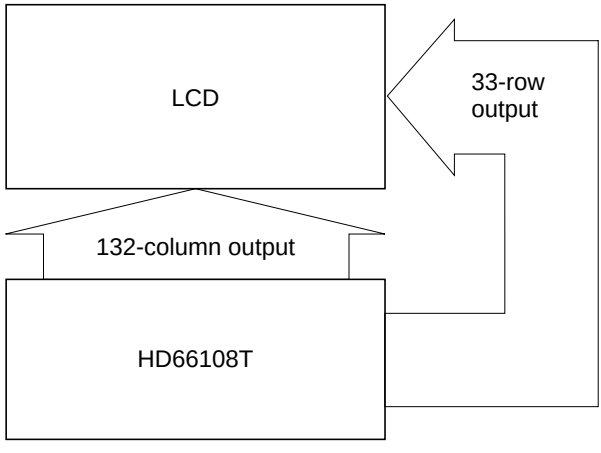


(b) System Configuration

Figure 13 65-Row-Output Mode from the Left and Right Sides



(a) LCD Driving Circuit Configuration



(b) System Configuration

Figure 14 33-Row-Output-Mode from the Right Side

4.2 Row Output Data Setting

If certain LCD driving output pins are assigned to row output, data must be written to display memory for row output. The specific area to which this data must be written depends on the row-output mode and the procedure of writing row data to the display memory (0 or 1 to which bits?) depends on which X pin drives which line of the LCD. Row data area is determined by the control register's (FCR) ROS and DUTY bits and is identical to the protected area, which will be described below. (165-column-output mode has no protected area, thus requiring no row data to be written (figure 15).)

Procedure of writing row data to the display memory is as follows. First, 1 must be written to the bit at the intersection between line Yj and line (column) Xi (column). Line Yj is filled with data to be displayed on the first line of the LCD and line Xi is connected to pin Xn, which drives the first line of the LCD. Following this, 0s must be written to the remaining bits on line Yj in the row data area. This rule applies to subsequent lines on the LCD.

Table 2 shows the relationship between FCR settings and protected areas.

Figure 16 shows the relationship between row data and display. Here the mode is 65-row output from the right side. Display data on Y0 is displayed on the first line of the LCD and data on Y64 is displayed on the 65th line of the LCD. If X164 is connected to the first line of the LCD and X100 is connected to the 65th line of the LCD, 1s must be written to the bits on the diagonal line between coordinates (X164, Y0) and (X100, Y64) and 0s to the remaining bits. Row data protect function must be turned off before writing row data and be turned on after writing row data. Turning on the row data protect function disables read/write of display memory area corresponding to the row output pins, i.e., prevents row data from being destroyed. In figure 16, display memory area corresponding to pins X100 to X164 is protected.

Figures 17 to 19 show examples of row data settings. Some multiplexing duty ratios result in invalid display areas. Although an invalid display area can be read from or written to, it will not be displayed.

Table 2 Relationship between FCR Settings and Protected Areas

Control Register (FCR)					
	ROS			LCD Driving Signal Output Pins Connected to	
PON	4	3	Mode	Protected Area of Display Memory	Figures
1	0	0	165-column	No area protected	15
1	0	1	65-row (R)	X100–X164	16, 19
1	1	0	65-row (L/R)	X0–X31 and X132–X164	17
1	1	1	33-row (R)	X132–X164	18

65-row (R) : 65-row-output mode from the right side
65-row (L/R): 65-row-output mode from the left and right sides
33-row (R): 33-row-output mode from the right side

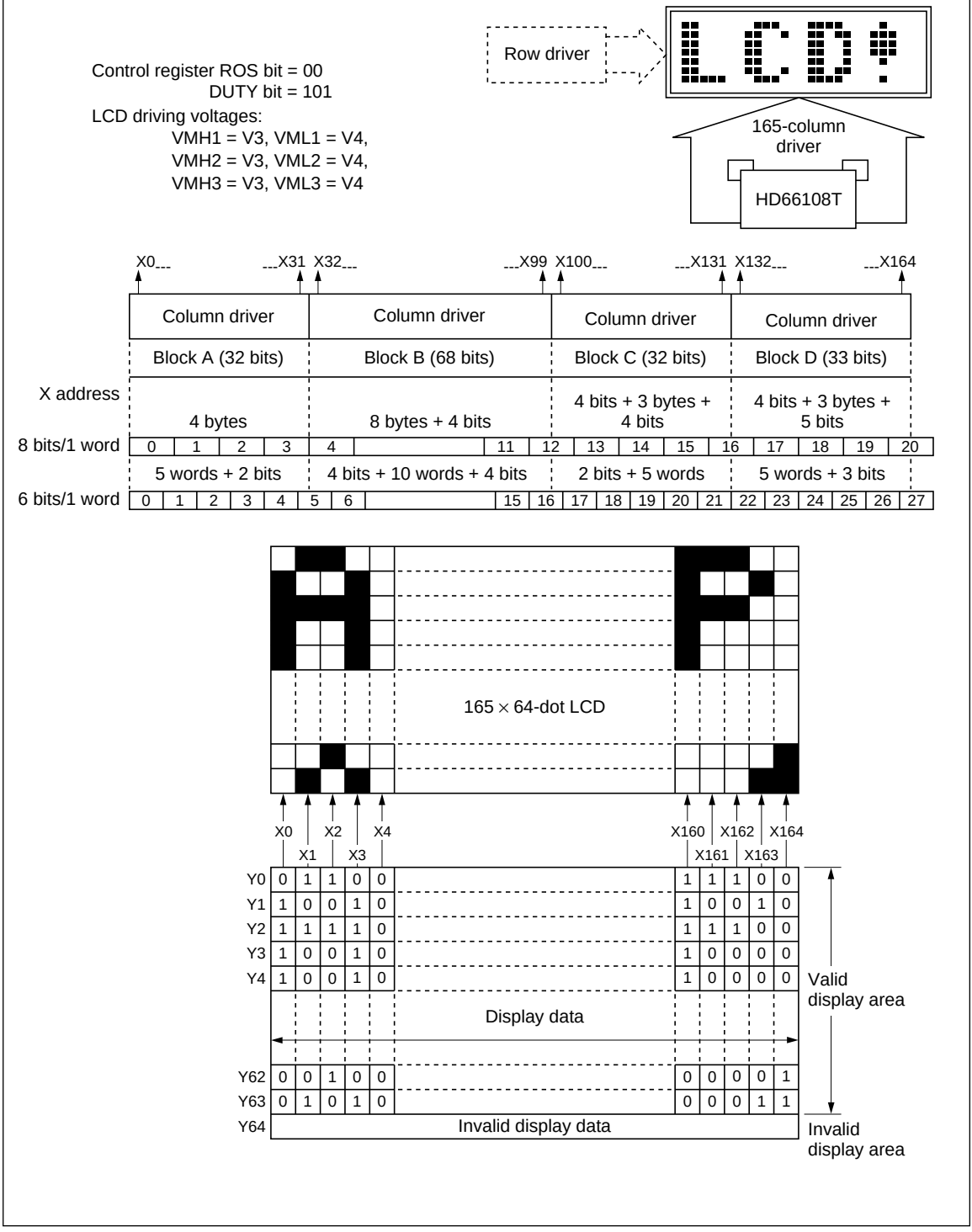


Figure 15 Relationship between Row Data and Display (165-Column Output, 1/64 Multiplexing Duty Ratio)

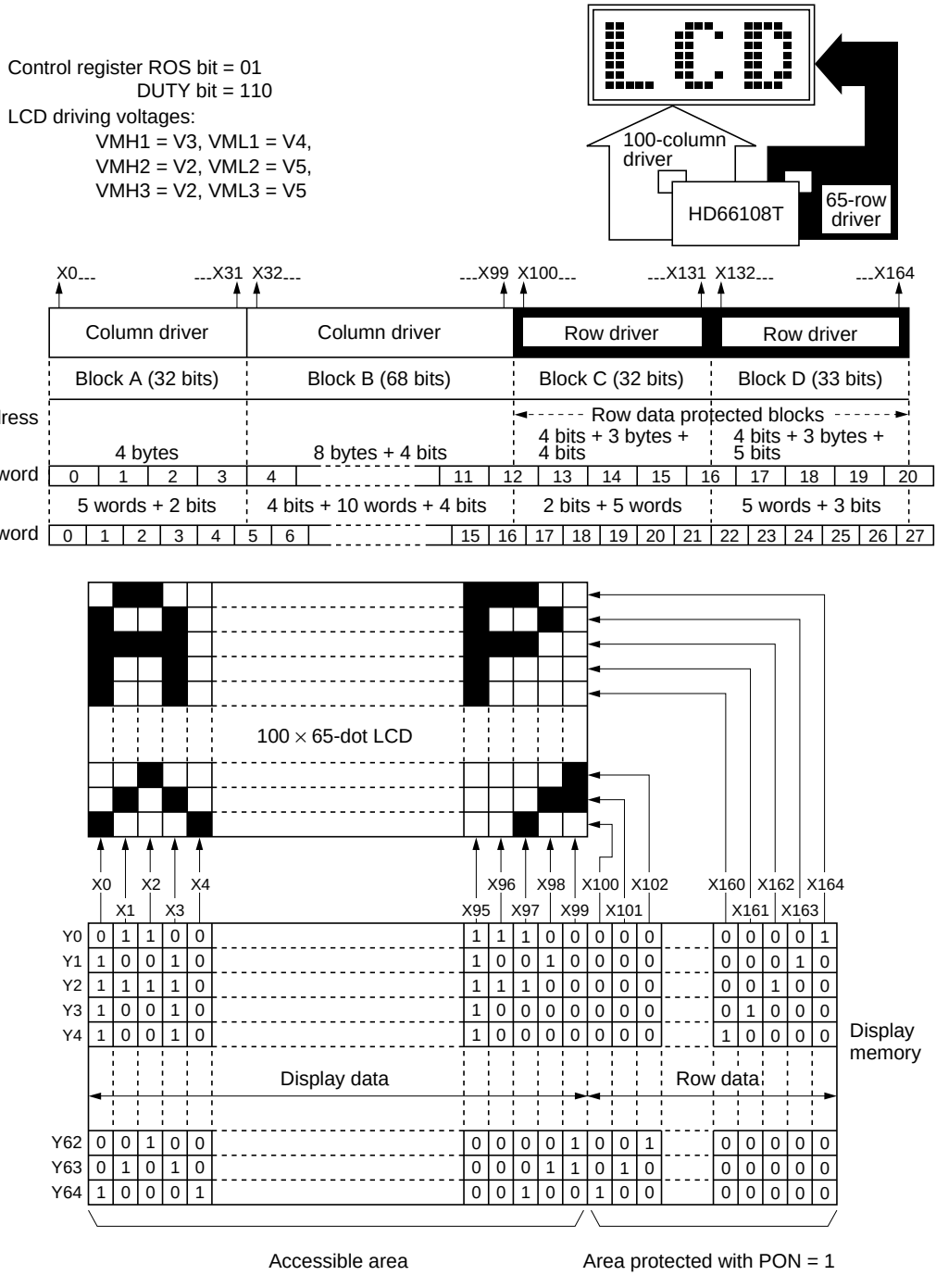


Figure 16 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/66 Multiplexing Duty Ratio)

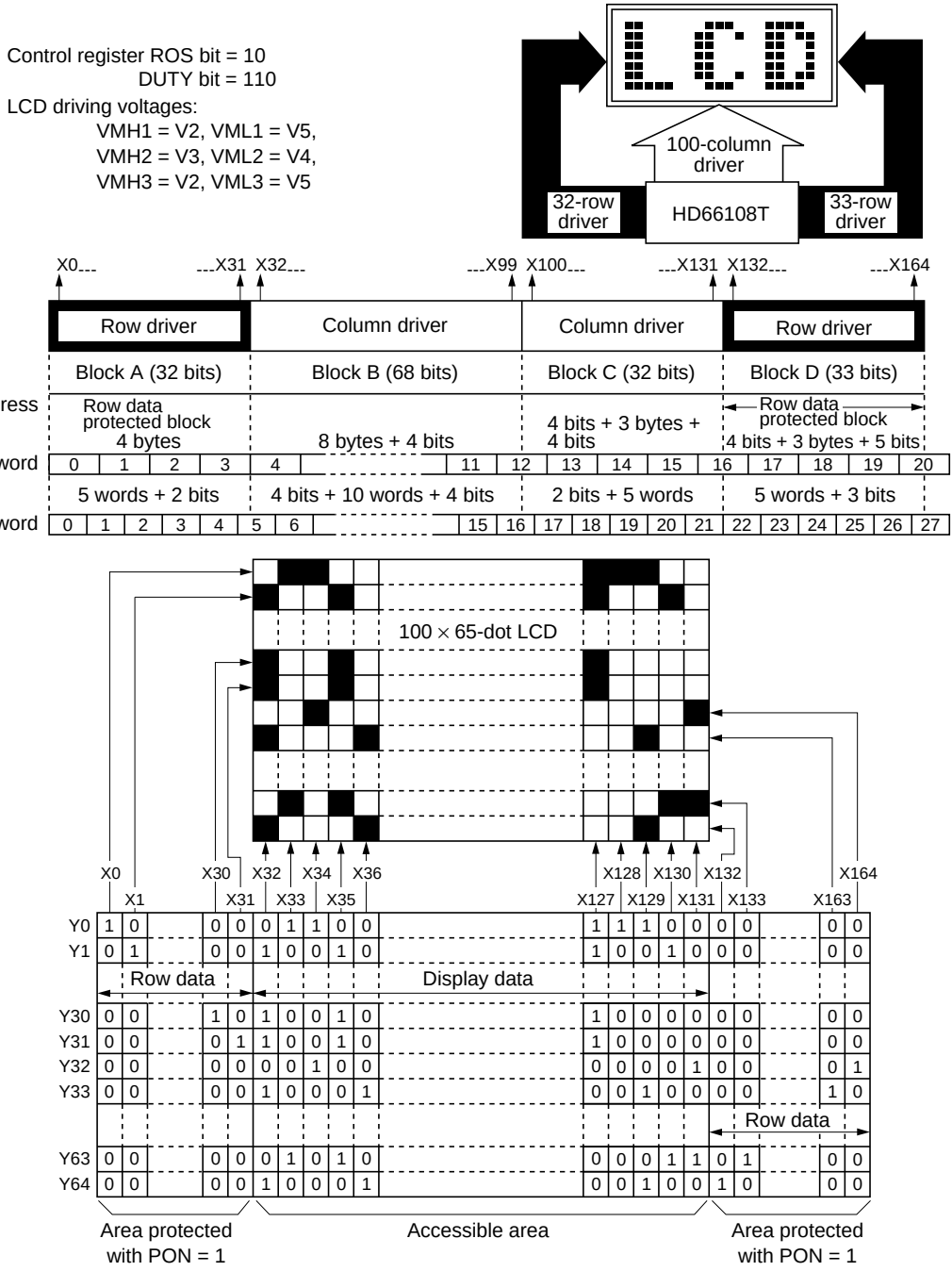


Figure 17 Relationship between Row Data and Display (65-Row Output from the Left and Right Sides, 1/66 Multiplexing Duty Ratio)

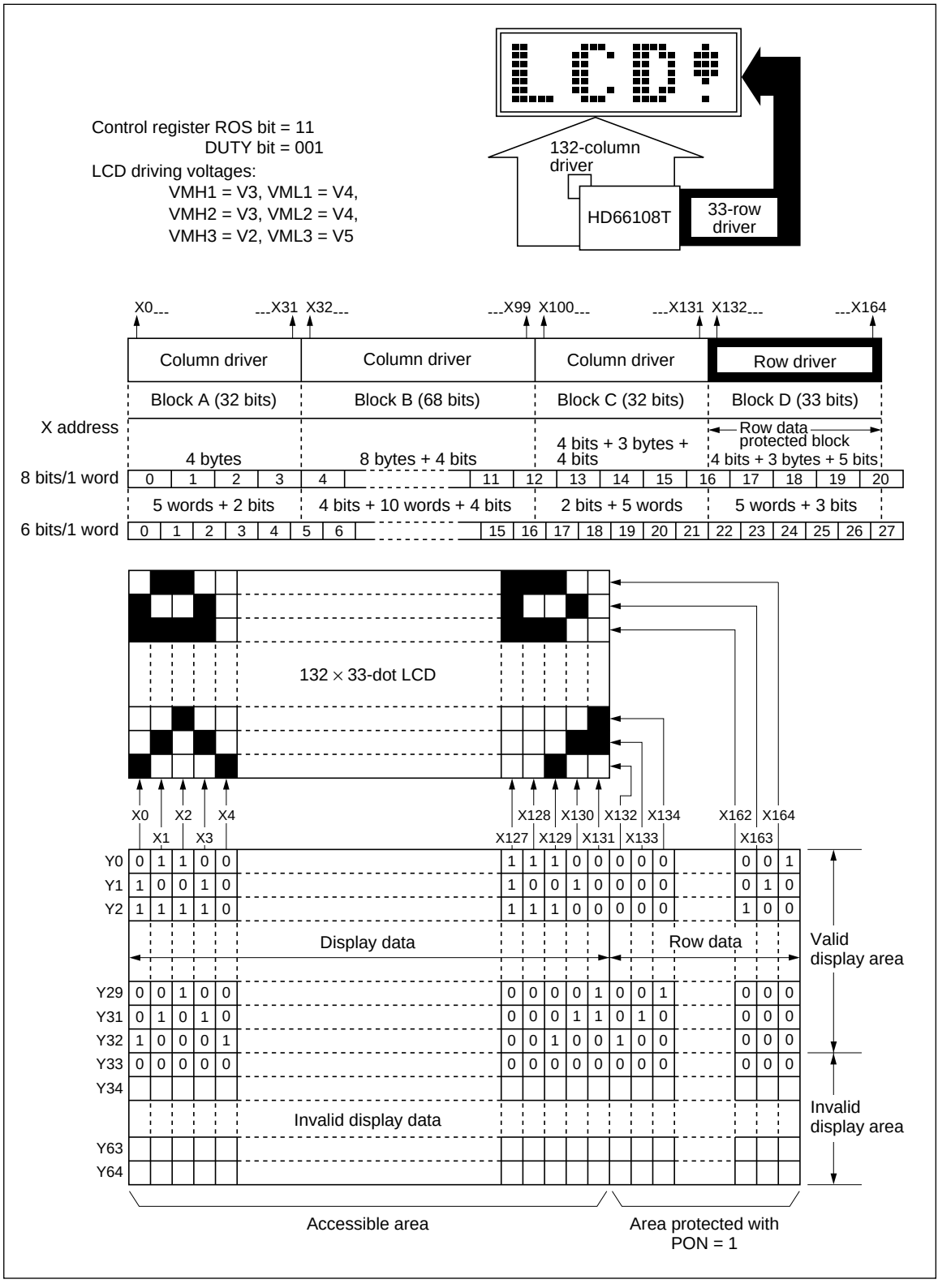
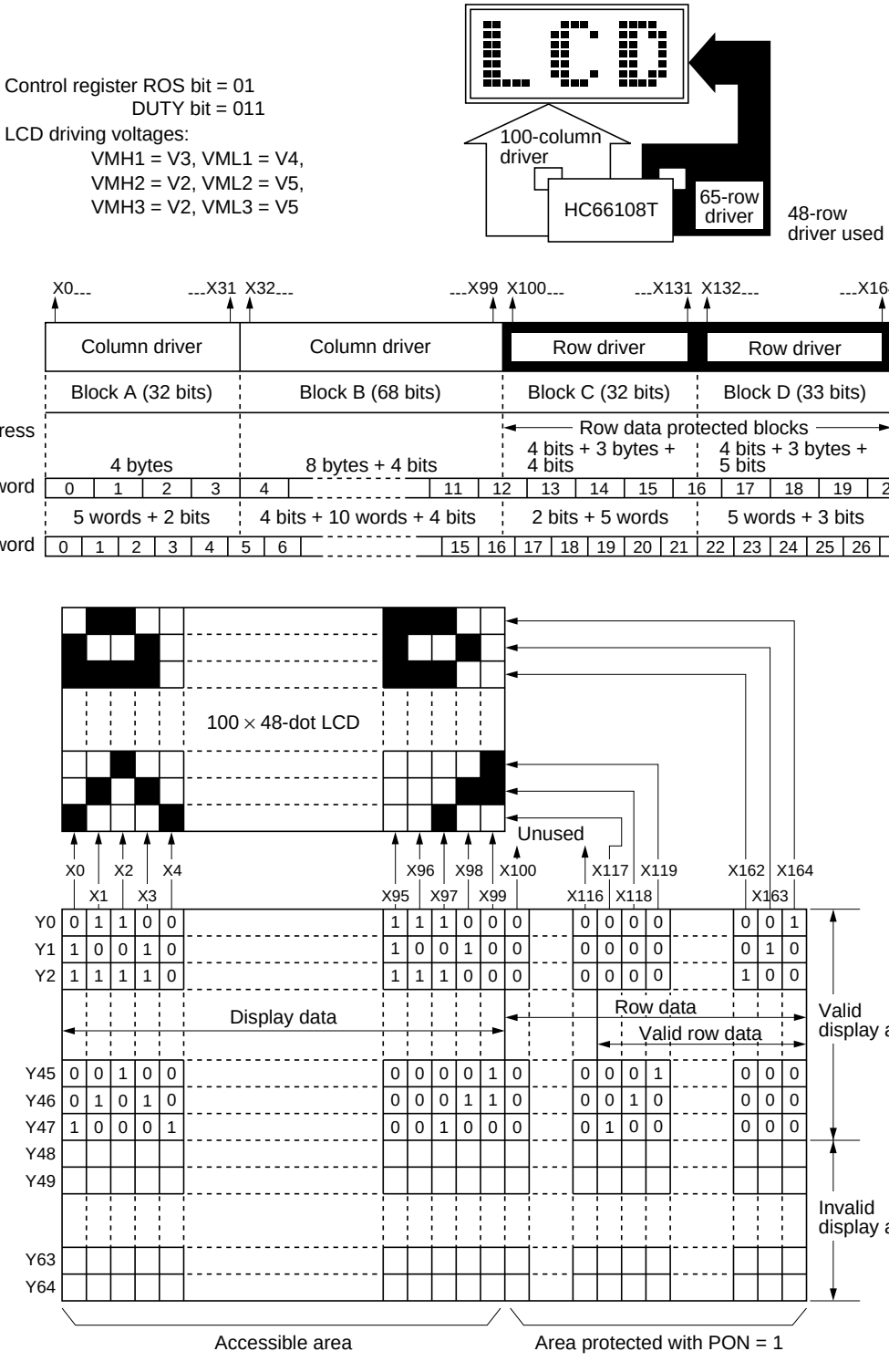


Figure 18 Relationship between Row Data and Display (33-Row Output from the Right Side, 1/34 Multiplexing Duty Ratio)



Note: Pins X100–X116 are left disconnected here.

Figure 19 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/48 Multiplexing Duty Ratio)

4.3 LCD Driving Voltage Setting

There are 6 levels of LCD driving voltages ranging from V1 to V6; V1 is the highest and V6 is the lowest. As shown in figure 20, column output waveform is made up of a combination of V1, V3, V4, and V6 while row output waveform is made up of V1, V2, V5, and V6. This means that V1 and V6 are common to both waveforms while mid-voltages are different.

To accommodate this situation, each block of the HD66108T is provided with power supply pins for mid-voltages as shown in figure 21. Each pair of V1R and V1L and V6R and V6L are internally connected and must be applied the same level of voltage. Block B is fixed for column output and must be applied V3 and V4 as mid-voltages. The other blocks must be applied different levels of voltages according to the function of their LCD driving output pins; if the LCD driving output pins are set for row output, VMHn and VMLn must be applied V2 and V5, respectively, while they must be applied V3 and V4, respectively, if the pins are set for column output (n = 1 to 3).

Table 3 Relationship between FCR Settings and LCD Driving Voltages

Control Register (FCR)			LCD Driving Voltage Pins									
ROS4	**ROS3**	**Mode**	**VIR/VIL**	**V3**	**V4**	**VMH1**	**VML1**	**VMH2**	**VML2**	**VMH3**	**VML3**	**V6R/V6L**
0	0	165-column	V1	V3	V4	V3	V4	V3	V4	V3	V4	V6
0	1	65-row (R)	V1	V3	V4	V3	V4	V2	V5	V2	V5	V6
1	0	65-row (L/R)	V1	V3	V4	V2	V5	V3	V4	V2	V5	V6
1	1	33-row (R)	V1	V3	V4	V3	V4	V3	V4	V2	V5	V6

65-row (R): 65-row-output mode from the right side
65-row (L/R): 65-row-output mode from the left and right sides
33-row (R): 33-row-output mode from the right side

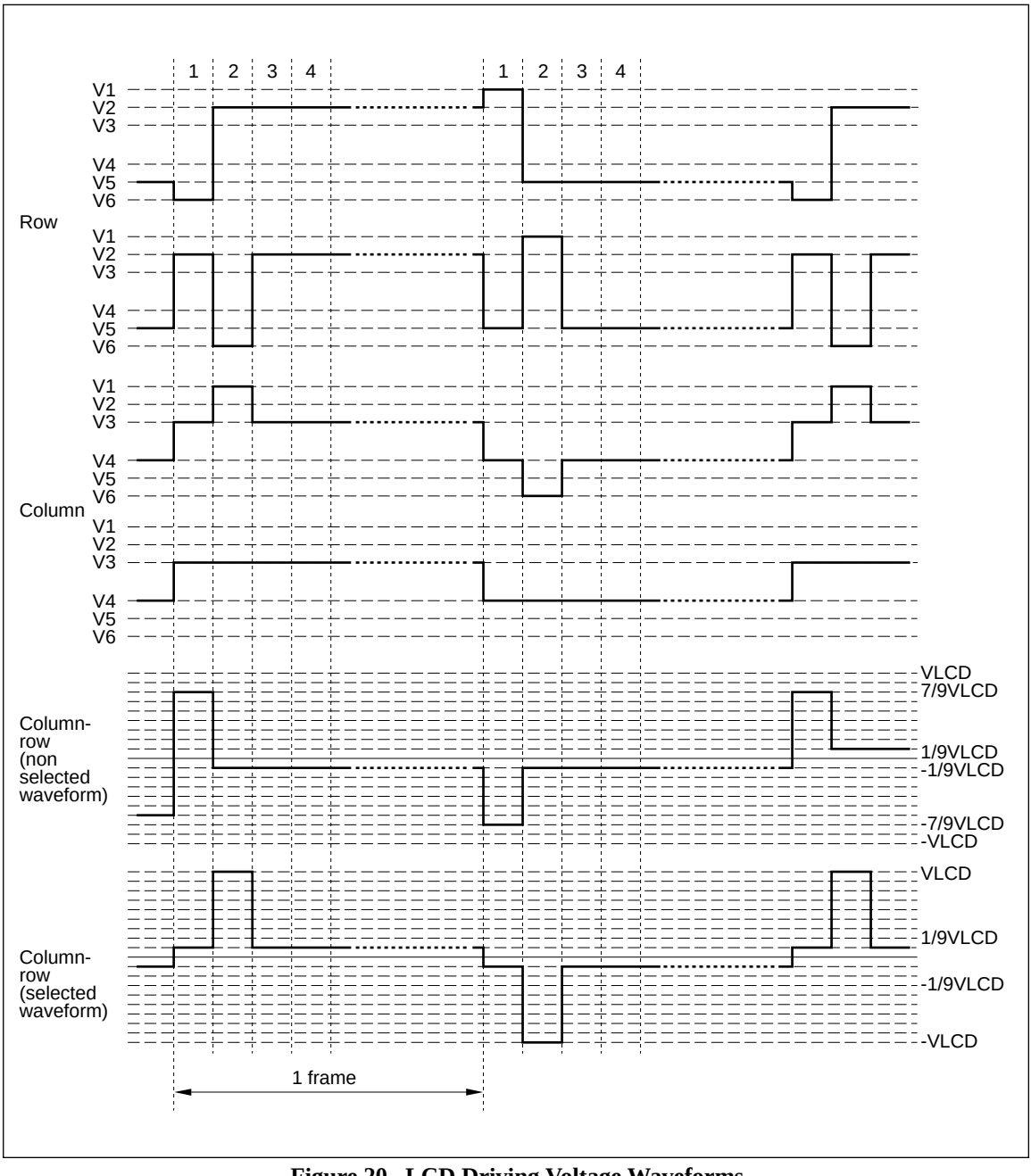


Figure 20 LCD Driving Voltage Waveforms

5. Multiplexing Duty Ratio and LCD Driving Waveform Settings

A multiplexing duty ratio and LCD driving waveform can be selected via internal registers.

A multiplexing duty ratio of 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, or 1/66 can be selected according to the LCD panel used. However, since there are only 65 row-output pins, only 65 lines will be displayed even if 1/66 multiplexing duty ratio is selected.

There are three types of LCD driving waveforms, as shown in figure 22: A-type waveform, B-type waveform, and C-type waveform.

The A-type waveform is called per-half-line inversion. Here, the waveforms of M signal and CL1 signal are the same and alternate every LCD line.

The B-type waveform is called per-frame inversion; in this case, the M signal inverts its polarity every frame so as to alternate every two LCD frames. This is the most common type.

The C-type waveform is called per-n-line inversion and inverts its polarity every n lines (n can be set as needed within 1 to 31 via the internal registers). The C-type waveform combines the advantages of the A-and B-types of waveforms. However, some lines will not be alternated depending on the multiplexing duty ratio and n. To avoid this, another C-type waveform is available which is generated from the EOR of the C-type waveform M signal mentioned above and the B-type waveform M signal. Since the relationship between n and display quality usually depends on the LCD panel, n must be determined by observing actual display results.

The B-type waveform should be used if the LCD panel specifies no particular type of waveform. However, in some cases, the C-type waveform may create a better display.

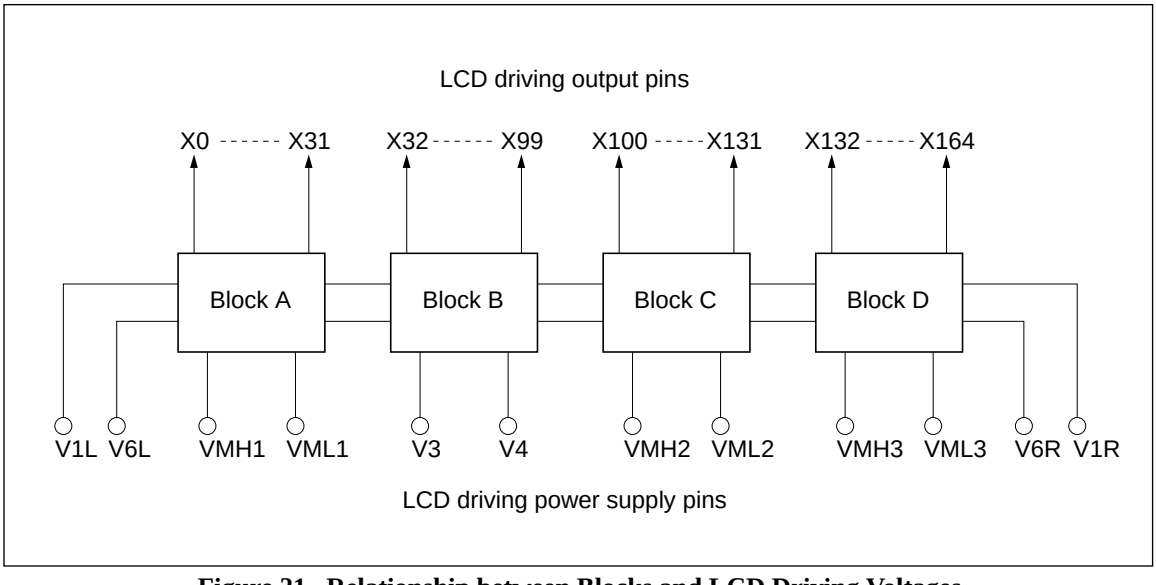


Figure 21 Relationship between Blocks and LCD Driving Voltages

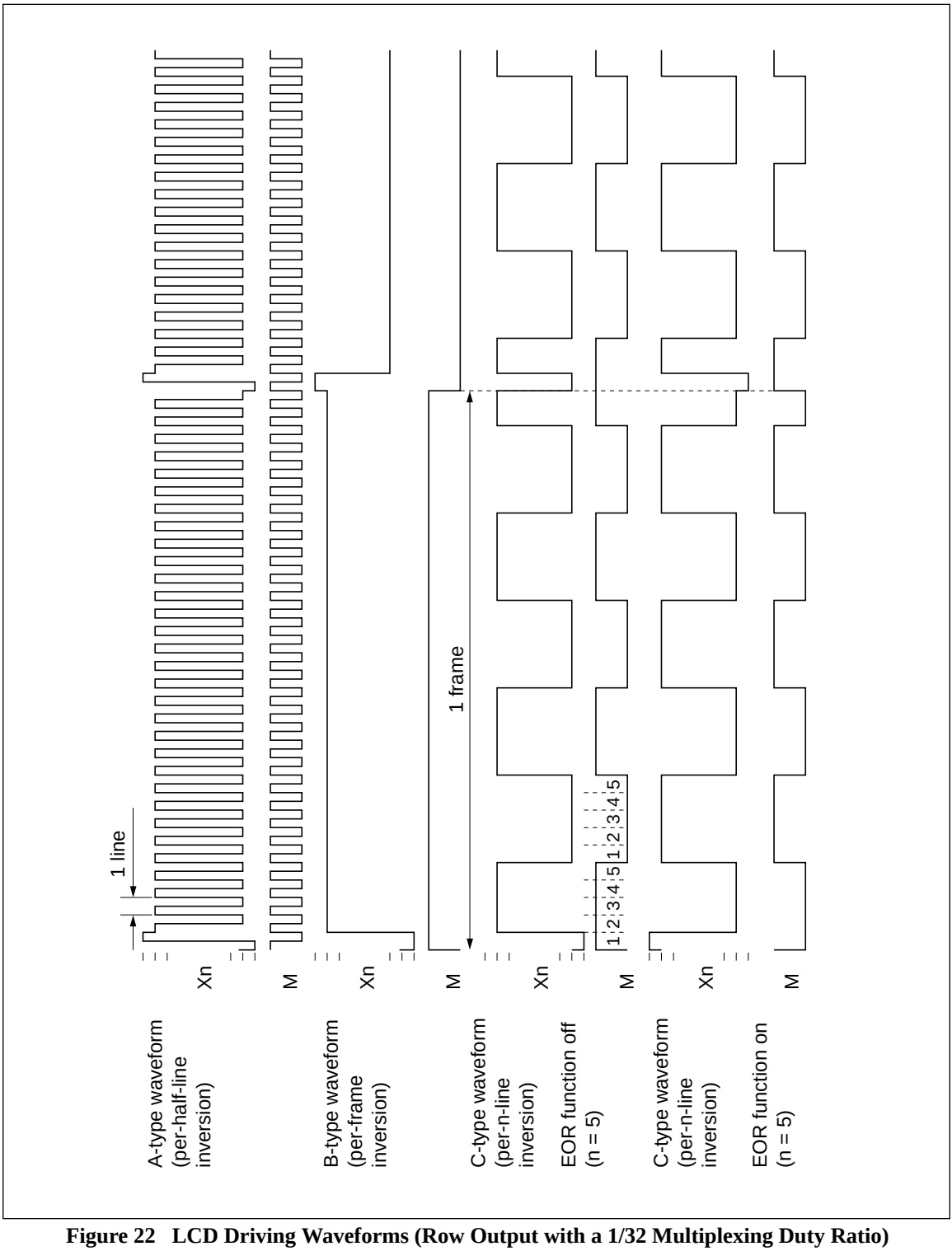


Figure 22 LCD Driving Waveforms (Row Output with a 1/32 Multiplexing Duty Ratio)

6. Clock and Frame Frequency

An input clock with a 200-kHz to 4-MH frequency can be used for the HD66108T. Note that raising clock frequency increases current consumption although it reduces busy time and enables high-speed operations. An optimum system clock frequency should thus be selected within 200 kHz to 4 MHz.

The clock frequency driving the LCD panel (= frame frequency) is usually 70 Hz to 90 Hz. Accordingly, the HD66108T is so designed that the frequency-division ratio of the input clock can be selected. The HD66108T generates around 80-Hz LCD frame frequency if the frequency-division ratio is 1. The frequency-division ratio can be obtained from the following equation.

$$Ni = \frac{f_F}{f_{CLK}} \times \frac{500}{80} \times D1$$

Ni: Frequency-division ratio
f_F: Frame frequency required for the LCD panel (Hz)
f_{CLK}: Input clock frequency (kHz)
D1: Duty correction value 1
D1 = 1 when multiplexing duty ratio is 1/32, 1/48 or 1/64
D1 = 32/34 when multiplexing duty ratio is 1/34
D1 = 32/36 when multiplexing duty ratio is 1/36
D1 = 48/50 when multiplexing duty ratio is 1/50
D1 = 64/66 when multiplexing duty ratio is 1/66

The frequency-division ratio nearest the value obtained from the above equation must be selected; selectable frequency-division ratios by internal registers are 2, 1, 1/2, 1/3, 1/4, 1/6, and 1/8.

7. Display Off Function

The HD66108T has a display off function which turns off display by rewriting the contents of the internal register. This prevents random display at power-on until display memory is initialized.

8. Standby Function

The HD66108T has a standby function providing low-power dissipation. Writing a 1 to bit 6 of the address register starts up the standby function.

The LCD driving voltages, ranking from V1 to V6, must be set to V_{CC} to prevent DC voltage from being applied to an LCD panel during standby state.

The HD66108T operates as follows in standby mode.

(1) Stops oscillation and external clock input
(2) Resets all registers to 0's except the STBY bit

Here, note that the display memory will not preserve data if the standby function is turned on; the display memory as well as registers must be set again after the standby function is terminated.

Table 4 shows the standby status of pins and table 5 shows the status of registers after standby function termination.

Writing a 0 to bit 6 of the address register terminates the standby function. Writing values into the DISP and Register No. bits at this time is ignored; these bits need to be set after the standby function has been completely terminated.

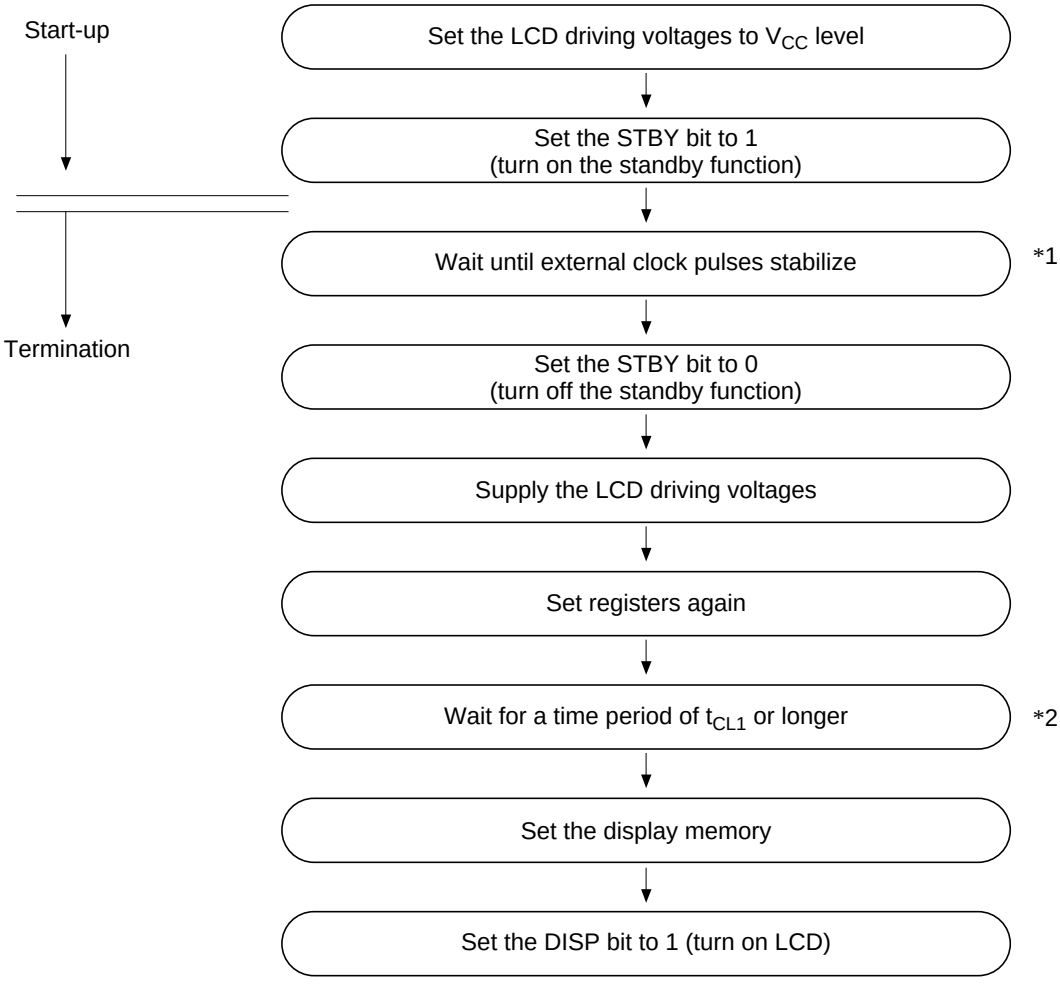
Figure 23 shows the flow for start-up and termination of the standby function and related operations.

Table 4 Standby Status of Pins

Pin	Status
OSC2	High
CO	Low
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn	V4 (column output pins)
Xn’	V5 (row output pins)

Table 5 Register Status after Standby Function Termination

Register Name	Status after Standby Function Termination
Address register	Reset to 0’s except for the STBY bit
X address register	Reset to 0’s
Y address register	Reset to 0’s
Control register	Reset to 0’s
Mode register	Reset to 0’s
C select register	Reset to 0’s
Display memory	Data not preserved



Notes: 1. Not necessary in the case of using internal oscillation.
2. Refer to equation 1 (section 3.1).

Figure 23 Start-Up and Termination of Standby Function and Related Operations

9. Multi-Chip Operation

Using multiple HD66108T chips (= multi-chip operation) provides the means for extending the number of display dots. Note the following items when using the multi-chip operation.

(1) The master chip and the slave chips must be determined; the $\overline{M}$/S pin of the master chip must be set low and the $\overline{M}$/S pin of the slave chips must be set high.

(2) All the HD66108T chips will be slave chips if HD61203 or its equivalent is used as a row driver.

(3) The master chip supplies the FLM, CL1, and M signals to the slave chips via the corresponding pins, which synchronizes the slave chips with the master chip.

(4) Since a master chip outputs synchronization signals, all data registers must be set.

(5) The following bits for slave chips must always be set:

INC, WLS, PON, and ROS (control register)
FFS (mode register)

It is not necessary to set the control register's DUTY bits, the mode register's DWS bits, or the C select register. For other registers' settings, refer to table 6.

(6) All chips must be set to LCD off in order to turn off the display.

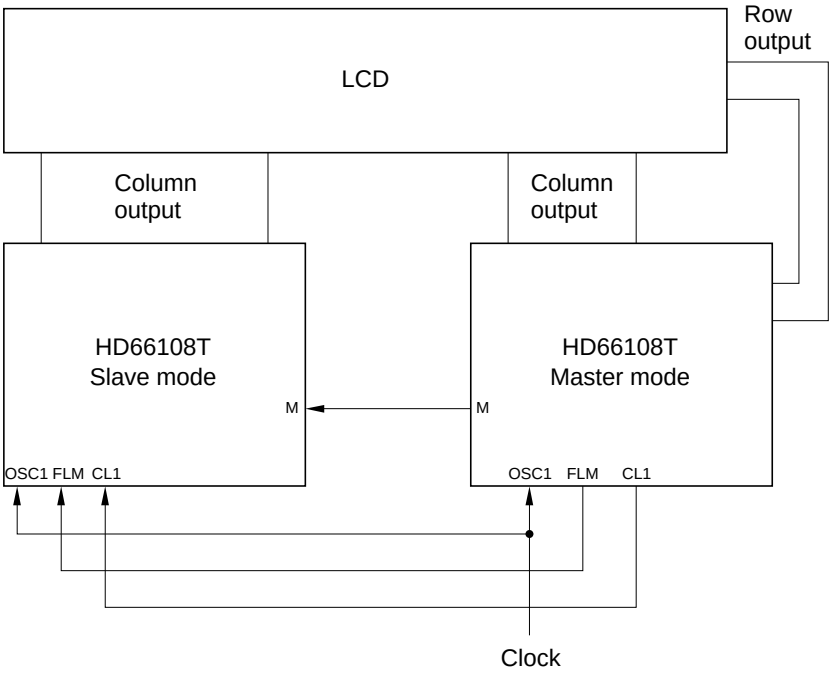
(7) The standby function of slave chips must be started up first while that of the master chip must be terminated first.

Figure 24 to 26 show the connections of the synchronization signals for different system configurations and table 6 lists the differences between master mode and slave mode.

Table 6 Comparison between Master and Slave Mode

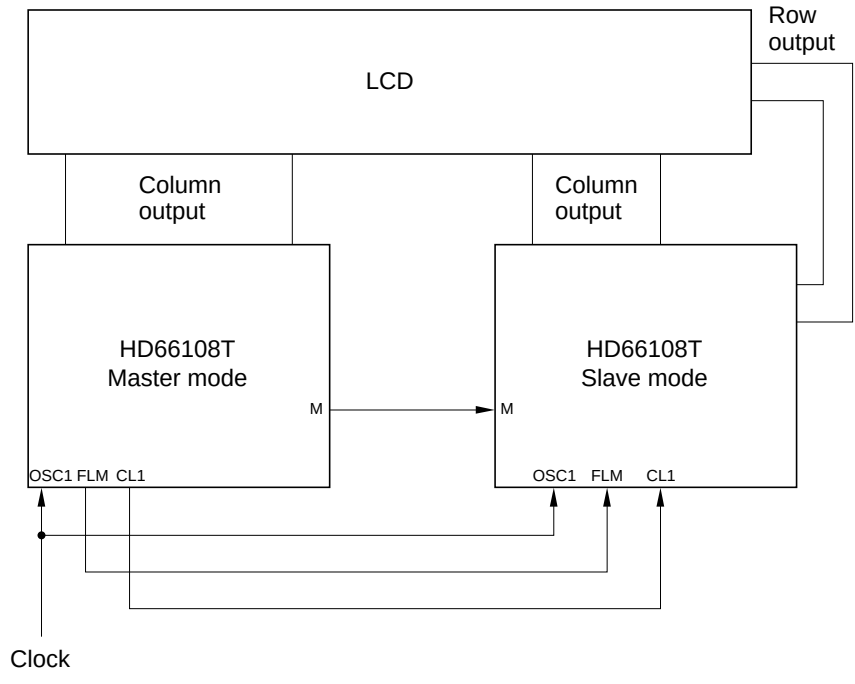
Item		Master Mode	Slave Mode
Pin:	$\overline{M}$/S	Must be set low	Must be set high
	OSC1, OSC2	Oscillation is possible	Oscillation is possible
	CO	= OSC1	= OCS1
	FLM, CL1, M	Output signals	Input signals
Register:	AR	Valid	Valid
	XAR	Valid	Valid
	YAR	Valid	Valid
	FCR	Valid	Valid except for the DUTY bits
	MDR	Valid	Valid except for the DWS bits
	CSR	Valid (only if the DWS bits are set for the C-type waveform)	Invalid

Notes: Valid: Needs to be set
Invalid: Needs not be set



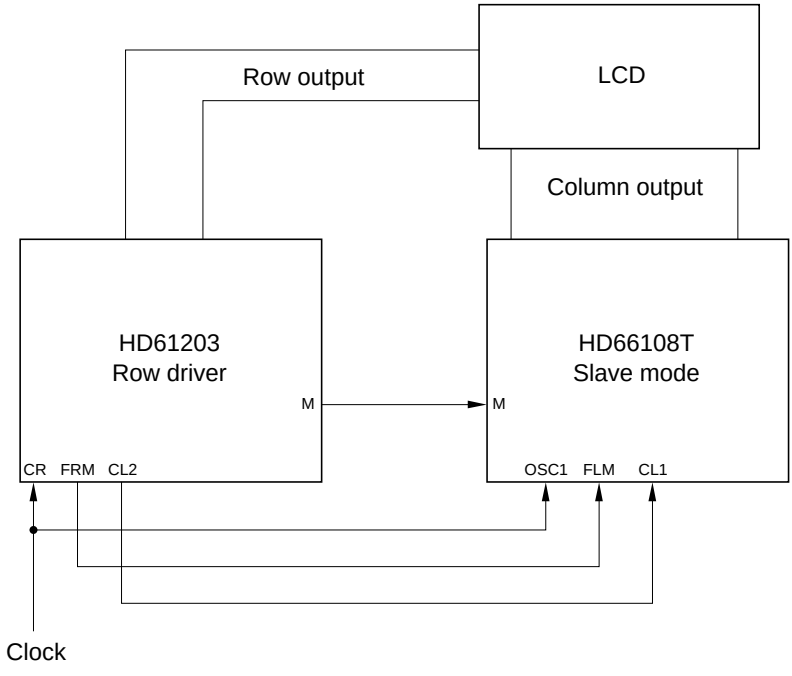
Note: Clock pulses for the slave chip can be supplied from the master chip CO pin.

Figure 24 Configuration Using 2 HD66108T Chips (1)



Note: Clock pulses for the slave chip can be supplied from the master chip CO pin.

Figure 25 Configuration Using 2 HD66108T Chips (2)



Notes: 1. The slave chip can oscillate CR clock pulses. In this case, the clock pulses must be supplied to the HD61203 from the HD66108T's CO pin.
2. The HD61203's control pins must be set in accordance with the type of RAMs.

Figure 26 Configuration Using 1 HD66108T Chip with Another Row Driver (HD61203)

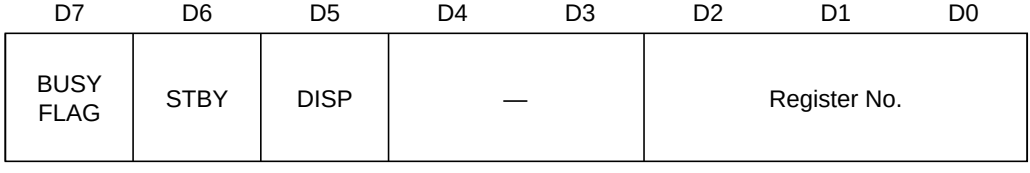
Internal Registers

All HD66108T's registers can be read from and written into. However, the BUSY FLAG and invalid bits cannot be written to and reading invalid bits or registers returns 0's.

1. Address Register (AR) (Accessed with RS = 0)

This register (figure 27) contains Register No. bits, BUSY FLAG bit, STBY bit, and DISP bit. Register No. bits select one of the data registers according to the register number written. The BUSY FLAG bit indicates the internal operation state if read. The STBY bit activates the standby function. The DISP bit turns the display on or off. This register is selected when RS pin is 0.

Bits D4 and D3 are invalid.



(1) STBY
1: Standby function on
0: Normal (standby function off)

Note: When standby function is on, all registers are reset to 0's.

(2) DISP
1: LCD on
0: LCD off

(3) Register No.

	Bit			
No.	**2**	**1**	**0**	**Register**
0	0	0	0	Display memory
1	0	0	1	X address register
2	0	1	0	Y address register
3	0	1	1	Control register
4	1	0	0	Mode register
5	1	0	1	C select register

(4) BUSY FLAG (can be read only)
1: Busy state
0: Ready state

Figure 27 Address Register

2. Display Memory (DRAM) (Accessed with RS = 1, Register Number = $(000)_2$)

Although display memory (figure 28) is not a register, it can be handled as one. 8- or 6-bit data can be selected by the control register WLS bit according to the character font in use. If 6-bit data is selected, D7 and D6 bits are invalid.

3. X Address Register (XAR) (Accessed with RS = 1, Register Number = $(001)_2$)

This register (figure 29) contains 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0). It sets X addresses and confirms X addresses after writing or reading to or from the display memory.

4. Y Address Register (YAR) (Accessed with RS = 1, Register Number = $(010)_2$)

This register (figure 30) contains 1 invalid bit (D7) and 7 valid bits (D6 to D0). It sets Y addresses and confirms Y addresses after writing or reading to or from the display memory.

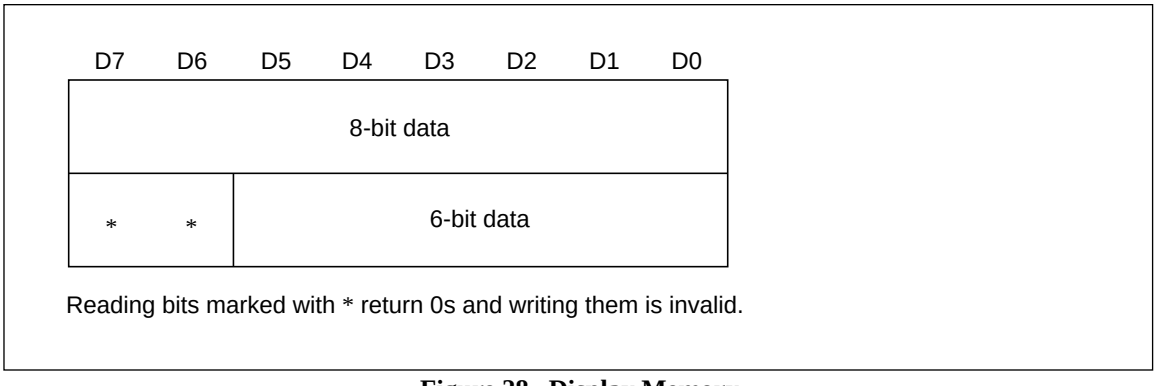


Figure 28 Display Memory

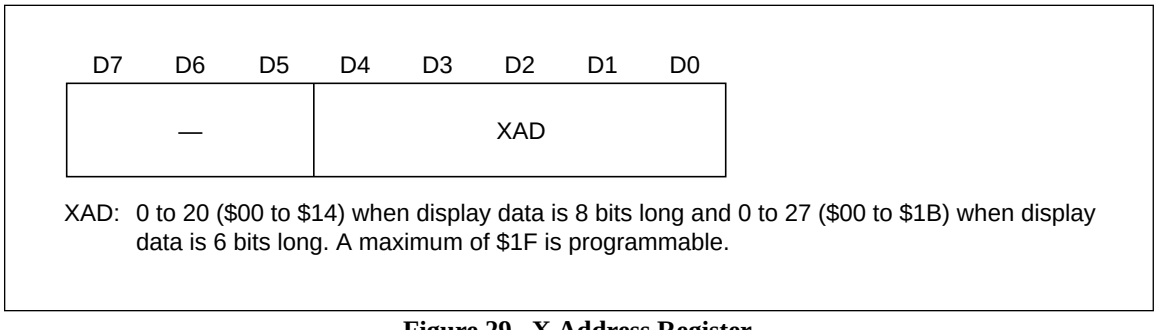


Figure 29 X Address Register

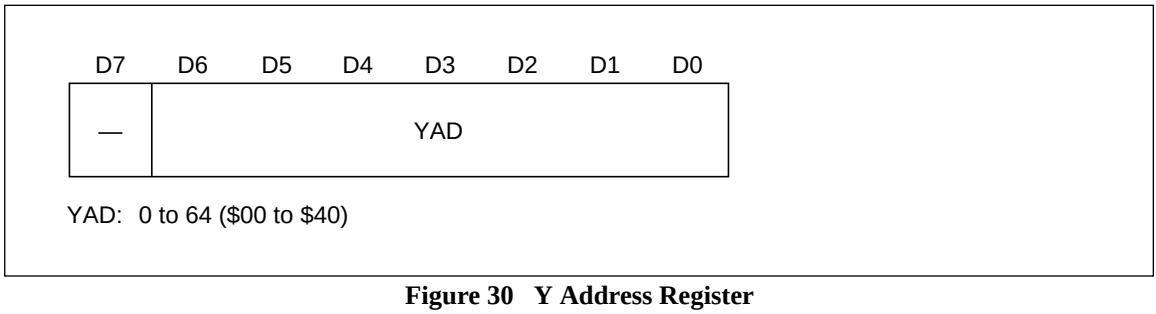
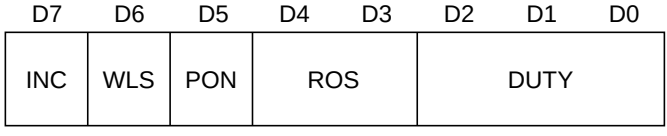


Figure 30 Y Address Register

5. Control Register (FCR) (Accessed with RS = 1, Register Number = $(011)_2$)

This register (figure 31), containing eight bits, has a variety of functions such as specifying the method for accessing RAM, determining RAM valid area, and selecting the function of the LCD driving signal output pins. It must be initialized as soon as possible after power-on since it determines the overall operation of the HD66108T. The PON bit may have to be reset afterwards. If the DUTY bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (section 3.1).



(1) INC (address increment direction select)
1: X address is incremented
0: Y address is incremented

(2) WLS (word length (of display data) select)
1: 6-bit word
0: 8-bit word

(3) PON (row data protect on)
1: Protect function on
0: Protect function off

(4) ROS (row output (function of LCD driving output pins) select)

	Bit		
No.	**4**	**3**	**Contents**
0	0	0	165 column outputs
1	0	1	65 row outputs from the right side
2	1	0	65 row outputs from the left and right sides
3	1	1	33 row outputs from the right side

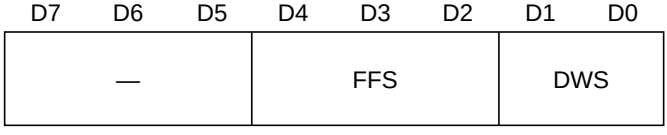
(5) DUTY (multiplexing duty ratio)

	Bit			Multiplexing
No.	**2**	**1**	**0**	**Duty Ratio**
0	0	0	0	1/32
1	0	0	1	1/34
2	0	1	0	1/36
3	0	1	1	1/48
4	1	0	0	1/50
5	1	0	1	1/64
6	1	1	0	1/66
7	1	1	1	Testing mode

Figure 31 Control Register

6. Mode Register (MDR) (Accessed with RS = 1, Register Number = $(100)_2$)

This register (figure 32), containing 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0), selects a system clock and type of LCD driving waveform. It must also be initialized after power-on since it determines overall HD66108T operation like the FCR register. If the FFS bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (section 3.1).



(1) FFS (frame frequency select)

No.	Bit 4	3	2	Frequency-Division Ratio
0	0	0	0	1
1	0	0	1	1/2
2	0	1	0	1/3
3	0	1	1	1/4
4	1	0	0	1/6
5	1	0	1	1/8
6	1	1	0	2
7	1	1	1	—

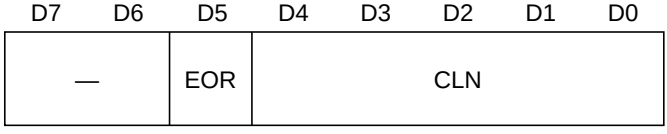
(2) DWS (LCD driving waveform select)

No.	Bit 1	0	Driving Waveform
0	0	0	A-type waveform
1	0	1	B-type waveform
2	1	0	C-type waveform
3	1	1	—

Figure 32 Mode Register

7. C Select Register (CSR) (Accessed with RS = 1, Register Number = $(101)_2$)

This register (figure 33) contains 2 invalid bits (D7 and D6) and 5 valid bits (D5 to D0). It controls C-type waveforms and is activated only when MDR register's DWS bits are set for this type of waveform.



(1) EOR (B-type waveform M signal ⊕ no. of counting lines on/off)
1: EOR function on
0: EOR function off

(2) CLN (No. of counting lines in C-type waveform)
1 to 31 should be set in these bits; 0 must not be set.

Figure 33 C Select Register

Reset Function

The $\overline{\text{RESET}}$ pin starts the HD66108T after power-on. A $\overline{\text{RESET}}$ signal must be input via this pin for at least 20 µs to prevent system failure due to excessive current created after power-on. Figure 34 shows the reset definition.

(1) Reset Status of Pins

Table 7 shows the reset status of output pins. The pins return to normal operation after reset.

Table 7 Reset Status of Pins

Pin	Status
OSC2	Outputs clock pulses or oscillates
CO	Outputs clock pulses
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn	V4 (column output pins)
Xn'	V5 (row output pins)

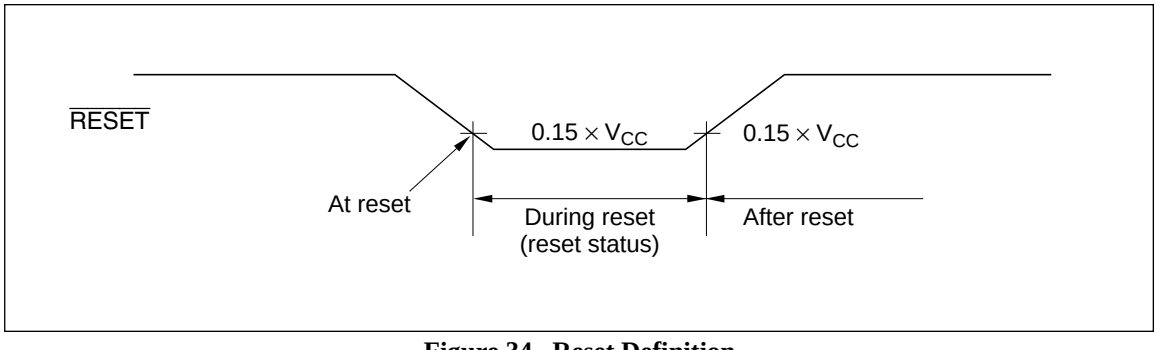


Figure 34 Reset Definition

(2) Reset Status of Registers

The $\overline{\text{RESET}}$ signal has no effect on registers or register bits except for the address register's STBY bit and the X and Y address registers, which are reset to 0's by the signal. Table 8 shows the reset status of registers.

(3) Status after Reset

The display memory does not preserve data which has been written to it before reset; it must be set again after reset.

A $\overline{\text{RESET}}$ signal terminates the standby mode.

Precautionary Notes When Using the HD66108T

(1) Install a 0.1-µF bypass capacitor as close to the LSI as possible to reduce power supply impedance (V_{CC} – GND and V_{CC} – V_{EE}).

(2) Do not leave input pins open since the HD66108T is a CMOS LSI; refer to "Pin Functions" on how to deal with each pin.

(3) When using the internal oscillation clock, attach an oscillation resistor as close to the LSI as possible to reduce coupling capacitance.

(4) Make sure to input the reset signal at power-on so that internal units operate as specified.

(5) Maintain the LCD driving power at V_{CC} during standby state so that DC is not applied to an LCD, in which Xn pins are fixed at V4 or V5 level.

Table 8 Reset Status of Registers

Register	Status
Address register	Pre-reset status with the STBY bit reset to 0
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Pre-reset status
Mode register	Pre-reset status
C select register	Pre-reset status
Display memory	Preserves no pre-reset data

Programming Restrictions

(1) After busy time is terminated, an X or Y address is not incremented until 0.5-clock time has passed. If an X or Y address is read during this time period, non-updated data will be read. (The addresses are incremented even in this case.) In addition, the address increment direction should not be changed during this time since it will cause malfunctions.

(2) Although the maximum output rows is 33 when 33-row-output mode from the right side is specified, any multiplexing duty ratio can be specified. Therefore, row output data sufficient to fill the specified duty must be input in the Y direction. Figure 35 shows how to set row data in the case of 1/34 multiplexing duty ratio. In this case, 0s must be set in Y33 since data for the 34th row (Y33) are not output.

(3) Do not set the C select register's CLN bits to 0 for the M signal of C-type waveform.

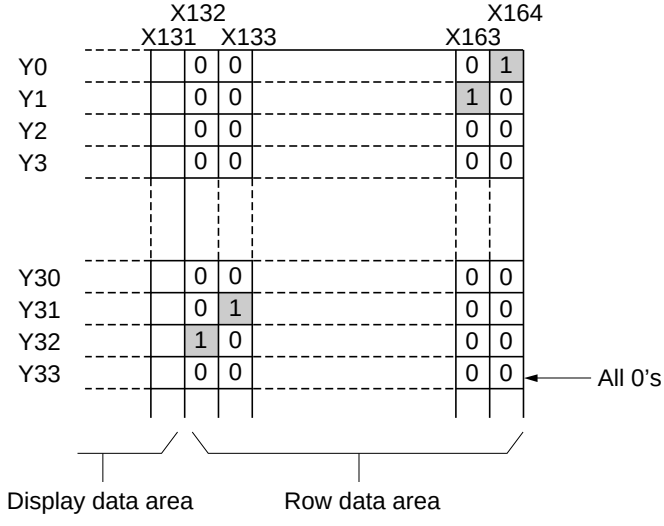


Figure 35 How to Set Row Data for 33-Row Output from the Right Side

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage (1)	$V_{CC}1$ to $V_{CC}3$	–0.3 to +7.0	V
Power supply voltage (2)	$V_{CC} – V_{EE}$	–0.3 to +16.5	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{op}	–20 to +75	°C
Storage temperature	T_{stg}	–20 to +125	°C

Notes: 1. Permanent LSI damage may occur if the maximum ratings are exceeded.
Normal operation should be under recommended operating conditions (V_{CC} = 2.7 to 6.0 V, GND = 0 V, Ta = –20 to +75°C). If these conditions are exceeded, LSI malfunctions could occur.

2. Power supply voltages are referenced to GND = 0 V. Power supply voltage (2) indicates the difference between V_{CC} and V_{EE}.

Electrical Characteristics

DC Characteristics (1) (V_{CC} = 5 V ±20%, GND = 0 V, $V_{CC} - V_{EE}$ = 6.0 to 15 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	OSC1	$V_{IH}1$	$0.8 \times V_{CC}$	—	V_{CC} + 0.3	V		
	$\overline{M}$/S, CL1, FLM, M, TEST1, TEST2	$V_{IH}2$	$0.7 \times V_{CC}$	—	V_{CC} + 0.3	V		
	$\overline{RESET}$	$V_{IH}3$	$0.85 \times V_{CC}$	—	V_{CC} +0.3	V		
	The other inputs	$V_{IH}4$	2.0	—	V_{CC} + 0.3	V	V_{CC} = 5 V ±10%	5
Input low voltage	OSC1	$V_{IL}1$	–0.3	—	$0.2 \times V_{CC}$	V		
	$\overline{M}$/S, CL1, FLM, M, TEST1, TEST2	$V_{IL}2$	–0.3	—	$0.3 \times V_{CC}$	V		
	$\overline{RESET}$	$V_{IL}3$	–0.3	—	$0.15 \times V_{CC}$	V		
	The other inputs	$V_{IL}4$	–0.3	—	0.8	V	V_{CC} = 5 V ±10%	6
Output high voltage	CO, CL1, FLM, M	$V_{OH}1$	$0.9 \times V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	
	DB7–DB0	$V_{OH}2$	2.4	—	—	V	$-I_{OH}$ = 0.2 mA V_{CC} = 5 V ±10%	7
Output low voltage	CO, CL1, FLM, M	$V_{OL}1$	—	—	$0.1 \times V_{CC}$	V	I_{OL} = 0.1 mA	
	DB7–DB0	$V_{OL}2$	—	—	0.4	V	I_{OL} = 1.6 mA V_{CC} = 5 V ±10%	8
Input leakage current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	—	2.5	µA	V_{in} = 0 to V_{CC}	
Tri-state leakage current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	—	10	µA	V_{in} = 0 to V_{CC}	
V pins leakage current	V1, V3, V4, V6, VMHn, VMLn	I_{VL}	–10	—	10	µA	V_{in} = V_{EE} to V_{CC}	
Current consumption	During display	$I_{CC}1$	—	—	400	µA	External clock f_{OSC} = 500 kHz	1
		$I_{CC}2$	—	—	1.0	mA	Internal oscillation Rf = 91 kΩ	1
	During standby	I_{SB}	—	—	10	µA		1, 2

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
ON resistance X0–X164 between Vi and Xj	R_{ON}	—	—	10	kΩ	$\pm I_{LD}$ = 50 µA $V_{CC} - V_{EE}$ = 10 V	3
V pins voltage range	ΔV	—	—	35	%		4
Oscillating frequency	f_{OSC}	315	450	585	kHz	Rf = 91 kΩ	

Notes:
1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity.
2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low. Exposing the LSI to light increases current consumption.
3. I_{LD} indicates the current supplied to one measured pin.
4. $\Delta V = 0.35 \times (V_{CC} - V_{EE})$. For levels V1, V2, and V3, the voltage employed should fall between the V_{CC} and the ΔV and for levels V4, V5, and V6, the voltage employed should fall between the V_{EE} and the ΔV (figure 36).
5. $V_{IH}3$ (min) = $0.7 \times V_{CC}$ when used under conditions other than V_{CC} = 5 V ±10%.
6. $V_{IL}3$ (max) = $0.15 \times V_{CC}$ when used under conditions other than V_{CC} = 5 V ±10%.
7. $V_{OH}2$ (min) = $0.9 \times V_{CC}$ ($-I_{OH}$ = 0.1 mA) when used under conditions other than V_{CC} = 5 V ±10%.
8. $V_{OL}2$ (max) = $0.1 \times V_{CC}$ (I_{OL} = 0.1 mA) when used under conditions other than V_{CC} = 5 V ±10%.

DC Characteristics (2) (V_{CC} = 2.7 to 4.0 V, GND = 0 V, $V_{CC} - V_{EE}$ = 6.0 to 15 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	$\overline{\text{RESET}}$	$V_{IH}1$	$0.85 \times V_{CC}$	—	V_{CC} + 0.3	V		
	The other inputs	$V_{IH}2$	$0.7 \times V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	$\overline{M}$/S, OSC1, CL1, FLM, TEST1, TEST2, M	$V_{IL}1$	–0.3	—	$0.3 \times V_{CC}$	V		
	The other inputs	$V_{IL}2$	–0.3	—	$0.15 \times V_{CC}$	V		
Output high voltage		$V_{OL}1$	$0.9 \times V_{CC}$	—	—	V	$-I_{OH}$ = 50 µA	
Output low voltage		$V_{OL}1$	—	—	$0.1 \times V_{CC}$	V	I_{OL} = 50 µA	
Input leakage current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	—	2.5	µA	V_{in} = 0 to V_{CC}	
Tri-state leakage current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	—	10	µA	V_{in} = 0 to V_{CC}	
V pins leakage current	V1, V3, V4, V6, VMHn, VMLn	I_{VL}	–10	—	10	µA	V_{in} = V_{EE} to V_{CC}	
Current consumption	During display	$I_{CC}1$	—	—	260	µA	External clock f_{OSC} = 500 kHz	1
		$I_{CC}2$	—	—	700	µA	Internal oscillation Rf = 75 kΩ	1
	During standby state	I_{SB}	—	—	10	µA		1, 2
ON resistance between Vi and Xj	X0–X164	R_{ON}	—	—	10	kΩ	$\pm I_{LD}$ = 50 µA $V_{CC} - V_{EE}$ = 10 V	3
V pins voltage range		ΔV	—	—	35	%		4
Oscillating frequency		f_{OSC}	315	450	585	kHz	Rf = 75 kΩ	

Notes: 1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity. Exposing the LSI to light increases current consumption.

2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low.

3. I_{LD} indicates the current supplied to one measured pin.

4. $\Delta V = 0.35 \times (V_{CC} - V_{EE})$. For levels V1, V2, and V3, the voltage employed should fall between the V_{CC} and the ΔV and for levels V4, V5, and V6, the voltage employed should fall between the V_{EE} and the ΔV (figure 36).

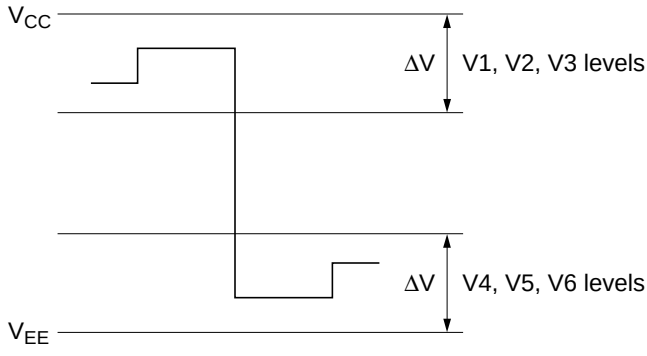


Figure 36 Driver Output Waveform and Voltage Levels

AC Characteristics (1) (V_{CC} = 4.5 to 6.0 V, GND = 0 V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (Figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ high-level pulse width	t_{WRH}	190	—	ns	
$\overline{RD}$ low-level pulse width	t_{WRL}	190	—	ns	
$\overline{WR}$ high-level pulse width	t_{WWH}	190	—	ns	
$\overline{WR}$ low-level pulse width	t_{WWL}	190	—	ns	
$\overline{WR}$–$\overline{RD}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns	
Write data setup time	t_{DSW}	100	—	ns	
Write data hold time	t_{DHW}	0	—	ns	
Read data output delay time	t_{DDR}	—	150	ns	Note
Read data hold time	t_{DHR}	20	—	ns	Note
External clock cycle time	t_{CYC}	0.25	5.0	µs	
External clock high-level pulse width	t_{WCH}	0.1	—	µs	
External clock low-level pulse width	t_{WCL}	0.1	—	µs	
External clock rise and fall time	tr, tf	—	20	ns	

Note: Measured by test circuit 1 (figure 39).

2. LCD Interface Timing (Figure 38)

Item			Symbol	Min	Max	Unit	Notes
$\overline{M}$/S = 0	CL1	High-level pulse width	$t_{WCH}1$	35	—	µs	1, 4
	CL1	Low-level pulse width	$t_{WCL}1$	35	—	µs	1, 4
	FLM	Delay time	$t_{DFL}1$	–2.0	+2.0	µs	4
	FLM	Hold time	$t_{HFL}1$	–2.0	+2.0	µs	4
	M output delay time		$t_{DMO}1$	–2.0	+2.0	µs	4
$\overline{M}$/S = 1	CL1	High-level pulse width	$t_{WCH}2$	35	—	µs	4
	CL1	Low-level pulse width	$t_{WCL}2$	$11 \times t_{CYC}$	—	µs	2, 4
	FLM	Delay time	$t_{DFL}2$	–2.0	$1.5 \times t_{CYC}$	µs	3, 4
	FLM	Hold time	$t_{HFL}2$	–2.0	+2.0	µs	4
	M delay time		t_{DMI}	–2.0	+2.0	µs	4

Notes: 1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6 V) or 75 kΩ (V_{CC} = 2.0 to 4.0 V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is $19 \times t_{CYC}$ in other cases.
3. When bits FFS are set for 1 or 2. The value is $8.5 \times t_{CYC}$ in other cases.
4. Measured by test circuit 2 (figure 39).

AC Characteristics (2) (V_{CC} = 2.7 to 4.5 V, GND = 0 V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (Figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ high-level pulse width	t_{WRH}	1.0	—	µs	
$\overline{RD}$ low-level pulse width	t_{WRL}	1.0	—	µs	
$\overline{WR}$ high-level pulse width	t_{WWH}	1.0	—	µs	
$\overline{WR}$ low-level pulse width	t_{WWL}	1.0	—	µs	
$\overline{WR}$–$\overline{RD}$ high-level pulse width	t_{WWRH}	1.0	—	µs	
$\overline{CS}$, RS setup time	t_{AS}	0.5	—	µs	
$\overline{CS}$, RS hold time	t_{AH}	0.1	—	µs	
Write data setup time	t_{DSW}	1.0	—	µs	
Write data hold time	t_{DHW}	0	—	µs	
Read data output delay time	t_{DDR}	—	0.5	µs	Note
Read data hold time	t_{DHR}	20	—	ns	Note
External clock cycle time	t_{CYC}	1.6	5.0	µs	
External clock high-level pulse width	t_{WCH}	0.7	—	µs	
External clock low-level pulse width	t_{WCL}	0.7	—	µs	
External clock rise and fall time	tr, tf	—	0.1	µs	

Note: Measured by test circuit 2 (figure 39).

2. LCD Interface Timing (Figure 38)

Item			Symbol	Min	Max	Unit	Notes
$\overline{M}$/S = 0	CL1	High-level pulse width	$t_{WCH}1$	35	—	µs	1, 4
	CL1	Low-level pulse width	$t_{WCL}1$	35	—	µs	1, 4
	FLM	Delay time	$t_{DFL}1$	–2.0	+2.0	µs	4
	FLM	Hold time	$t_{HFL}1$	–2.0	+2.0	µs	4
	M output delay time		$t_{DMO}1$	–2.0	+2.0	µs	4
$\overline{M}$/S = 1	CL1	High-level pulse width	$t_{WCH}2$	35	—	µs	4
	CL1	Low-level pulse width	$t_{WCL}2$	$11 \times t_{CYC}$	—	µs	2, 4
	FLM	Delay time	$t_{DFL}2$	–2.0	$1.5 \times t_{CYC}$	µs	3, 4
	FLM	Hold time	$t_{HFL}2$	–2.0	+2.0	µs	4
	M delay time		t_{DMI}	–2.0	+2.0	µs	4

Notes: 1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6 V) or 75 kΩ (V_{CC} = 2.7 to 4.0 V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is $19 \times t_{CYC}$ in other cases.
3. When bits FFS are set for 1 or 2. The value is $8.5 \times t_{CYC}$ in other cases.
4. Measured by test circuit 2 (figure 39).

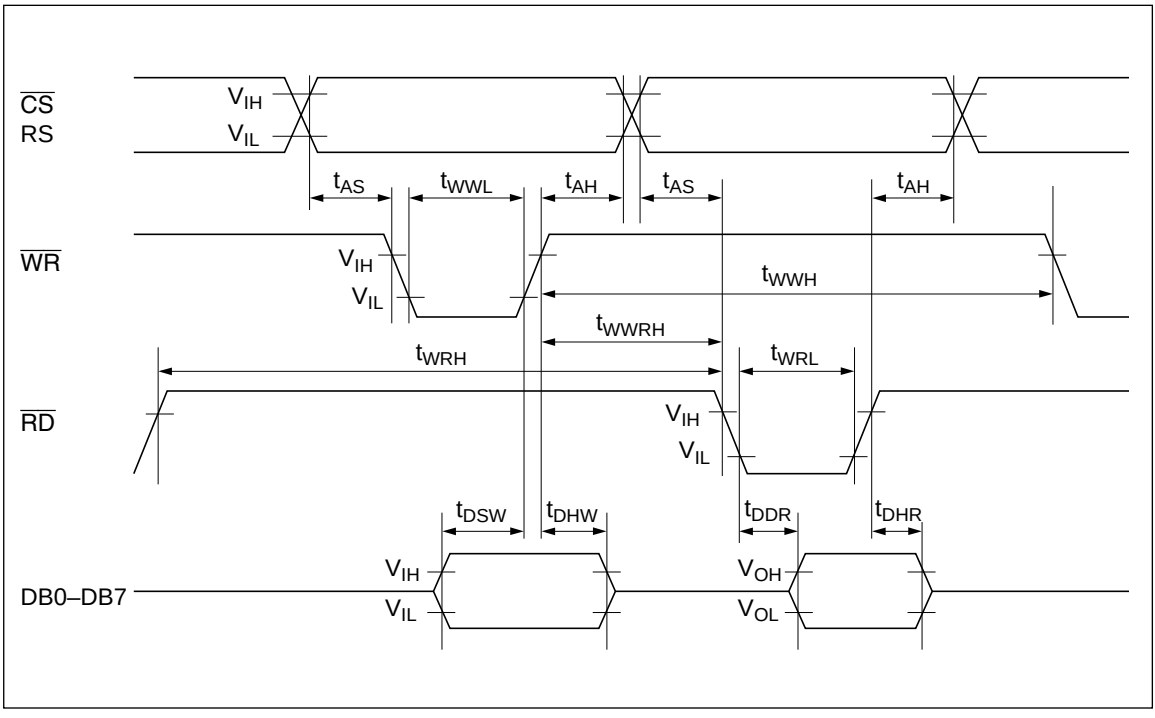


Figure 37 CPU Bus Timing

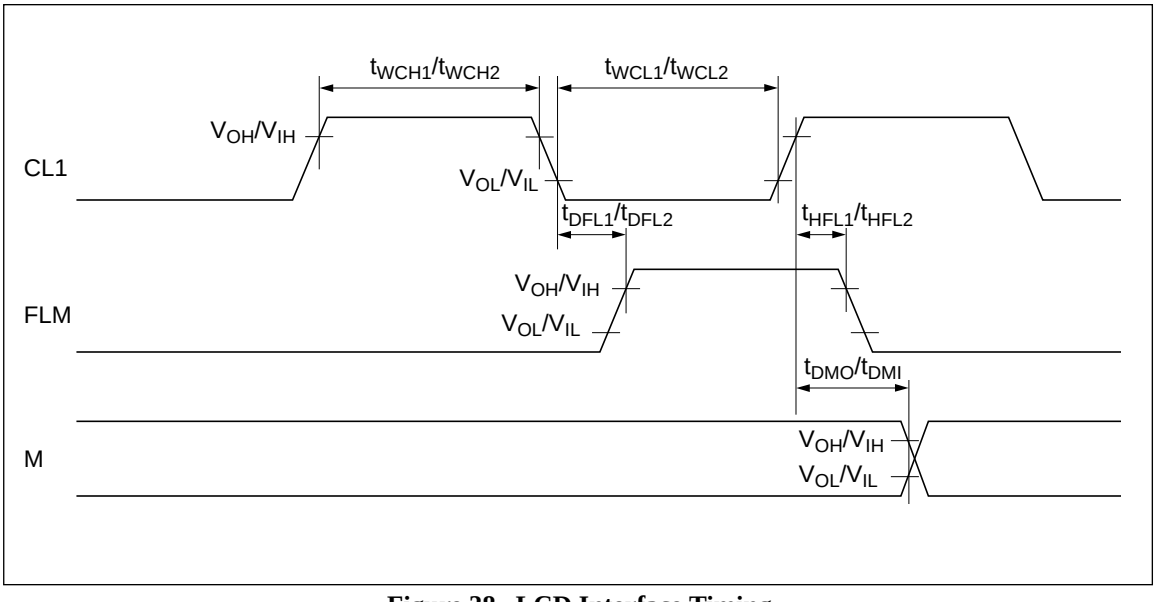
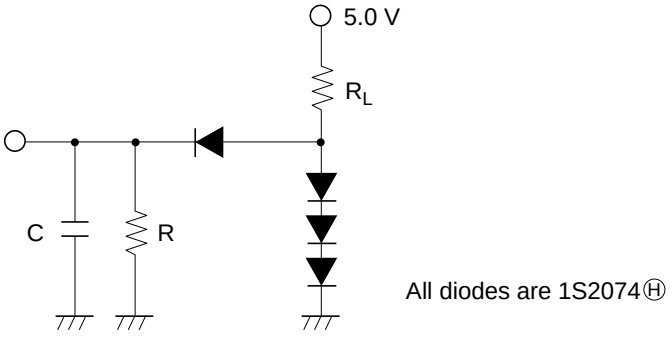
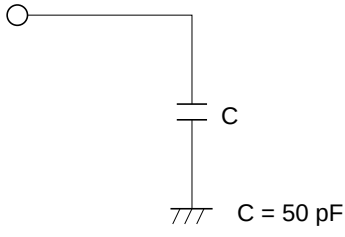


Figure 38 LCD Interface Timing



R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF

Test Circuit 1

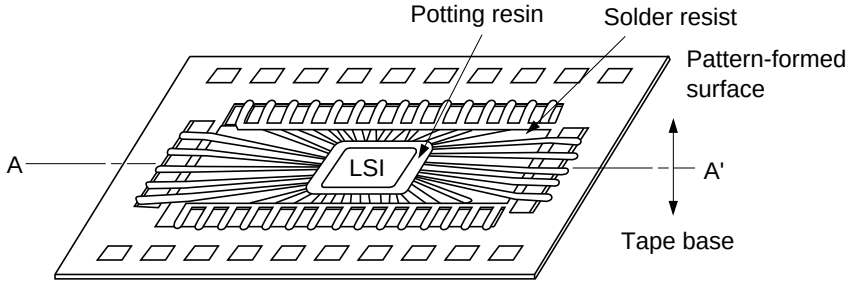


Test Circuit 2

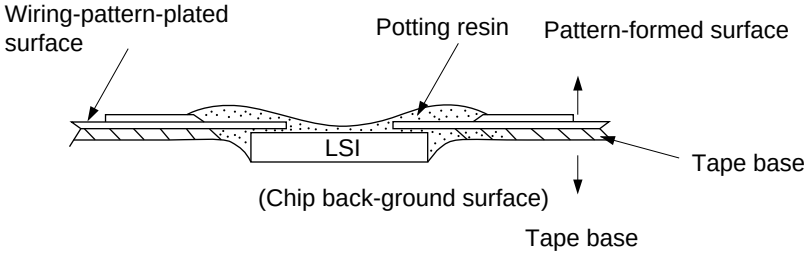
Figure 39 Load Circuits

TCP Sketches and Mounting

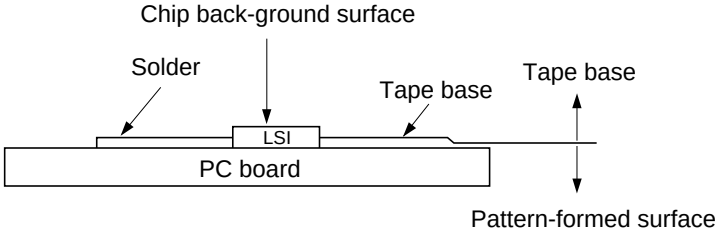
The following shows TCP sketches and TCP mounting on a printed circuit board. These drawings do not restrict TCP shape.



TCP Rough Sketch



A-A' Cross-Sectional View



TCP Mounting on PC Board

HD66520T

(160-Channel 4-Level Grayscale Display Column Driver with Internal Bit-Map RAM)

Preliminary

HITACHI

Description

The HD66520 is a column driver for liquid crystal dot-matrix graphic display systems. This LSI incorporates 160 liquid crystal drive circuits and a 160 × 240 × 2-bit bit-map RAM, which is suitable for LCDs in portable information devices. It also includes a general-purpose SRAM interface so that draw access can be easily implemented from a general-purpose CPU. The HD66520 also has a new arbitration method which prevents flicker when the CPU performs draw access asynchronously. The on-chip display RAM greatly decreases power consumption compared to previous liquid crystal display systems because there is no need for high-speed data transfer. The chip also incorporates a four-level grayscale controller for enhanced graphics capabilities, such as icons on a screen.

Features

- Duty cycle: 1/64 to 1/240
- Liquid crystal drive circuits: 160
- Low-voltage logic circuit: 3.0 to 3.6-V operation power supply voltage
- High-voltage liquid crystal drive circuit: 8 to 28-V liquid crystal drive voltage
- Grayscale display: FRC four-level grayscale display
- Grayscale memory management: Packed pixel
- Internal bit-map display RAM: 76800 bits (160 × 240 lines × two planes)
- CPU interface
  - — SRAM interface
  - — Address bus: 16 bits, data bus: 8 bits
- High-speed draw function: Supports burst transfer mode
- Arbitration function: Implemented internally (draw access has priority)
- Access time
  - — 180 ns (write access)
  - — 300 ns (read access)
- Low power consumption:
  V_{CC} = 3.3-V operation
  - — 270 µA during display (logic circuit, liquid crystal drive circuit)
  - — 7 mA during RAM access (logic circuit)
- On-chip address management function
- Refresh unnecessary
- Internal display off function
- Package: 208-pin TCP

Hitachi semiconductor

Pin Description

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Function
Power supply	$V_{CC}1$ $V_{CC}2$		V_{CC} V_{CC}	— —		V_{CC}–GND: logic power supply
	GND1 GND2		GND GND	— —		
	$V_{EE}1$ $V_{EE}2$		LCD drive circuit power supply	— —		V_{CC}–V_{EE}: LCD drive circuit power supply
	V1L, V1R		LCD select high-level voltage	Input	2	LCD drive level power supplies See figure 1. The user should apply the same potential to the L and R side.
	V2L, V2R		LCD select low-level voltage	Input	2	
	V3L, V3R		LCD deselect high-level voltage	Input	2	
	V4L, V4R		LCD de-select low-level voltage	Input	2	
Control signals	LS0, LS1		LSI ID select switch pin 0 and 1	Input	2	Pins for setting LSI ID no (refer to **Pin Functions** for details).
	SHL		Shift direction control signal	Input	1	Reverses the relationship between LCD drive output pins Y and addresses.
	FLM		First line marker	Input	1	First line select signal.
	CL1		Data transfer clock	Input	1	Clock signal to transfer the line data to an LCD display driver block.
	M		AC switching signal	Input	1	Switching signal to convert LCD drive output to AC.
	$\overline{\text{DISPOFF}}$		Display off signal	Input	1	Control signal to fix LCD driver outputs to LCD select high level. When low, LCD drive outputs Y1 to Y160 are set to V1, or LCD select high level. Display can be turned off by setting a common driver to V1.

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Function
Bus inter-face	A0 to A15		Address input	Input	16	Upper 9 bits (A15–A7) are used for the duty-directional addresses, and lower 7 bits (A6–A0) for the output-pin directional addresses (refer to **Pin Functions** for details).
	DB0 to DB7		Data input/ output	I/O	8	Packed-pixel 2-bit/pixel display data transfer (refer to **Pin Functions** for details).
	$\overline{CS}$		Chip select signal	Input	1	LSI select signal during draw access (refer to **Pin Functions** for details).
	$\overline{WE}$		Write signal	Input	1	Write-enable signal during draw access (refer to **Pin Functions** for details).
	$\overline{OE}$		Output enable signal	Input	1	Output-enable signal during draw access (refer to **Pin Functions** for details).
LCD drive output	Y1 to Y160		LCD drive output	Output	160	Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on the combination of the M signal and data levels.

Note: The number of input outer leads: 48

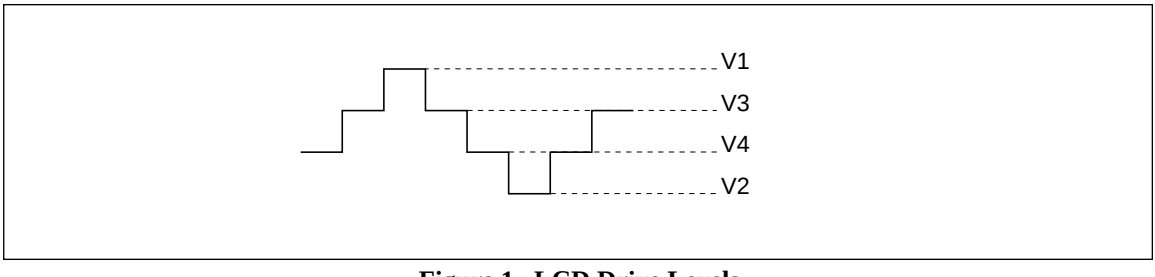


Figure 1 LCD Drive Levels

Pin Functions

Control Signals

LS0 and LS1 (Input): The LS pins can assign four (0 to 3) ID numbers to four LSIs, thus making it possible to connect a maximum of four HD66520s sharing the same $\overline{CS}$ pin to the same bus (figure 2.)

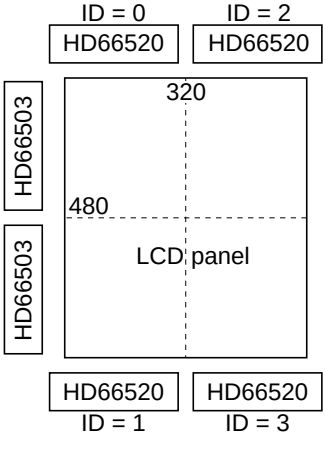
SHL (Input): This pin reverses the relationship between LCD drive output pins Y1 to Y160 and addresses. There is no need to change the address assignment for the display regardless of whether the HD66520 is mounted from the back or the front of the LCD panel. Refer to Driver Layout and Address Management for details.

FLM (Input): When the pin is high, it resets the display line counter, returns the display line to the start line, and synchronizes common signals with frame timing.

CL1 (Input): At each falling edge of data-transfer clock pulses input to this pin, the latch circuits latch display data and output it to the liquid crystal display driver section.

M (Input): AC voltage needs to be applied to liquid crystals to prevent deterioration due to DC voltage application. The M pin is a switch signal for liquid crystal drive voltage and determines the AC cycle.

$\overline{DISPOFF}$ (Input): A control signal to fix liquid crystal driver output to liquid crystal select high level. When this pin is low, liquid crystal drive outputs Y1 to Y160 are set to liquid crystal select high level V1. The display can be turned off by setting the outputs of the common driver to level V1. In this case, display RAM data will be retained. Therefore, if signal $\overline{DISPOFF}$ returns to high level, liquid crystal drive outputs will return to normal display state. Draw access can be executed when signal $\overline{DISPOFF}$ is either in high or low state.



LS1	LS0	ID No.	RAM Address Arrangement
L	L	0	Upper-left of LCD panel
L	H	1	Lower-left of LCD panel
H	L	2	Upper-right of LCD panel
H	H	3	Lower-right of LCD panel

L: Low level
H: High level

Figure 2 LS Pins and Address Assignment

Power Supply Pins

V_{CC}1–2 and GND1–2: These pins supply power to the logic circuit.

V_{CC}1–2 and V_{EE}1–2: These pins supply power to the liquid crystal circuits.

V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R: These pins are used to input the level power supply to drive the liquid crystal.

Bus Interface

$\overline{CS}$ (Input): A basic signal of the RAM area. When $\overline{CS}$ is low (active), the system can access the on-chip RAM of the LSI whose address space, set by LS0, LS1, and SHL pins, contains the input address. When $\overline{CS}$ is high, the RAM is in standby.

In addition, this signal is used for arbitration control when draw access from the CPU competes with display access that is used to transfer line data to the liquid crystal panel. Note that there are restraints for the pulse width, as shown in figure 3. The example shown here is when V_{CC} = 3 V for a write operation.

A0 to A15 (Input): A bus to transfer addresses during RAM access. Upper nine bits (A15 to A7) are duty-direction addresses, and lower seven bits (A6 to A0) are output pin-direction addresses.

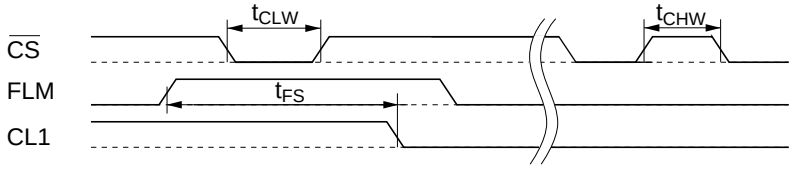
$\overline{WE}$ (Input): Signal $\overline{WE}$ is in active state during low level and standby state during high level and is used to write display data to the RAM. Only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address can be written to when $\overline{CS}$ is low.

$\overline{OE}$ (Input): Signal $\overline{OE}$ is in active state during low level and standby state during high level and is used to read display data from the RAM. Only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address can be read from when $\overline{CS}$ is low.

DB0 to DB7 (Input/Output): The pins function as data input/output pins. They can accommodate to a data format with 2 bits/pixel, which implement packed-pixel four-level grayscale display.

$180 \le t_{CHW}$ (ns)
$180 \le t_{CLW} \le t_{FS} - 1000$ (ns)

t_{CHW}: $\overline{CS}$ high-level width
t_{CLW}: $\overline{CS}$ low-level width



Note: Refer to restraints for details on pulse-width restraints.

Figure 3 $\overline{CS}$ (Input)

Block Diagram

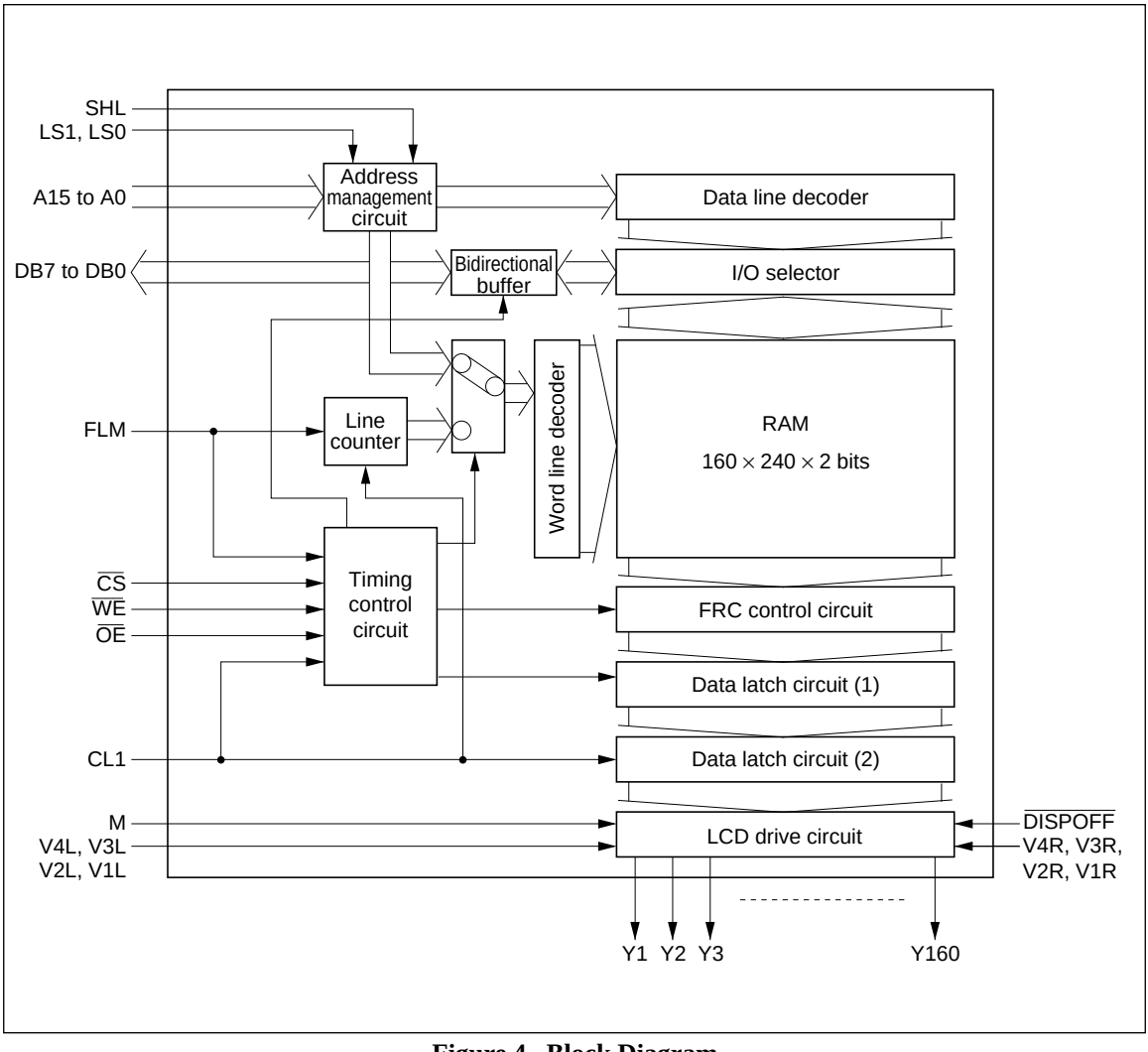


Figure 4 Block Diagram

Address Management Circuit: Converts the addresses input via A15–A0 from the system to the addresses for a memory map of the on-chip RAM. When several LSIs (HD66520s) are used, only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address, accepts the access from the system, and enables the inside. The address management circuit enables configuration of the LCD display system with memory addresses not affected by the connection direction, and reduces burdens of software and hardware in the system. Refer to the How to Use the LS1 and LS0 Pins to set pins LS0, LS1, and SHL.

Timing Control Circuit: This circuit controls arbitration between display access and draw access. Specifically, it controls access timing while receiving signals FLM, CL1, $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ as input. FLM and CL1 are used to perform refresh (display access), that is, to transfer line data to the liquid crystal circuit. $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ are used for the CPU to perform draw operation (draw access), that is, to read and write display data from and to the internal RAM. This circuit also generates a timing signal for the FRC control circuit to implement four-level grayscale display.

Line Counter: Operates refresh functions. When FLM is high, the counter clears the count value and generates an address to select the first line in the RAM section. The counter increments its value whenever CL1 is valid and generates an address to select subsequent lines in the RAM section.

Bidirectional Buffer: Controls the transfer direction of the display data according to signals from pins $\overline{WE}$ and $\overline{OE}$ in draw operation from the system.

Word Line Decoder: Decodes duty addresses (A15 to A7) and selects one of 240 lines in the display RAM section, and activates one-line memory cells in the display RAM section.

Data Line Decoder: Decodes pin addresses (A6 to A0) and selects a data line in the display RAM section for the 7-bit memory cells in one-line memory cells activated by the word line decoder.

I/O Selector: Reads and writes 8-bit display data for the memory cells in the RAM section.

Display RAM: 160 × 240 × 2-bit memory cell array. Since the memory is static, display data can be held without refresh operation during power supply.

FRC Circuit: Implements FRC (frame rate control) function for four-level grayscale display. For details, refer to **Half Tone Display.**

Data Latch Circuit (1): Latches 160-pixel grayscale display data processed by the FRC control circuit after being read from the display RAM section by refresh operation. This circuit is needed to arbitrate between display access for performing liquid crystal display and draw access from the CPU.

Data Latch Circuit (2): This circuit again outputs the data in data latch circuit (1) synchronously with signal CL1.

LCD Drive Circuit: Selects one of LCD select/deselect power levels V4R to V1R and V4L to V1L according to the grayscale display data, AC signal M, and display-off signal $\overline{DISPOFF}$. The circuit is configured with 160 circuits each generating LCD voltage to turn on/off the display.

Configuration of Display Data Bit

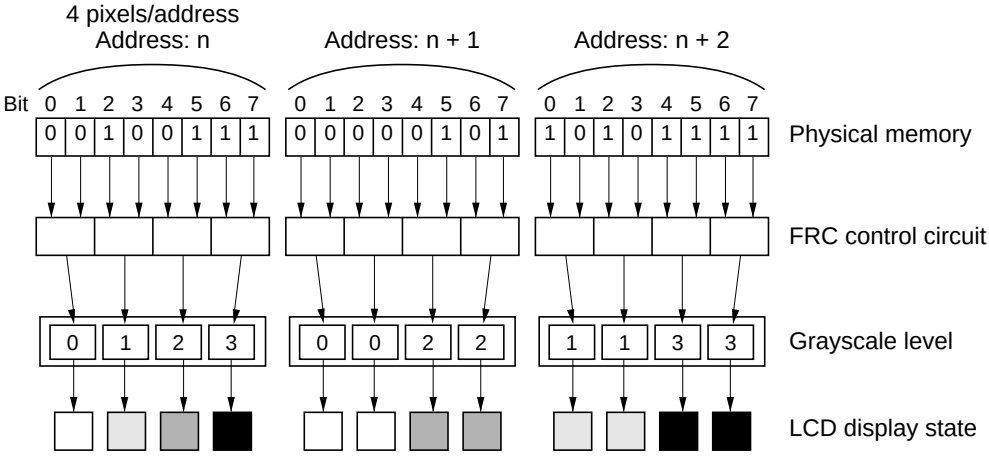
Packed Pixel Method

For grayscale display, multiple bits are needed for one pixel. In the HD66520, two bits are assigned to one pixel, enabling a four-level grayscale display.

One address (eight bits) specifies four pixels, and pixel bits 0 and 1 are managed as consecutive bits.

When grayscale display data is manipulated in bit units, one memory access is sufficient, which enables smooth high-speed data rewriting.

The bit data to input to pin DB7, DB5, DB3, and DB1 becomes MSB and the bit data to input via pin DB6, DB4, DB2, and DB0 is LSB.



Note: Black is shown when the LCD select high-level power supply V1 (M = 1) and LCD select low-level power V2 (M = 0) are selected. White is shown when the LCD non-select high-level power supply V3 (M = 1) and LCD non-select low-level power supply V4 (M = 0) are selected.

Figure 5 Packed Pixel System

Half Tone Display (FRC: Frame Rate Control Function)

The HD66520 incorporates an FRC function to display four-level grayscale half tone.

The FRC function utilizes liquid crystal characteristics whose brightness is changed by an effective value of applied voltage. Different voltages are applied to each frame and half brightness is expressed in addition to display on/off.

Since the HD66520 has two-bit grayscale data per one pixel, it can display four-level grayscale and improve user interface (figure 6). Figure 7 shows the relationships between voltage patterns applied to each frame, the effective voltage value, and brightness obtained.

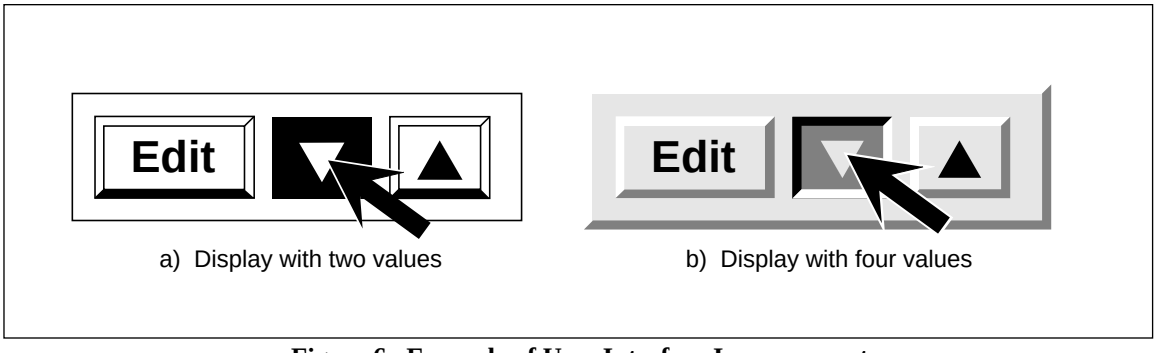
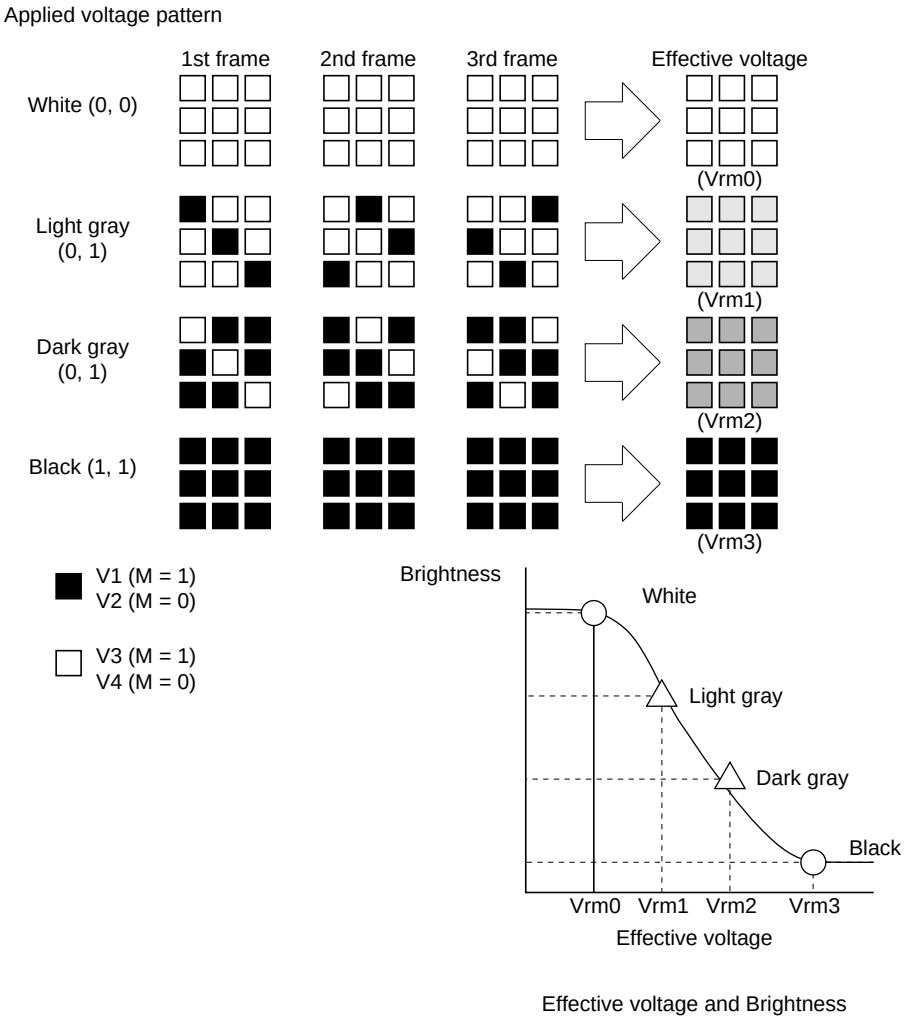


Figure 6 Example of User Interface Improvement



Effective voltage and Brightness

Note: Black is shown when the LCD select high-level power supply V1 (M = 1) and LCD select low-level power V2 (M = 0) are selected. White is shown when the LCD non-select high-level power supply V3 (M = 1) and LCD non-select low-level power supply V4 (M = 0) are selected.

Figure 7 Effective Voltage Values vs. Brightness

Address Management

The HD66520 has an address management function that corresponds to three display sizes all of which are standard sizes for portable information devices: a 160-dot-wide by 240-dot-long display (small information devices); a 320-dot-wide by 240-dot-long display (quarter VGA size); and a 320-dot-wide by 480-dot-long display (half VGA size). Up to four HD66520s can be connected to at a time to configure easily liquid crystal displays with the resolutions mentioned above.

Driver Layout and Address Management

The Y lines on a liquid crystal panel and memory data in a driver are inverted horizontally depending on the connection side of the liquid crystal panel and the driver. When several drivers are connected, address management is needed for each driver. Although reinverted bit-map plotting or address management by the $\overline{CS}$ pin in each driver are possible by using special write addressing, the load on the software is significantly increased. To avoid this, the HD66520 provides memory addresses independent of connection side, but responds to the setting of pins LS0, LS1, and SHL.

How to Use the LS1 and LS0 Pins

Pins LS1 and LS0 set the LSI position (up to four) as shown in figure 8 by assigning ID numbers 0 to 3 to each HD66520.

LS1	LS0	ID No.	Address Arrangement
L	L	0	Upper-left side
L	H	1	Lower-left side
H	L	2	Upper-right side
H	H	3	Lower-right side

L: Low level
H: High level

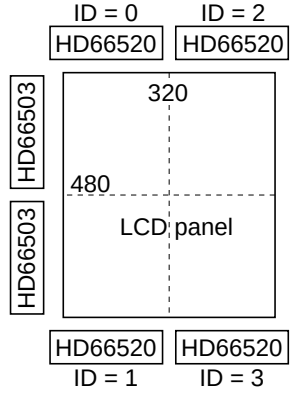


Figure 8 LS0 and LS1 Pin Setting and Internal Memory Map

How to Use the SHL Pin

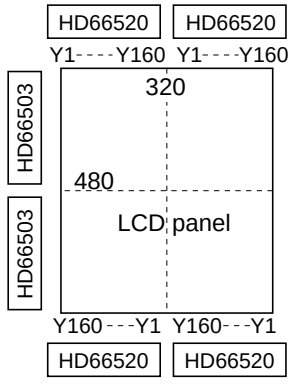
It is possible to invert the relationship between the addresses and output pins Y1 to Y160 by setting the SHL pin (figure 9). The upper left section on the screen can be assigned to address H'0000 regardless of which side of the LCD panel the HD66520 is connected to.

The Relationship between the Data Bus and Output Pins

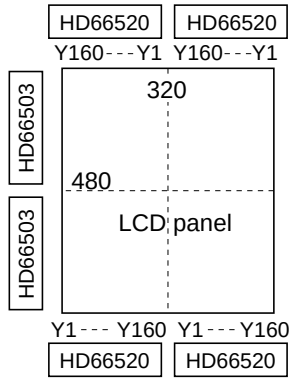
The 8-bit data on the data bus has a 2-bit/pixel configuration for a 4-level grayscale display. In addition, the 8-bit data on the data bus has a relationship as shown in table regardless of the relationship between pins LS0, LS1, and SHL.

Table 1 Data Bus and Output Pins

Data Bus	Output Pins				
DB 0.1	Y1	Y5	· · · · · · · · ·	Y153	Y157
DB 2.3	Y2	Y6	· · · · · · · · ·	Y154	Y158
DB 4.5	Y3	Y7	· · · · · · · · ·	Y155	Y159
DB 6.7	Y4	Y8	· · · · · · · · ·	Y156	Y160



When the HD66520 is connected to the back of the panel (SHL = Low).



When the HD66520 is connected to the front of the panel (SHL = High).

Figure 9 Address Assignment and SHL Pin Setting

Since the relationship between data bus pins DB0 to DB7 and the output pins are fixed, connect the data from the CPU to data bus pins DB0 to DB7 according to the driver arrangement on the panel as shown in figure 10.

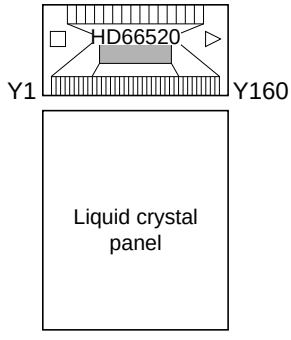
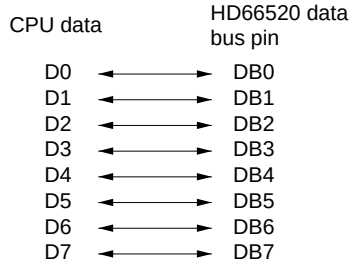
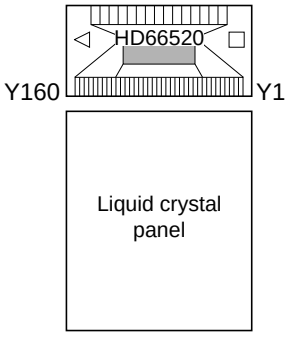
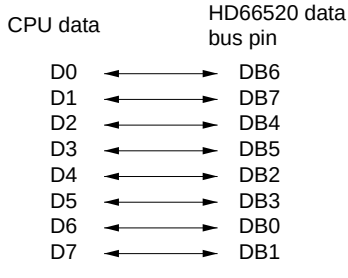
Drive Arrangement	Data Bus Connection
When Y1 is placed on the left side of the liquid crystal panel 	
When Y160 is placed on the left side of the liquid crystal panel 	

Figure 10 Relationship between Data Bus Pins DB0 to DB7 and Output Pins

Application Example

The HD66520 is suitable for a 160-dot-wide by 240-dot-long display (small information devices); a 320-dot-wide by 240-dot-long display (quarter VGA size); and a 320-dot-wide by 480-dot-long display (half VGA size). All of these are standard sizes for portable information devices. The following shows the system configuration.

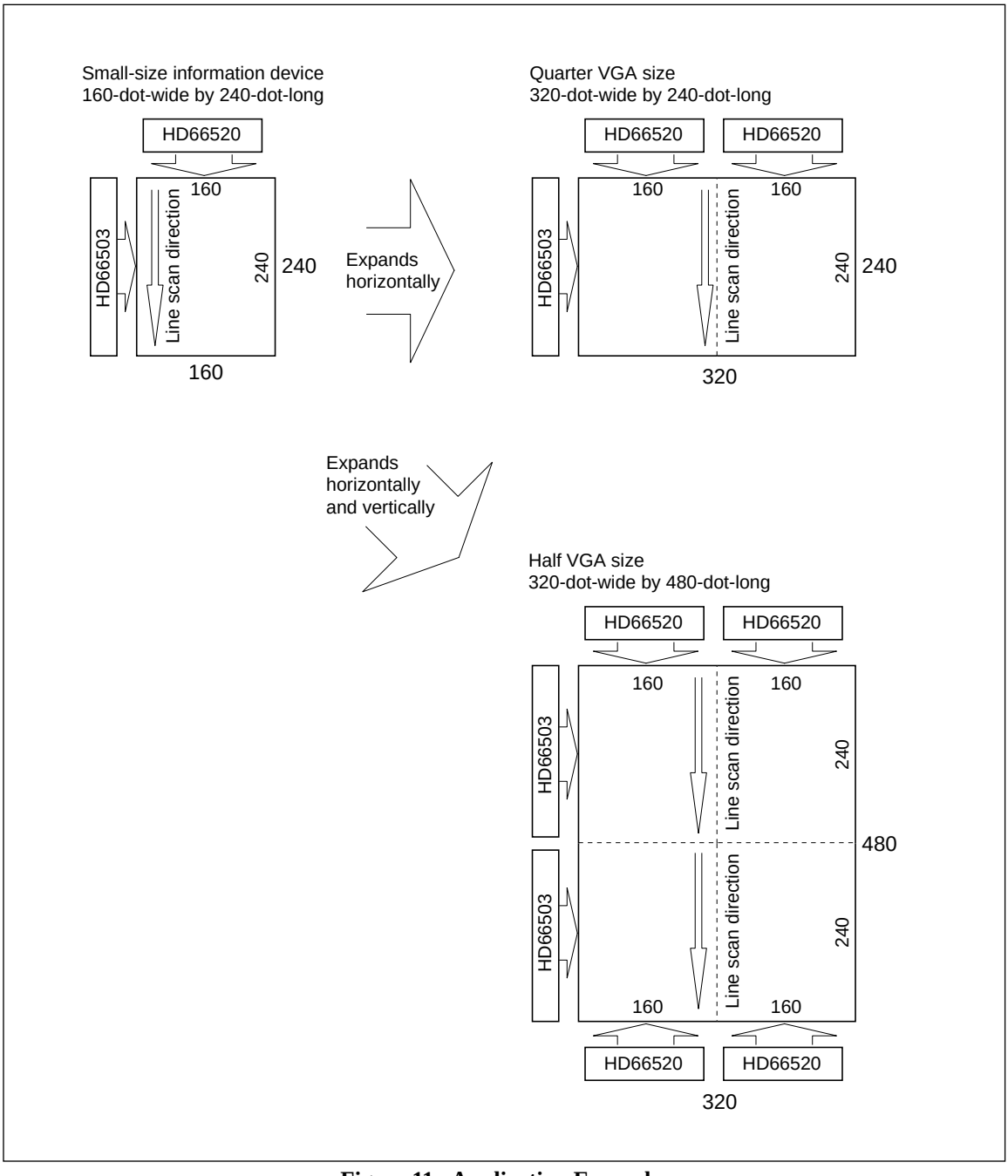


Figure 11 Application Examples

Small Information Device (SHL = Low)

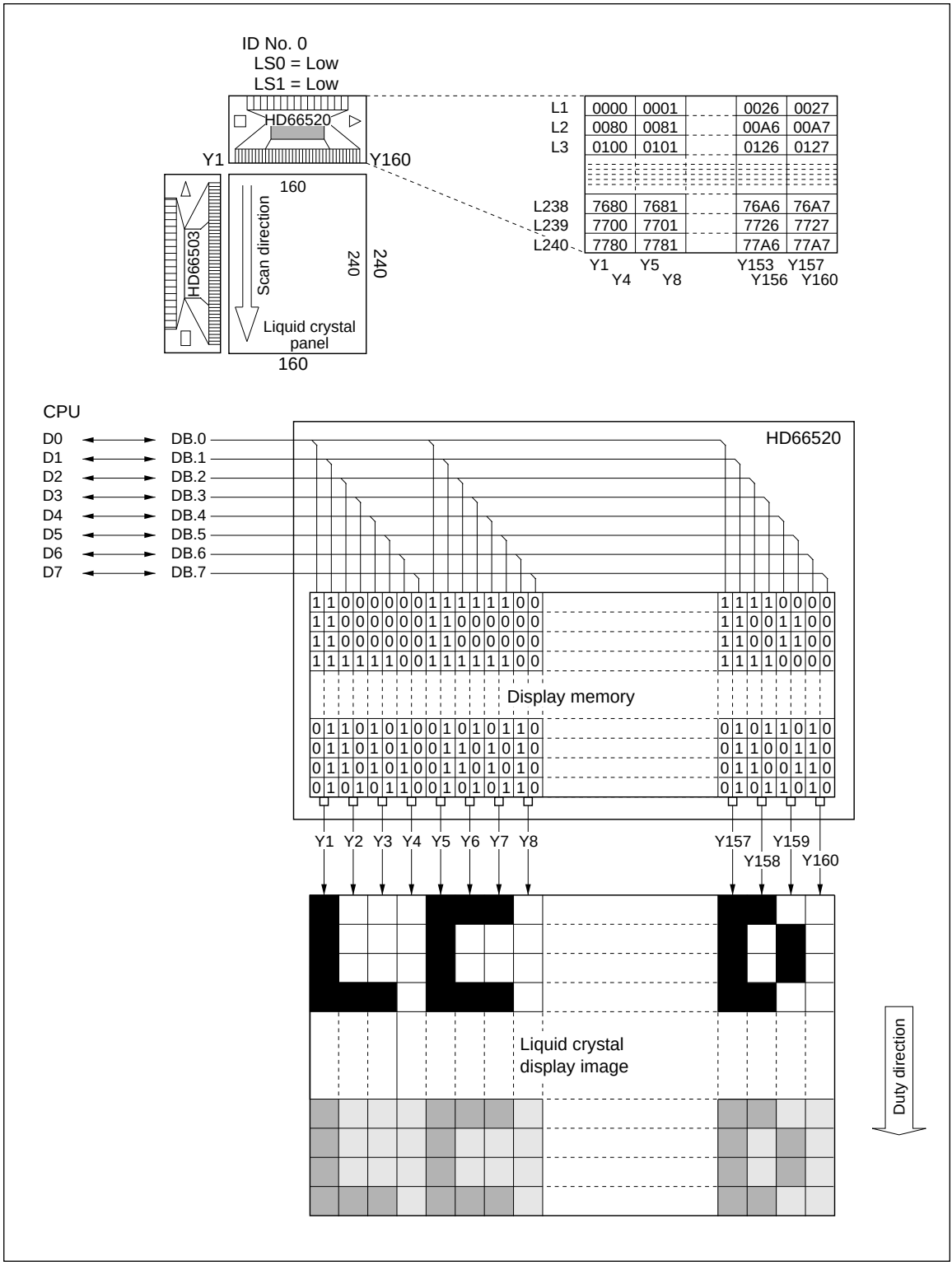


Figure 12 Small Information Device (1)

Small Information Device (SHL = High)

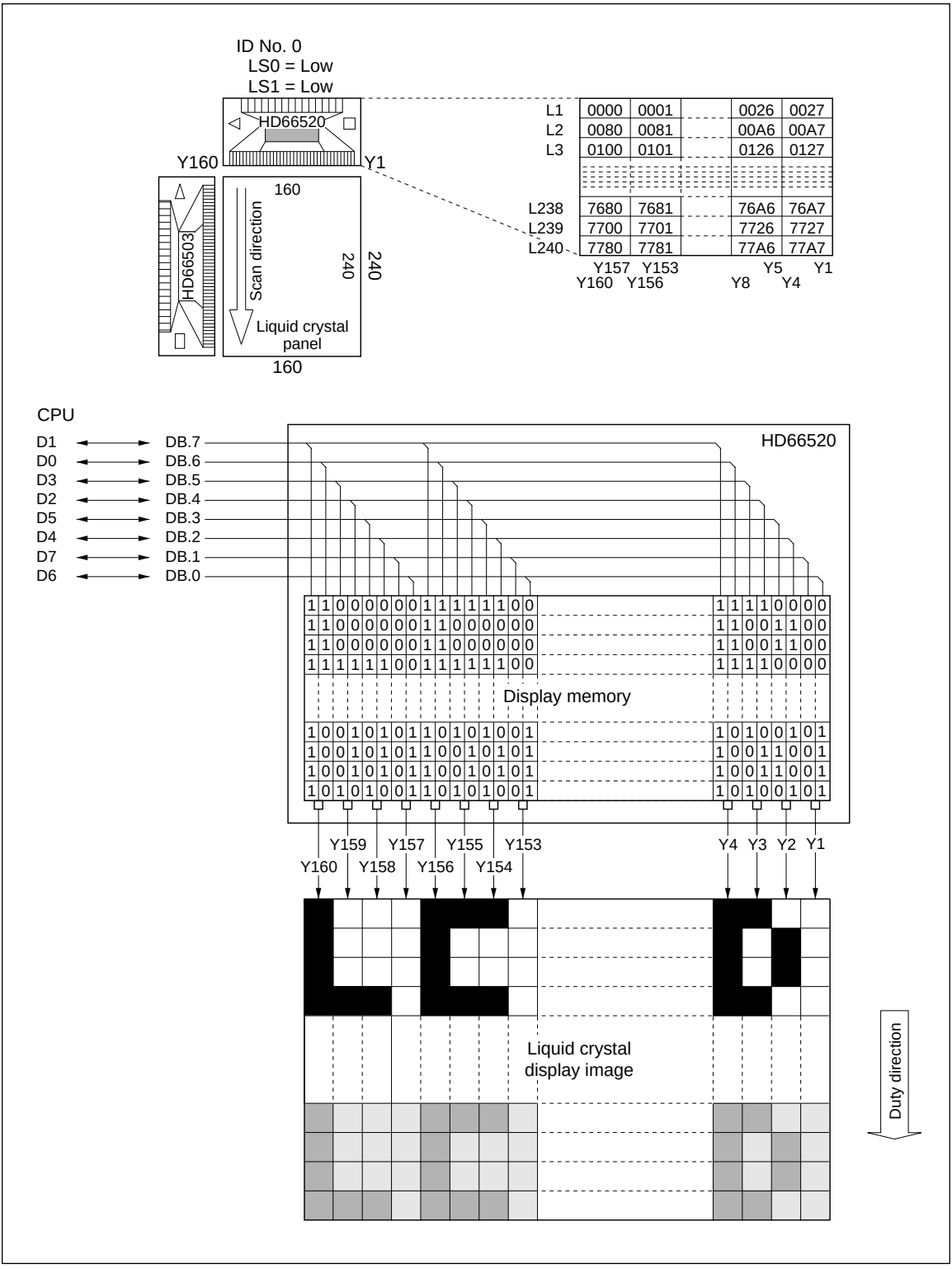


Figure 13 Small Information Device (2)

Quarter VGA Size (SHL = Low)

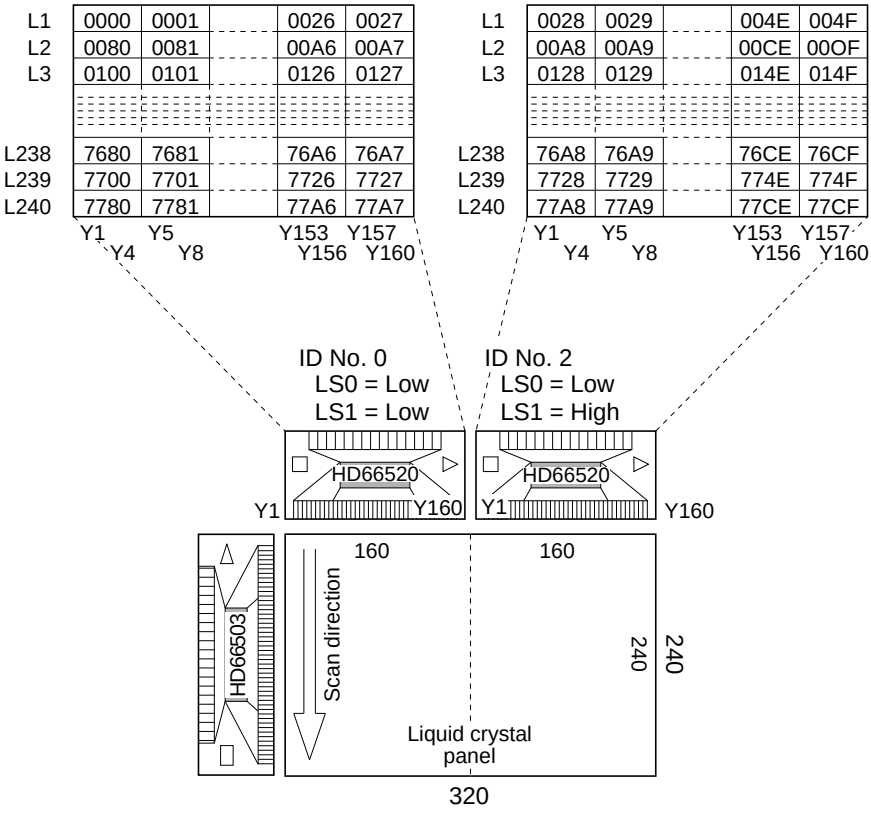


Figure 14 Quarter VGA Size (1)

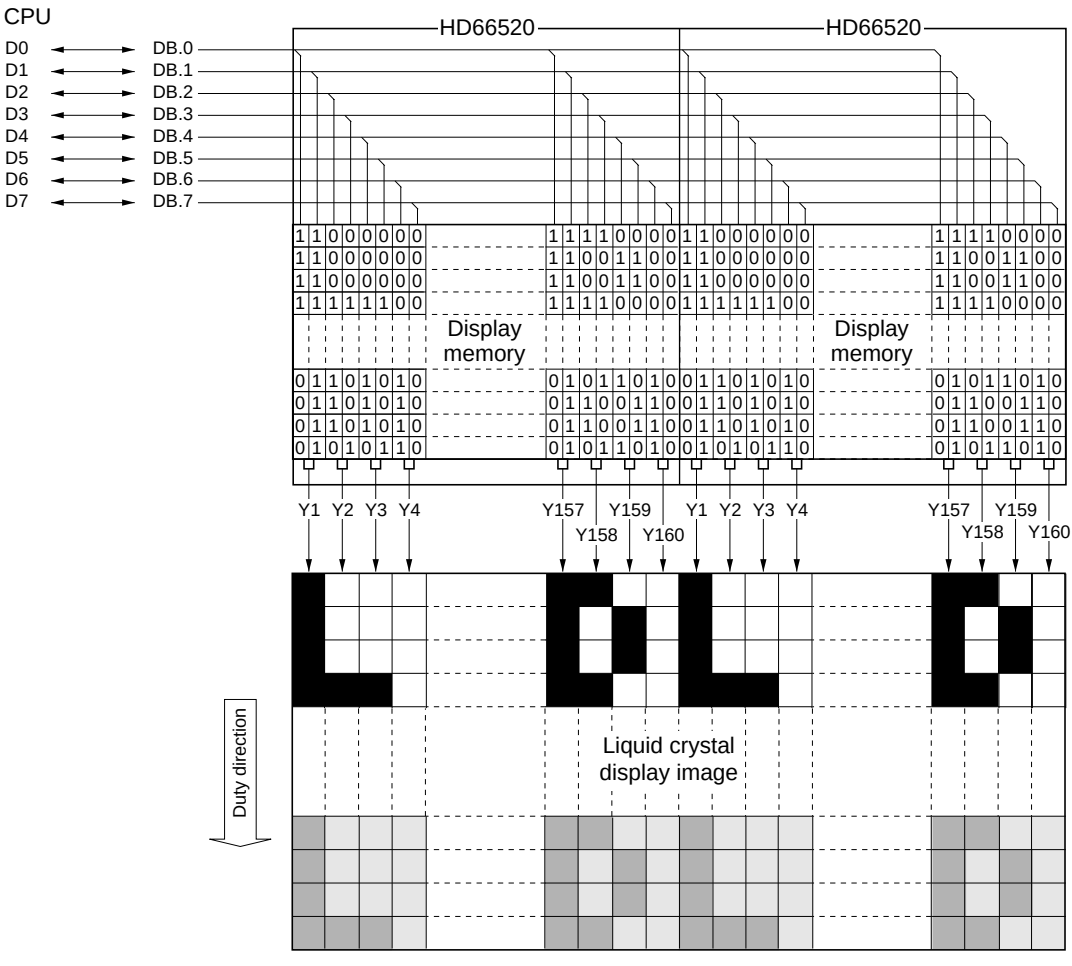


Figure 15 Quarter VGA Size (2)

Quarter VGA Size (SHL = High)

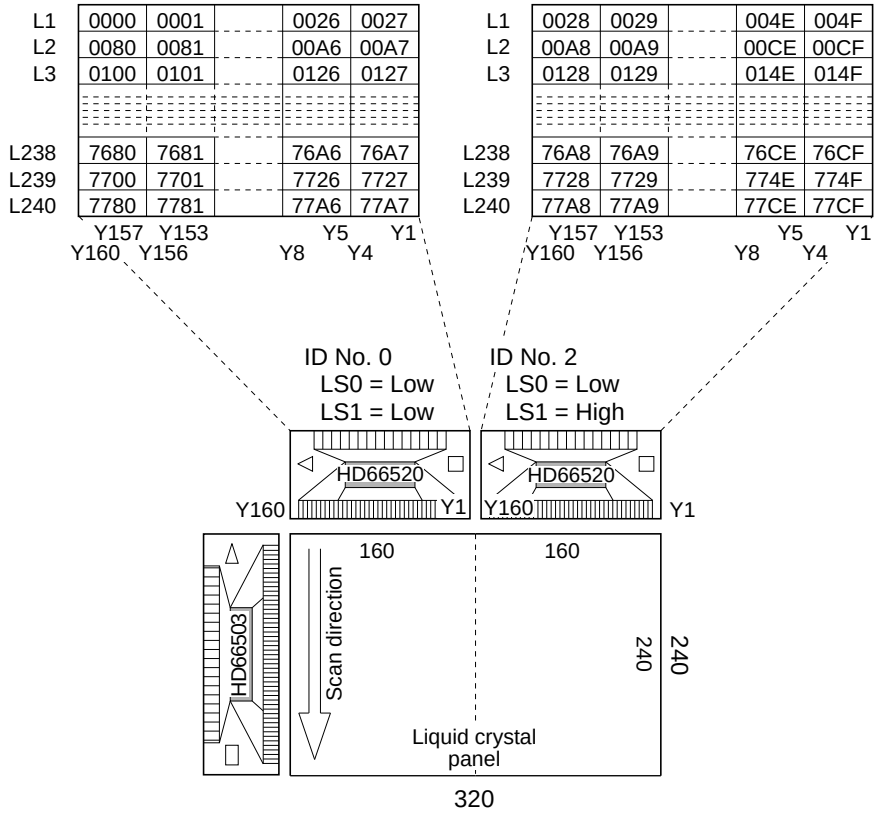


Figure 16 Quarter VGA Size (1)

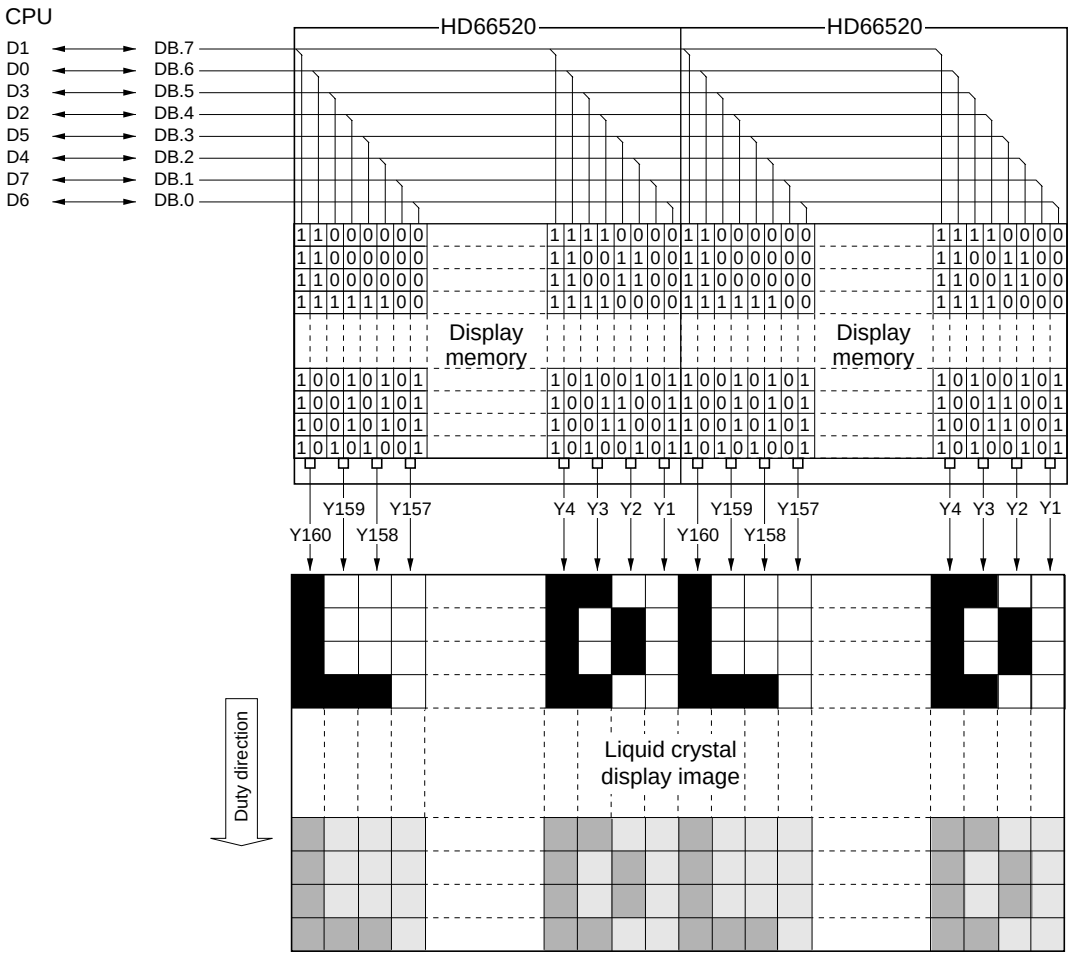


Figure 17 Quarter VGA Size (2)

Half VGA Size (SHL = Low)

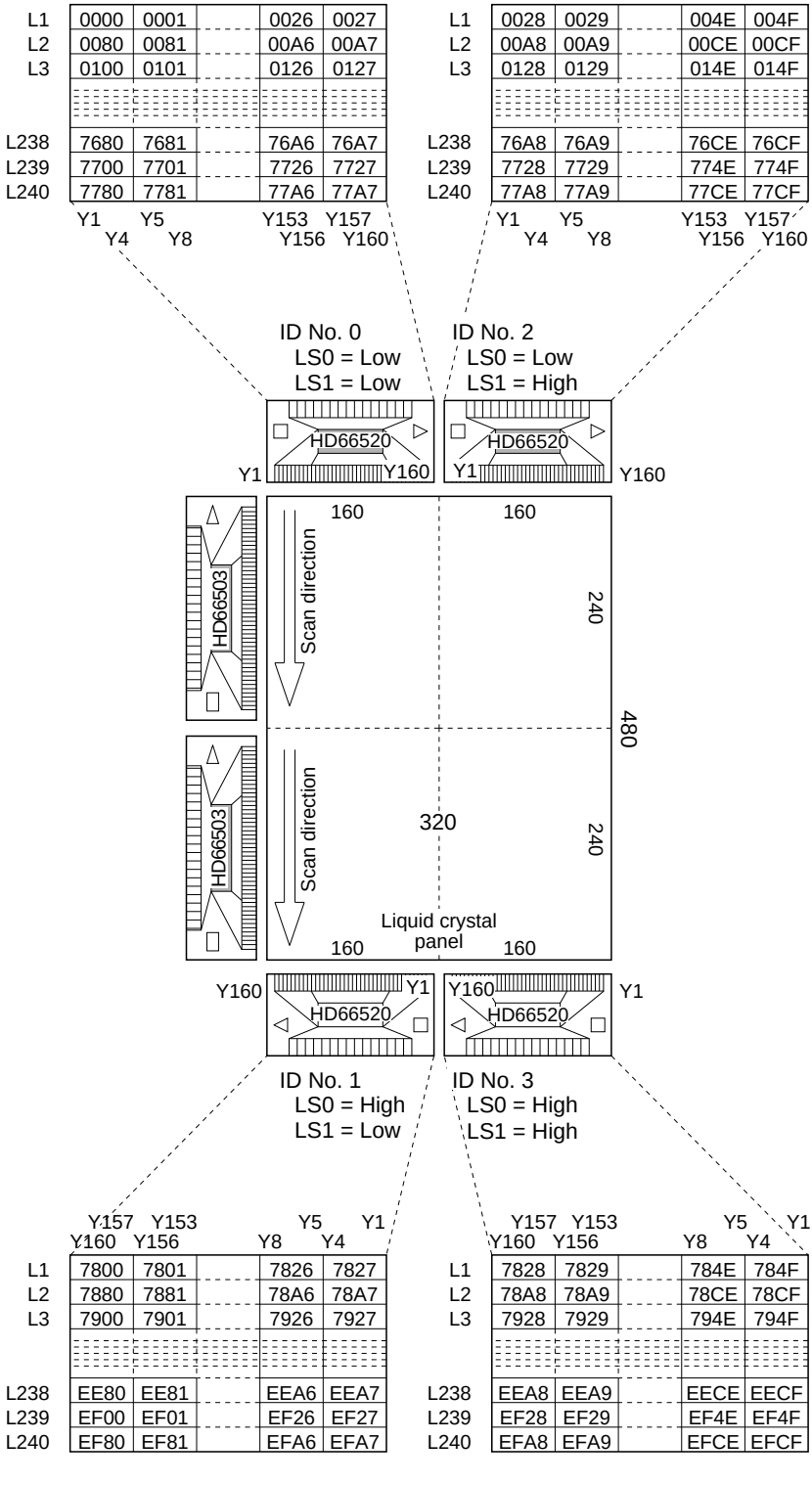


Figure 18 Half VGA Size (1)

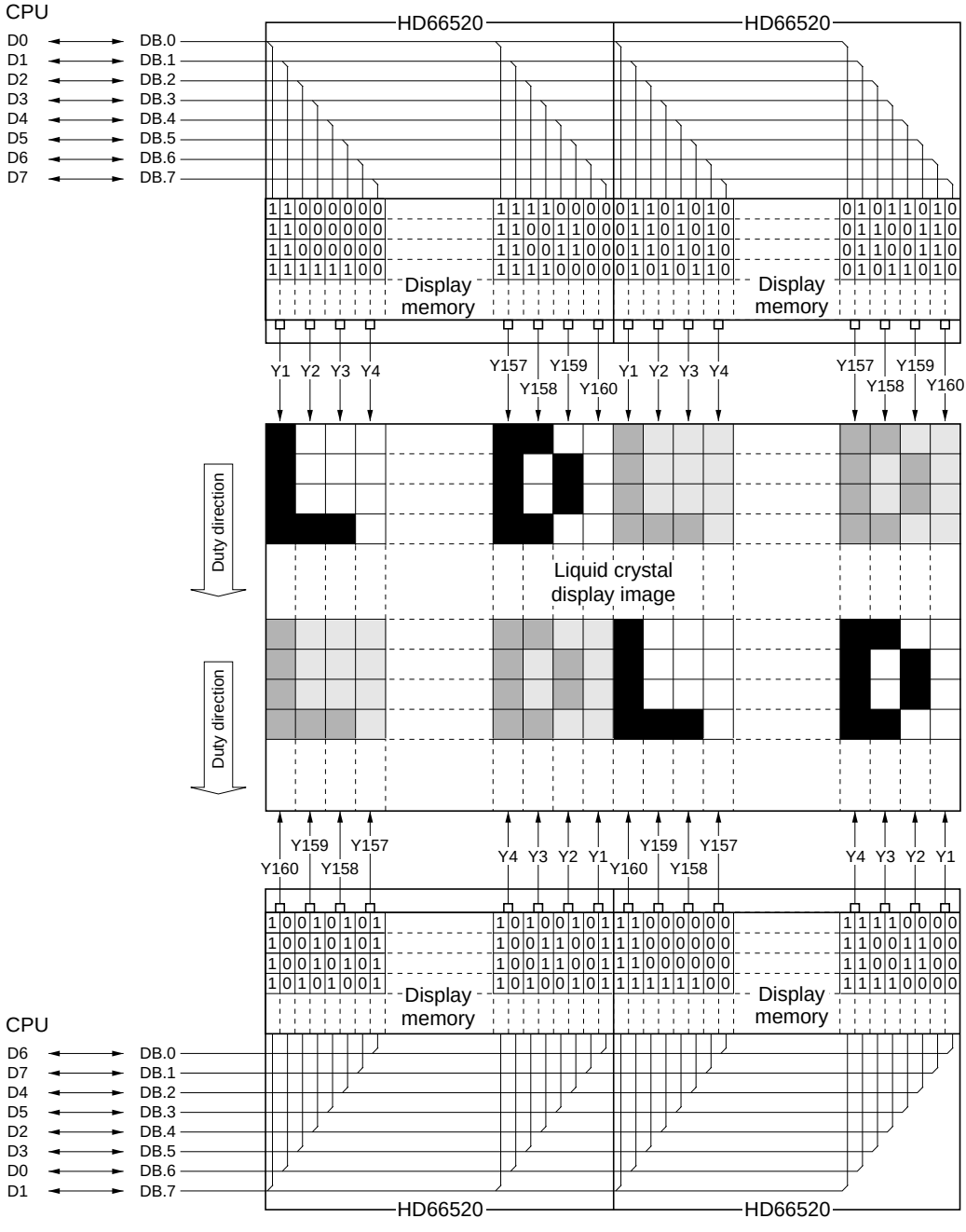


Figure 19 Half VGA Size (2)

Half VGA Size (SHL = High)

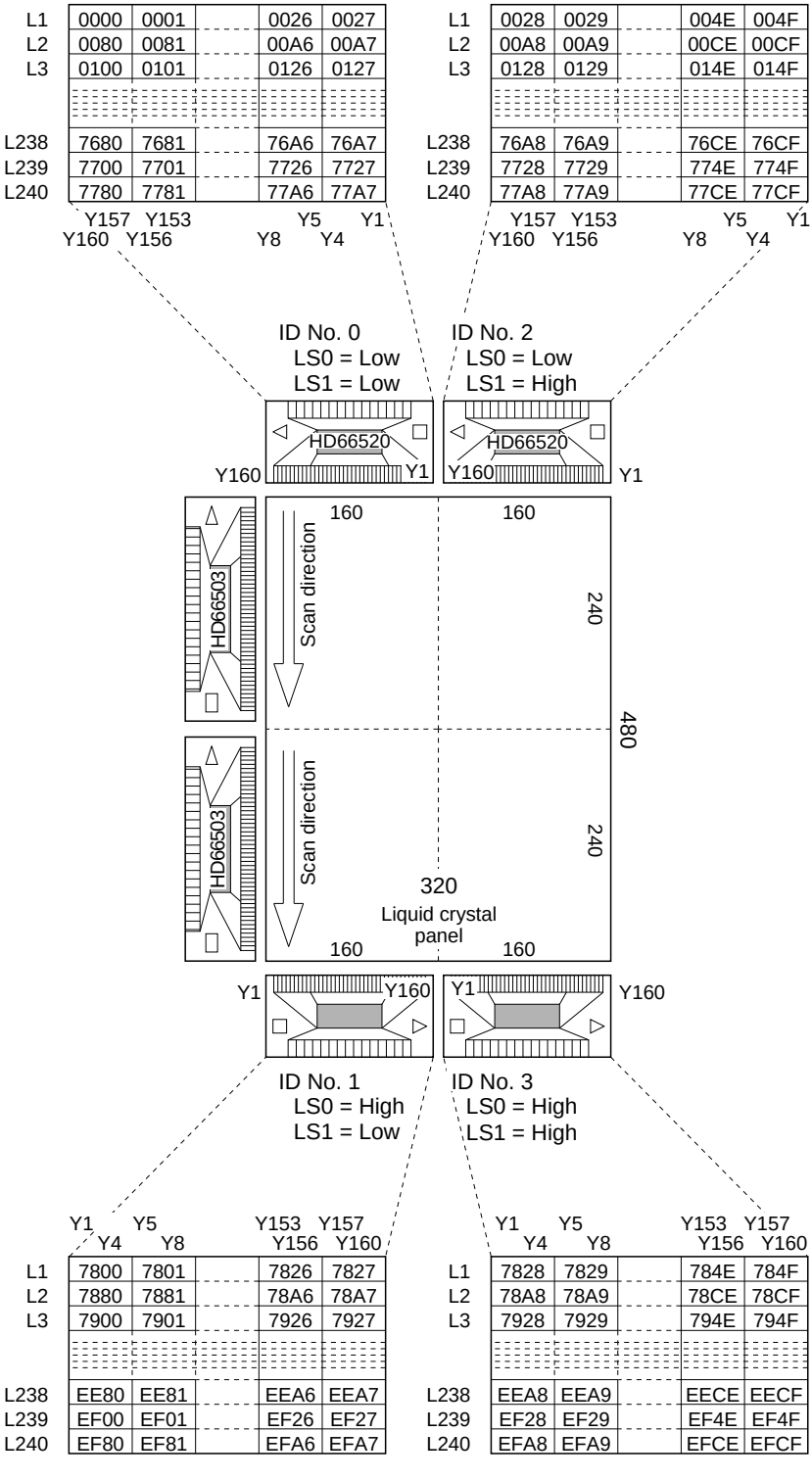


Figure 20 Half VGA Size (1)

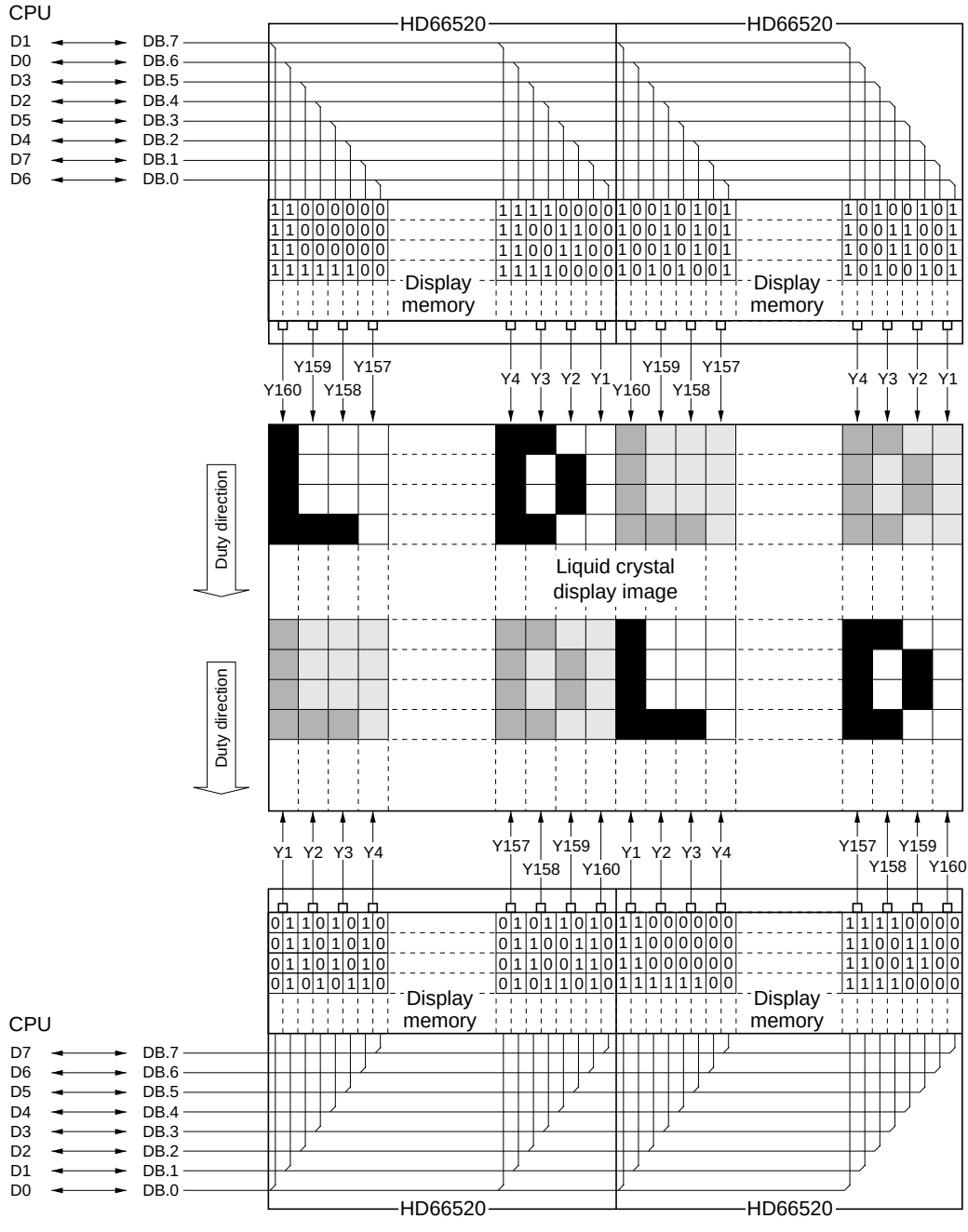


Figure 21 Half VGA Size (2)

Display-Data Transfer

Display RAM data is transferred to 160-bit data latch circuits 1 and 2 at each falling edge of the CL1 clock pulse. Since display data transfer and RAM access to draw data are completely synchronous-separated in the LSI, there will be no draw data loss or display flickering due to display data transfer timing.

The first line data transfer involves the first line marker (FLM), which initializes a line counter, and transfers the first line data to data latch circuits 1 and 2. Subsequent line data transfers involve transferring the second and the subsequent line data to data latch circuits 1 and 2 while incrementing the line counter value.

First Line Data Transfer

The line counter is initialized synchronously with an FLM signal. The first line is transferred to data latch circuits 1 and 2 at the falling edge of the CL1 (figure 22).

Subsequent Line Data Transfer

The second and the subsequent line data are transferred to data latch circuits 1 and 2 at the falling edge of the CL1 to update the line counter value (figure 23).

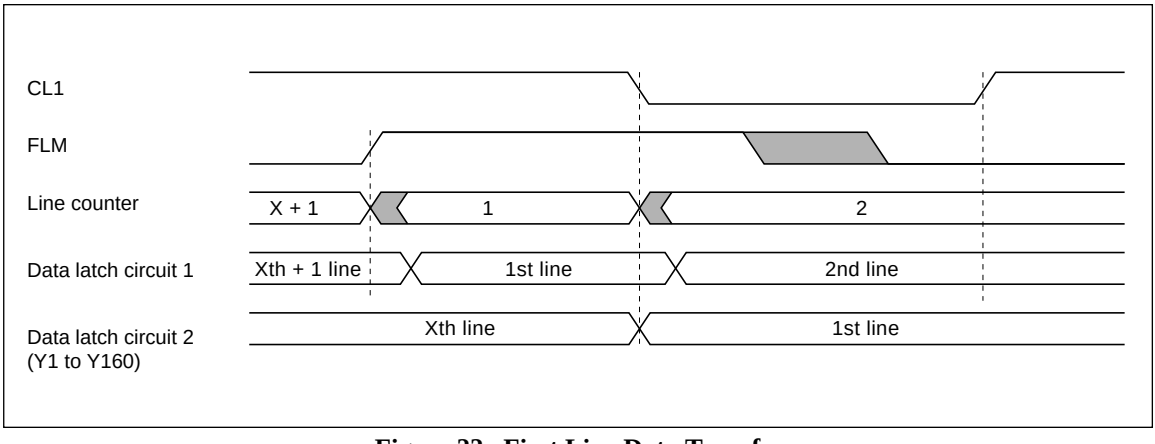
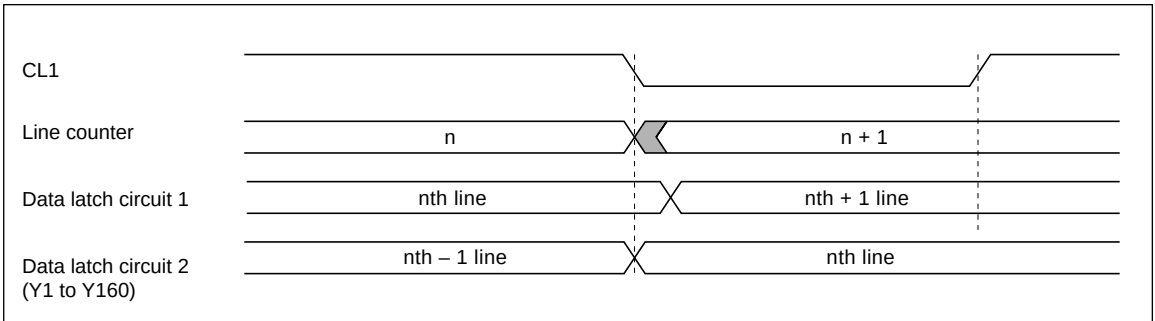


Figure 22 First Line Data Transfer



Note: Outputs Y1 to Y160 are converted into four levels before output according the liquid crystal altemating signal.

Figure 23 Subsequent Line Data Transfer

Draw Access

Random Cycle

Random cycle sequence is the same as that for the general-purpose SRAM interface (figures 24 and 25). It can easily be connected to a CPU address bus and data bus.

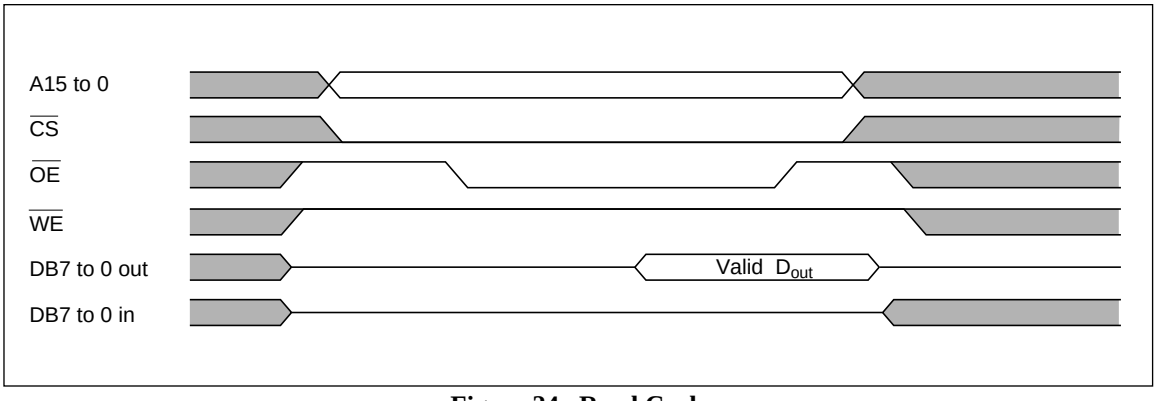


Figure 24 Read Cycle

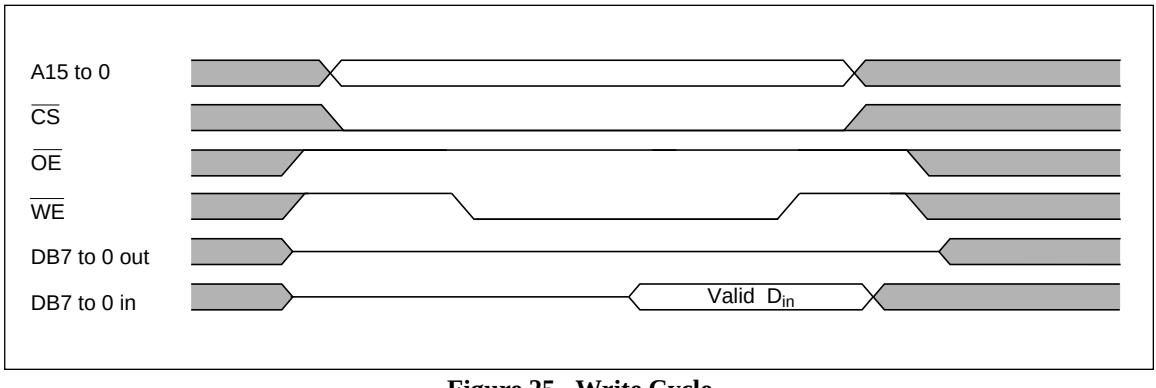


Figure 25 Write Cycle

Burst Cycle

Continuous access (burst cycle) can be performed by enabling addresses and $\overline{OE}$ or $\overline{WE}$ when $\overline{CS}$ is low (figures 26 and 27). Refer to restraints for the period of continuous transfer.

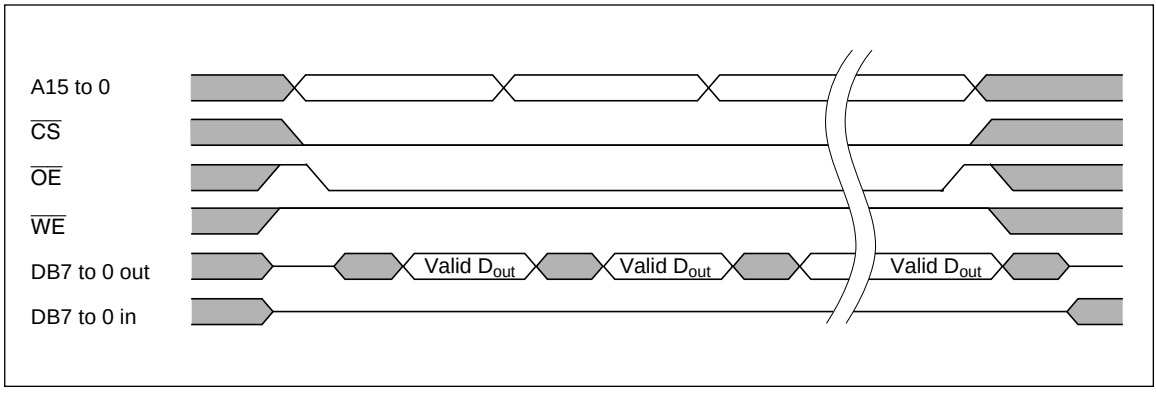


Figure 26 Burst Read Cycle

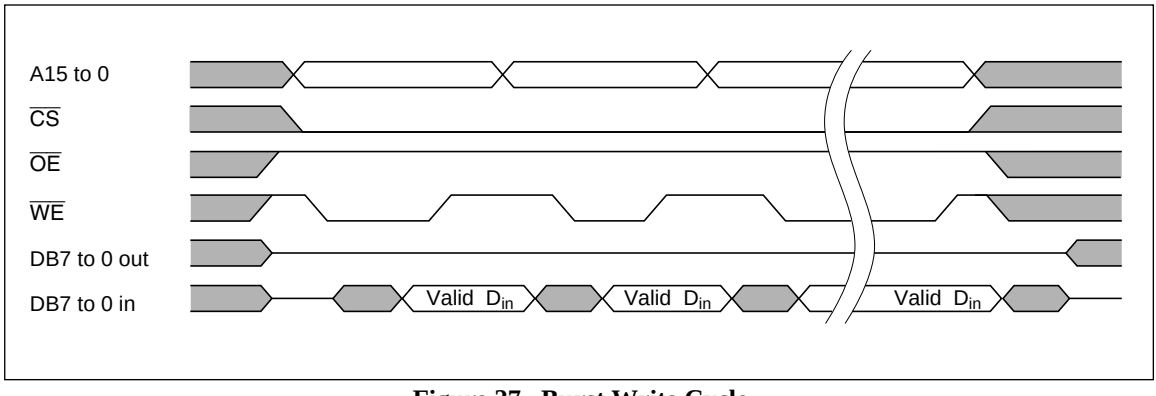


Figure 27 Burst Write Cycle

Arbitration Control

The HD66520 controls the arbitration between draw access and display access. The draw access reads and writes display data of the display memory incorporated in the HD66520. The display access outputs display memory line data to the liquid crystal panel. In this case, draw access is performed before display access, so continuous access is enabled without having the system to wait. For arbitration control, draw access is recognized as valid when signal $\overline{CS}$ is low.

The following describes the typical examples of display memory access state during arbitration control.

Sequence Line Data Transfer Display Access Performed by Subsequent Line Data Transfer

If no draw access is attempted, normal display access is performed when signal CL1 is low (figure 28).

Draw Access 1

If draw access is attempted when signal CL1 is high, draw access is performed regardless of the display access (figure 29).

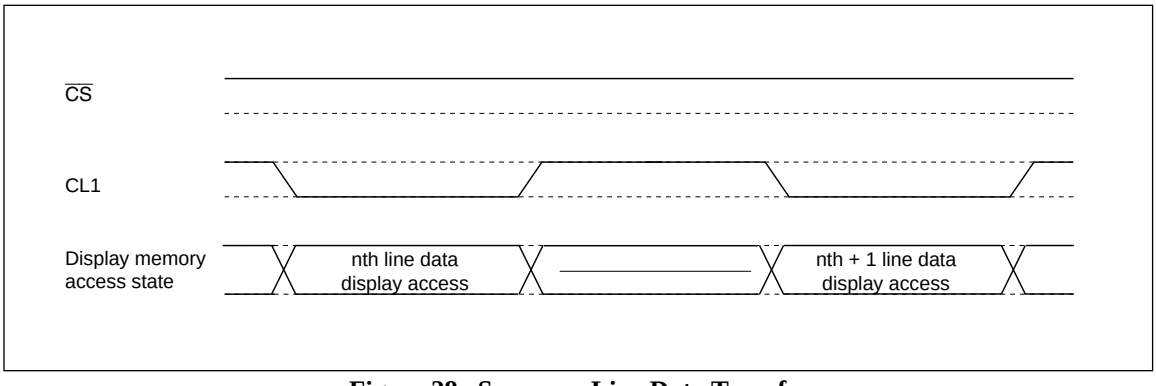


Figure 28 Sequence Line Data Transfer

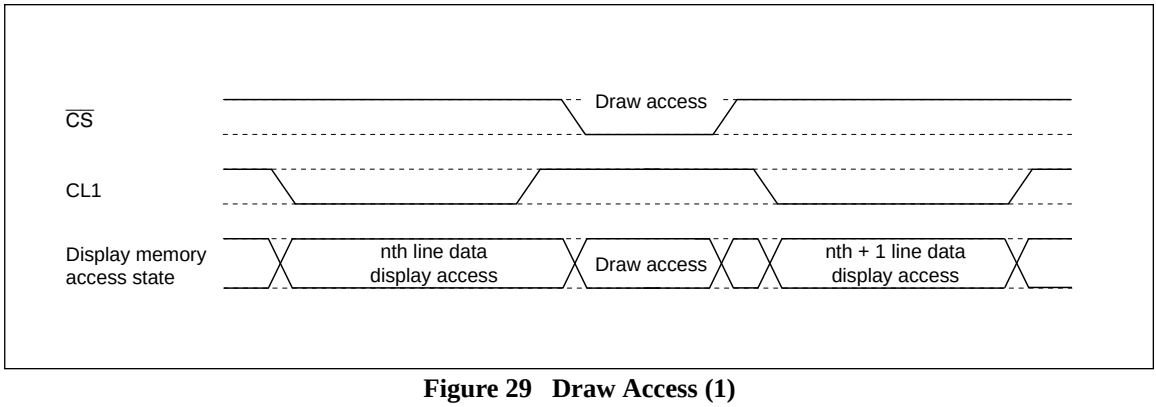


Figure 29 Draw Access (1)

Draw Access 2

If draw access is attempted when signal CL1 is low, the display access is suspended to perform draw access (figure 30). After the draw access, the display access is performed again. As a result, even if draw access is attempted asynchronously, at least one of the display accesses will be performed.

Display Access by First Line Data Transfer

If no draw access is attempted, display access for the first line is performed when signal FLM is high and CL1 is low. The display access for the second line is performed when signal CL1 is low (figure 31).

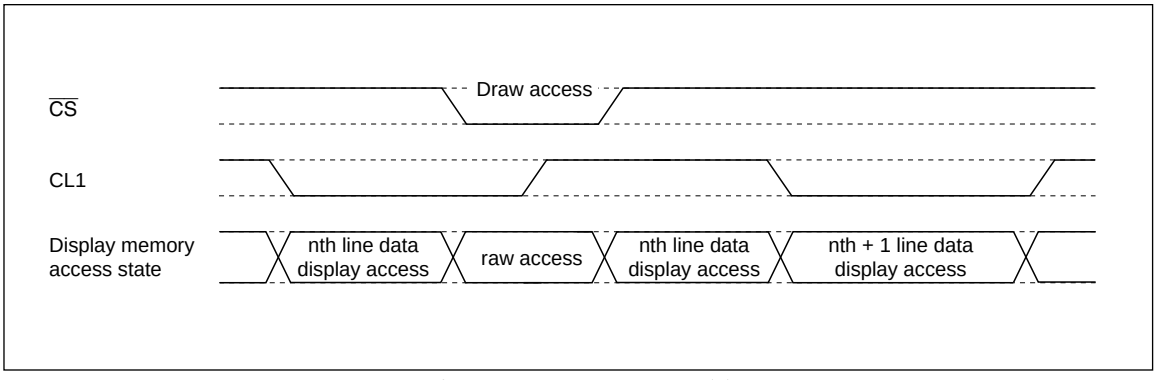


Figure 30 Draw Access (2)

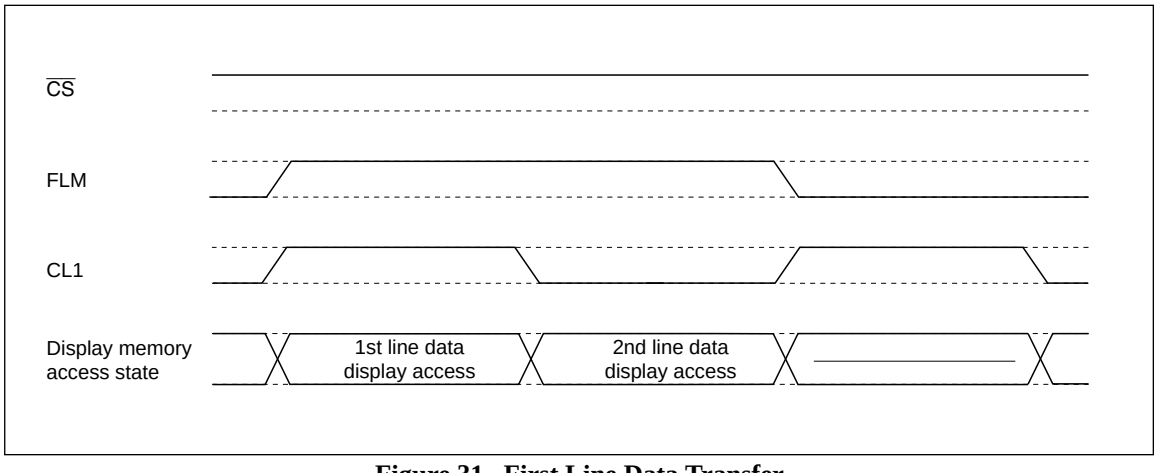


Figure 31 First Line Data Transfer

Draw Access 3

If draw access is attempted when signal FLM is high, stop the display access is suspended to perform the draw access (figure 32). After the draw access, the display access is performed again. As a result, even if draw access is attempted asynchronously, at least one of the two display accesses will be performed.

Note: In order to satisfy draw access 3 and transfer the first line data, there are restraints for the period when pins FLM and CL1 are both high and for the low level pulse width of pin $\overline{CS}$. Refer to Restraints for details on the restraints for the pulse width.

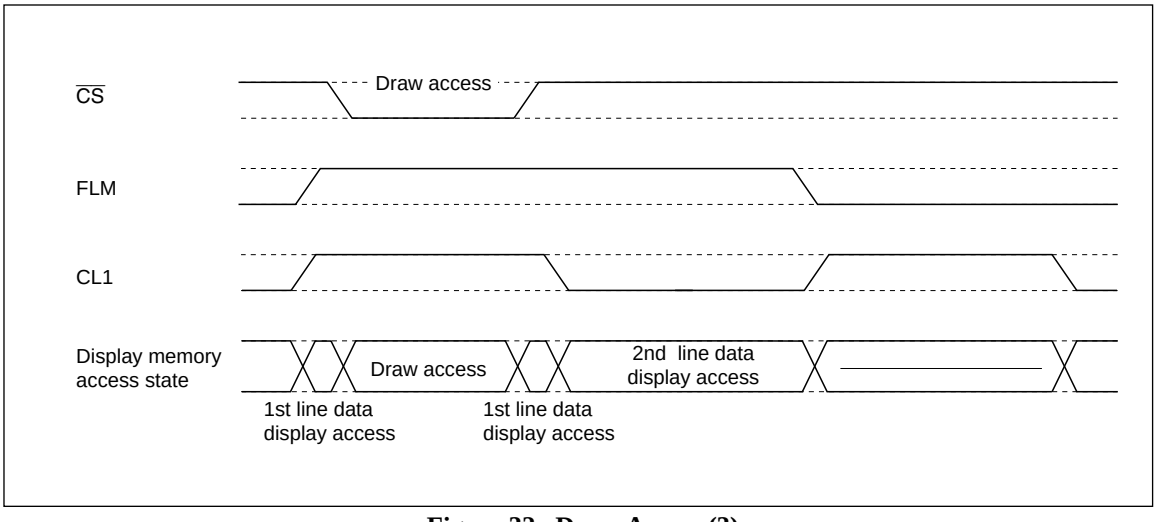


Figure 32 Draw Access (3)

Example of System Configuration

Figure 33 shows a system configuration for a 320-dot-wide by 240-dot-long LCD panel using HD66520s and common driver HD66503 with internal liquid crystal display timing control circuits. All required functions can be prepared for liquid crystal display with just three chips except for liquid crystal display power supply circuit functions.

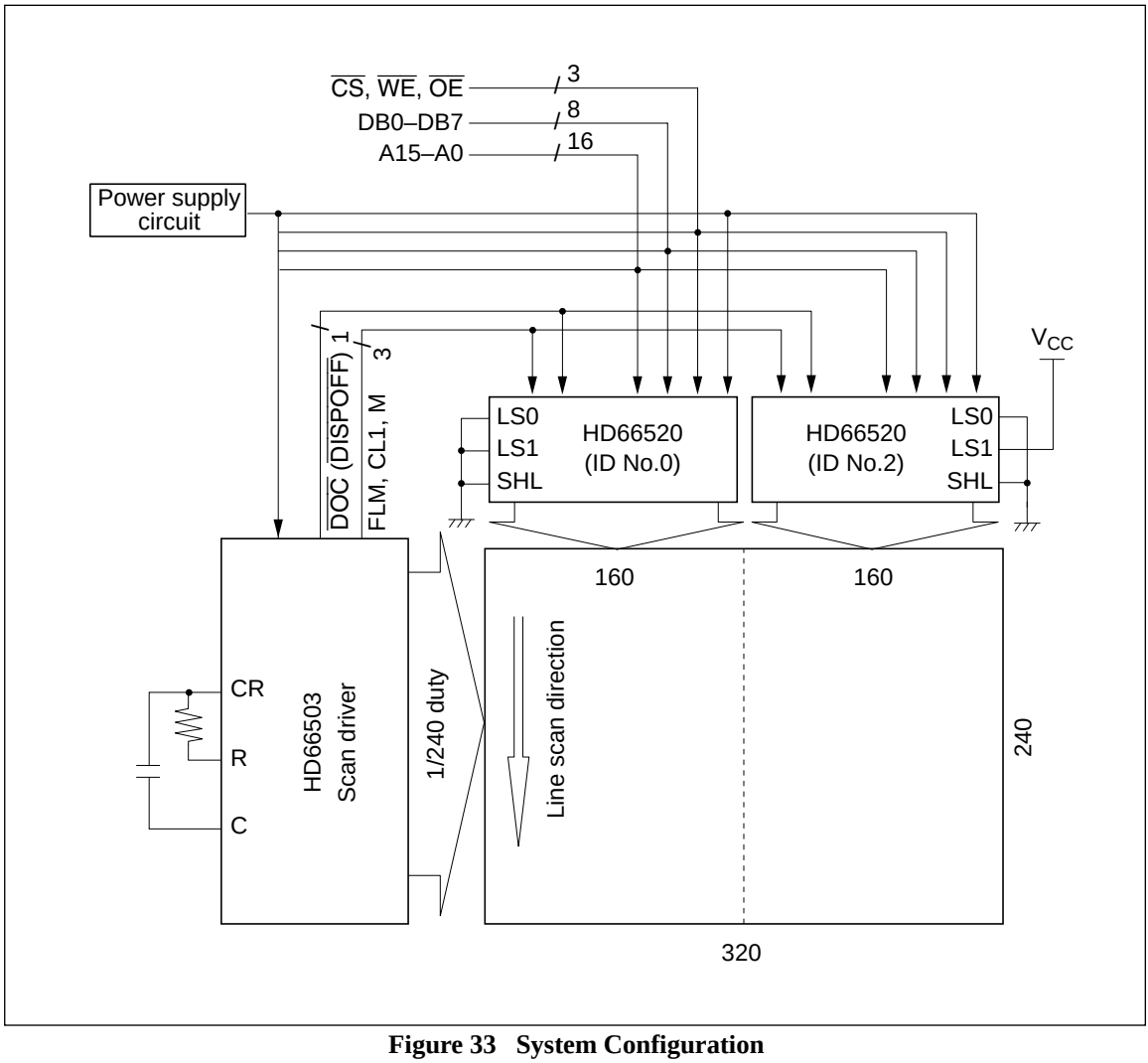


Figure 33 System Configuration

Restraints

The HD66520 can perform continuous draw access (burst access) when signal $\overline{CS}$ is low. As a result, display data can be rewritten at high speed.

However, since signal $\overline{CS}$ is necessary to perform arbitration control between draw access and display access to the display memory, the following restraints exist for the pulse width of signal $\overline{CS}$.

- Read operation

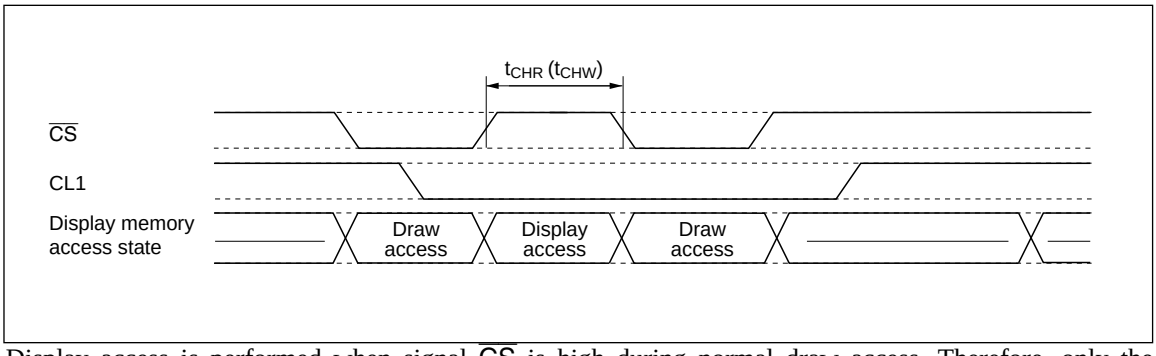
Item	Symbol	Min	Max	Unit
Chip select high level width	t_{CHR}	180	—	ns
Chip select low level width	t_{CLR}	300	t_{FS} – 1000	ns

- Write operation

Item	Symbol	Min	Max	Unit
Chip select high level width	t_{CHR}	180	—	ns

Chip select low level width	t_{CLR}	
180	t_{FS} – 1000	
ns		

Chip Select High Level Width



Display access is performed when signal $\overline{CS}$ is high during normal draw access. Therefore, only the

minimum display access time is necessary for the chip select high level width (figure 34).

Figure 34 Chip Select High Level Width

Chip Select Low Level Width

When continuous draw access (burst access) is performed when signal $\overline{CS}$ is low, the maximum display access time, that is, t_{FS}-1000 (ns) is necessary for the chip select low level width (figure 35). This is needed to secure the display access period for the first line.

When common driver HD66503 is used together with the HD66520, t_{FS} can be calculated with the following formula.

$$f_{FS} = \frac{1}{4 \cdot n_{DUTY} \cdot f_{FLM}}$$

f_{FLM}: frame frequency
n_{DUTY}: duty

When write operation is performed with the burst access having a frame frequency of 70 Hz and a duty cycle of 1/240, display data of 77 bytes can be consequtively written in one burst access (write cycle is 180 ns).

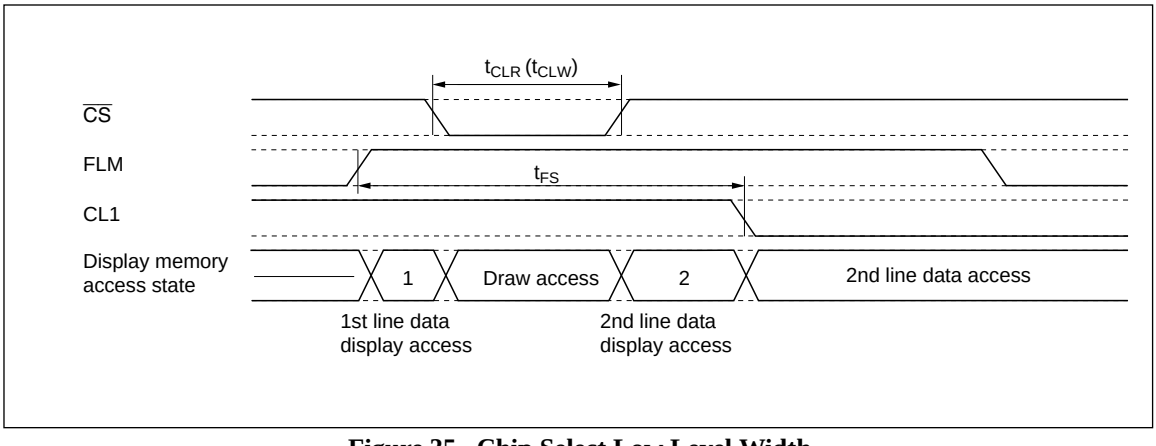


Figure 35 Chip Select Low Level Width

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).

2. Applies to pins LS0, LS1, SHL, FLM, CL1, M, A0 to A15, DB0 to DB7, $\overline{\text{DISPOFF}}$, $\overline{\text{CS}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$.

3. Applies to pins V1L, V1R, V2L. V2R, V3L, V3R, V4L, V4R.

4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

Electrical Characteristics

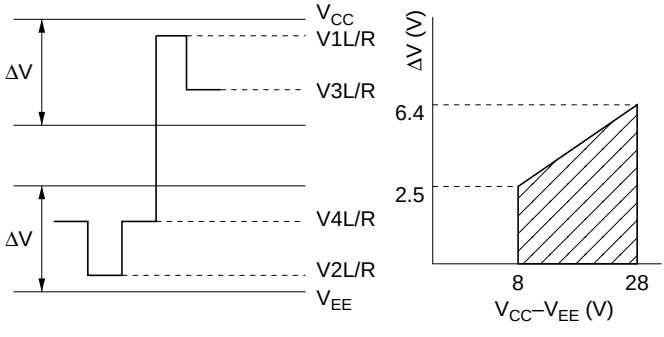
DC Characteristics 1 (V_{CC} = 3.0 to 3.6 V, GND = 0 V, $V_{CC} - V_{EE}$ = 8 to 28 V, Ta = –20 to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input leakage current (1)	I_{IL1}	Except for DB0 to DB7	–2.5	—	2.5	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current (2)	I_{IL2}	V1L/R, V2L/R, V3L/R, V4L/R	–25	—	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Tri-state leakage current	I_{IST}	DB0 to DB7	–10	—	10	µA	$V_{IN} = V_{CC}$ to GND	
Vi-Yj on resistance	R_{ON}	Y1 to Y160	—	1.0	2.0	kΩ	I_{ON} = 100 µA	1

Note: 1. Indicates the resistance between one pin from Y1 to Y160 and another pin from V1L/V1R, V2L/V2R, V3L/V3R, V4L/V4R when load current is applied to the Y pin; defined under the following conditions:

$V_{CC}–V_{EE}$ = 28 V
V1L/V1R, V3L/V3R = V_{CC} – 2/10 ($V_{CC}–V_{EE}$)
V4L/V4R, V2L/V2R = V_{EE} + 2/10 ($V_{CC}–V_{EE}$)

V1L/V1R and V3L/V3R should be near the V_{CC} level, and V2L/V2R and V4L/V4R should be near the V_{EE} level. All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage $V_{CC}–V_{EE}$.



Relationship between Driver Output Waveform and Output Voltage

DC Characteristics 2 (V_{CC} = 3.0 to 3.6 V, GND = 0 V, V_{CC}–V_{EE} = 8 to 28 V, Ta = –20 to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input high level voltage (1)	V_{IH1}	LS0–1, SHL, FLM, CL1, M, $\overline{DISPOFF}$	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage (1)	V_{IL1}		0	—	$0.2 \times V_{CC}$	V		
Input high level voltage (2)	V_{IH2}	DB0 to DB7, $\overline{CS}$, A0 to A15, $\overline{WE}$, $\overline{OE}$	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage (2)	V_{IL2}		0	—	$0.15 \times V_{CC}$	V		
Output high level voltage	V_{OH}	DB0 to DB7	$0.9 \times V_{CC}$	—	—	V	I_{OH} = –50 µA	
Output low level voltage	V_{OL}		—	—	$0.1 \times V_{CC}$	V	I_{OL} = 50 µA	
Current consumption during RAM access	I_{CC}	Measurement pin V_{CC}	—	—	18	mA	Access time 300 ns V_{CC} = 3.3 V	2
Current consumption in LCD drive part	I_{EE}	Measurement pin V_{EE}	—	—	200	µA	V_{CC}–V_{EE} = 28 V V_{CC} = 3.3 V t_{CYC} = 59.5 µs No access	2, 3
Current consumption during display operation	I_{DIS}	Measurement pin GND	—	—	120	µA		

Notes: 1. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

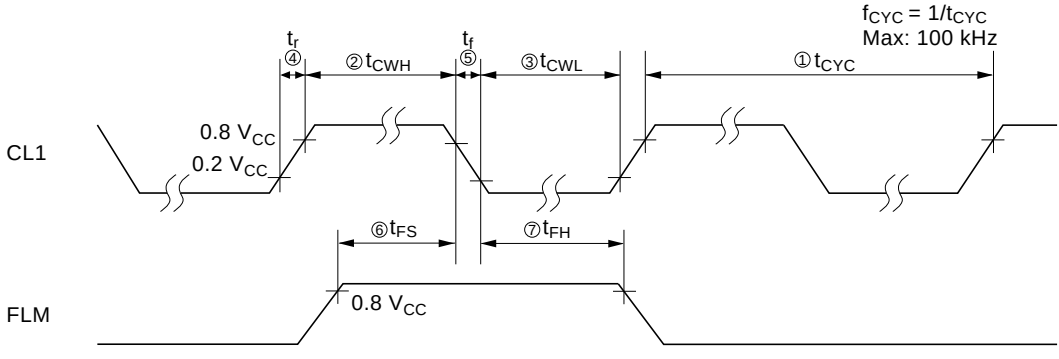
2. Indicates the current when the memory access is stopped and the still image of a zig-zag pattern is displayed in its place.

AC Characteristics 1 (V_{CC} = 3.0 to 3.6 V, GND = 0 V, V_{CC}–V_{EE} = 8 to 28 V, Ta = –20 to +75°C)

• Display-Data Transfer Timing

No.	Item	Symbol	Applicable Pins	Min	Max	Unit	Notes
1	Clock cycle time	t_{CYC}	CL1	10	—	µs	1
2	CL1 high-level width	t_{CWH}	CL1	1.0	—	µs	
3	CL1 low-level width	t_{CWL}	CL1	1.0	—	µs	
4	CL1 rise time	t_r	CL1	—	50	ns	
5	CL1 fall time	t_f	CL1	—	50	ns	
6	FLM setup time	t_{FS}	FLM, CL1	2.0	—	µs	2
7	FLM hold time	t_{FH}	FLM, CL1	1.0	—	µs	

Notes: 1.



2. When executing draw access with burst transfer, the period described in the restrains must be satisfied in the relationship with the arbitration control.

AC Characteristics 2 (V_{CC} = 3.0 to 3.6 V, GND = 0 V, V_{CC}–V_{EE} = 8 to 28 V, Ta = –20 to +75°C)

- Draw Access Timing

— Read Cycle

Measurement conditions:
Input level: V_{IH} = 2.4 V, V_{IL} = 0.8 V
Output level: V_{OH}/V_{OL} = 1.5 V
Output load: 1 TTL gate + 100 pF capacitor

No.	Item	Symbol	Min	Max	Unit	Note
8	Read cycle time	t_{RC}	300	—	ns	
9	Address access time	t_{AA}	—	300	ns	
10	Chip select access time	t_{CA}	—	300	ns	
11	CS high level width	t_{CHR}	180	—	ns	
12	CS low level width	t_{CLR}	300	t_{FS}-1000	ns	
13	OE delay time	t_{OE}	—	150	ns	
14	OE delay time (low impedance)	t_{OLZ}	5	—	ns	
15	Output-disable delay time	t_{OHZ}	0	30	ns	
16	Output hold time	t_{OH}	5	—	ns	
27	Address/chip select setup time	t_{SU}	0	—	ns	1

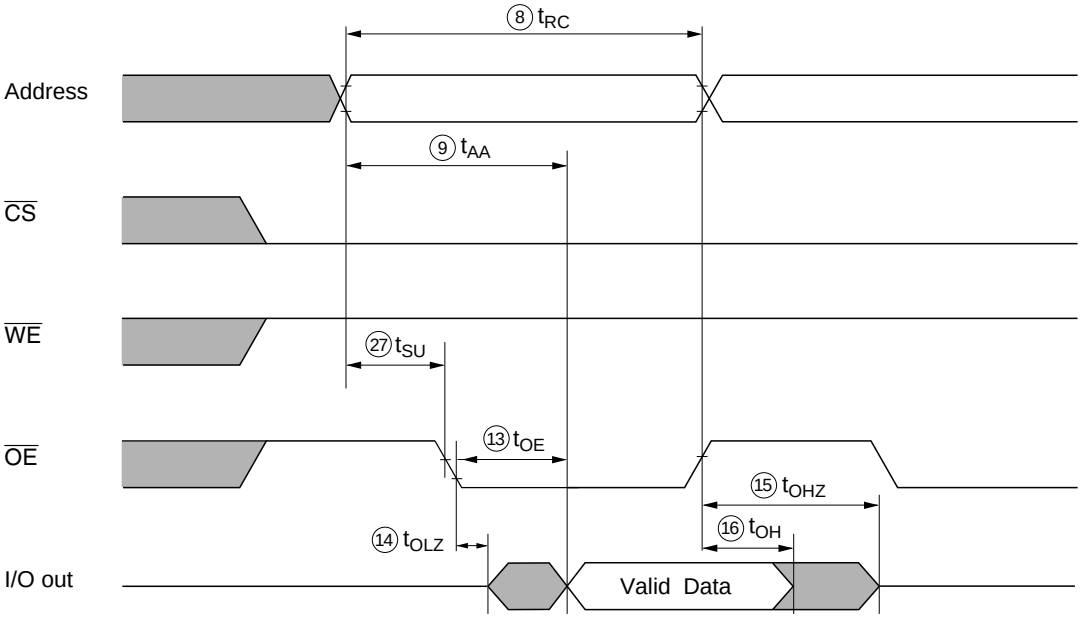
— Write Cycle

Measurement conditions:
Input level: V_{IH} = 2.4 V, V_{IL} = 0.8 V

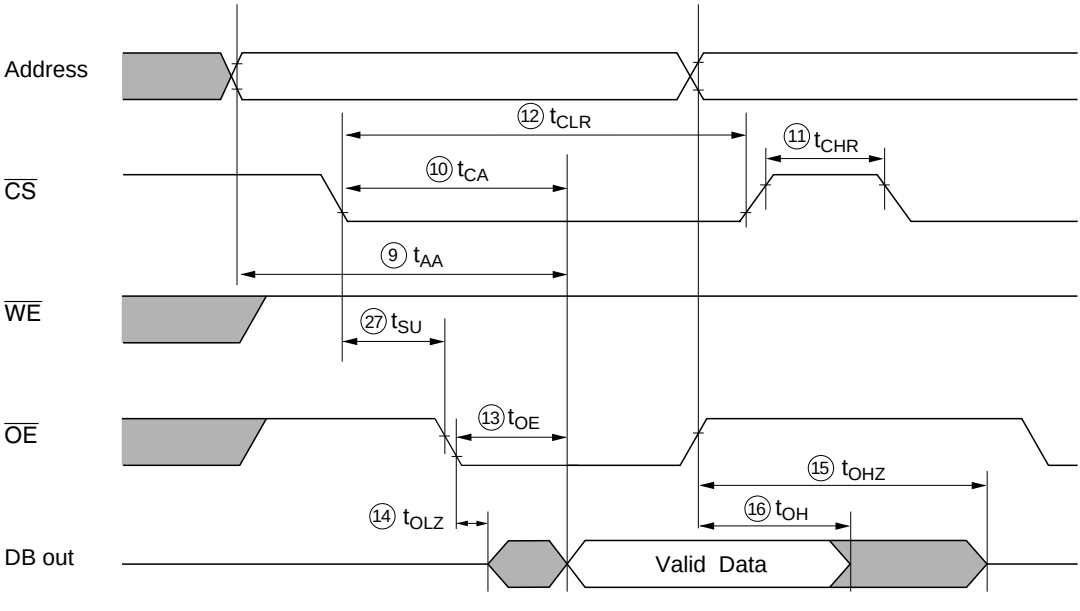
No.	Item	Symbol	Min	Max	Unit	Note
17	Write cycle time	t_{WC}	180	—	ns	
18	Address-to-WE setup time	t_{ASW}	30	—	ns	
19	CS high level width	t_{CHW}	180	—	ns	
20	CS low level width	t_{CLW}	180	t_{FS}-1000	ns	
21	Address-to-WE hold time	t_{AHW}	0	—	ns	
22	CS-to-WE hold time	t_{CH}	0	—	ns	
23	WE low level width	t_{WLW}	100	—	ns	
24	WE high level width	t_{WHW}	30	—	ns	
25	Data-to-WE setup time	t_{DS}	80	—	ns	
26	Data-to-WE hold time	t_{DH}	30	—	ns	

Note: 1. This is a setup time between $\overline{OE}$ and either address or $\overline{CS}$, whichever enabled later.

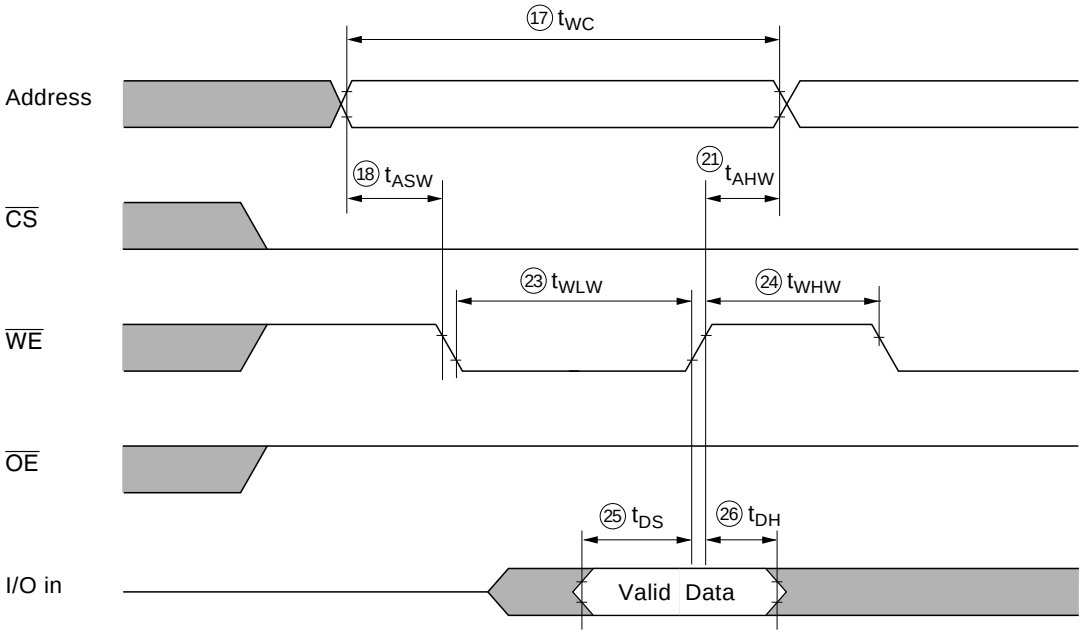
Read Cycle 1



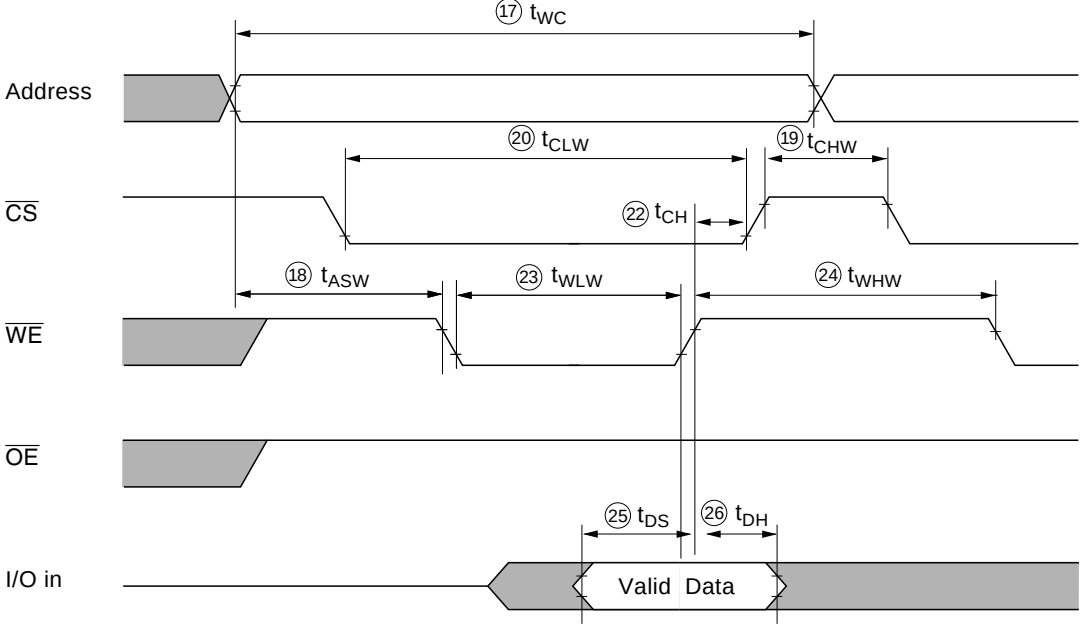
Read Cycle 2



Write Cycle 1



Write Cycle 2



HD66204

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

HITACHI

Description

The HD66204F/HD66204FL/HD66204TF/HD66204TFL, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66204 has a complete line-up: the HD66204F, a standard device powered by 5 V ± 10%; the HD66204FL, a 2.7 to 5.5 V, low power dissipation device suitable for battery-driven portable equipment such as "notebook" personal computers and palm-top personal computers; and the HD66204TF and HD66204TFL, thin package devices powered by 5 V ± 10% and 2.7 to 5.5 V, respectively.

Features

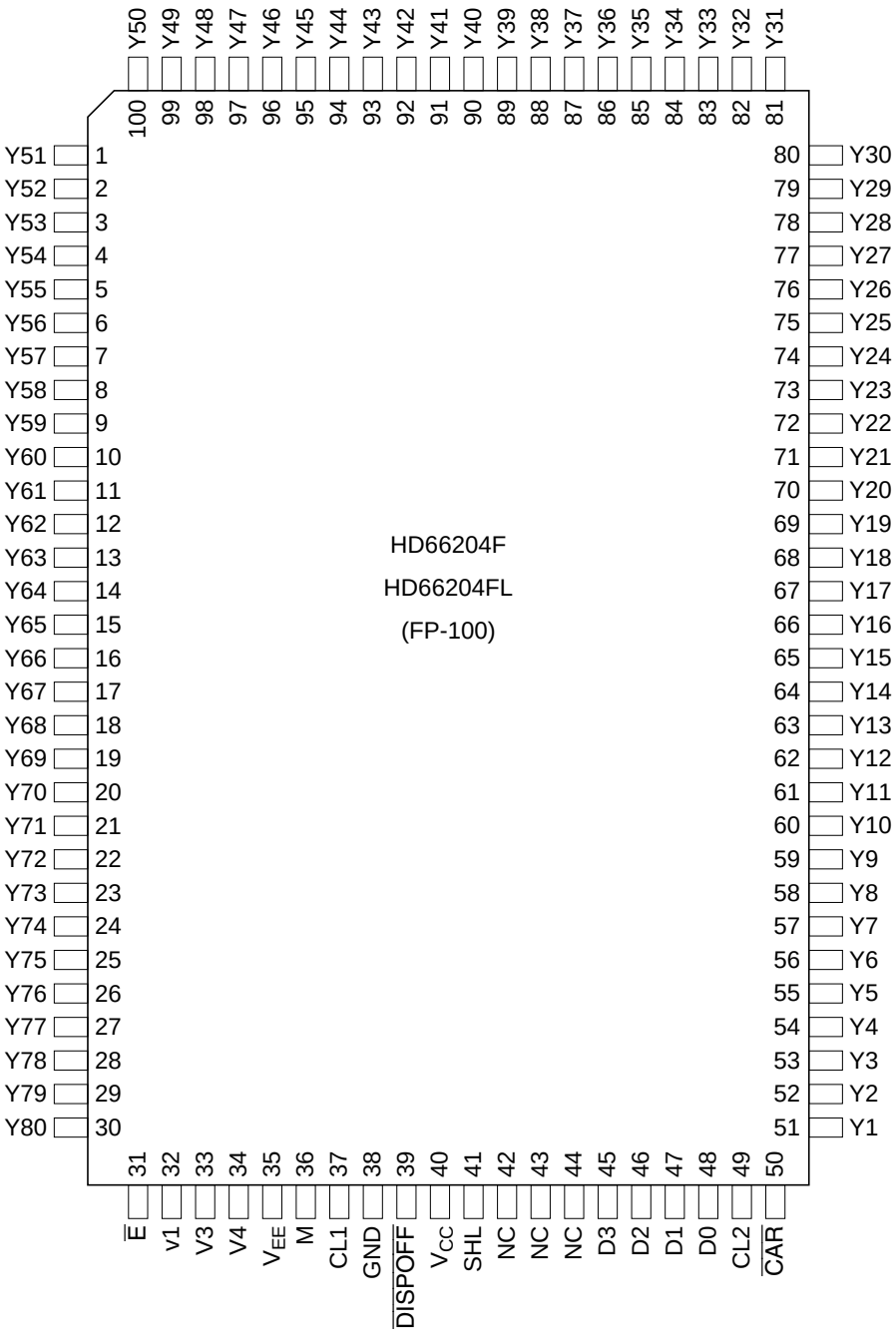
- Duty cycle: 1/64 to 1/240
- High voltage
  - LCD drive: 10 to 28 V
- High clock speed
  - 8 MHz max under 5-V operation (HD66204F/HD66204TF)
  - 4 MHz max under 3-V operation (HD66204FL/HD66204TFL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  - LCTC series: HD63645, HD64645, HD64646
  - LVIC series: HD66840, HD66841
  - CLINE: HD66850

Ordering Information

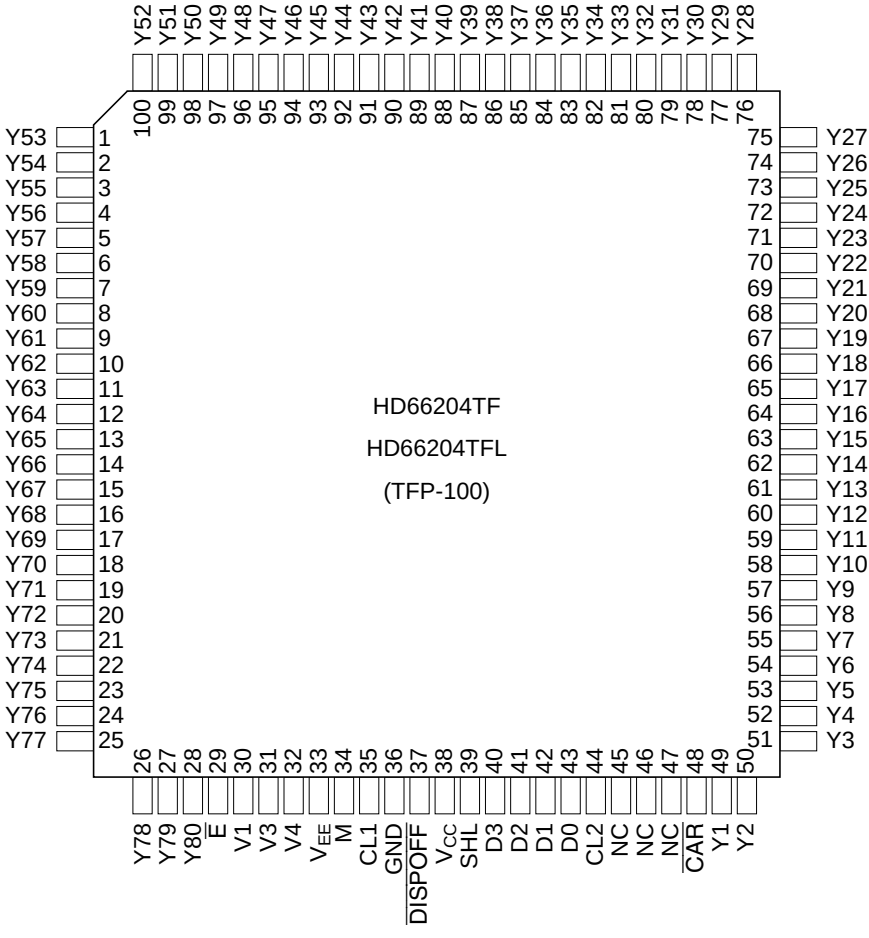
Type No.	Voltage Range	Package
HD66204F	5 V ± 10%	100-pin plastic QFP (FP-100)
HD66204TF	5 V ± 10%	100-pin thin plastic QFP (TFP-100)
HCD66204	5 V ± 10%	Chip
HD66204FL	2.7 to 5.5 V	100-pin plastic QFP (FP-100)
HD66204TFL	2.7 to 5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66204L	2.7 to 5.5 V	Chip

Hitachi semiconductor

Pin Arrangement



(Top view)


Y52 Y51 Y50 Y49 Y48 Y47 Y46 Y45 Y44 Y43 Y42 Y41 Y40 Y39 Y38 Y37 Y36 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
Y53 1
Y54 2
Y55 3
Y56 4
Y57 5
Y58 6
Y59 7
Y60 8
Y61 9
Y62 10
Y63 11
Y64 12
Y65 13
Y66 14
Y67 15
Y68 16
Y69 17
Y70 18
Y71 19
Y72 20
Y73 21
Y74 22
Y75 23
Y76 24
Y77 25
75 Y27
74 Y26
73 Y25
72 Y24
71 Y23
70 Y22
69 Y21
68 Y20
67 Y19
66 Y18
65 Y17
64 Y16
63 Y15
62 Y14
61 Y13
60 Y12
59 Y11
58 Y10
57 Y9
56 Y8
55 Y7
54 Y6
53 Y5
52 Y4
51 Y3
HD66204TF
HD66204TFL
(TFP-100)
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
Y78 Y79 Y80 E V1 V3 V4 VEE M CL1 GND DISPOFF VCC SHL D3 D2 D1 D0 CL2 NC NC NC CAR Y1 Y2

(Top view)

Pin Description

Symbol	Pin No. (FP-100/TFP-100)	Pin Name	Input/Output	Classification
V_{CC}	40/38	V_{CC}	—	Power supply
GND	38/36	GND	—	Power supply
V_{EE}	35/33	V_{EE}	—	Power supply
V1	32/30	V1	Input	Power supply
V3	33/31	V3	Input	Power supply
V4	34/32	V4	Input	Power supply
CL1	37/35	Clock 1	Input	Control signal
CL2	49/44	Clock 2	Input	Control signal
M	36/34	M	Input	Control signal
D0–D3	48–45/43–40	Data 0–data 3	Input	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{E}$	31/29	Enable	Input	Control signal
$\overline{CAR}$	50/48	Carry	Output	Control signal
$\overline{DISPOFF}$	39/37	Display off	Input	Control signal
Y1–Y80	51–100, 1–30/49–100, 1–28	Y1–Y80	Output	LCD drive output
NC	42, 43, 44/45, 46, 47	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D0–D3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D0–D3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66204 if HD66204s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISPOFF}$ sets LCD drive outputs Y1–Y80 to V1 level.

LCD Drive Output

Y1–Y80: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

NC: Must be open.

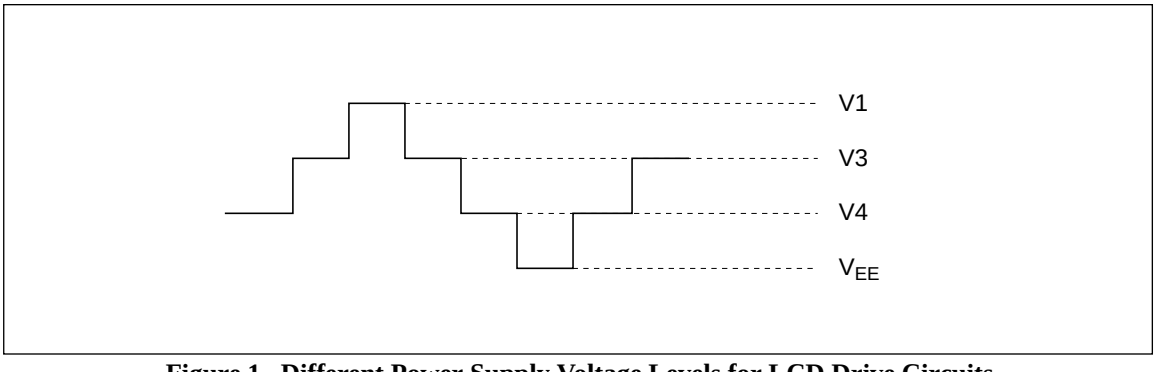


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

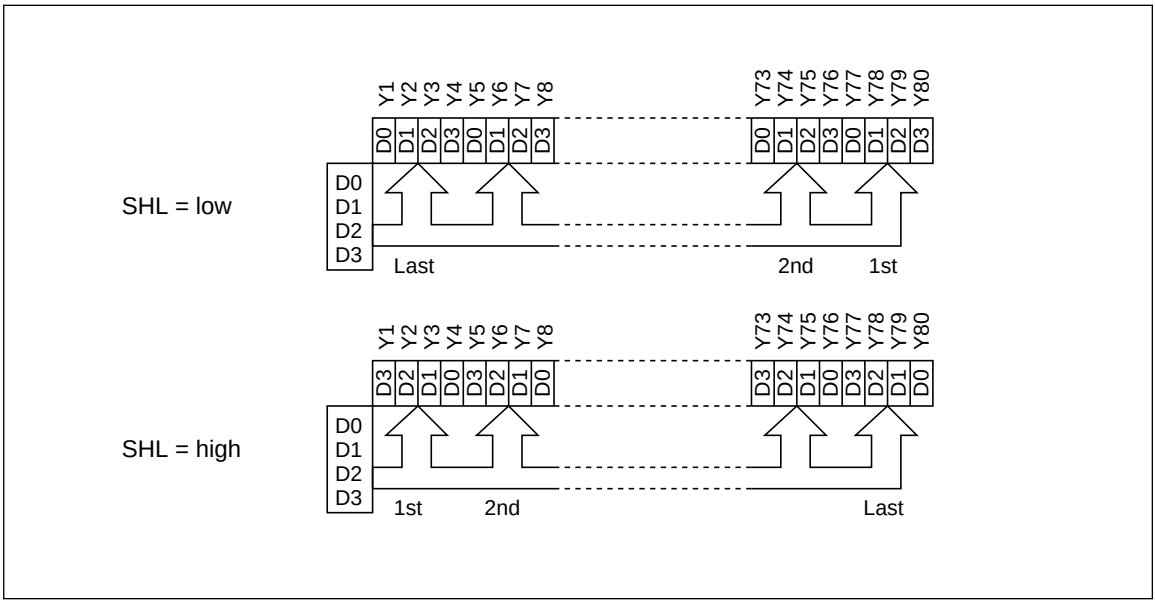


Figure 2 Selection of Destinations of Display Data Output

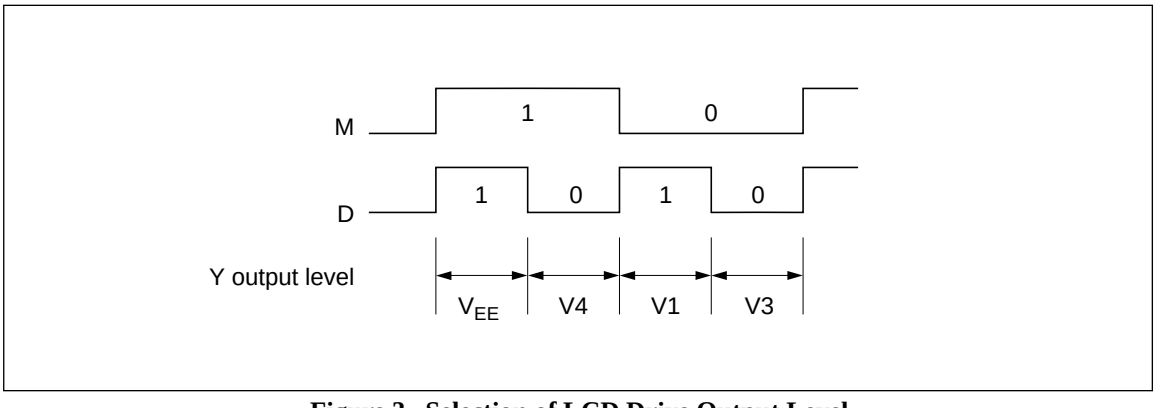


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D_0 to D_3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

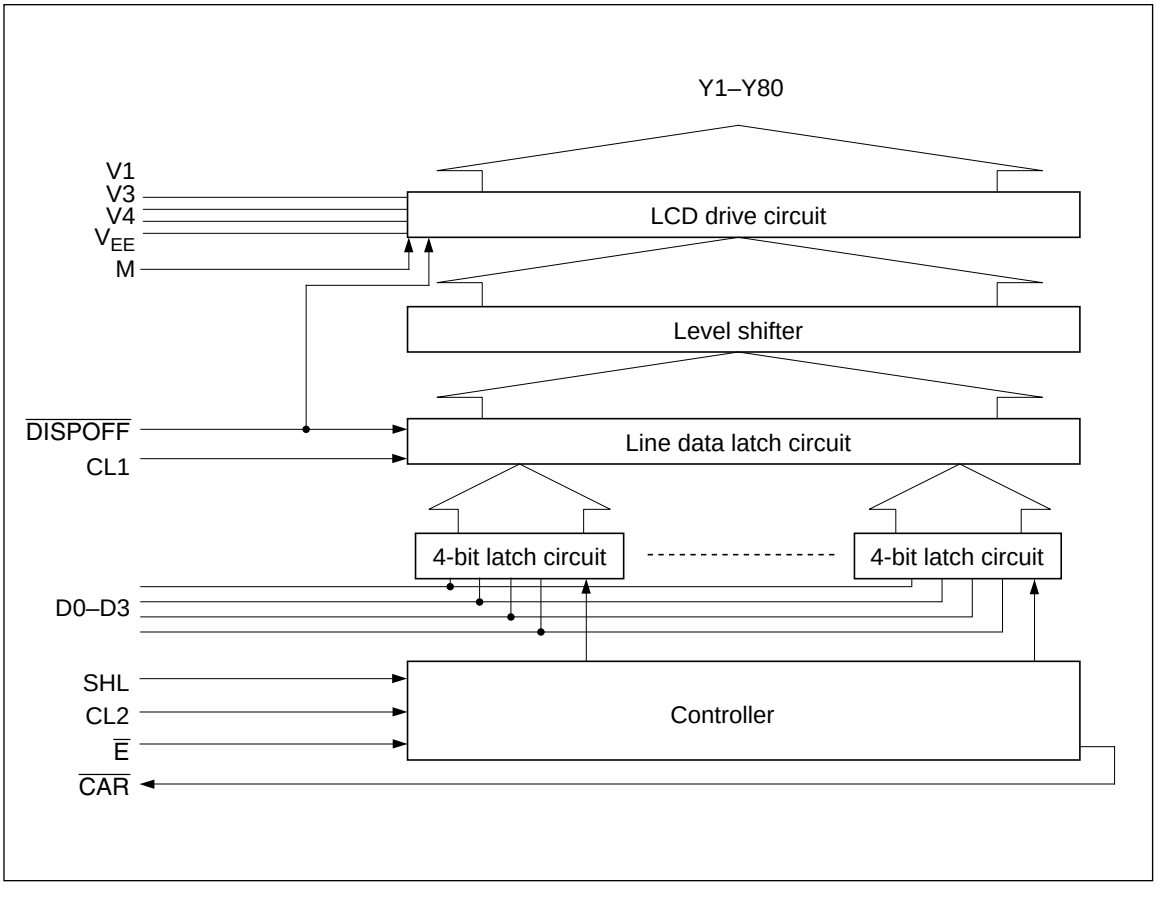
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and V_{EE}, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



Comparison of the HD66204 with the HD61104

Item	HD66204	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10 to 28 V	10 to 26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as V_{EE} level)	V1, V2, V3, V4

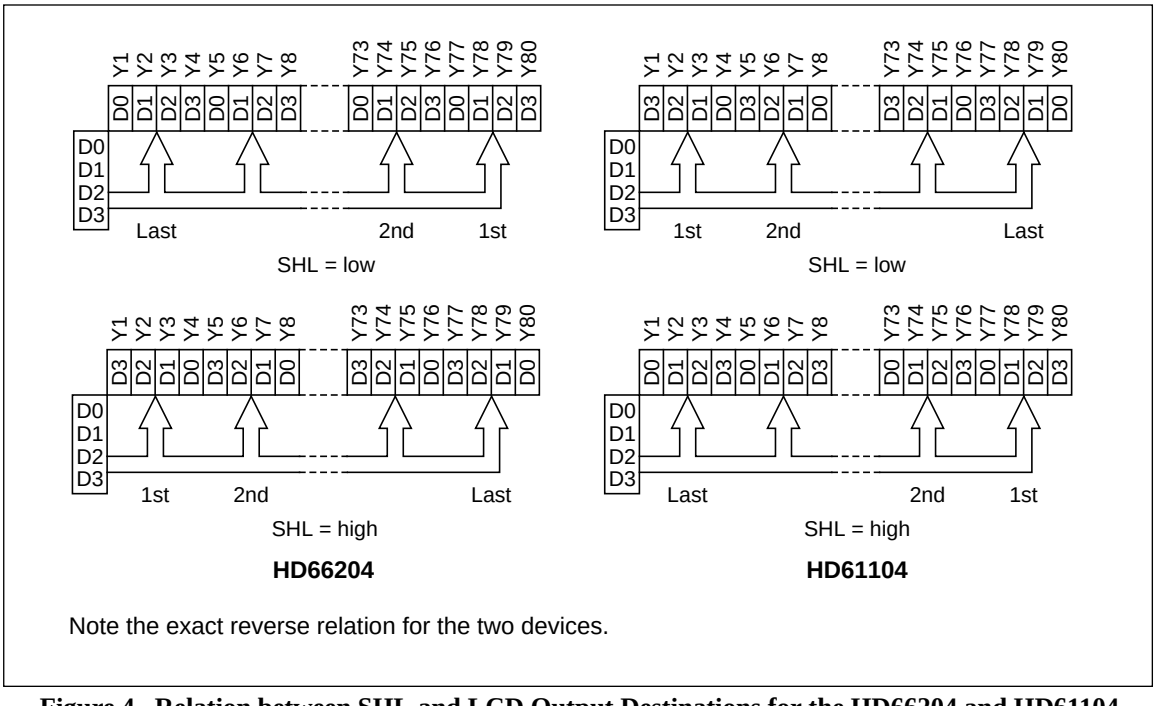


Figure 4 Relation between SHL and LCD Output Destinations for the HD66204 and HD61104

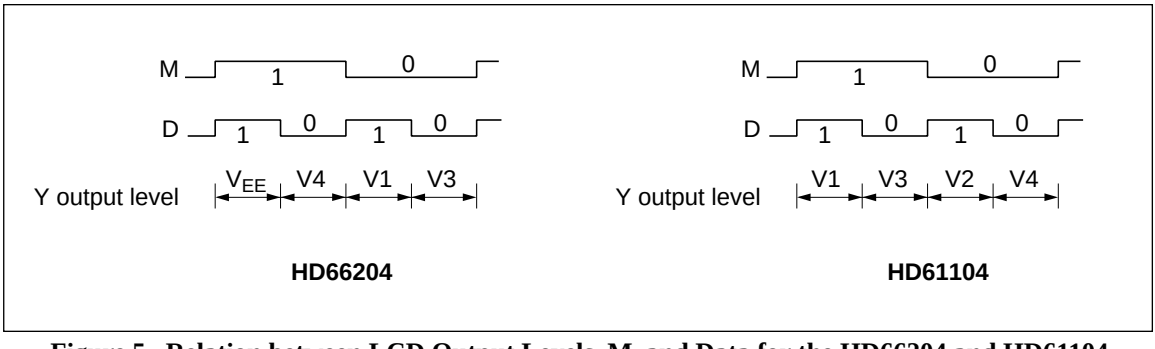
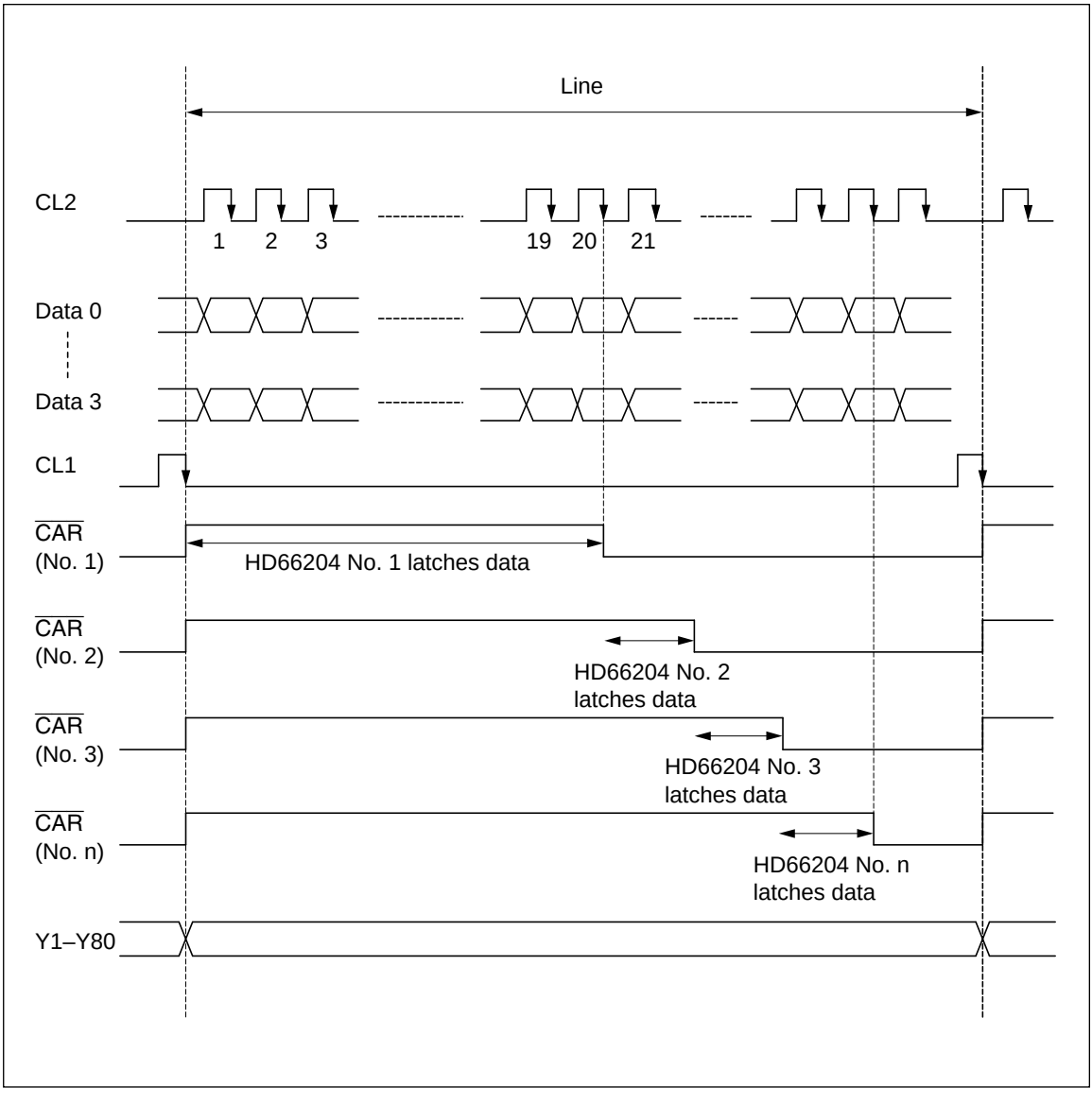
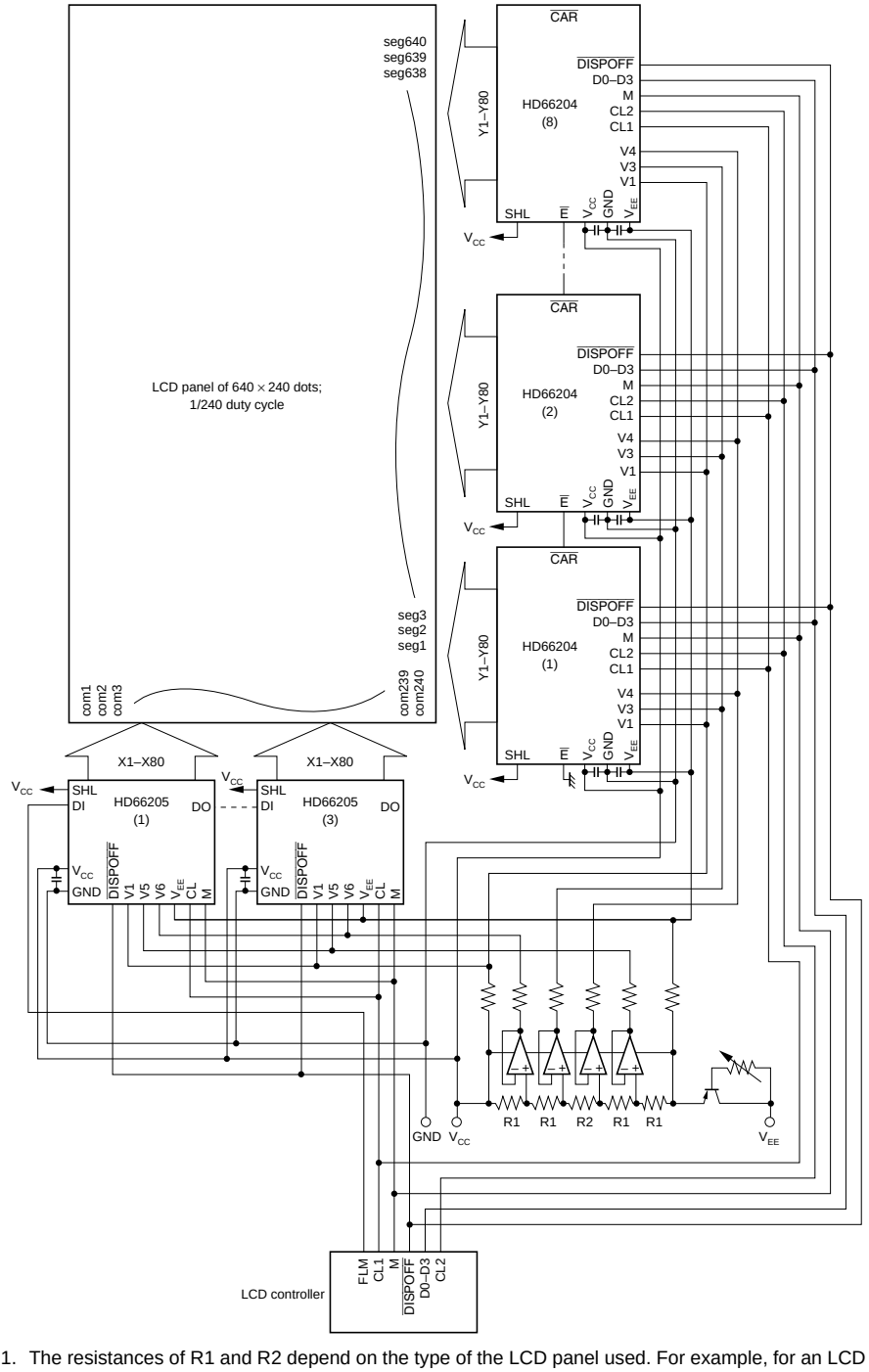


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66204 and HD61104

Operation Timing



Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-μF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$.
3. Applies to pins V1, V3, and V4.
4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins: 1. CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$
2. $\overline{CAR}$
3. Y1–Y80, V1, V3, V4
4. V1, V3, V4

Notes: 1. Indicates the resistance between one pin from Y1–Y80 and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.
V_{CC} – GND = 28 V
V1, V3 = $V_{CC} - \{2/10(V_{CC} - V_{EE})\}$
V4 = $V_{EE} + \{2/10(V_{CC} - V_{EE})\}$
V1 and V3 should be near V_{CC} level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

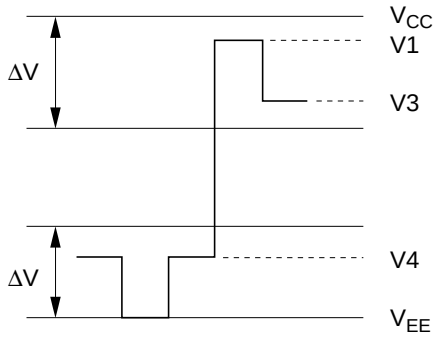


Figure 6 Relation between Driver Output Waveform and Level Voltages

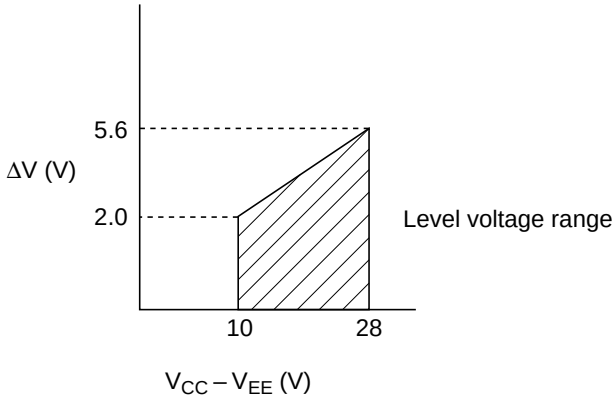


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	*1	ns	1
Clock fall time	t_f	CL1, CL2	—	*1	ns	1
Data setup time	t_{DS}	D0–D3, CL2	20	—	ns	
Data hold time	t_{DH}	D0–D3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	
Disp off ($\overline{DISPOFF}$) rise time	t_{r2}	$\overline{DISPOFF}$	—	200	ns	
Disp off ($\overline{DISPOFF}$) fall time	t_{f2}	$\overline{DISPOFF}$	—	200	ns	

AC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	*1	ns	1
Clock fall time	t_f	CL1, CL2	—	*1	ns	1
Data setup time	t_{DS}	D0–D3, CL2	50	—	ns	
Data hold time	t_{DH}	D0–D3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	
Disp off ($\overline{DISPOFF}$) rise time	t_{r2}	$\overline{DISPOFF}$	—	200	ns	
Disp off ($\overline{DISPOFF}$) fall time	t_{f2}	$\overline{DISPOFF}$	—	200	ns	

Notes: 1. t_r, $t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 50$ ns
2. The load circuit shown in figure 8 is connected.

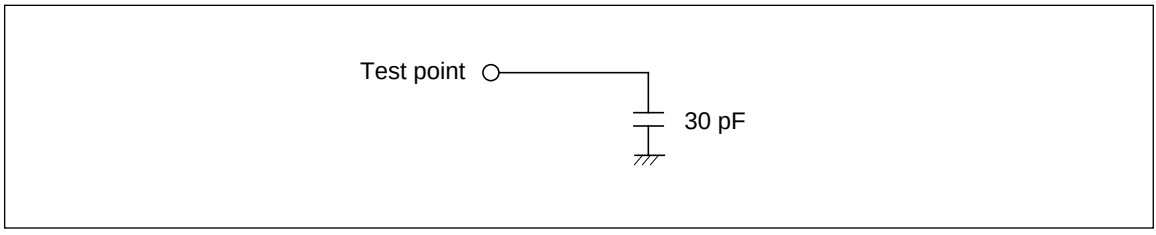


Figure 8 Load Circuit

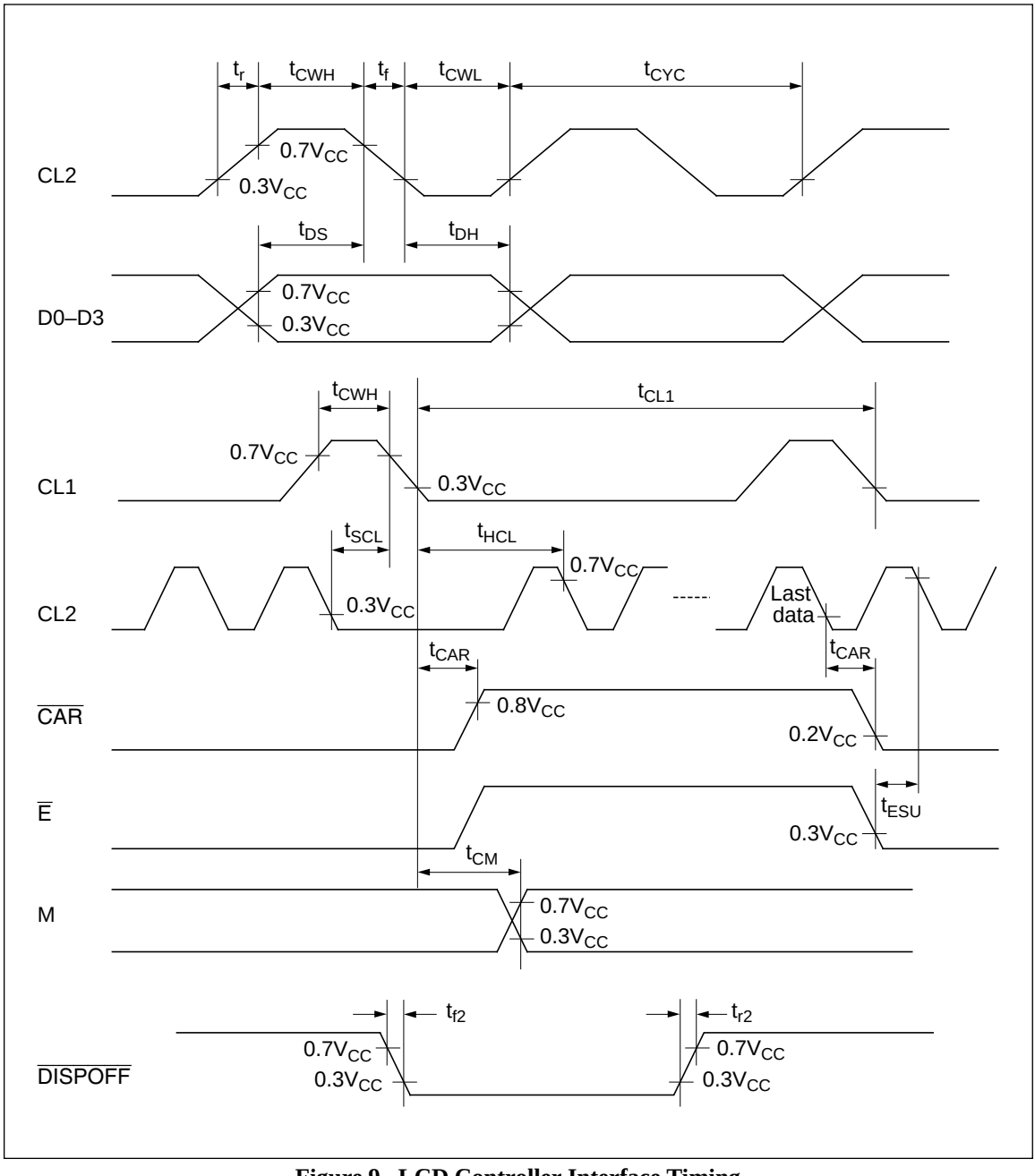


Figure 9 LCD Controller Interface Timing

HD66205

(Dot Matrix Liquid Crystal Graphic Display
Common Driver with 80-Channel Outputs)

HITACHI

Description

The HD66205F/HD66205FL/HD66205TF/HD66205TFL/HD66205T/HD66205TL, the row LCD driver, features low output impedance and as many as 80 LCD outputs powered by 80 internal LCD drive circuits, and can drive a large liquid crystal graphic display. Because this device is fabricated by the CMOS process, it is suitable for battery-driven portable equipment, which fully utilizes the low power dissipation of liquid crystal elements. The HD66205 has a complete line-up: the HD66205F, a standard device powered by 5 V ± 10%; the HD66205FL, a 2.7 to 5.5 V, low power dissipation device; the HD66205TF and HD66205TFL, thin film package devices each powered by 5 V ± 10% and 2.7 to 5.5 V; and the HD66205T, tape carrier package (TCP) devices powered by 2.7 to 5.5 V, respectively.

Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10 to 28 V
- Display off function
- Internal 80-bit shift register
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Hitachi semiconductor

Ordering Information 1 (Flat Package and Die Shipment)

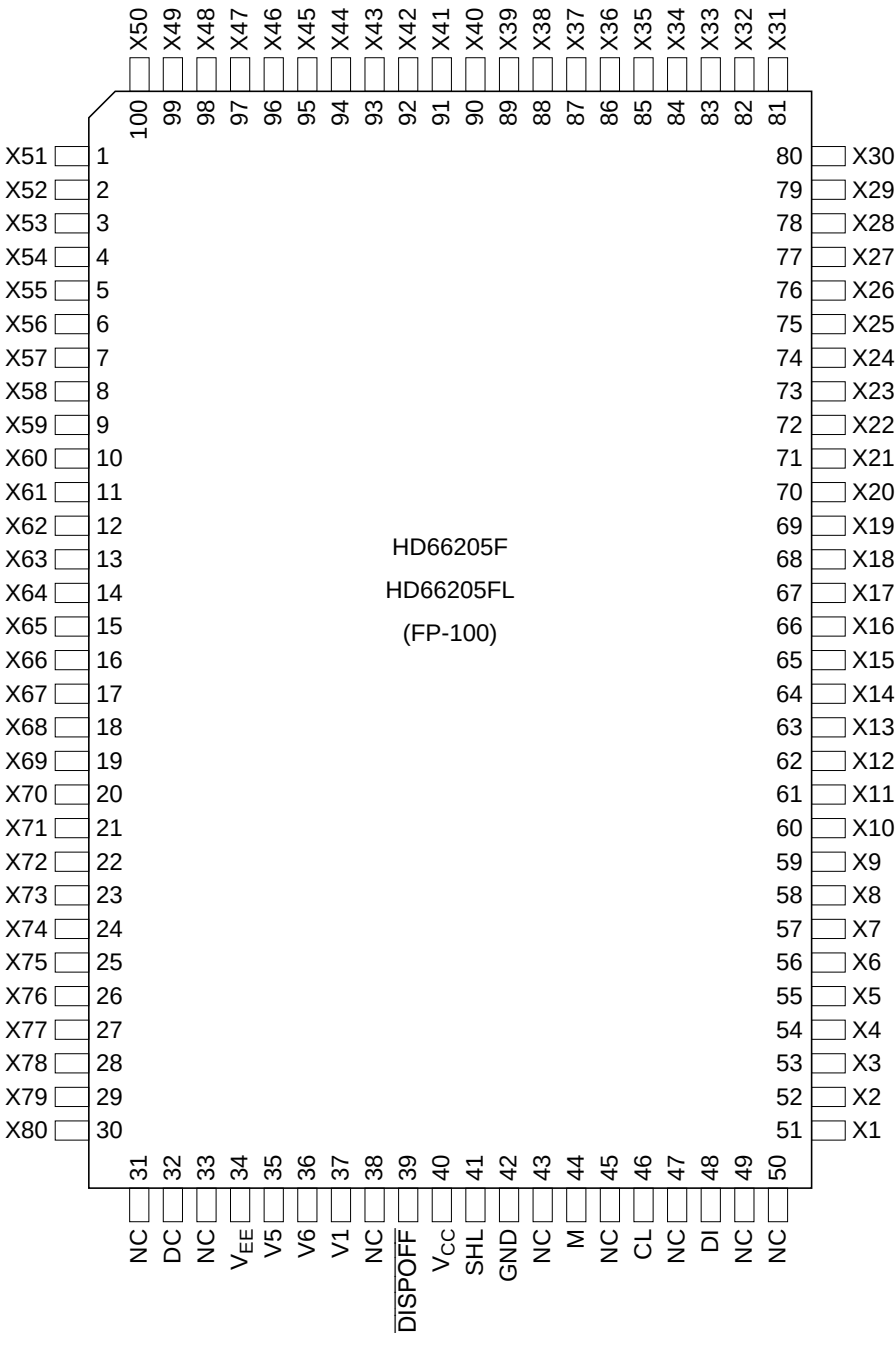
Type No.	Voltage Range	Package
HD66205F	5 V ± 10%	100-pin plastic QFP (FP-100)
HD66205FL	2.7 to 5.5 V	100-pin plastic QFP (FP-100)
HD66205TF	5 V ± 10%	100-pin thin plastic QFP (TFP-100)
HD66205TFL	2.7 to 5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66205	5 V ± 10%	Chip
HCD66205L	2.7 to 5.5 V	Chip

Ordering Information 2 (Tape Carrier Package)

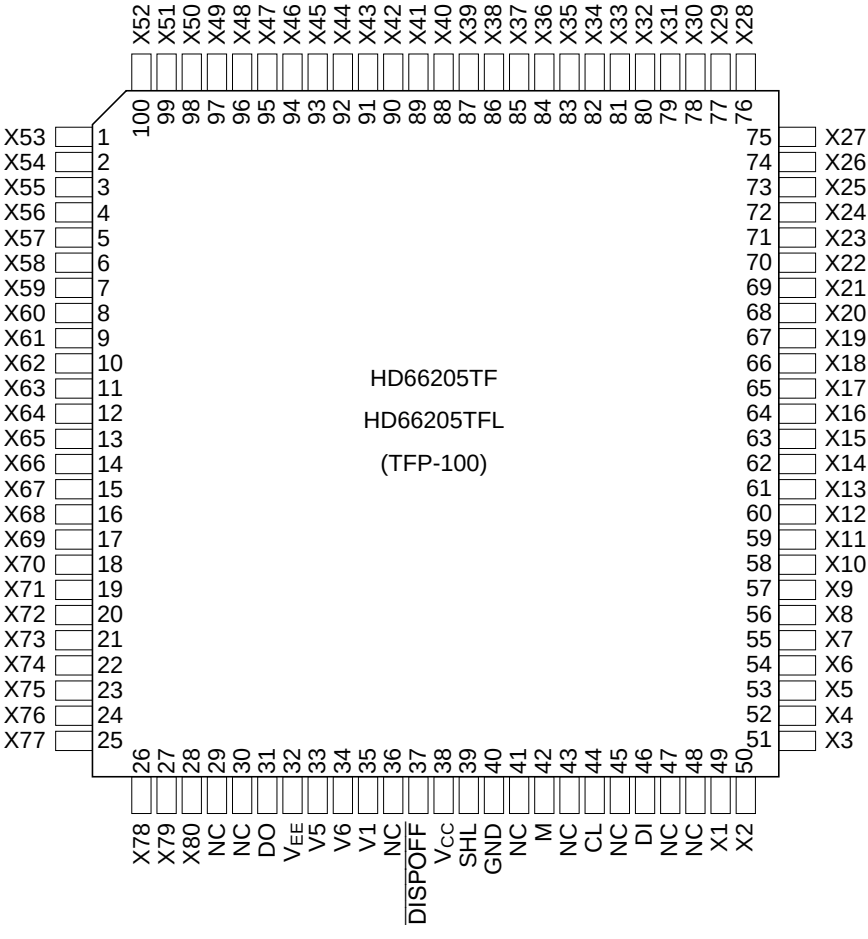
Type No.	Voltage Range	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66205TA1	2.7 to 5.5V	0.15mm	0.80mm	4 sprocket holes
HD66205TA2	2.7 to 5.5V	0.18mm	0.80mm	4 sprocket holes
HD66205TA3	2.7 to 5.5V	0.20mm	0.80mm	4 sprocket holes
HD66205TA6	2.7 to 5.5V	0.22mm	0.70mm	4 sprocket holes
HD66205TA7	2.7 to 5.5V	0.25mm	0.70mm	4 sprocket holes
HD66205TA9L	2.7 to 5.5V	0.22mm	0.70mm	3 sprocket holes

Notes: 1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75mm.
4. Tape film is Upirex (a trademark of Ube industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in “The Information of TCP.”

Pin Arrangement



(Top view)


X52 X51 X50 X49 X48 X47 X46 X45 X44 X43 X42 X41 X40 X39 X38 X37 X36 X35 X34 X33 X32 X31 X30 X29 X28
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
X53 1
X54 2
X55 3
X56 4
X57 5
X58 6
X59 7
X60 8
X61 9
X62 10
X63 11
X64 12
X65 13
X66 14
X67 15
X68 16
X69 17
X70 18
X71 19
X72 20
X73 21
X74 22
X75 23
X76 24
X77 25
75 X27
74 X26
73 X25
72 X24
71 X23
70 X22
69 X21
68 X20
67 X19
66 X18
65 X17
64 X16
63 X15
62 X14
61 X13
60 X12
59 X11
58 X10
57 X9
56 X8
55 X7
54 X6
53 X5
52 X4
51 X3
HD66205TF
HD66205TFL
(TFP-100)
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
X78 X79 X80 NC NC DO VEE V5 V6 V1 NC DISPOFF VCC SHL GND NC M NC CL NC DI NC NC X1 X2

(Top view)

Pin Description

Symbol	Pin No. (FP-100/TFP-100)	Pin Name	Input/Output	Classification
V_{CC}	40/38	V_{CC}	—	Power supply
GND	42/40	GND	—	Power supply
V_{EE}	34/32	V_{EE}	—	Power supply
V1	37/35	V1	Input	Power supply
V5	35/33	V5	Input	Power supply
V6	36/34	V6	Input	Power supply
CL	46/44	Clock	Input	Control signal
M	44/42	M	Input	Control signal
DI	48/46	Data in	Input	Control signal
DO	32/31	Data out	Output	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{\text{DISPOFF}}$	39/37	Display off	Input	Control signal
X_1–X_{80}	51–100, 1–30/ 1–28, 49–100	X1–X80	Output	LCD drive output
NC	31, 33, 38, 43, 45, 47, 49, 50/ 29, 30, 36, 41, 43, 45, 47, 48	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V5, V6: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V5 and V6 are non-selected levels. See figure 1.

Control Signal

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts display data input via the DI pin.

M: Changes LCD drive outputs to AC.

DI: Inputs display data. DI of the first HD66205 must be connected to an LCD controller, and those of the other HD66205s must be connected to DI of the previous HD66205.

DO: Outputs display data. DO of the last HD66205 must be open, and those of the other HD66205s must be connected to DI of the next HD66205.

SHL: Selects the data shiftt direction for the shift register. See figure 2.

$\overline{\text{DISPOFF}}$: A low $\overline{\text{DISPOFF}}$ sets LCD drive outputs X1–X80 to V1 level.

LCD Drive Output

X1–X80: Each X outputs one of the four voltage levels V1, V5, V6, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

Other

NC: Must be open.

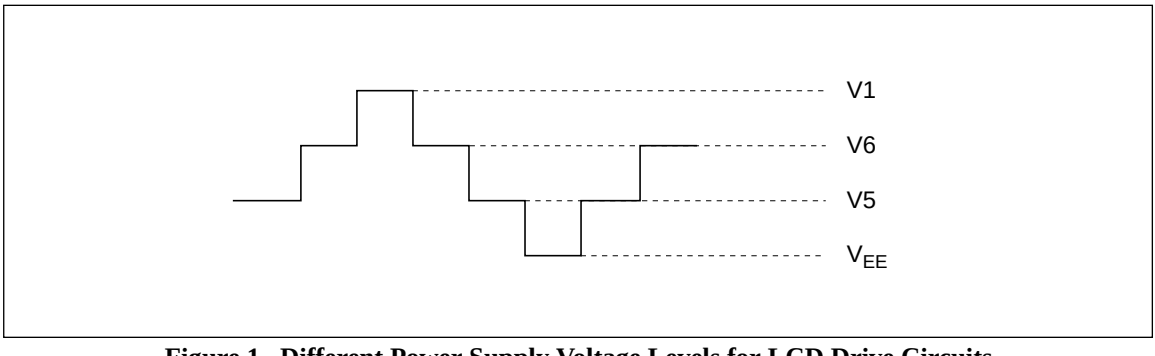


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL level	Data shift direction	Common signal scan direction
Low	DI → SR1 → SR2 → SR80	X1 → X80
High	DI → SR80 → SR79 → SR1	X80 → X1

Figure 2 Selection of Display Data Shift Direction

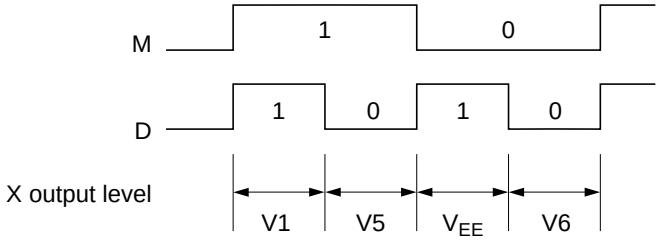


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V5, V6, and V_{EE}, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the shift register.

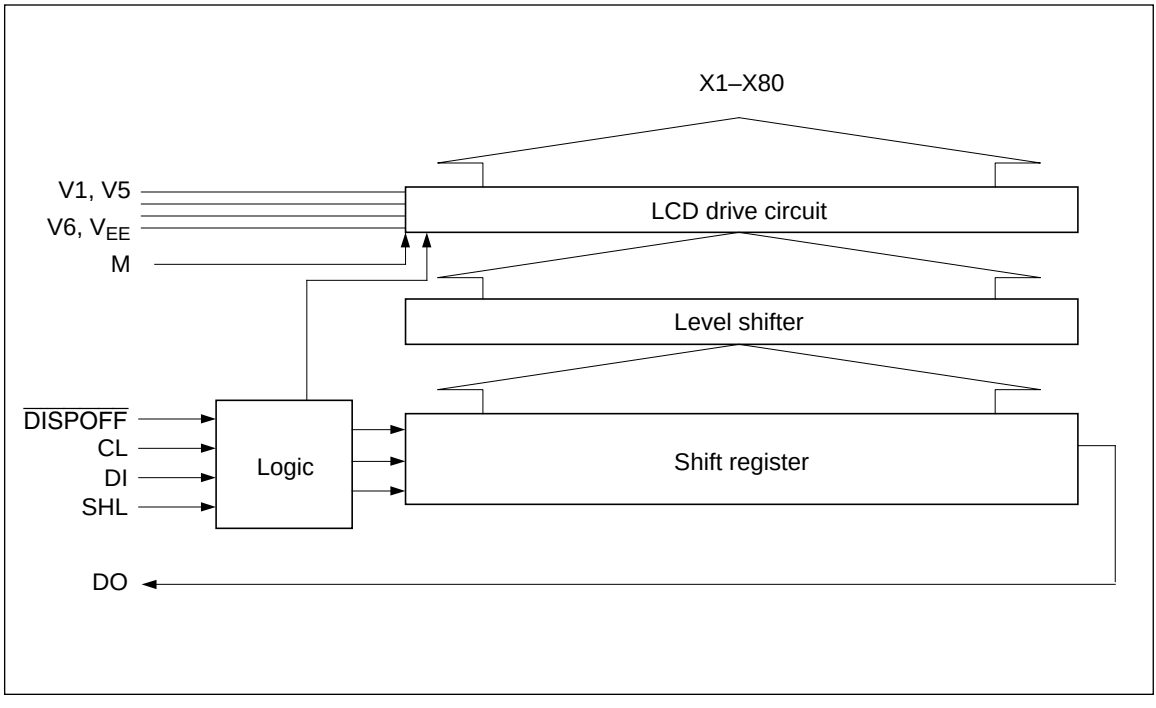
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Shift Register

The 80-bit shift register shifts data input via the DI pin by one bit, and the one bit of shifted-out data is output from the DO pin. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse.

Block Diagram



Comparison of the HD66205 with the HD61105

Item	HD66205	HD61105
Display off function	Provided	Not provided
LCD drive voltage range	10 to 28 V	10 to 26 V
Shift clock phase selection function	Not provided	Provided (FCS pin)
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V5, V6 (V2 level is the same as V_{EE} level)	V1, V2, V5, V6

SHL level	Data shift direction	Common signal scan direction
Low	DI → SR1 → SR2 → SR80	X1 → X80
High	DI → SR80 → SR79 → SR1	X80 → X1

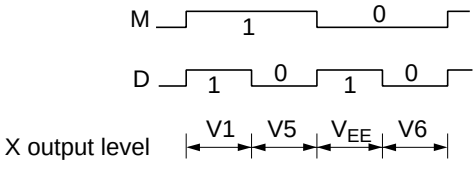
HD66205

SHL level	Data shift direction	Common signal scan direction
Low	DI → SR80 → SR79 → SR1	X80 → X1
High	DI → SR1 → SR2 → SR80	X1 → X80

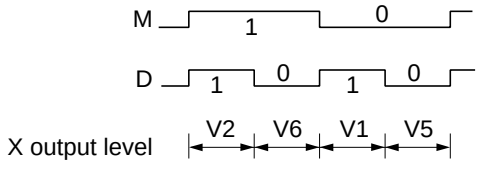
HD61105

Note the exact reverse relation for the two devices.

Figure 4 Relation between SHL and LCD Output Destinations for the HD66205 and HD61105



HD66205



HD61105

Figure 5 Relation between LCD Output Levels, M, and Data for the HD66205 and HD61105

Operation Timing

Figure 6 shows the operation timing for the Application Example.

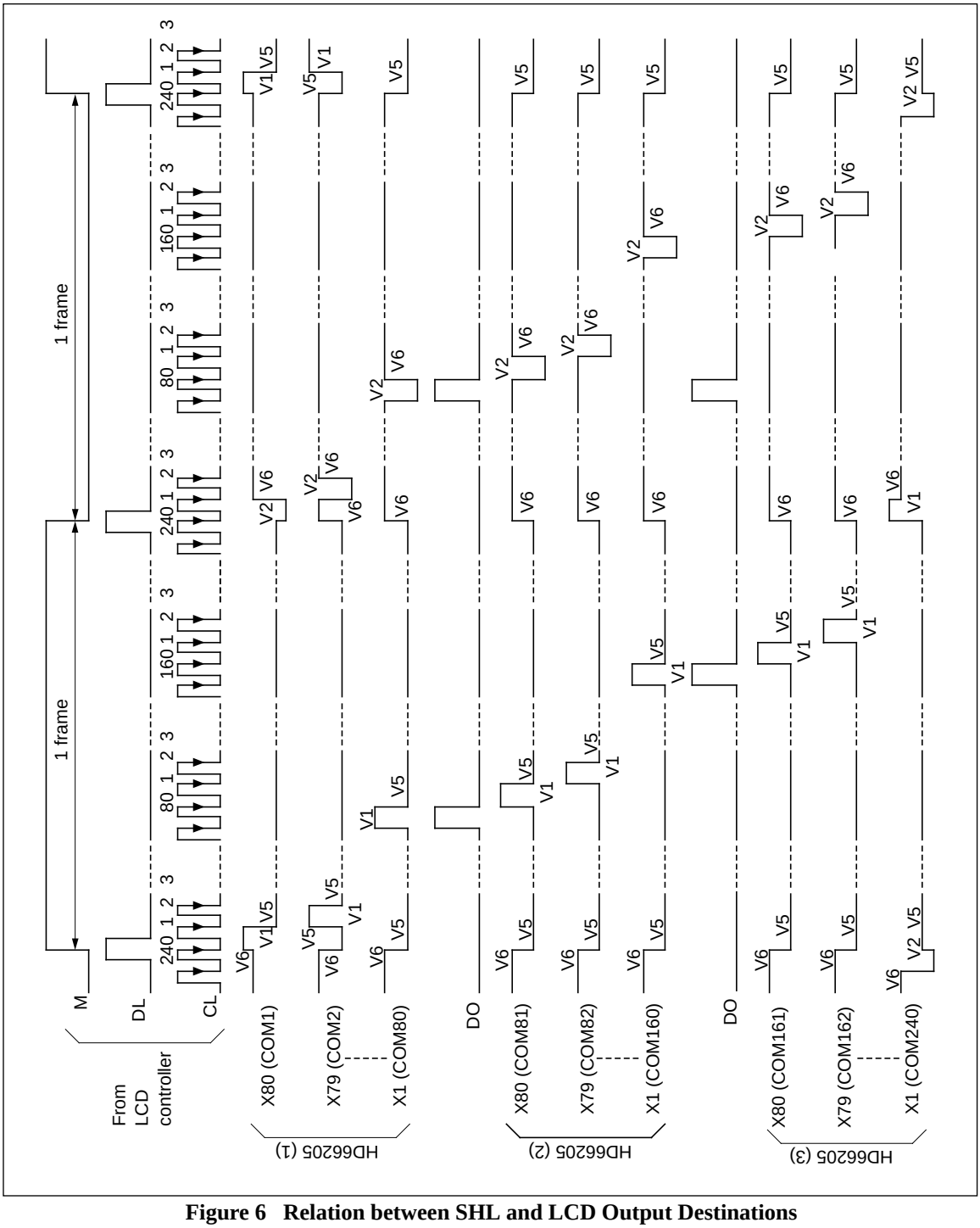
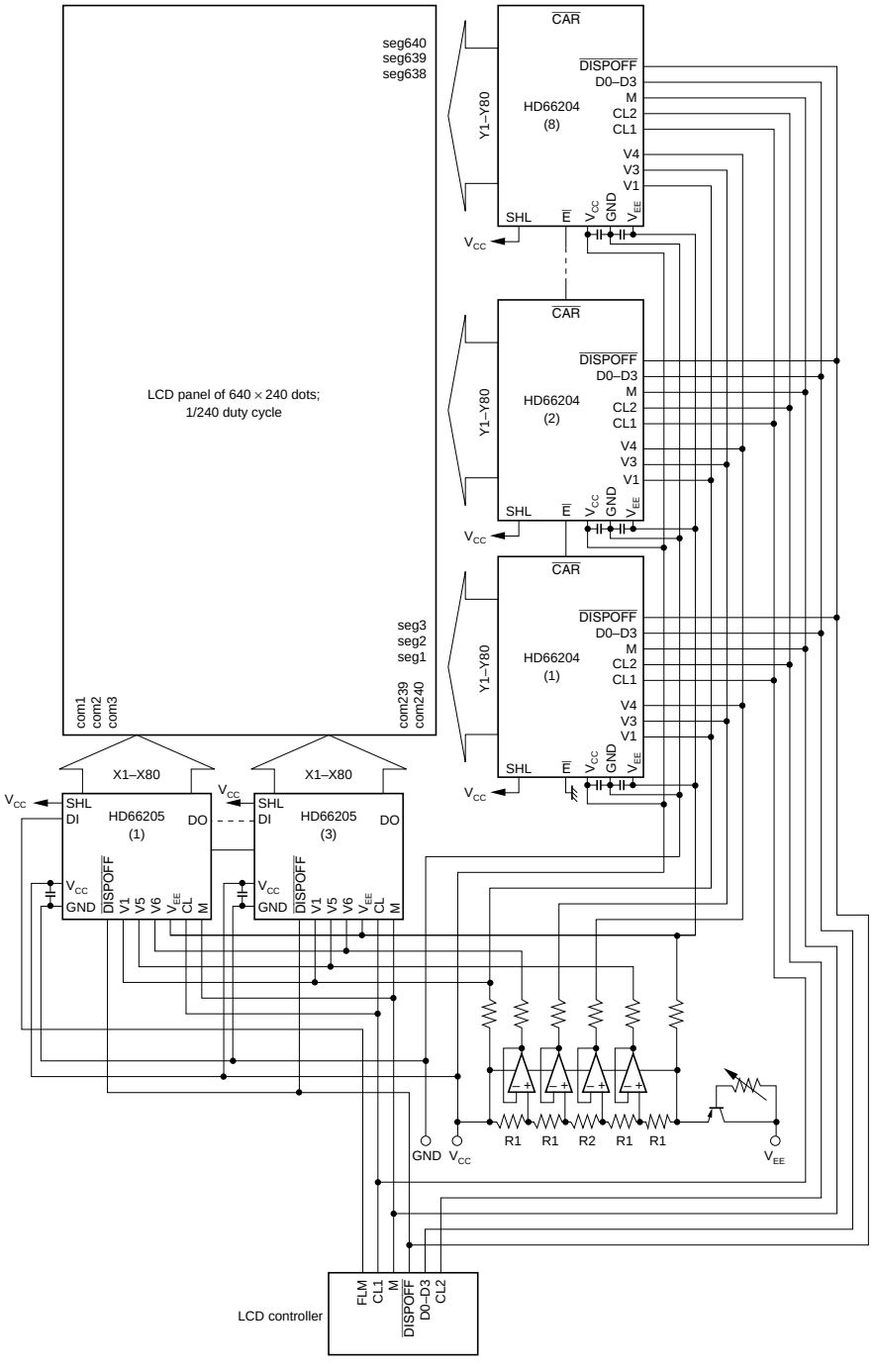


Figure 6 Relation between SHL and LCD Output Destinations

Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	4

Notes: 1. The reference point is GND (0 V).
2. Applies to pins CL, M, SHL, DI, $\overline{\text{DISPOFF}}$.
3. Applies to pins V1, V5, and V6.
4. –40 to +125°C for TCP devices.
5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66205F/HD66205TF (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	2.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	100	µA	f_{CL} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2

Pins and notes on next page.

DC Characteristics for the HD66205FL/HD66205TFL/HD66205T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	2.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	100	µA	f_{CL} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V	2
Current consumption 2	I_{EE}	—	—	250	µA	Same as above	2

Pins: 1. CL, M, SHL, DI, $\overline{\text{DISPOFF}}$
2. DO
3. X1–X80, V1, V5, V6
4. V1, V5, V6

Notes: 1. Indicates the resistance between one pin from X1–X80 and another pin from V1, V5, V6, and V_{EE}, when load current is applied to the X pin; defined under the following conditions.

$V_{CC} - V_{EE}$= 28 V
$V1, V6 = V_{CC} - \{1/10(V_{CC} - V_{EE})\}$
$V5 = V_{EE} + \{1/10(V_{CC} - V_{EE})\}$

V1 and V6 should be near V_{CC} level, and V5 should be near V_{EE} level (figure 7). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 8).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

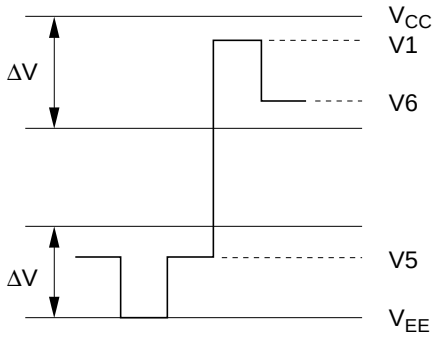


Figure 7 Relation between Driver Output Waveform and Level Voltages

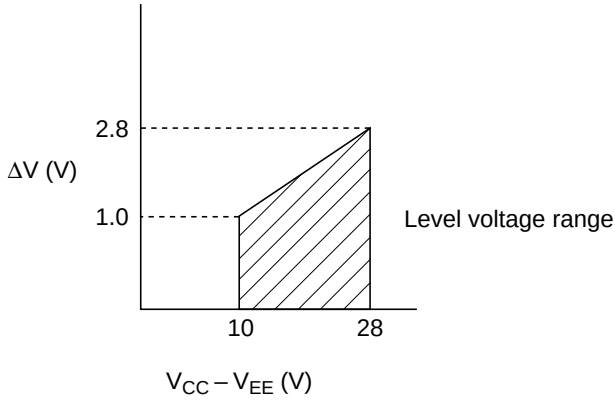


Figure 8 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66205F/HD66205TF (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Note
Clock cycle time	t_{CYC}	CL	10	—	µs	
Clock high-level width	t_{CWH}	CL	50	—	ns	
Clock low-level width	t_{CWL}	CL	1.0	—	µs	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, CL	100	—	ns	
Data hold time	t_{DH}	DI, CL	100	—	ns	
Data output delay time	t_{DD}	DO, CL	—	3.0	µs	1
Data output hold time	t_{DHW}	DO, CL	100	—	ns	
Disp off ($\overline{\text{DISPOFF}}$) rise time	t_{r2}	$\overline{\text{DISPOFF}}$	—	200	ns	
Disp off ($\overline{\text{DISPOFF}}$) fall time	t_{f2}	$\overline{\text{DISPOFF}}$	—	200	ns	

AC Characteristics for the HD66205FL/HD66205TFL/HD66205T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Note
Clock cycle time	t_{CYC}	CL	10	—	µs	
Clock high-level width	t_{CWH}	CL	80	—	ns	
Clock low-level width	t_{CWL}	CL	1.0	—	µs	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, CL	100	—	ns	
Data hold time	t_{DH}	DI, CL	100	—	ns	
Data output delay time	t_{DD}	DO, CL	—	7.0	µs	1
Data output hold time	t_{DHW}	DO, CL	100	—	ns	
Disp off ($\overline{\text{DISPOFF}}$) rise time	t_{r2}	$\overline{\text{DISPOFF}}$	—	200	ns	
Disp off ($\overline{\text{DISPOFF}}$) fall time	t_{f2}	$\overline{\text{DISPOFF}}$	—	200	ns	

Note: 1. The load circuit shown in figure 9 is connected.

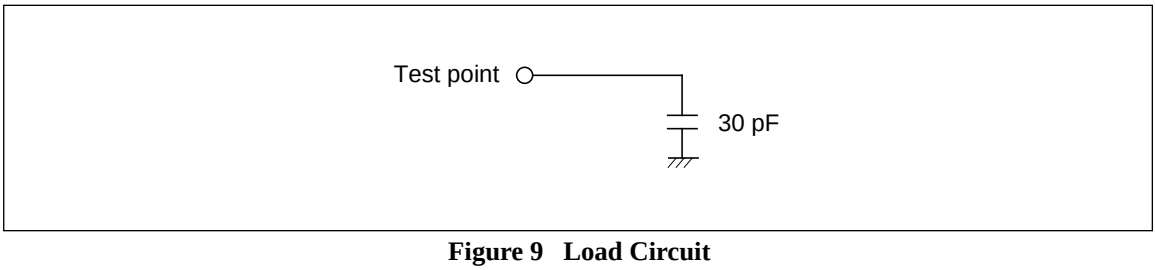


Figure 9 Load Circuit

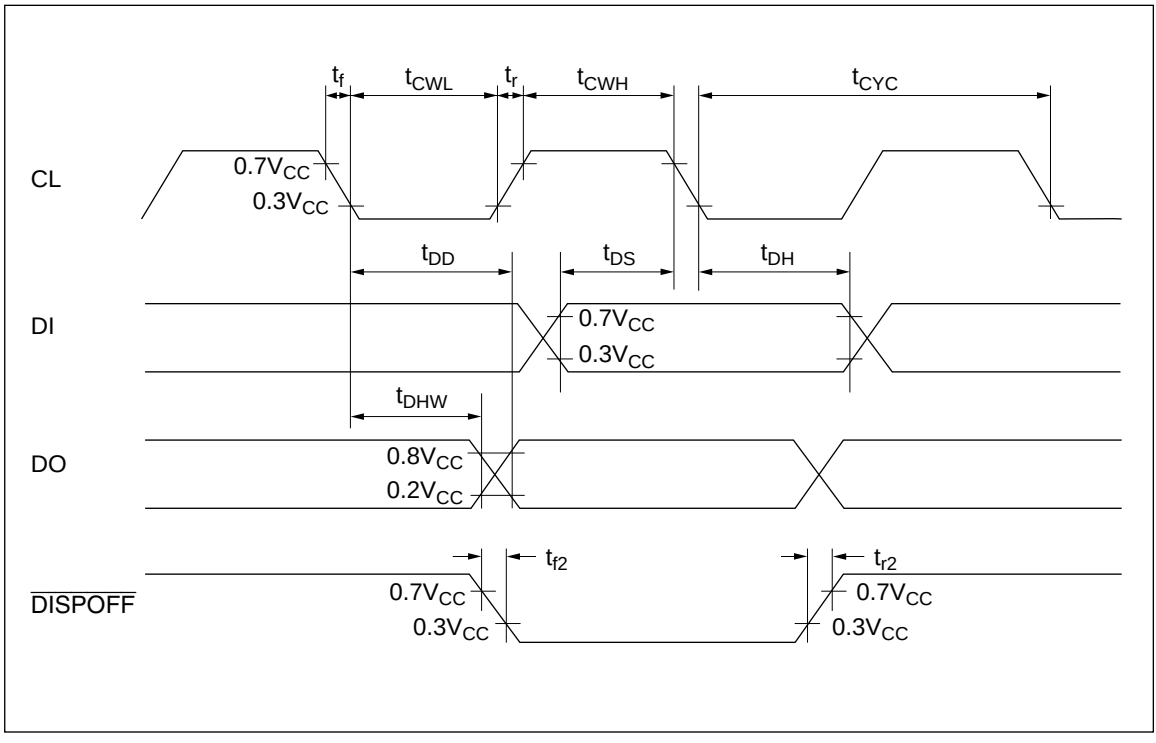


Figure 10 LCD Controller Interface Timing

HD66214T (Micro-TAB)

(80-Channel Column Driver in Micro-TCP)

HITACHI

Description

The HD66214T, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66214, packaged in an 8-mm-wide micro-tape carrier package (micro-TCP), enables a compact LCD system with a narrower frame (peripheral areas for LCD drivers)—about half as large as that os an existing system. The HD66214T is a low power dissipation device powered by 2.7 to 5.5 V suitable for battery-driven portable equipment such as notebook personal computers and palm-top personal computers.

Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10 to 28 V
- High clock speed
  - — 8 MHz max under 5-V operation
  - — 4 MHz max under 3-V operation
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850
- 98–pin TCP

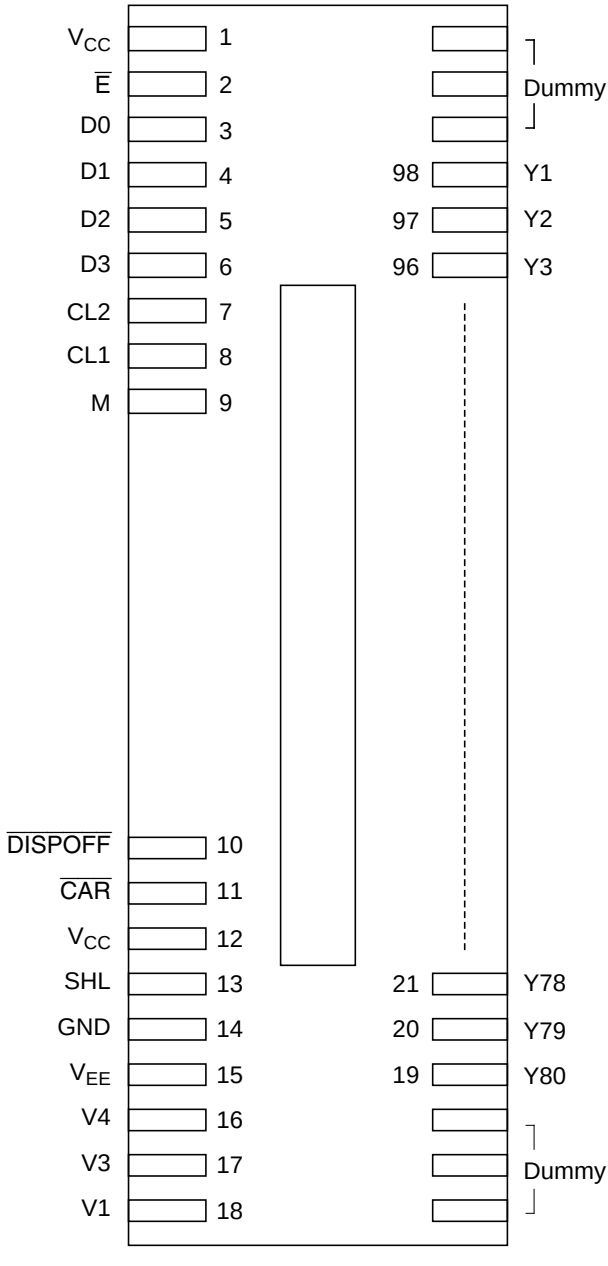
Ordering Information

Type No.	Voltage Range	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66214TA1	2.7 to 5.5 V	0.15 mm	0.80 mm	3 sprocket holes
HD66214TA2	2.7 to 5.5 V	0.18 mm	0.80 mm	3 sprocket holes
HD66214TA3	2.7 to 5.5 V	0.20 mm	0.80 mm	3 sprocket holes
HD66214TA6	2.7 to 5.5 V	0.20 mm	0.45 mm	3 sprocket holes
HD66214TA9L	2.7 to 5.5 V	0.22 mm	0.45 mm	2 sprocket holes

Notes: 1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75 mm.
4. Tape film is Upirex (a trademark of Ube Industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in “The Information of TCP. ”

Hitachi semiconductor

Pin Arrangement



Top view

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	1, 12	V_{CC}	—	Power supply
GND	14	GND	—	Power supply
V_{EE}	15	V_{EE}	—	Power supply
V1	18	V1	Input	Power supply
V3	17	V3	Input	Power supply
V4	16	V4	Input	Power supply
CL1	8	Clock 1	Input	Control signal
CL2	7	Clock 2	Input	Control signal
M	9	M	Input	Control signal
D_0–D_3	3 to 6	Data 0 to data 3	Input	Control signal
SHL	13	Shift left	Input	Control signal
$\overline{E}$	2	Enable	Input	Control signal
$\overline{CAR}$	11	Carry	Output	Control signal
$\overline{DISPOFF}$	10	Display off	Input	Control signal
Y1–Y80	19 to 98	Y1 to Y80	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D0–D3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D0–D3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66214 if HD66214s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISPOFF}$ sets LCD drive outputs Y1–Y80 to V1 level.

LCD Drive Output

Y1–Y80: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

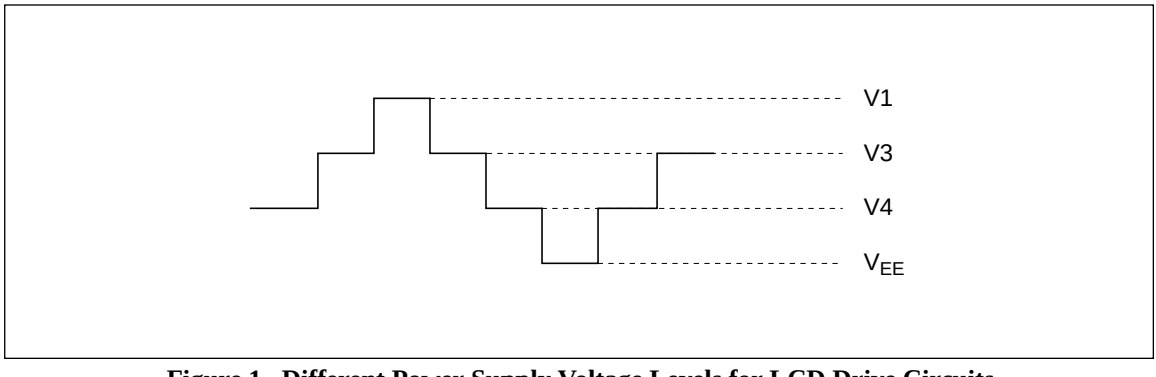


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

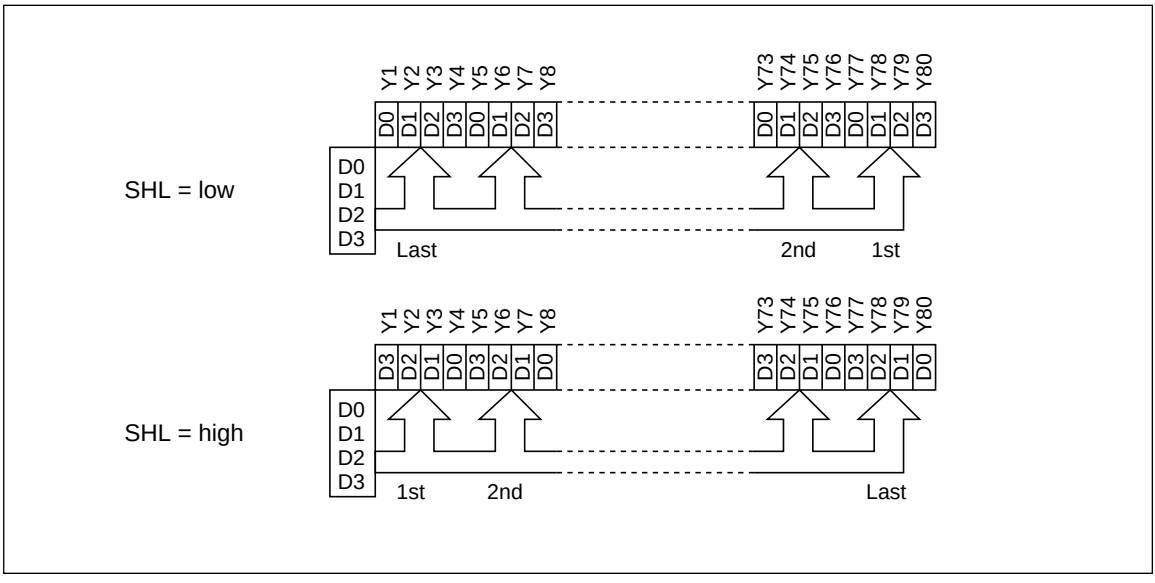


Figure 2 Selection of Destinations of Display Data Output

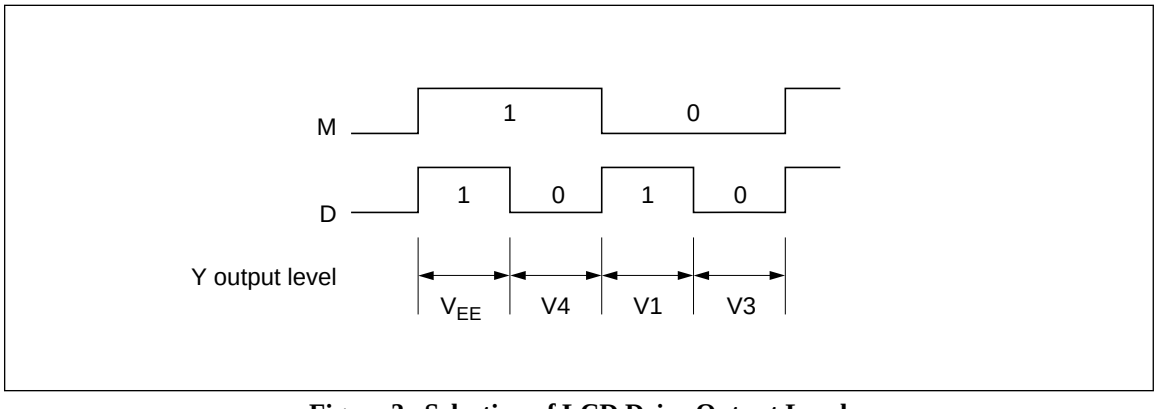


Figure 3 Selection of LCD Drive Output Level

Block Functions

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D0 to D3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

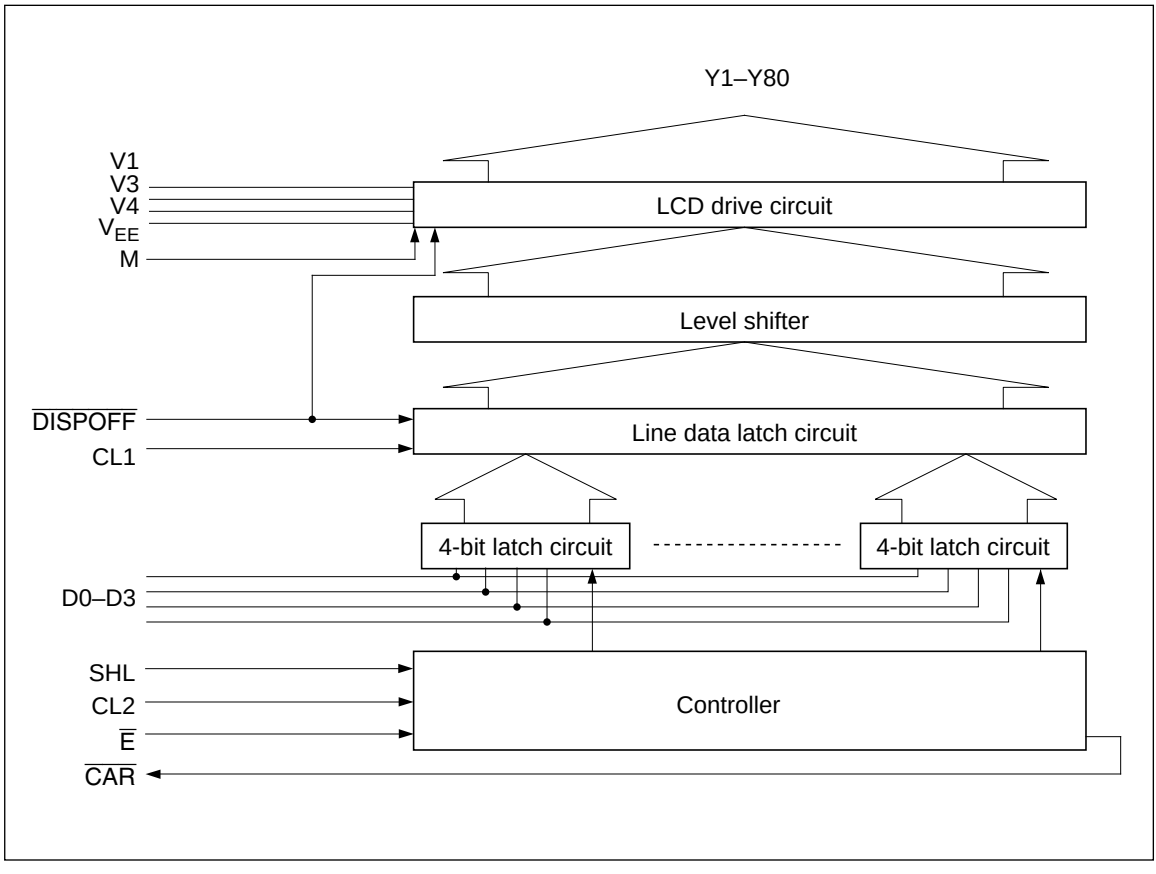
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

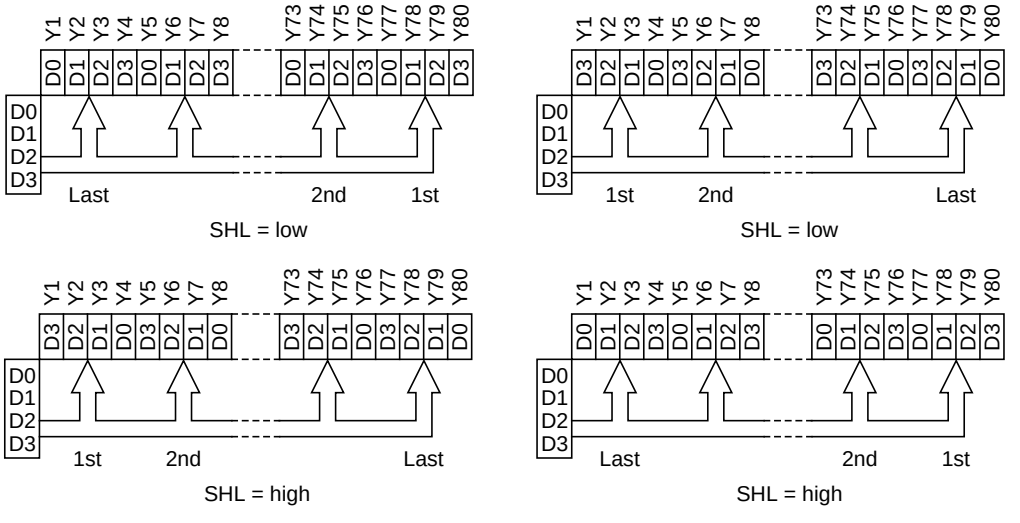
The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and V_{EE}, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



Comparison of the HD66214 with the HD61104

Item	HD66214	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10 to 28 V	10 to 26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as V_{EE} level)	V1, V2, V3, V4
Storage temperature	–40 to 125°C	–55 to 125°C
Package	TCP (tape carrier package)	QFP (quad flat package)



Note the exact reverse relation for the two devices.

Figure 4 Relation between SHL and LCD Output Destinations for the HD66214 and HD61104

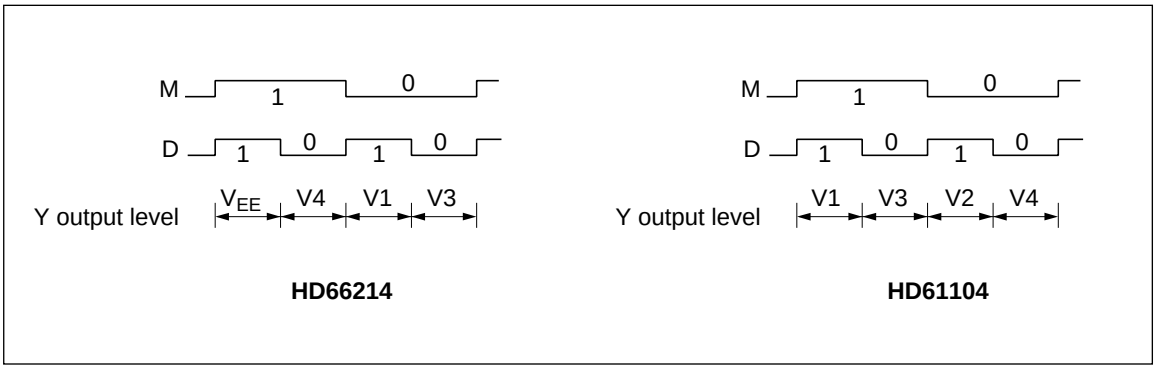
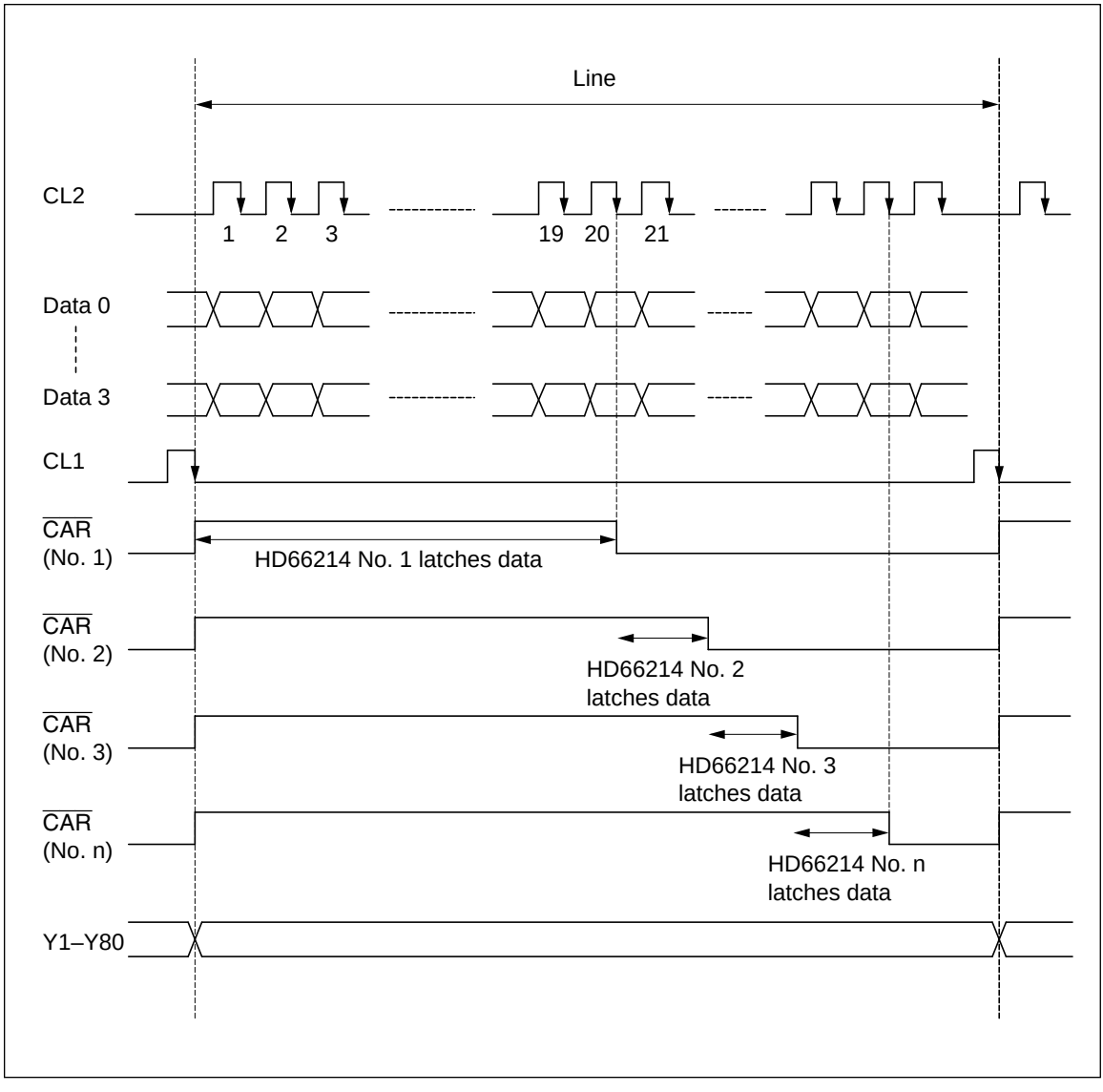
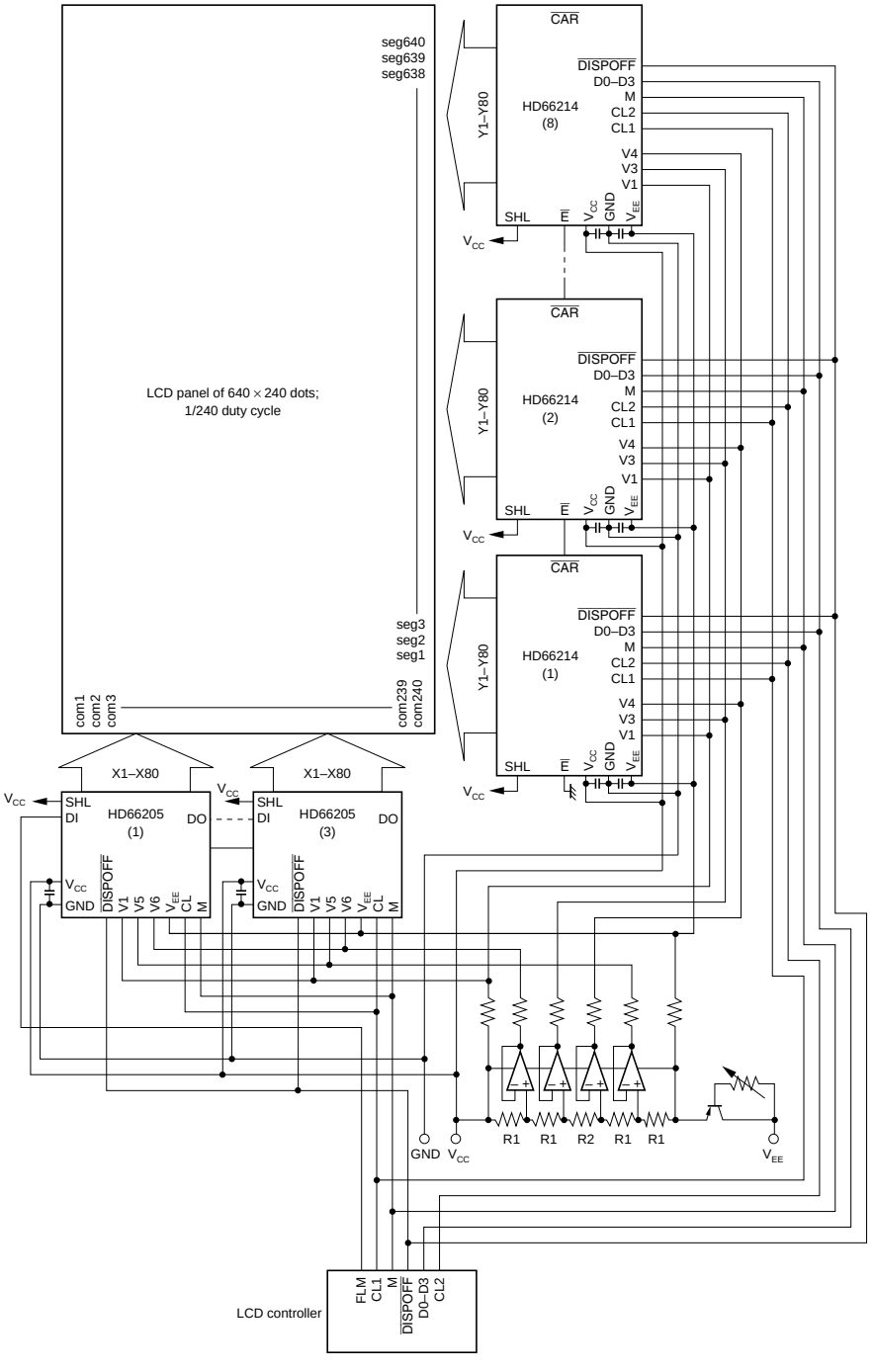


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66214 and HD61104

Operation Timing



Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D0–D3, $\overline{DISPOFF}$.
3. Applies to pins V1, V3, and V4.
4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66214T (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} – V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66214T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.7 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins: 1. CL1, CL2, M, SHL, $\overline{E}$, D0–D3, $\overline{DISPOFF}$
2. $\overline{CAR}$
3. Y1–Y80, V1, V3, V4
4. V1, V3, V4

Notes: 1. Indicates the resistance between one pin from Y1–Y80 and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.
V_{CC} – GND = 28 V
V1, V3 = $V_{CC} - \{2/10(V_{CC} - V_{EE})\}$
V4 = $V_{EE} + \{2/10(V_{CC} - V_{EE})\}$
V1 and V3 should be near Vcc level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

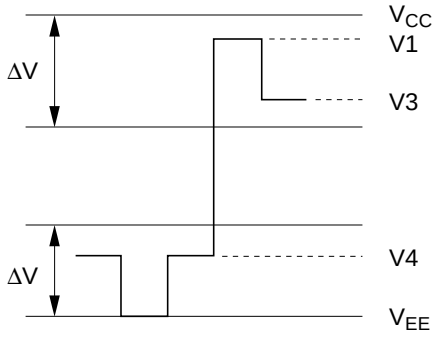


Figure 6 Relation between Driver Output Waveform and Level Voltages

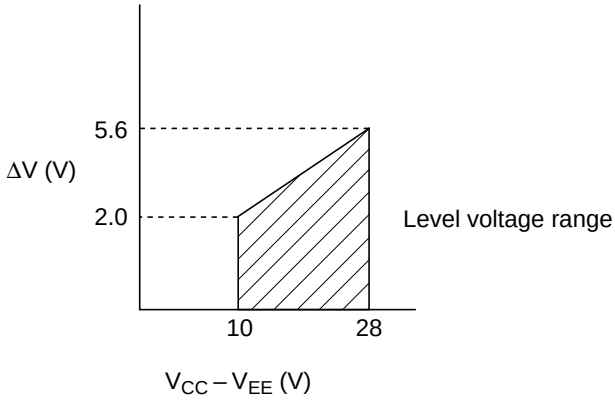


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66214T (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	*1	ns	1
Clock fall time	t_f	CL1, CL2	—	*1	ns	1
Data setup time	t_{DS}	D0–D3, CL2	20	—	ns	
Data hold time	t_{DH}	D0–D3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66214T (V_{CC} = 2.7 to 5.5 V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	120	—	ns	
Clock rise time	t_r	CL1, CL2	—	*1	ns	1
Clock fall time	t_f	CL1, CL2	—	*1	ns	1
Data setup time	t_{DS}	D0–D3, CL2	50	—	ns	
Data hold time	t_{DH}	D0–D3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. t_r, $t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 50$ ns
2. The load circuit shown in figure 8 is connected.

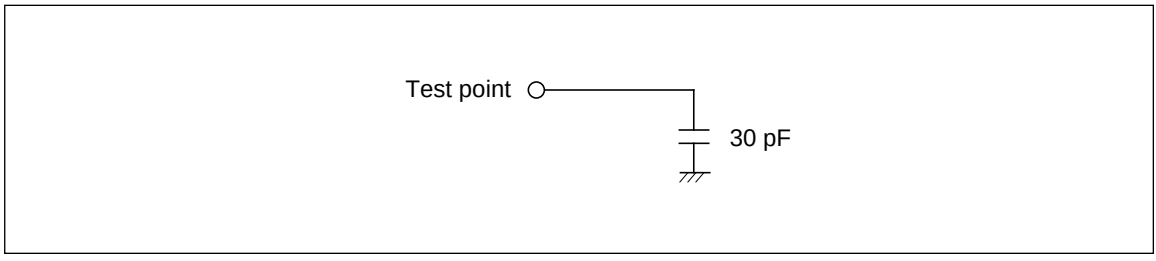


Figure 8 Load Circuit

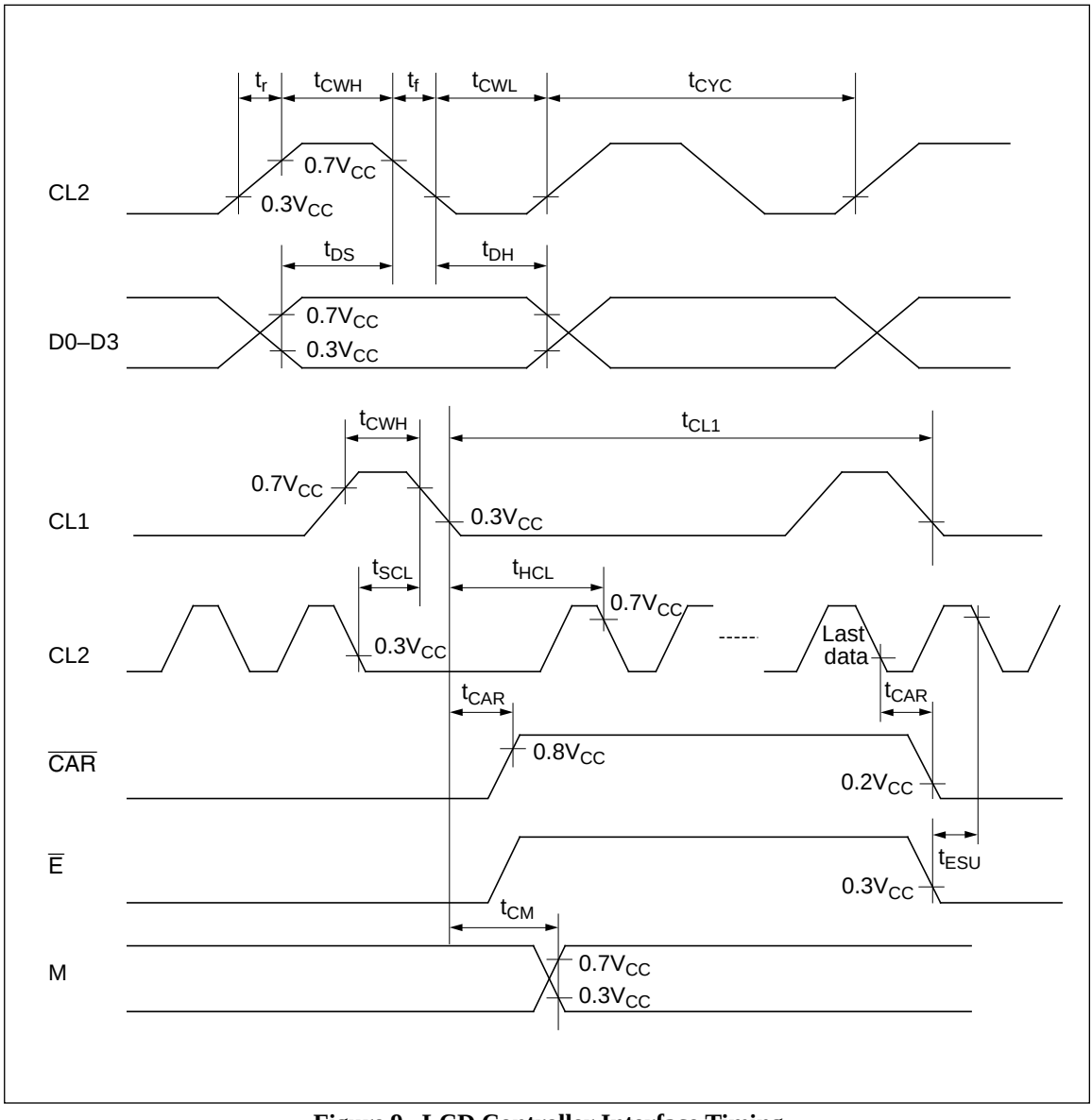


Figure 9 LCD Controller Interface Timing

HD66224T

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

HITACHI

Description

The HD66224T is a column driver for dot matrix liquid crystal graphic display system. It has 80 liquid crystal drive circuits and can drive large LCDs. The column driver latches parallel data for display (4/8 bit parallel) from the controller, then generates a drive signal and selects the proper LCD drive voltage. A built-in standby function that allows all internal drivers except one to be placed in standby mode (IST) lowers device power consumption. The column driver package is a 7.5-mm wide ultra-small tape carrier package (TCP), allowing designs using half the frame area of conventional displays.

The column driver can be used in a wide range of battery-powered designs because its logic power supply can operate with an input voltage ranging from 2.5 to 5.5 V.

Features

- Display duty cycle: 1/64 to 1/240
- Number of liquid crystal drive circuits: 80
- Parallel data transfer: 4/8 bits
- High voltage: Drive voltage 10–28 V (absolute maximum rating 30 V)
- High-speed operation: Maximum clock speed 8 MHz (for 5 V) or 6.5 MHz (for 2.5 V)
- Logic power supply voltage: 2.5–5.5 V
- Built-in display off function
- Built-in automatic generation function for chip-enable signal
- Built-in standby function
- 107-pin 35 mm TCP

Ordering Information

Type No.	Data Input	Input Format	Outer Lead Pitch (µm)
HD66224TA1	4-bit input	Straight	210
HD66224TA2	4-bit input	Straight	200
HD66224TB0	8-bit input	Straight	200

Note: The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Internal Block Diagram

Figure 1 is a block diagram of the HD66224T.

Liquid-Crystal Drive Circuit

The LCD drive circuit selects from four available voltage levels (V_1, V_3, V_4, and V_{EE}) based on the combination of the data of latch circuit 2 and input to pin M. The circuit outputs the selected voltage to the LCDs.

Level Shifter

The level shifter circuit raises the voltage of the logic power-supply voltage to the level used for driving the LCDs.

Latch Circuit 2

The 80-bit latch circuit 2 latches data from latch circuit 1 on the falling edge of clock CL1 and outputs the data to the level shifter circuit.

Latch Circuit 1

Latch circuit 1 consists of 4/8-bit parallel data latches that store input data D_0 to D_7 when signaled by the shift register.

Control Circuit

The control circuit generates signals that fetch the data for input to latch circuit 1.

Data Rearrange Circuit

The data rearrange circuit performs left to right (SHL) inversion on data D_0 to D_7.

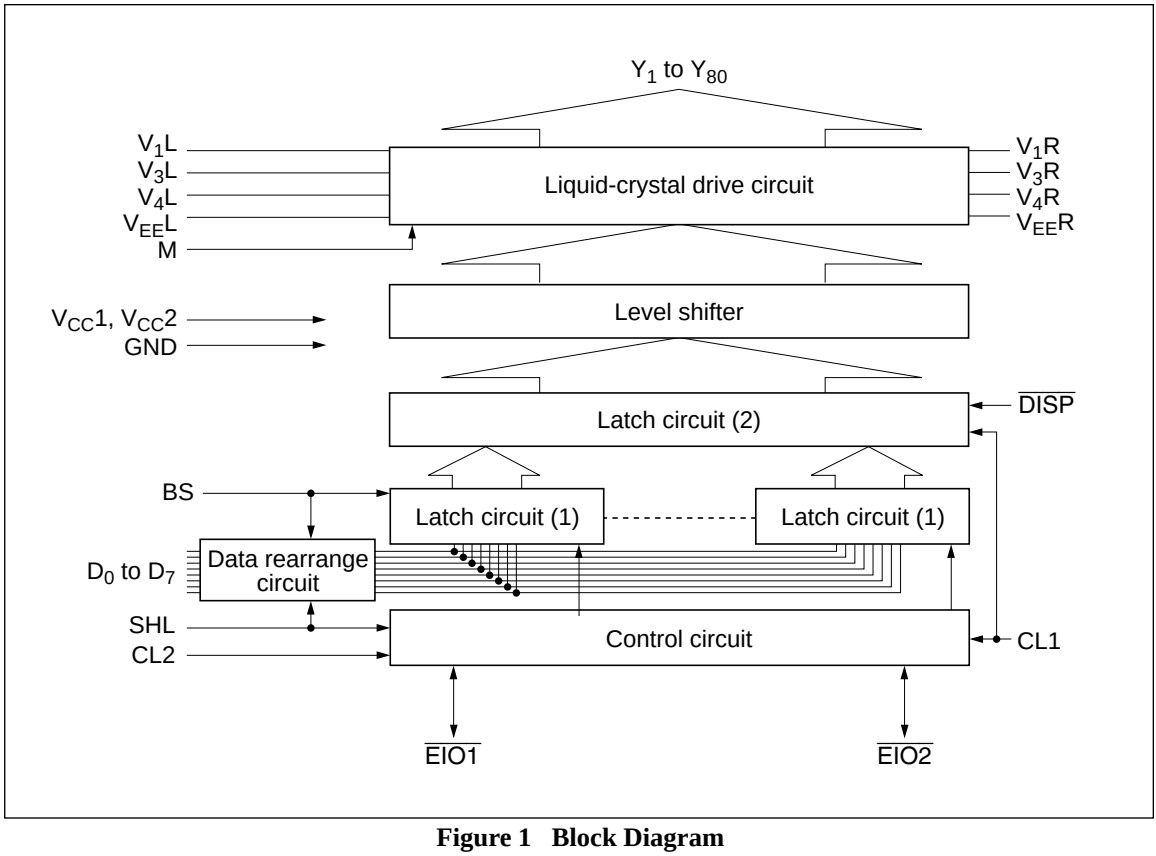
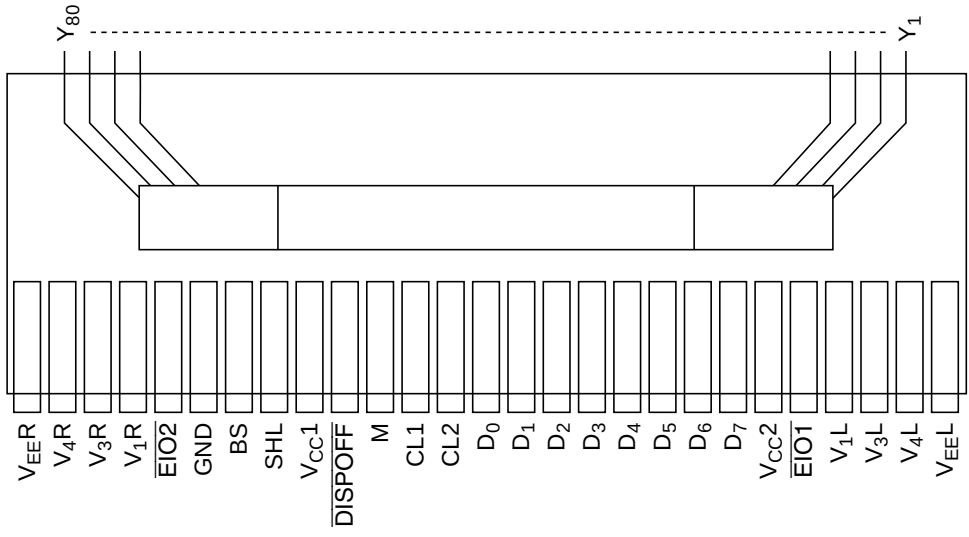


Figure 1 Block Diagram

Pin Arrangement



Note: This illustration does not correspond to the external shape of the TCP package.

Pin Description

Table 1 Pin Description

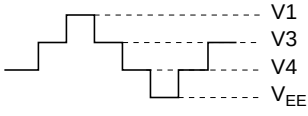
Type	Symbol	Pin Number	Pin Name	I/O	Function
Power supply	$V_{CC}1$	89	$V_{CC}1$	—	V_{CC} – GND: Connect to logic power supply.
	$V_{CC}2$	102	$V_{CC}2$		V_{CC} – V_{EE}: Connect to power supply for liquid-crystal drive circuit.
	GND	86	GND		
	$V_{EE}L$	107	$V_{EE}L$		
	$V_{EE}R$	81	$V_{EE}R$		
	V_1L	104	V_1L	I	Liquid crystal drive level power supply
	V_1R	84	V_1R		
	V_3L	105	V_3L		
	V_3R	83	V_3R		
	V_4L	106	V_4L		V_1, V_{EE}: selected level
	V_4R	82	V_4R		V_3, V_4: nonselected level
					The power supply should maintain the condition Vcc ≥ $V_1 > V_3 > V_4 > V_{EE}$. The L and R sides of V_1,V_3, and V_4 are separated within the device, so the potentials externally supplied to them must be identical.
Control signal	CL1	92	Clock 1	I	Synchronizes the drive signal that latches display data into latch circuit 2.
	CL2	93	Clock 2	I	Synchronizes the drive signal that latches display data into latch circuit 1.
	M	91	M	I	Converts the liquid crystal drive output to AC.
	D_0–D_7	94 to 101	Data 0–7	I	**Display Data** / **LCD Drive Output** / **LCD**: High / Selected level / On; Low / Nonselected level / Off

Table 1 Pin Description (cont)

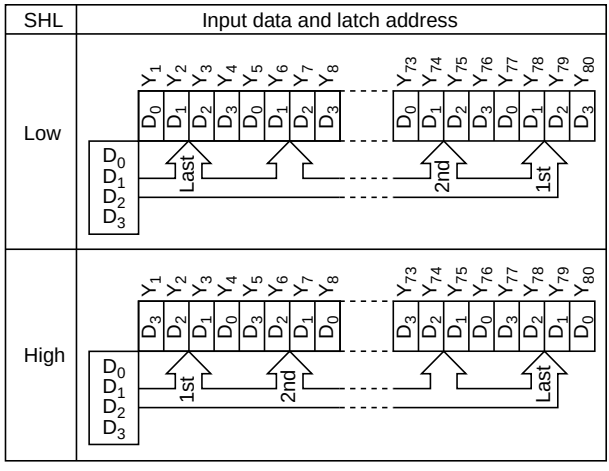
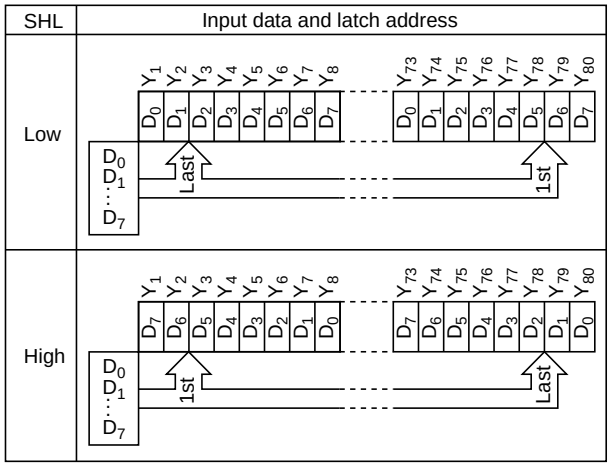
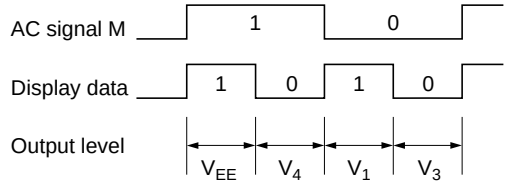
Type	Symbol	Pin Number	Pin Name	I/O	Function
Control signal (cont)	SHL	88	Shift left	I	Inverts the data output destination. 4-bit input mode:  8-bit input mode: 

Table 1 Pin Description (cont)

Type	Symbol	Pin Number	Pin Name	I/O	Function
Control signal (cont)	$\overline{\text{DISPOFF}}$	90	Display off	I	When the liquid crystal output nonselected level control input pin drives $\overline{\text{DISPOFF}}$ low, the liquid crystal drive output (Y_1 to Y_{80}) is set to the V1 level.
	$\overline{\text{EIO1}}$	103	Enable I/O 1	I/O	I/O pins for chip selection. Input/output is controlled by SHL input.
	$\overline{\text{EIO2}}$	85	Enable I/O 2		**SHL** / **Enable I/O 1** / **Enable I/O 2**: 0 — Output — Input; 1 — Input — Output. When the enable input signal goes low, data fetch begins. When all data has been fetched, the enable output changes from high to low and the next stage IC starts up.
	BS	87	Bus select	I	Switches the number of input bits for the display data. When high, places the device in 8-bit input mode; when low, changes the device to the 4-bit input mode.
Liquid crystal drive output	Y_1 to Y_{80}	1 to 80	Y_1 to Y_{80}	O	Outputs one of the four voltage levels V_1, V_3, V_4, or V_{EE}, based on the combination of the M signal and the display data.



Note: 0 and low levels indicate ground level. 1 and high levels indicate V_{CC} level.

Sample Application

Figure 2 shows an example of an LCD panel comprised of 640 × 200 dots, using the HD66224T. The recommended common driver is HD66215. For 640 × 400 dots, extend the configuration shown to configure two screens.

R1 and R2 differ depending on the LCD panel used. For a 1/15 bias, for example, R1 = 3 kΩ and R2 = 33 kΩ are used so that R1 (4R1 + R2) = 1/15.

When designing a board locate bypass capacitors as close to each device as possible, to stabilize the power supply. We recommend that two capacitors (of about 0.1 pF) be used with each HD66224T. One capacitor should be connected between V_{CC} and GND, and one between V_{CC} and V_{EE}.

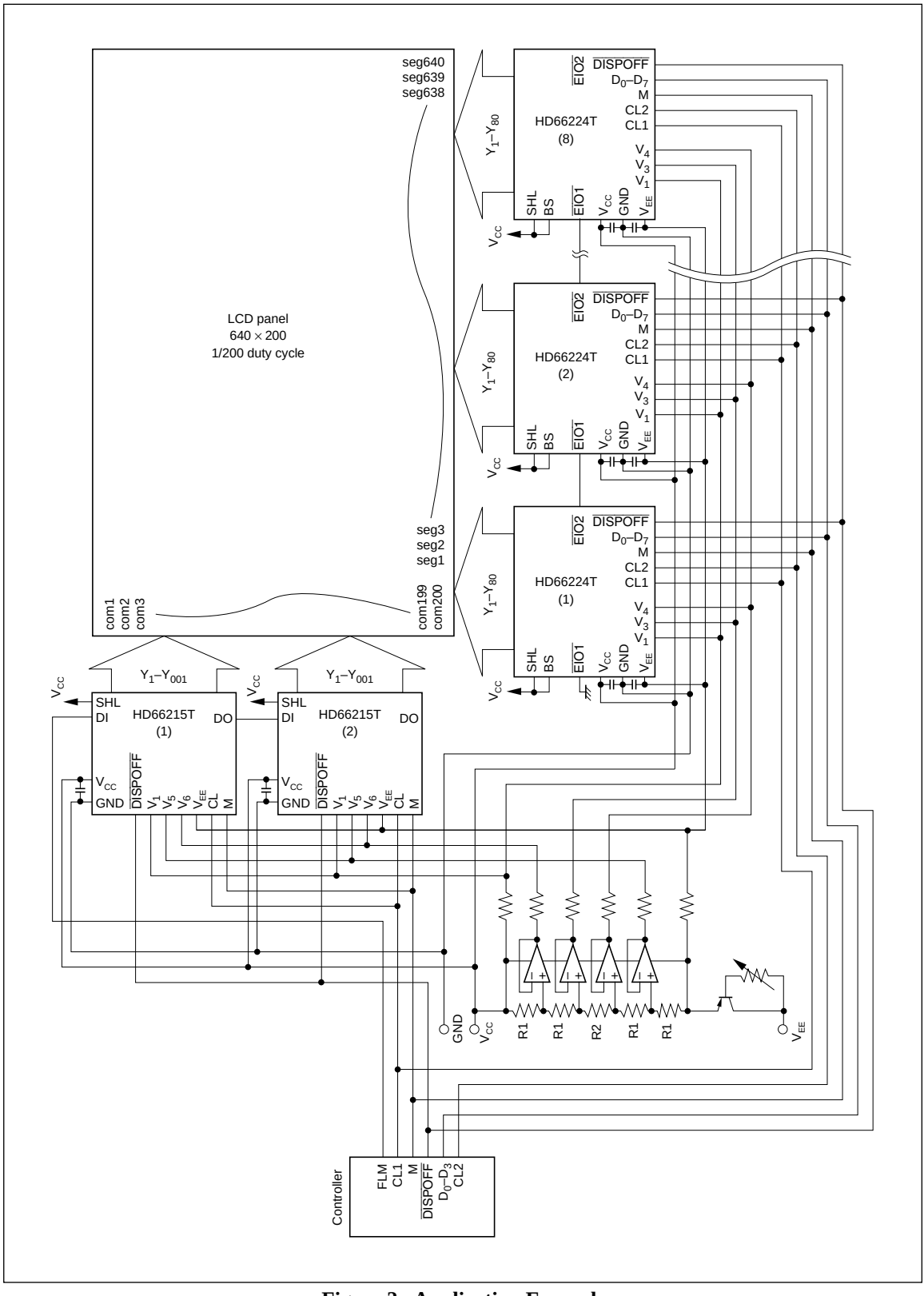


Figure 2 Application Example

Absolute Maximum Ratings

Parameters		Symbol	Rating	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	Liquid crystal drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3		
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature		T_{opr}	–20 to + 75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. Indicates the potential from GND.

2. Applies to the CL1, CL2, M, SHL, $\overline{EIO1}$, $\overline{EIO2}$, D_0 to D_7, and $\overline{DISPOFF}$ pins.
3. Applies to the V_1, V_3, and V_4 pins.
4. When a device is used outside of the absolute maximum ratings, it may suffer permanent damage. Exceeding the limits may cause malfunctions and have negative effects on device reliability. We recommend that device operating parameters be kept within these limits.

Electrical Characteristics

Table 2 **DC Characteristics (1)** (V_{CC} = 5 V ± l0%, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions	Notes
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, D_0 to D_7	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	V_{IL}	$\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	0	—	$0.2 \times V_{CC}$	V		
Output high level voltage	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA	
Resistance between Vi and Yj	R_{ON}	Y_1 to Y_{80}, V_1, V_3, V_4	—	0.6	1.5	kΩ	I_{ON} = 100 µA	1, 2
Input leakage current 1	I_{IL1}	CL1, CL2, M, SHL, D0 to D7, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	–1.0	—	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	V_1, V_3, V_4	–25	—	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz, f_{CL1} = 20 kHz, $V_{CC} - V_{EE}$ = 28 V	3
Current consumption 2	I_{EE}	—	—	150	500	µA		
Current consumption 3	I_{ST}	—	—	—	200	µA		3, 4

Notes: 1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:

$V_{CC} - V_{EE}$ = 28 V
V_1, $V_3 = V_{CC} - 2/10(V_{CC} - V_{EE})$
$V_4 = V_{EE} + 2/10(V_{CC} - V_{EE})$

2. Describes the voltage range for the liquid-crystal drive level power supply. A voltage near V_{CC} is supplied to V_1 and V_3. A voltage near V_{EE} is supplied to V4. Use within the range of ΔV for each. These ranges should be set so that the impedance ROM of the driver output obtained is stable. Note also that ΔV depends on the power supply voltage ($V_{CC} - V_{EE}$). See figure 3.
3. Excluding the current flowing to the input area and output area. When the driver uses an intermediate level for input, a through current flows to the input circuit and the power supply current increases, so be sure that $V_{IH} = V_{CC}$ and V_{IL} = GND.
4. Current during standby.

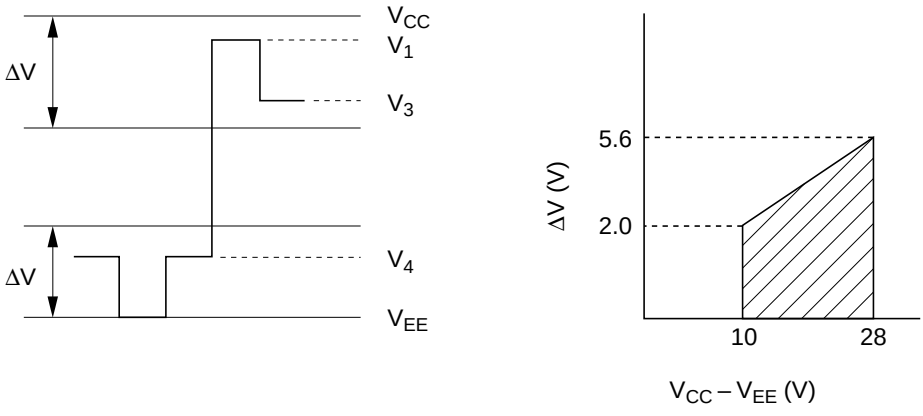


Figure 3 Relationship between Driver Output Waveform and Level Voltages

Table 3 **DC Characteristics (2)** (V_{CC} = 2.5 to 4.5 V, GND = 0 V, V_{CC}–V_{EE} = 10–28 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, D_0 to D_7	$0.8 \times V_{CC}$	—	V_{CC}	V	—
Input low level voltage	V_{IL}	$\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	0	—	$0.2 \times V_{CC}$	V	—
Output high level e voltag	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA
Output low level voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA
Resistance between V_i and Y_j*1, *2	R_{ON}	Y_1 to Y_{80}, V_1, V_3, V_4	—	0.6	1.5	kΩ	I_{ON} = 100 µA
Input leakage current 1	I_{IL1}	CL1, CL2, M, SHL, D_0 to D_7, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND
Input leakage current 2	I_{IL2}	V_1, V_3, V_4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}
Current consumption 1*3	I_{GND}	—	—	—	1.5	mA	f_{CL2} = 6.5 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V V_{CC} – V_{EE} = 28 V
Current consumption 2*3	I_{EE}	—	—	—	500	µA	
Current consumption 3*3, *4	I_{ST}	—	—	—	50	µA	

Notes: 1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:

$V_{CC} – V_{EE}$ = 28 V
V_1, V_3 = $V_{CC} – 2/10(V_{CC} – V_{EE})$
V_4 = $V_{EE} + 2/10(V_{CC} – V_{EE})$

2. Describes the voltage range for the liquid-crystal drive level power supply. A voltage near V_{CC} is supplied to V_1 and V_3. A voltage near V_{EE} is supplied to V_4. Use within the range of ΔV for each. These ranges should be set so that the impedance ROM of the driver output obtained is stable. Note also that ΔV depends on the power supply voltage ($V_{CC} – V_{EE}$). See figure 3.
3. Excluding the current flowing to the input area and output area. When the driver uses an intermediate level for input, a through current flows to the input circuit and the power supply current increases, so be sure that V_{IH} = V_{CC} and V_{IL} = GND.
4. Current during standby.

Table 4 **AC Characteristics (1)** (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	125	—	ns
Clock high level width 2	t_{CWH2}		45		
Clock low level width 2	t_{CWL2}				
Data setup time	t_{DS}	D_0 to D_7, CL2	30		
Data hold time	t_{DH}				
Clock high level width 1	t_{CWH1}	CL1	45		
CL2 rise to CL1 rise	t_{LD}	CL1, CL2	30		
CL2 fall to CL1 fall	t_{SCL}		45		
CL1 rise to CL2 rise	t_{LS}				
CL1 fall to CL2 fall	t_{HCL}				
Input signal rise time*1	t_r		—	50	
Input signal fall time*1	t_f				

Table 5 **AC Characteristics (2)** (V_{CC} = 2.5 V to 4.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Max	Unit
Clock cycle time*2	t_{CYC}	CL2	152	—	ns
Clock high level width 2	t_{CWH2}		65		
Clock low level width 2	t_{CWL2}				
Data setup time	t_{DS}	D_0 to D_7, CL2	50		
Data hold time	t_{DH}		40		
Clock high level width 1	t_{CWH1}	CL1	65		
CL2 rise to CL1 rise	t_{LD}	CL1, CL2	20		
CL2 fall to CL1 fall	t_{SCL}		65		
CL1 rise to CL2 rise	t_{LS}				
CL1 fall to CL2 fall	t_{HCL}				
Input signal rise time*1	t_r		—	50	
Input signal fall time*1	t_f		—	50	

Notes (tables 4 and 5):

1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:
   $V_{CC} – V_{EE}$ = 28 V
   V_1, $V_3 = V_{CC} – 2/10(V_{CC} – V_{EE})$
   $V_4 = V_{EE} + 2/10(V_{CC} – V_{EE})$
2. t_r, $t_f \leq$ 11 ns

AC Characteristic Test Waveforms

Figure 4 shows test point loading and test waveforms. Connect test points through a 15-pF capacitor to ground, as shown at the top of figure 4.

BS = GND (4-Bit Fetch Mode)

When the data fetch operation enable signal goes low (with SHL = GND and $\overline{EIO2}$ = GND), data standby is cleared. On the next rising edge of clock CL2, the standby is cleared. Figure 5 shows timing for 4-bit fetch mode operation. When CL2 falls, the first 4-bit data fetch is performed. The 4-bit fetches continue on each subsequent falling edge of CL2 until 76 bits have been fetched. The enable signal (when SHL = GND, $\overline{EIO1}$) then goes to GND level. When 80 bits have been fetched, fetch is automatically halted (standby). If the $\overline{EIO1}$ pin is connected to the $\overline{EIO2}$ pin of the next stage, the next device will begin 4-bit fetch operation.

The data output changes when CL1 falls. The output destination for the fetched data when SHL = GND is output pin Y_{80} for d_1, and Y_1 for d_{80}.

When SHL = V_{CC}, the destinations are reversed; d_{80} is output to Y_{80} and d_1 is output to Y_1. The output level (V_1 through $V_{4)}$ is actually selected by the combination of the display data and AC signal M.

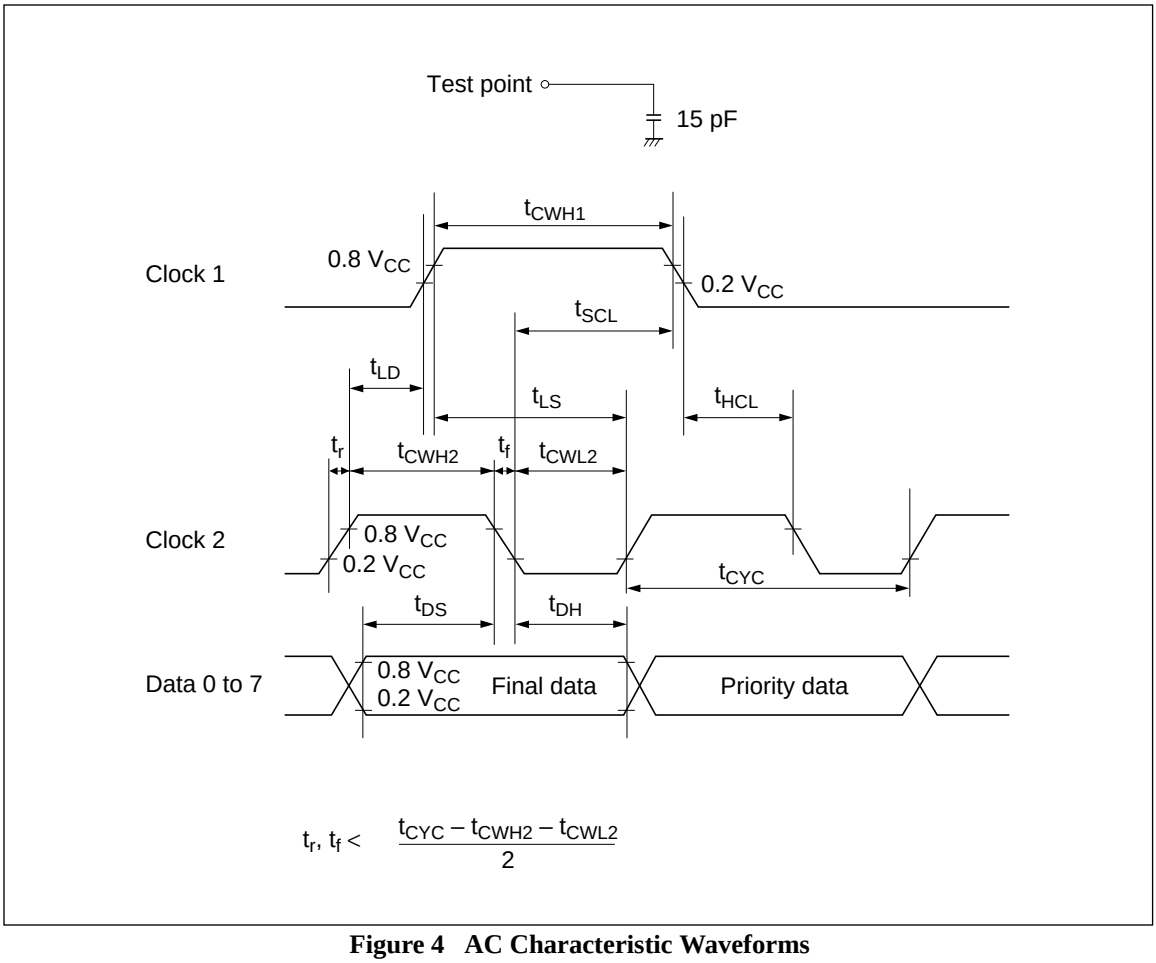


Figure 4 AC Characteristic Waveforms

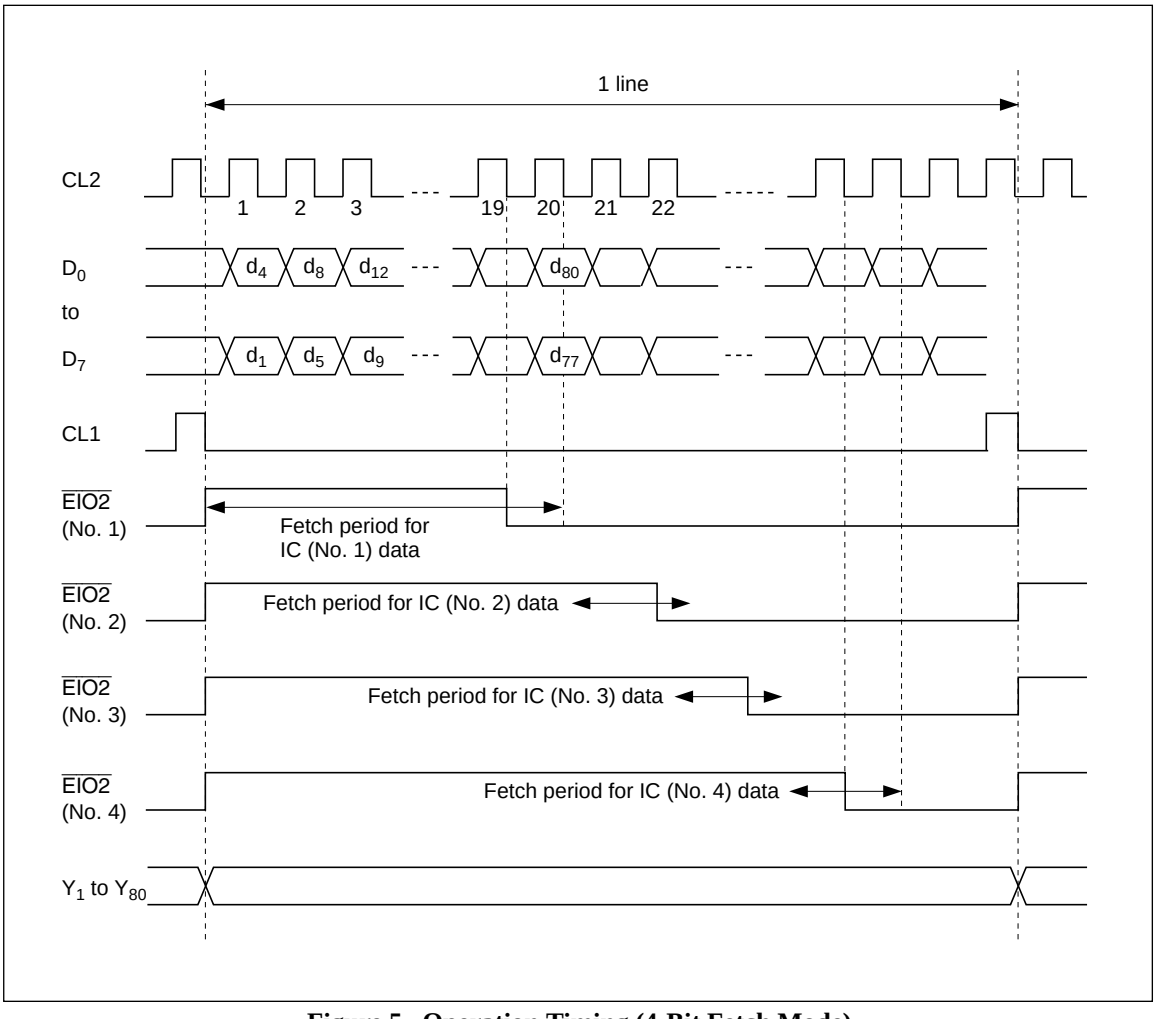


Figure 5 Operation Timing (4-Bit Fetch Mode)

BS = V_{CC} (8-Bit Fetch Mode)

The 8-bit data fetch basic functions are the same as in the 4-bit fetch mode. Figure 6 shows timing for 8-bit fetch mode operation.

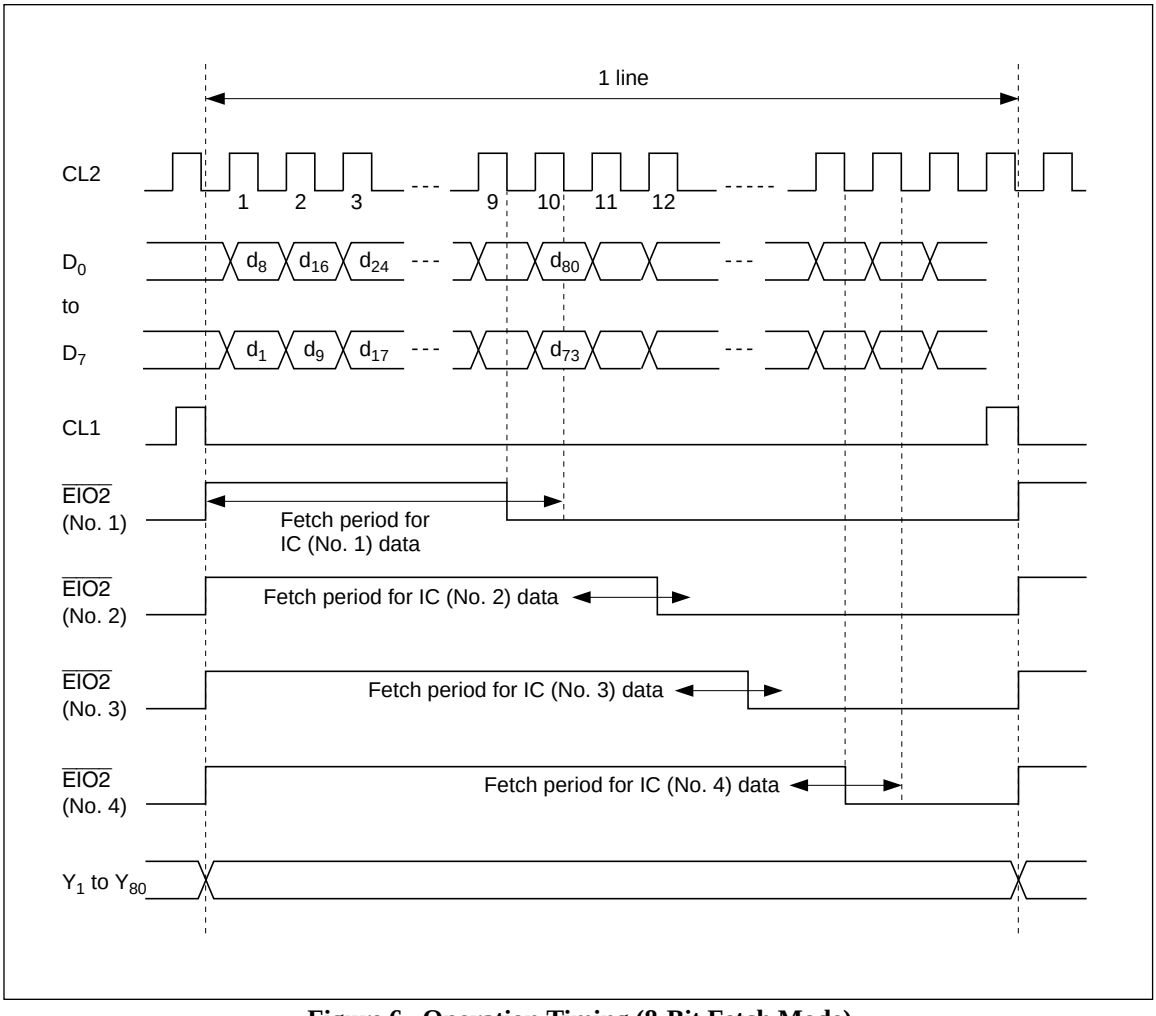


Figure 6 Operation Timing (8-Bit Fetch Mode)

HD66215T

(Common Driver for a Dot Matrix Liquid Crystal Graphic Display with 100-Channel Outputs)

HITACHI

Description

The HD66215T is a common driver for a large dot matrix liquid crystal graphic display (LCD). The driver's 100 channels can be divided into two groups of 50 channels by selecting data input/output pins. Outputs X_1 to X_{10} and X_{91} to X_{100} can be disabled by mode selection. Unused output pins can be equally distributed above and below the pins used for the LCD panel so that the panel can be neatly centered on the LCD board. A 101-channel output mode can also be selected for an application to various display panels. The driver is powered by about 3V, making it suitable for battery-driven portable equipment featuring the low power dissipation of liquid crystal elements.

The HD66215T, packaged in a micro-tape carrier package (micro-TCP), allows design of a compact LCD system with a frame (an area peripheral to the LCD panel) about half the width of conventional systems.

Features

- Duty cycle: About 1/64 to 1/240
- 100 internal LCD drive circuits (101-channel mode can be selected for a 101-output version)
- High output voltage for driving the LCD: 10 to 28 V
- Output division function (50 × 2-output)
- 10-output through modes
- 101-output mode
- Display off function
- Internal 100-bit shift register
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850
- Micro-TCP with 3-sprocket-hole width
- Operating voltage: 2.5 to 5.5 V

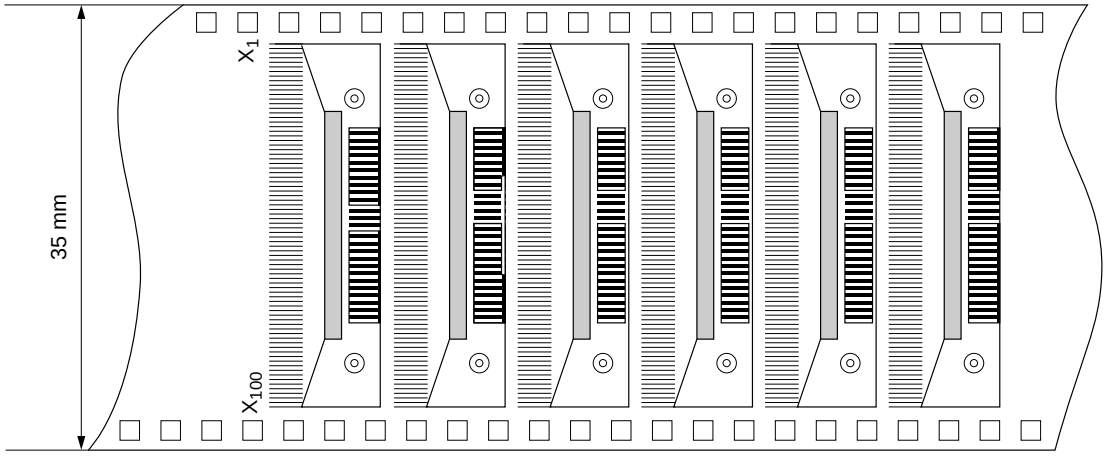
Ordering Information

Type No.	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66215TA0	0.23 mm	1.20 mm	3 sprocket holes
HD66215TA1	0.22 mm	1.00 mm	3 sprocket holes
HD66215TA2	0.18 mm	0.85 mm	3 sprocket holes

Notes:
1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
2. Device length includes test pad areas.
3. Spacing between two sprocket holes is 4.75 mm.
4. Tape film is Upirex (a trademark of Ube Industries, Ltd.).
5. 35-mm-wide tape is used.
6. Leads are plated with Sn.
7. The details of TCP pattern are shown in "The Information of TCP."

Hitachi semiconductor

Tape Carrier Package



Pin Arrangement

1	V_1L
2	V_6L
3	V_5L
4	$V_{EE}L$
5	MODE1
6	DIO4
7	$\overline{\text{DISPOFF}}$
8	V_{CC}
9	SHL/R
10	DIO3
11	DIO2
12	GND
13	M
14	CL
15	DIO1
16	MODE2
17	$V_{EE}R$
18	V_5R
19	V_6R
20	V_1R

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	8	V_{CC}	—	Power supply
GND	12	GND		
V_1L, V_1R	1, 20	V_1L, V_1R	Input	
V_6L, V_6R	2, 19	V_6L, V_6R		
V_5L, V_5R	3, 18	V_5L, V_5R		
$V_{EE}L$, $V_{EE}R$	4, 17	$V_{EE}L$, $V_{EE}R$		
CL	14	Clock		Control signal
M	13	M		
SHL/R	9	Shift left/right		
DIO1	15	Data	Input/output	
DIO2	11			
DIO3	10			
DIO4	6			
$\overline{DISPOFF}$	7	Display off	Input	
MODE1, MODE2	5, 16	Mode1, Mode2		
X_1–X_{100}	21–120	X_1–X_{100}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_1L, V_1R, V_5L, V_5R, V_6L, V_6R, $V_{EE}L$, $V_{EE}R$: Supply different levels of power to drive the LCD. V_1 and V_{EE} are selected levels, and V_5 and V_6 are non-selected levels. See figure 1.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes LCD drive outputs to AC.

SHL/R: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1–DIO4: Input or output data. DIO1 and DIO2 are data input/output pins for X_1–X_{50}, and DIO3 and DIO4 are input/output pins for X_{51}–X_{100} (X_{101}) in 50 × 2-output modes. In a 100-output mode, DIO2 and DIO3 must be short-circuited, and DIO1 and DIO4 are used as data input/output pins.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets LCD drive outputs X_1–X_{100} (X_{101}) to V_1 level.

MODE1, MODE2: Select an LCD output mode (table 1). In 10-output through modes, ten unused output pins are made invalid. These ten pins must be open in these modes since they output M signals.

LCD Drive Outputs

X_1–X_{100}: Each X outputs one of the four voltage levels, V_1, V_5, V_6, or V_{EE}, depending on a combination of the M signal and data levels. See figure 3.

Table 1 Selection of LCD Output

MODE1	MODE2	Selected Mode
0	0	Normal (100-output)
0	1	10-output through (X_1–X_{10})
1	0	(X_{91}–X_{100})
1	1	101-output

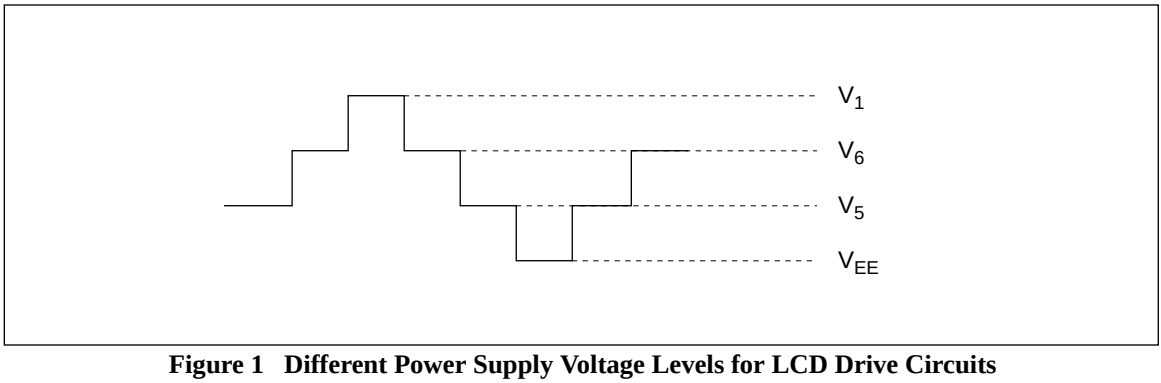


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 100 × 1-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{100}$
	In 50 × 2-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 100 × 1-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_1$
	In 50 × 2-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{100} \rightarrow X_{51}$

For 10-output through modes and 101-output mode, see Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in Each Mode.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in Normal Mode (100-Output Mode)

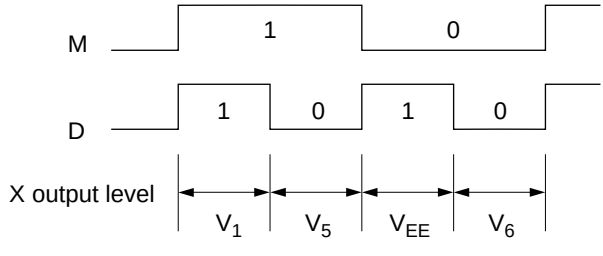
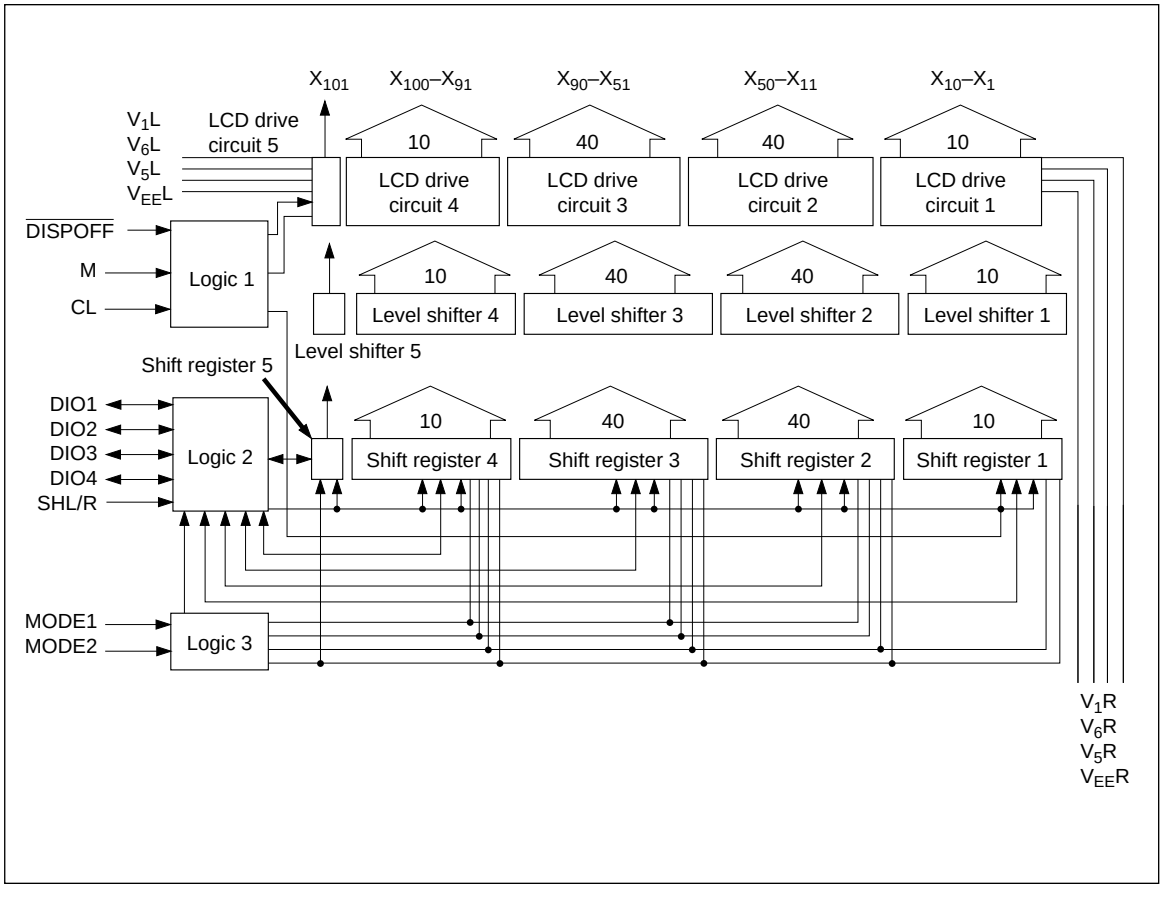


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuits

The 100-bit LCD drive circuits generate four voltage levels, V_1, V_5, V_6, and V_{EE}, which drive an LCD panel. One of the four levels is output to the corresponding X pin, depending on a combination of the M signal and the data in the shift register.

Level Shifters

The level shifters change logic control signals (2.5 to 5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Registers

The 100-bit shift registers shift data input via the DIO pin by one bit. The bit that is shifted out is output from the DIO pin to the next driver IC. Both shifting and output occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL/R pin selects the data shift direction.

Logic 3

Logic 3 selects which shift register operates depending on the settings of MODE1 and MODE2.

Data Shift and Common Signal Scan Direction

Figure 4–7 show the data shift direction and common signal scan direction selected by SHL/R and DIO pins in each mode.

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 100 × 1-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{100}$
	In 50 × 2-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 100 × 1-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_1$
	In 50 × 2-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{100} \rightarrow X_{51}$

Figure 4 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 100-Output Mode (MODE1 = 0 and MODE2 = 0)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 90-output mode				
	Input	Short-circuited		Output	$X_{11} \rightarrow X_{100}$
	In 40- and 50-output mode				
	Input	Output	Input	Output	$X_{11} \rightarrow X_{50}$
					$X_{51} \rightarrow X_{100}$
High	In 90-output mode				
	Output	Short-circuited		Input	$X_{100} \rightarrow X_{11}$
	In 40- and 50-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_{11}$
					$X_{100} \rightarrow X_{51}$

Figure 5 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO pins in 10-Output (X_1–X_{10}) Through Mode (MODE1 = 0 and MODE 2 = 1)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 90-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{90}$
	In 50- and 40-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{90}$
High	In 90-output mode				
	Output	Short-circuited		Input	$X_{90} \rightarrow X_1$
	In 50- and 40-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{90} \rightarrow X_{51}$

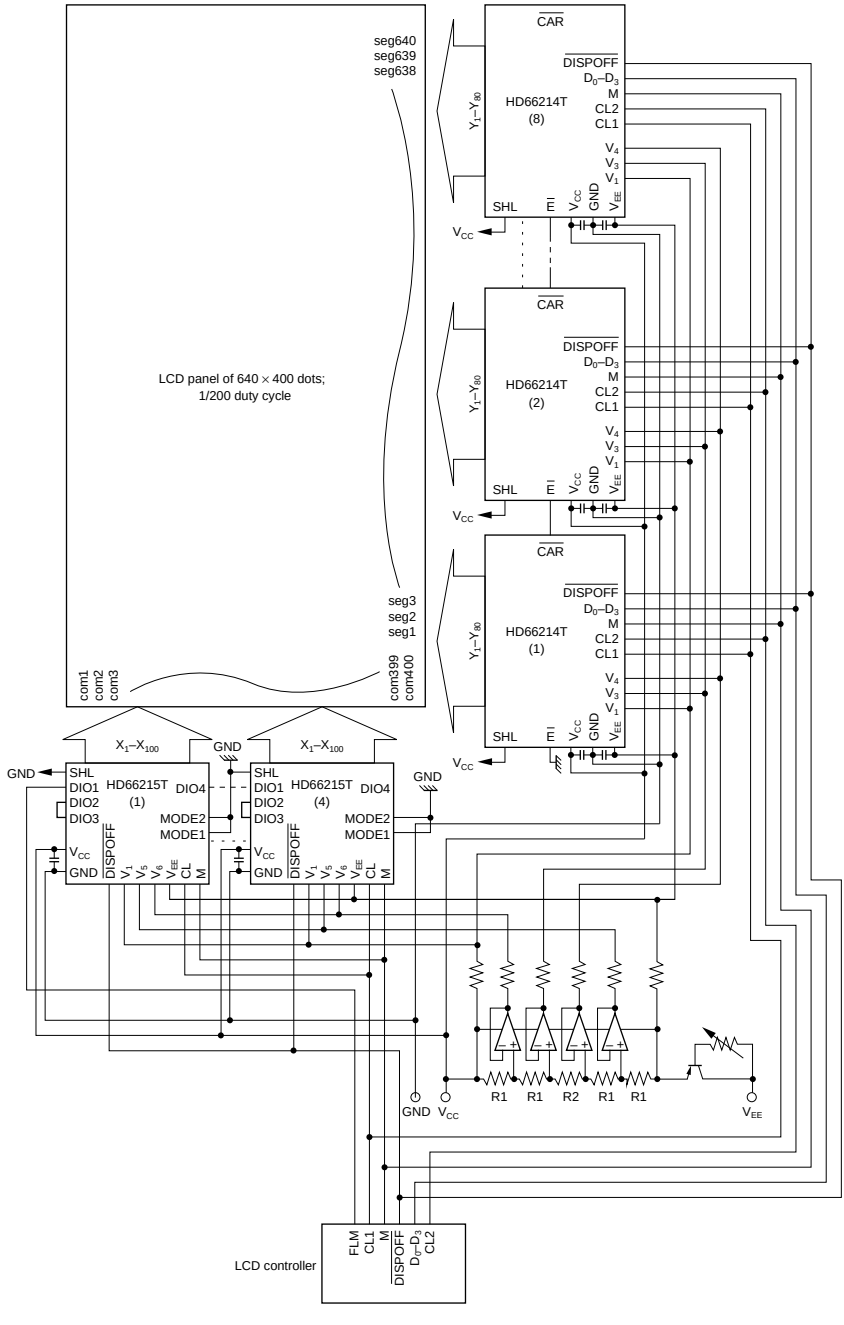
Figure 6 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 10-Output (X_{91}–X_{100}) Through Mode (MODE1 = 1 and MODE2 = 0)

SHL/R	DIO1	DIO2	DIO3	DIO4	Data shift direction and common signal scan direction
Low	In 101-output mode				
	Input	Short-circuited		Output	$X_1 \rightarrow X_{101}$
	In 50- and 51-output mode				
	Input	Output	Input	Output	$X_1 \rightarrow X_{50}$
					$X_{51} \rightarrow X_{101}$
High	In 101-output mode				
	Output	Short-circuited		Input	$X_{101} \rightarrow X_1$
	In 50- and 51-output mode				
	Output	Input	Output	Input	$X_{50} \rightarrow X_1$
					$X_{101} \rightarrow X_{51}$

In 101-output mode, any 10-output through mode cannot be used.

Figure 7 Selection of Data Shift Direction and Common Signal Scan Direction by SHL/R and DIO Pins in 101-Output Mode (MODE1 = 1 and MODE2 = 1)

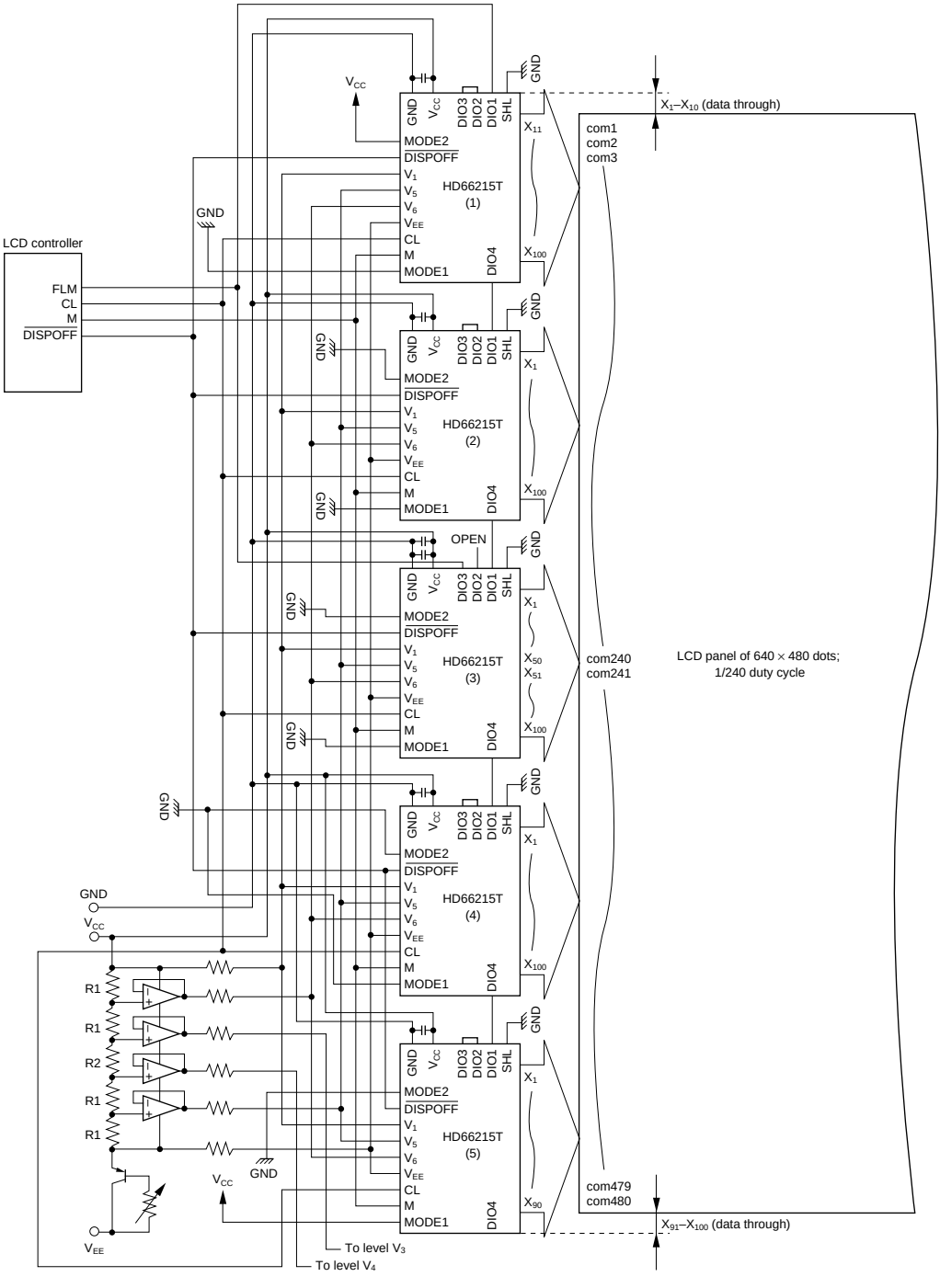
Application Examples



Notes: 1. The resistances of R1 and R2 depend on the type of LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Figure 8 LCD Panel of 640 × 400 Dots, 1/200 Duty Cycle



Notes: 1. The resistances of R1 and R2 depend on the type of LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4·R1 + R2) should be 1/15.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Figure 9 LCD Panel of 640 × 480 Dots, 1/240 Duty Cycle

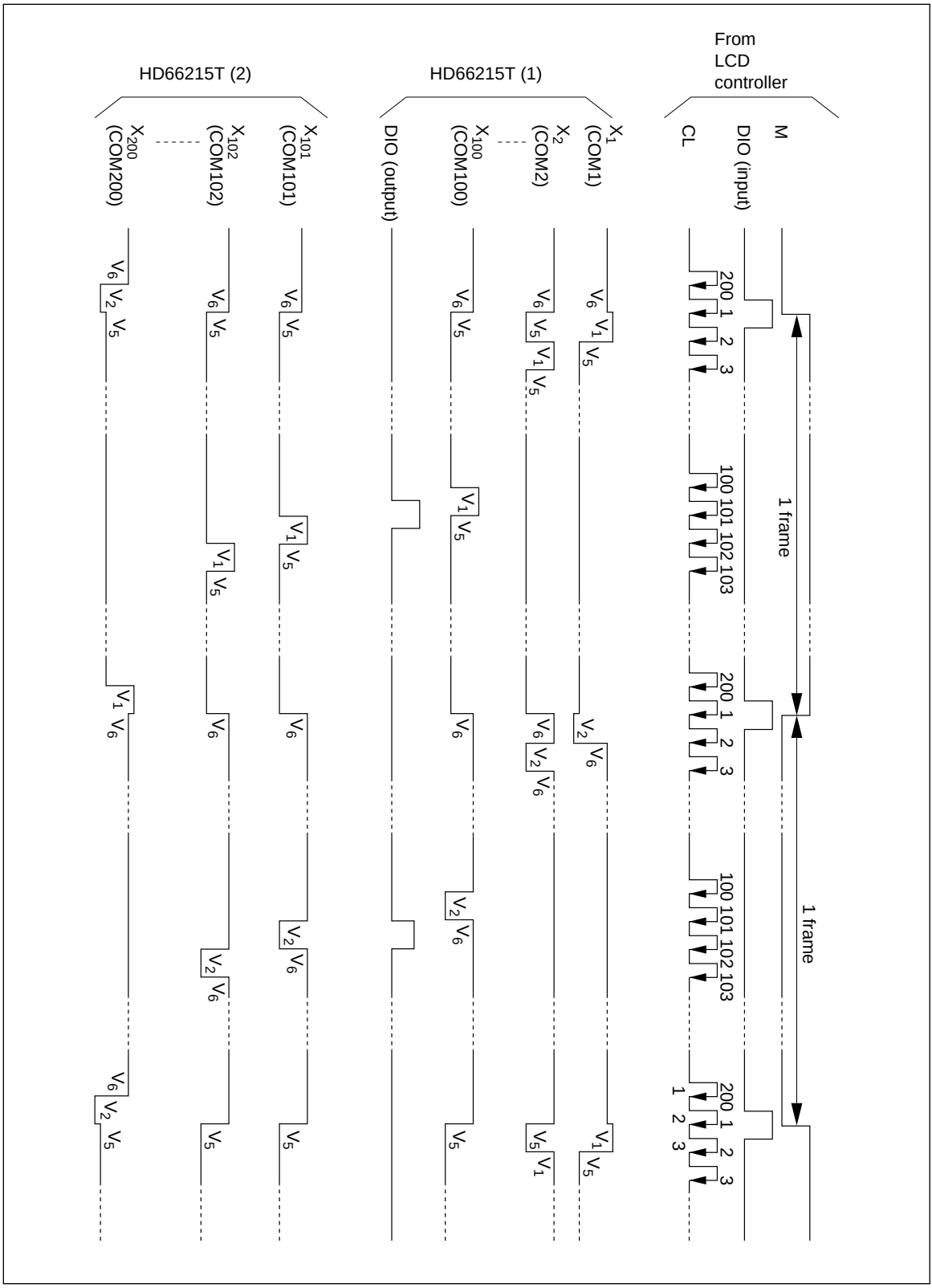


Figure 10 Operational Timing in Normal Mode (100-Output Mode, 1/200 Duty Cycle)

HD66215T Connection Examples

Figure 11 shows an example of an HD66215T driving a 480-line LCD panel with a 1/240 to 1/250 duty cycle. Here, selecting MODE1 and MODE2 disables outputs X_1–X_{10} of driver IC1 and outputs X_{91}–X_{100} of driver IC5. As a result, unused driver output pins can be equally distributed above and below the pins used for the LCD panel so that the panel can be neatly centered on the LCD board. In addition, since the 100 channels of the driver can be divided into two groups of 50 channels by selecting data input/output pins, data input is divided at the center of the panel (IC3).

Figure 12 shows an example of an HD66215T driving a 400-line LCD panel with a 1/200 to 1/210 duty cycle.

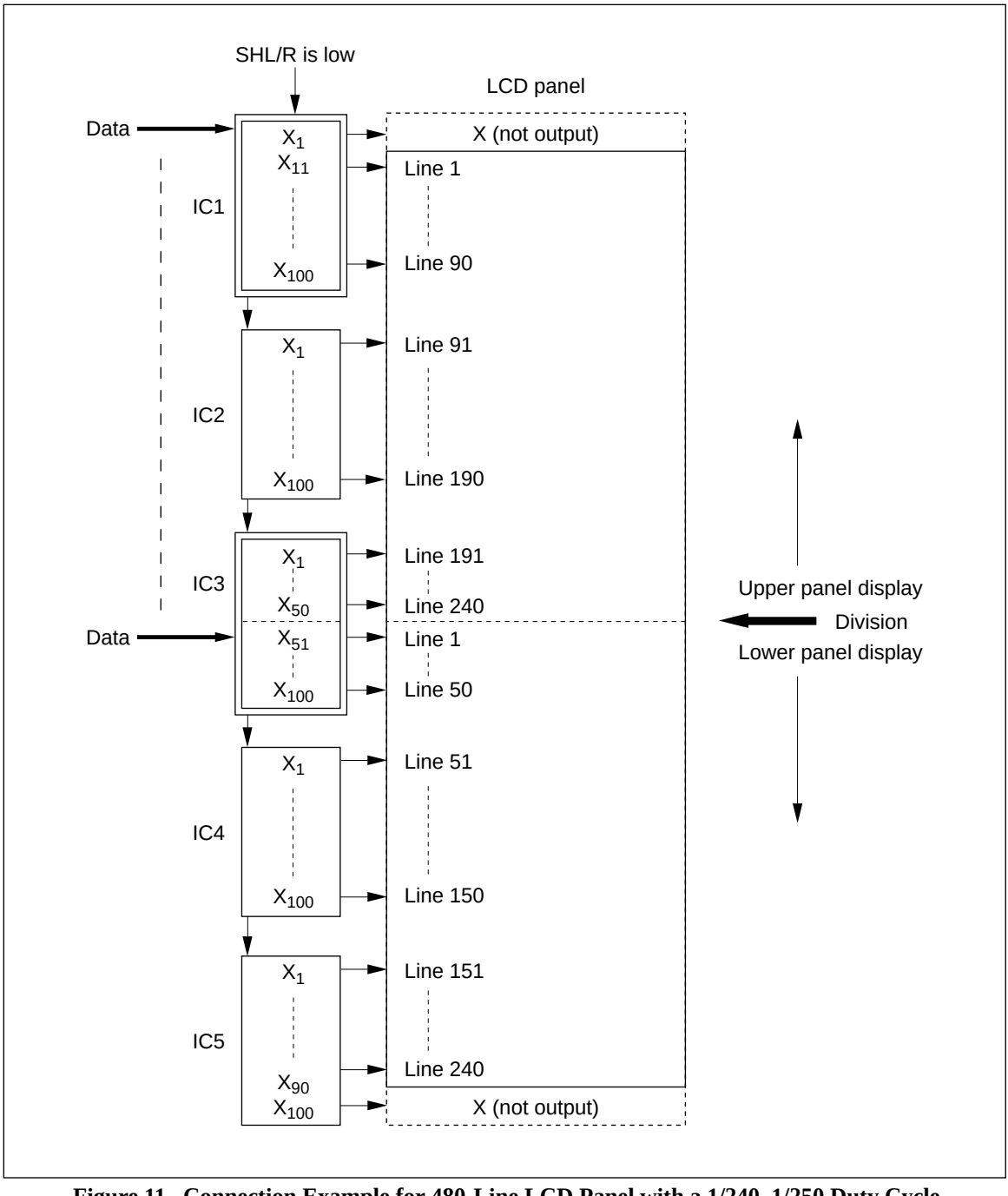


Figure 11 Connection Example for 480-Line LCD Panel with a 1/240–1/250 Duty Cycle

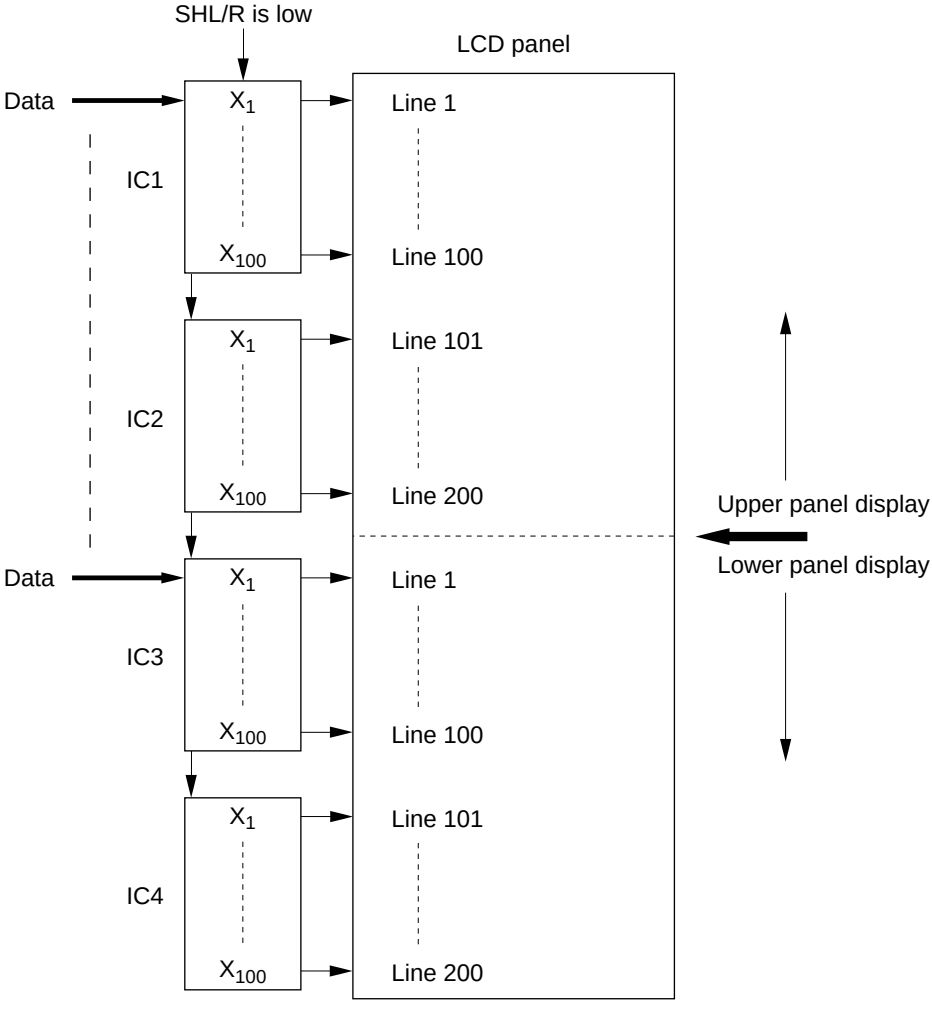


Figure 12 Connection Example for 400-Line LCD Panel with a 1/200–1/210 Duty Cycle

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits		V_{CC}	–0.3 to +7.0	V	2
Power supply voltage for LCD drive circuits		V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3		
Input voltage	1	V_{T1}	–0.3 to V_{CC} + 0.3		2, 3
	2	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3		2, 4
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125		

Notes: 1. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunction or unreliability.

2. The reference point is GND (0 V).
3. Applies to pins CL, M, SHL/R, DIO1–DIO4 (input), $\overline{\text{DISPOFF}}$.
4. Applies to pins V_1, V_5, and V_6.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item		Symbol	Pins	Min	Typ	Max	Unit	Condition	Notes
Input high voltage		V_{IH}	1	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low voltage		V_{IL}	1	0	—	$0.3 \times V_{CC}$			
Output high voltage		V_{OH}	2	V_{CC} – 0.4	—	—		I_{OH} = –0.4 mA	
Output low voltage		V_{OL}	2	—	—	0.4		I_{OL} = 0.4 mA	
Vi–Xj on resistance		R_{ON}	3	—	0.5	1.0	kΩ	I_{ON} = 100 µA	1
Input leakage current	1	I_{IL1}	4	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
	2	I_{IL2}	5	–25	—	25		V_{IN} = V_{CC} to V_{EE}	
	3	I_{IL3}	2	–5.0	—	5.0		V_{IN} = V_{CC} to GND	
Current consumption	(5 V)	I_{GND}	—	—	—	100		f_{CL} = 19.2 kHz	2
		I_{EE}	—	—	—	250		V_{CC} – V_{EE} = 28 V f_{FLM} = 80 Hz V_{CC} – GND = 5 V	
	(3 V)	I_{GND}	—	—	—	50		f_{CL} = 19.2 kHz	2
		I_{EE}	—	—	—	250		V_{CC} – V_{EE} = 28 V f_{FLM} = 80 Hz V_{CC} – GND = 3 V	

Pins:
1. CL, M, SHL/R, $\overline{\text{DISPOFF}}$, DIO1–DIO4 (input)
2. DIO1–DIO4 (input)
3. X_1–X_{100}, V_1, V_5, V_6
4. CL, M, SHL/R, MODE1, MODE2, $\overline{\text{DISPOFF}}$
5. V_1, V_5, V_6

Notes:
1. Indicates the resistance between one pin from X_1–X_{100} and another pin from V_1, V_5, V_6, and V_{EE}, when load current is applied to the X pin. Defined under the following conditions:
   V_{CC} – V_{EE} = 28 V
   V_1, V_6 = V_{CC} – {1/10 (V_{CC} –V_{EE})}
   V_5 = V_{EE} + {1/10 (V_{CC} –V_{EE})}
   V_1 and V_6 should be near V_{CC} level, and V5 should be near V_{EE} level (figure 4). All voltage must be within Δ V. Δ V is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that Δ V depends on power supply voltages V_{CC} – V_{EE} (figure 5).
2. Excludes input and output current. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

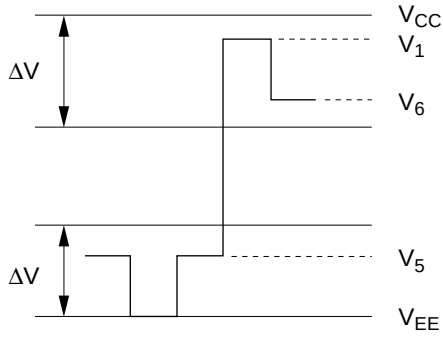


Figure 13 Relation between Driver Output Waveform and Level Voltages

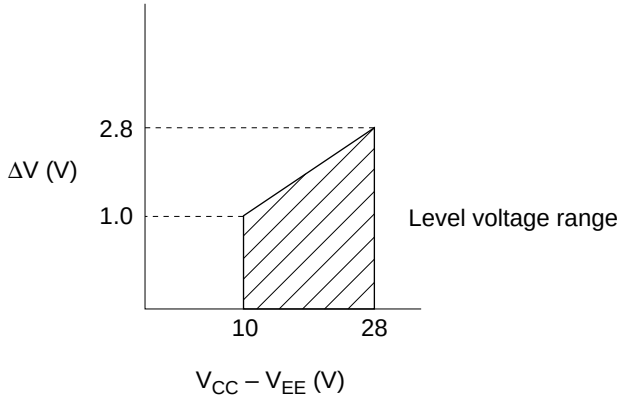


Figure 14 Relation between $V_{CC} - V_{EE}$ and Δ V

AC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL	10	—	µs
Clock high-level width	t_{CWH}		65	—	ns
Clock low-level width	t_{CWL}		1.0	—	µs
Clock rise time	t_r		—	50	ns
Clock fall time	t_f				
Data setup time	t_{DS}	DIO1–DIO4, CL	100	—	
Data hold time	t_{DH}				
Data output delay time*	t_{DD}		—	7.0	µs
Data output hold time	t_{DHW}		100	—	ns

Note: * The load circuit is shown in figure 15 is connected.

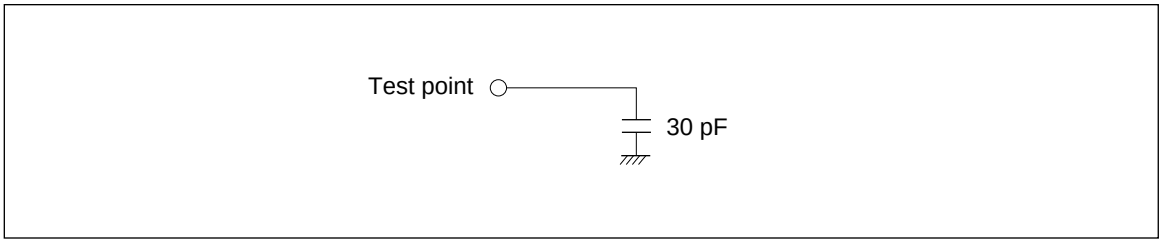


Figure 15 Load Circuit

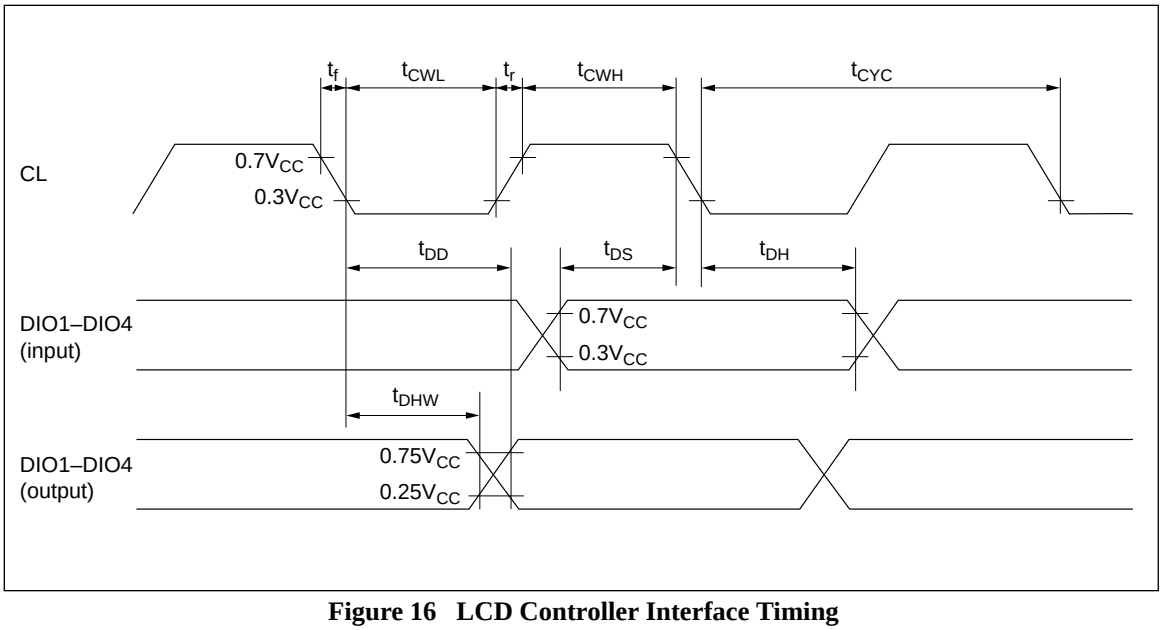


Figure 16 LCD Controller Interface Timing

HD66106F

(LCD Driver for High Voltage)

HITACHI

Description

The HD66106F LCD driver has a high duty ratio and many outputs for driving a large capacity dot matrix LCD panel.

It includes 80 LCD drive circuits and can drive at up to 1/480 duty cycle. For example, only 14 drivers are enough to drive an LCD panel of 640 × 480 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator.

Using this LSI sharply lowers the cost of an LCD system.

Features

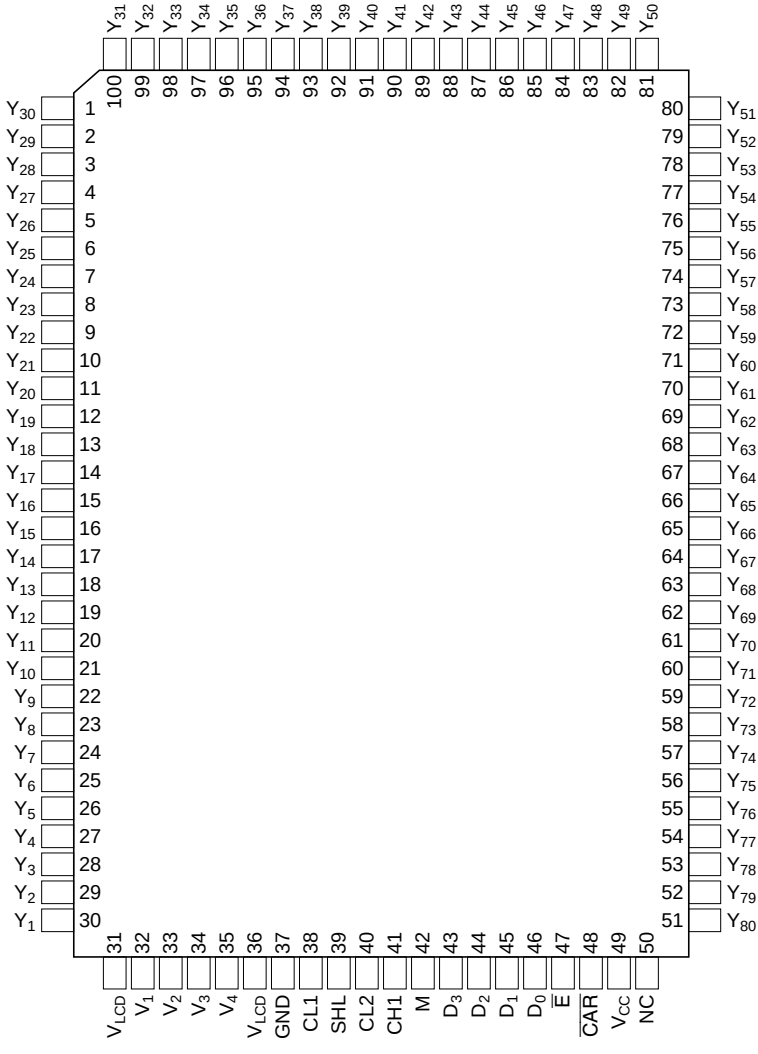
- Column and row driver
- 80 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby function
- Recommended LCD controller LSIs: HD63645F and HD64645F (LCTC)
- Power supply: +5 V ± 10% for the internal logic, and 14.0 V to 37.0 V for LCD drive circuits
- Operation frequency: 6.0 MHz (max.)
- CMOS process

Ordering Information

Type No.	Package
HD66106FS	100-pin plastic QFP (FP-100A)
HD66106D	Chip

Hitachi semiconductor

Pin Arrangement



(Top view)

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1–V_4 supply power for driving LCD (figure 1).

Control Signals

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used a s a column driver, and shifts line select data at the negative edge when it is used as a row driver.

Table 1 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	49	V_{CC}	I
GND	37	Ground	I
V_{LCD}	31, 36	V_{LCD}	I
V_1	32	LCD voltage 1	I
V_2	33	V_2 LCD voltage 2	I
V_3	34	V_3 LCD voltage 3	I
V_4	35	V_4 LCD voltage 4	I
CL1	38	Clock 1	I
CL2	40	Clock 2	I
M	42	M	I
D_0–D_3	46–43	Data 0 to data 3	I
SHL	39	Shift left	I
$\overline{E}$	47	Enable	I
$\overline{CAR}$	48	Carry	O
CH1	41	Channel 1	I
Y_1–Y_{80}	30–1, 100–51	Drive outputs 1–80	O
NC	50	No connection	—

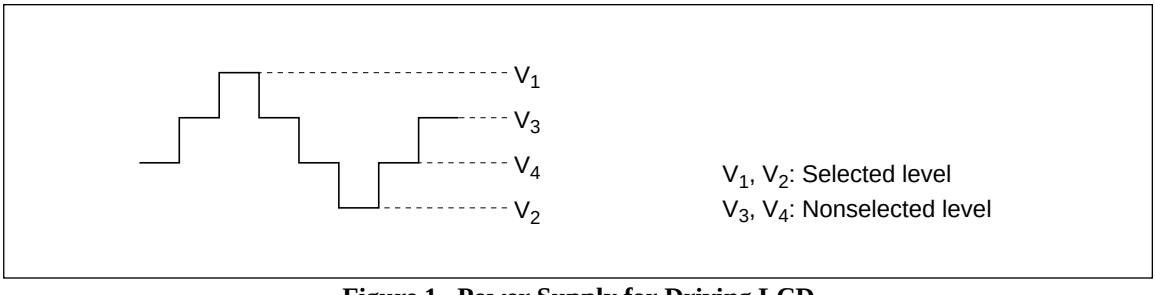


Figure 1 Power Supply for Driving LCD

M: M changes LCD drive outputs to AC.

D_0–D_3: D_0–D_3 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). $\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

Table 2 Relation between Display Data and LCD State

Display Data	LCD Outputs	LCD
1 (= high level)	Selected level	On
0 (= low level)	Nonselected level	Off

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI Is Used as a Row Driver)

SHL	Shift Direction of Shift Register				Scan Direction of Selected Line			
V_{CC}	$\overline{E}$	→ 1	→ 2	→ 3 ----------→ 80	Y1	→ Y2	→ Y3 ----------→ Y80	
GND	$\overline{E}$	→ 80	→ 79	→ 78----------→ 1	Y80	→ Y79	→Y78----------→ Y1	

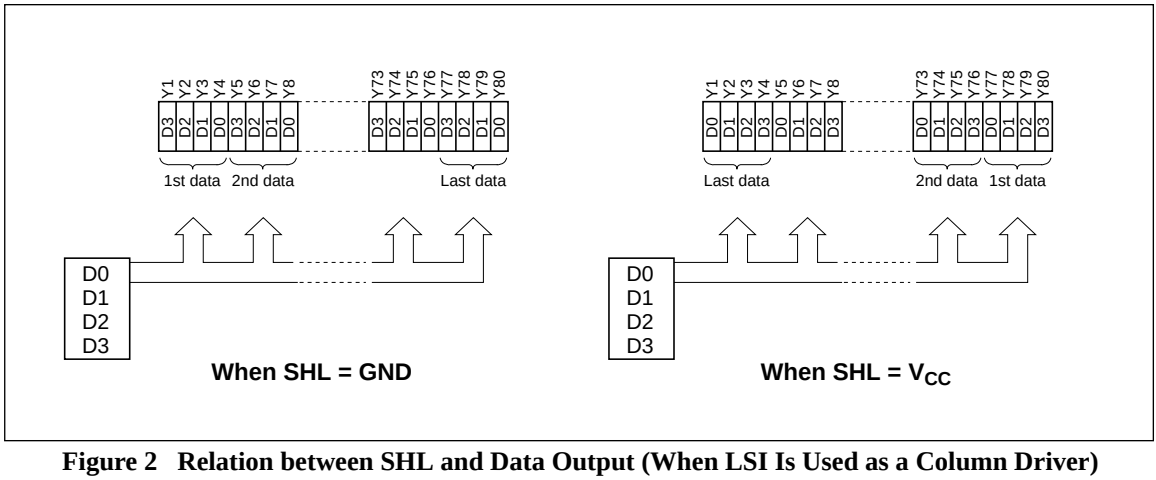


Figure 2 Relation between SHL and Data Output (When LSI Is Used as a Column Driver)

CH1: CH1 selects the driver function. The chip drives columns when CH1 = V_{CC}, and rows when CH1 = GND.

Y_1–Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 3).

NC: NC is not used. Do not connect any wire.

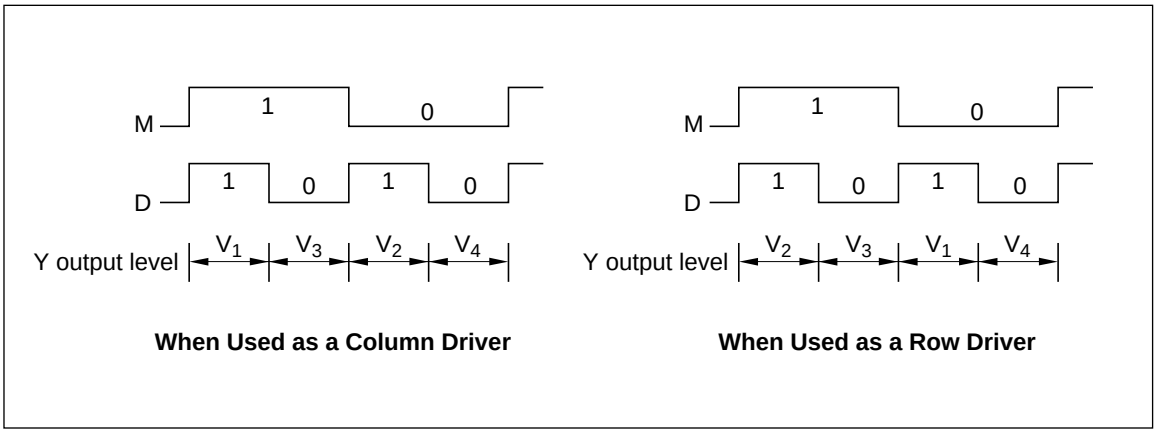


Figure 3 Selection of LCD Drive Output Level

Internal Block Diagram

LCD Drive Circuits

The HD66106F (figure 4) begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Latch Circuit 2

When the LSI is used as a column driver, latch circuit 2 functions as an 80-bit latch circuit. It latches the data sent from latch circuit 1 at the fall of CL1 and transfers its outputs to the LCD drive circuits.

When the LSI is used as a row driver, this circuit functions as an 80-bit bidirectional shift register. The data sent from the $\overline{E}$ pin shifts at the fall of CL2. When SHL = V_{CC}, the data shifts from bit 1 to bit 80 in order of entry. When SHL = GND, the data shifts from bit 80 to bit 1.

Latch Circuit 1

Latch circuit 1 is composed of twenty 4-bit parallel data latches. It latches the display data D_0–D_3 at the fall of CL2 when the LSI is used as a column driver. The signals sent from the selector determine which 4-bit latch should latch the data.

Selector

The selector is composed of a 5-bit up and down counter and a decoder. When the LSI is used as a column driver, it generates the latch signal to be sent to latch circuit 1, incrementing the counter at the negative edge of CL2.

Controller

The controller operates when the LSI is used as a column driver. It stops data latching when twenty pulses of CL2 have been input (= power-down function) and automatically generates the chip enable signal announcing the start of data latching into the next LSI.

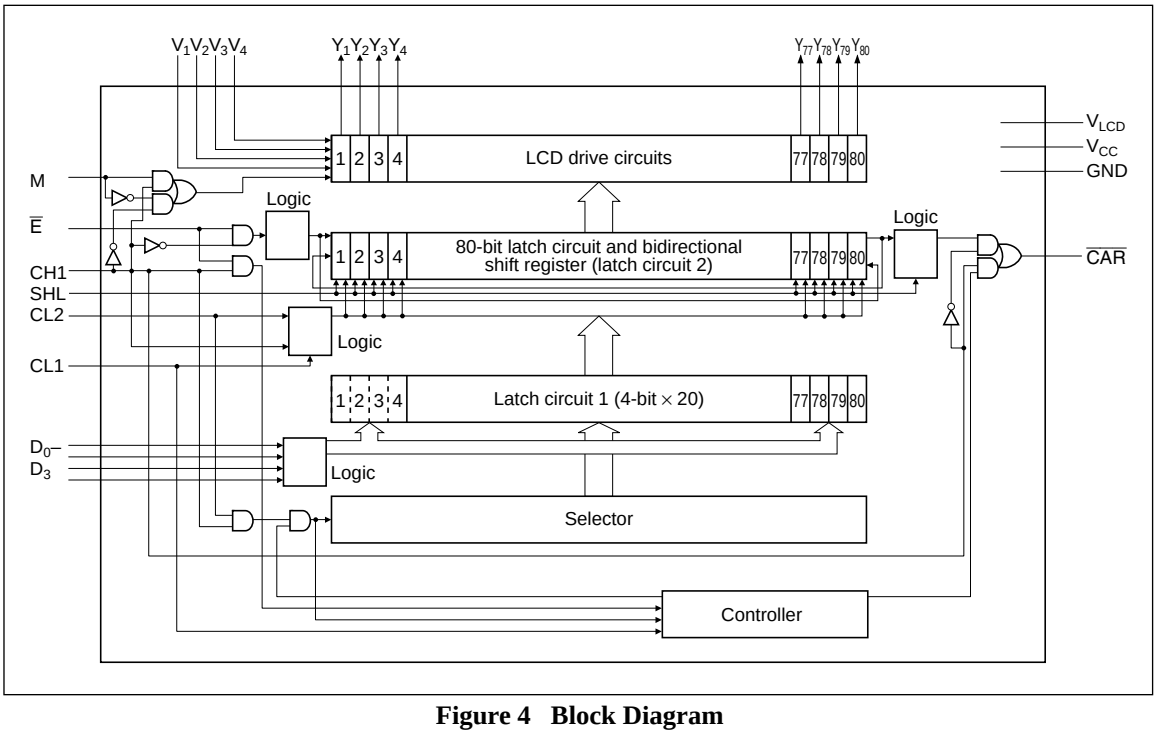


Figure 4 Block Diagram

Functional Description

When Used as a Column Driver

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Data outputs change at the fall of CL1. Latched data d_1 is transferred to the output pin Y_1 and d_{80} to Y_{80} when SHL = GND. Conversely, d_{80} is transferred to Y_1 and d_1 to Y_{80} when SHL = V_{CC}. The output level is selected out of V_1–V_4 according to the combination of display data and the alternating signal M (figure 5).

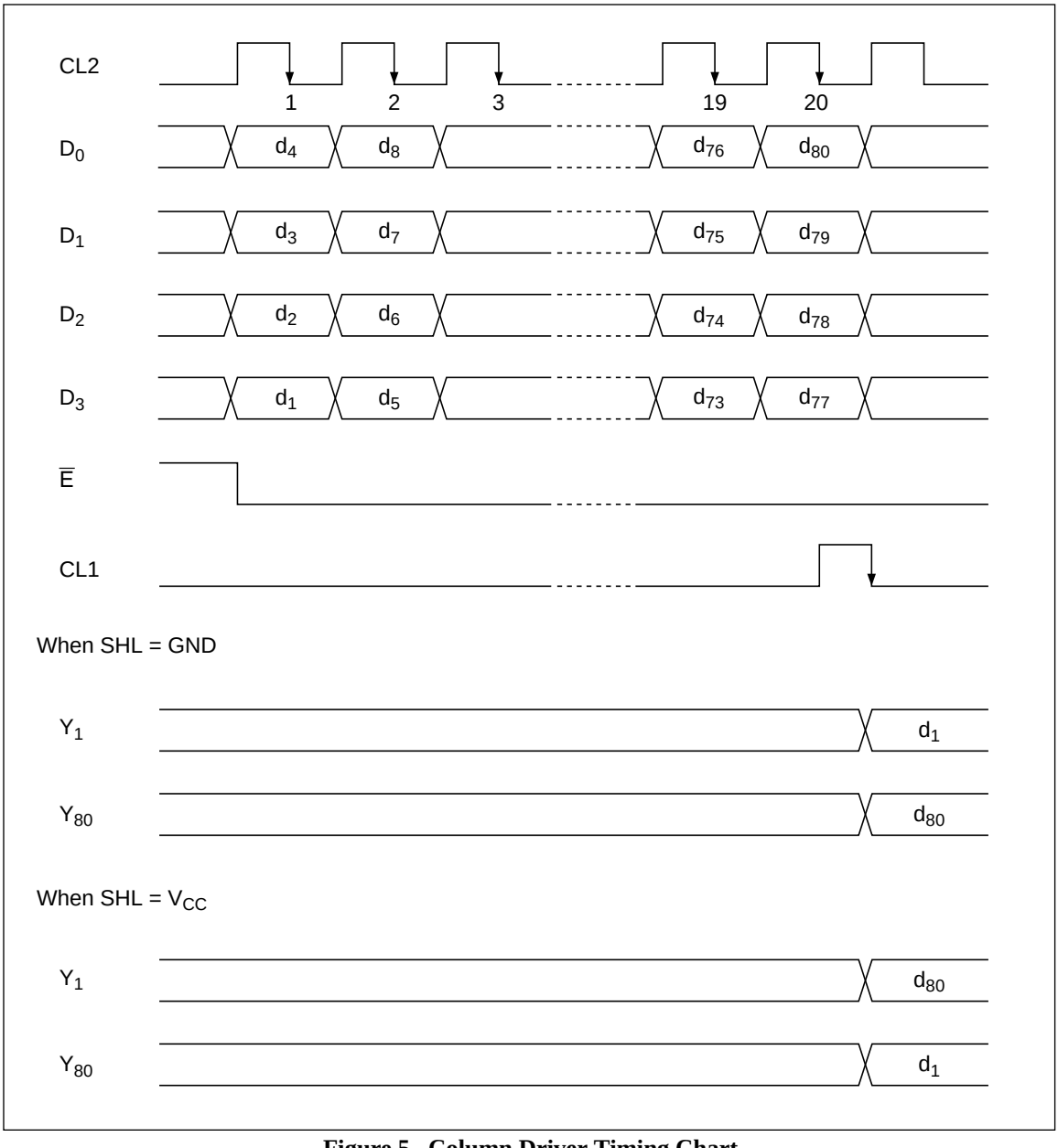


Figure 5 Column Driver Timing Chart

When Used as a Row Driver

The HD66106F shifts the line scan data sent from the pin $\overline{E}$ in order at the fall of CL2. When SHL = V_{CC}, data is shifted from Y_1 to Y_{80} and Y_{80} to Y_1 when SHL = GND.

In both cases, the data delayed for 80 bits by the shift register is output from the $\overline{CAR}$ pin to become the line scan data for the next LSI (figure 6).

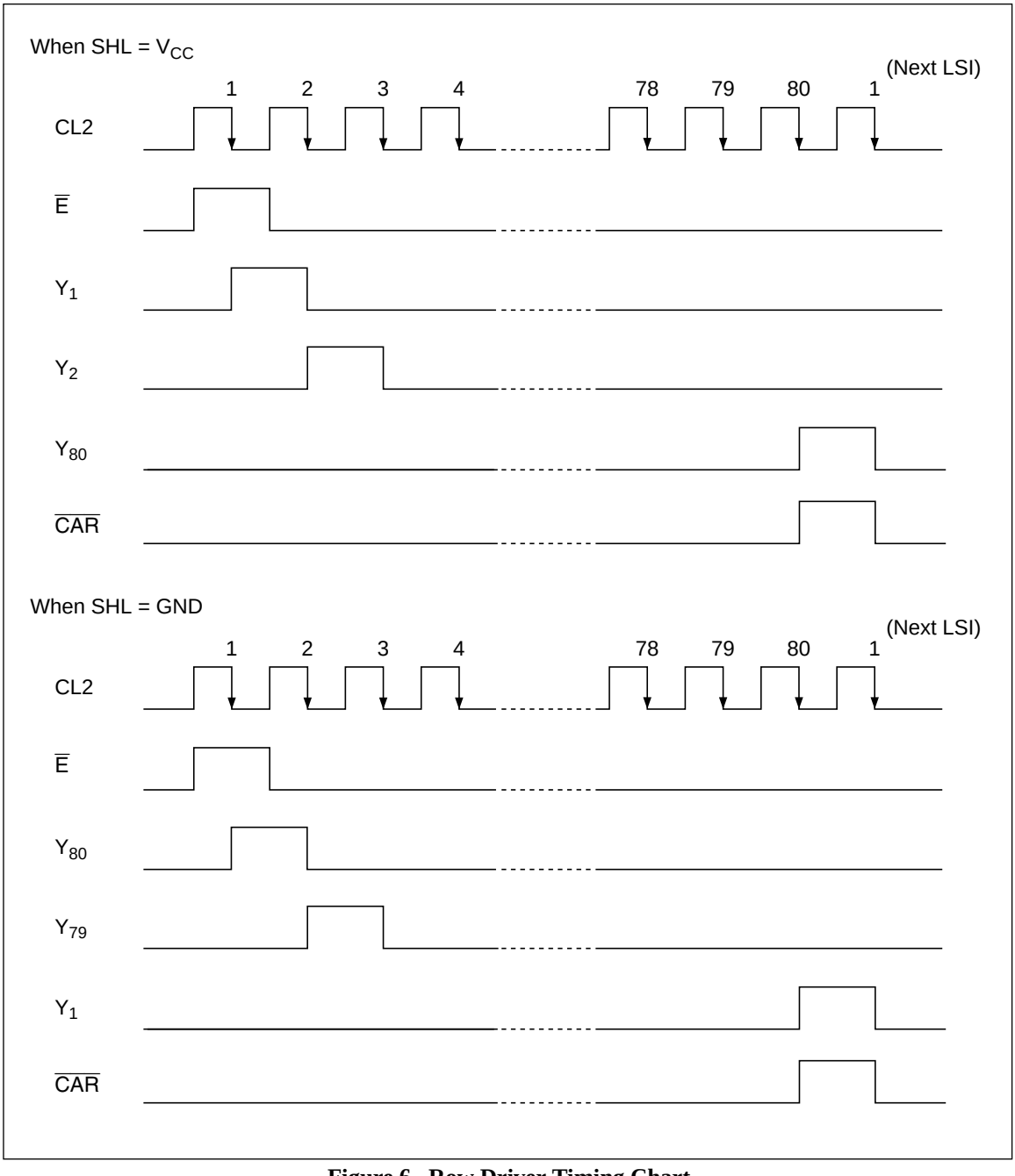


Figure 6 Row Driver Timing Chart

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 7). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}–GND (figure 8).

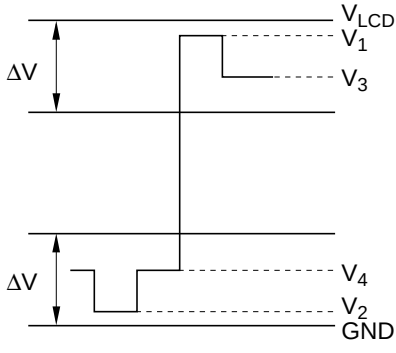


Figure 7 Driver's Output Waveform and Each Level of Voltage

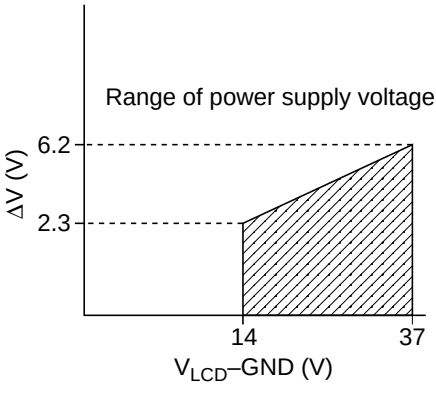
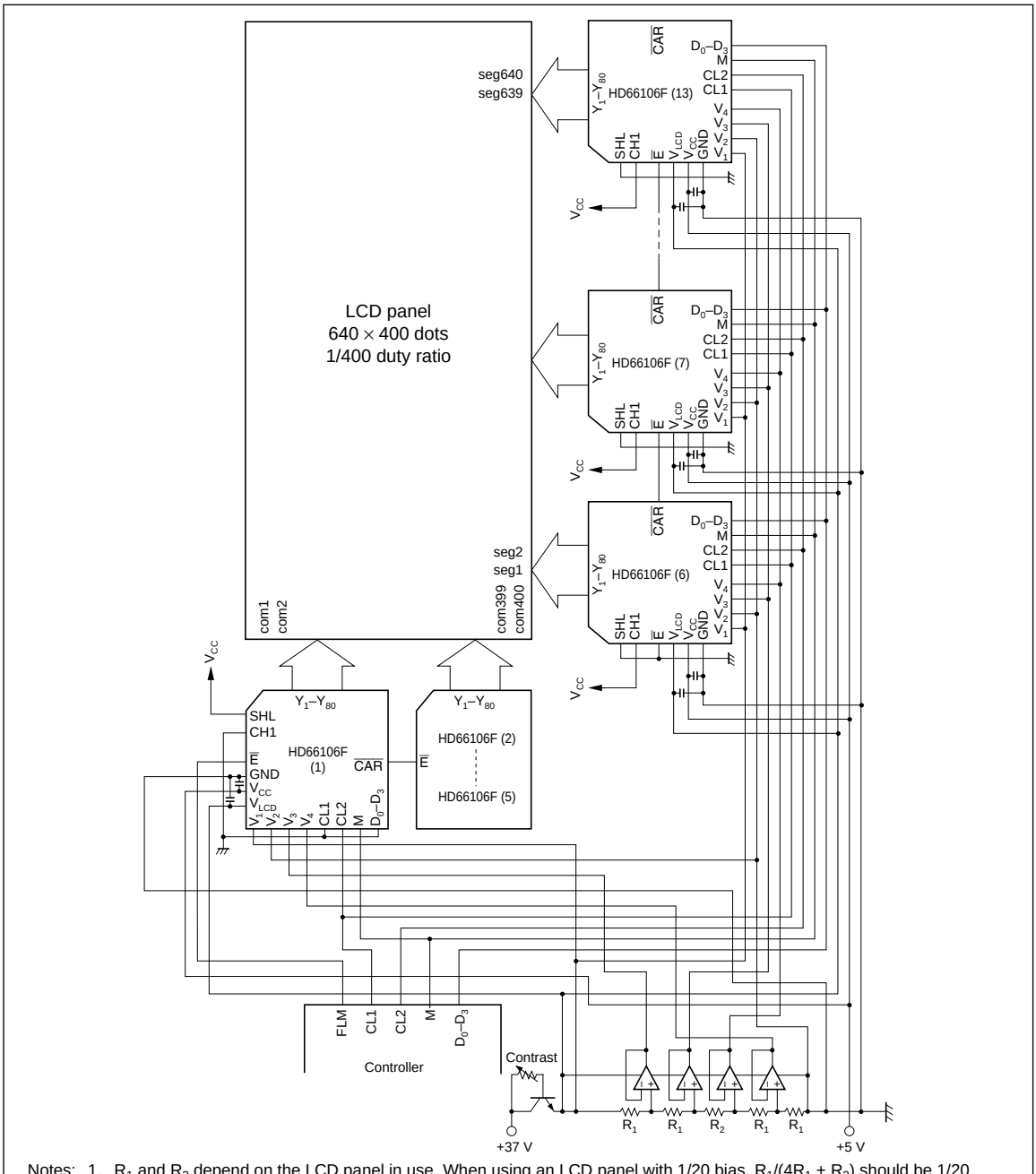


Figure 8 Power Supply Voltage V_{LCD}–GND and ΔV

Application Example

Application Diagram

Figure 9 shows an example of an LCD panel of 640 × 400 dots driven by HD66106Fs.



Notes: 1. R_1 and R_2 depend on the LCD panel in use. When using an LCD panel with 1/20 bias, $R_1/(4R_1 + R_2)$ should be 1/20. For example, R_1 = 3 kΩ and R_2 = 48 kΩ.

2. Use bypass capacitors to stabilize power supply when designing a board. It is desirable to use two capacitors with some 0.1 µF per LSI, putting one between V_{LCD} and GND, and the other between V_{CC} and GND.

Figure 9 Application Example

Timing Waveform Example

Figure 10 and 11 show the timing waveforms of the application example shown in figure 9.

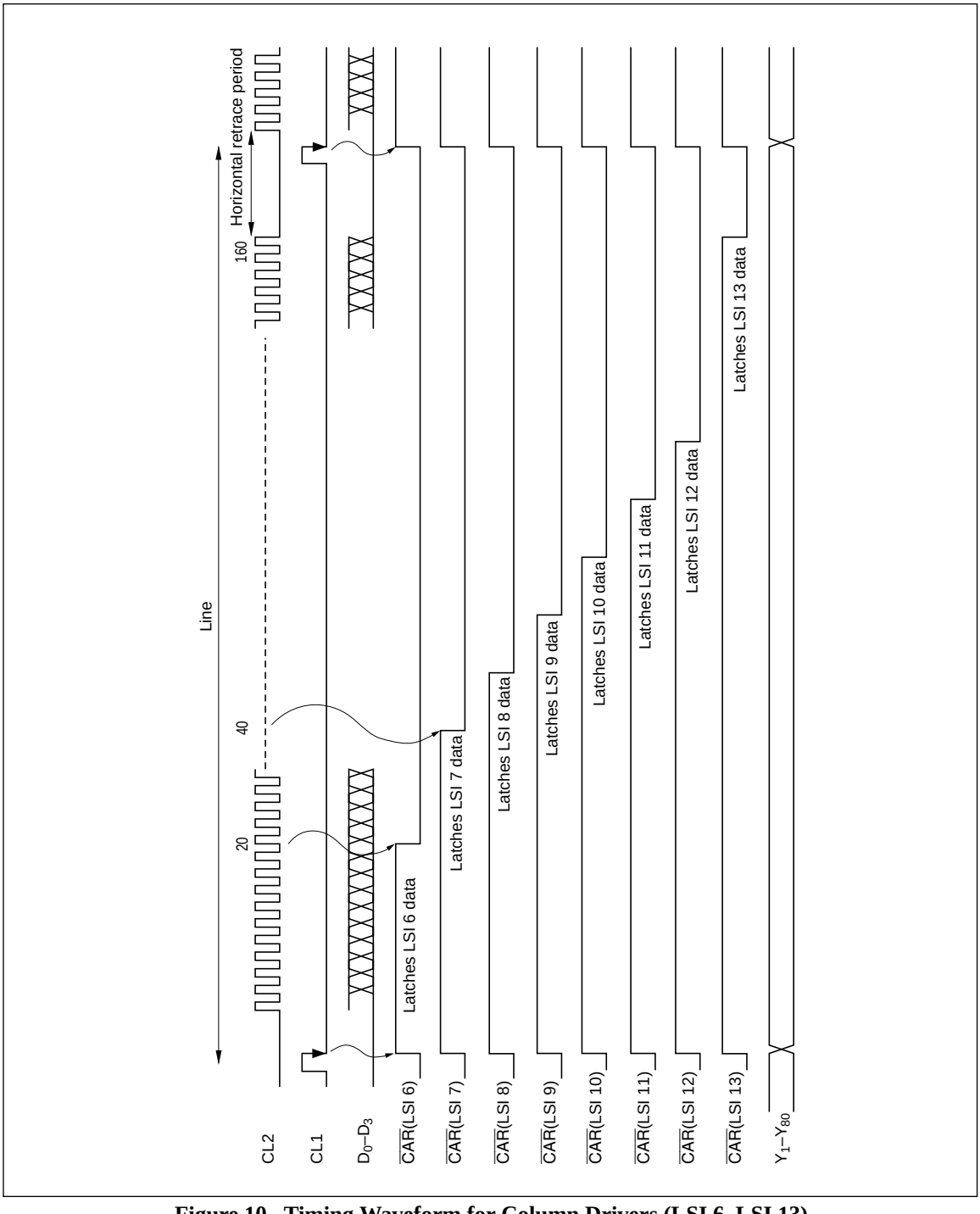


Figure 10 Timing Waveform for Column Drivers (LSI 6–LSI 13)

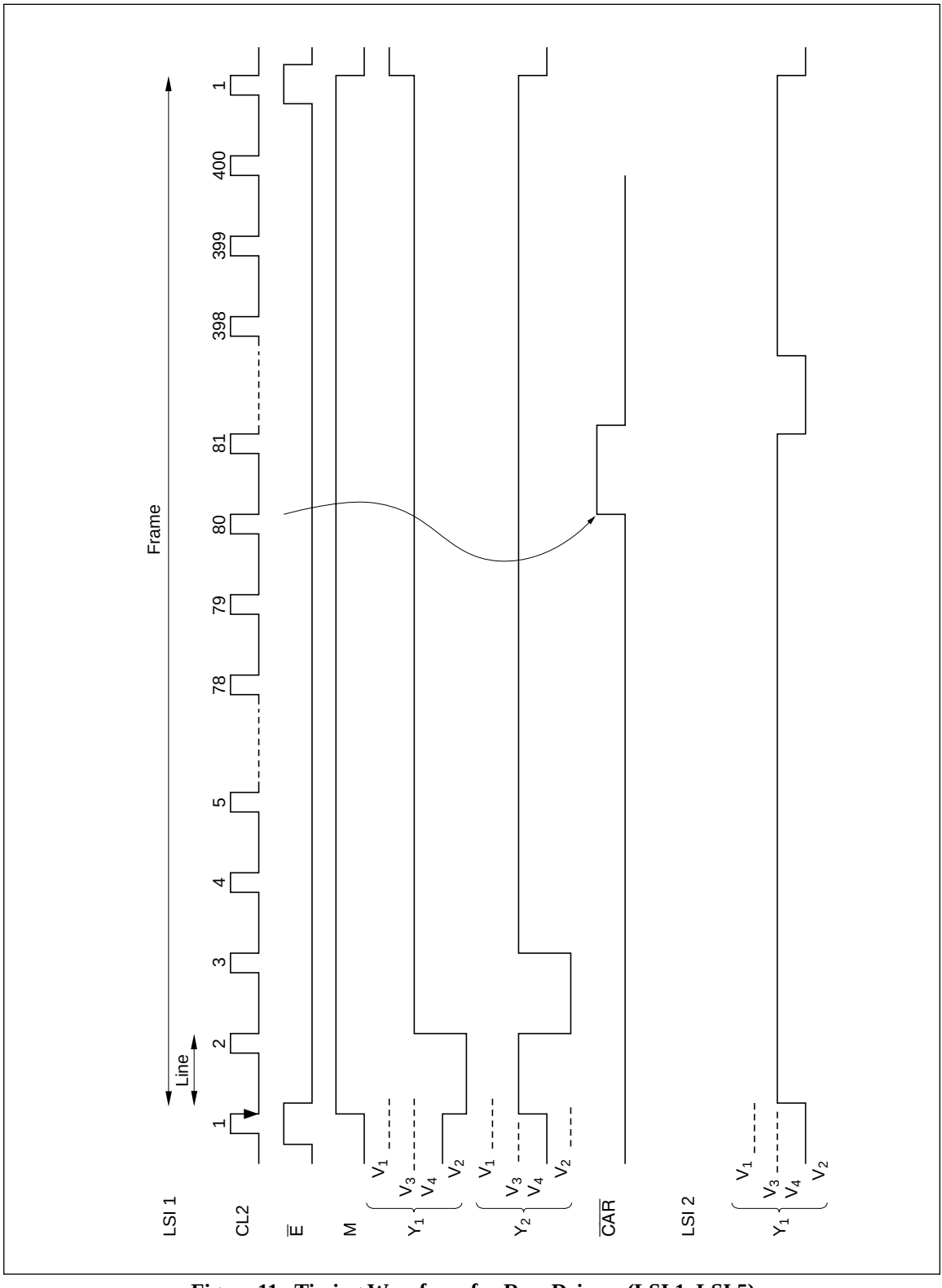


Figure 11 Timing Waveform for Row Drivers (LSI 1–LSI 5)

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Supply voltage	Logic circuits	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuits	V_{LCD}	–0.3 to +38	V	1
Input voltage (logic)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (LCD drive)		V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

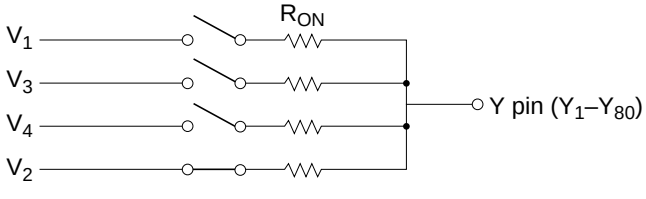
Notes: 1. Reference point is GND (= 0 V).
2. Applies to the input pins for logic circuits.
3. Applies to the input pins for LCD drive circuits.
4. Using an LSI beyond its maximum rating may result in its permanent destruction. LSIs should usually be used under electrical characteristics for normal operations. Exceeding any of these limits may adversely affect reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 V to 37 V, Ta = –20°C to 75°C unless otherwise noted)

Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage		V_{IH}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	0.8 × V_{CC}	—	V_{CC}	V		
Input low voltage		V_{IL}		0	—	0.2 × V_{CC}	V		
Output high voltage		V_{OH}	$\overline{CAR}$	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage		V_{OL}		—	—	0.4	V	I_{OL} = 0.4 mA	
Vi-Yj on resistance		R_{ON}	Y_1–Y_{80}, V_1–V_4	—	—	3.0	kΩ	I_{ON} = 100 µA	4
Input leakage current (1)		I_{IL1}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	–5.0	—	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current (2)		I_{IL2}	V_1–V_4	–50.0	—	50.0	µA	V_{IN} = V_{LCD} to GND	
Current consumption	(1)	I_{CC1}		—	—	3.0	mA	f_{CL2} = 6 MHz, f_{CL1} = 28 kHz	1
	(2)	I_{LCD1}		—	—	0.5	mA		2
	(3)	I_{ST}		—	—	0.2	mA	At the standby state f_{CL2} = 6 MHz, f_{CL1} = 28 kHz	
	(4)	I_{CC2}		—	—	0.2	mA	f_{CL1} = 28 kHz, f_m = 35 Hz	1
	(5)	I_{LCD2}		—	—	0.1	mA		3

Notes:
1. Input and output current is excluded. When the input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit. V_{IH} and V_{IL} must be fixed at V_{CC} and GND respectively to avoid it.
2. Applies when the LSI is used as a column driver.
3. Applies when the LSI is used as a row driver.
4. Indicates the resistance between Y pin and V pin (one of V_1, V_2, V_3, and V_4) when it supplies load current to one of Y_1–Y_{80} pins.
   Conditions: V_{LCD} – GND = 37 V
   V_1, V_3 = V_{LCD} – 2/20 (V_{LCD} – GND)
   V_2, V_4 = GND + 2/20 (V_{LCD} – GND)



AC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 V to 37 V, Ta = –20°C to +75°C unless otherwise noted)

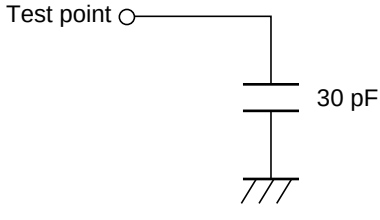
Column Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{cyc}	CL2	166	—	—	ns	
Clock high level width	t_{CWH}	CL2	50	—	—	ns	
Clock low level width	t_{CWL}	CL2	50	—	—	ns	
Clock setup time	t_{SCL}	CL2	200	—	—	ns	
Clock hold time	t_{HCL}	CL2	200	—	—	ns	
Clock rise/fall time	t_{ct}	CL1, CL2	—	—	30	ns	
Data setup time	t_{DSU}	D_0–D_3	30	—	—	ns	
Data hold time	t_{DH}	D_0–D_3	30	—	—	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	50	—	—	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	—	—	80	ns	1
M phase difference	t_{CM}	M, CL1	—	—	300	ns	

Row Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock low level width	t_{WL1}	CL2	5	—	—	µs	
Clock high level width	t_{WH1}	CL2	125	—	—	ns	
Data setup time	t_{DS}	$\overline{E}$	100	—	—	ns	
Data hold time	t_{DH}	$\overline{E}$	30	—	—	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	—	—	3	µs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	—	—	ns	1
Clock rise/fall time	t_{ct}	CL2	—	—	30	ns	

Note: 1. Values when the following load circuit is connected:



Column Driver

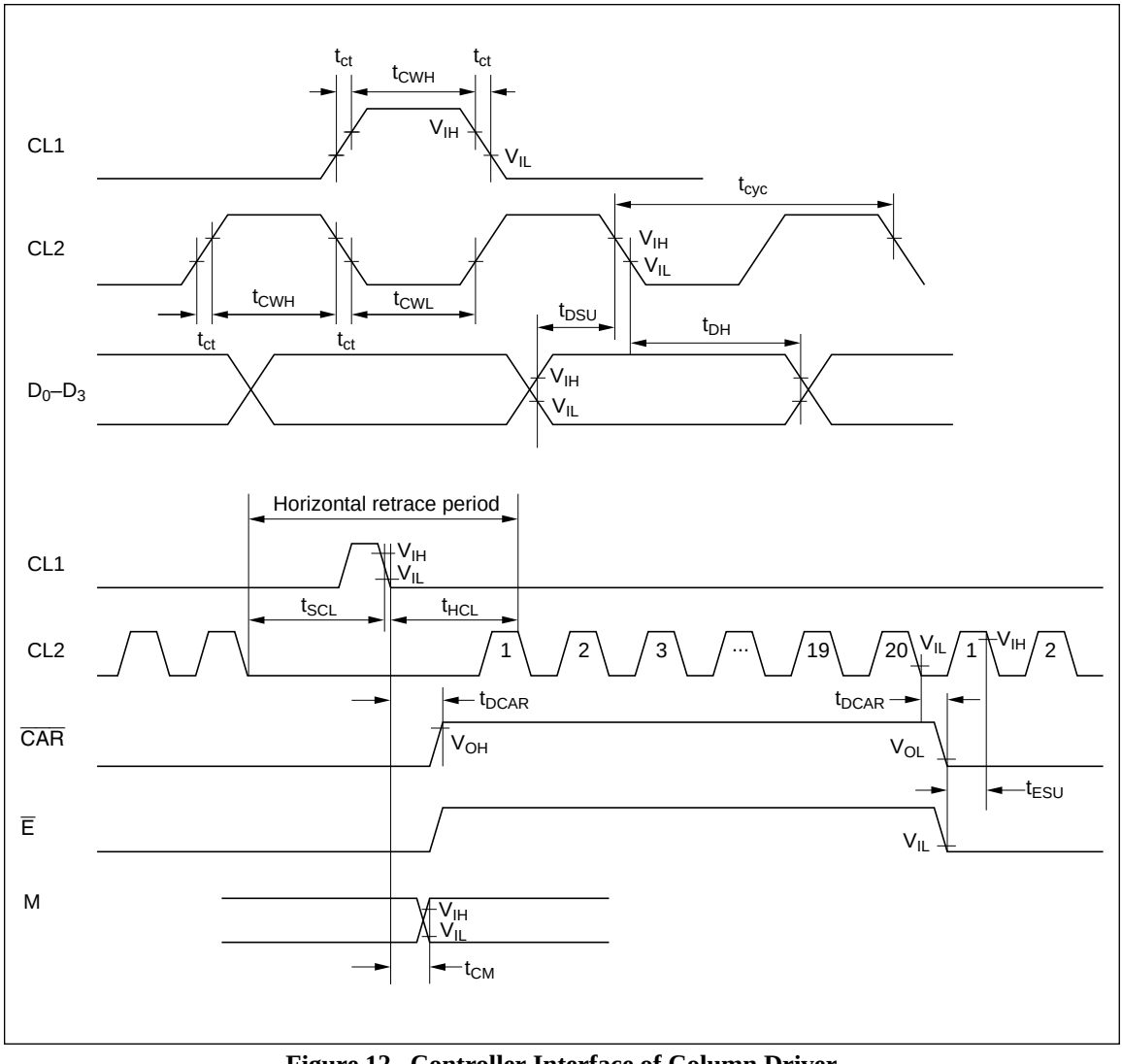


Figure 12 Controller Interface of Column Driver

Row Driver

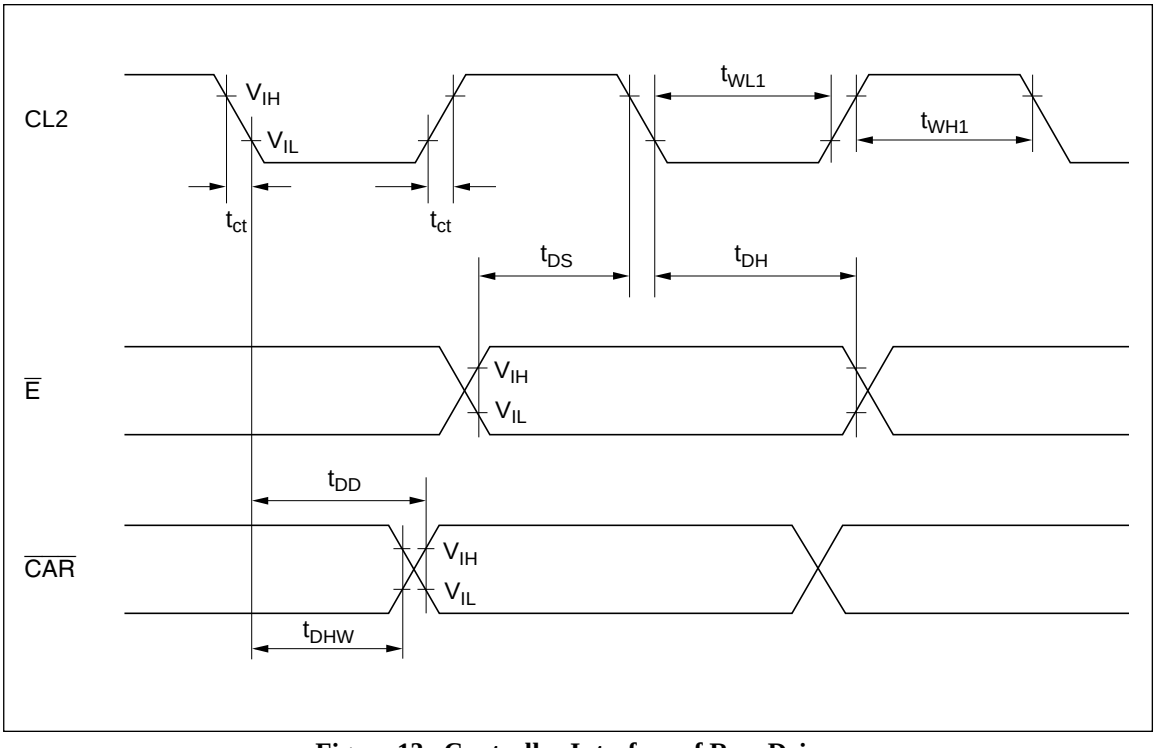


Figure 13 Controller Interface of Row Driver

HD66107T

(LCD Driver for High Voltage)

HITACHI

Description

The HD66107T is a multi-output, high duty ratio LCD driver used for large capacity dot matrix LCD panels. It consists of 160 LCD drive circuits with a display duty ratio up to 1/480: the seven HD66107Ts can drive a 640 × 480 dots LCD panel. Moreover, the LCD driver enables interfaces with various LCD controllers due to a built-in automatic generator of chip enable signals. Use of the HD66107T can help reduce the cost of an LCD-panel configuration, since it reduces the number of LCD drivers, compared with use of the HD61104 and HD61105.

Features

- Column and row driver
- 160 or 80 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit and 8-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby mode
- Recommended LCD controller LSIs: HD63645F, HD64645F, and HD64646FS (LCTC), HD66840/HD66841 (LVIC), HD66850 (CLINE)
- Power supply voltage
  - — Internal logic: +5 V ± 10%
  - — LCD drive circuit: 14.0 to 37.0 V
- Operation frequency: 8.0 MHz (max.)
- CMOS process
- 192-pin TCP

Ordering Information

Type No.	Number of Outputs	Outer Lead Pitch (µm)	Material of Tape*2	Note
HD66107T11	160	180	Kapton	
HD66107T24	160	180	Upilex	
HD66107T12	160	250	Kapton	
HD66107T00	160	280	Kapton	
HD66107T01	80	280	Kapton	12 perforated holes
HD66107T25	80	280	Kapton	8 perforated holes

Notes: 1. “Kapton” is a trademark of Dupont, Ltd.
“Upilex” is a trademark of Ube Industries, Ltd.
2. The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuits. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}: V_1 to V_4 supply power for driving an LCD (figure 1).

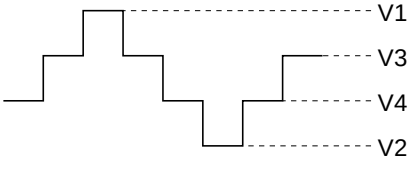
Control Signal

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

Table 1 Pin Function

Symbol	Pin No.	Pin Name	Input/Output
V_{CC}	167	V_{CC}	
GND	161, 186, 187	Ground	
V_{LCD}	166, 192	V_{LCD}	
V1L, R V2L, R V3L, R V4L, R	191, 165 188, 162 190, 164 189, 163	V1L, V1R V2L, V2R V3L, V3R V4L, V4R	
CL1	183	Clock 1	Input
CL2	184	Clock 2	Input
M	182	M	Input
D_0–D_7	174–181	DATA0–DATA7	Input
SHL	172	Shift left	Input
CH2	171	Channel 2	Input
BS	173	Bus select	Input
TEST	185	TEST	Input
Y1–Y160	1–160	Y1–Y160	Output
$\overline{E}$	169	Enable	Input
$\overline{CAR}$	168	Carry	Output
CH1	170	Channel	Input



V1, V2: Selected level
V3, V4: Nonselected level

Figure 1 Power Supply for Driving an LCD

M: M changes LCD drive outputs to AC.

D_0–D_7: D_0–D_7 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

$\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip devices are columns when CH1 = V_{CC}, and rows when CH1 = GND.

CH2: CH2 selects the number of output data bits. The number of output data bits is 160 when CH2 = GND, and 80 when CH2 = V_{CC}.

BS: BS selects the number of input data bits. When BS = V_{CC}, the chip latches 8-bits data. When BS = GND, the chip latches 4-bits data via D_0 to D_3. Fix D_4 through D_7 to GND.

TEST: Used for testing. Fixed to GND, otherwise.

Table 2 Relation between Display Data and LCD State

Display Data	LCD Output	LCD
1 (= high level)	V1L, R/V2L, R	On
0 (= low level)	Nonselected level	Off

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI Is Used as Row Driver)

SHL	Shift Direction of Shift Register					Scan Direction of Selected Line				
V_{CC}	E→	1→	2→	3→	4----------→160	Y1→	Y2→	Y3→	Y4	----------→Y160
GND	E→	160→	159→	158→	157----------→1	Y160→Y159→Y158→Y157				----------→Y1

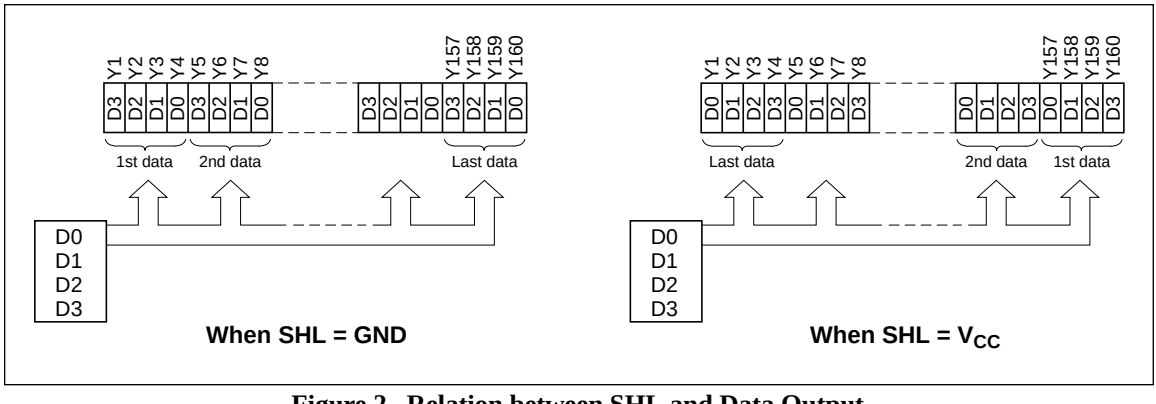


Figure 2 Relation between SHL and Data Output

LCD Drive Interface

Y1–Y160: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, V_4—according to the combination of M and display data (figure 3).

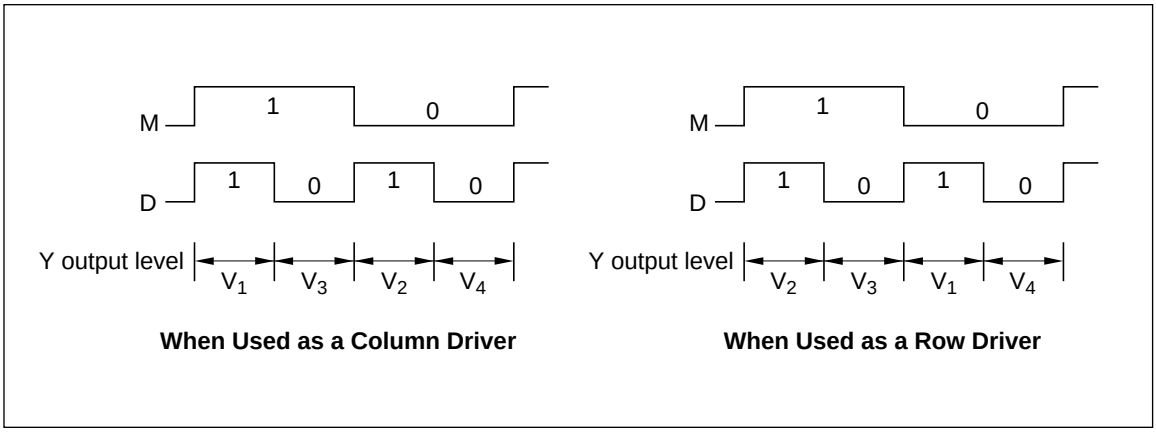
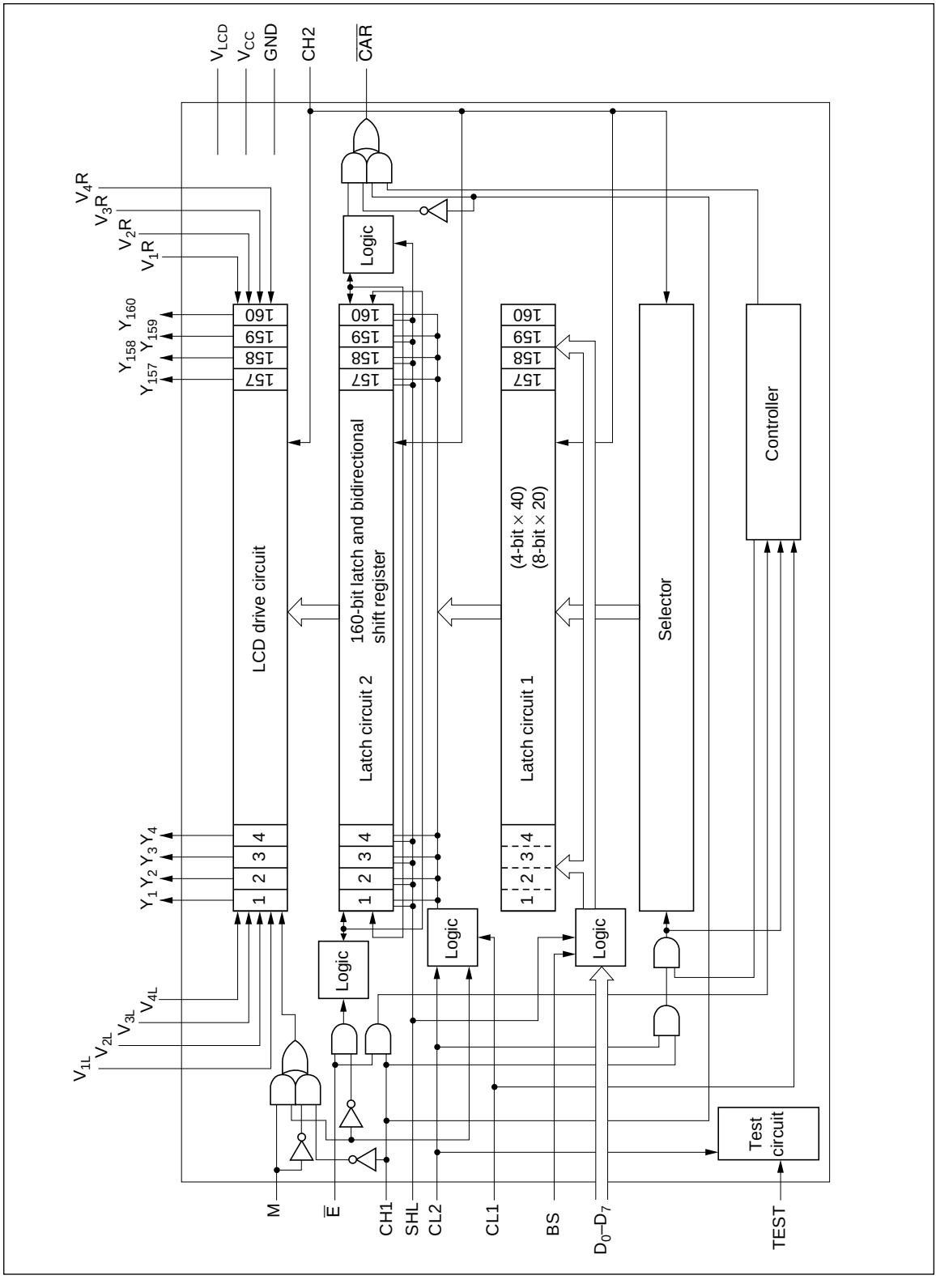


Figure 3 Selection of LCD Driver Output Level

Block Diagram



Function

LCD Drive Circuits

The LCD drive circuits generate four levels of voltages—V_1, V_2, V_3, and V_4—for driving an LCD. They select and transfer one of the four levels to the output circuit according to the combination of M and the data in the latch circuit 2.

Latch Circuit 2

Latch circuit 2 is used as a 160-bit latch circuit during column driving. Latch circuit 2 latches data input from latch circuit 1 at the falling edge of CL1 and outputs latched data to the drive circuits.

In the case of row driving, latch circuit 2 is used as a 160-bit bidirectional shift register. Data input from $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted in input order from bit 1 to bit 160 of the shift register. When SHL = GND, data is shifted from bit 160 to bit 1 of the register. Moreover, this latch circuit can be used as an 80-bit shift register. In this case, Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Latch Circuit 1

Latch circuit 1 consists of twenty 8-bit parallel data latch circuits. It latches data D_0 through D_7 at the falling edge of CL2 during column driving. The selector signals specify which 8-bit circuit latches data. Moreover, this circuit can be used as forty 4-bit parallel data latch circuits by switching BS, in which case the circuit latches data D_0 through D_3. Moreover, this latch circuit can be used as an 80-bit shift register. In this case Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Selector

The selector consists of a 6-bit up and down counter and a decoder. During column driving it generates a latch signal for latch circuit 1, incrementing the counter at the falling edge of CL2.

Controller

This controller is enabled during column driving. It provides a power-down function which detects completion of data latch and stops LSI operations.

Moreover, the controller automatically generates a chip enable signal ($\overline{CAR}$) which starts next-stage data latching.

Test Circuit

The test circuit divides the external clock and generates test signals.

Fundamental Operations

Column Driving (1)

- CH2 = GND (160-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

The HD66107T starts data latch when $\overline{E}$ is at low level. In this case, 8-bit parallel data is latched at the falling edge of CL2. When 160-bit data latch is completed, the HD66107T automatically stops and enters standby mode and $\overline{CAR}$ is goes to low level. If $\overline{CAR}$ is connected with $\overline{E}$ of the next-stage LSI, this next-stage LSI is activated when $\overline{CAR}$ of the previous LSI goes low.

Data is output at the falling edge of CL1. When SHL = GND, data d_1 is output to pin Y_1 and d_{160} to Y_{160}. On the other hand, when SHL = V_{CC}, data d_{160} is output to pin Y_1 and d_1 to Y_{160}. The output level is selected from among V_1–V_4 according to the combination of display data and alternating signal M. See figure 4.

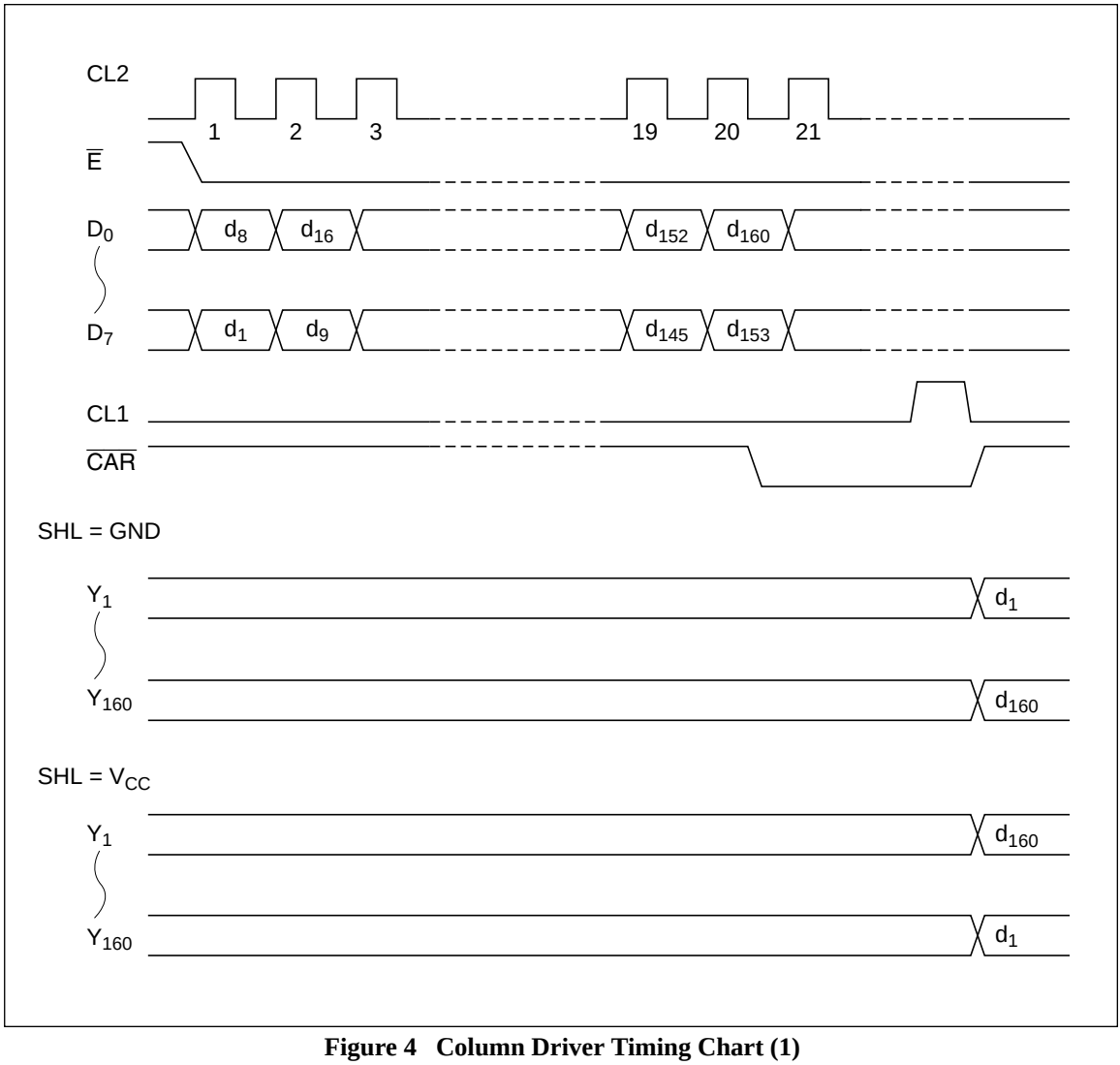


Figure 4 Column Driver Timing Chart (1)

Column Driving (2)

- CH2 = GND (160-bit data output mode)
- BS = GND (4-bit data latch mode)

4-bit display data (D_0–D_3) is latched at the falling edge of CL2. Other operations are performed in the same way as described in "Column Driving (1)". See figure 5.

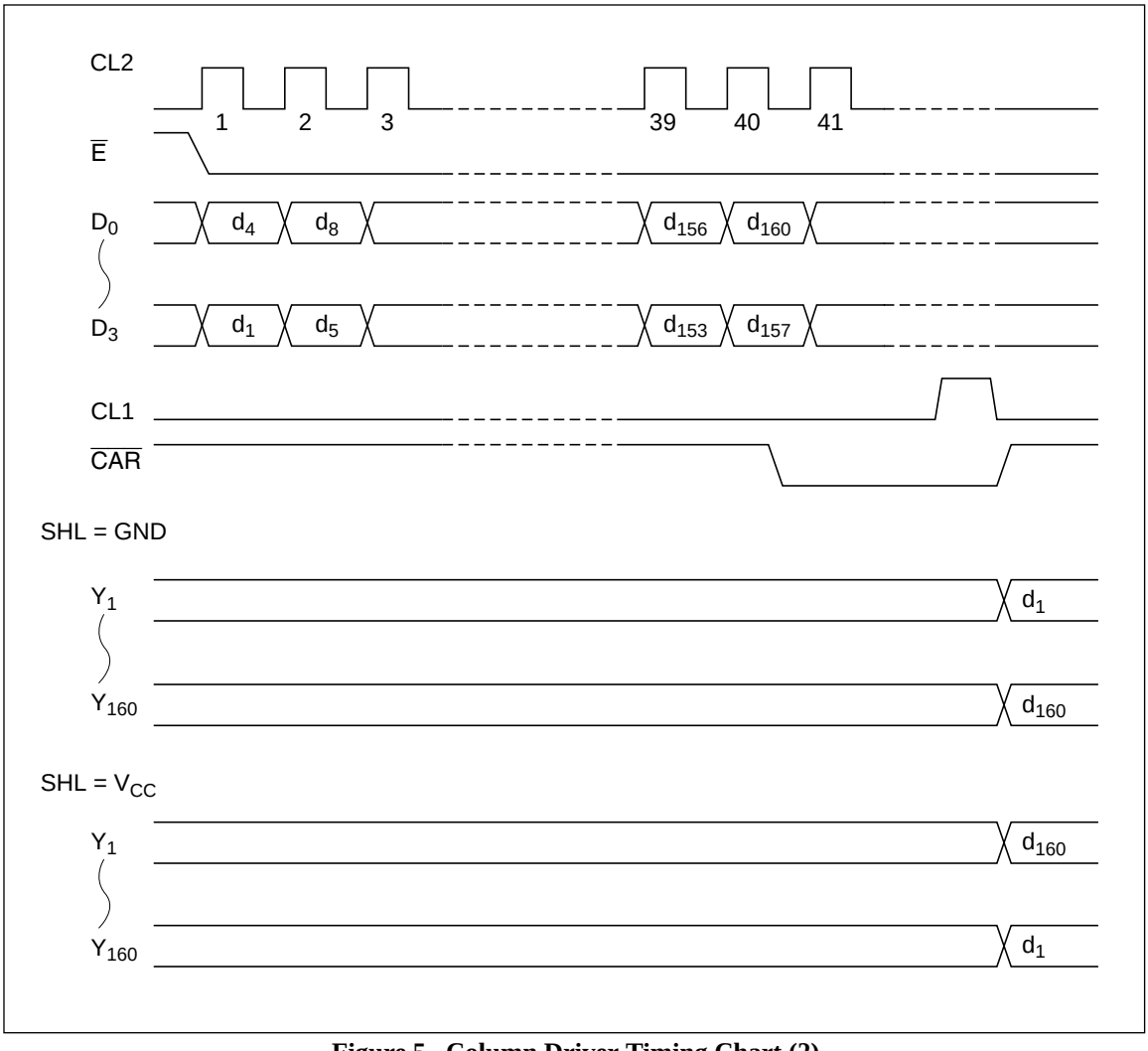


Figure 5 Column Driver Timing Chart (2)

Column Driving (3)

- CH2 = V_{CC} (80-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

When CH2 is high (V_{CC}), the HD66107T can be used as an 80-bit column driver. In this case, Y_{41} through Y_{120} are enabled, the states of Y_1 through Y_{40} and Y_{121} through Y_{160} remain unchanged.

When SHL = GND, data d_1 is output to pin Y_{41} and d_{80} is output to Y_{120}. Conversely, when SHL = V_{CC}, data d_{80} is output to Y_{41} and d_1 is output to Y_{120}. See figure 6.

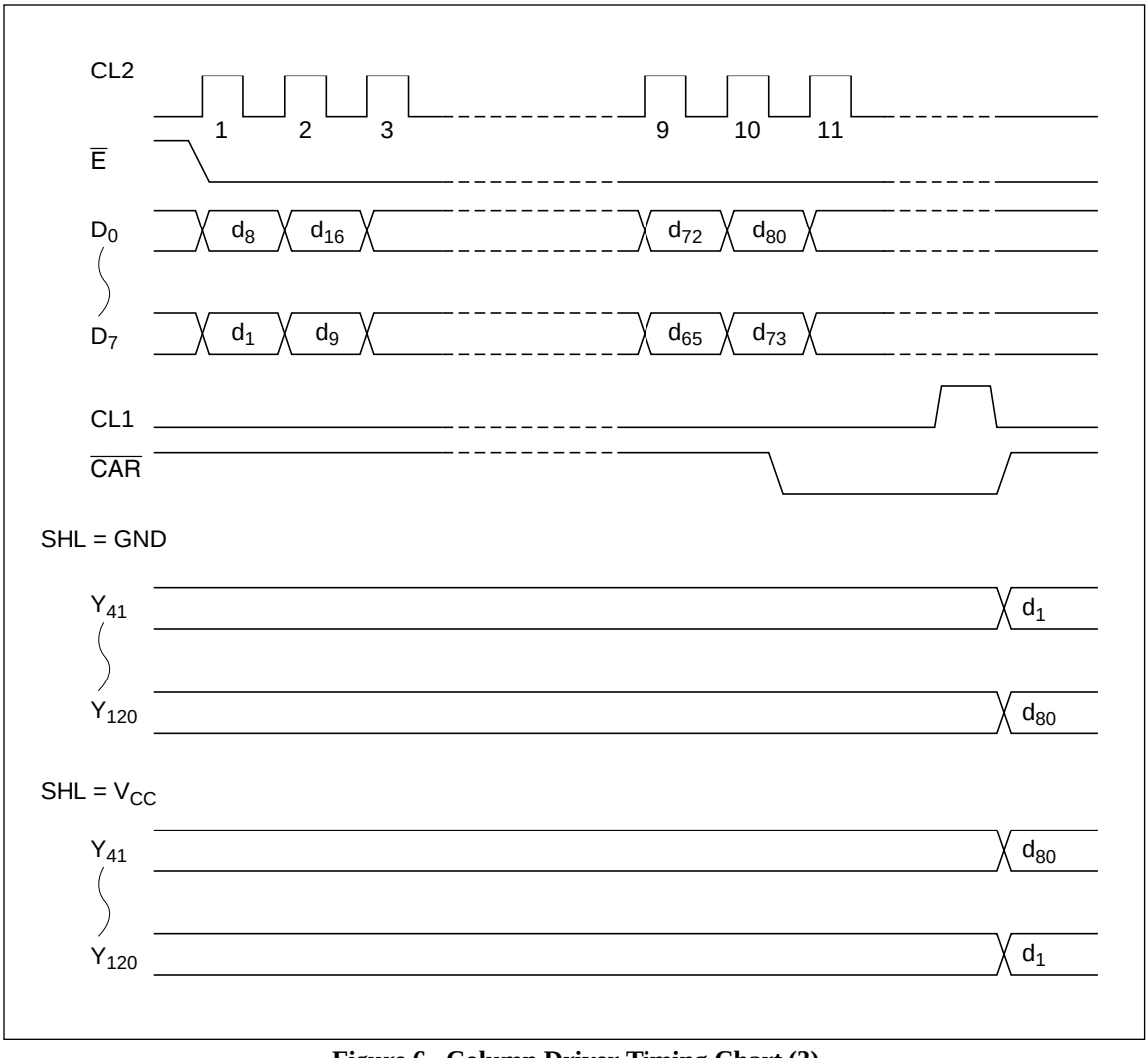


Figure 6 Column Driver Timing Chart (3)

Column Driving (4)

- CH2 = V_{CC} (80-bit data output mode)
- BS = GND (4-bit data latch mode)

When CH2 = V_{CC} and BS = GND, 4-bit parallel data is latched, while 80-bit data is output. The output of latched data is performed in described in "Column Driving (3)." See figure 7.

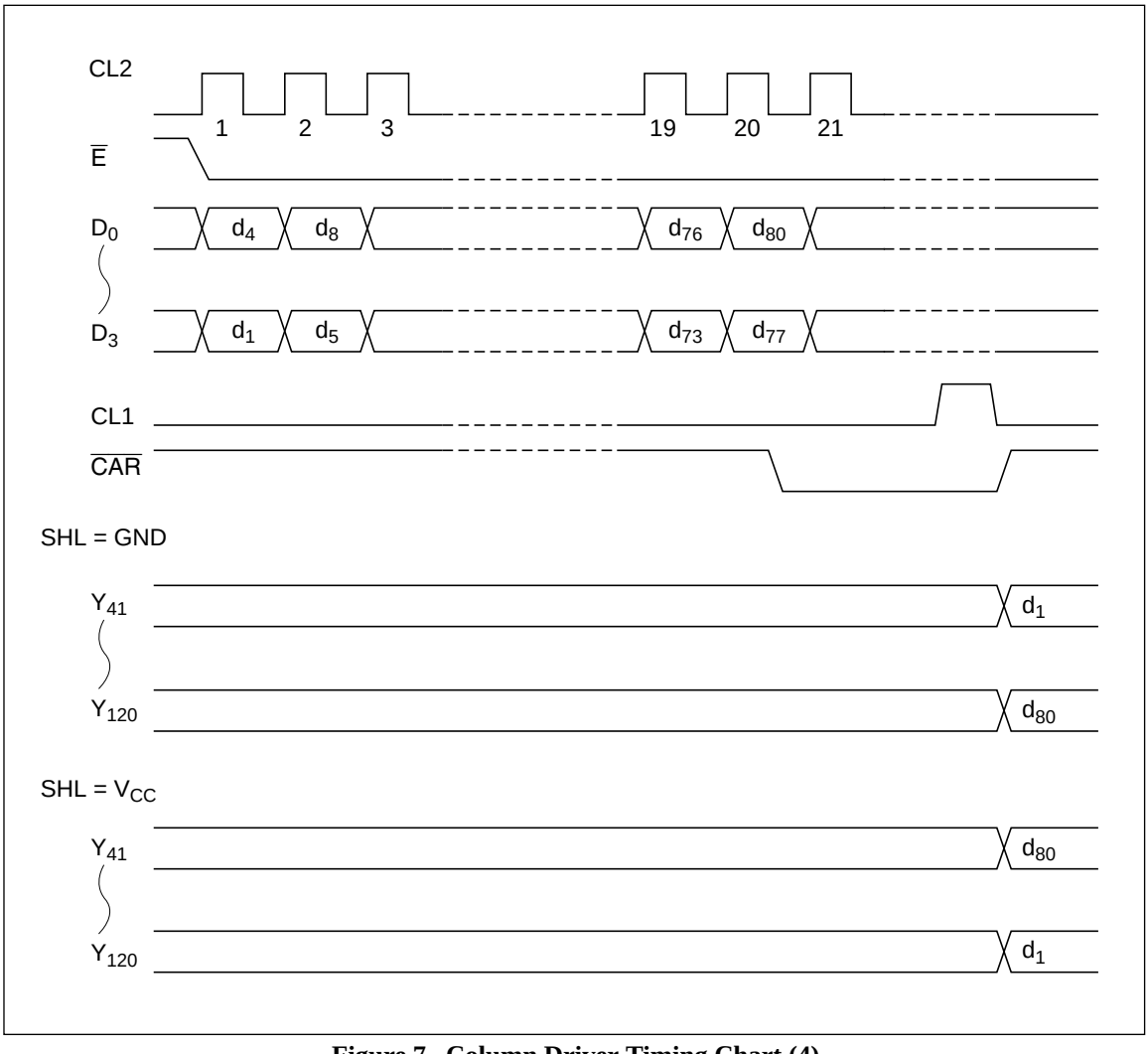


Figure 7 Column Driver Timing Chart (4)

Row Driving (1)

- CH2 = GND (160-bit data output mode)

The HD66107T shifts line scan data input through $\overline{E}$ at the falling edge of CL2.

When SHL = V_{CC}, 160-bit data is shifted from Y_1 to Y_{160}, whereas when SHL = GND, data is shifted from Y_{160} to Y_1. In both cases the HD66107T outputs the data delayed for 160 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next IC driver. See figure 8.

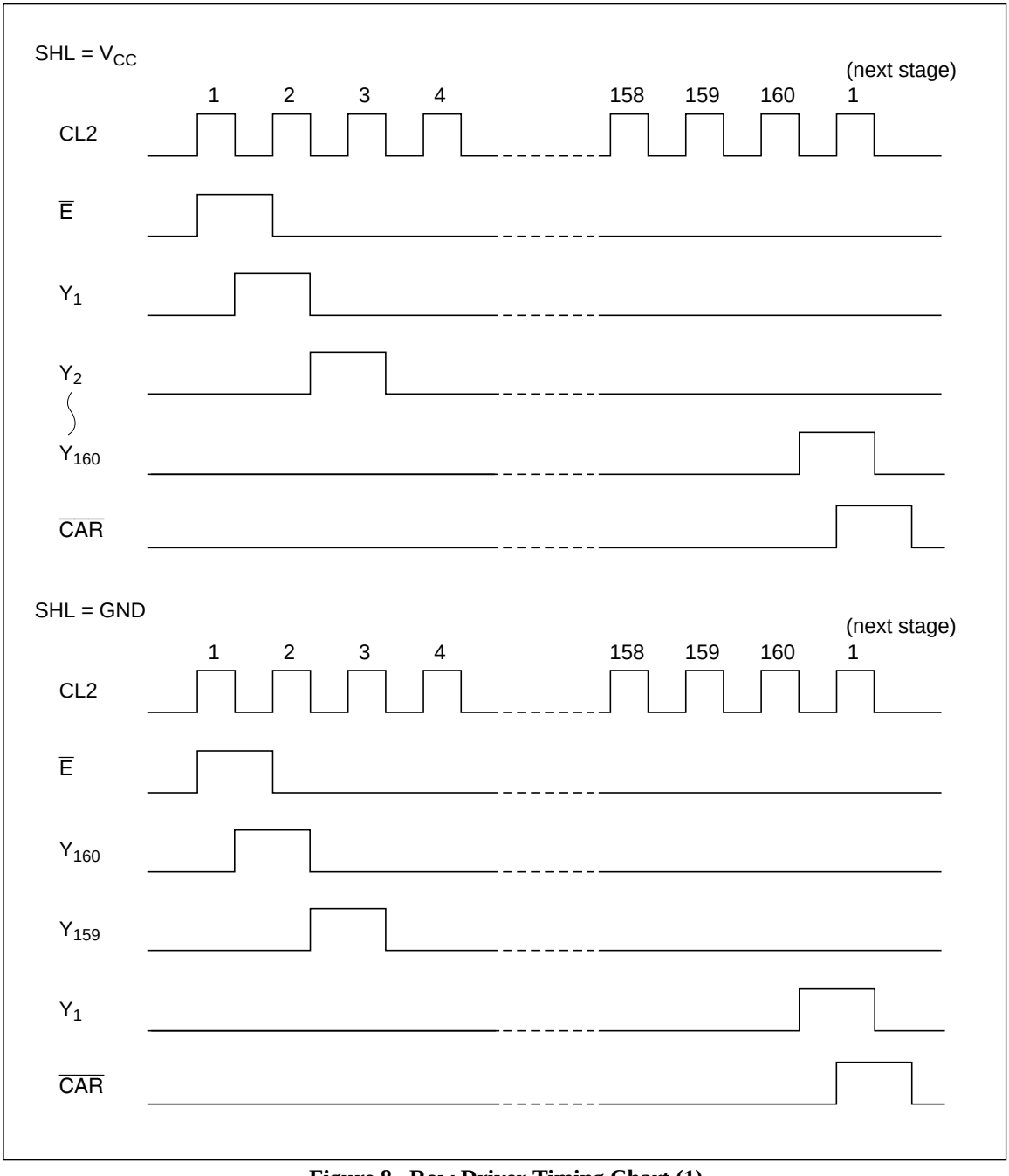


Figure 8 Row Driver Timing Chart (1)

Row Driving (2)

- CH2 = V_{CC} (80-bit data output mode)

When CH2 is high, the HD66107T can be used as an 80-bit row driver. In this case, Y_{41} to Y_{120} are enabled, while the other bits remain unchanged.

Line scan data input through $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted from Y_{41} to Y_{120}. Conversely, when SHL = GND, data is shifted from Y_{120} to Y_{41}. In both cases the HD66107T outputs the data delayed for 80 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next LSI. See figure 9.

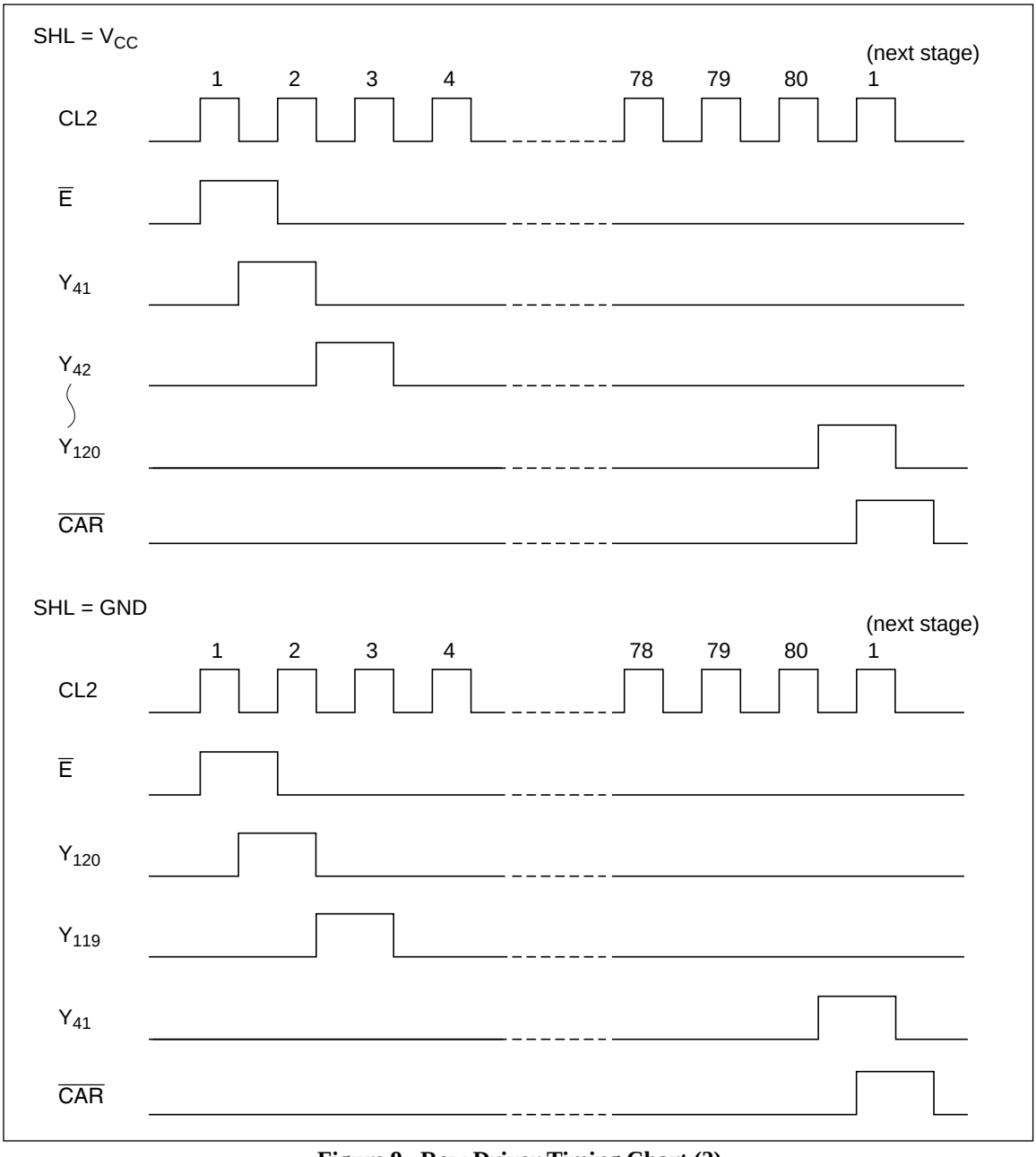
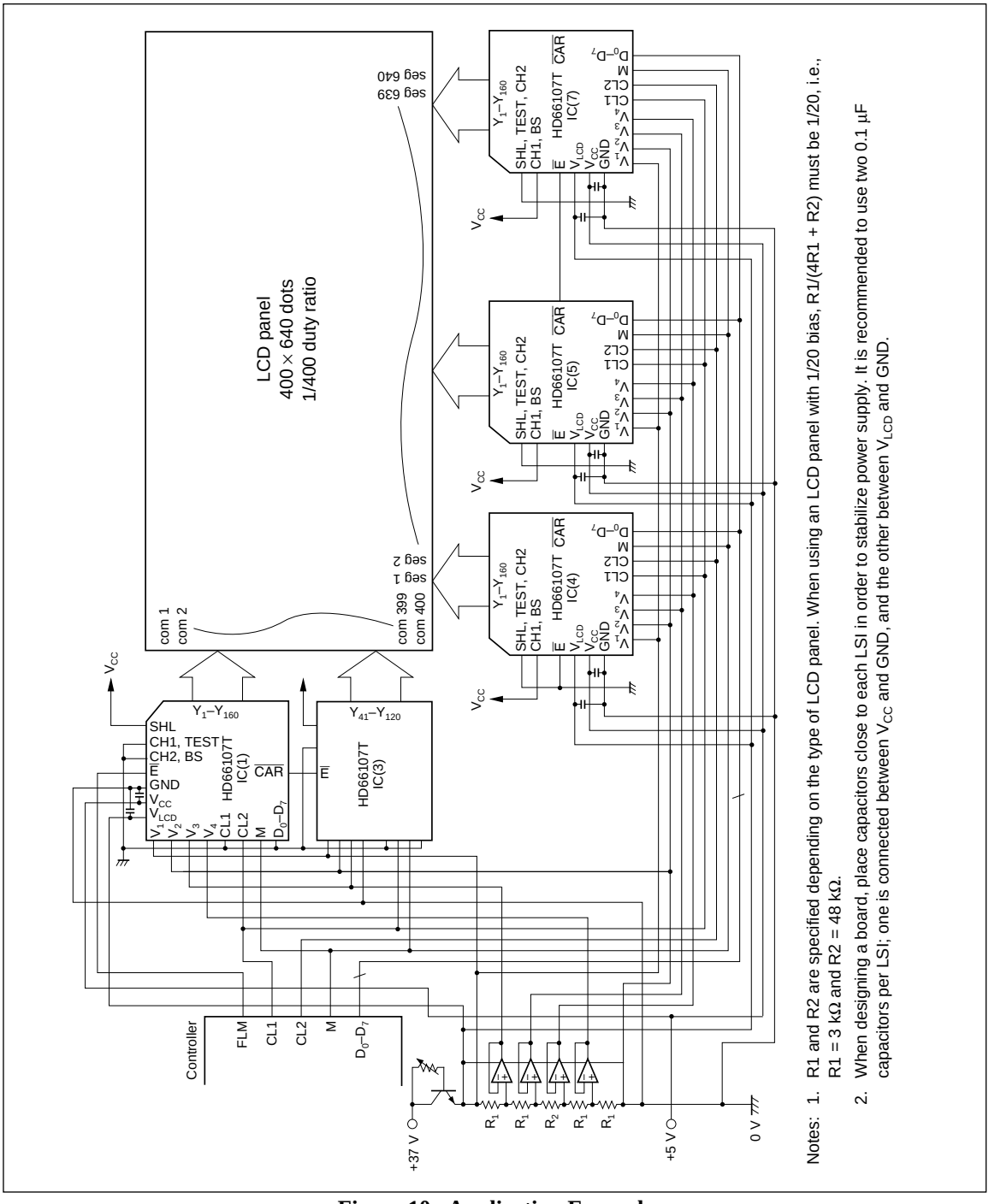


Figure 9 Row Driver Timing Chart (2)

Application

The following example shows a system configuration for driving a 640 × 400-dot LCD panel using the HD66107T.



Notes: 1. R1 and R2 are specified depending on the type of LCD panel. When using an LCD panel with 1/20 bias, R1/(4R1 + R2) must be 1/20, i.e., R1 = 3 kΩ and R2 = 48 kΩ.

2. When designing a board, place capacitors close to each LSI in order to stabilize power supply. It is recommended to use two 0.1 µF capacitors per LSI; one is connected between V_{CC} and GND, and the other between V_{LCD} and GND.

Figure 10 Application Example

Waveform Examples

Column Driving

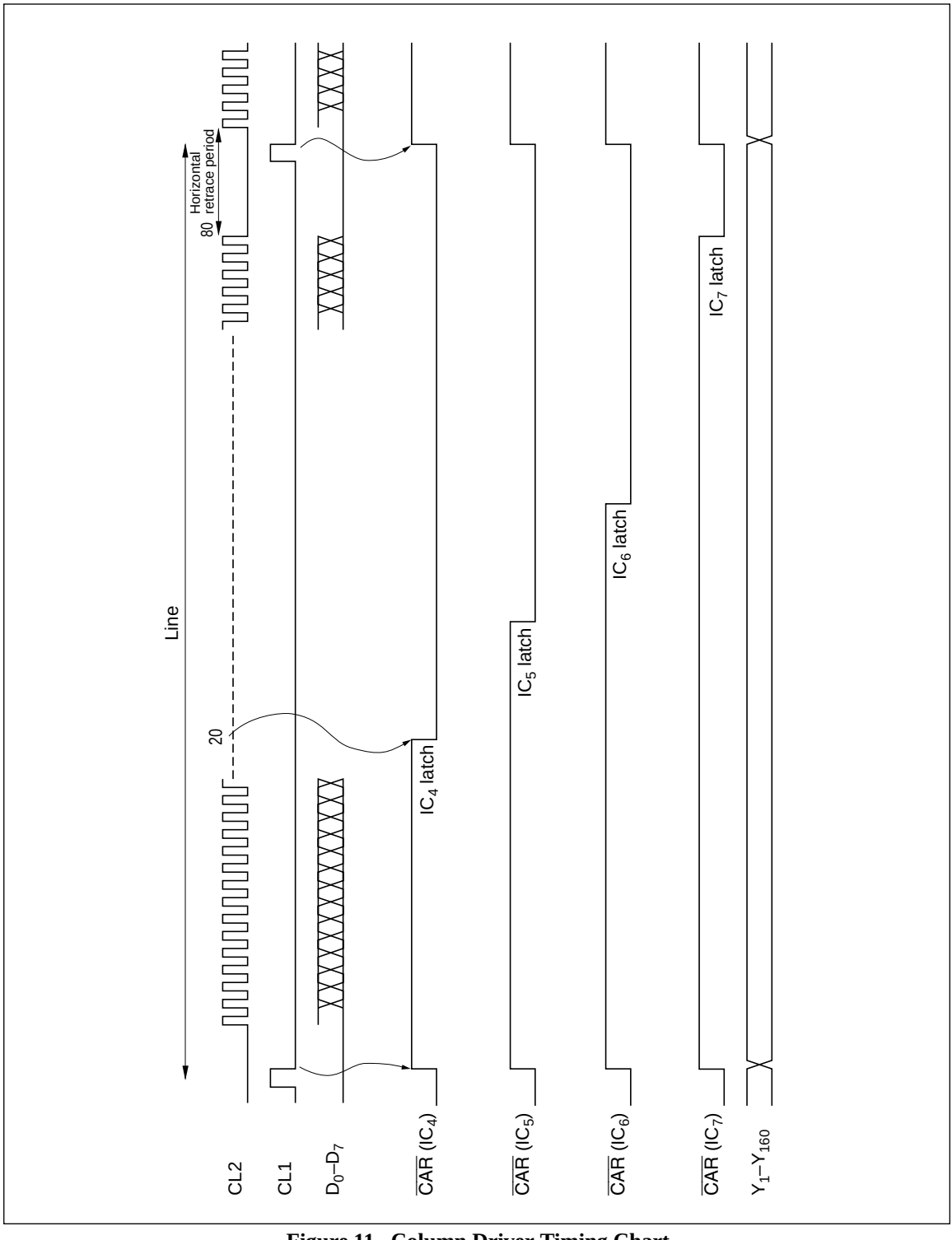


Figure 11 Column Driver Timing Chart

Row Driving

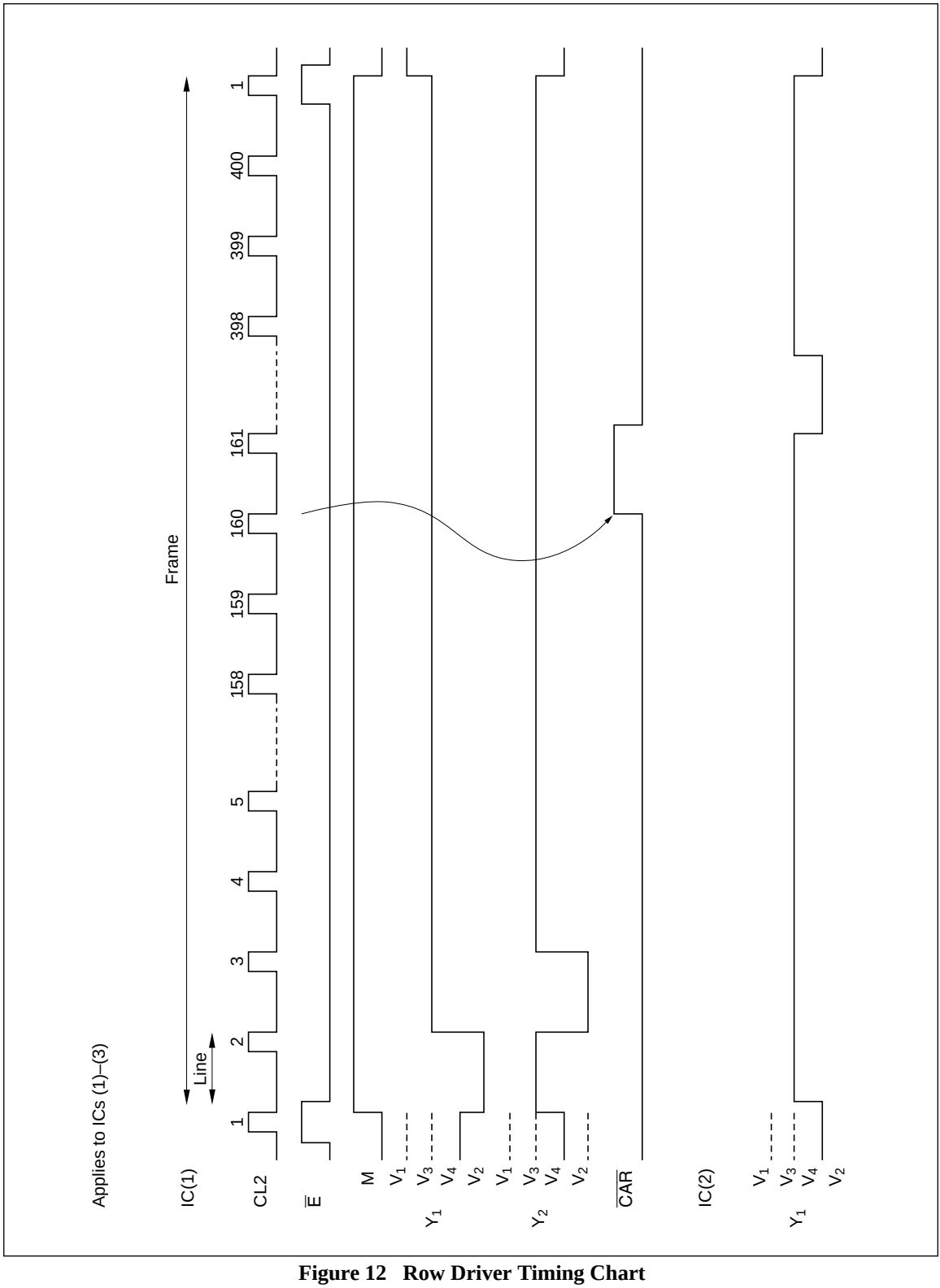


Figure 12 Row Driver Timing Chart

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuit	V_{LCD}	–0.3 to +38	V	1
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. Reference point is GND (= 0 V).
2. Applies to input pins for logic circuit.
3. Applies to input pins for LCD drive circuits.
4. If the LSI is used beyond absolute maximum ratings, it may be permanently damaged. It should always be used within the above electrical characteristics to prevent malfunction or degradation of the LSI's reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ±10%, V_{LCD} = 14 to 37 V, Ta = –20 to 75°C)

Item	Symbol	Pin	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL, BS, CH2, TEST, D_0–D_7, $\overline{E}$, CH1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}		0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}		—	0.4	V	I_{OL} = 0.4 mA	
Vi–Vj on resistance	R_{ON}	Y1–Y160, V1–V4	—	3.0	kΩ	I_{ON} = 150 µA	4
Input leak current (1)	I_{IL1}	CL1, CL2, M, SHL, BS, CH2, TEST, D_0–D_7, $\overline{E}$, CH1	–5.0	5.0	µA	V_{IN} = V_{CC} – GND	
Input leak current (2)	I_{IL2}	V1–V4	–100	100	µA	V_{IN} = V_{LCD} – GND	
Power dissipation (1)	I_{CC1}		—	5.0	mA	f_{CL2} = 8 MHz f_{CL1} = 28 kHz	1, 2
Power dissipation (2)	I_{LCD1}		—	2.0	mA		
Power dissipation (3)	I_{ST}		—	0.5	mA	In standby mode: f_{CL2} = 8 MHz, f_{CL1} = 28 kHz	1, 2
Power dissipation (4)	I_{CC2}		—	1.0	mA	f_{fCL1} = 28 kHz fm = 35 Hz	1, 3
Power dissipation (5)	I_{LCD2}		—	0.5	mA		

Notes: 1. Input and output current is excluded. When an input is at the intermediate level is CMOS, excessive current flows from the power supply though the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed to V_{CC} and GND respectively.

2. Applies to column driving.

3. Applies to row driving.

4. Indicates the resistance between one pin from Y_1–Y_{160} and another pin from V_1–V_4 when load current is applied to the Y pin; defined under the following conditions.

   V_{LCD}–GND = 37 V
   V1, V3 = V_{LCD} – {2/20 (V_{LCD}–GND)}
   V2, V4 = V_{LCD} + {2/20 (V_{LCD}–GND)}

   This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltage should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 13).
   Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}–GND (figure 14).

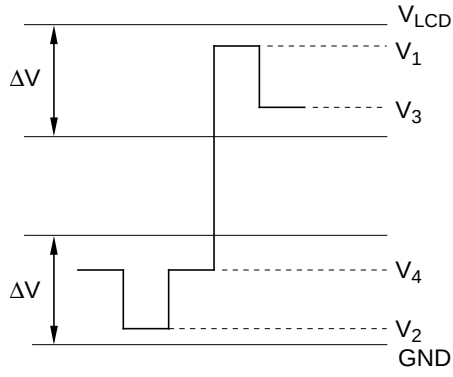


Figure 13 Driver's Output Waveform and Each Level of Voltage

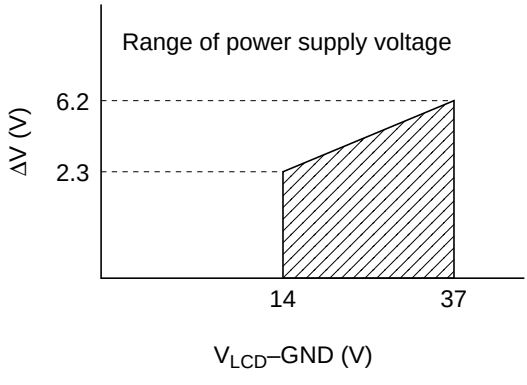


Figure 14 Power Supply Voltage V_{LCD}–GND and ΔV

AC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 to 37 V, Ta = –20 to 75°C)

Column Driving

Item	Symbol	Pin Name	Min	Max	Unit	Note
Clock cycle time	t_{cyc}	CL2	125	—	ns	
Clock high-level width (1)	t_{CWH1}	CL2	30	—	ns	
Clock high-level width (2)	t_{CWH2}	CL1	60	—	ns	
Clock low-level width	t_{CWL}	CL2	30	—	ns	
Clock setup time	t_{SCL}	CL2	200	—	ns	
Clock hold time	t_{HCL}	CL2	200	—	ns	
Clock rising/falling time	t_{Ct}	CL1, CL2	—	30	ns	
Data setup time	t_{DSU}	D_0–D_7	30	—	ns	
Data hold time	t_{DH}	D_0–D_7	30	—	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	25	—	ns	
Output delay time (1)	t_{DCAR1}	$\overline{CAR}$	—	70	ns	1
Output delay time (2)	t_{DCAR2}	$\overline{CAR}$	—	200	ns	1
M phase difference	t_{CM}	M, CL1	—	300	ns	

Note: 1. Specified when connecting the load circuit shown in figure 15.

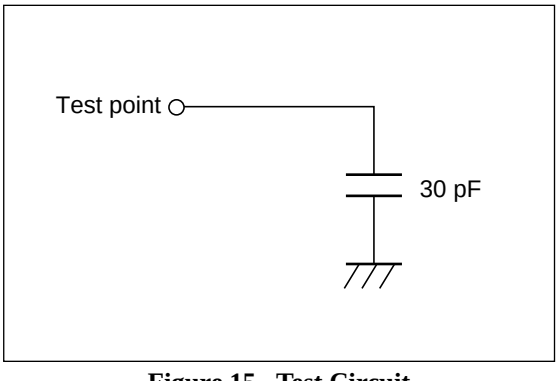


Figure 15 Test Circuit

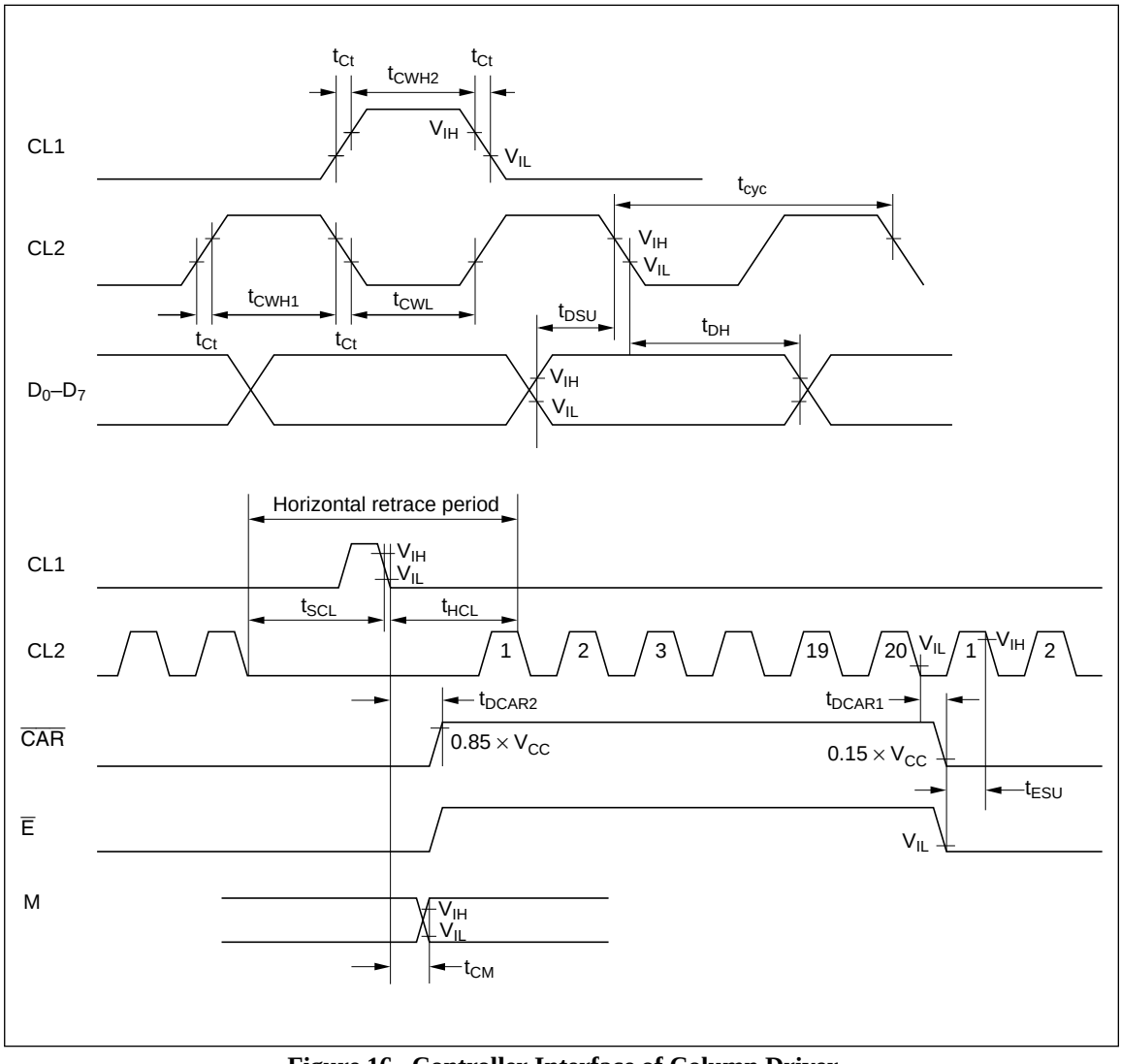


Figure 16 Controller Interface of Column Driver

Row Driving

Item	Symbol	Pin Name	Min	Max	Unit	Note
Clock low-level width	t_{WL1}	CL2	5	—	µs	
Clock high-level width	t_{WH1}	CL2	60	—	ns	
Data setup time	t_{DS2}	$\overline{E}$	100	—	ns	
Data hold time	t_{DH2}	$\overline{E}$	30	—	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	—	3	µs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	—	ns	1
Clock rising/falling time	t_{Ct}	CL2	—	30	ns	

Note: 1. Specified when connecting the load circuit shown in figure 15.

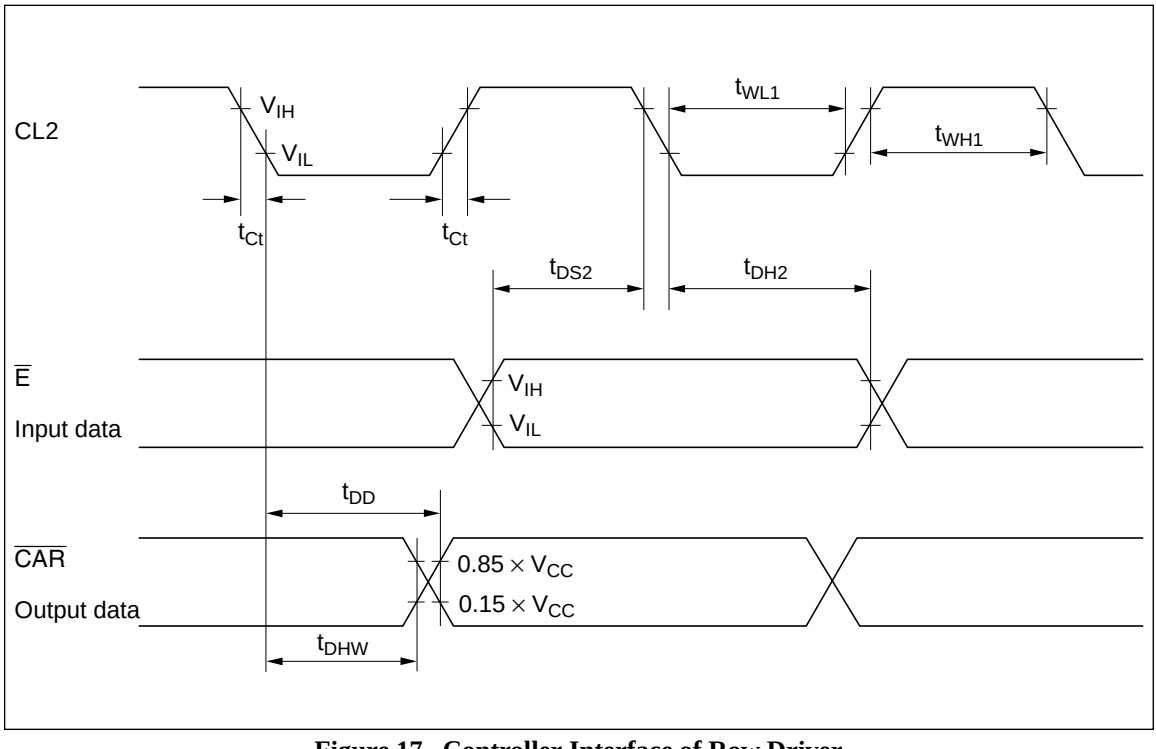


Figure 17 Controller Interface of Row Driver

HD66110ST

(Column Driver)

HITACHI

Description

The HD66110ST, the column driver for a large liquid crystal display (LCD) panel, features as many as 160 LCD outputs powered by 160 internal LCD drive circuits, and a high duty cycle. This device can interface to various LCD controllers by using an internal automatic chip enable signal generator. Its strip shape enables a slim tape carrier package (TCP).

Features

- 191-pin TCP
- CMOS fabrication process
- High voltage
  - LCD drive: 14 to 40 V
- High speed
  - Maximum clock speed:
    12 MHz (V_{CC} = 4.5 to 5.5 V)
    10 MHz (V_{CC} = 2.7 to 5.5 V)
- 4- and 8-bit data bus interface
- Display off function
- Standby function
- Various LCD controller interfaces
  - LCTC series: HD63645, HD64645, HD64646
  - LVIC series: HD66840, HD66841
  - CLINE: HD66850

Ordering Information

Type No.	Outer lead pitch (µm)
HD66110STB0	92
HD66110STB2	92

Note: The details of TCP pattern are shown in “The Information of TCP.”

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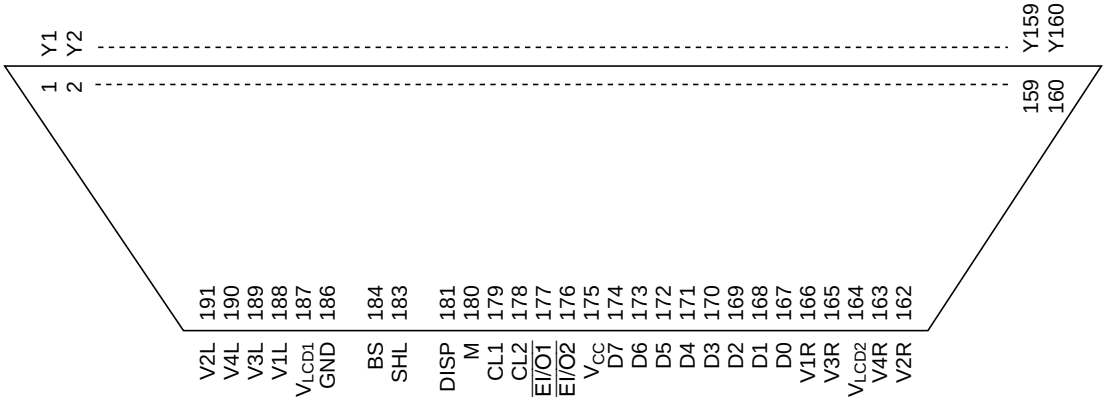
Pin Arrangement



Note: This is just an example of TCP; other TCP shapes are also possible.

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	175	V_{CC}	—	Power supply
GND	186	GND	—	Power supply
V_{LCD1}	187	V_{LCD1}	—	Power supply
V_{LCD2}	164	V_{LCD2}	—	Power supply
V1R	166	V1R	Input	Power supply
V2R	162	V2R	Input	Power supply
V3R	165	V3R	Input	Power supply
V4R	163	V4R	Input	Power supply
V1L	188	V1L	Input	Power supply
V2L	191	V2L	Input	Power supply
V3L	189	V3L	Input	Power supply
V4L	190	V4L	Input	Power supply
CL1	179	Clock 1	Input	Control signal
CL2	178	Clock 2	Input	Control signal
M	180	M	Input	Control signal
D_0–D_7	167–174	Data 0–data 7	Input	Control signal
SHL	183	Shift left	Input	Control signal
$\overline{EI/O1}$, $\overline{EI/O2}$	177, 176	Enable IO1, enable IO2	Input/output	Control signal
$\overline{DISP}$	181	Display off	Input	Control signal
BS	184	Bus select	Input	Control signal
Y_1–Y_{160}	1–160	Y_1–Y_{160}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{LCD1}, V_{LCD2}, GND: V_{CC} – GND supplies power to the internal logic circuits. V_{LCD} – GND supplies power to the LCD drive circuits. See figure 1.

V1R, V1L, V2R, V2L, V3R, V3L, V4R, V4L: Supply different levels of power to drive the LCD. V1 and V2 are selected levels, and V3 and V4 are non-selected levels.

Control Signals

CL1: Inputs display data latch pulses for latch circuit 2. Latch circuit 2 latches display data input from latch circuit 1, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for latch circuit 1. Latch circuit 1 latches display data input via D_0–D_7 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_7: Input display data. High-voltage level (V_{CC} level) of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level (GND level) data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output, and determines which chip enable pin ($\overline{EI/O1}$ or $\overline{EI/O2}$) is an input and which is an output. See figure 2.

$\overline{EI/O1}$, $\overline{EI/O2}$: If SHL is GND level, $\overline{EI/O1}$ inputs the chip enable signal, and $\overline{EI/O2}$ outputs the signal. If SHL is Vcc level, $\overline{EI/O1}$ outputs the chip enable signal, and $\overline{EI/O2}$ inputs the signal. The chip enable input pin of the first HD66110RT must be grounded, and those of the other HD6611STs must be connected to the chip enable output pin of the previous HD66110RT. The chip enable output pin of the last HD66110RT must be open.

$\overline{DISP}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{160} to V2 level.

BS: Selects either the 4-bit or 8-bit display data bus interface. If BS is V_{CC} level, the 8-bit bus is selected, and if BS is GND level, the 4-bit bus is selected. In 4-bit bus mode, data is latched via D_0–D_3; D_4–D_7 must be grounded.

LCD Drive Output

Y_1–Y_{160}: Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on a combination of the M signal and display data levels. See figure 3.

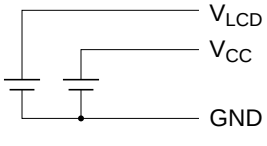


Figure 1 Power Supply for Logic and LCD Drive Circuits

SHL = GND, BS = GND

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8		Y153	Y154	Y155	Y156	Y157	Y158	Y159	Y160
D3	D2	D1	D0	D3	D2	D1	D0	----------	D3	D2	D1	D0	D3	D2	D1	D0

1st data — Last data

$\overline{EI/O1}$: chip enable input
$\overline{EI/O2}$: chip enable output

SHL = V_{CC}, BS = GND

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8		Y153	Y154	Y155	Y156	Y157	Y158	Y159	Y160
D0	D1	D2	D3	D0	D1	D2	D3	----------	D0	D1	D2	D3	D0	D1	D2	D3

Last data — 1st data

$\overline{EI/O1}$: chip enable output
$\overline{EI/O2}$: chip enable input

SHL = GND, BS = V_{CC}

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8		Y153	Y154	Y155	Y156	Y157	Y158	Y159	Y160
D7	D6	D5	D4	D3	D2	D1	D0	----------	D7	D6	D5	D4	D3	D2	D1	D0

1st data — Last data

$\overline{EI/O1}$: chip enable input
$\overline{EI/O2}$: chip enable output

SHL = V_{CC}, BS = V_{CC}

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8		Y153	Y154	Y155	Y156	Y157	Y158	Y159	Y160
D0	D1	D2	D3	D4	D5	D6	D7	----------	D0	D1	D2	D3	D4	D5	D6	D7

Last data — 1st data

$\overline{EI/O1}$: chip enable output
$\overline{EI/O2}$: chip enable input

Figure 2 Selection of Destinations of Display Data Output

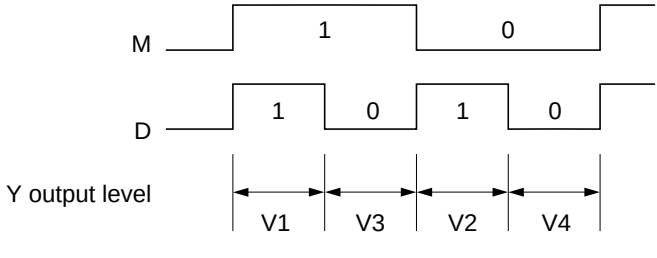


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

The 160-bit LCD drive circuit generates four voltage levels V1, V2, V3, and V4, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the latch circuit 2.

Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Latch Circuit 2

160-bit latch circuit 2 latches data input from latch circuit 1, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit 1

160-bit latch circuit 1 latches 4-bit or 8-bit parallel data input via the D_0 to D_7 pins at the timing generated by the shift register.

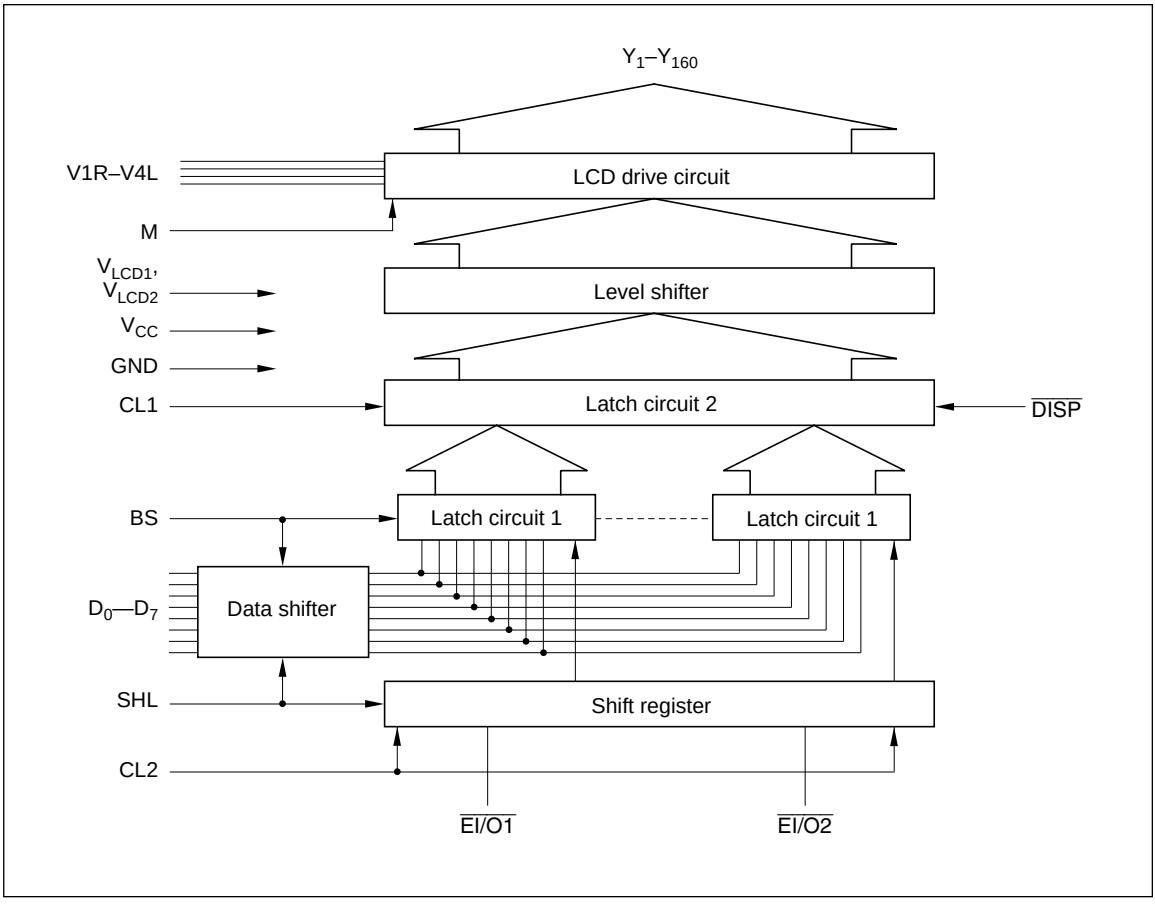
Shift Register

The 40-bit shift register generates and outputs data latch signals for latch circuit 1 at the falling edge of each clock 2 (CL2) pulse.

Data Shifter

The data shifter shifts the destination of display data output, when necessary.

Block Diagram



Comparison of HD66110RT with the HD66110ST

Item		HD66110RT	HD66110ST
LCD drive voltage range		28 to 40 V	14 to 40 V
Speed	V_{CC} = 4.5 to 5.5 V	12 MHz	12 MHz
	V_{CC} = 2.7 to 4.5 V	—	10 MHz
Number of pins (power supply)		26 (7)	31 (12)
Voltage supply pin format		Single side	Dual side

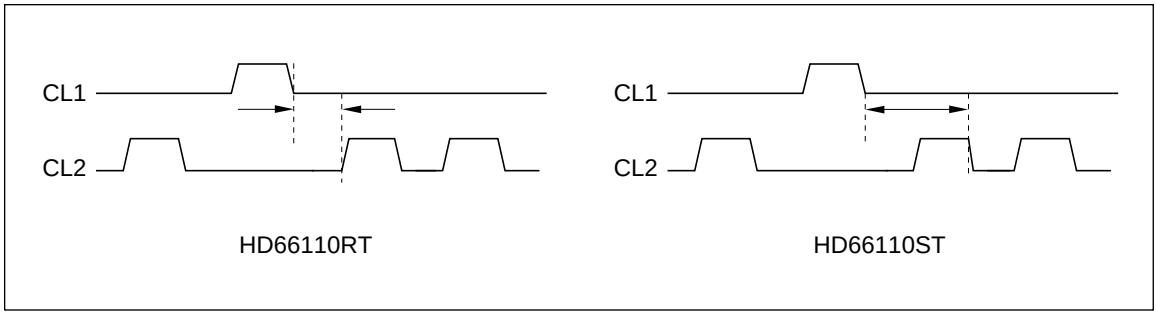


Figure 4 t_{HCL} Definitions of the HD66110RT and HD66110ST

Operation Timing

4-Bit Bus Mode (BS = GND)

Figure 5 shows 4-bit data latch timing when SHL = GND, that is, the $\overline{EI/O1}$ pin is a chip enable input and $\overline{EI/O2}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{EI/O1}$ pin is a chip enable output and $\overline{EI/O2}$ pin is a chip enable input.

When a low chip enable signal is input via the $\overline{EI/O1}$ pin, the HD66110RT is first released from data standby state, and, at the falling edge of the following CL2 pulse, it is released entirely from standby state and starts latching data.

It simultaneously latches 4 bits of data at the falling edge of each CL2 pulse. When it has latched 156 bits of data, it sets the $\overline{EI/O2}$ signal low. When it has latched 160 bits of data, it automatically stops and enters standby state, initiating the next HD66110RT, as long as its $\overline{EI/O2}$ pin is connected to the $\overline{EI/O1}$ pin of the next HD66110RT.

The HD66110RTs output one line of data from the Y_1–Y_{160} pins at the falling edge of each CL1 pulse. Data d_1 is output from Y_1, and d_{160} from Y_{160} when SHL = GND, and d_1 is output from Y_{160}, and d_{160} from Y_1 when SHL = V_{CC}.

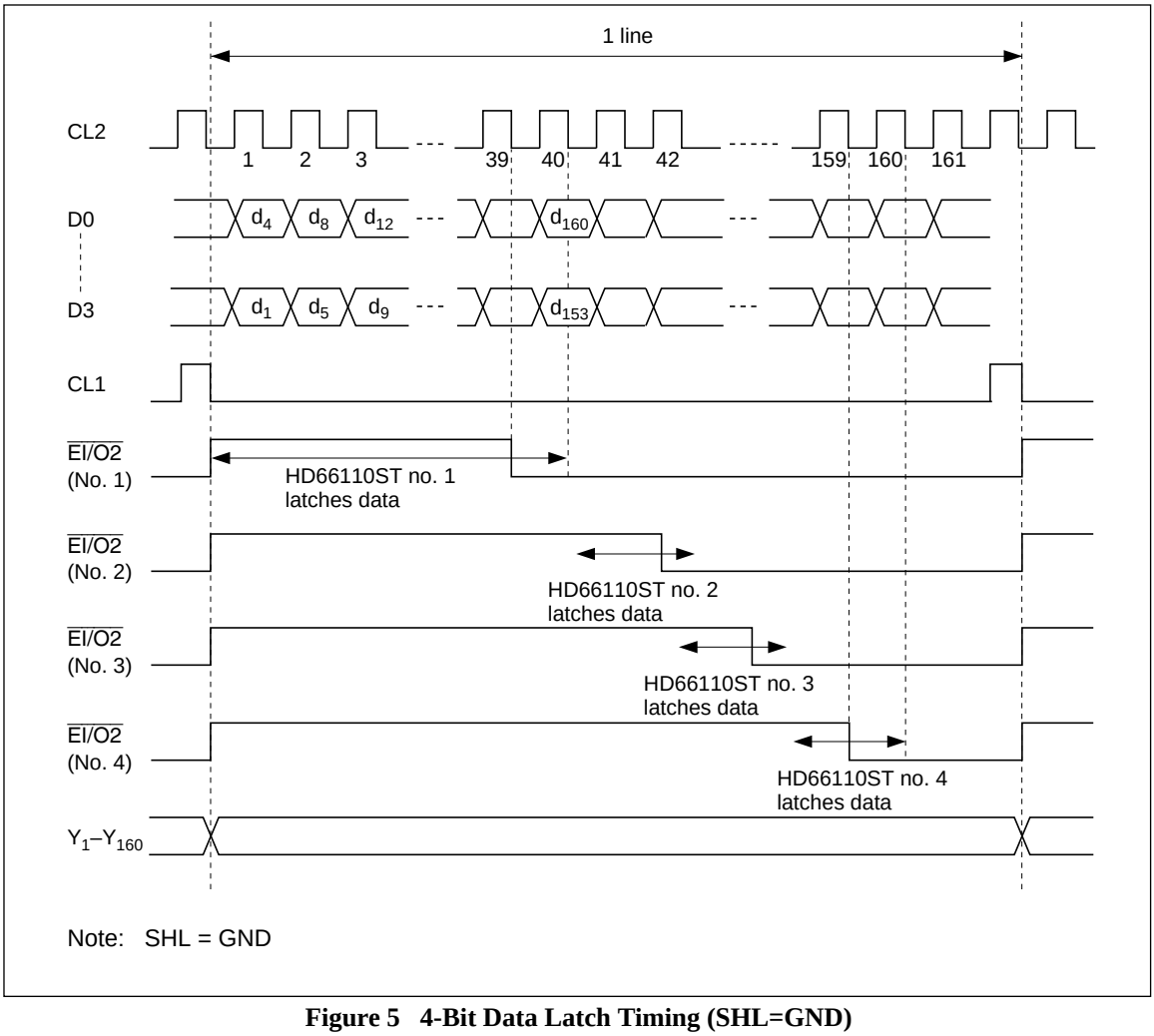


Figure 5 4-Bit Data Latch Timing (SHL=GND)

8-Bit Bus Mode (BS = V_{CC})

Figure 6 shows 8-bit data latch timing when SHL = GND, that is, the $\overline{EI/O1}$ pin is a chip enable input and $\overline{EI/O2}$ pin is a chip enable output.

When SHL = V_{CC}, the $\overline{EI/O1}$ pin is a chip enable output and $\overline{EI/O2}$ pin is a chip enable input.

The operation is the same as that in 4-bit bus mode except that 8 bits of data are latched simultaneously.

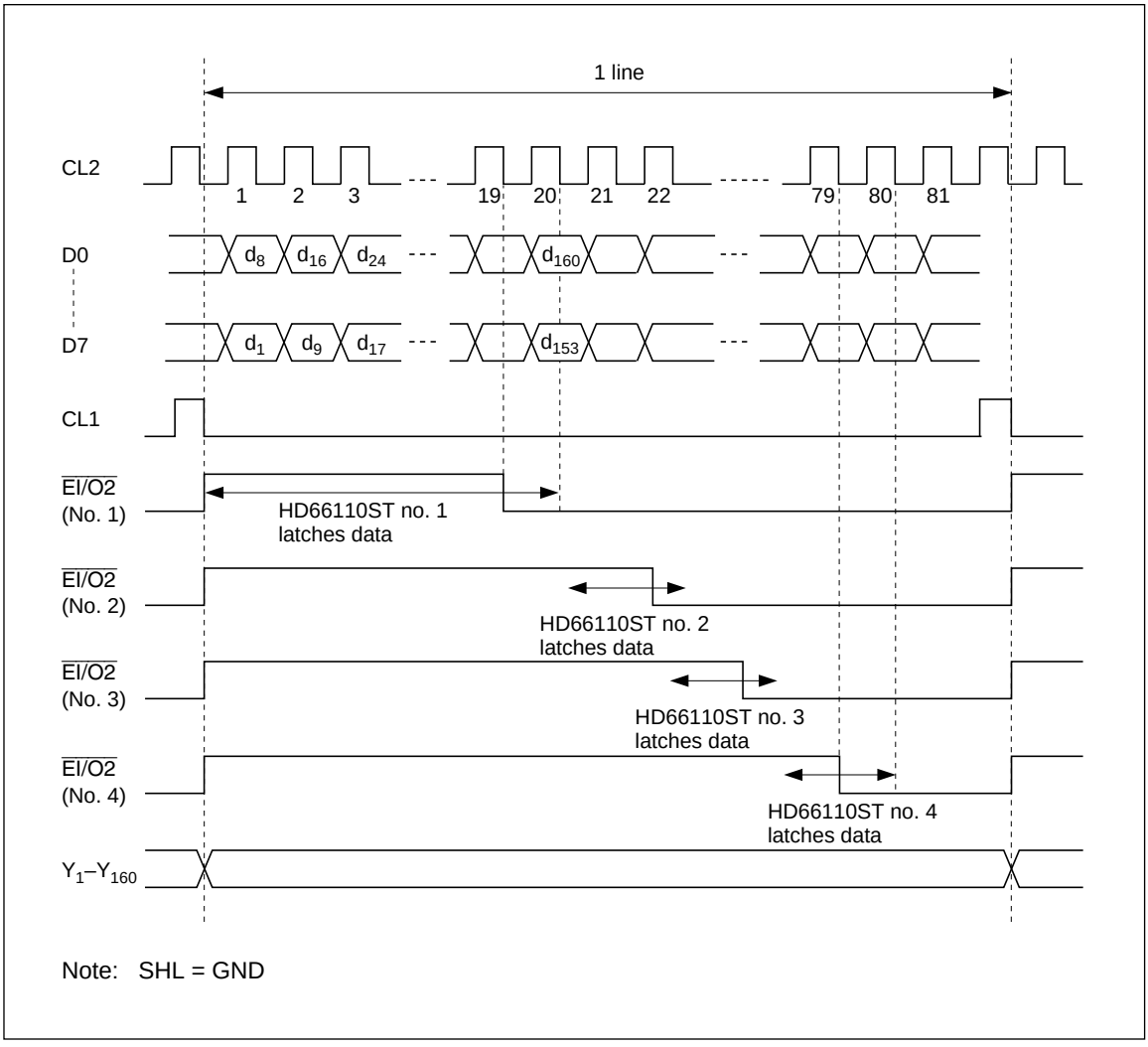
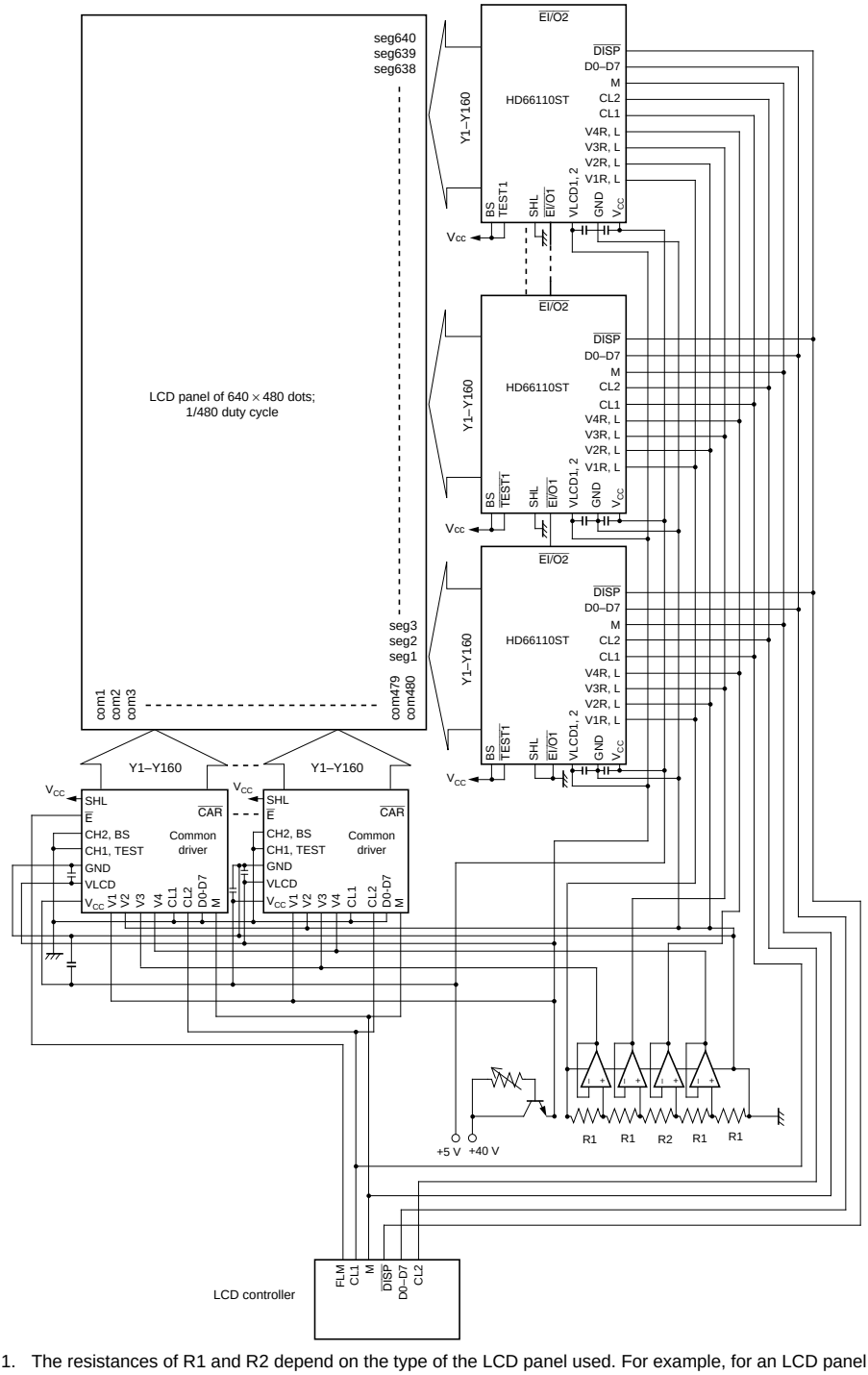


Figure 6 8-Bit Data Latch Timing (SHL=GND)

Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/20 bias, R1 and R2 must be 3 kΩ and 48 kΩ, respectively. That is, R1/(4•R1+R2) should be 1/20.

2. To stabilize the power supply, place two 0.1-µF capacitors near each LCD driver: one between the Vcc and GND pins, and the other between the V_{LCD} and GND pins.

3. The load must be less than 30 pF between the $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110STs.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 2, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 3
Input voltage 2	V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Indicates the voltage between GND and V_{LCD}.
3. Applies to input pins for logic circuits, that is, control signal pins.
4. Applies to input pins for LCD drive level voltages, that is, V1–V4 pins.
5. Power should be applied to V_{CC}-GND first, and then V_{LCD}-GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond the absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.7 to 4.5 V, V_{LCD} – GND = 14 to 40 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH}=–0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL}=0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON}=150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	V_{IN}=V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	V_{IN}=V_{LCD} to GND	
Current consumption 1	I_{CC}	—	—	2.2	mA	f_{CL2} = 10 MHz f_{CL1} = 28 kHz V_{CC} = 3.0 V	2
Current consumption 2	I_{LCD}	—	—	3.0	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.3	mA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics 2 (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 14 to 40 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	V_{IN} = V_{LCD} to GND	
Current consumption 1	I_{CC}	—	—	5.0	mA	f_{CL2} = 12 MHz f_{CL1} = 28 kHz	2
Current consumption 2	I_{LCD}	—	—	3.0	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.7	mA	Same as above	2, 3

Pins: 1. CL1, CL2, M, SHL, BS, $\overline{EI/O1}$, $\overline{EI/O2}$, $\overline{DISP}$, D_0 – D_7
2. $\overline{EI/O1}$, $\overline{EI/O2}$
3. Y_1 – Y_{160}, V1 –V4
4. V1 – V4

Notes: 1. Indicates the resistance between one pin from Y_1 – Y_{160} and another pin from V1 – V4 when load current is applied to the Y pin; defined under the following conditions.

V_{LCD} – GND = 40 V
V1, V3 = V_{LCD} – {1/20 (V_{LCD} – GND)}
V2, V4 = V_{LCD} + {1/20 (V_{LCD} – GND)}

V1 and V3 should be near V_{LCD} level, and V2 and V4 should be near GND level (figure 7). All voltage must be within ΔV. ΔV is the range within which RON, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{LCD} – GND (figure 8).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

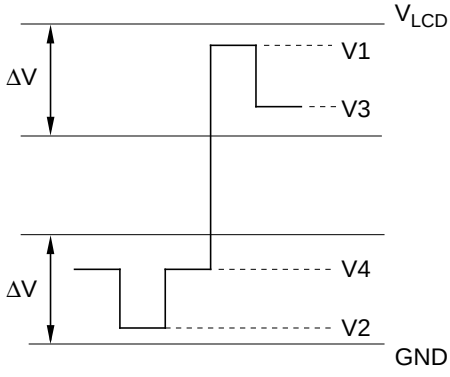


Figure 7 Relation between Driver Output Waveform and Level Voltages

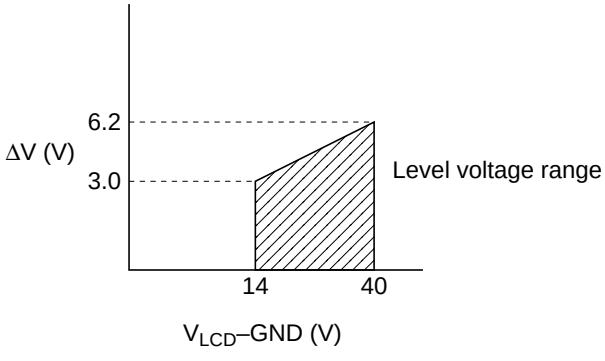


Figure 8 Relation between V_{LCD} – GND and ΔV

AC Characteristics 1 (V_{CC} = 2.7 to 4.5 V, V_{CD} – GND = 14 to 40 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL2	100	—	ns	
Clock high-level width 1	t_{CWH2}	CL2	37	—	ns	
Clock low-level width	t_{CWL2}	CL2	37	—	ns	
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	100	—	ns	
Clock rise time	t_r	CL1, CL2	—	50	ns	2
Clock fall time	t_f	CL1, CL2	—	50	ns	2
Data setup time	t_{DS}	D_0–D_7, CL2	35	—	ns	
Data hold time	t_{DH}	D_0–D_7, CL2	35	—	ns	
M phase difference time	t_{CM}	M, CL1	—	300	ns	

Notes: 1. The load must be less than 30 pF between $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110STs.
2. t_r, $t_f < (t_{cyc} - t_{CWH2} - t_{CWL2})/2$ and t_r, $t_f \leq 50$ ns

AC Characteristics 2 (V_{CC} = 5 ± 10%, V_{LCD} – GND = 14 to 40 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CVC}	CL2	83	—	ns	
Clock high-level width 1	t_{CWH2}	CL2	20	—	ns	
Clock low-level width	t_{CWL2}	CL2	20	—	ns	
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	100	—	ns	
Clock rise time	t_r	CL1, CL2	—	50	ns	2
Clock fall time	t_f	CL1, CL2	—	50	ns	2
Data setup time	t_{DS}	D_0–D_7, CL2	10	—	ns	
Data hold time	t_{DH}	D_0–D_7, CL2	10	—	ns	
M phase difference time	t_{CM}	M, CL1	—	300	ns	

Notes: 1. The load must be less than 30 pF between $\overline{EI/O2}$ and $\overline{EI/O1}$ connections of HD66110STs.
2. t_r, $t_f < (t_{cyc} - t_{CWH2} - t_{CWL2})/2$ and t_r, $t_f \leq 50$ ns

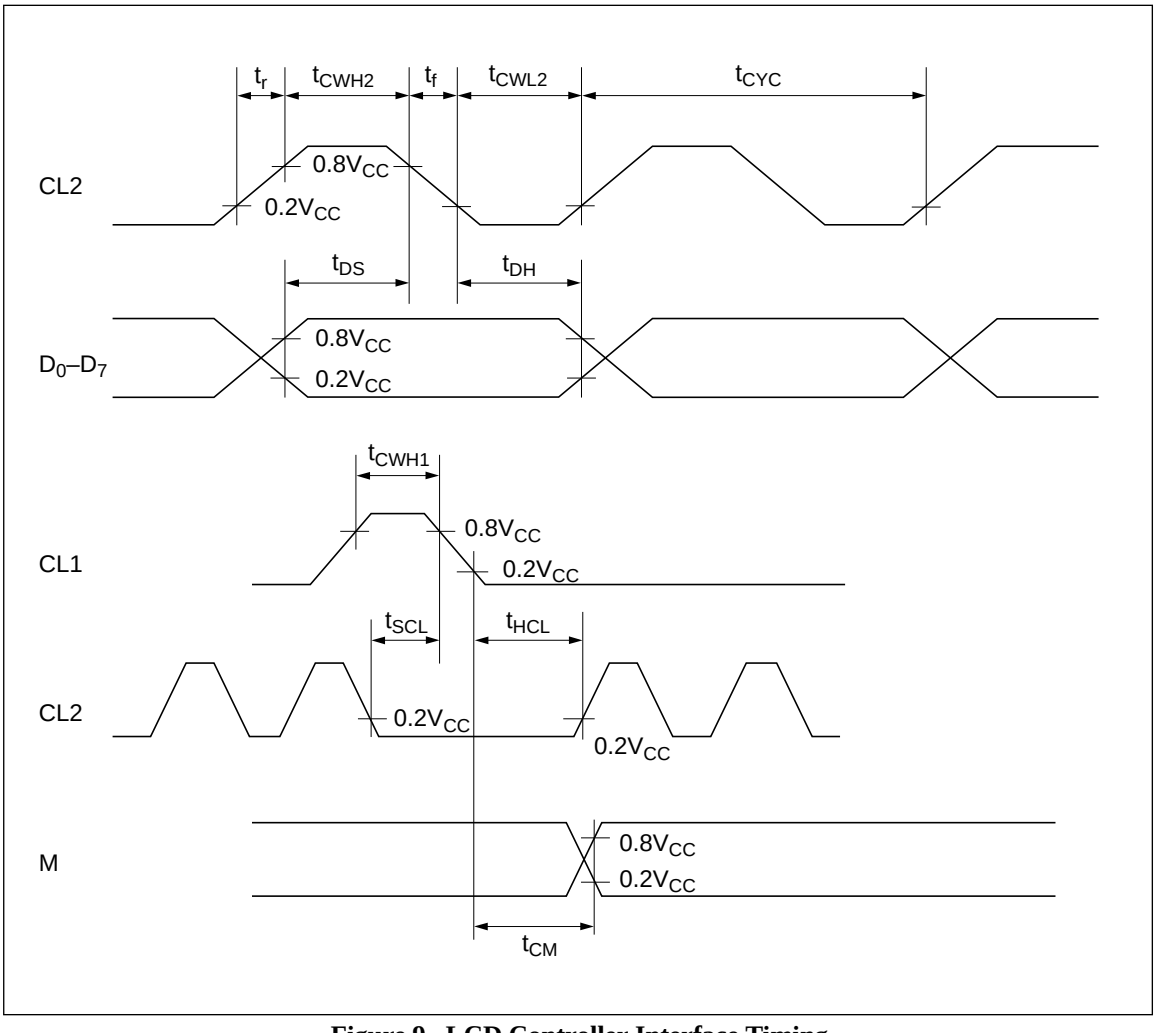


Figure 9 LCD Controller Interface Timing

HD66113T

(120-Channel Common Driver Packaged in a Slim Tape Carrier Package)

HITACHI

Description

The HD66113T is a common driver for large dot matrix liquid crystal graphics displays. It features 120 channels which can be divided into two groups of 60 channels by selecting data input/output pins. The driver is powered by about 3 V, making it suitable for the design of portable equipment which fully utilizes the low power dissipation of liquid crystal elements. The HD66113T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area (wiring area).

Features

- Duty cycle: About 1/100 to 1/480
- 120 LCD drive circuits
- High LCD driving voltage: 14 V to 40 V
- Output division function (2 × 60-channel outputs)
- Display off function
- Operating voltage: 2.5 V to 5.5 V
- Slim-TCP
- Low output impedance: 0.7 kΩ (typ)

Ordering Information

Type No.	Outer Lead Pitch (µm)
HD66113TA0	190

Note: The details of TCP pattern are shown in “The Information of TCP.”

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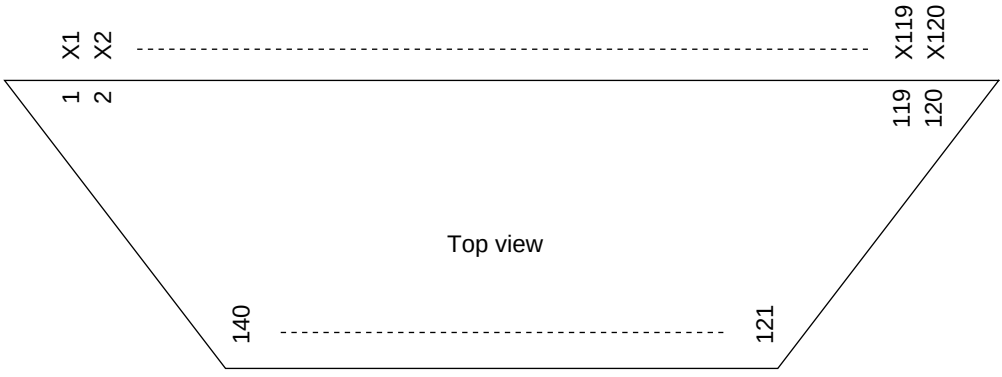
Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

Pin Assignments

V_{LCD1}	V_1L	V_6L	V_5L	V_2L	GND	DIO1	M	$\overline{DISPOFF}$	SHL	CH	DI	CL	DIO2	V_{CC}	V_2R	V_5R	V_6R	V_1R	V_{LCD2}
140	139	138	137	136	135	134	133	132	131	130	129	128	127	126	125	124	123	122	121

Pin Descriptions

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{LCD}1, 2	140, 121	V_{LCD}	—	Power supply
V_{CC}	126	V_{CC}	—	Power supply
GND	135	GND	—	Power supply
V_1L, V_1R	139, 122	V_1L, V_1R	Input	Power supply
V_2L, V_2R	136, 125	V_2L, V_2R	Input	Power supply
V_5L, V_5R	137, 124	V_5L, V_5R	Input	Power supply
V_6L, V_6R	138, 123	V_6L, V_6R	Input	Power supply
CL	128	Clock	Input	Control signal
M	133	M	Input	Control signal
CH	130	CH	Input	Control signal
SHL	131	Shift left	Input	Control signal
DIO1	134	Data	Input/output	Control signal
DIO2	127	Data	Input/output	Control signal
DI	129	Data	Input	Control signal
$\overline{\text{DISPOFF}}$	132	Display off	Input	Control signal
X1–X120	1–120	X1–X120	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_{LCD}, GND: Supply power to the LCD drive circuits (figure 1).

V_1L, V_1R, V_2L, V_2R, V_5L, V_5R, V_6L, V_6R: Supply different power levels to drive the LCD. V_1 and V_2 are selected levels, and V_5 and V_6 are non-selected levels.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes the LCD drive outputs to AC.

CH: Selects the data shift mode. (CH = high: 2 × 60-output mode, CH = low: 120-output mode)

SHL: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1, DIO2: Input or output data. DIO1 is input and DIO2 is output when SHL is high. DIO1 is output and DIO2 is input when SHL is low.

DI: Input data. DI is input to X61–X120 when CH and SHL are high, and to X60–X1 when SHL is low.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets the LCD drive outputs X1–X120 to the V_2 level. A high $\overline{\text{DISPOFF}}$ is normally used.

LCD Drive Outputs

X1–X120: Each X outputs one of four voltage levels V_1, V_2, V_5, or V_6, depending on the combination of the M signal and the data level (figure 3).

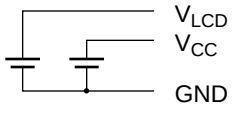


Figure 1 Power Supply for LCD Driver

SHL	Data shift direction
High	Shift to right DIO1 → SR1 → SR2 → SR3 • • • → SR120 → DIO2
Low	Shift to left DIO2 → SR120 → SR119 • • • → SR1 → DIO1

Note: SR1 to SR120 correspond to the outputs of X1 to X120, respectively.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL

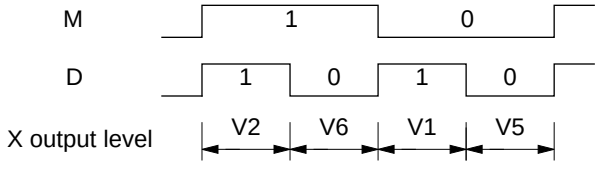
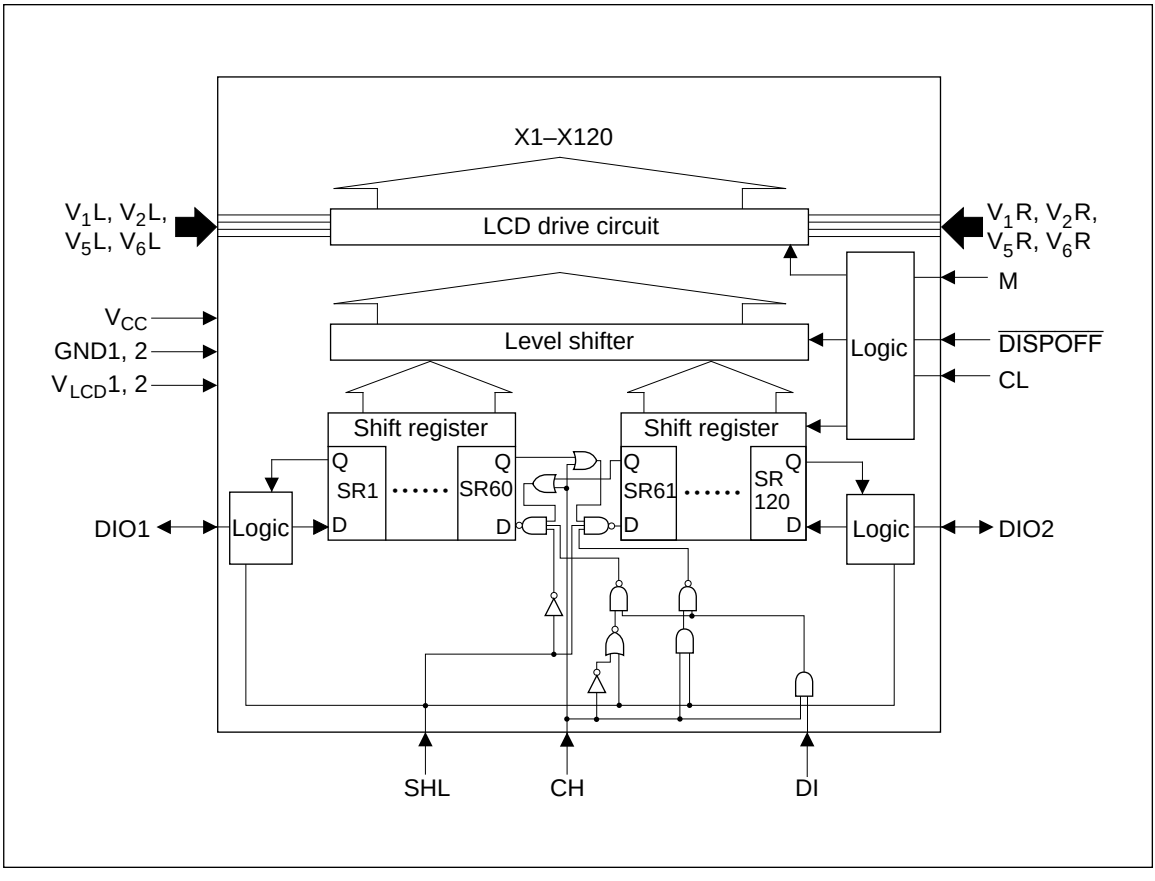


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuit

The 120-bit LCD drive circuit generates four voltage levels V_1, V_2, V_5, and V_6, which drive the LCD panel. One of these four levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signals (2.5 V–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 120-bit shift register shifts the data input via the DIO pin by one bit at a time. The one bit of shifted-out data is output from the DIO pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL pin selects the data shift direction.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Input voltage 3	V_{T3}	–0.3 to +7.0	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes:
1. The reference point is GND (0 V).
2. Applies to pins CL, M, SHL, DI, $\overline{\text{DISPOFF}}$, and CH.
3. Applies to pins V_1 and V_6.
4. Applies to pins V_2 and V_5.
5. Power should be applied to V_{CC}–GND first, and then V_{LCD}–GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its specified operating range in order to prevent malfunctions or loss of reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 V to 5.5 V, GND = 0 V, and T_a = –20°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Xj on resistance	R_{ON}	3	—	0.7	1.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5	—	5	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{LCD} to GND	
Current consumption 1	I_{GND}	—	—	—	0.5	mA	f_{CL} = 36 kHz f_M = 75 kHz	2
Current consumption 2	I_{LCD}	—	—	—	1.0	mA		

Note: Pins: 1. CL, M, SHL, CH, DI, DIO1, DIO2, $\overline{\text{DISPOFF}}$
2. DIO1, DIO2
3. X1–X120, V
4. V_1, V_2, V_5, V_6

Notes: 1. Indicates the resistance between one of the pins X1–X120 and one of the voltage supply pins V_1, V_2, V_5, or V_6, when load current is applied to the X pin; defined under the following conditions:

V_{LCD}–GND = 40 V
V_1, V_6 = V_{CC} – {1/20 (V_{LCD}–GND)}
V_5, V_2 = GND + {1/20 (V_{LCD}–GND)}

All voltages must be within ΔV, $V_{LCD} \geq V_1 \geq V_6 \geq V_{LCD} - 7.0$ V, and 7.0 V ≥ $V_5 \geq V_2 \geq$ GND. Note that ΔV depends on the power supply voltage V_{LCD}–GND (figure 5).

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held at V_{CC} and GND, respectively.

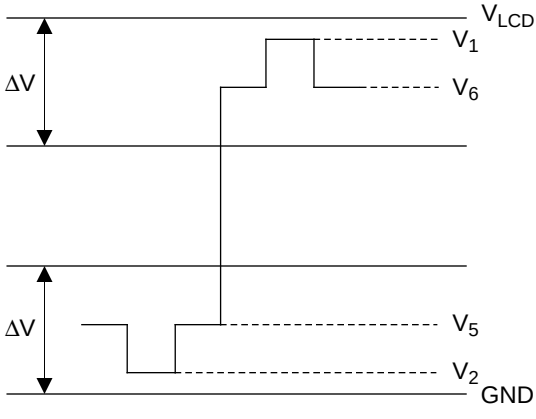


Figure 4 Relation between Driver Output Waveform and Voltage Levels

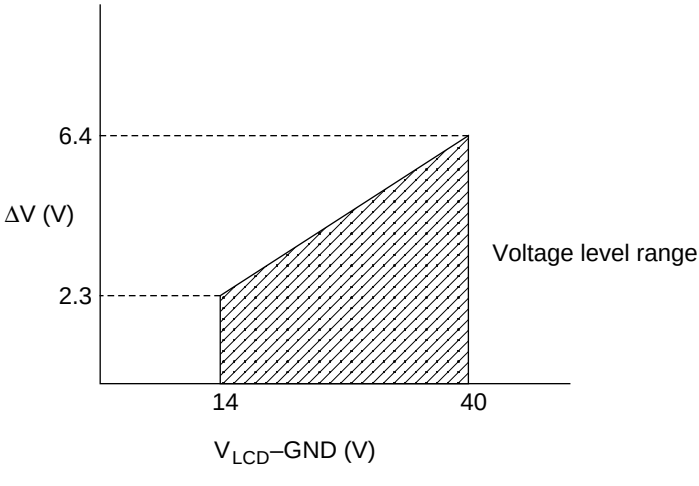


Figure 5 Relation between V_{LCD}–GND and ΔV

AC Characteristics (V_{CC} = 2.5 V to 5.5 V, GND = 0 V, and T_a = –20°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	1
Clock fall time	t_f	CL	—	30	ns	1
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	350	ns	2
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	1.2	µs	3
Output delay time 2	t_{pd2}	X (n), M	—	1.2	µs	3

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, and T_a = –20°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	1
Clock fall time	t_f	CL	—	30	ns	1
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	150	ns	2
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	0.7	µs	3
Output delay time 2	t_{pd2}	X (n), M	—	0.7	µs	3

Notes: 1. t_r, t_f < ($t_{cyc} = t_{CWH} – t_{CWL}$)/2 and t_r, $t_f \leq 30$ ns

2, 3 The load circuit shown in figure 6 is connected.

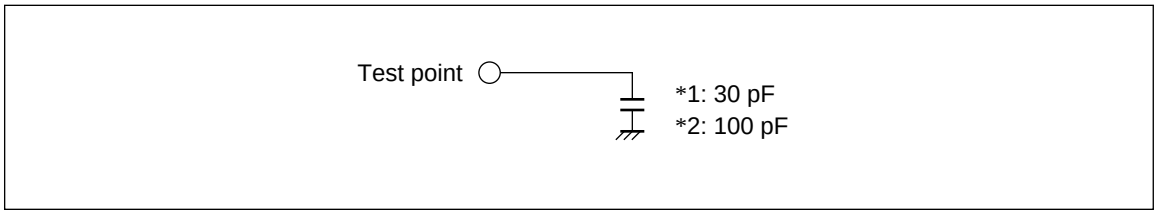


Figure 6 Load Circuit

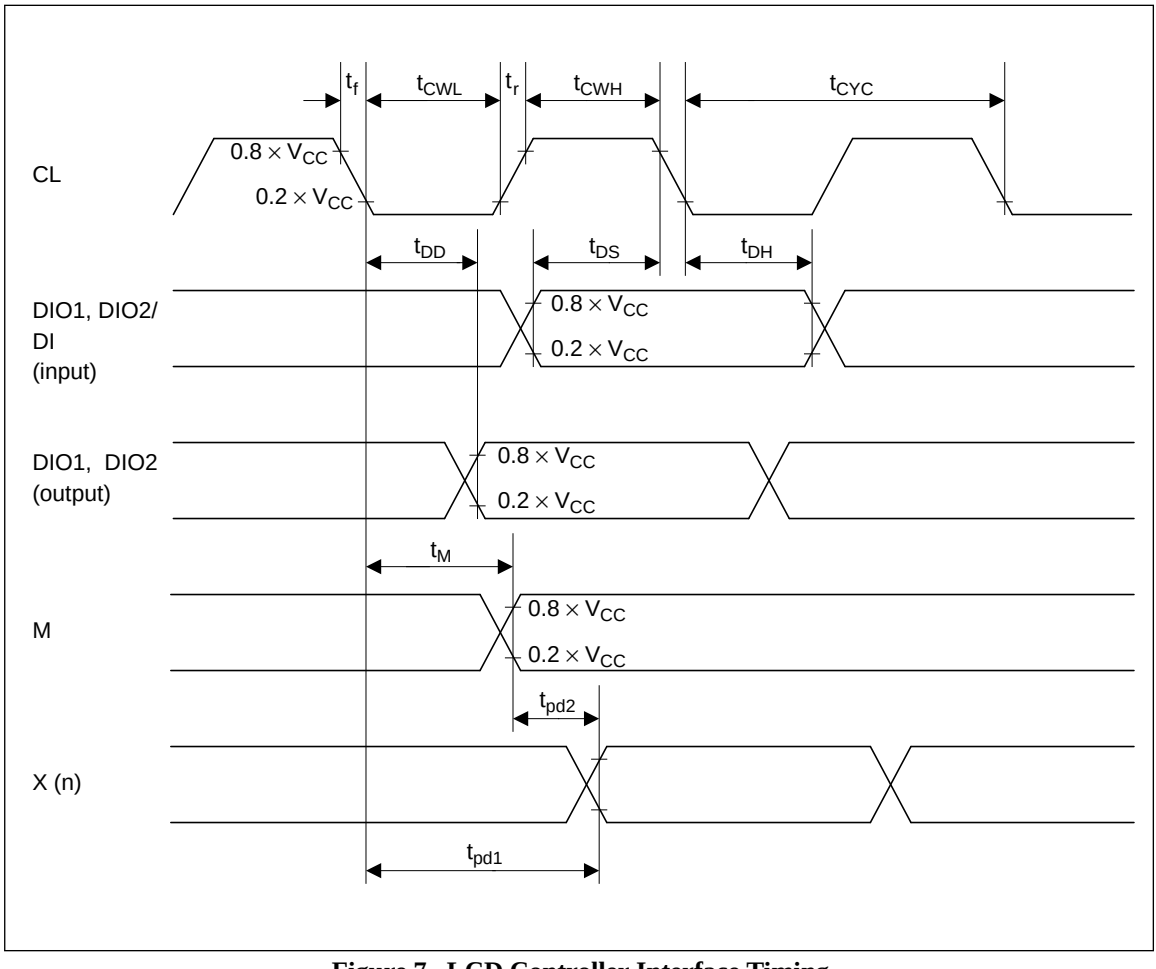
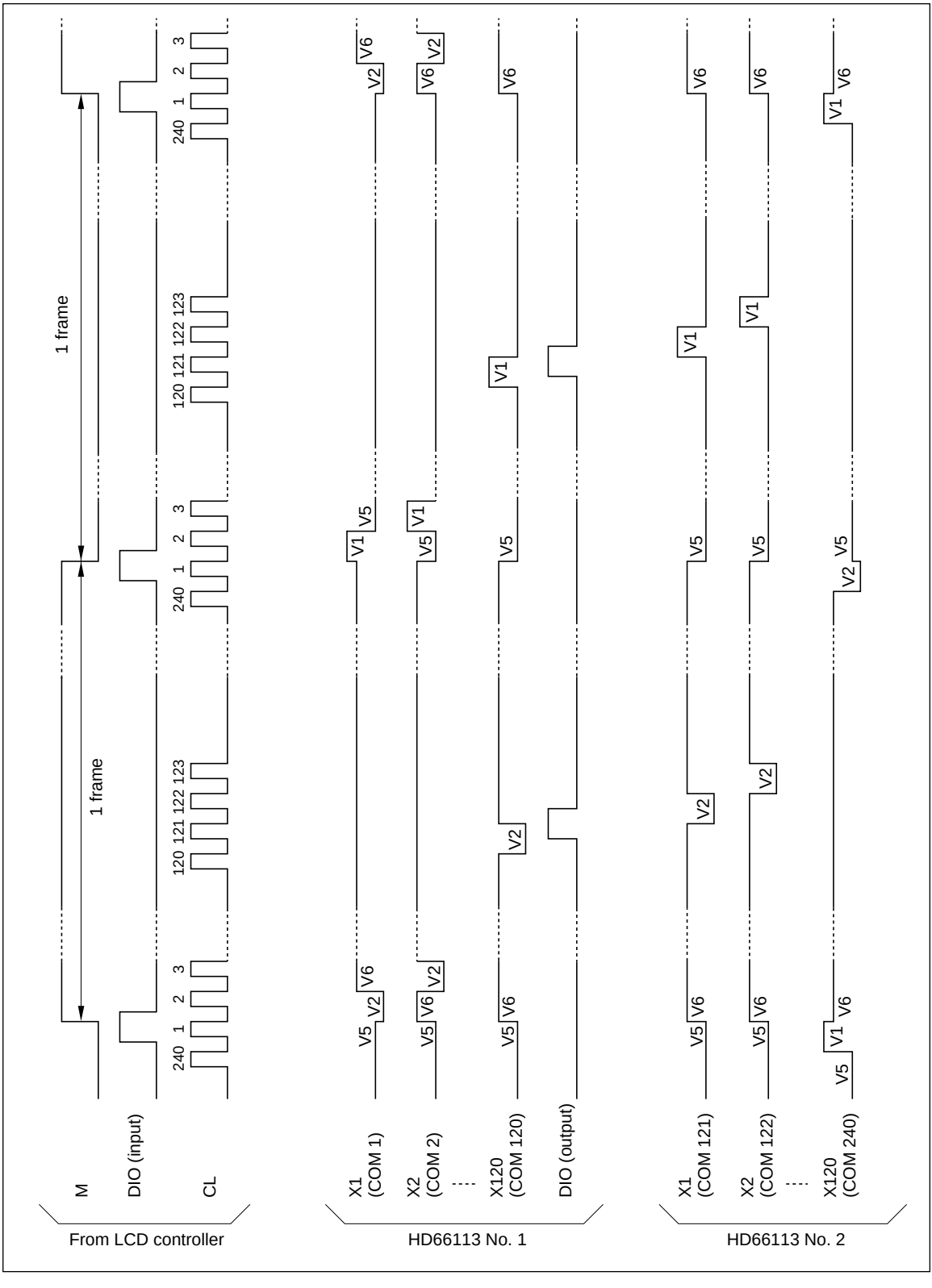


Figure 7 LCD Controller Interface Timing

Operation Timing (1/480 Duty Cycle)



Connection Examples

Figures 8 and 9 show examples of how HD66113Ts can be configured to drive a 600-line LCD panel with a 1/300 duty cycle. Figures 10 and 11 show examples of how HD66113Ts can be configured to drive a 240-line LCD panel with a 1/240 duty cycle. The HD66113T's 120 channels can be divided into two groups of 60 channels, and its data shift direction can be changed by selecting the data output mode pin (CH) and data shift pin (SHL), respectively.

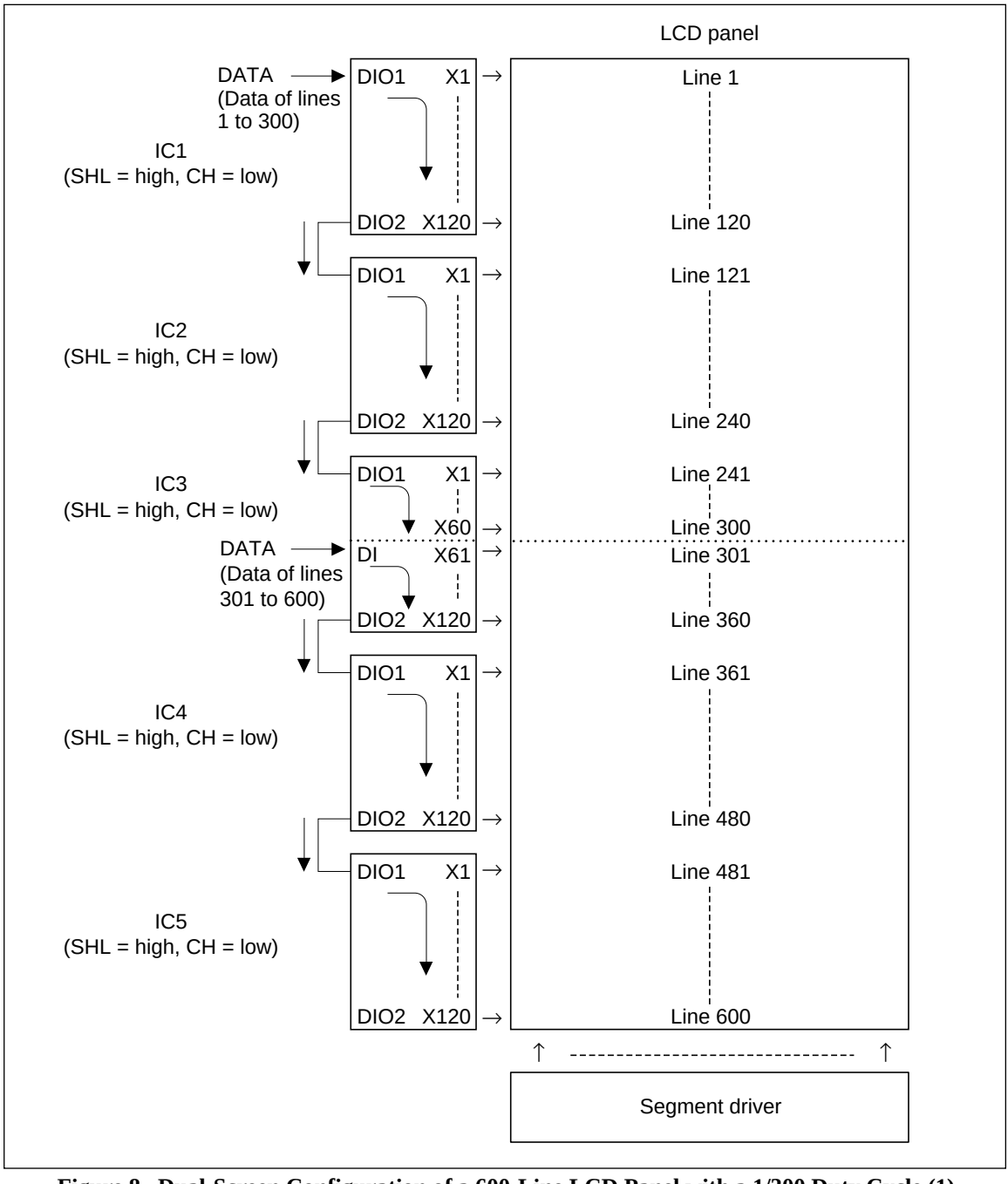


Figure 8 Dual-Screen Configuration of a 600-Line LCD Panel with a 1/300 Duty Cycle (1)

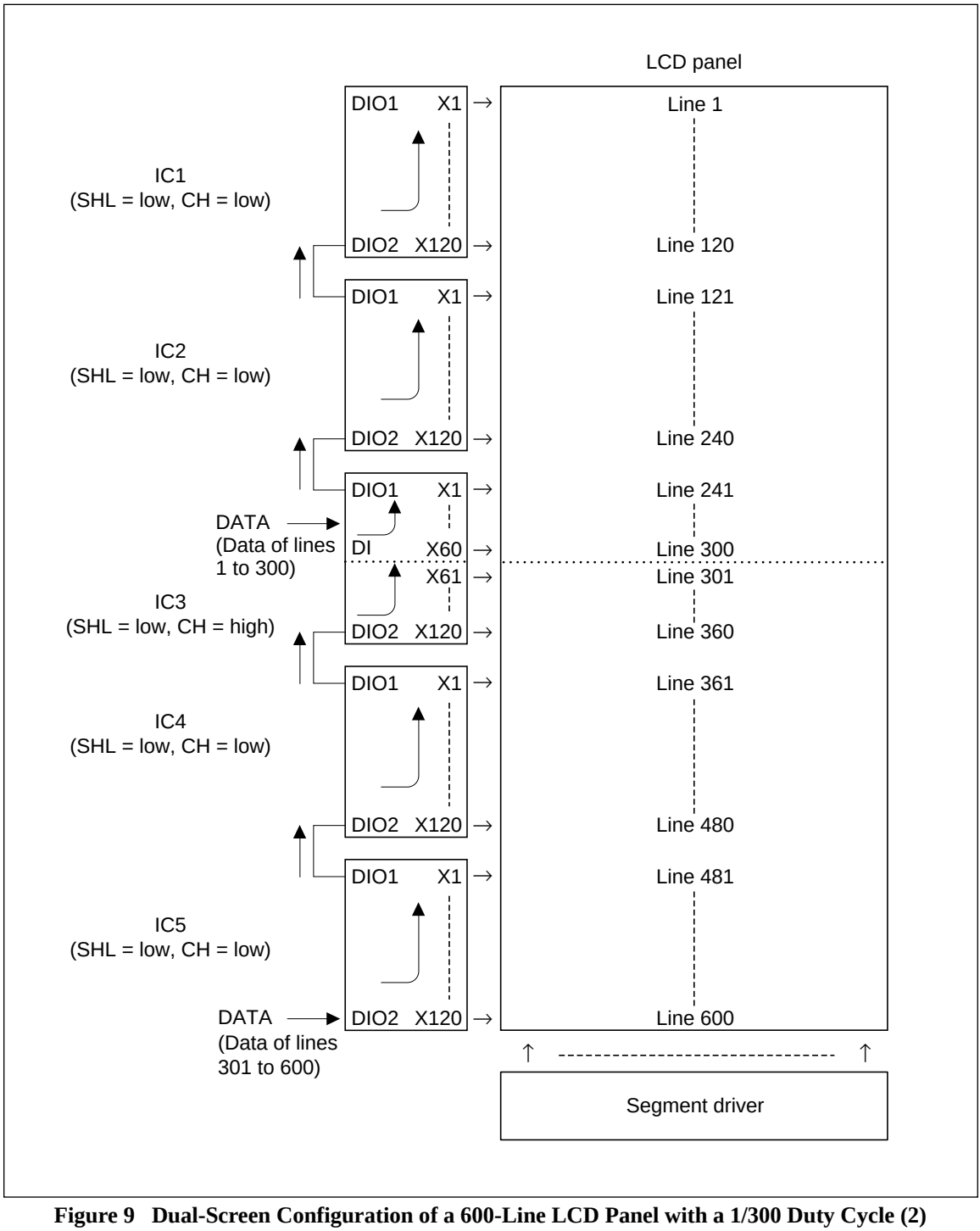


Figure 9 Dual-Screen Configuration of a 600-Line LCD Panel with a 1/300 Duty Cycle (2)

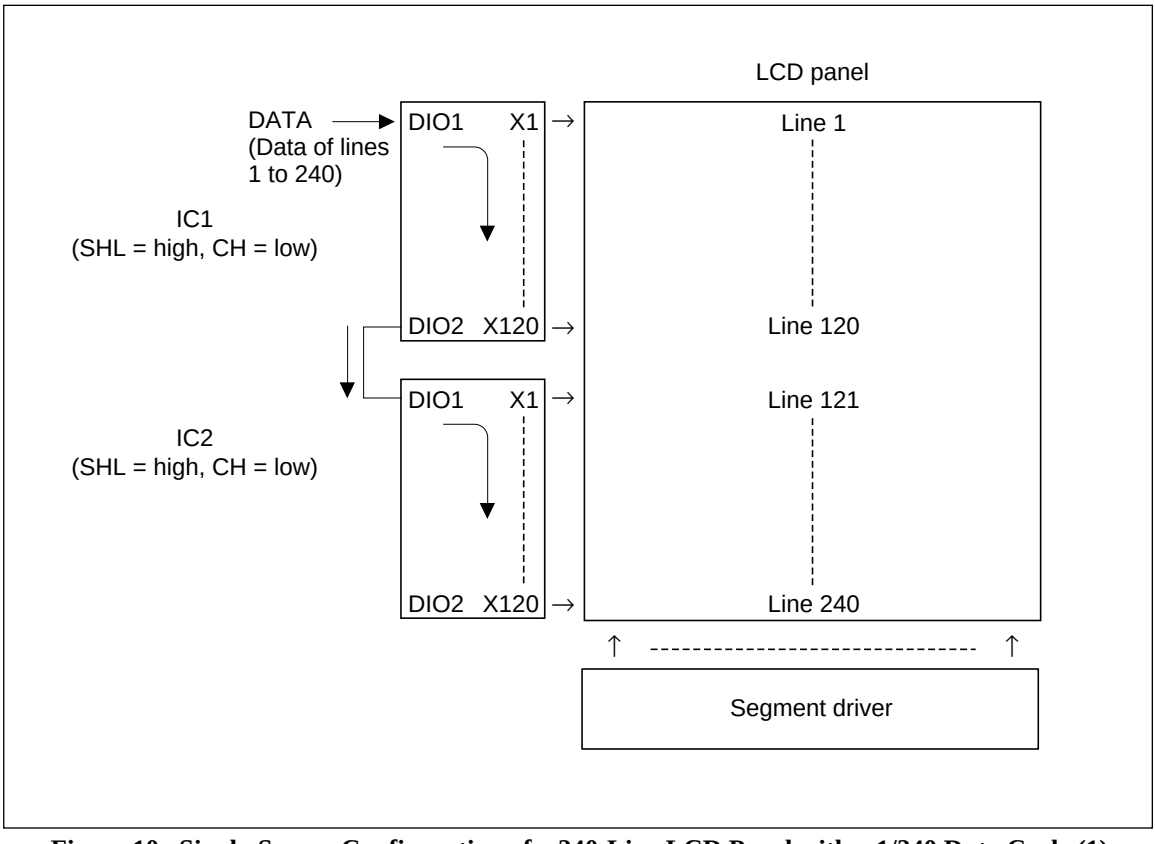


Figure 10 Single-Screen Configuration of a 240-Line LCD Panel with a 1/240 Duty Cycle (1)

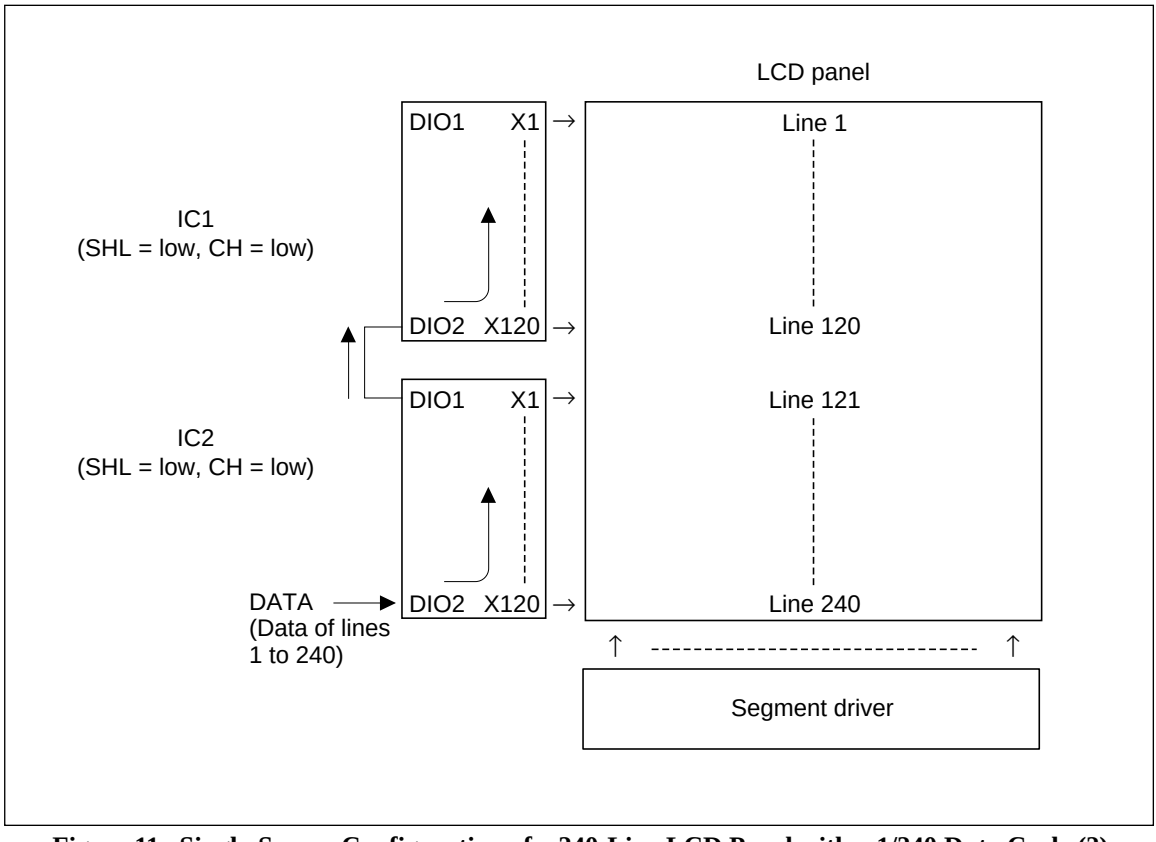


Figure 11 Single-Screen Configuration of a 240-Line LCD Panel with a 1/240 Duty Cycle (2)

HD66115T

160-Channel Common Driver Packaged in a Slim Tape Carrier Package

HITACHI

Description

The HD66115T is a common driver for large dot matrix liquid crystal graphics displays. It features 160 channels which can be divided into two groups of 80 channels by selecting data input/output pins. The driver is powered by about 3 V, making it suitable for the design of portable equipment which fully utilizes the low power dissipation of liquid crystal elements. The HD66115T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area (wiring area).

Features

- Duty cycle: About 1/100 to 1/480
- 160 LCD drive circuits
- High LCD driving voltage: 14 V to 40 V
- Output division function (2 × 80-channel outputs)
- Display off function
- Operating voltage: 2.5 V to 5.5 V
- Slim-TCP
- Low output impedance: 0.7 kΩ (typ)

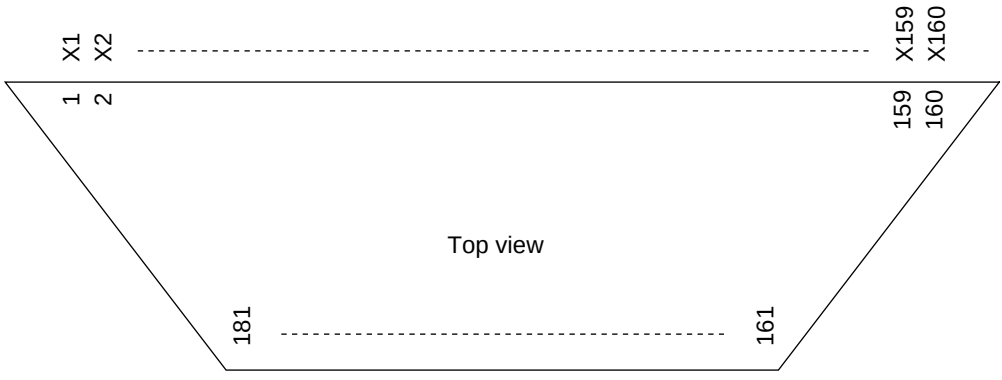
Ordering Information

Type No.	Outer Lead Pitch (µm)
HD66115TA0	180
HD66115TA1	250

Note: The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

Pin Assignments

V2L	V5L	V6L	V1L	$V_{LCD}1$	GND1	CH	SHL	$\overline{DISPOFF}$	M	CL	GND2	DIO1	DI	DIO2	V_{CC}	V1R	V6R	$V_{LCD}2$	V5R	V2R
181	180	179	178	177	176	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161

Pin Descriptions

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{LCD}1, 2	177, 163	V_{LCD}	—	Power supply
V_{CC}	166	V_{CC}	—	Power supply
GND1, 2	176, 170	GND	—	Power supply
V_1L, V_1R	165, 178	V_1L, V_1R	Input	Power supply
V_2L, V_2R	161, 181	V_2L, V_2R	Input	Power supply
V_5L, V_5R	162, 180	V_5L, V_5R	Input	Power supply
V_6L, V_6R	164, 179	V_6L, V_6R	Input	Power supply
CL	171	Clock	Input	Control signal
M	172	M	Input	Control signal
CH	175	CH	Input	Control signal
SHL	174	Shift left	Input	Control signal
DIO1	169	Data	Input/output	Control signal
DIO2	167	Data	Input/output	Control signal
DI	168	Data	Input	Control signal
$\overline{\text{DISPOFF}}$	173	Display off	Input	Control signal
X1–X160	1–160	X1–X160	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_{LCD}, GND: Supply power to the LCD drive circuits (figure 1).

V_1L, V_1R, V_2L, V_2R, V_5L, V_5R, V_6L, V_6R: Supply different power levels to drive the LCD. V_1 and V_2 are selected levels, and V_5 and V_6 are non-selected levels.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes the LCD drive outputs to AC.

CH: Selects the data shift mode. (CH = high: 2 × 80-output mode, CH = low: 160-output mode)

SHL: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1, DIO2: Input or output data. DIO1 is input and DIO2 is output when SHL is high. DIO1 is output and DIO2 is input when SHL is low.

DI: Input data. DI is input to X81–X160 when CH and SHL are high, and to X81–X1 when SHL is low.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets the LCD drive outputs X1–X160 to the V_2 level. A high $\overline{\text{DISPOFF}}$ is normally used.

LCD Drive Outputs

X1–X160: Each X outputs one of four voltage levels V_1, V_2, V_5, or V_6, depending on the combination of the M signal and the data level (figure 3).

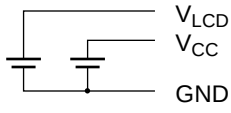


Figure 1 Power Supply for LCD Driver

SHL	Data shift direction
High	Shift to right DIO1 → SR1 → SR2 → SR3 • • • → SR160 → DIO2
Low	Shift to left DIO2 → SR160 → SR159 • • • → SR1 → DIO1

Note: SR1 to SR160 correspond to the outputs of X1 to X160, respectively.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL

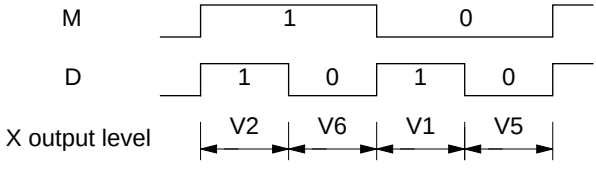
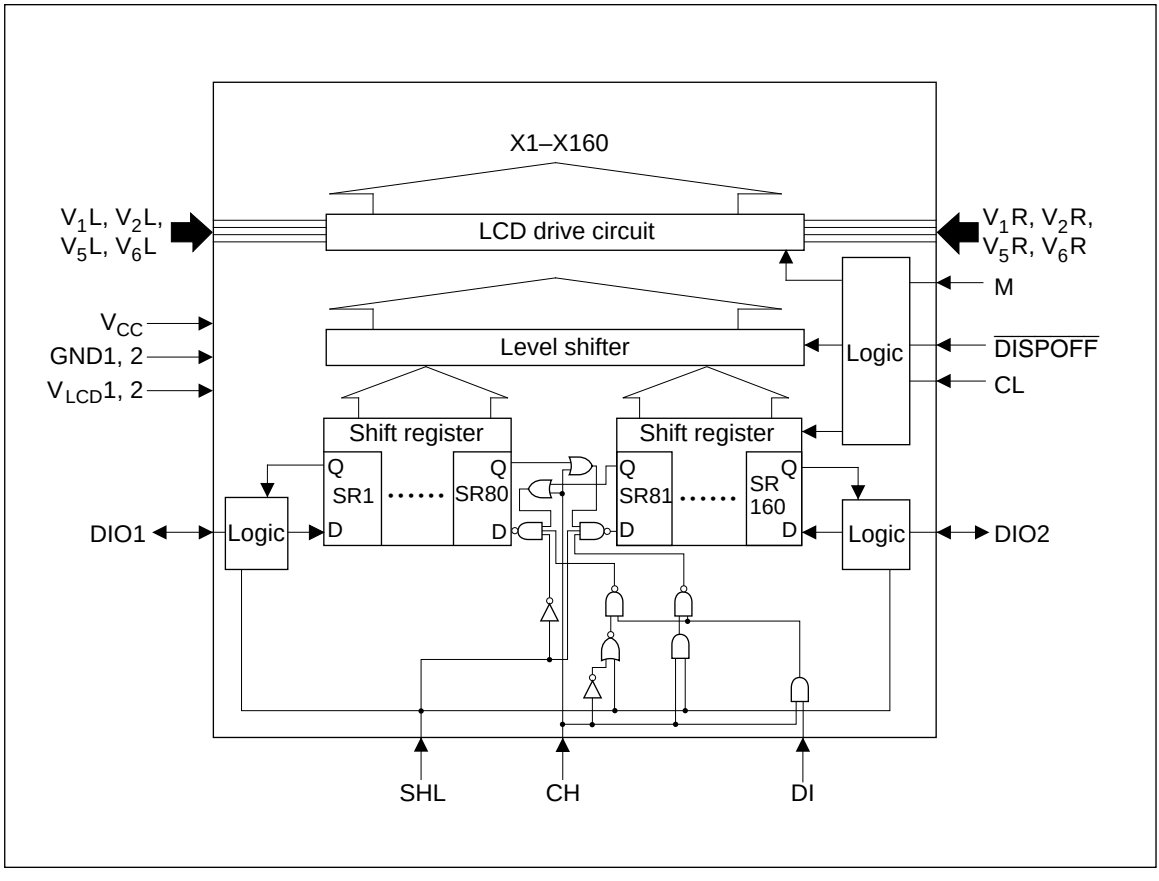


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuit

The 160-bit LCD drive circuit generates four voltage levels V_1, V_2, V_5, and V_6, which drive the LCD panel. One of these four levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signals (2.5 V–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 160-bit shift register shifts the data input via the DIO pin by one bit at a time. The one bit of shifted-out data is output from the DIO pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL pin selects the data shift direction.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{LCD} – 7.0 to V_{LCD} + 0.3	V	1, 3
Input voltage 3	V_{T3}	–0.3 to +7.0	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes:
1. The reference point is GND (0 V).
2. Applies to pins CL, M, SHL, DI, $\overline{\text{DISPOFF}}$, and CH.
3. Applies to pins V_1 and V_6.
4. Applies to pins V_2 and V_5.
5. Power should be applied to V_{CC}–GND first, and then V_{LCD}–GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its specified operating range in order to prevent malfunctions or loss of reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, V_{LCD} – GND = 14 to 40 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	0.8 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.2 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Xj on resistance	R_{ON}	3	—	0.7	1.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5	—	5	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{LCD} to GND	
Current consumption 1	I_{GND}	—	—	—	0.5	µA	f_{CL} = 36 kHz f_M = 75 kHz	2
Current consumption 2	I_{LCD}	—	—	—	1.0	µA		

Note: Pins: 1. CL, M, SHL, CH, DI, DIO1, DIO2, $\overline{\text{DISPOFF}}$
2. DIO1, DIO2
3. X1–X160, V
4. V_1, V_2, V_5, V_6

Notes: 1. Indicates the resistance between one of the pins X1–X160 and one of the voltage supply pins V_1, V_2, V_5, or V_6, when load current is applied to the X pin; defined under the following conditions:

Ta = 25°C Note that RON depends on Ta (°C) (figure 4).
V_{LCD}–GND = 40 V
V_1, V_6 = V_{CC} – {1/20 (V_{LCD}–GND)}
V_5, V_2 = GND + {1/20 (V_{LCD}–GND)}

All voltages must be within ΔV, $V_{LCD} \geq V_1 \geq V_6 \geq V_{LCD} - 7.0$ V, and 7.0 V ≥ $V_5 \geq V_2 \geq$ GND. Note that ΔV depends on the power supply voltage V_{LCD}–GND (figure 6).

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held at V_{CC} and GND, respectively.

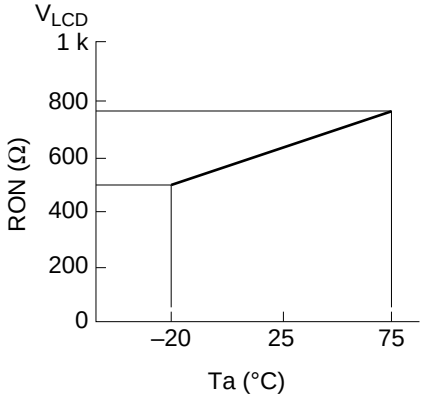


Figure 4 Relation between RON and Ta

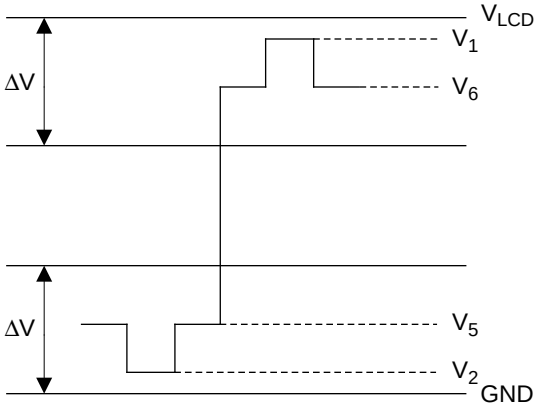


Figure 5 Relation between Driver Output Waveform and Voltage Levels

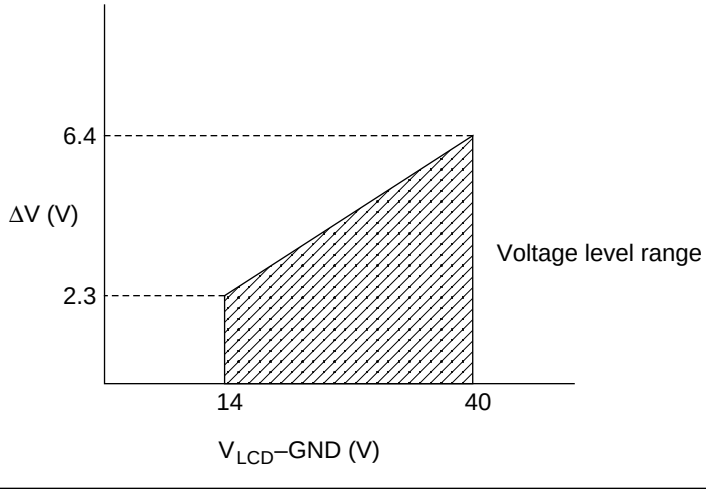


Figure 6 Relation between V_{LCD}–GND and ΔV

AC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	350	ns	1
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	1.2	µs	2
Output delay time 2	t_{pd2}	X (n), M	—	1.2	µs	2

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	150	ns	1
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	0.7	µs	2
Output delay time 2	t_{pd2}	X (n), M	—	0.7	µs	2

Note: 1, 2 The load circuit shown in figure 6 is connected.

Figure 7 Load Circuit

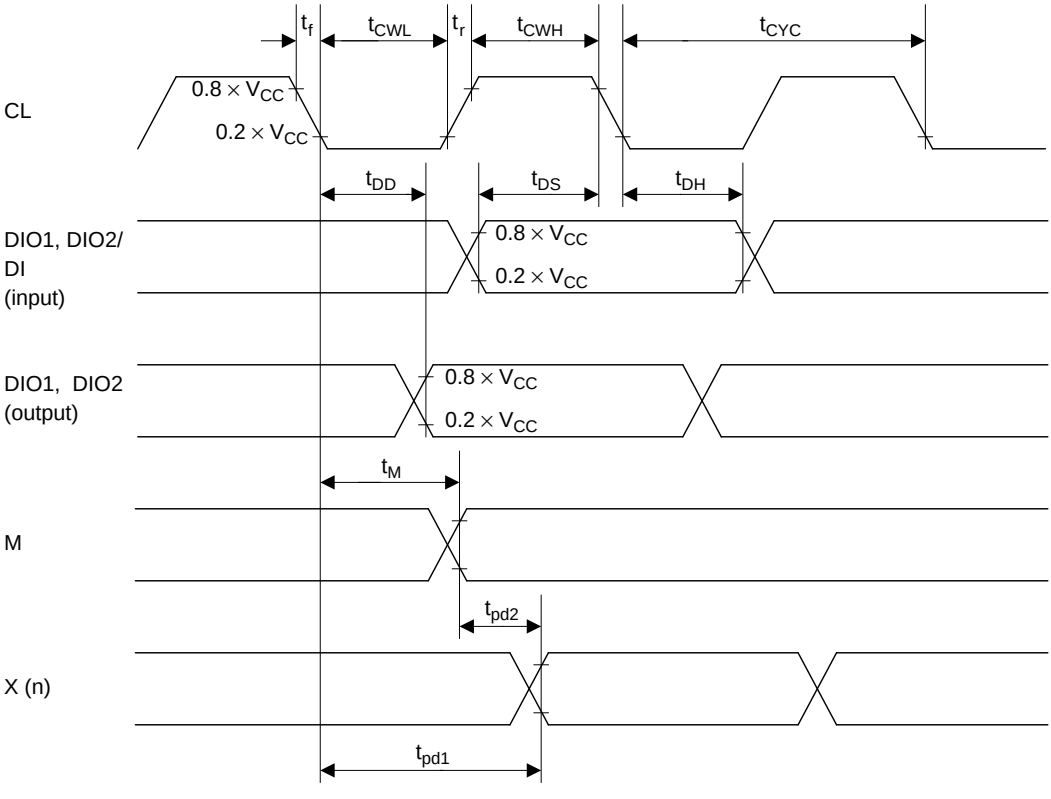
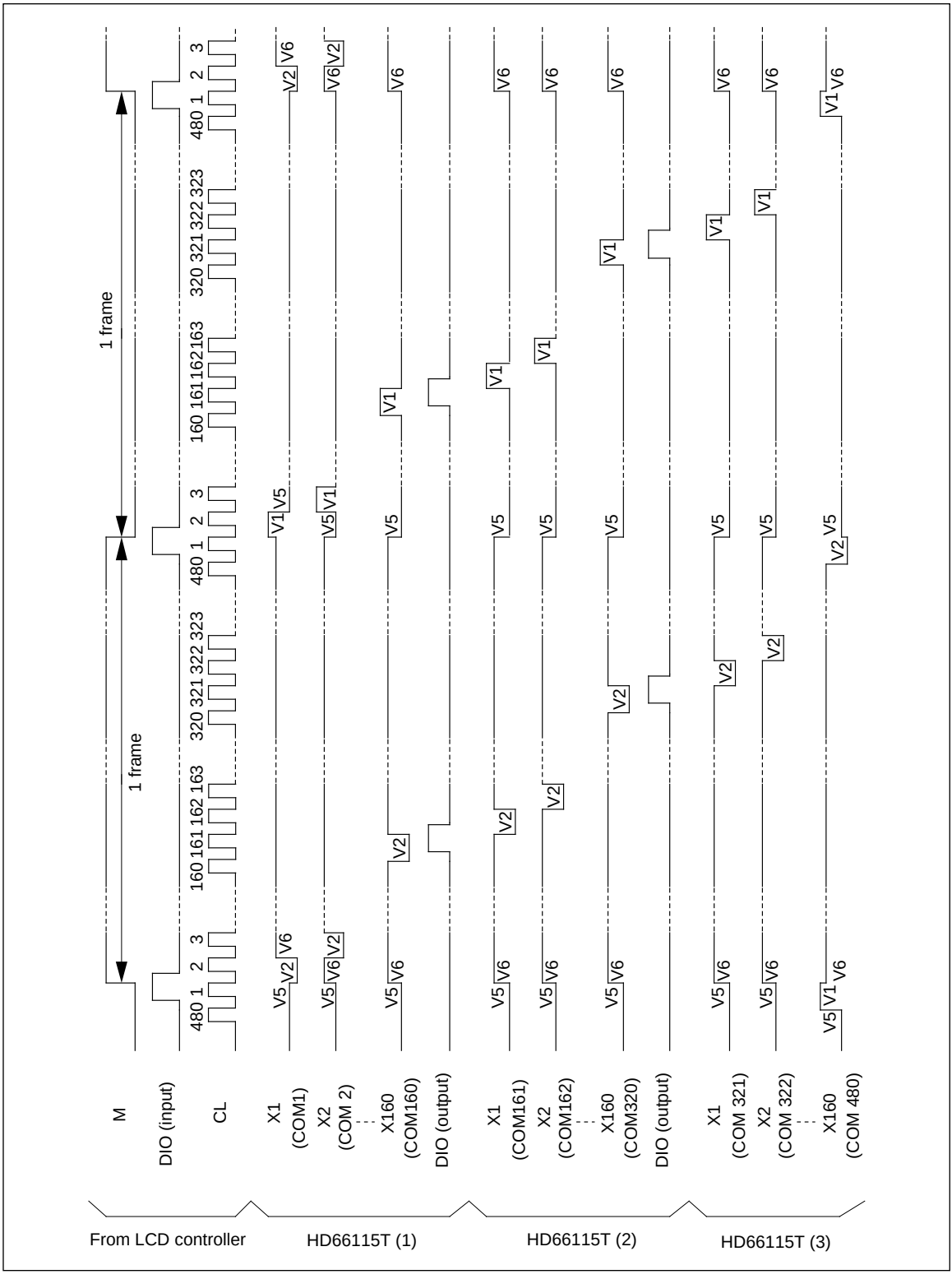


Figure 8 LCD Controller Interface Timing

Operation Timing (1/480 Duty Cycle)



Connection Examples

Figures 8 and 9 show examples of how HD66115Ts can be configured to drive a 480-line LCD panel with a 1/240 duty cycle. Figures 10 and 11 show examples of how HD66115Ts can be configured to drive a 480-line LCD panel with a 1/480 duty cycle. The HD66115T's 160 channels can be divided into two groups of 80 channels, and its data shift direction can be changed by selecting the data output mode pin (CH) and data shift pin (SHL), respectively.

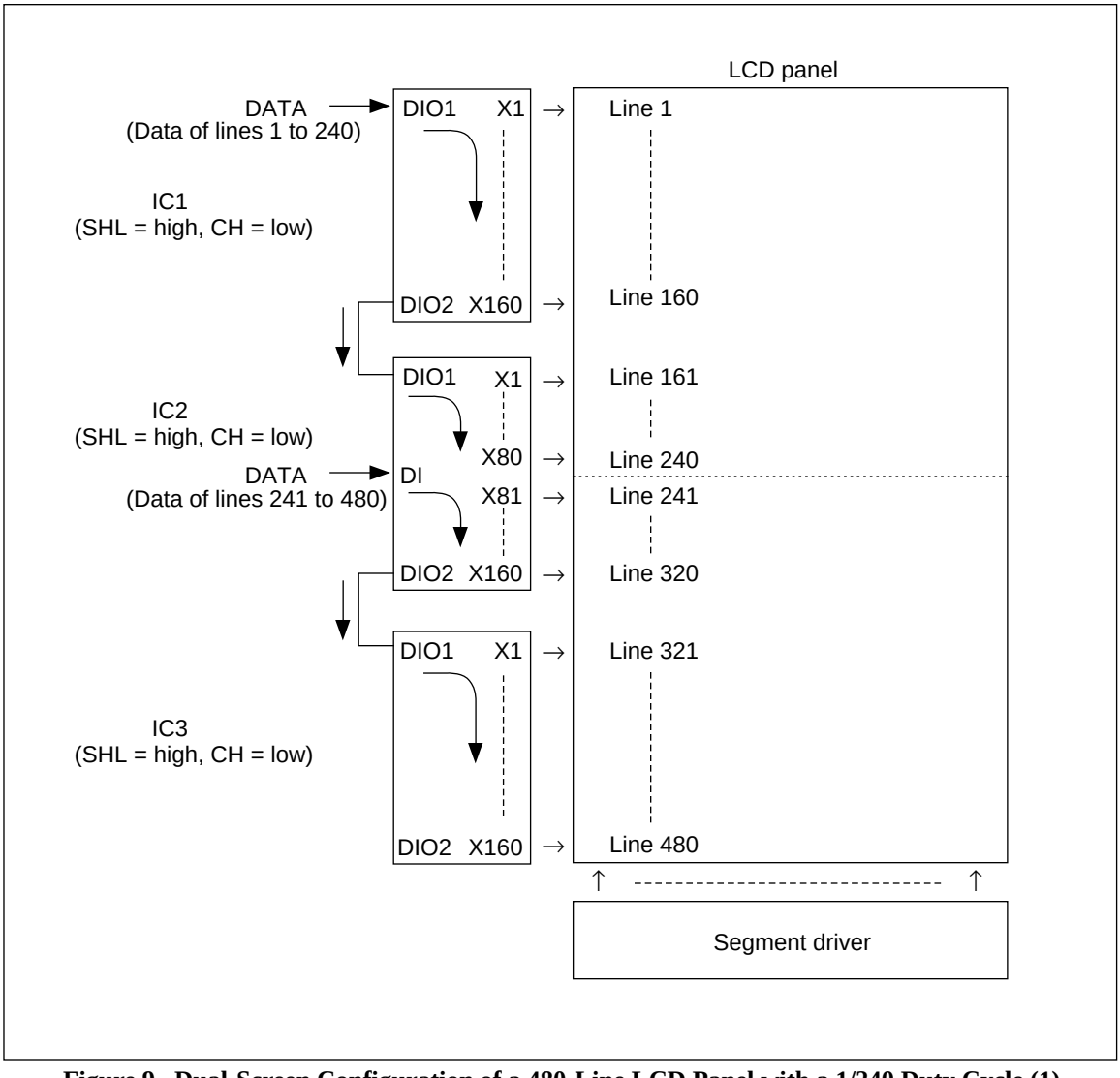


Figure 9 Dual-Screen Configuration of a 480-Line LCD Panel with a 1/240 Duty Cycle (1)

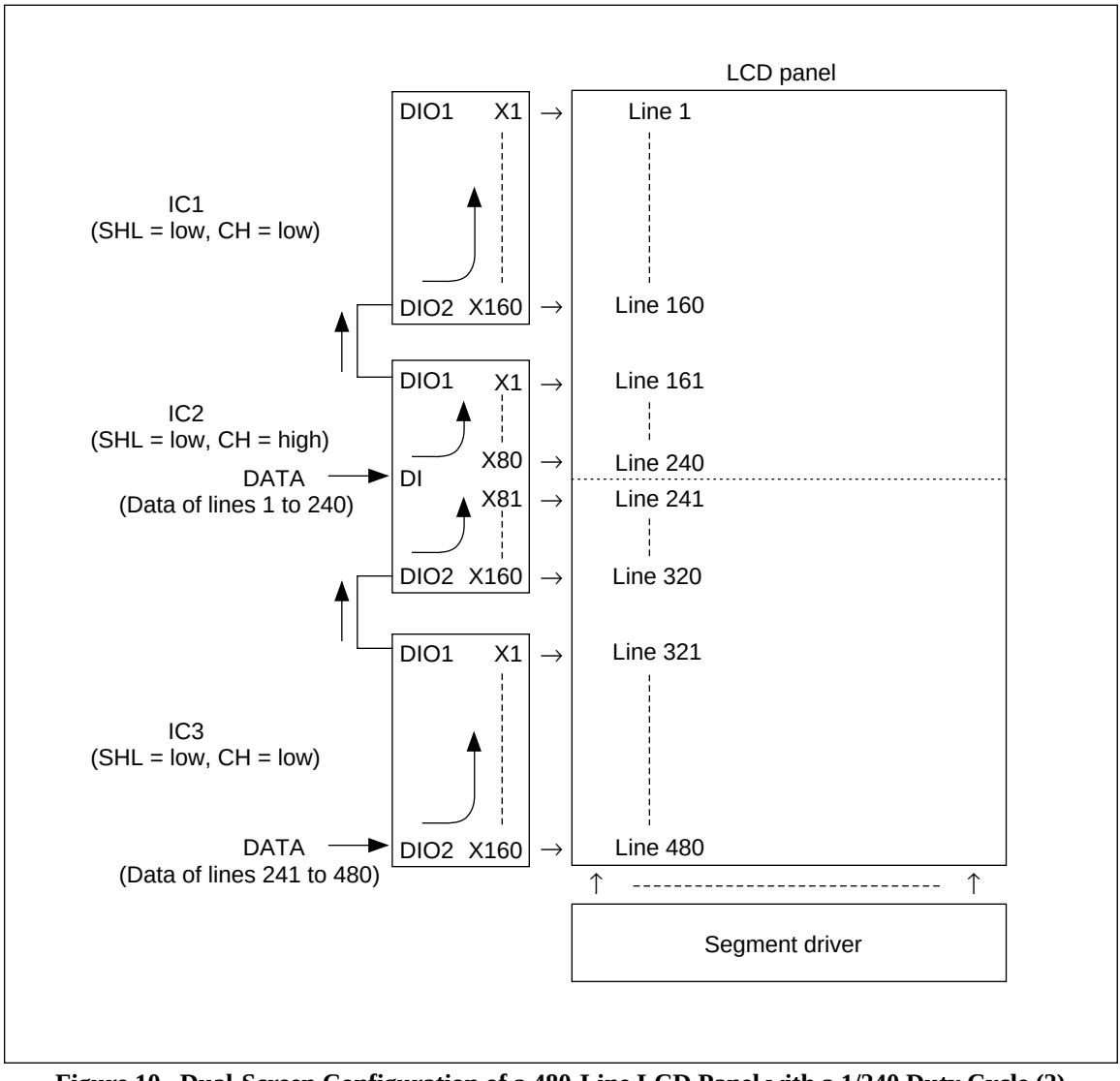


Figure 10 Dual-Screen Configuration of a 480-Line LCD Panel with a 1/240 Duty Cycle (2)

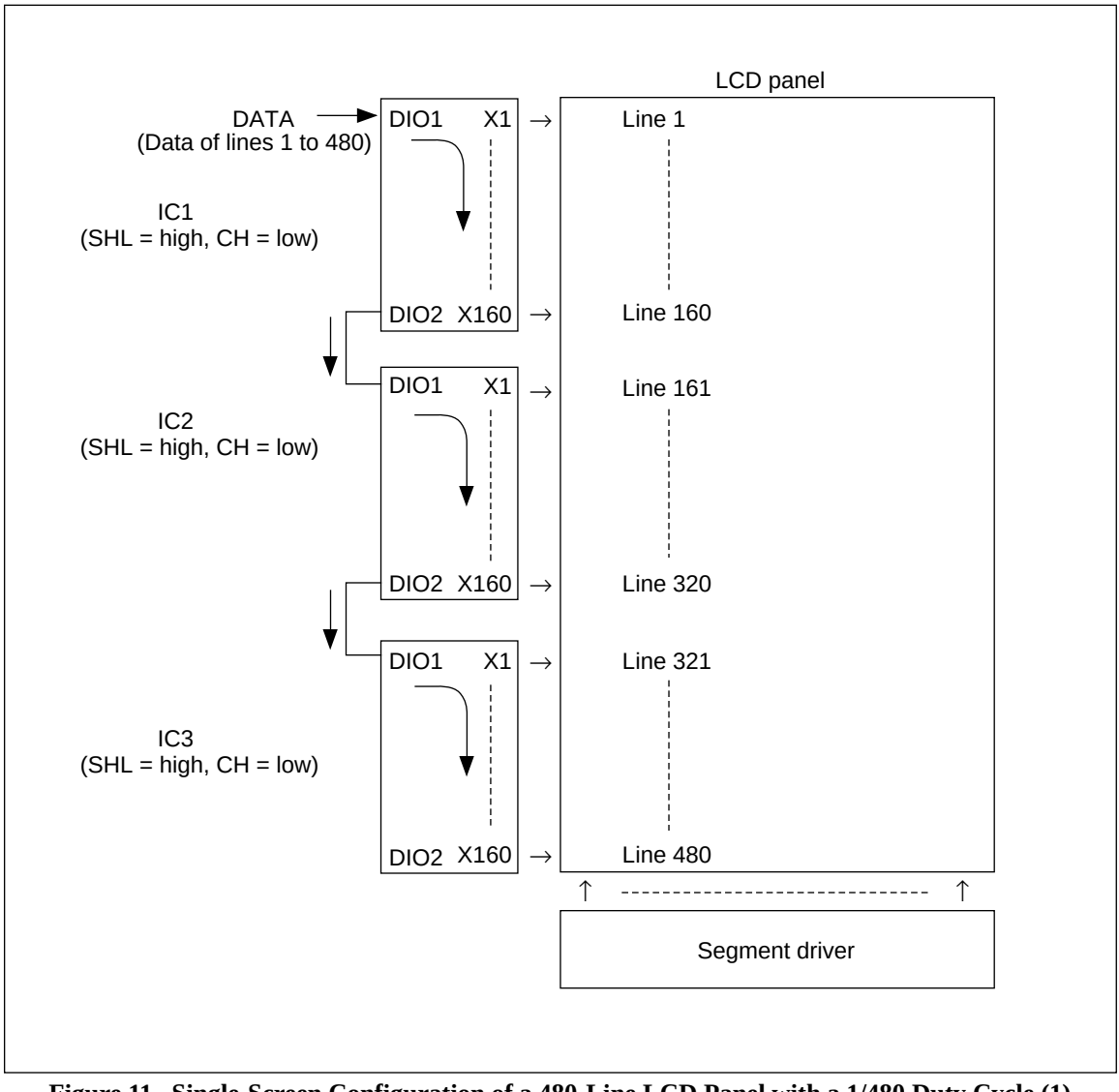


Figure 11 Single-Screen Configuration of a 480-Line LCD Panel with a 1/480 Duty Cycle (1)

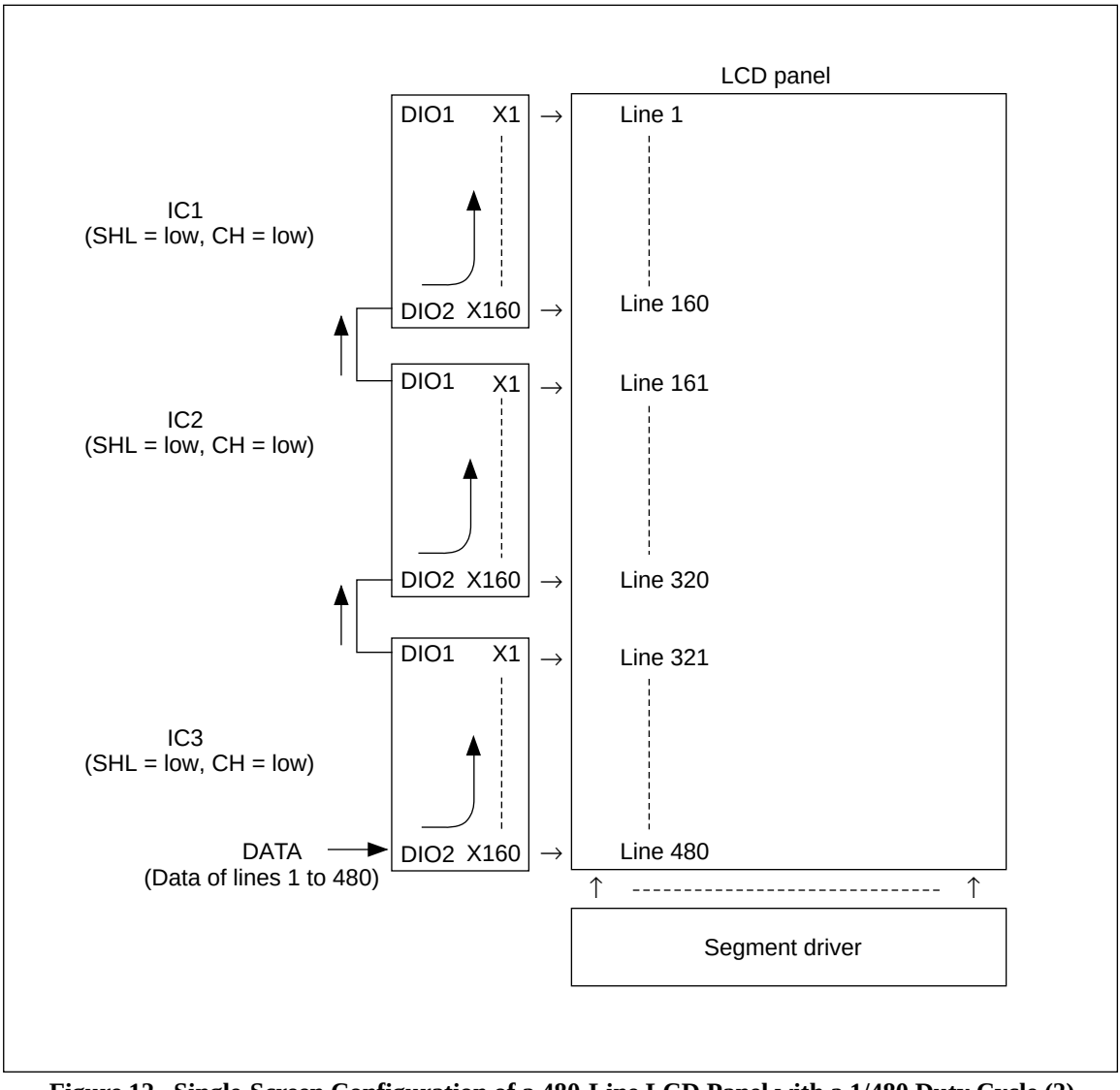


Figure 12 Single-Screen Configuration of a 480-Line LCD Panel with a 1/480 Duty Cycle (2)

HD66120T

(240-Channel Segment Driver for Dot-Matrix Graphic Liquid Crystal Display)

HITACHI

Description

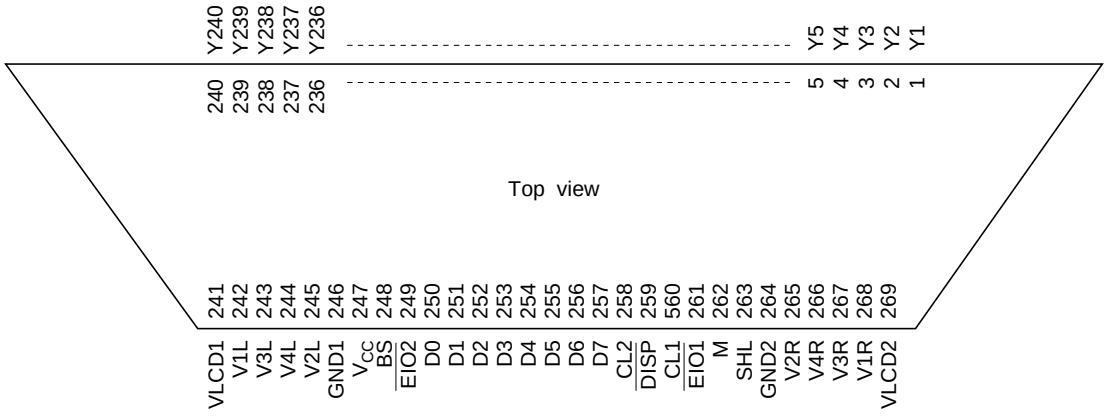
The HD66120T is a segment driver for dot-matrix graphic liquid crystal display (LCD). It features a maximum driving voltage of 40 V, enabling a high duty cycle. This driver operates at about 3 V, making it suitable for battery-driven applications that make use of the low power dissipation of liquid crystal elements. The HD66120T, packaged in a fine-pitch slim tape carrier package (TCP), helps to reduce the size of the frame around an LCD panel.

Features

- Duty cycle: 1/100 to 1/480
- High LCD driving voltage: 14 to 40 V
- 240 LCD drive circuits
- Low operating voltage: 2.7 to 5.5 V
- 4- and 8-bit data bus interface
- High-speed shift clocks
  - — 10 MHz (max) at 3-V operation
  - — 20 MHz (max) at 5-V operation
- Display off function
- Slim-TCP package
- Fine output lead pitch: 70 µm
- Compact user area: 9.44 mm (when output lead pitch is 70 µm)
- Internal chip enable signal generator
- Standby function

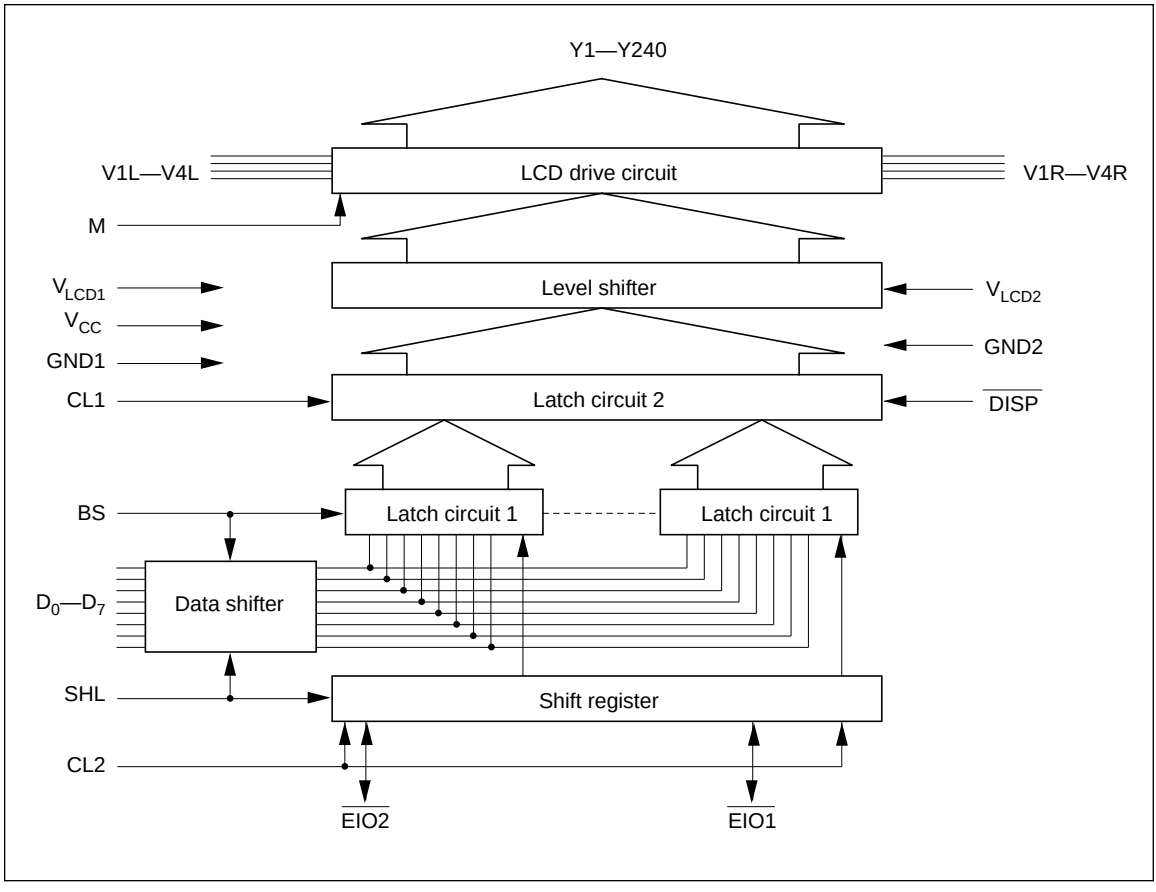
Hitachi semiconductor

Pin Arrangement



Note: This figure does not specify the TCP dimensions; other TCP shapes are also possible.

Block Diagram



Block Functions

LCD Drive Circuit

The 240-bit LCD drive circuit generates four voltage levels V1, V2, V3, and V4, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on the combination of the M signal and the data in latch circuit 2.

Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Latch Circuit 2

240-bit latch circuit 2 latches data input from latch circuit 1, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit 1

240-bit latch circuit 1 latches 4-bit or 8-bit parallel data input via the D_0 to D_7 pins at the timing generated by the shift register.

Shift Register

The 60-bit shift register generates and outputs data latch signals for latch circuit 1 at the falling edge of each clock 2 (CL2) pulse.

Data Shifter

The data shifter shifts the destinations of display data output, when necessary.

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	247	V_{CC}	—	Power supply
GND1, GND2	246, 264	GND1, GND2	—	Power supply
V_{LCD1}, V_{LCD2}	241, 269	V_{LCD1}, V_{LCD2}	—	Power supply
V1L, V1R	242, 268	V1L, V1R	Input	Power supply
V2L, V2R	245, 265	V2L, V2R	Input	Power supply
V3L, V3R	243, 267	V3L, V3R	Input	Power supply
V4L, V4R	244, 266	V4L, V4R	Input	Power supply
CL1	260	Clock 1	Input	Control signal
CL2	258	Clock 2	Input	Control signal
M	262	M	Input	Control signal
D_0–D_7	250–257	Data 0–data 7	Input	Control signal
SHL	263	Shift left	Input	Control signal
$\overline{EIO1}$, $\overline{EIO2}$	261, 249	Enable IO 1, enable IO 2	Input/output	Control signal
$\overline{DISP}$	259	Display off	Input	Control signal
BS	248	Bus select	Input	Control signal
Y_1–Y_{240}	1–240	Y_1–Y_{240}	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, V_{LCD}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{LCD}–GND supplies power to the LCD drive circuits. See figure 1.

V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R: Supply different levels of power to drive the LCD. V1 and V2 are selected levels, and V3 and V4 are non-selected levels.

Control Signals

CL1: Inputs display data latch pulses for latch circuit 2. Latch circuit 2 latches display data input from latch circuit 1, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for latch circuit 1. Latch circuit 1 latches display data input via D_0–D_7 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_7: Input display data. High-voltage level (V_{CC} level) of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level (GND level) data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output, and determines which chip enable pin ($\overline{EIO1}$ or $\overline{EIO2}$) is an input and which is an output. See figure 2.

$\overline{EIO1}$, $\overline{EIO2}$: If SHL is GND level, $\overline{EIO1}$ inputs the chip enable signal, and $\overline{EIO2}$ outputs the signal. If SHL is V_{CC} level, $\overline{EIO1}$ outputs the chip enable signal, and $\overline{EIO2}$ inputs the signal. The chip enable input pin of the first HD66120T must be grounded, and those of the other HD66120Ts must be connected to the chip enable output pin of the previous HD66120T. The chip enable output pin of the last HD66120T must be open.

$\overline{DISP}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{240} to V2 level.

BS: Selects either the 4-bit or 8-bit display data bus interface. If BS is V_{CC} level, the 8-bit bus is selected, and if BS is GND level, the 4-bit bus is selected. In 4-bit bus mode, data is latched via D_0–D_3; D_4–D_7 must be grounded.

LCD Drive Output

Y_1–Y_{240}: Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on the combination of the M signal and display data levels. See figure 3.

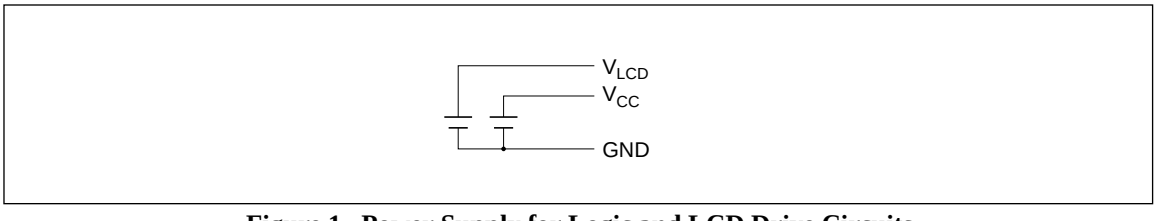


Figure 1 Power Supply for Logic and LCD Drive Circuits

SHL = V_{CC}, BS = GND

Y240	Y239	Y238	Y237	Y236	Y235	Y234	Y233		Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
D0	D1	D2	D3	D0	D1	D2	D3	----------	D0	D1	D2	D3	D0	D1	D2	D3
Last data													1st data			

$\overline{EIO1}$: chip enable input
$\overline{EIO2}$: chip enable output

SHL = GND, BS = GND

Y240	Y239	Y238	Y237	Y236	Y235	Y234	Y233		Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
D3	D2	D1	D0	D3	D2	D1	D0	----------	D3	D2	D1	D0	D3	D2	D1	D0
Last data													1st data			

$\overline{EIO1}$: chip enable input
$\overline{EIO2}$: chip enable output

SHL = V_{CC}, BS = V_{CC}

Y240	Y239	Y238	Y237	Y236	Y235	Y234	Y233		Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
D0	D1	D2	D3	D4	D5	D6	D7	----------	D0	D1	D2	D3	D4	D5	D6	D7
Last data													1st data			

$\overline{EIO1}$: chip enable input
$\overline{EIO2}$: chip enable output

SHL = GND, BS = V_{CC}

Y240	Y239	Y238	Y237	Y236	Y235	Y234	Y233		Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
D7	D6	D5	D4	D3	D2	D1	D0	----------	D7	D6	D5	D4	D3	D2	D1	D0
1st data													Last data			

$\overline{EIO1}$: chip enable input
$\overline{EIO2}$: chip enable output

Figure 2 Selection of Destinations of Display Data Output

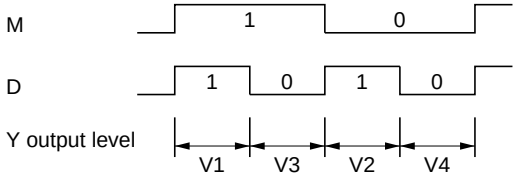


Figure 3 Selection of LCD Drive Output Level

Operation Timing

4-Bit Bus Mode (BS = GND)

Figure 4 shows 4-bit data latch timing when SHL = GND, that is, the $\overline{EIO1}$ pin is a chip enable input and $\overline{EIO2}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{EIO1}$ pin is a chip enable output and $\overline{EIO2}$ pin is a chip enable input.

When a low chip enable signal is input via the $\overline{EIO1}$ pin, the HD66120T is first released from data standby state, and, at the falling edge of the following CL2 pulse, it is released entirely from standby state and starts latching data. It simultaneously latches 4 bits of data at the falling edge of each CL2 pulse. When it has latched 236 bits of data, it sets the $\overline{EIO2}$ signal low. When it has latched 240 bits of data, it automatically stops and enters standby state, initiating the next HD66120T, as long as its $\overline{EIO2}$ pin is connected to the $\overline{EIO1}$ pin of the next HD66120T.

The HD66120Ts output one line of data from the Y_1–Y_{240} pins at the falling edge of each CL1 pulse. Data d1 is output from Y1, and d_{240} from Y_{240} when SHL = GND, and d_1 is output from Y_{240}, and d_{240} from Y_1 when SHL = V_{CC}. Data output level is either V_{LCD}, V2, V3, or V4 depending on the combination of the M signal and the data level.

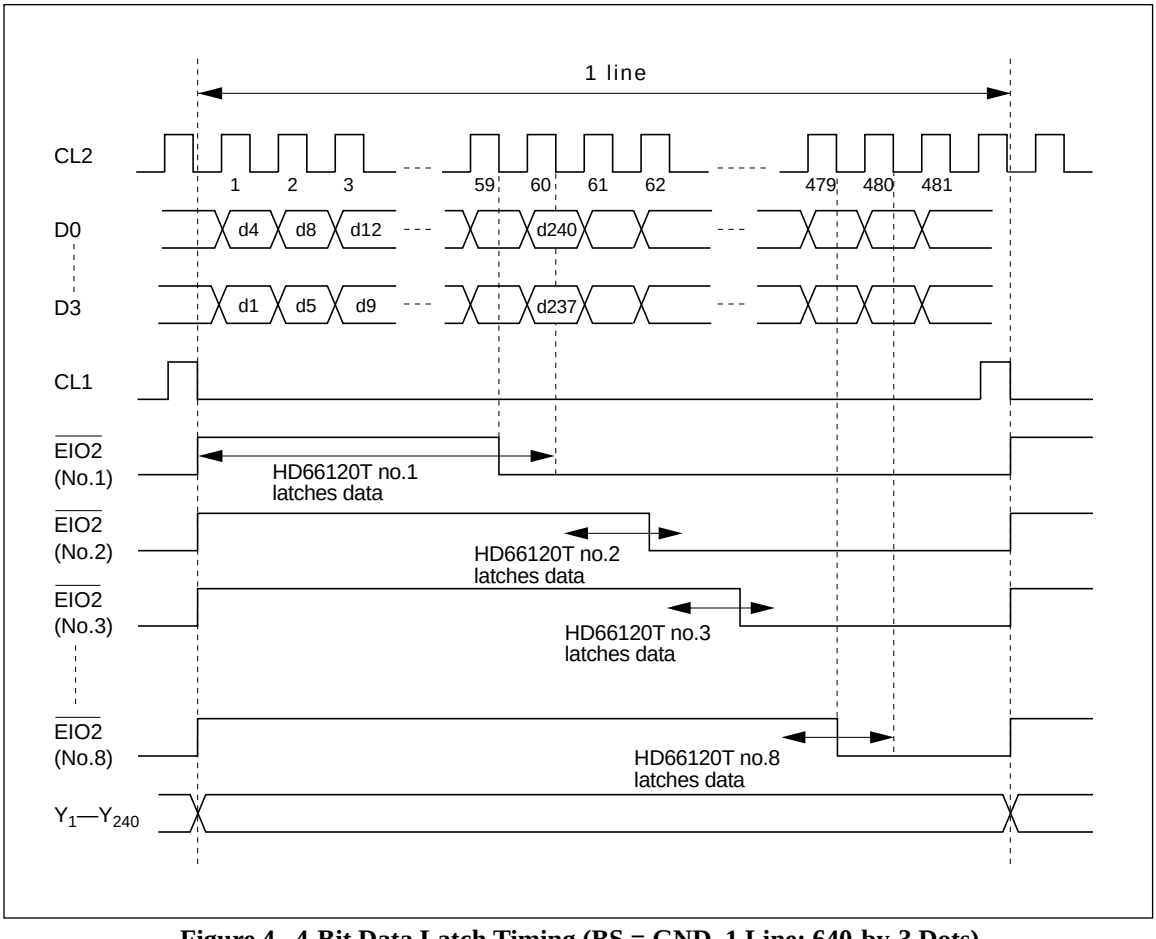


Figure 4 4-Bit Data Latch Timing (BS = GND, 1 Line: 640-by-3 Dots)

8-Bit Bus Mode (BS = V_{CC})

Figure 5 shows 8-bit data latch timing when SHL = GND, that is, the $\overline{EIO1}$ pin is a chip enable input and $\overline{EIO2}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{EIO1}$ pin is a chip enable output and $\overline{EIO2}$ pin is a chip enable input.

The operation is the same as that in 4-bit bus mode except that 8 bits of data are latched simultaneously.

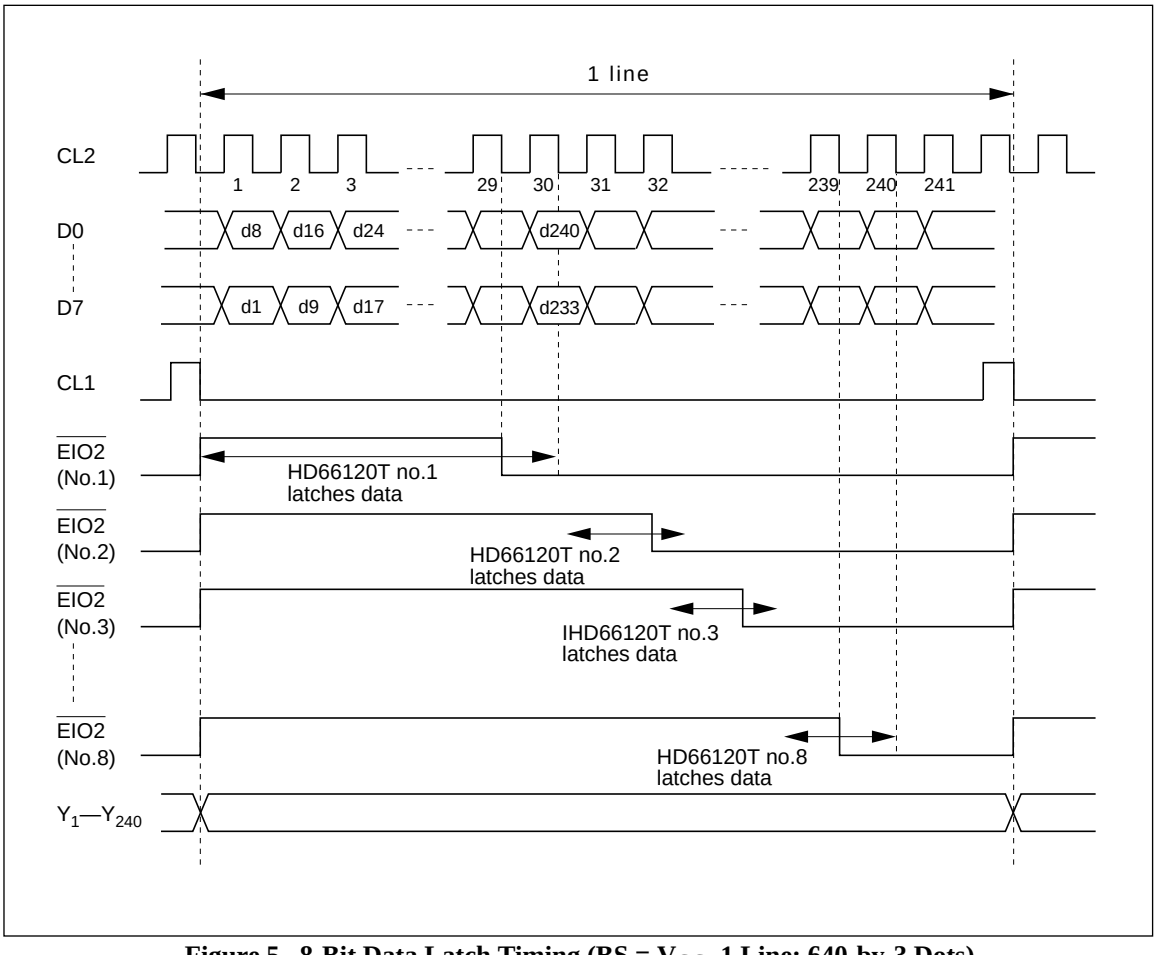
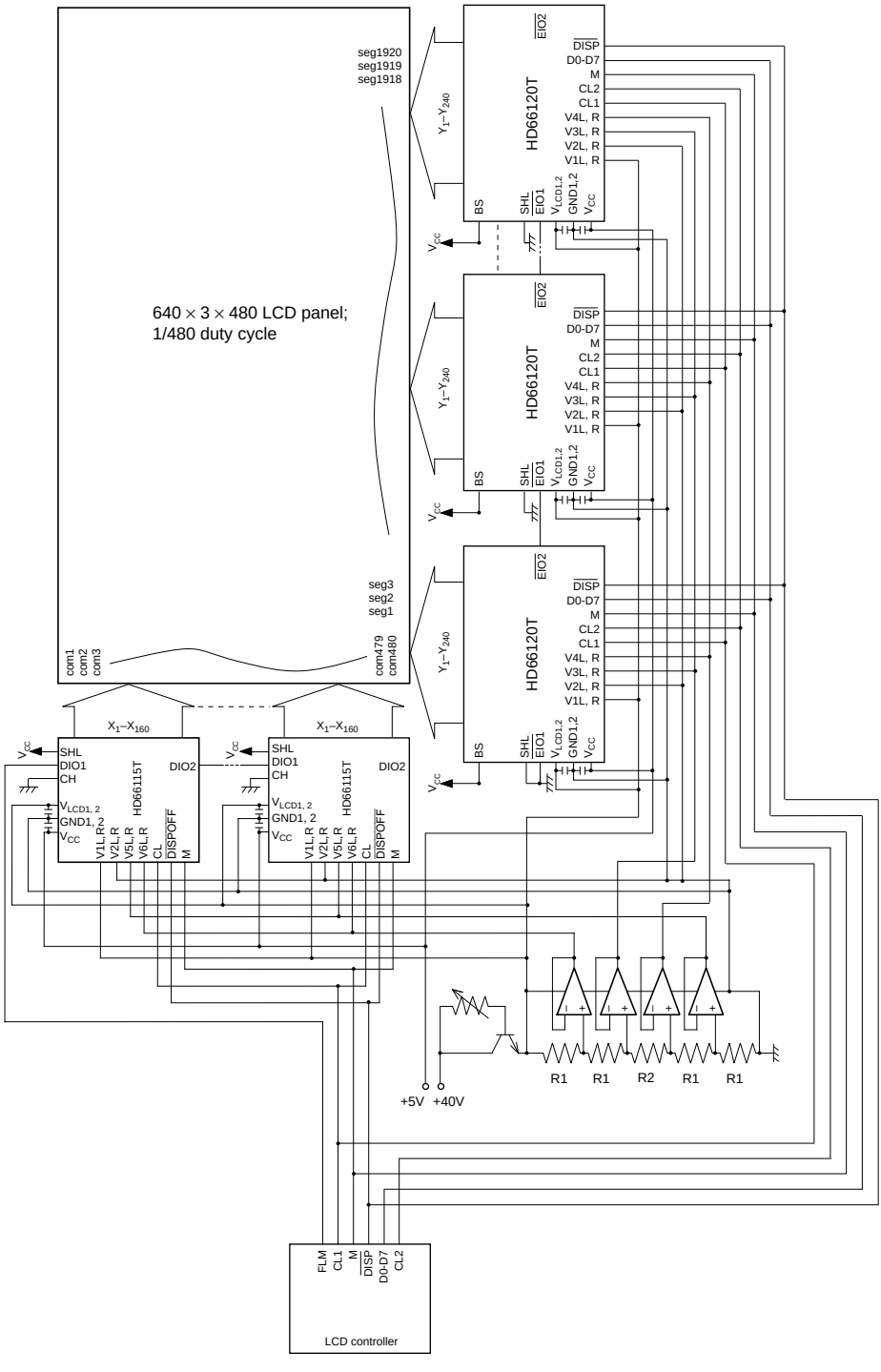


Figure 5 8-Bit Data Latch Timing (BS = V_{CC}, 1 Line: 640-by-3 Dots)

Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/20 bias, R1 and R2 must be 3 kΩ and 48 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/20.

2. To stabilize the power supply, place two 0.1-µF capacitors near each HD66120T, one between the V_{CC} and GND pins, and the other between the V_{LCD} and GND pins.

3. The load must be less than 30 pF between the $\overline{EIO2}$ and $\overline{EIO1}$ connections of HD66120Ts.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 4
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 4
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0 V).
2. Applies to input pins for logic circuits.
3. Applies to V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R pins.
4. Power should be applied to V_{CC}–GND first, and then V_{LCD}–GND. It should be disconnected in the reverse way.
5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.7 to 4.5 V, V_{LCD} – GND = 14 to 40 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	V_{IN} = V_{LCD} to GND	2
Current consumption 1	I_{CC}	—	—	3.3	mA	V_{CC} = 3.0 V f_{CL2} = 10 MHz f_{CL1}= 36 kHz f_M = 75 Hz	2
Current consumption 2	I_{LCD}	—	—	3.8	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.45	mA	Same as above	2, 3

Pins and notes at the end of the DC characteristics 2 table.

DC Characteristics 2 (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 14 to 40 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	V_{IN} = V_{LCD} to GND	2
Current consumption 1	I_{CC}	—	—	10	mA	f_{CL2} = 12 MHz f_{CL1} = 36 kHz f_M = 75 Hz	2
Current consumption 2	I_{LCD}	—	—	3.8	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	1.0	mA	Same as above	2, 3

Pins: 1. CL1, CL2, M, SHL, BS, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISP}$, D_0–D_7
2. $\overline{EIO1}$, $\overline{EIO2}$
3. Y_1–Y_{240}, V_{LCD1}, V_{LCD2}, V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R
4. V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R

Notes: 1. Indicates the resistance between one pin from Y_1–Y_{240} and another pin from V1–V4, when load current is applied to the Y pin; defined under the following conditions.

V_{LCD} – GND = 40 V
V1, V3 = V_{LCD} – {1/20(V_{LCD} – GND)}
V2, V4 = GND + {1/20(V_{LCD} – GND)}

V1 and V3 should be near V_{LCD} level, and V2 and V4 should be near GND level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{LCD}–GND (figure 7).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

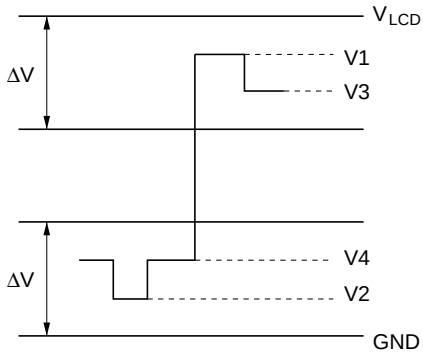


Figure 6 Relation between Driver Output Waveform and Level Voltages

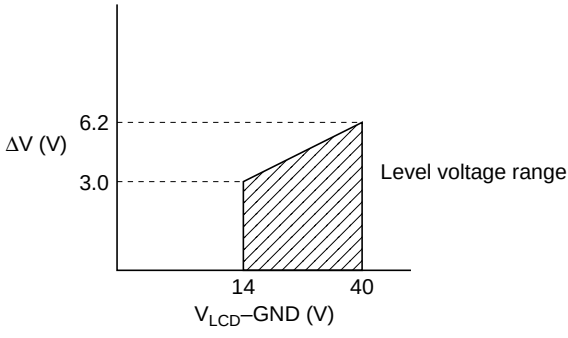


Figure 7 Relation between V_{LCD} – GND and ΔV

AC Characteristics 1 (V_{CC} = 2.7 to 4.5 V, V_{LCD} – GND = 14 to 40 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	100	—	ns
Clock high-level width 1	t_{CWH2}	CL2	37	—	ns
Clock low-level width 1	t_{CWL2}	CL2	37	—	ns
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns
Clock hold time	t_{HCL}	CL1, CL2	100	—	ns
Clock rise time	t_r	CL1, CL2	—	50*1	ns
Clock fall time	t_f	CL1, CL2	—	50*1	ns
Data setup time	t_{DS}	D_0–D_7, CL2	35	—	ns
Data hold time	t_{DH}	D_0–D_7, CL2	35	—	ns
M phase difference time	t_{CM}	M, CL1	—	300	ns
Output delay time 1	t_{pd1}	CL1, Y_1–Y_{240}	—	1.2	µs
Output delay time 2	t_{pd2}	M, Y_1–Y_{240}	—	1.2	µs

Notes at the end of the AC characteristics 2 table.

AC Characteristics 2 (V_{CC} = 5 V ± 10%, V_{LCD} – GND = 28 to 40 V, and Ta = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	50	—	ns
Clock high-level width 1	t_{CWH2}	CL2	15	—	ns
Clock low-level width 1	t_{CWL2}	CL2	15	—	ns
Clock high-level width 2	t_{CWH1}	CL1	15	—	ns
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns
Clock hold time	t_{HCL}	CL1, CL2	100	—	ns
Clock rise time	t_r	CL1, CL2	—	50*1	ns
Clock fall time	t_f	CL1, CL2	—	50*1	ns
Data setup time	t_{DS}	D_0–D_7, CL2	5	—	ns
Data hold time	t_{DH}	D_0–D_7, CL2	15	—	ns
M phase difference time	t_{CM}	M, CL1	—	300	ns
Output delay time 1	t_{pd1}	CL1, Y_1–Y_{240}	—	0.7	µs
Output delay time 2	t_{pd2}	M, Y_1–Y_{240}	—	0.7	µs

Notes: 1. The clock rise and fall times (t_r, t_f) must satisfy the following relationships:
t_r, $t_f < (t_{CYC} - t_{CWH2} - t_{CWL2})/2$
t_r, $t_f \leq 50$ ns

2. The load must be less than 30 pF between the $\overline{EIO2}$ and $\overline{EIO1}$ connections of HD66120Ts.

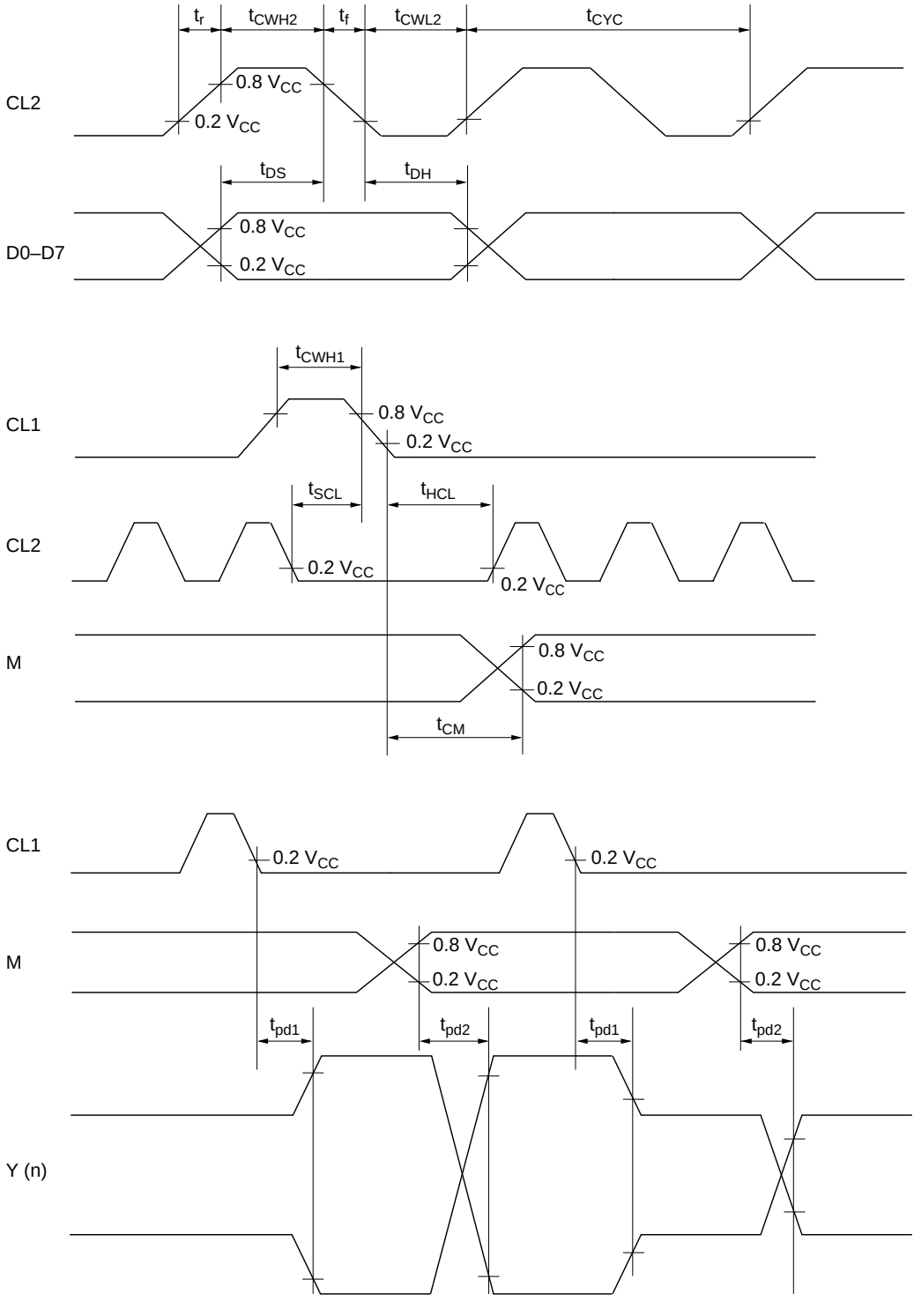


Figure 8 LCD Controller Interface Timing

HD61602/HD61603

(Segment Type LCD Driver)

HITACHI

Description

The HD61602 and the HD61603 are liquid crystal display driver LSIs with a TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for the liquid crystal display driver. Using the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Wide-range operating voltage
  - — Operates in a wide range of supply voltage: 2.2 V to 5.5 V
  - — Compatible with TTL interface at 4.5 V to 5.5 V
- Low current consumption
  - — Can run from a battery power supply (100 µA max. at 5 V)
  - — Standby input enables standby operation at lower current consumption (5 µA max. on 5 V)
- Internal power supply circuit for liquid crystal display driver (HD61602)
  - — Internal power supply circuit for liquid crystal display driver facilitates the connection to a microprocessor system

Ordering Information

Type No.	Package
HD61602R	80-pin plastic QFP (FP-80)
HD61602RH	80-pin plastic QFP (FP-80A)
HD61603R	80-pin plastic QFP (FP-80)

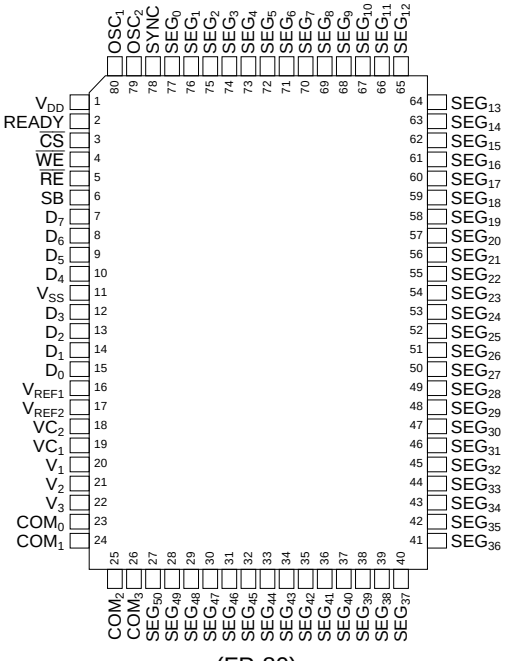
Versatile Segment Driving Capacity

Type No.	Driving Method		Display Segments	Example of Use	Frame Freq. (Hz) at f_{OSC} = 100 kHz	Package
HD61602	Static		51	8 segments × 6 digits + 3 marks	33	80-pin plastic QFP (FP-80, FP-80A, TFP-80)
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	65	
	1/3 bias	1/3 duty	153	9 segments × 17 digits	208	
		1/4 duty	204	8 segments × 25 digits + 4 marks	223	
HD61603	Static		64	8 segments × 8 digits	33	80-pin plastic QFP (FP-80)

Hitachi semiconductor

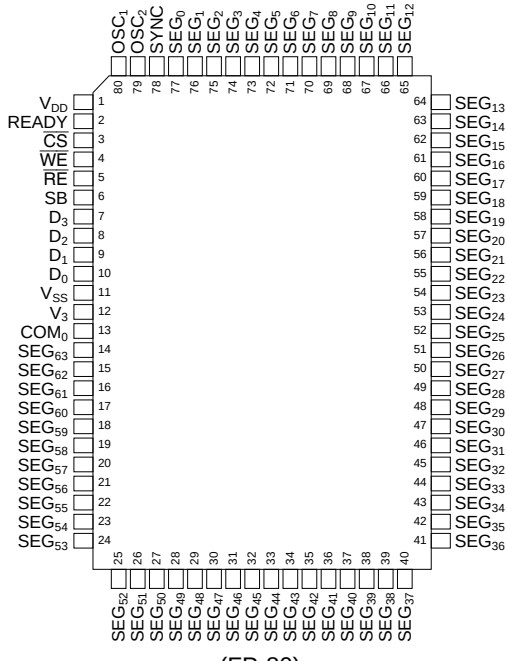
Pin Arrangement

HD61602R



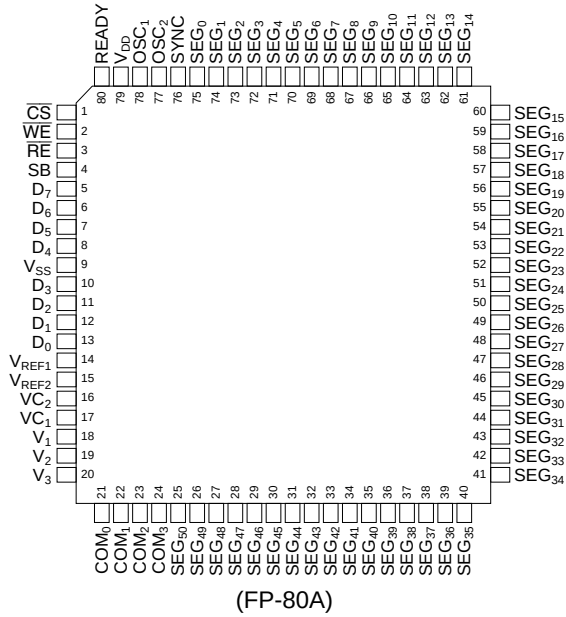
(FP-80)

HD61603R



(FP-80)

HD61602RH

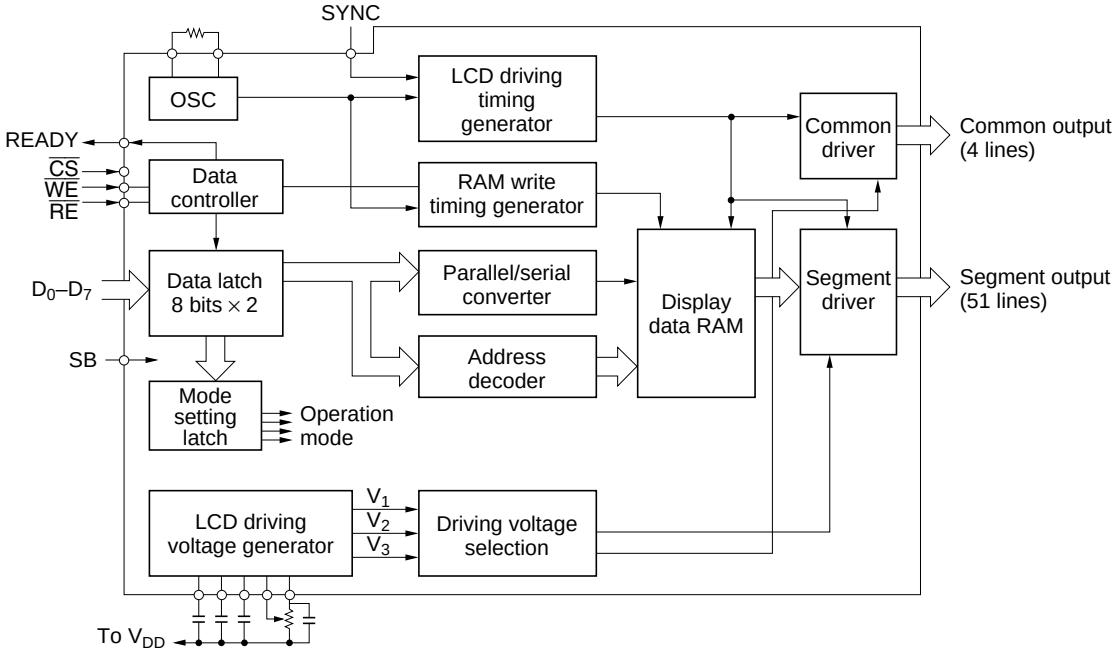


(FP-80A)

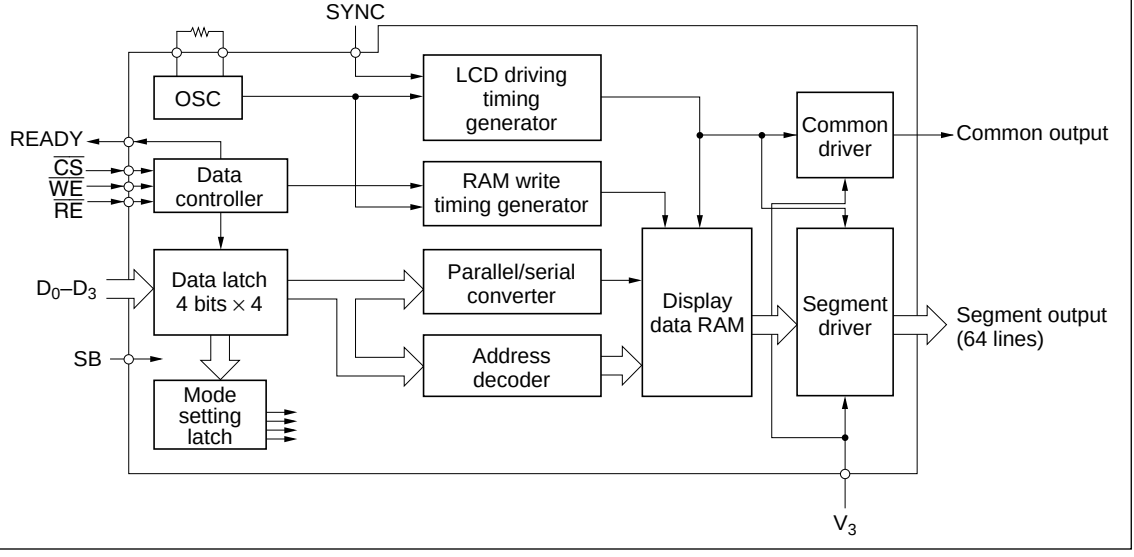
(Top view)

Block Diagram

HD61602



HD61603



Terminal Functions

HD61602 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D_0 to D_7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0–D_7	8	Input	MCU	Data input terminal for 8-bit × 2-byte data.
V_{SS}	1	Power supply		Negative power supply.
V_{REF1}	1	Output	External R	Reference voltage output. Generates LCD driving voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2} \approx V_1$.
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}.
V_1, V_2, V_3	3	Output (Input)	External C	LCD driving voltage outputs. An external C is connected to each terminal.
COM_0–COM_3	4	Output	LCD	LCD common (backplate) driving output.
SEG_0–SEG_{50}	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC1.

Note: Logic polarity is positive. 1 = high = active.

HD61603 Terminal Functions

Terminal Name	No. of Lines	Input/Output	Connected to	Function
V_{DD}	1	Power supply		Positive power supply.
READY	1	NMOS open drain output	MCU	While data is being set in the display data RAM and mode setting latch in the LSI after data transfer, low is output from the READY terminal to inhibit the next data input. There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is low.
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D_0 to D_3 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.
SB	1	Input	MCU	High level input stops the LSI operations. 1. Stops oscillation and clock input. 2. Stops LCD driver. 3. Stops writing data into display RAM.
D_0–D_3	4	Input	MCU	Data input terminal from where 4-bit × 4 data are input.
V_{SS}	1	Power supply		Negative power supply.
V_3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V_3 is used as driving voltage.
COM_0	1	Output	LCD	LCD common (backplate) driving output.
SEG_0–SEG_{63}	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips applications. LCD driver timing circuit is reset by high input. LCD is off.
OSC_1 OSC_2	2	Input Output	External R	Attach external R to these terminals for oscillation. An external clock (100 kHz) can be input to OSC_1.

Note: Logic polarity is positive. 1 = high = active.

Display RAM

HD61602 Display RAM

The HD61602 has an internal display RAM shown in figure 1. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to 1 segment of the LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

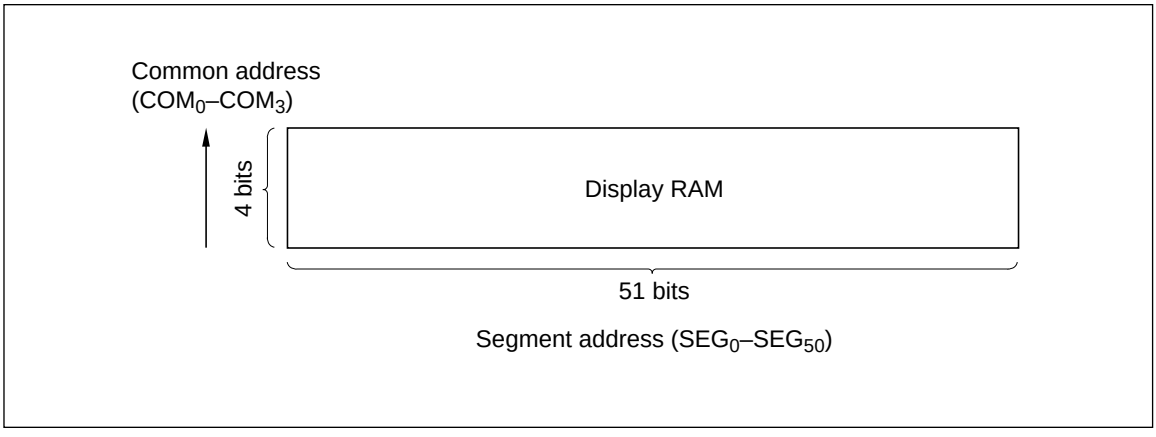


Figure 1 Display RAM

Reading Data from Display RAM: A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.

A common address corresponds to the output timing of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

1. Static drive

   In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 2).

2. 1/2 duty cycle drive

   In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 3).

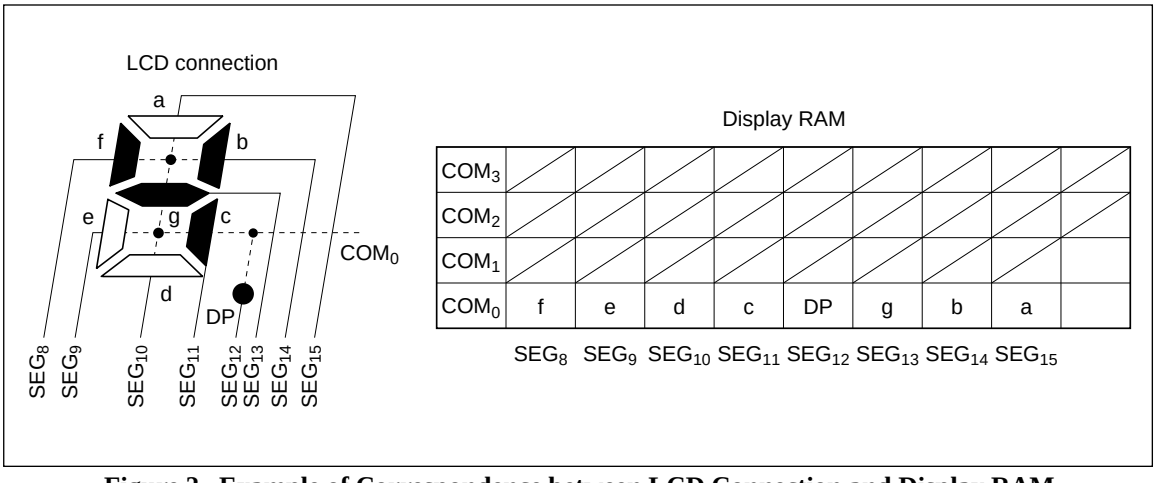


Figure 2 Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61602)

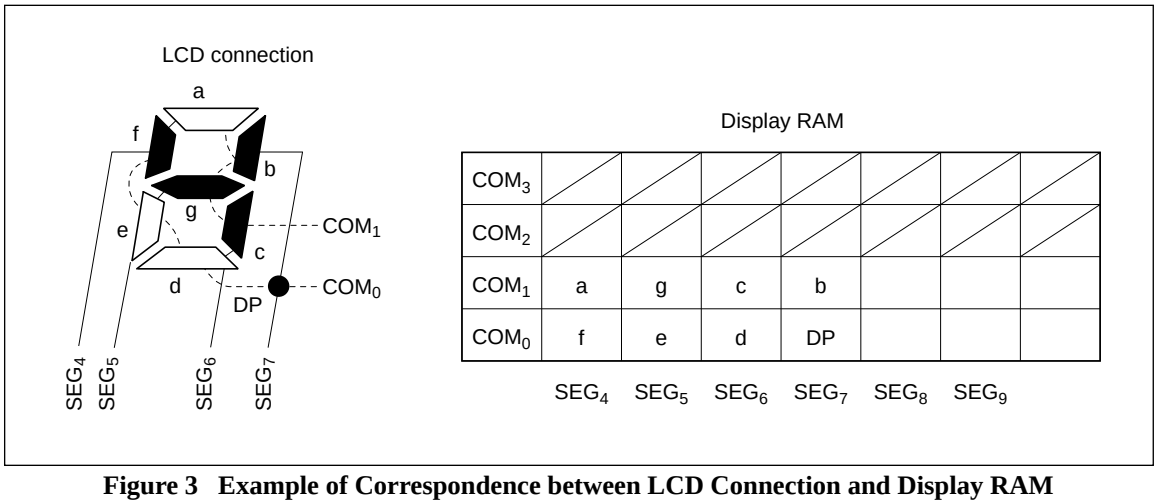


Figure 3 Example of Correspondence between LCD Connection and Display RAM (1/2 Duty Cycle, HD61602)

3. 1/3 duty cycle drive

   In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed.

   "Y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation to turn on/off the display of "Y" (figure 4).

4. 1/4 duty cycle drive

   In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed (figure 5).

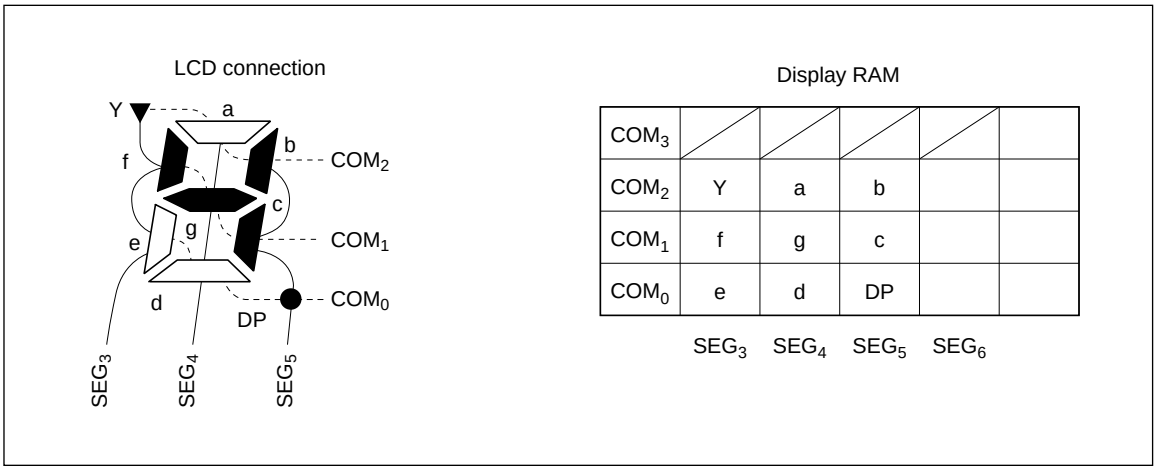


Figure 4 Example of Correspondence between LCD Connection and Display RAM (1/3 Duty Cycle, HD61602)

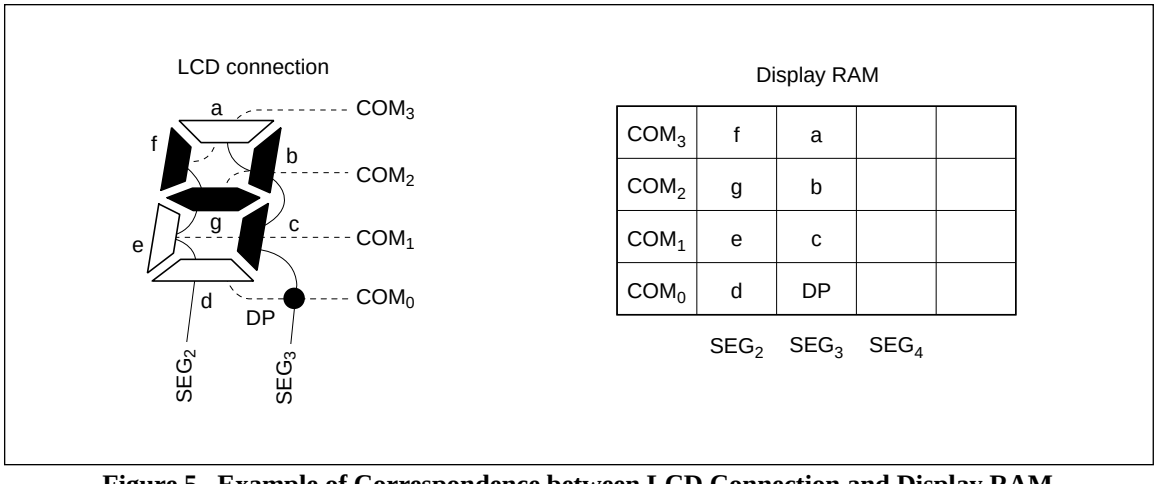


Figure 5 Example of Correspondence between LCD Connection and Display RAM (1/4 Duty Cycle, HD61602)

Writing Data into Display RAM: Data is written into the display RAM in the following five methods:

1. Bit manipulation

   Data is written into any bit of RAM on a bit basis.

2. Static display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

3. 1/2 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.

4. 1/3 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.

5. 1/4 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the driving methods as described in “Reading Data from Display RAM”.

8-bit data is written on a digit basis corresponding to the above duty cycle driving methods. The digits are allocated as shown figure 8 (allocation of digits). As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 6 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 7 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 for static, Ad12 for 1/2 duty cycle, or Ad25 for 1/4 duty cycle, display RAM does not have enough bits for the data.

Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

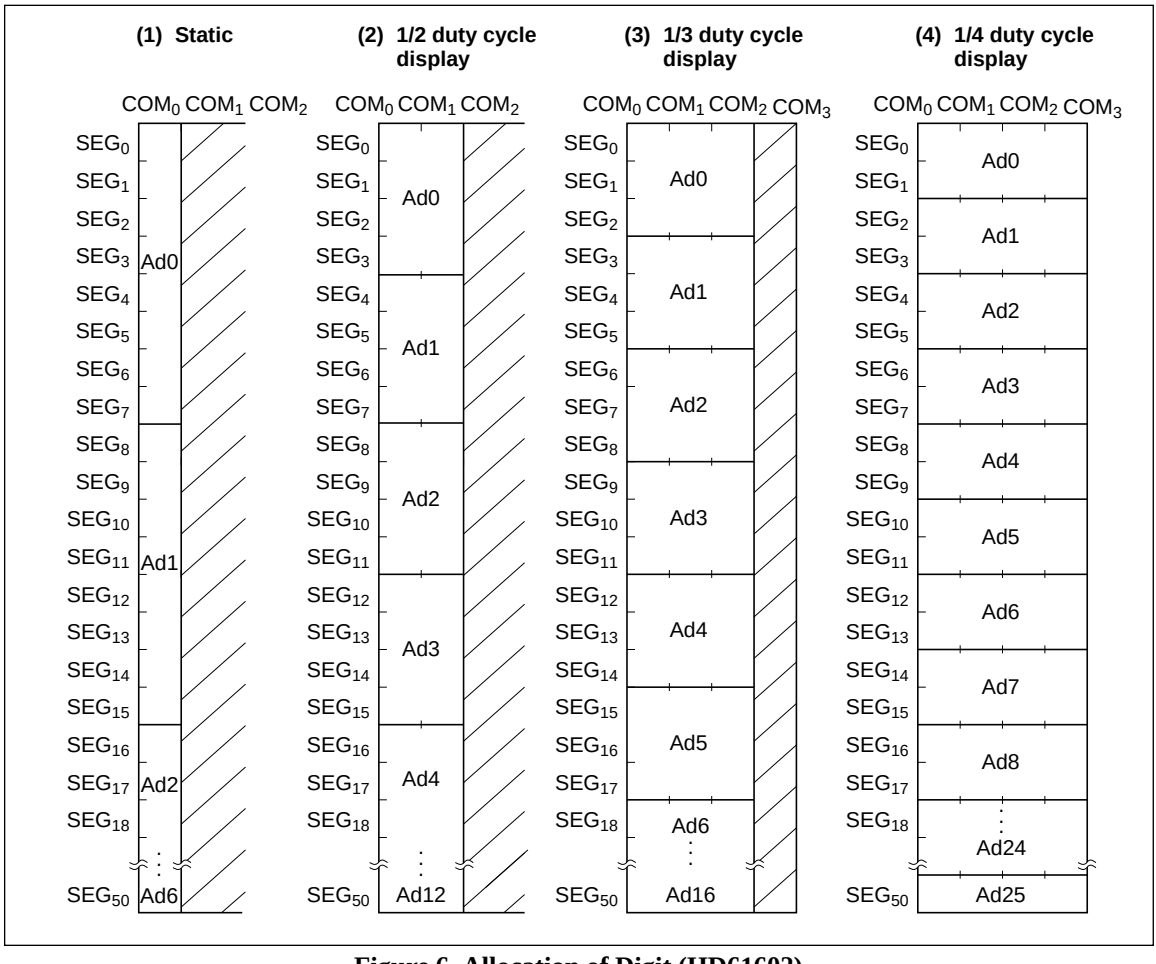


Figure 6 Allocation of Digit (HD61602)

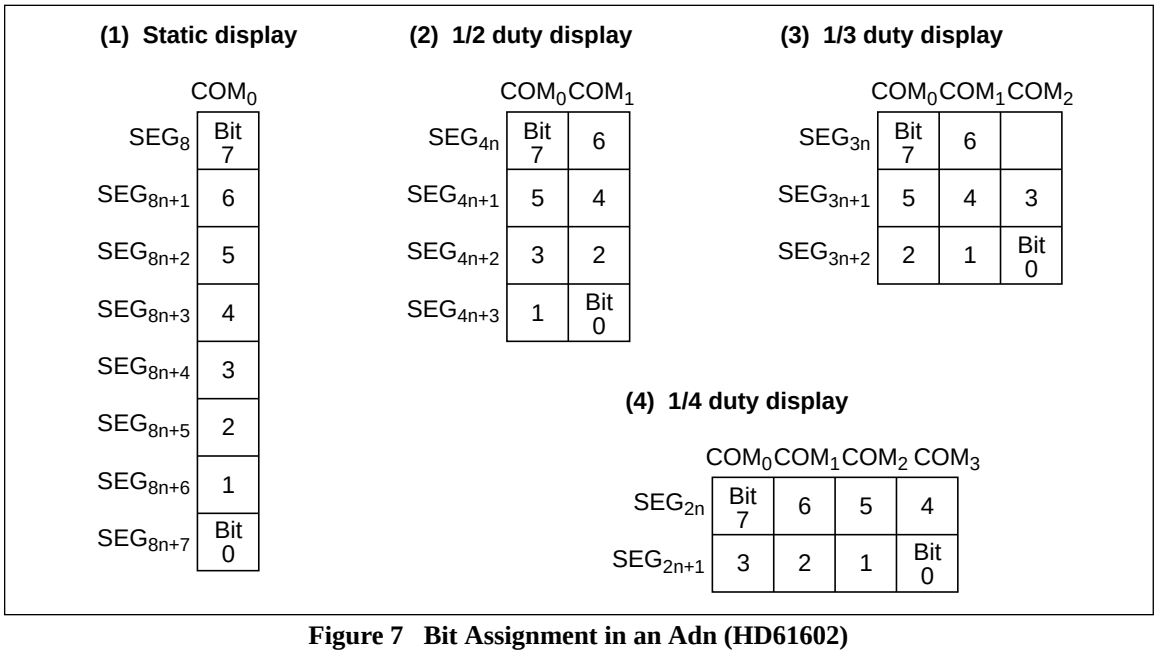


Figure 7 Bit Assignment in an Adn (HD61602)

HD61603 Display RAM

The HD61603 has an internal display RAM as shown in figure 8. Display data is stored in the RAM and output to the segment output terminal.

Reading Data from Display RAM: Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Figure 9 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

Writing Data into Display RAM: Data is written into the display RAM in the following two methods:

1. Bit manipulation

   Data is written into any bit of RAM on a bit basis.

2. Static display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

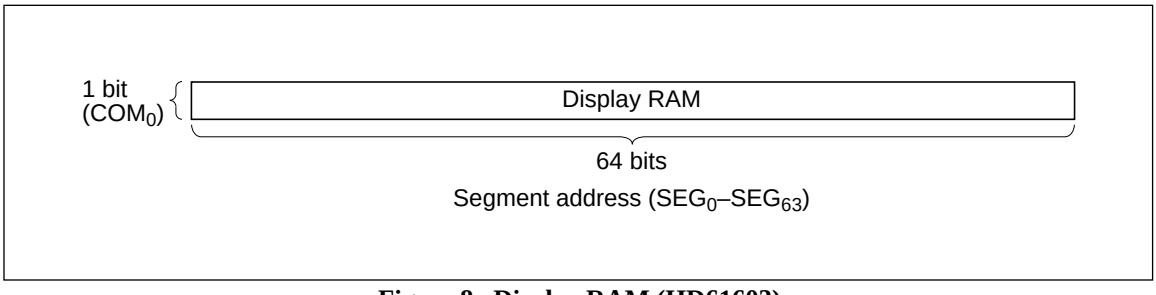


Figure 8 Display RAM (HD61603)

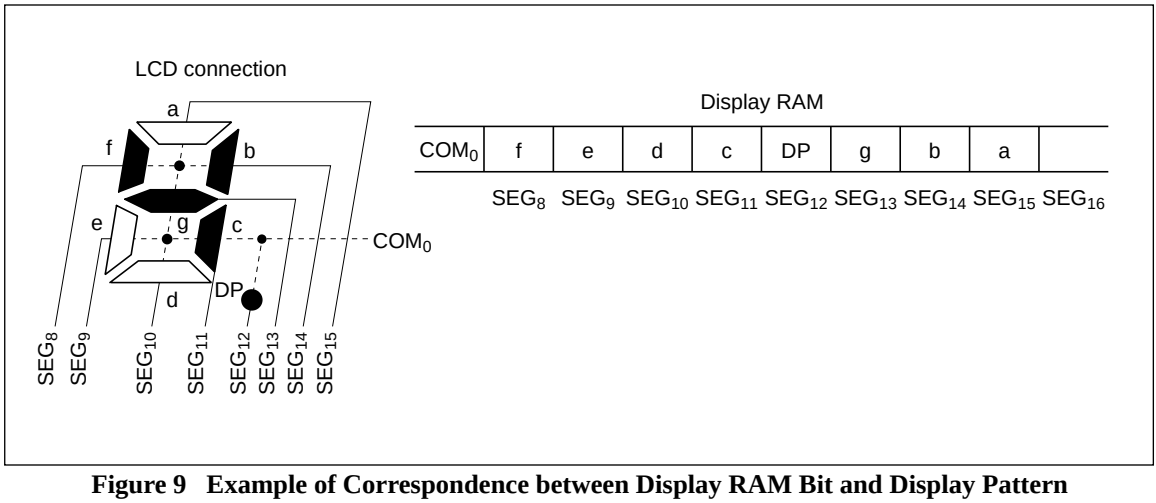


Figure 9 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 10. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 11 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

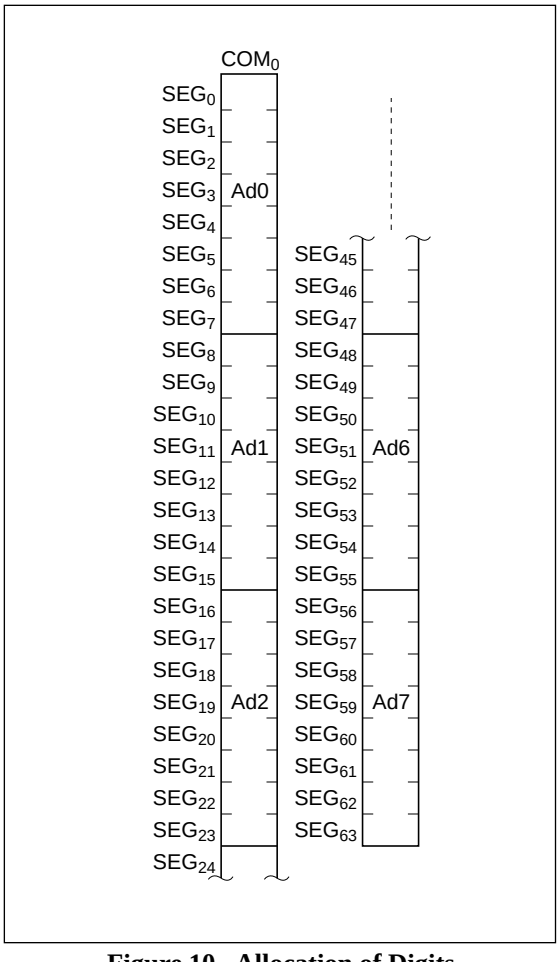


Figure 10 Allocation of Digits (HD61603)

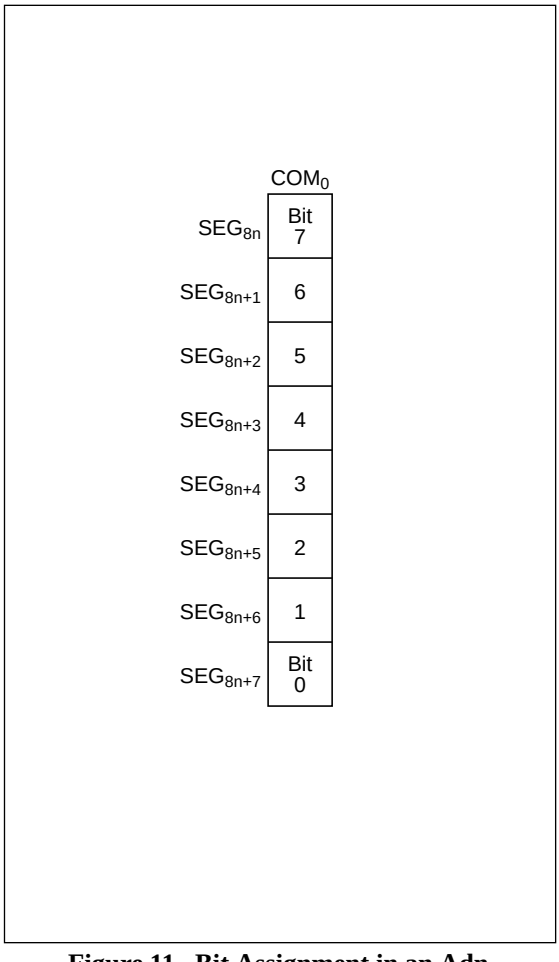


Figure 11 Bit Assignment in an Adn (HD61603)

Operating Modes

HD61602 Operating Modes

The HD61602 has the following operating modes:

1. LCD drive mode

   Determines the LCD driving method.

   a. Static drive mode
      LCD is driven statically.

   b. 1/2 duty cycle drive mode
      LCD is driven at 1/2 duty cycle and 1/2 bias.

   c. 1/3 duty cycle drive mode
      LCD is driven at 1/3 duty cycle and 1/3 bias.

   d. 1/4 duty cycle drive mode
      LCD is driven at 1/4 duty cycle and 1/3 bias.

2. Data display mode

   Determines how to write display data into the data RAM.

   a. Static display mode
      8-bit data is written into the display RAM according to the digit in static drive.

   b. 1/2 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.

   c. 1/3 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.

   d. 1/4 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/4 duty cycle drive.

3. READY output mode

   Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

   a. READY is mode always available (figure 12).

   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$ (figure 13).

4. LCD OFF mode

   In this mode, the HD61602 stops driving LCD and turns it off.

5. External driving voltage mode

   A mode for using external driving voltage (V_1, V_2, and V_3).

The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. Bit manipulation is independent of data display mode and can be used regardless of it.

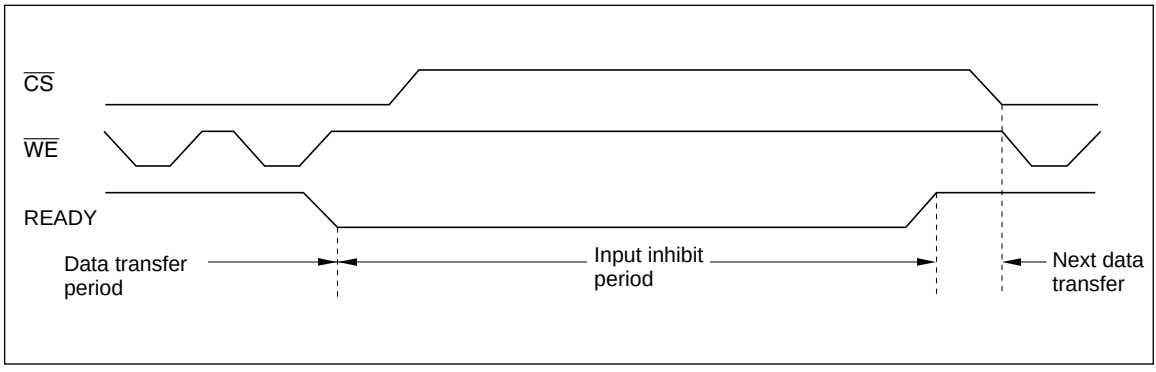


Figure 12 READY Output Timing (When It Is Always Available)

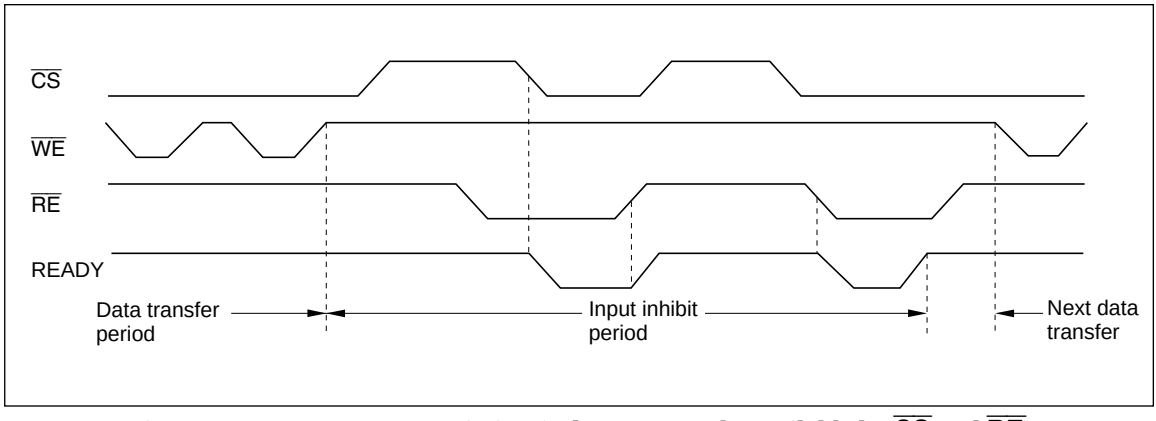


Figure 13 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

HD61603 Operating Modes

The HD61603 has the following modes:

1. READY output mode

   Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   a. READY is always available (figure 14).

   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

2. LCD OFF mode

   In this mode, the HD61603 stops driving the LCD and turns it off.

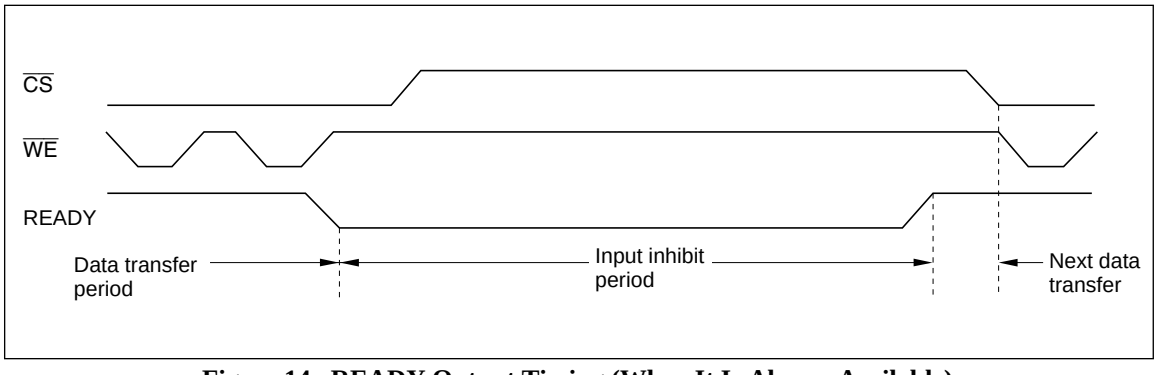


Figure 14 READY Output Timing (When It Is Always Available)

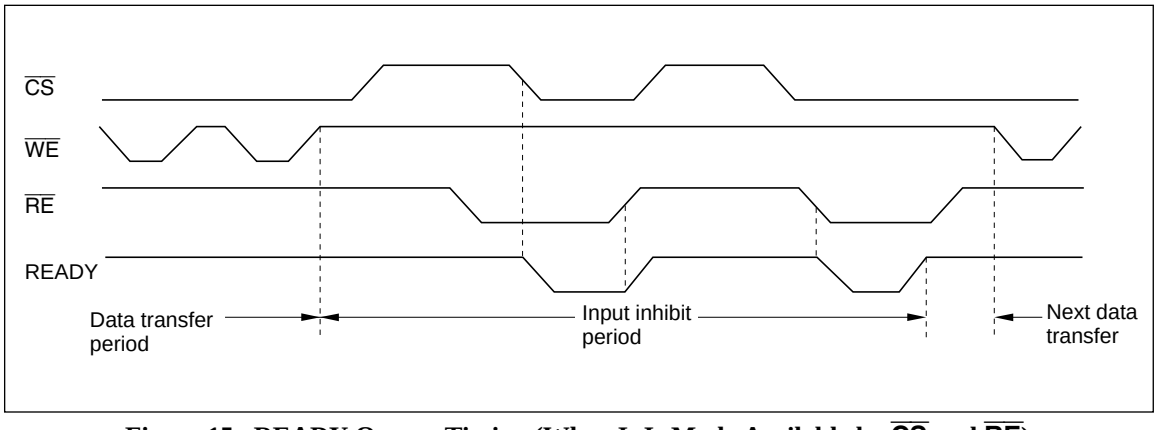


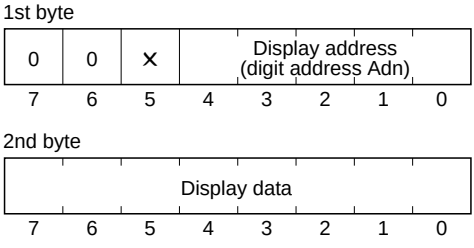
Figure 15 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

Input Data Formats

HD61602 Input Data Formats

Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (updates display on an 8-segment basis)



   a. Display address

      Digit address Adn in accordance with display mode

   b. Display data

      Pattern data that is written into the display RAM according to display mode and the address

2. Bit manipulation data (updates display on a segment basis)

   a. Display data

      Data that is written into 1 bit of the specified display RAM.

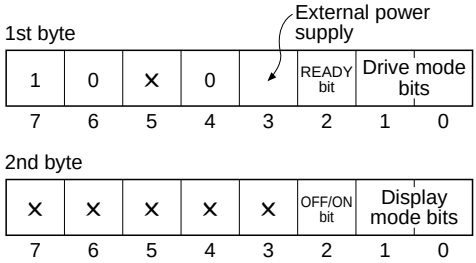
   b. COM address

      Common address of display RAM

   c. SEG address

      Segment address of display RAM

3. Mode setting data



   a. Display mode bits

      00: Static display mode

      01: 1/2 duty cycle display mode

      10: 1/3 duty cycle display mode

      11: 1/4 duty cycle display mode

   b. OFF/ON bit

      1: LCD off (set to 1 when SYNC is entered)

      0: LCD on

   c. Drive mode bits

      00: Static drive

      01: 1/2 duty cycle drive

      10: 1/3 duty cycle drive

      11: 1/4 duty cycle drive

   d. READY bit

      0: READY bus mode; READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered)

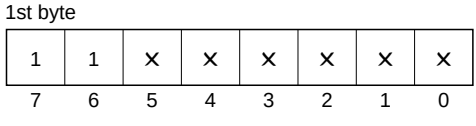
      1: READY port mode; READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

   e. External power supply bit

      0: Driving voltage is generated internally.

      1: Driving voltage is supplied externally. (Set to 1 when SYNC is entered.)

4. 1-byte instruction

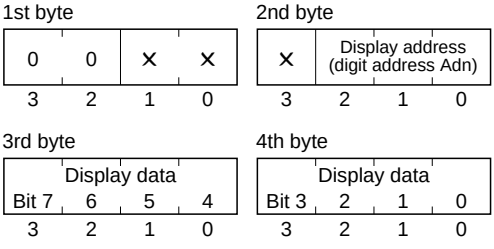


The first data (first byte) is ignored when bit 6 and bit 7 in the byte are 1.

HD61603 Input Data Formats

Input data is composed of 4 bits × 4. Input them as four 4-bit data after READY output changes from low to high or low pulse is entered into $\overline{RE}$ terminal.

1. Display data (updates display on an 8-segment basis)



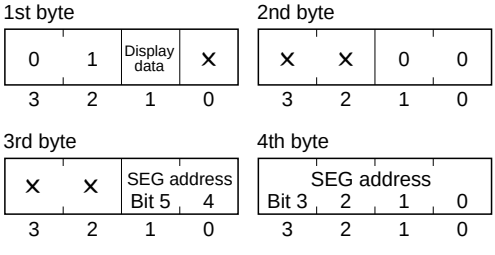
   a. Display address

      Digit address Adn shown in figure 10.

   b. Display data

      Pattern data that is written into the display RAM as shown in figure 11.

2. Bit manipulation data (updates display on a segment basis)



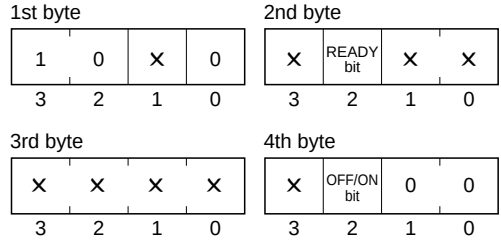
   a. Display data

      Data that is written into 1 bit of the specified display RAM.

   b. SEG address

      Segment address of display RAM (segment output)

3. Mode setting data



   a. OFF/ON bit

      1: LCD off (set to 1 when SYNC is entered.)

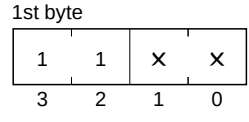
      0: LCD on

   b. READY bits

      0: READY bus mode; READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (reset to 0 when SYNC is entered.)

      1: READY port mode; READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$.

4. 1-byte instruction



The first data (4 bits) is ignored when bit 3 and 2 in the data are 1.

How to Input Data

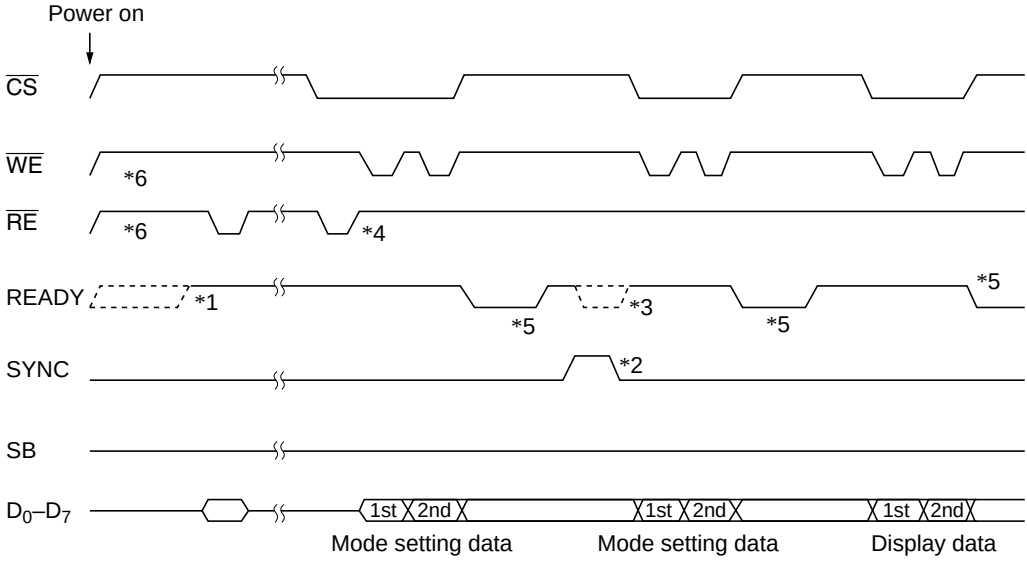
How to Input HD61602 Data

Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted, because the first 8-bit data is distinguished from the second one by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ inputs low (no display data changes).
2. Input 2 or more "1-byte instruction" data in which bit 7 and 6 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 16.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
2. High pulse should be applied to SYNC terminal when using two or more chips synchronously.
3. In the mode in which READY is always available, READY output is in definite while SYNC is high.
4. Reset the byte counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
7. It is not always necessary to follow this example.

Figure 16 Example of Data Transfer Sequence

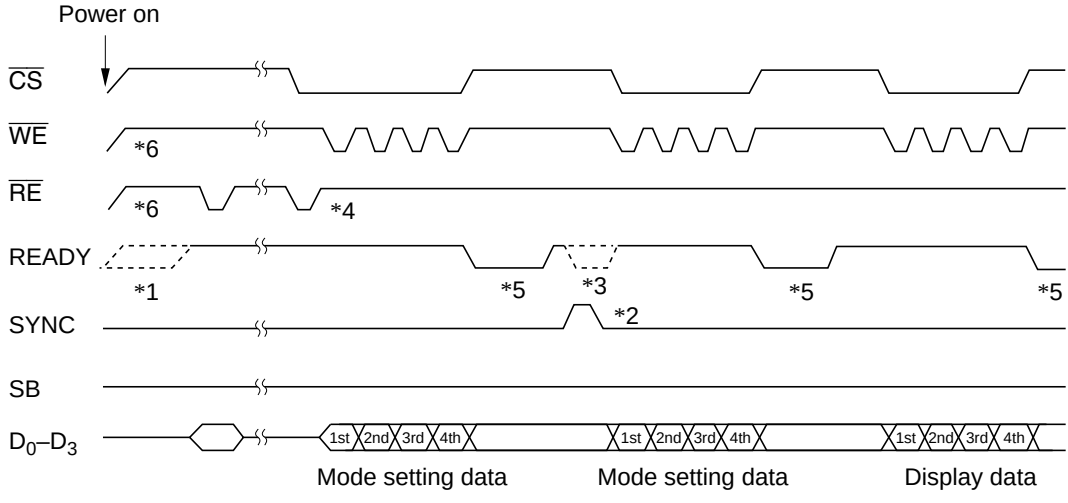
How to Input HD61603 Data

Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted, because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

If data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ low.
2. Input 4 or more "1-byte instruction" data (4-bit data) in which bit 3 and 2 are 1 (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D_0 to D_3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for an access, refer to the timing specifications and figure 17.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation start at power on (clock: OSC_2 clock).
2. High pulse should be applied to SYNC terminal when using two or more chips synchronously.
3. In the mode in which READY is always available, READY output is in definite while SYNC is high.
4. Reset the 4-bit data counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resister if $\overline{WE}$ or $\overline{RE}$ may be floating.
7. It is not always necessary to follow this example.

Figure 17 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled until the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes:

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 18 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61602 and HD61603.

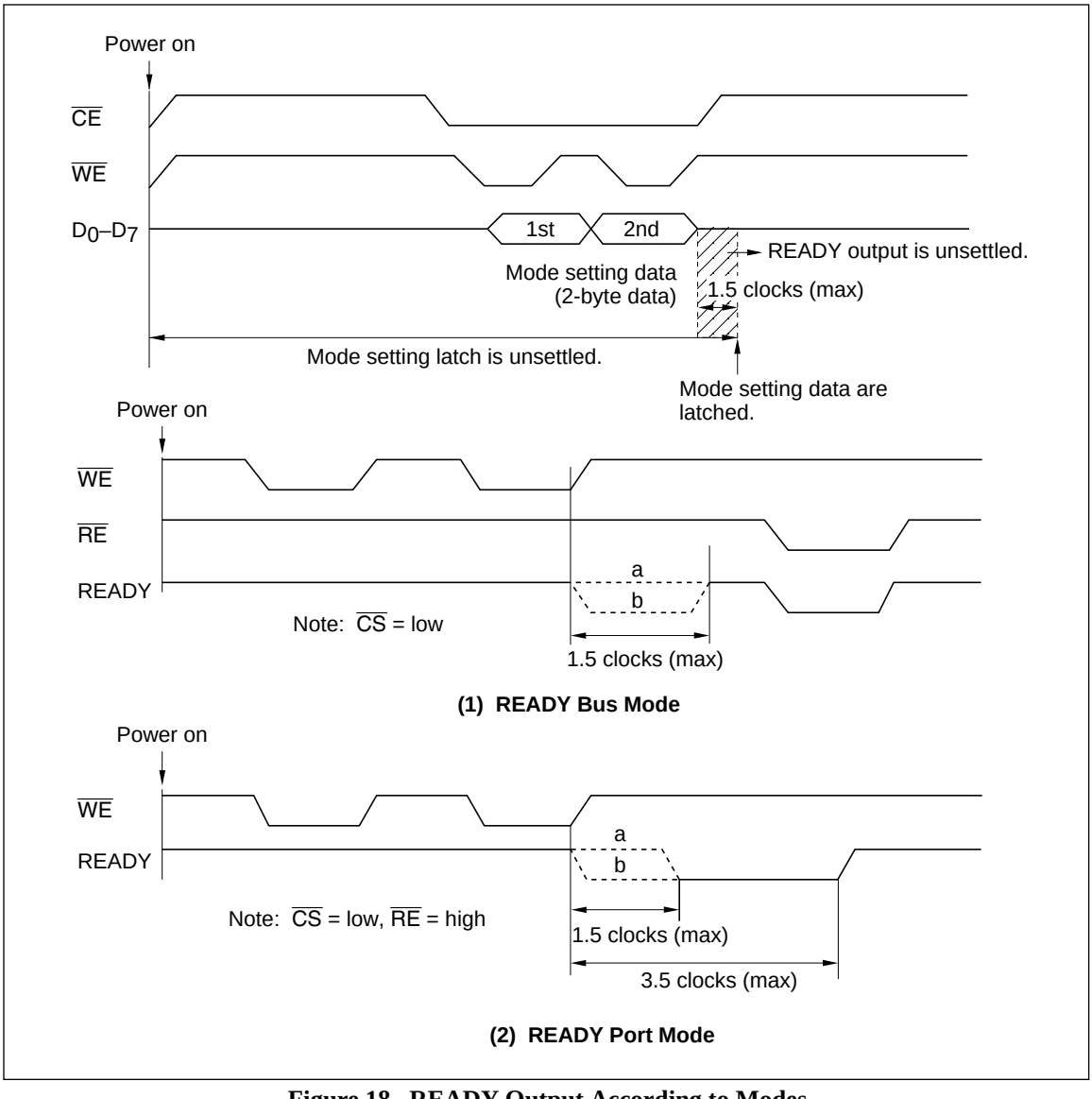


Figure 18 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multichip Operation

When an LCD is driven with two or more chips, the driving timing of the LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See 3. Mode Setting Data in “Input Data Formats”.) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, a high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise by-pass capacitor ($\geq$ 1 µF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61602)

What is LCD Voltage?

HD61602 drives liquid crystal display using four levels of voltages (figure 19); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61602.

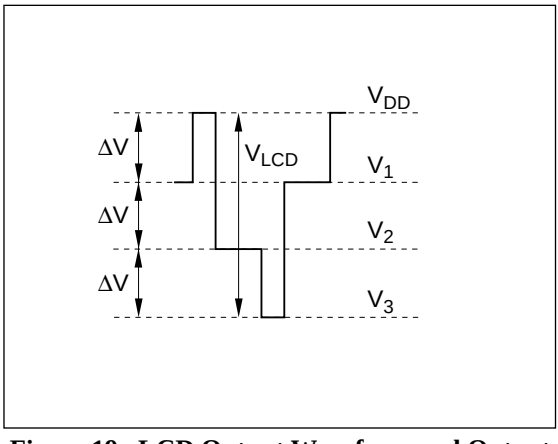


Figure 19 LCD Output Waveform and Output Levels

When Internal Drive Power Supply Is Used

When the internal drive power supply is used, attach C_1–C_4 for charge pump circuits and variable resistance R_1 for deciding display drive voltage to HD61602 as shown in figure 20.

Internal voltage is available by setting external voltage switching bits of mode setting data 0.

Figure 21 shows voltage characteristics between V_{DD} and V_{REF1}. Voltage is divided at R_1, and then input into V_{REF2}. Voltage between V_{DD} and V_{REF2} is equivalent to ΔV in figure 21, and so V_{LCD} can be changed by regulating the voltage.

V_{REF2} is usually regulated by variable resistance, but when replacing R_1 with two nonvariable resistances take V_{REF1} between max and min into consideration as shown in figure 21.

Internal drive power supply is generated by using capacitance, and so large current cannot flow. When large liquid crystal display panel is used, examine the external drive power supply.

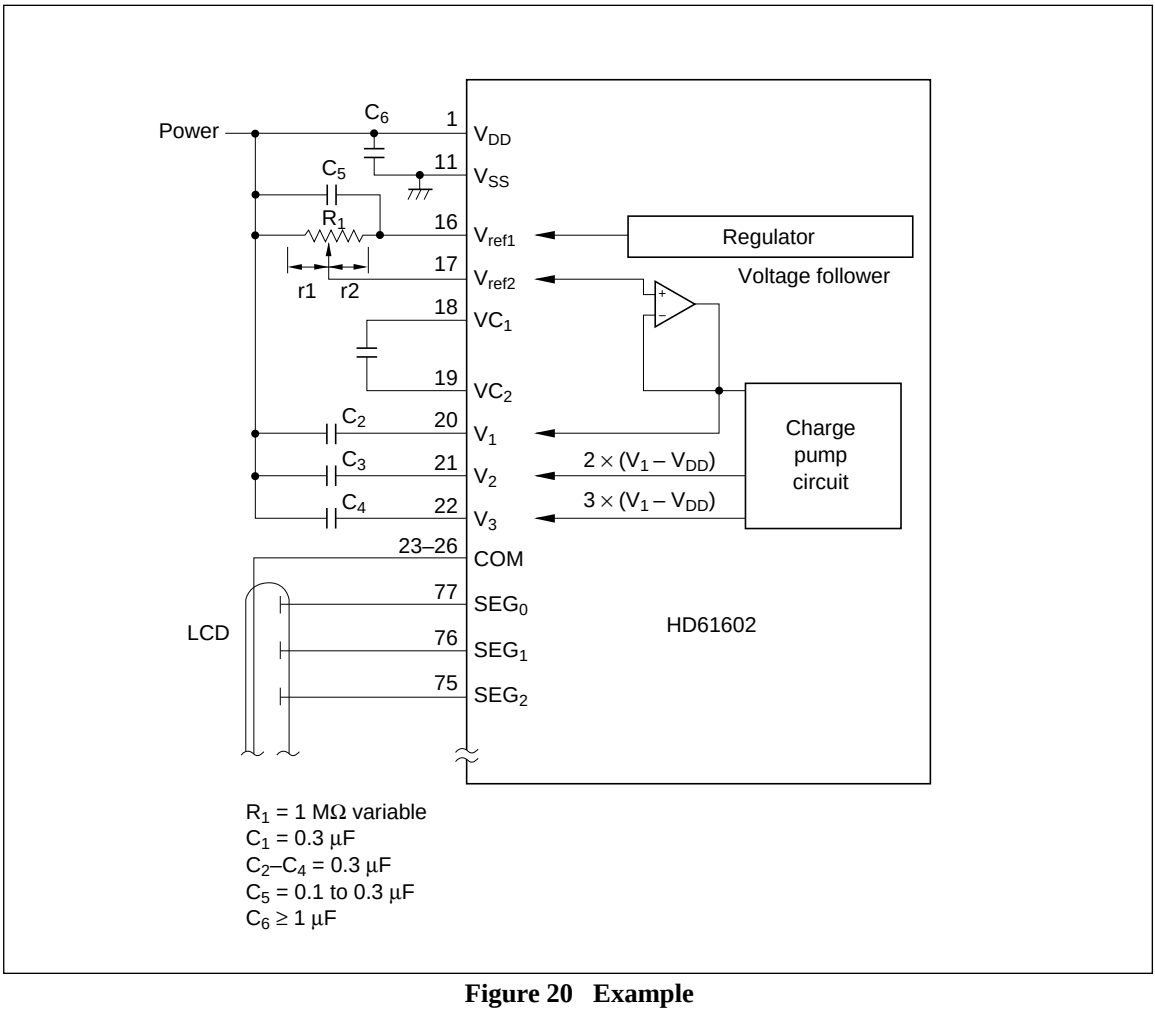


Figure 20 Example

When External Drive Power Supply Is Used

An external power supply can be used by setting external voltage switching bits of mode setting data to 1. When a large liquid crystal display panel is used, in multichip designs, which need accurate liquid crystal drive voltage, use the external power supply. See figure 22.

R_2–R_5 is connected in series between V_{DD} and V_{SS}, and by these resistance ratio each voltage of ΔV and V_{LCD} is generated and then supplied to V_1, V_2, and V_3. C_2–C_4 are smoothing capacitors.

When regulating brightness, change the resistance value by setting R_5 variable resistance.

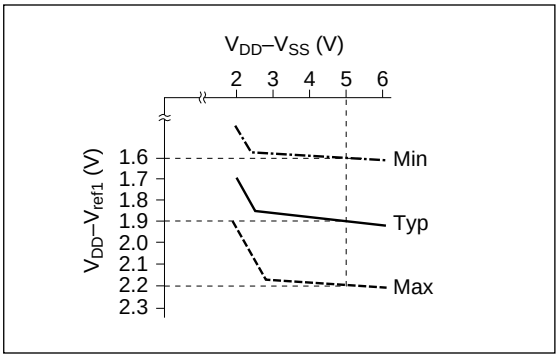
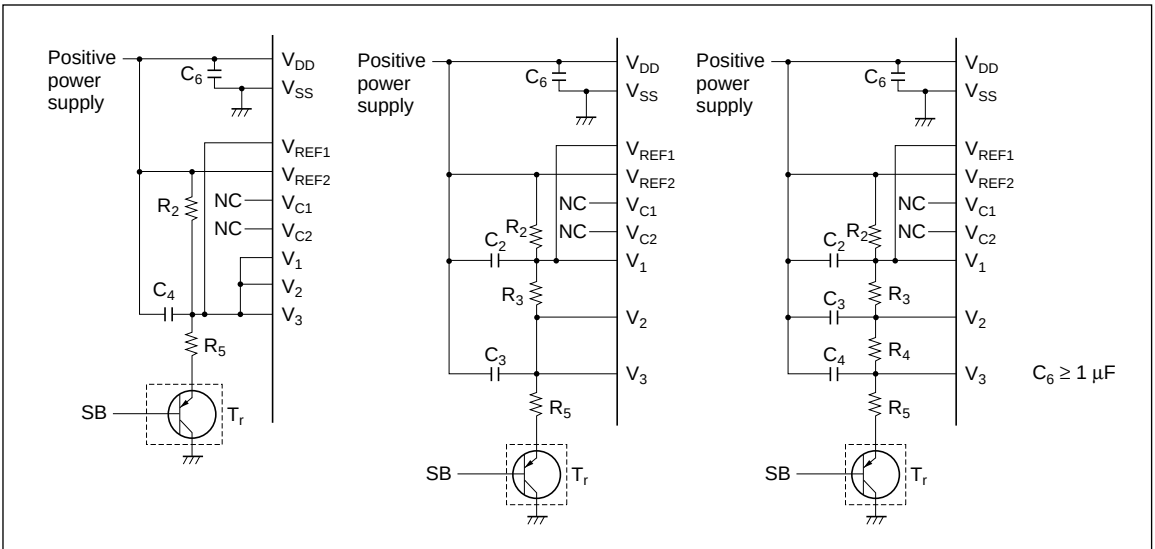


Figure 21 Voltage Characteristics between V_{DD} and V_{ref1}



Notes: 1. When standby mode is used, a transistor is required.
2. R_2–R_5 should be some kΩ–some tens of kΩ, and C_2–C_4 should be 0.1 µF–0.3 µF.

Figure 22 Example when External Drive Voltage Is Used

Liquid Crystal Display Drive Voltage (HD61603)

As shown in figure 23, apply LCD drive voltage from the external power supply.

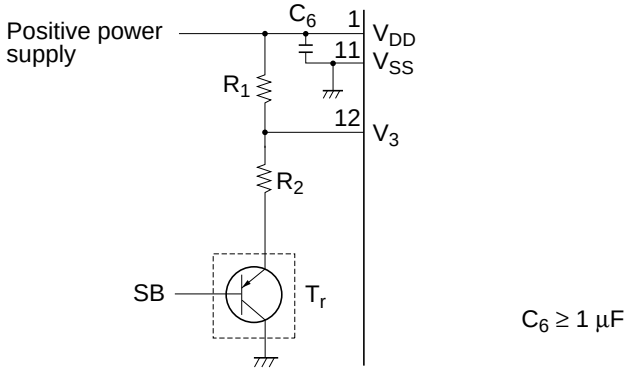
Oscillation Circuit

When Internal Oscillation Circuit Is Used

When the internal oscillation circuit is used, attach an external resister R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC_1 side shorter.)

When External Clock Is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC_1 can be used for the input pin. In this case, open pin OSC_2.



Note: When standby mode is used, a transistor is required.

Figure 23 Example of Drive Voltage Generator

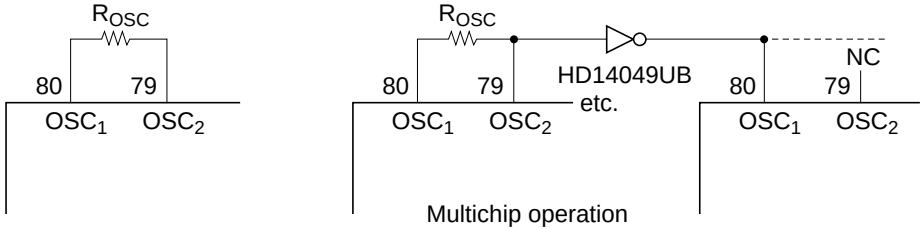


Figure 24 Example of Oscillation Circuit

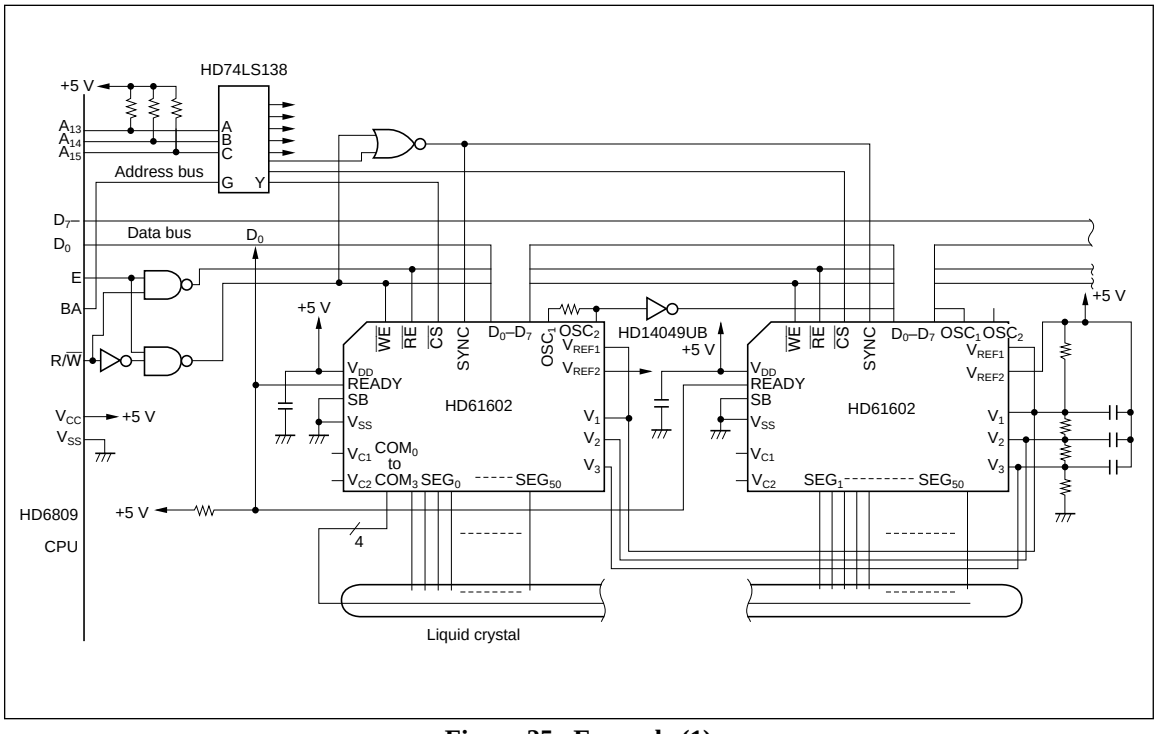


Figure 25 Example (1)

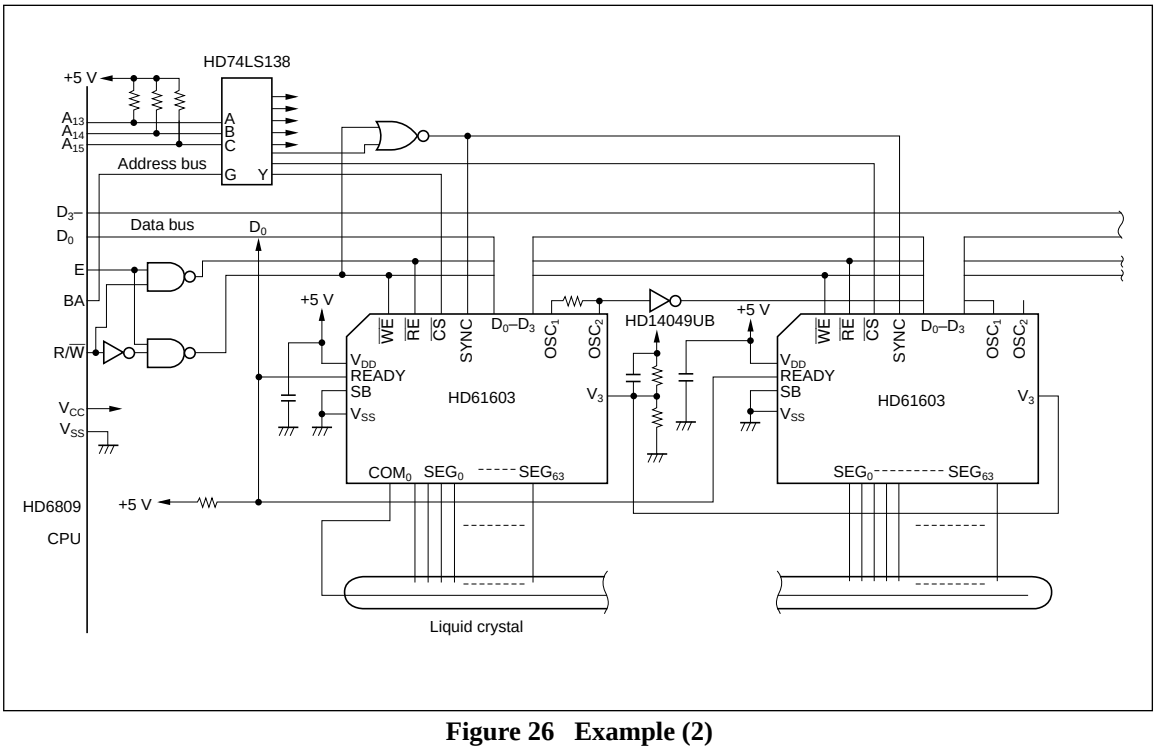


Figure 26 Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	–0.3 to +7.0	V
Terminal voltage*	V_T	–0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

* Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

		Limit			
Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	2.2	—	5.5	V
	V_1, V_2, V_3	0	—	V_{DD}	V
Terminal voltage*	V_T	0	—	V_{DD}	V
Operating temperature	T_{opr}	–20	—	75	°C

* Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics (1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC_1	V_{IH1}	0.8 V_{DD}	—	V_{DD}	V	
	Others	V_{IH2}	2.0	—	V_{DD}	V	
Input low voltage	OSC_1	V_{IL1}	0	—	0.2 V_{DD}	V	
	Others	V_{IL2}	0	—	0.8	V	
Output leakage current	READY	I_{OH}	—	—	5	µA	V0 = V_{DD}
Output low voltage	READY	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA
Input leakage current*1	Input terminal	I_{IL1}	–1.0	—	1.0	µA	V_{IN} = 0–V_{DD}
	V_1	I_{IL2}	–20	—	20	µA	V_{IN} = V_{DD}–V_3
	V_2, V_3	I_{IL3}	–5.0	—	5.0	µA	
LCD driver voltage drop	COM_0–COM_3	V_{d1}	—	—	0.3	V	±Id = 3 µA for each COM, V_3 = V_{DD}–3 V
	SEG_0–SEG_{50}	V_{d2}	—	—	0.6	V	±Id = 3 µA for each SEG, V_3 = V_{DD}–3 V
Power supply current		I_{DD}	—	—	100	µA	During display*2 R_{OSC} = 360 kΩ
		I_{DD}	—	—	5	µA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	—	—	0.4	V	V_{REF2} = V_{DD}–1 V, C_1–C_4 = 0.3 µF, RL = 3 MΩ

Notes: 1. V_1, V_2: apply only to HD61602.
2. Except the transfer operation of display data and bit data.

DC Characteristics (2) (V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Limit Typ	Limit Max	Unit	Test Condition
Input high voltage		V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
Input low voltage		V_{IL}	0	—	0.1 V_{DD}	V	
Output leakage current	READY	I_{OH}	—	—	5	µA	V_{IN} = V_{DD}
Output low voltage	READY	V_{OL}	—	—	0.1 V_{DD}	V	I_{OL} = 0.04 mA
Input leakage current*1	Input terminal	I_{IL1}	–1.0	0	1.0	µA	V_{IN} = 0–V_{DD}
	V_1	I_{IL2}	–20	—	20	µA	V_{IN} = V_{DD}–V_3
	V_2, V_3	I_{IL3}	–5.0	—	5.0	µA	
LCD driver voltage drop	COM_0–COM_3	V_{d1}	—	—	0.3	V	±Id = 3 µA for each COM, V_3 = V_{DD}–3 V
	SEG_0–SEG_{50}	V_{d2}	—	—	0.6	V	±Id = 3 µA for each SEG, V_3 = V_{DD}–3 V
Power supply current		I_{SS}	—	—	50	µA	During display*2 R_{OSC} = 330 kΩ
		I_{SS}	—	—	5	µA	At standby
Internal driving voltage drop	V_1, V_2, V_3	V_{TR}	—	—	0.4	V	V_{REF2} = V_{DD}–1 V, C_1–C_4 = 0.3 µF, RL = 3 MΩ, V_{DD} = 3–3.8 V

Notes: 1. V_1, V_2: apply only to HD61602.
2. Except the transfer operation of display data and bit data.

AC Characteristics (1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc} = 360 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing		t_S	400	—	—	ns	
		t_H	10	—	—	ns	
		t_{WH}	300	—	—	ns	
		t_{WL}	400	—	—	ns	
		t_{WR}	400	—	—	ns	
		t_{DL}	—	—	1.0	µs	Figure 31
		t_{EN}	400	—	—	ns	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	—	—	25	ns	

AC Characteristics (2) (V_{SS} = 0 V, V_{DD} = 2.2 to 3.8 V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC_2	f_{osc}	70	100	130	kHz	R_{osc} = 330 kΩ
External clock frequency	OSC_1	f_{osc}	70	100	130	kHz	
External clock duty	OSC_1	Duty	40	50	60	%	
I/O signal timing (V_{DD} = 3.0–3.8 V)		t_S	1.5	—	—	µs	
		t_H	1.0	—	—	µs	
		t_{WH}	1.5	—	—	µs	
		t_{WL}	1.5	—	—	µs	
		t_{DL}	—	—	2.0	µs	Figure 32
		t_{WR}	1.5	—	—	µs	
		t_{EN}	2.0	—	—	µs	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	—	—	25	ns	

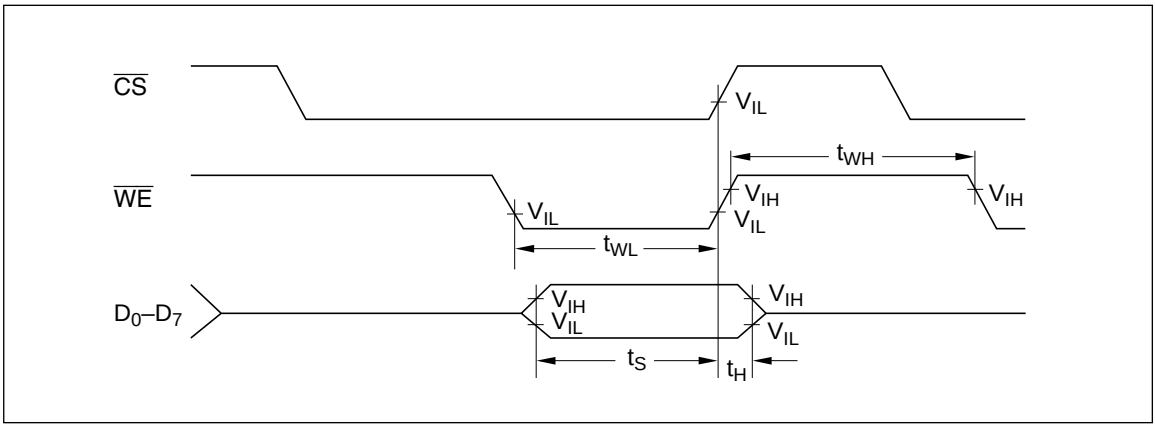


Figure 27 Write Timing ($\overline{RE}$ Is Fixed at High Level, and SYNC at Low Level)

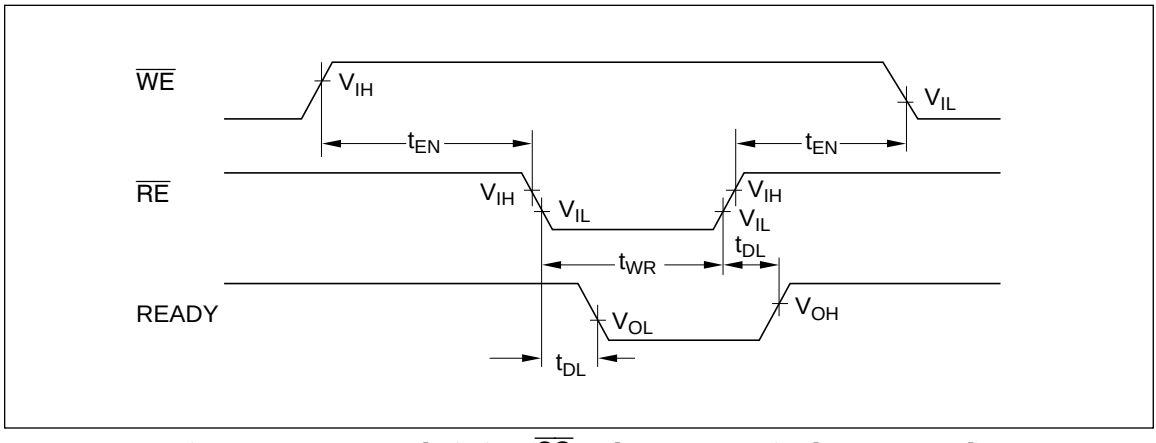


Figure 28 Reset/Read Timing ($\overline{CS}$ and SYNC Are Fixed at Low Level)

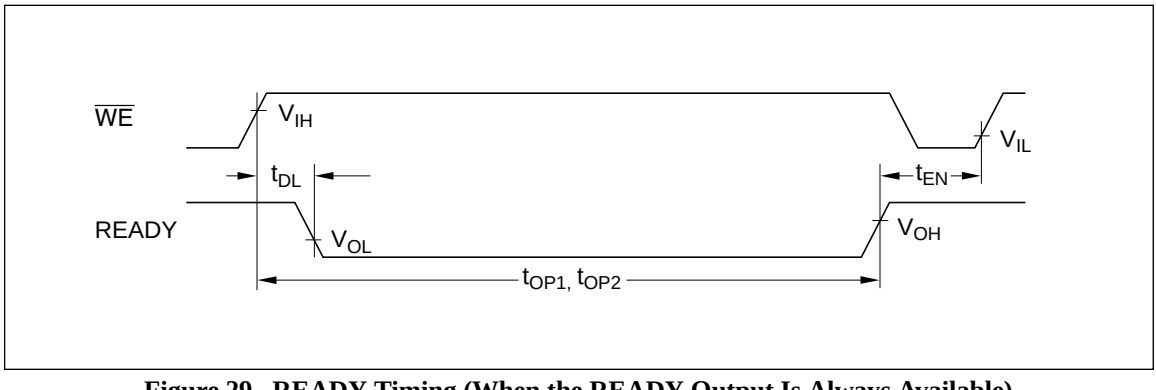


Figure 29 READY Timing (When the READY Output Is Always Available)

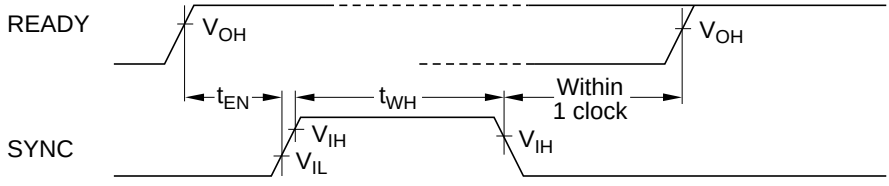


Figure 30 SYNC Timing

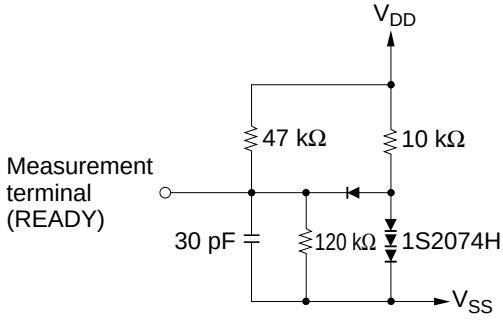


Figure 31 Bus Timing Load Circuit (LS-TTL Load)

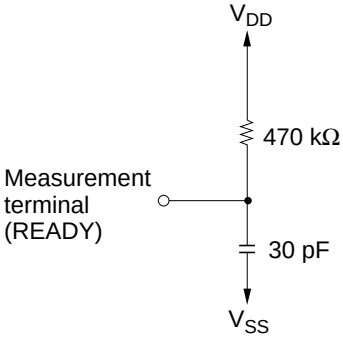


Figure 32 Bus Timing Load Circuit (CMOS Load)

HD61604/HD61605

(Segment Type LCD Driver)

HITACHI

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors such as the HMCS6800 series.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal display drive method.

The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  - — Can drive from a battery power supply (100 µA max. on 5 V)
  - — Standby input enables standby operation at lower current consumption (5 µA max. on 5 V)

Ordering Information

Type No.	Package
HD61604R	80-pin plastic QFP (FP-80)
HD61605R	

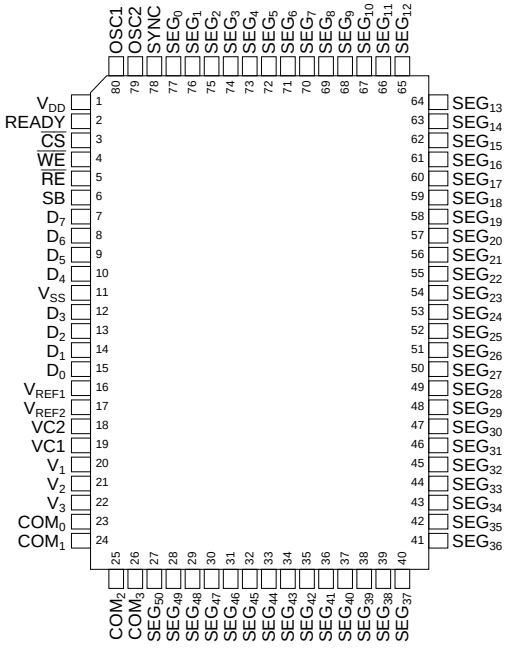
Versatile Segment Driving Capacity

Type No.	Driving Method		Display Segments	Example of Use	Frame Freq (Hz) at f_{OSC} = 100 kHz
HD61604R	Static		51	8 segments × 6 digits + 3 marks	98
	1/2 bias	1/2 duty cycle	102	8 segments × 12 digits + 6 marks	195
	1/3 bias	1/3 duty cycle	153	9 segments × 17 digits	521
		1/4 duty cycle	204	8 segments × 25 digits + 4 marks	781
HD61605R	Static		64	8 segments × 8 digits	98

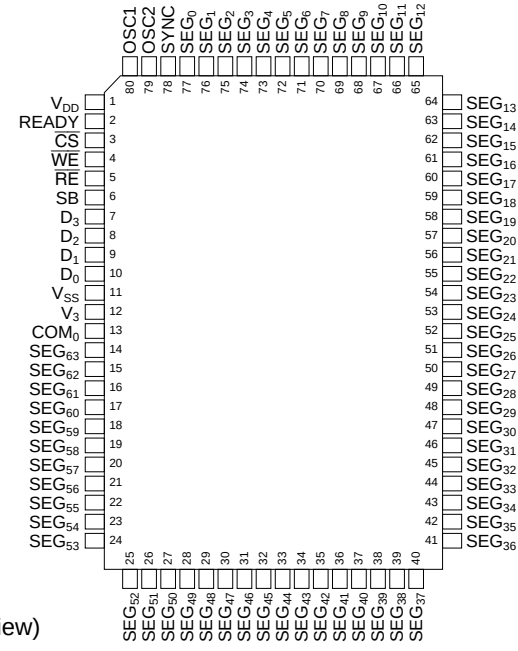
Hitachi semiconductor

Pin Arrangement

HD61604R



HD61605R



(Top view)

Block Diagram

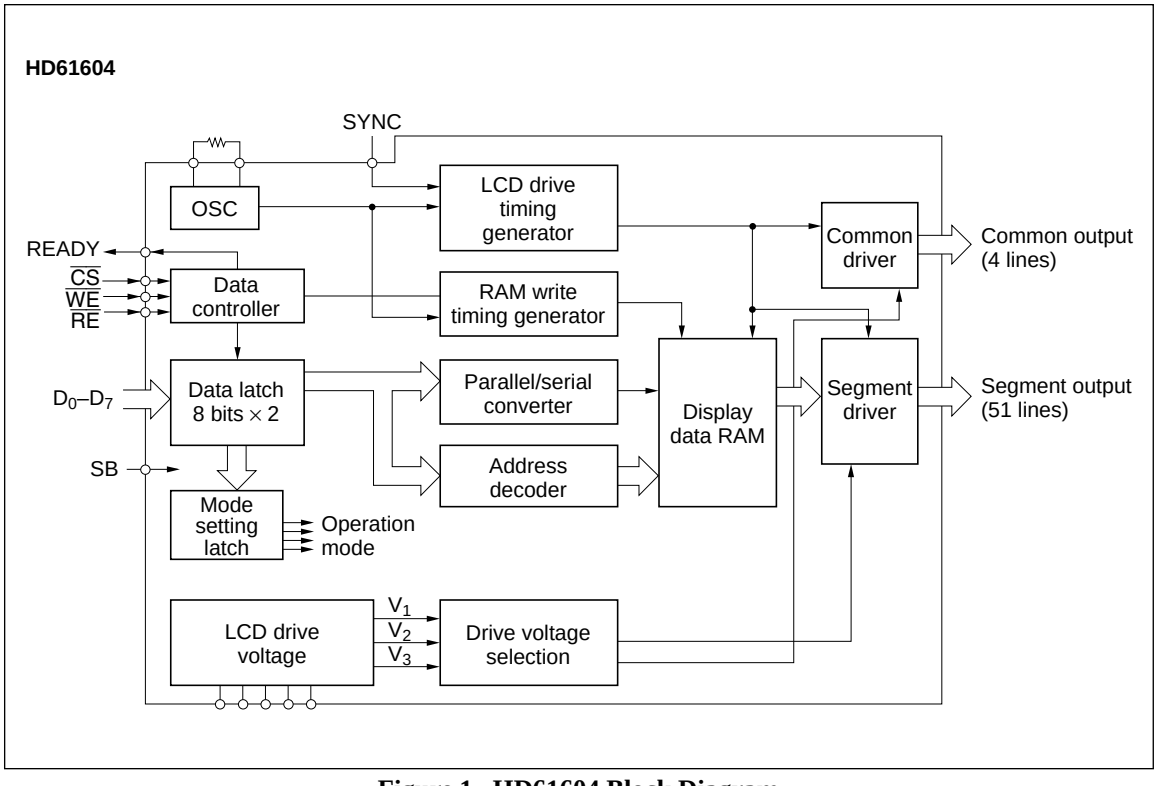


Figure 1 HD61604 Block Diagram

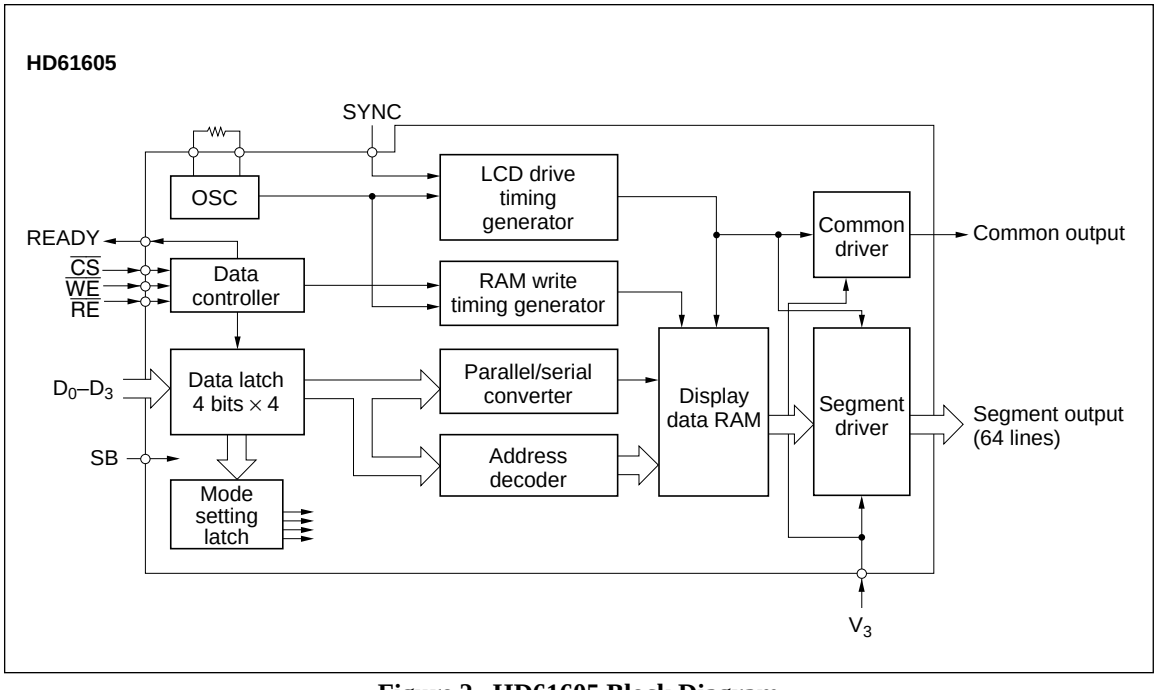


Figure 2 HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_7 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D_0–D_7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chip applications. LCD drive timing generator is reset by high input. LCD is off.

COM_0–COM_3 (Common): LCD common (backplate) drive output.

SEG_0–SEG_{50} (Segment): LCD segment drive output.

V_1, V_2, V_3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_{C1}, V_{C2}: Do not connect any wire.

V_{REF1}: Connect this pin to V1 pin.

V_{REF2}: Hold at V_{DD} level.

V_{DD}: Positive power supply.

V_{SS}: Negative power supply.

HD61605 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_3 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operation.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D_0–D_3: Data input pin from which 4-bit × 4-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0 (Common): LCD common (backplate) drive output.

SEG_0–SEG_{63} (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_3 (LCD Voltage): Power supply input for LCD drive.

Voltage between V_{DD} and V_3 is used as drive voltage.

V_{SS}: Negative power supply.

V_{DD}: Positive power supply.

Table 1 HD61604 Pin Description

Pin Name	No. of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0–D_7	8	Input	MCU
SYNC	1	Input	MCU
COM_0–COM_3	4	Output	LCD
SEG_0–SEG_{50}	51	Output	LCD
V_1, V_2, V_3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
V_{C1}, V_{C2}	2	Output	
V_{REF1}	1	Input	V_1
V_{REF2}	1	Input	V_{DD}
V_{DD}	1	Power supply	
V_{SS}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2 HD61605 Pin Description

Pin Name	No. of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D_0–D_3	4	Input	MCU
SYNC	1	Input	MCU
COM_0	1	Output	LCD
SEG_0–SEG_{63}	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V_3	1	Input	Power supply
V_{SS}	1	Power supply	
V_{DD}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

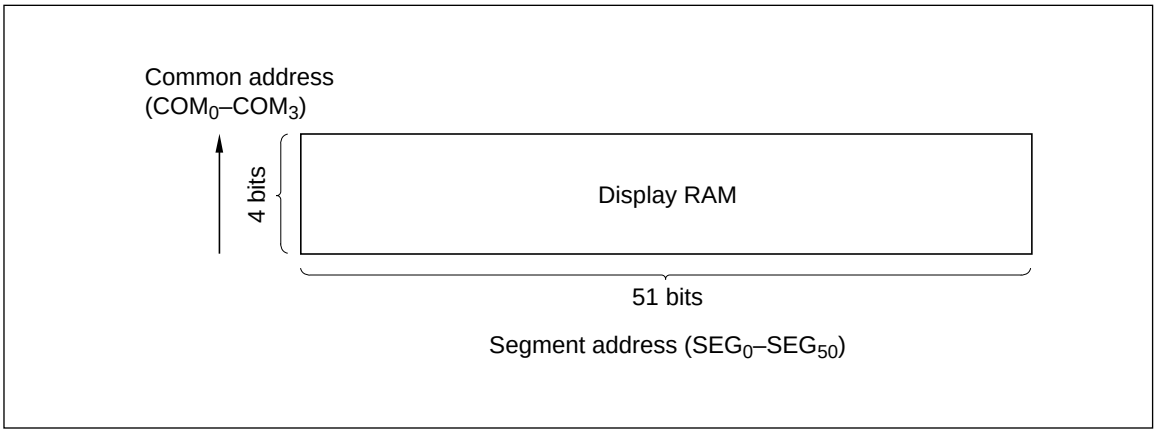


Figure 3 Display RAM (HD61604)

Reading Data from HD61604 Display RAM: A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timing of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

1. Static drive

   In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 4).

2. 1/2 duty cycle drive

   In the 1/2 duty cycle drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 5).

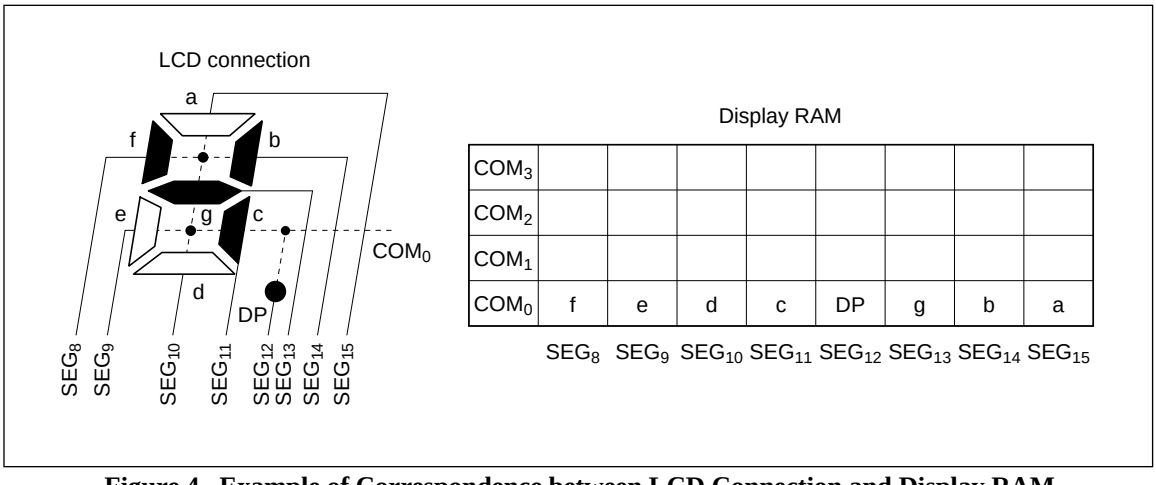


Figure 4 Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

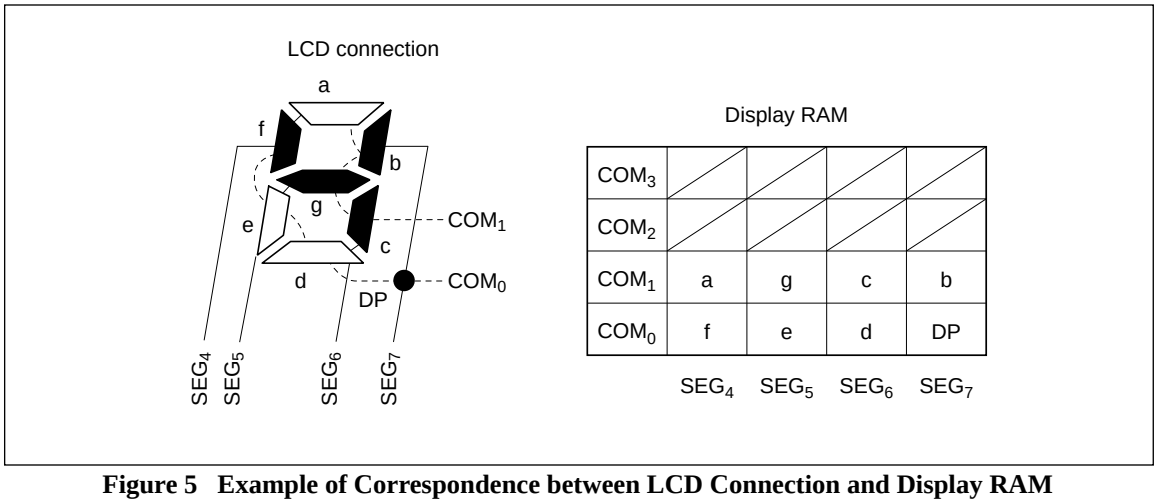


Figure 5 Example of Correspondence between LCD Connection and Display RAM (1/2 Duty Cycle, HD61604)

3. 1/3 duty cycle drive

   In the 1/3 duty cycle drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed. "y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "y" cycle (figure 6).

4. 1/4 duty cycle drive

   In the 1/4 duty cycle drive, all the columns of COM_0 to COM_3 are displayed (figure 7).

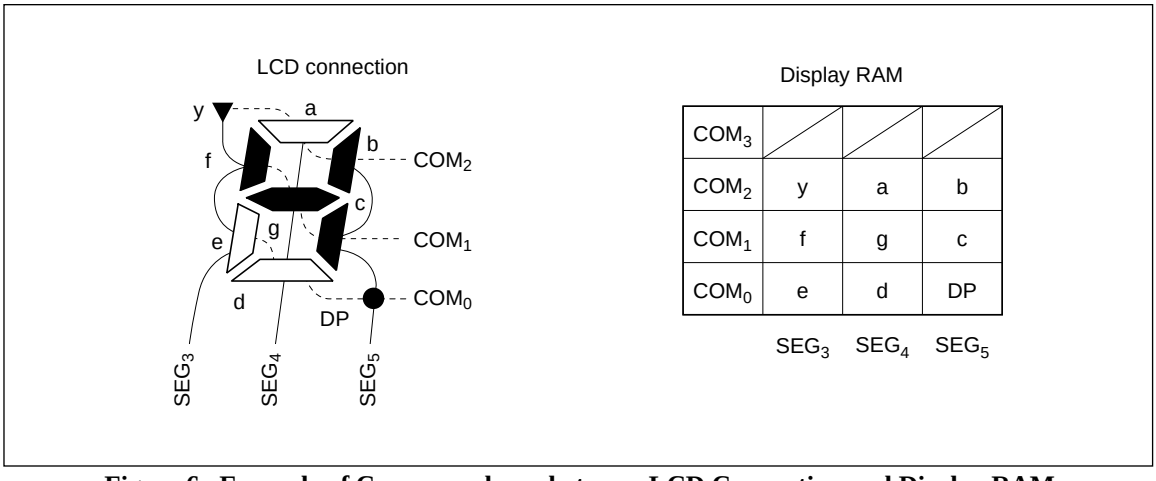


Figure 6 Example of Correspondence between LCD Connection and Display RAM (1/3 Duty Cycle, HD61604)

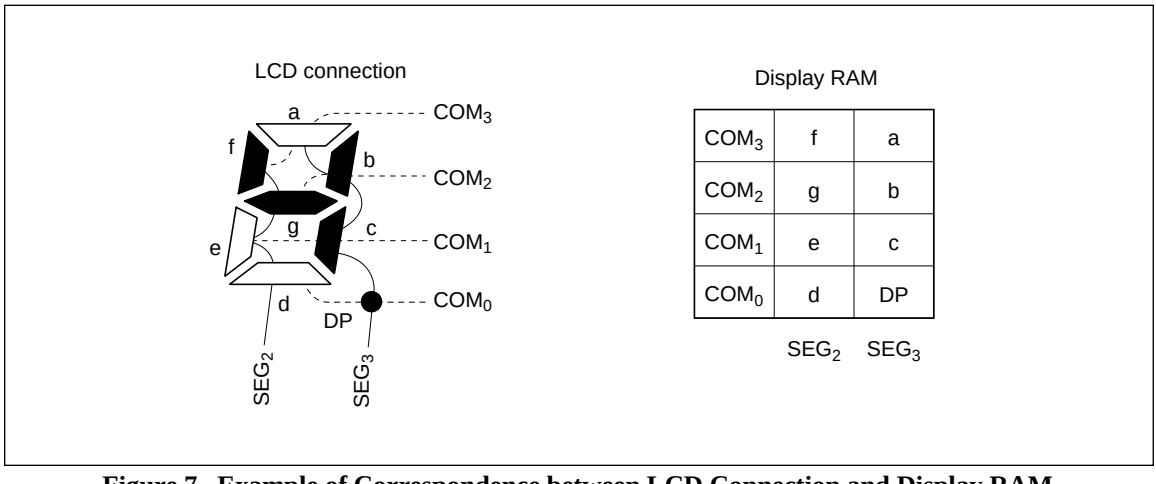


Figure 7 Example of Correspondence between LCD Connection and Display RAM (1/4 Duty Cycle, HD61604)

Writing Data into HD61604 Display RAM: Data is written into the display RAM in the following five methods:

1. Bit manipulation

   Data is written into any bit of RAM on a bit basis.

2. Static display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

3. 1/2 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.

4. 1/3 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.

5. 1/4 duty cycle display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of “Reading Data from Display RAM”.

8-bit data is written on a digit basis corresponding to the above duty cycle driving methods. The digits are allocated as shown in figure 8. As the data can be transferred on a digit basis from a micro-processor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty cycle, or Ad25 for 1/4 duty cycle, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

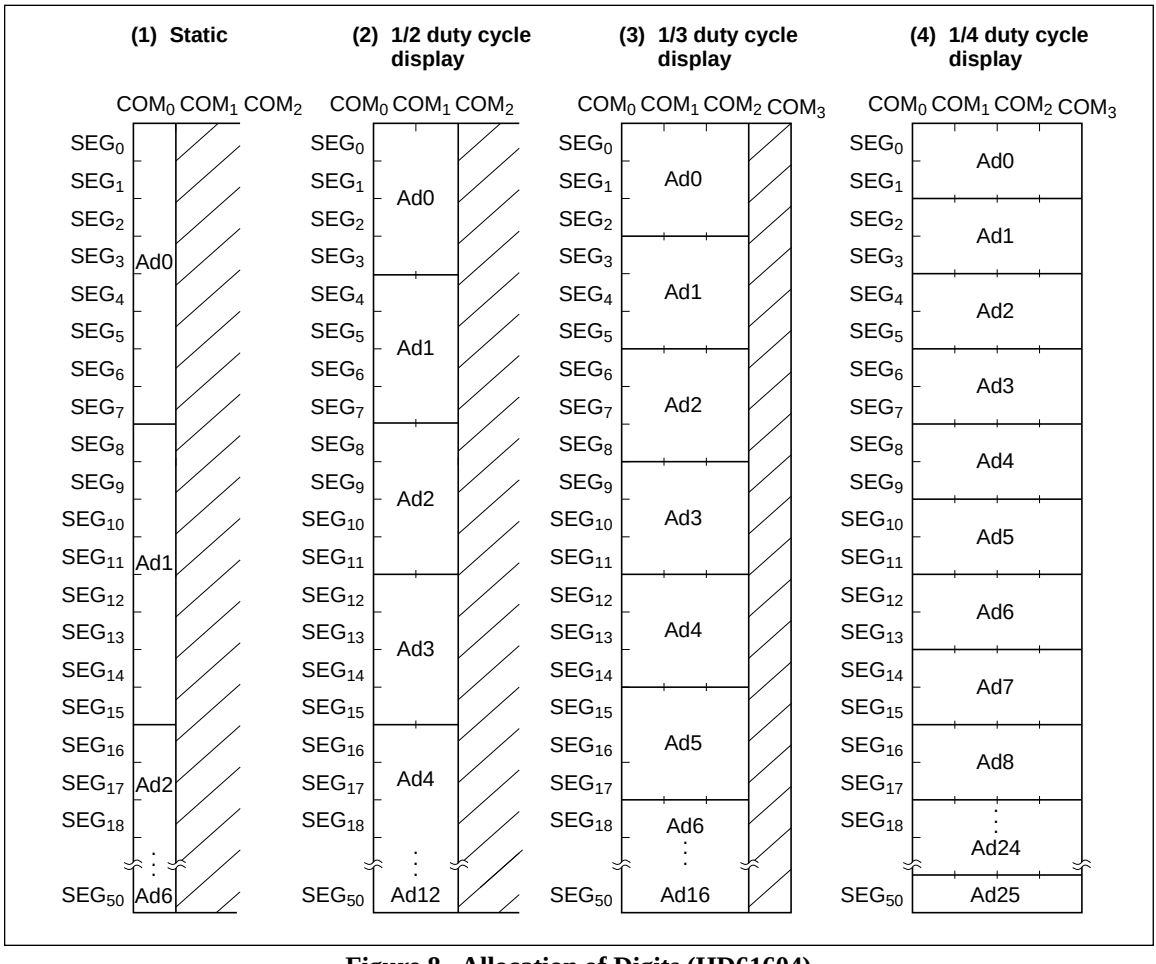


Figure 8 Allocation of Digits (HD61604)

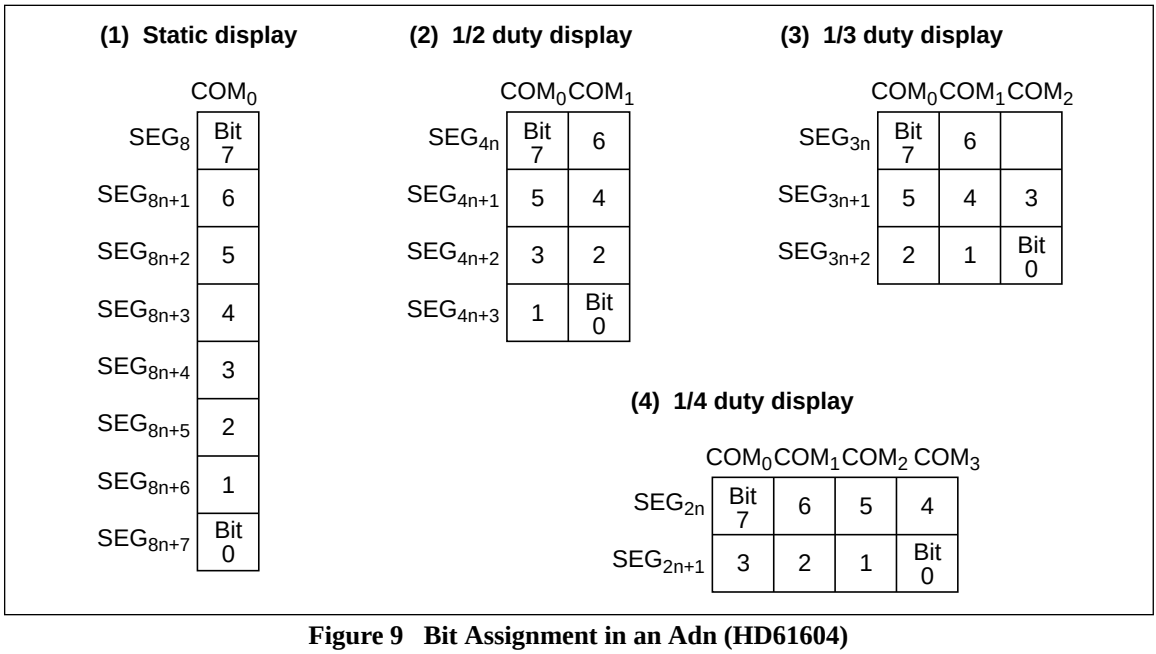


Figure 9 Bit Assignment in an Adn (HD61604)

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in figure 10. Display data is stored in the RAM and output to the segment output pin.

Reading Data from HD61605 Display RAM: Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM.

Writing Data into HD61605 Display RAM: Data is written into the display RAM in the following two methods:

1. Bit manipulation

   Data is written into any bit of RAM on a bit basis.

2. Static display mode

   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

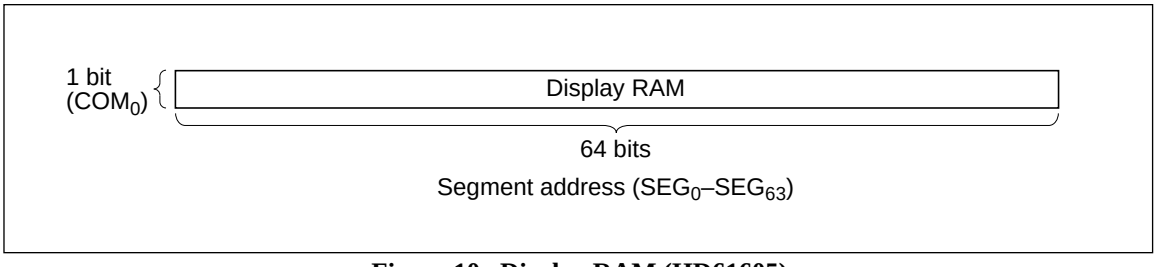


Figure 10 Display RAM (HD61605)

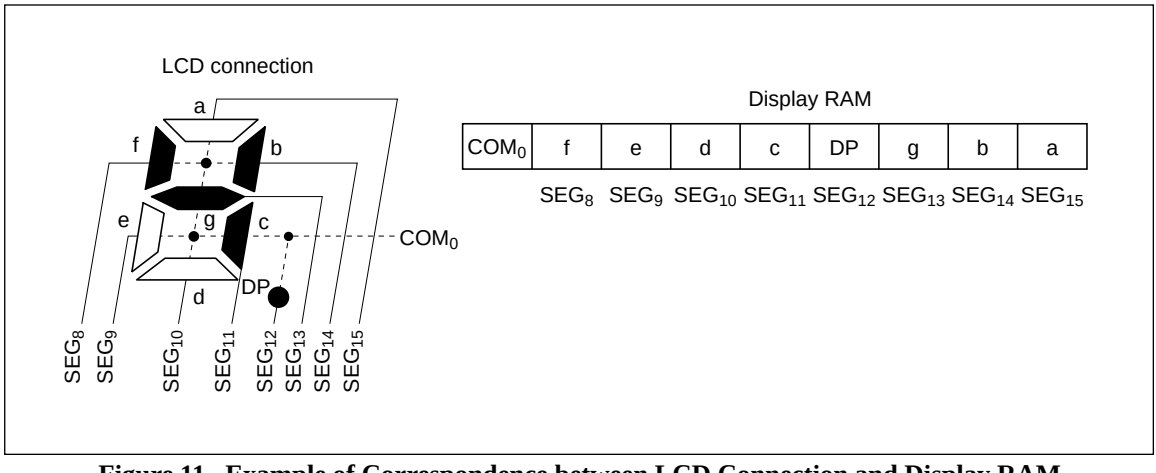


Figure 11 Example of Correspondence between LCD Connection and Display RAM (HD61605)

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

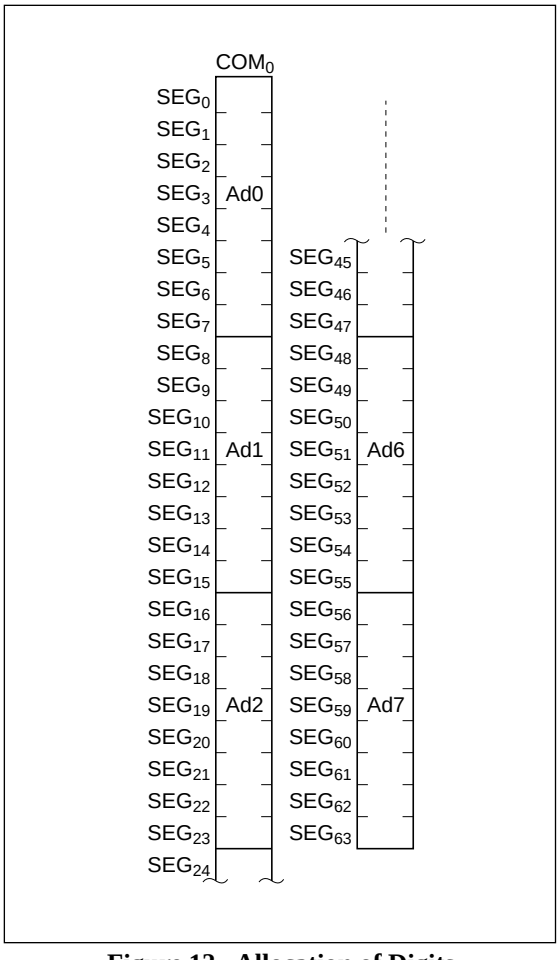


Figure 12 Allocation of Digits (HD61605)

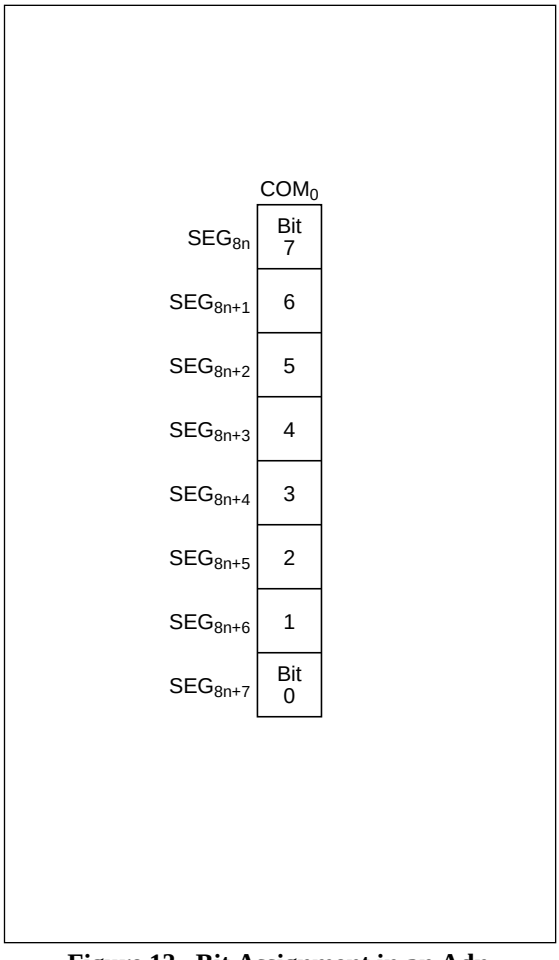


Figure 13 Bit Assignment in an Adn (HD61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

1. LCD drive mode

   Determines the LCD driving method.

   a. Static drive mode
      LCD is driven statically.

   b. 1/2 duty cycle drive mode
      LCD is driven with 1/2 duty cycle and 1/2 bias.

   c. 1/3 duty cycle drive mode
      LCD is driven with 1/3 duty cycle and 1/3 bias.

   d. 1/4 duty cycle drive mode
      LCD is driven at 1/4 duty cycle and 1/4 bias.

2. Data display mode

   Determines how to write display data into the data RAM.

   a. Static display mode
      8-bit data is written into the display RAM according to the digit in static drive.

   b. 1/2 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.

   c. 1/3 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.

   d. 1/4 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/4 duty cycle drive.

3. READY output mode

   Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   a. READY is always available (figure 14).

   b. READY is made available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

4. LCD off mode

   In this mode, the HD61604 stops driving the LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

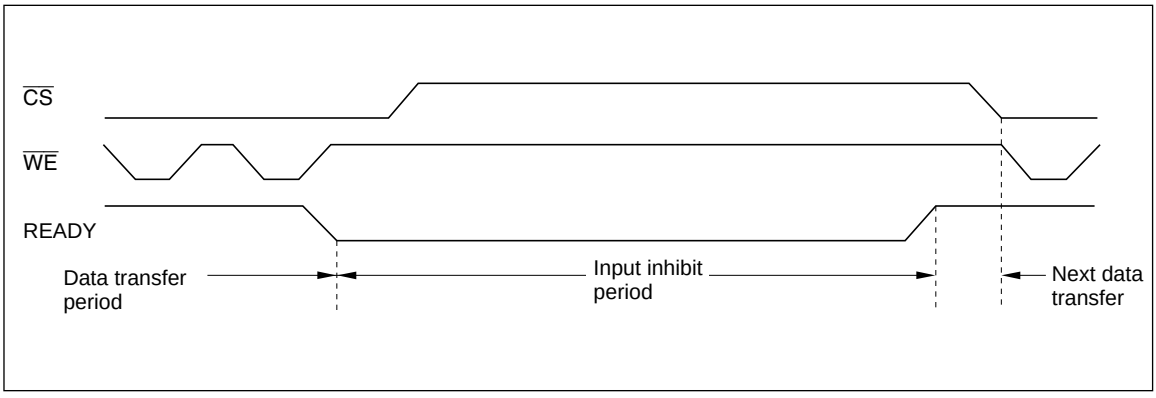


Figure 14 READY Output Timing (When It Is Always Available)

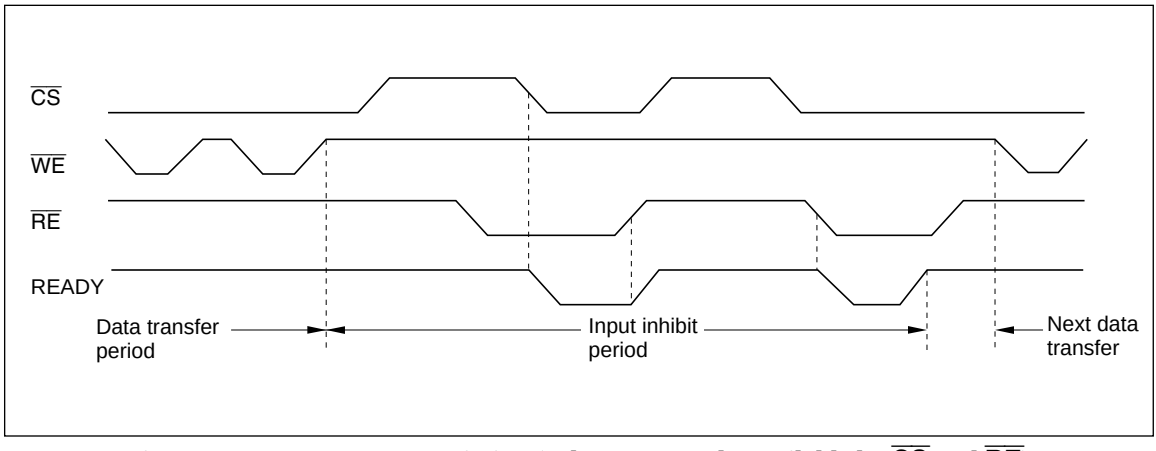


Figure 15 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

HD61605 Operating Modes

The HD61605 has the following operating modes:

1. READY output mode

   Determines the READY output timing.

   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

   a. READY is always available (figure 16).

   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$ (figure 17).

2. LCD off mode

   In this mode, the HD61605 stops driving the LCD and turns it off.

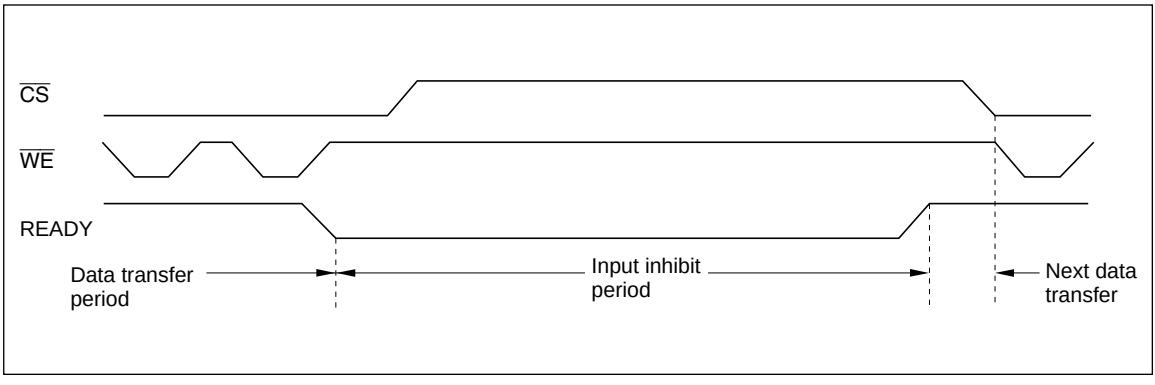


Figure 16 READY Output Timing (When It Is Always Available)

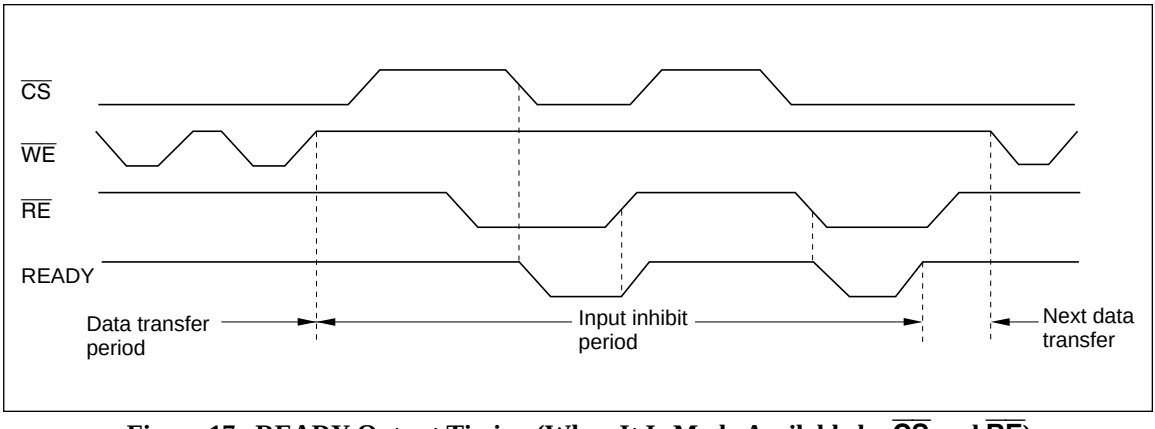


Figure 17 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

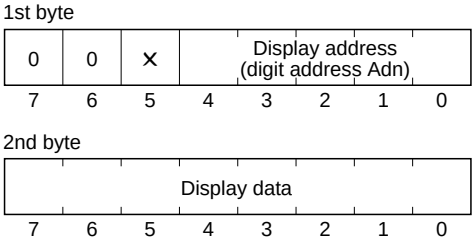
Input Data Formats

HD61604 Input Data Formats

Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

1. Display data

   Updates display on an 8-segment basis.



   a. Display address

      Digit address Adn in accordance with display mode

   b. Display data

      Pattern data written into the display RAM according to display mode and the address

2. Bit manipulation data

   Updates display on a segment basis.

   a. Display data

      Data written into 1 bit of the specified display RAM

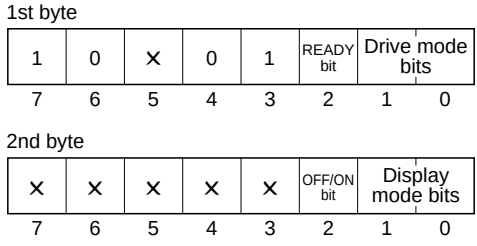
   b. COM address

      Common address of display RAM

   c. SEG address

      Segment address of display RAM

3. Mode setting data



   a. Display mode bits

      00: Static display mode

      01: 1/2 duty cycle display mode

      10: 1/3 duty cycle display mode

      11: 1/4 duty cycle display mode

   b. OFF/ON bit

      1: LCD off (set to 1 when SYNC is entered)

      0: LCD on

   c. Drive mode bits

      00: Static drive

      01: 1/2 duty cycle drive

      10: 1/3 duty cycle drive

      11: 1/4 duty cycle drive

   d. READY bit

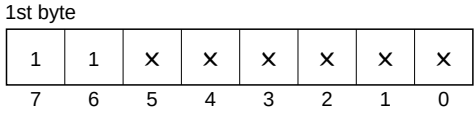
      0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)

      1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

Note: Input the same data to display mode bits and drive mode bits.

4. 1-byte instruction

   The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

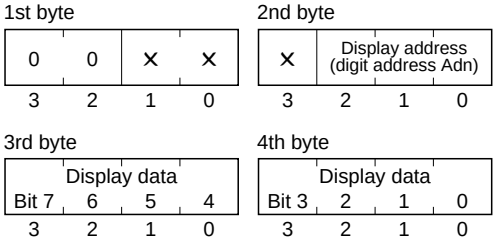


HD61605 Input Data Formats

Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse is enters into $\overline{RE}$ pin.

1. Display data

   Updates display on an 8-segment basis.



   a. Display address

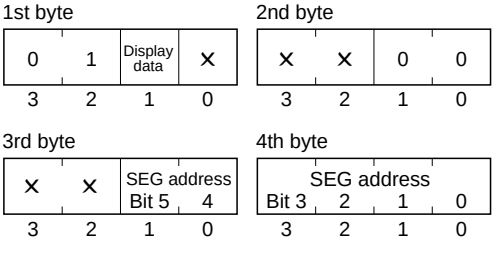
      Digit address Adn shown in figure 12.

   b. Display data

      Pattern data written into the display RAM as shown in figure 13.

2. Bit manipulation data

   Updates display on a segment basis.



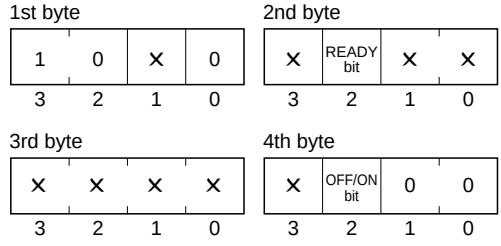
   a. Display data

      Data written into the 1 bit of the specified display RAM.

   b. SEG address

      Segment address of display RAM (segment output).

3. Mode setting data



   a. OFF/ON bit

      1: LCD off (set to 1 when SYNC is entered)

      0: LCD on

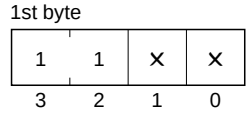
   b. READY bit

      0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)

      1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

4. 1-byte instruction

   The first data (4 bits) is ignored when the bit 3 and 2 in the data are 1.



How to Input Data

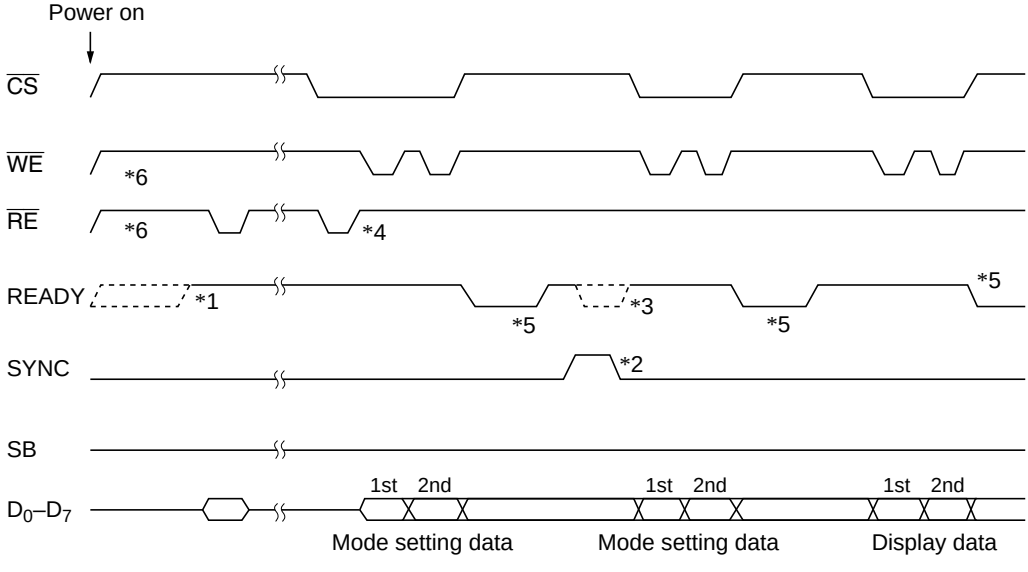
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted, because the first 8-bit data is distinguished from the second one by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
2. Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and figure 18.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
2. High pulse should be applied to SYNC pin when using two or more chips simultaneously.
3. In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
4. Reset the byte counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.
7. It is not always necessary to follow this example.

Figure 18 Example of Data Transfer Sequence

How to Input Data into HD61605

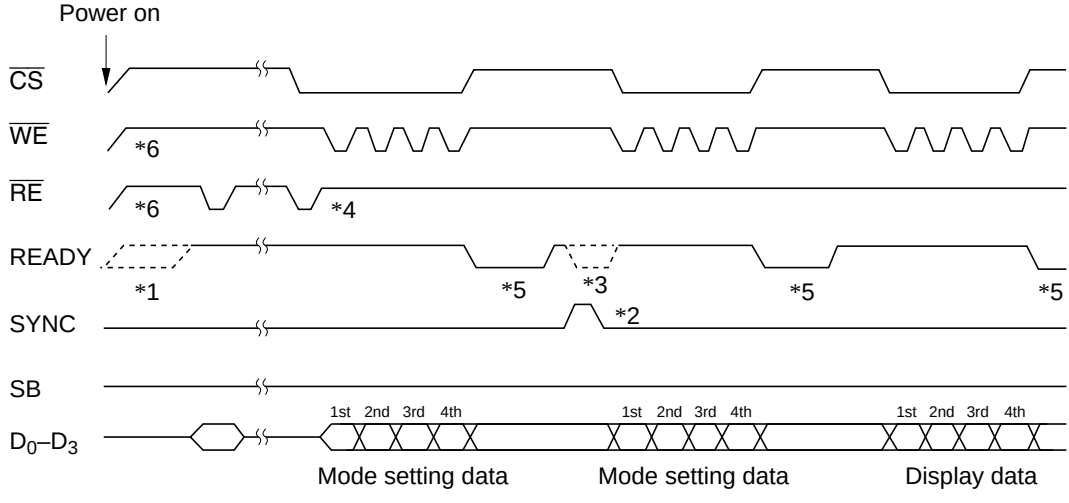
Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).

2. Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_3) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and figure 19.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
2. High pulse should be applied to SYNC pin when using two or more chips simultaneously.
3. In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
4. Reset the 4-bit data counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
7. It is not always necessary to follow this example.

Figure 19 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled until the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes.

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in figure 20 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605.

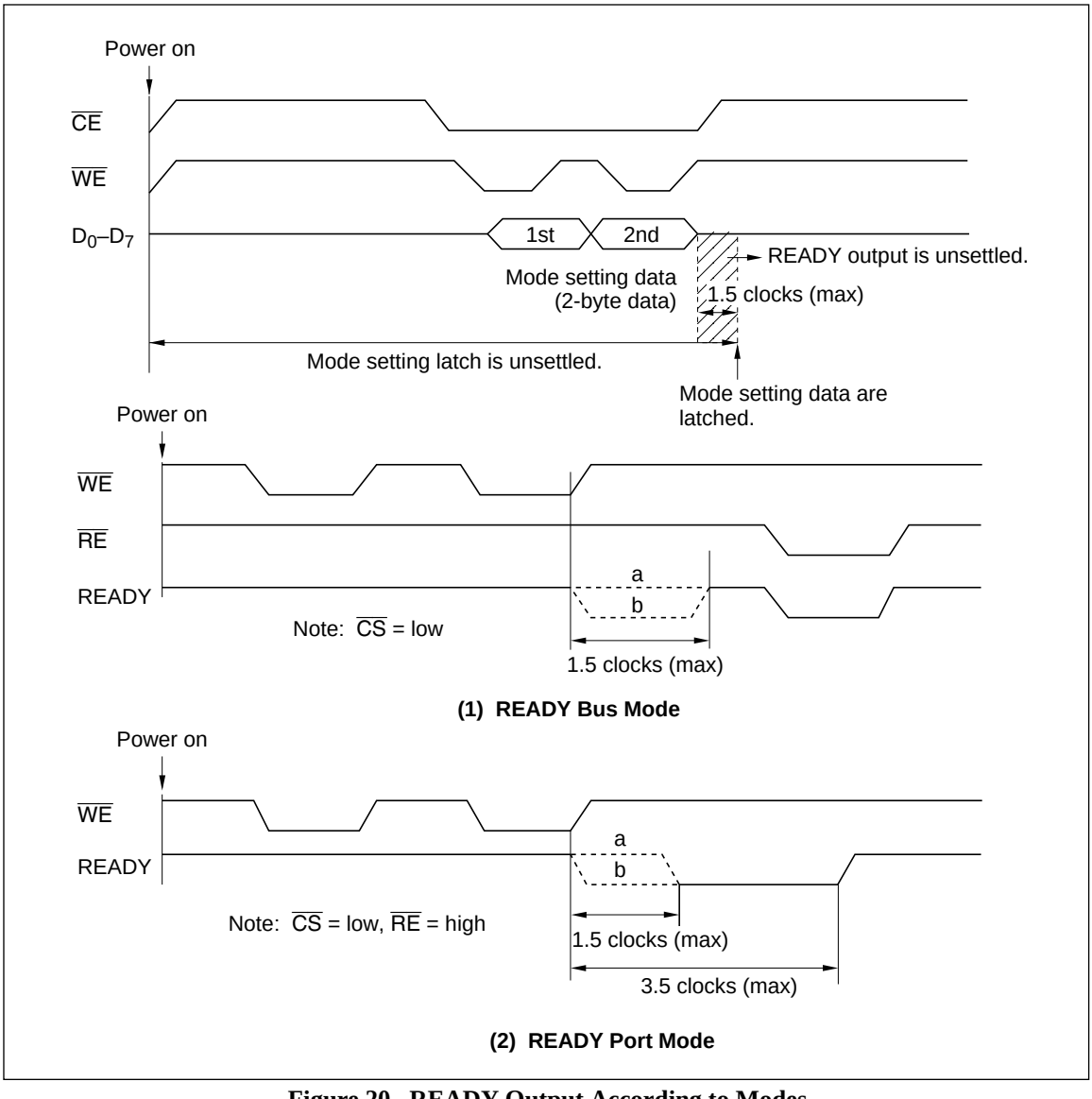


Figure 20 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low). In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multichip Operation

When an LCD is driven with two or more chips, the driving timing of the LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in “Input Data Formats.”) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

When SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geq$ 1 µF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages (figure 21); V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to the liquid crystal display. V_3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2–R5 in series between V_{DD} and V_{SS} (figure 22) generates ΔV or V_{LCD} by using the resistance ratio to supply these voltage to pins V_1, V_2, V_3, C2–C4 are the smoothing capacitors. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

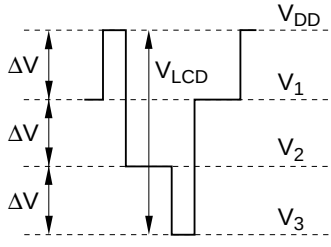
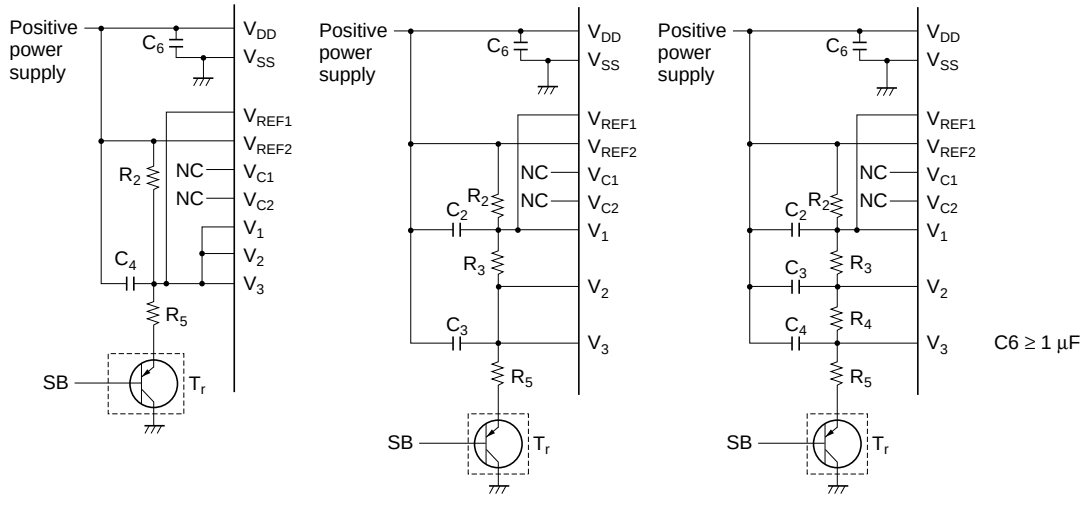


Figure 21 LCD Output Waveform and Output Levels (1/3 Duty Cycle, 1/3 Bias)



Notes: 1. When standby mode is used, a transistor is required.
2. R2–R5 should be some kΩ–some tens of kΩ, and C2–C4 should be 0.1 µF–0.3 µF.

Figure 22 Example when External Drive Voltage Is Used

Liquid Crystal Display Drive Voltage (HD61605)

As shown in figure 23, apply LCD drive voltage from the external power supply.

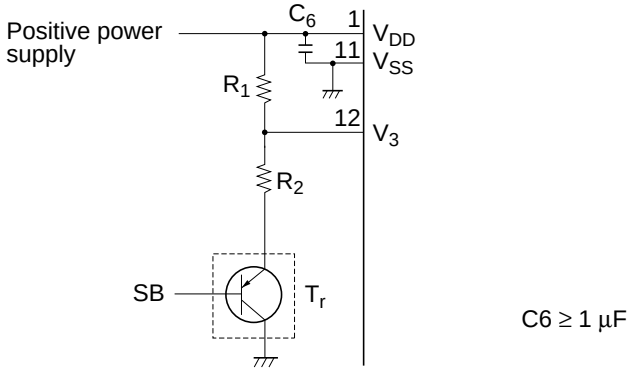
Oscillation Circuit

When Internal Oscillation Circuit Is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock Is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.



Note: When standby mode is used, a transistor is required.

Figure 23 Example of Drive Voltage Generator

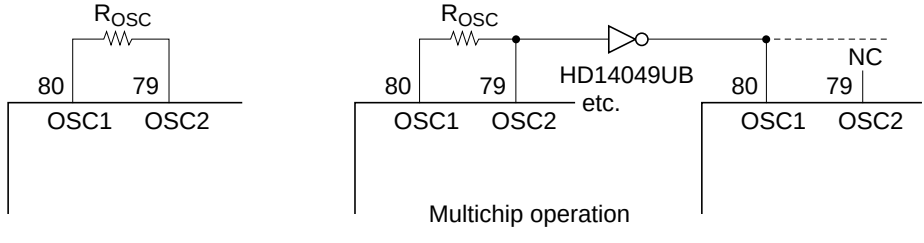


Figure 24 Example of Oscillation Circuit

Applications

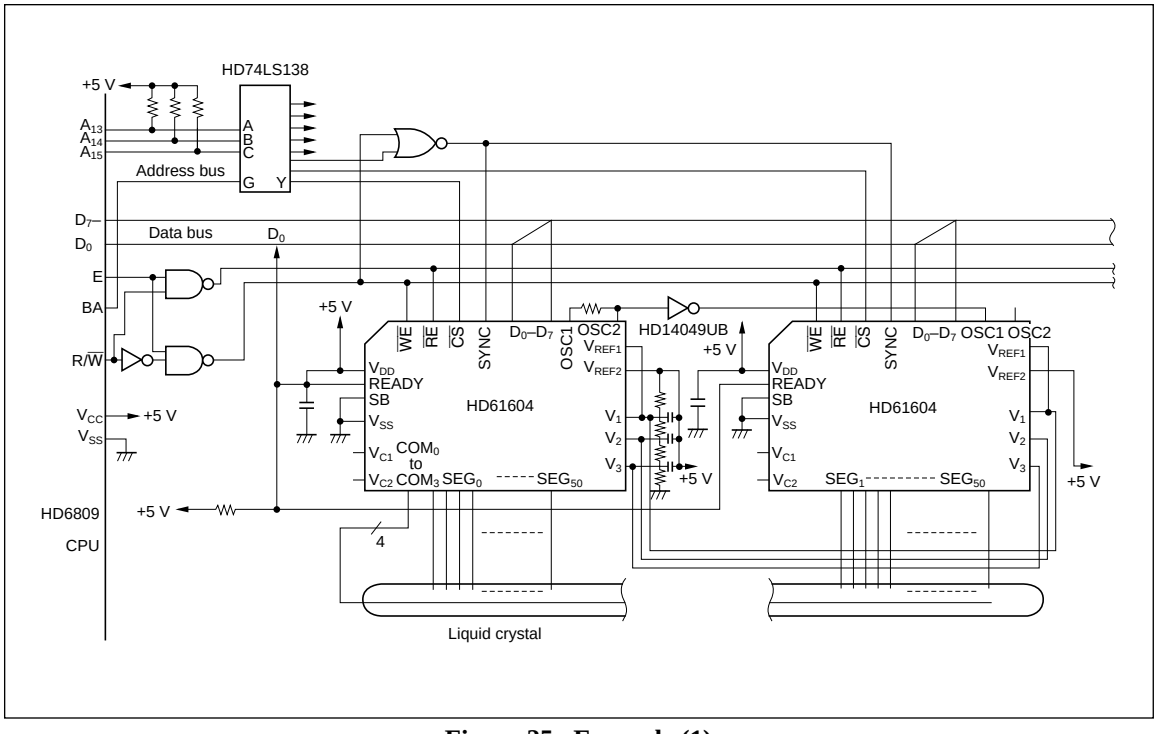


Figure 25 Example (1)

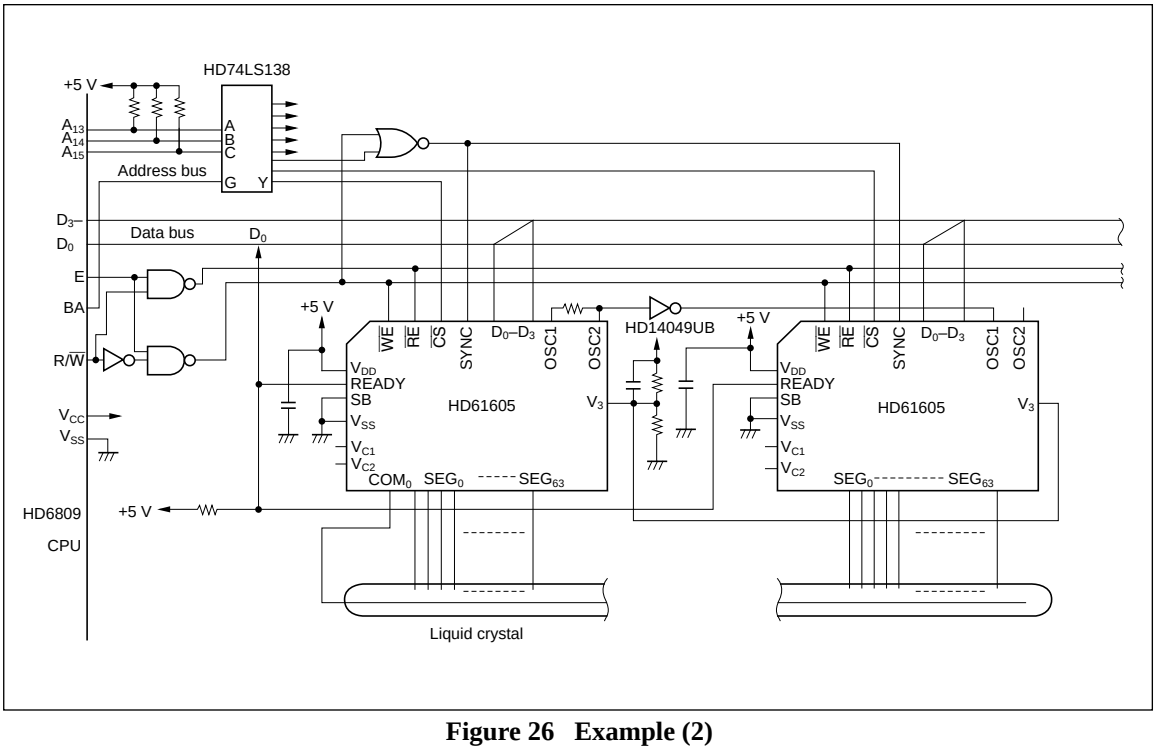


Figure 26 Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	–0.3 to +7.0	V
Pin voltage*	V_T	–0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

* Value referenced to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

		Limit			
Item	Symbol	Min	Typ	Max	Unit
Power supply voltage*	V_{DD}	4.5	—	5.5	V
	V_1, V_2, V_3	0	—	V_{DD}	V
Pin voltage*	V_T	0	—	V_{DD}	V
Operating temperature	T_{opr}	–20	—	+75	°C

* Value referenced to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC1	V_{IH1}	0.8 V_{DD}	—	V_{DD}	V	
	Others	V_{IH2}	2.0	—	V_{DD}	V	
Input low voltage	OSC1	V_{IL1}	0	—	0.2 V_{DD}	V	
	Others	V_{IL2}	0	—	0.8	V	
Output leakage current	READY	I_{OH}	—	—	5	µA	Pull up the pin to V_{DD}
Output low voltage	READY	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA
Input leakage current*1	Input pin	I_{IL1}	–1.0	—	1.0	µA	V_{IN} = 0 to V_{DD}
	V_1	I_{IL2}	–20	—	20	µA	V_{IN} = V_{DD} to V_3
	V_2, V_3	I_{IL3}	–5.0	—	5.0	µA	
LCD driver voltage drop	COM_0–COM_3	V_{d1}	—	—	0.3	V	±Id = 3 µA for each COM, V_3 = V_{DD} – 3 V
	SEG_0–SEG_{50}	V_{d2}	—	—	0.6	V	±Id = 3 µA for each SEG, V_3 = V_{DD} – 3 V
Current consumption*2		I_{DD}	—	—	100	µA	During display* R_{OSC} = 360 kΩ
		I_{DD}	—	—	5	µA	At standby

* Except the transfer operation of display data and bit data.

Notes: 1. V_1, V_2: applied only to HD61604.
2. Do not connect any wire to the output pins and connect the input pins to V_{DD} or V_{SS}.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC2	f_{osc}	70	100	130	kHz	R_{osc} = 360 kΩ
External clock frequency	OSC1	f_{osc}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	—	—	ns	
		t_H	10	—	—	ns	
		t_{WH}	300	—	—	ns	
		t_{WL}	400	—	—	ns	
		t_{WR}	400	—	—	ns	
		t_{DL}	—	—	1.0	µs	Figure 31
		t_{EN}	400	—	—	ns	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	—	—	25	ns	

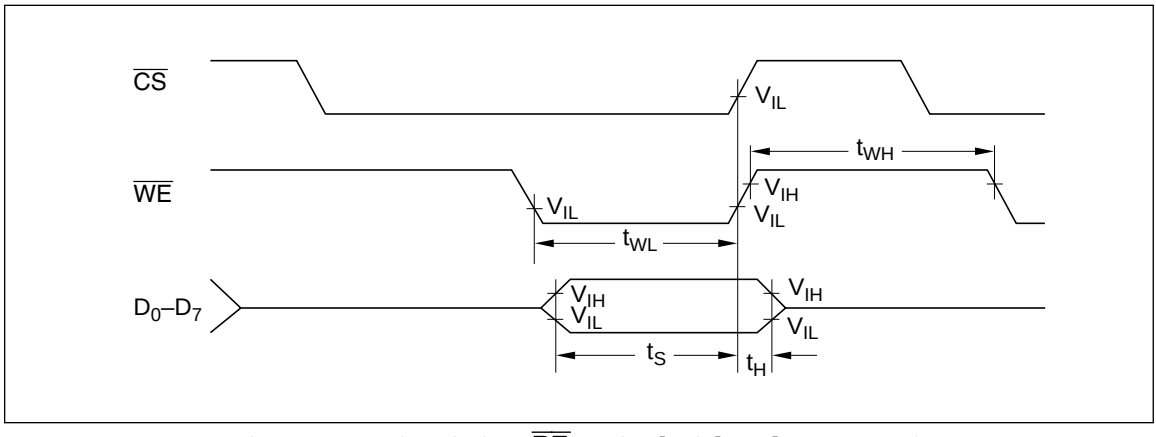


Figure 27 Write Timing ($\overline{RE}$ Is Fixed High and SYNC Low)

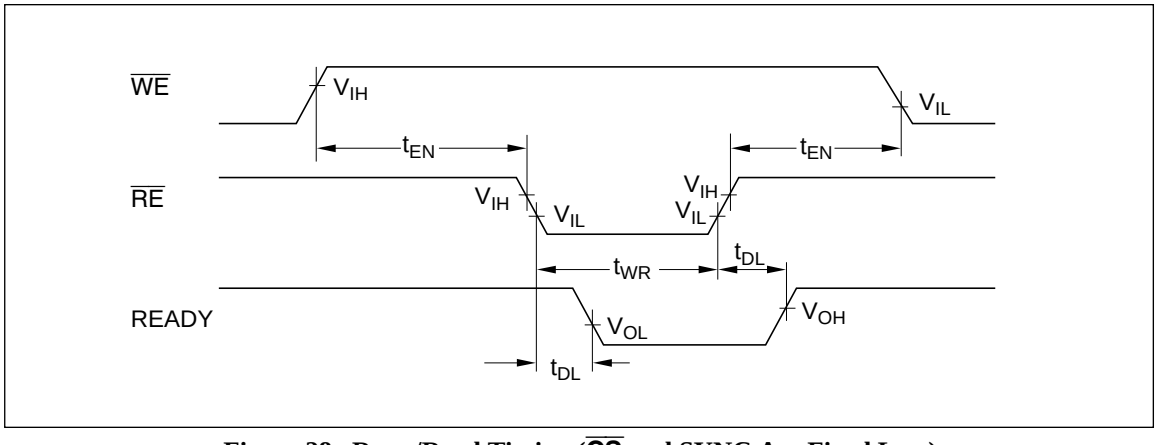


Figure 28 Reset/Read Timing ($\overline{CS}$ and SYNC Are Fixed Low)

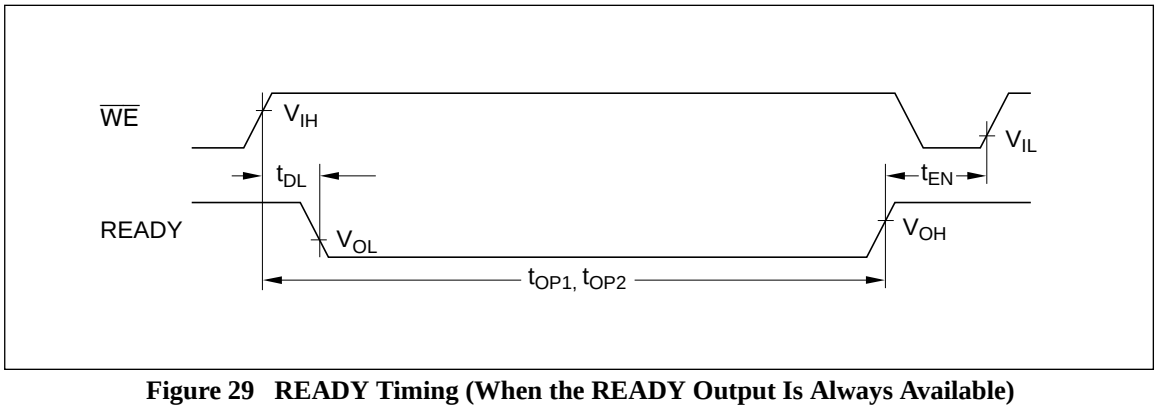


Figure 29 READY Timing (When the READY Output Is Always Available)

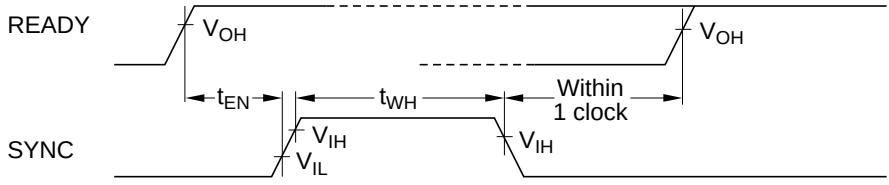


Figure 30 SYNC Timing

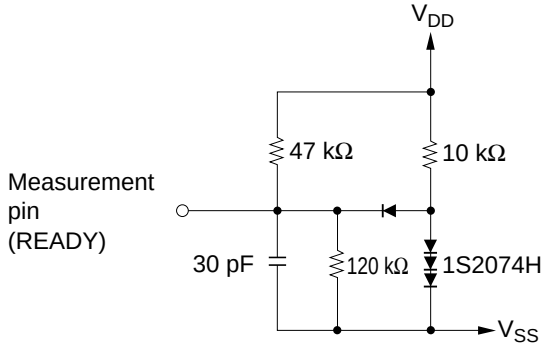


Figure 31 Bus Timing Load Circuit (LS-TTL Load)

HD61830/HD61830B LCDC

(LCD Timing Controller)

HITACHI

Description

The HD61830/HD61830B is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcontroller in the external RAM to generate dot matrix liquid crystal driving signals.

It has a graphic mode in which 1-bit data in the external RAM corresponds to the on/off state of 1 dot on liquid crystal display and a character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830/HD61830B is produced by the CMOS process. Thus, combined with a CMOS microcontroller it can complete a liquid crystal display device with lower power dissipation.

Features

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - — Graphic mode: 512k dots (2^{16} bytes)
  - — Character mode: 4096 characters (2^{12} characters)
- Internal character generator ROM: 7360 bits
  - — 160 types of 5×7 dot characters
  - — 32 types of 5×11 dot characters

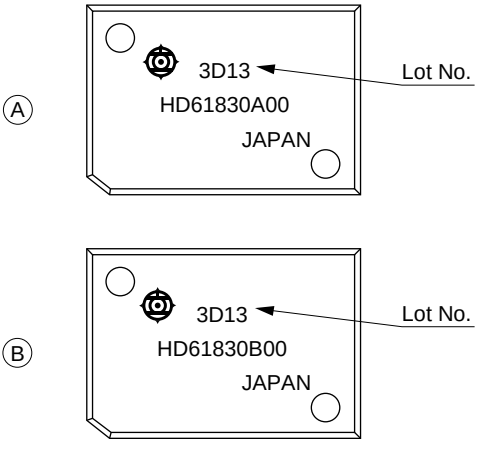
    Total 192 characters
  - — Can be extended to 256 characters (4 kbytes max.) with external ROM
- Interfaces to 8-bit MPU
- Display duty cycle (can be selected by a program) Static to 1/128 duty cycle
- Various instruction functions
  - — Scroll, cursor on/off/blink, character blink, bit manipulation
- Display method: Selectable A or B types
- Internal oscillator (with external resistor and capacitor) HD61830
- Operating frequency
  - — 1.1 MHz HD61830
  - — 2.4 MHz HD61830B
- Low power dissipation
- Power supply: Single +5 V ±10%
- CMOS process

Hitachi semiconductor

Differences between Products HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal or external	External only
Operating frequency	1.1 MHz	2.4 MHz
Pin arrangement and signal name	Pin 6: C Pin 7: R Pin 9: CPO	Pin 6: $\overline{CE}$ Pin 7: $\overline{OE}$ Pin 9: NC
Package marking to see figure	Ⓐ	Ⓑ

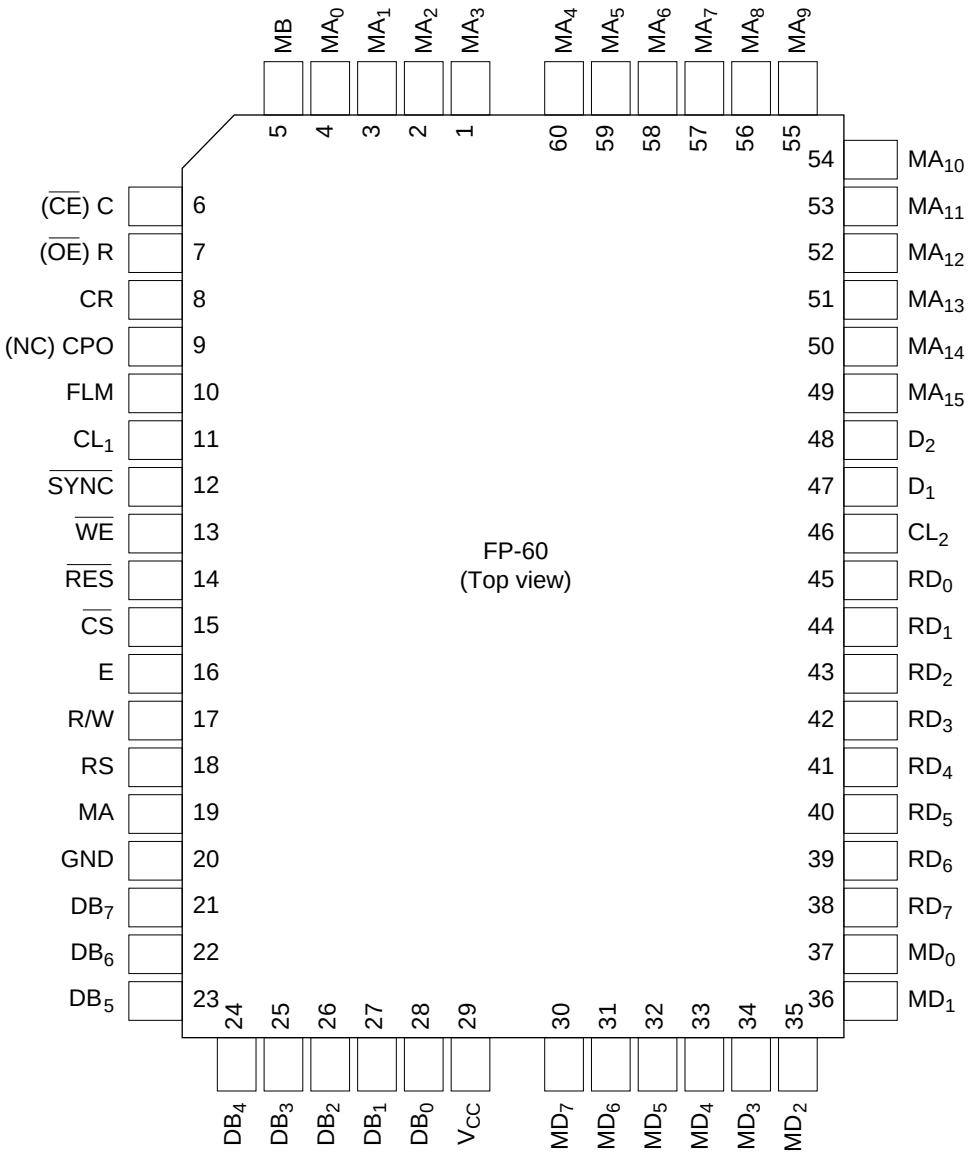
Package Marking



Ordering Information

Type No.	Package
HD61830A00H	60-pin plastic QFP (FP-60)
HD61830B00H	

Pin Arrangement

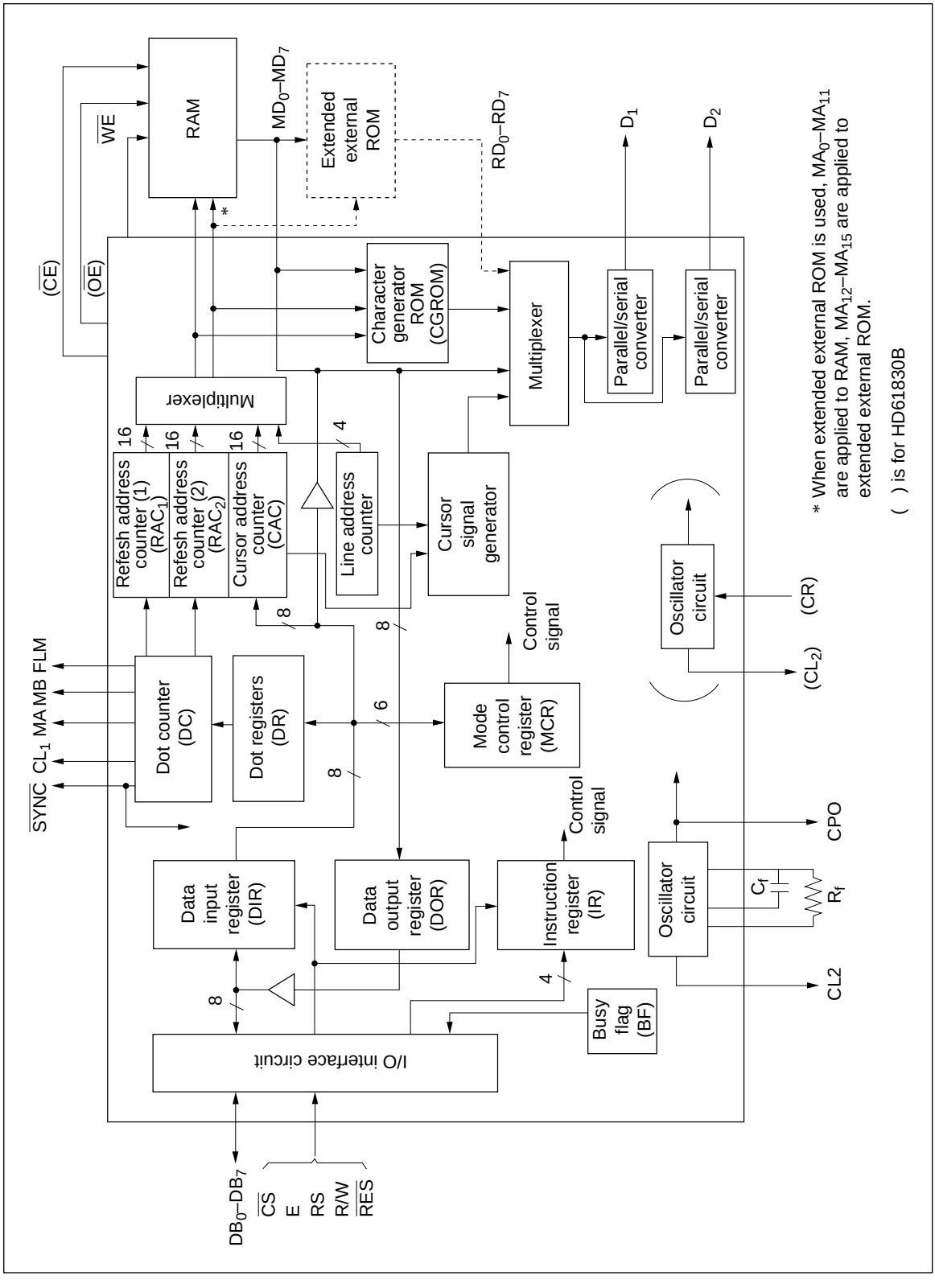


( ) is for HD61830B

Terminal Functions

Symbol	Pin Number	I/O	Function
DB_0–DB_7	28–21	I/O	Data bus: Three-state I/O common terminal Data is transferred to MPU through DB_0 to DB_7.
$\overline{CS}$	15	I	Chip select: Selected state with $\overline{CS}$ = 0
R/W	17	I	Read/Write: R/W = 1: MPU ← HD61830 R/W = 0: MPU → HD61830
RS	18	I	Register select: RS = 1: Instruction register RS = 0: Data register
E	16	I	Enable: Data is written at the fall of E Data can be read while E is 1
CR	8	I	CR oscillator (HD61830), External clock input (HD61830B)
C	6	—	CR oscillator to capacitor (HD61830 only)
R	7	—	CR oscillator to resistor (HD61830 only)
CPO	9	O	Clock signal for HD61830 in slave mode (HD61830 only)
$\overline{CE}$	6	O	Chip enable (HD61830B only) $\overline{CE}$ = 0: Chip enables make external RAM in active
$\overline{OE}$	7	O	Output enable (HD61830B only) $\overline{OE}$ = 1: Output enable informs external RAM that HD61830B requires data bus
NC	9	Open	Unused terminal. Don't connect any wires to this terminal (HD61830B only)
MA_0–MA_{15}	4–1, 60–49	O	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 (0: Character 1st line, F: Character 16th line)
MD_0–MD_7	37–30	I/O	Display data bus: Three-state I/O common terminal
RD_0–RD_7	45–38	I	ROM data input: Dot data from external character generator is input
$\overline{WE}$	13	O	Write enable: Write signal for external RAM
CL_2	46	O	Display data shift clock for LCD drivers
CL_1	11	O	Display data latch signal for LCD drivers
FLM	10	O	Frame signal for display synchronization
MA	19	O	Signal for converting liquid crystal driving signal into AC, A type
MB	5	O	Signal for converting liquid crystal driving signal into AC, B type
D_1	47	O	Display data serial output
D_2	48		D_1: For upper half of screen D_2: For lower half of screen
$\overline{SYNC}$	12	I/O	Synchronous signal for parallel operation Three-state I/O common terminal (with pull-up MOS) Master: Synchronous signal is output Slave: Synchronous signal is input
$\overline{RES}$	14	I	Reset: Reset = 0 results in display off, slave mode and H_p = 6

Block Diagram



Block Functions

Registers

The HD61830/HD61830B has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR), and mode control register (MCR).

The IR is a 4-bit register that stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register, and so on. The lower order 4 bits DB_0 to DB_3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR, and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at the high level).

The DR are registers used to store dot information such as character pitches and the number of vertical dots, and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display on/off and cursor on/off/blink. The information sent from the MPU is written in it via the DIR.

Busy Flag (BF)

The busy flag = 1 indicates the HD61830 is performing an internal operation. Instructions cannot be accepted. As shown in Control Instruction, read busy flag, the busy flag is output on DB_7 under the conditions of RS = 1, R/W = 1, and E = 1. Make sure the busy flag is 0 before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

Refresh Address Counters (RAC1/RAC2)

The refresh address counters, RAC1 and RAC2, control the addresses of external RAM, character generator ROM (CGROM), and extended external ROM. The RAC1 is used for the upper half of the screen and the RAC2 for the lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA_{12}–MA_{15}) are ignored. The 4 bits of line address counter are output instead and used as the address of extended ROM.

Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 characters) or 5×11 (32 characters). The use of extended ROM allows 8×16 (256 characters max.) to be used.

Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by instruction. It holds an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of the cursor address counter is automatically increased by 1 after the display data is read or written and after the set/clear bit instruction is executed.

Cursor Signal Generator

The cursor can be displayed by instruction in character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM, or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS = 1, and the data register code is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS = 0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

1. Mode Control: Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor off	Internal CG	Character display (Character mode)
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor off	External CG	
		0	1			Cursor on		
		1	0			Cursor off, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Graphic/character mode	Ext./Int. CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

2. Set Character Pitch: Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is included in the determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

H_p indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the H_p indicates the number of bits of 1-byte display data to be displayed.

There are three H_p values (table 1).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p – 1) binary				0	(H_p – 1) binary		

Table 1 H_p Values

Hp	DB2	DB1	DB0	Horizontal Character Pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

3. Set Number of Characters: H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = H_p \times H_N$$

H_N can be set to an even number from 2 to 128 (decimal).

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(H_N – 1) binary						

4. Set Number of Time Divisions (Inverse of Display Duty Ratio): N_X indicates the number of time divisions in multiplex display.

$1/N_X$ is the display duty ratio.

A value of 1 to 128 (decimal) can be set to N_X.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time-divisions reg.	0	0	0	(N_X – 1) binary						

5. Set Cursor Position: C_p indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying C_p = 8 (decimal). The cursor horizontal length is equal to the horizontal character pitch H_p. A value of 1 to 16 (decimal) can be set to C_p. If a smaller value than the vertical character pitch V_p is set ($C_p \leq V_p$), and a character overlaps with the cursor, the cursor has higher priority of display (at cursor display on). If C_p is greater than V_p, no cursor is displayed. The cursor horizontal length is equal to H_p.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(C_p – 1) binary			

6. Set Display Start Low Order Address: Cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address (DB_3–DB_0) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

Set Display Start High Order Address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

7. Set Cursor Address (Low Order) (RAM Write Low Order Address): Cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM.

That is, data at the address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the character specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements setting the cursor address (table 2).

The cursor address counter is a 16-bit up-counter with set and reset functions. When bit N changes from 1 to 0, bit N + 1 is incremented by 1. When setting the low order address, the LSB (bit 1) of the high order address is incremented by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in the table 2.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

Set Cursor Address (High Order) (RAM Write High Order Address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

Table 2 Cursor Address Setting

Condition	Requirement
When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
When you want to rewrite only the low order address.	Do not fail to set the high order address again after setting the low order address.
When you want to rewrite only the high order address.	Set the high order address. You do not have to set the low order address again.

8. Write Display Data: After the code $"OC" is written into the instruction register with RS = 1, 8-bit data with RS = 0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

9. Read Display Data: Data can be read from the RAM with RS = 0 after writing code $"OD" into the instruction register. Figure 1 shows the read procedure.

This instruction outputs the contents of data output register on the data bus (DB_0 to DB_7) and then transfers RAM data specified by the cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second one. Thus, make one dummy read when reading data after setting the cursor address.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

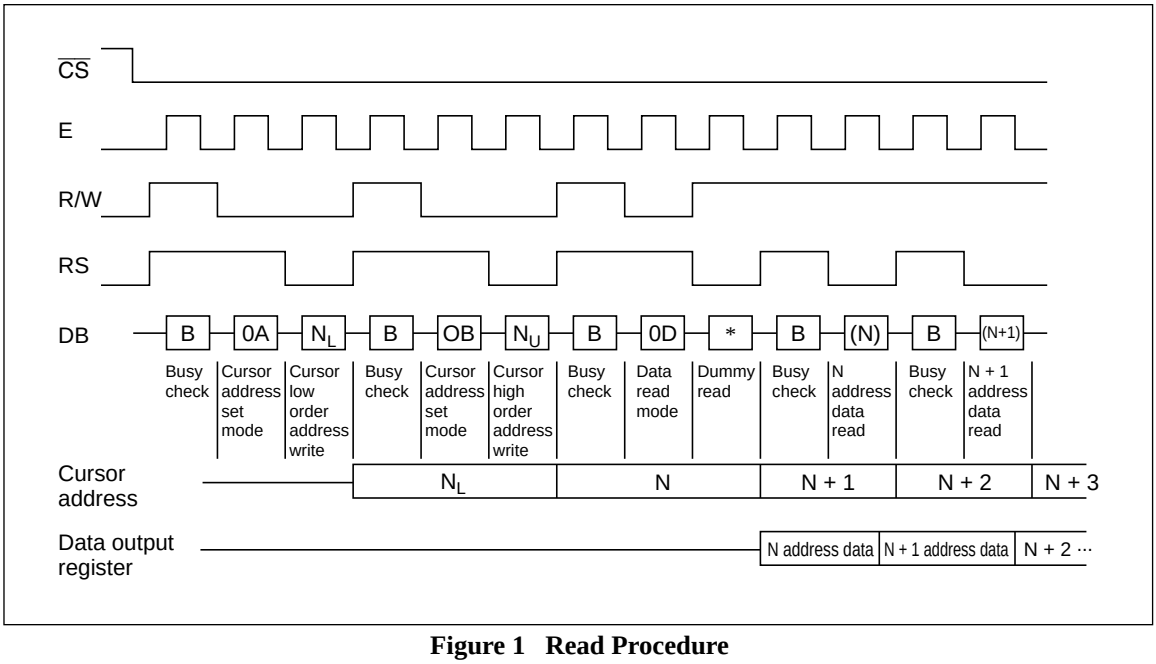


Figure 1 Read Procedure

10. Clear Bit: The clear/set bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value from 1 to 8. $N_B = 1$ and $N_B = 8$ indicates LSB and MSB, respectively.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B – 1) binary		

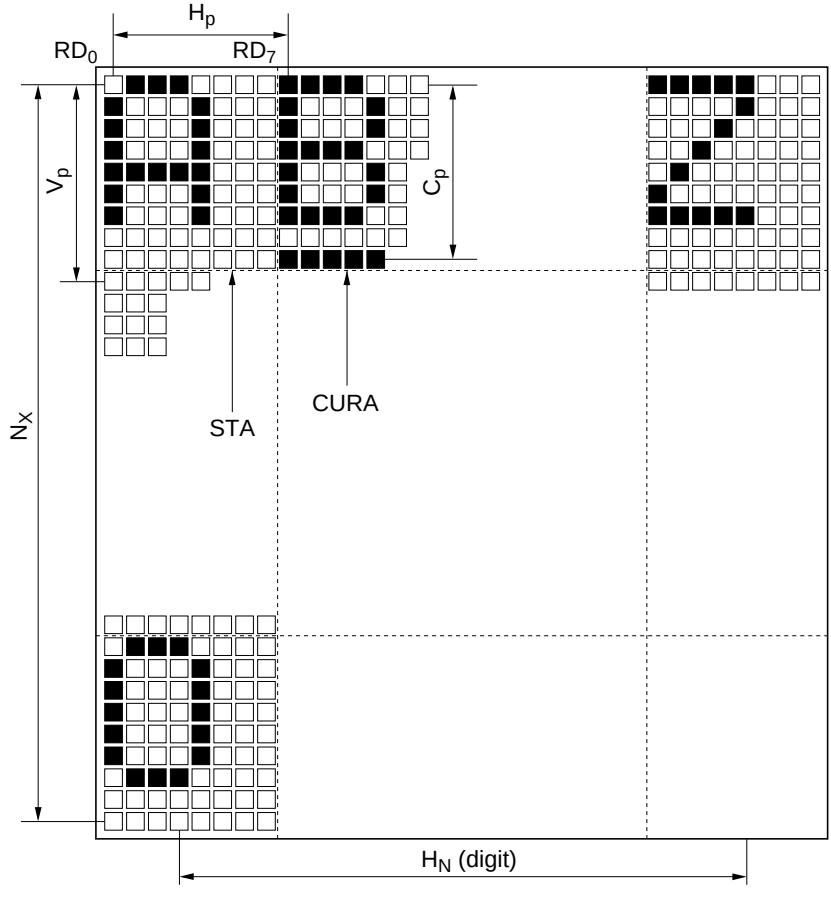
Set Bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B – 1) binary		

11. Read Busy Flag: When the read mode is set with RS = 1, the busy flag is output to DB_7. The busy flag is set to 1 during the execution of any of the other instructions. After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag = 1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS = 1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS = 1.

The busy flag can be read without specifying any instruction register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0	*						



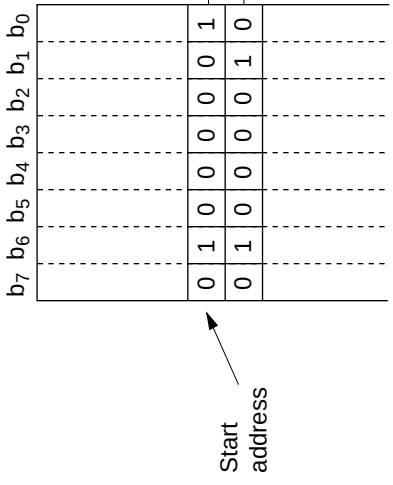
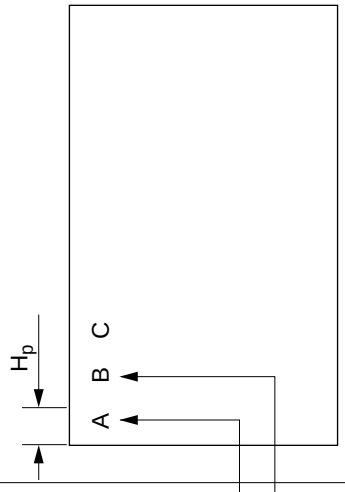
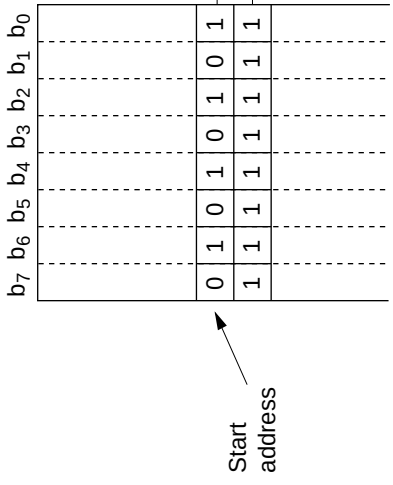
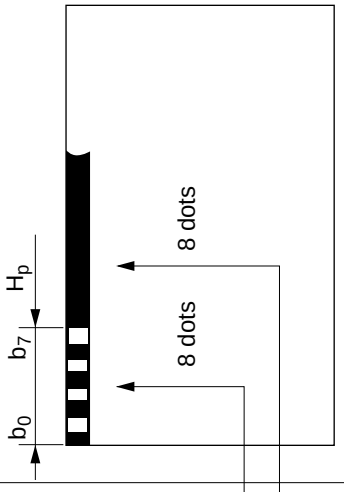
Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Horizontal character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of horizontal characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode	2 to 128 digits (an even number)
V_p	Vertical character pitch	Vertical character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_X	Number of time divisions	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on the screen is m, and the number of horizontal dots is n,

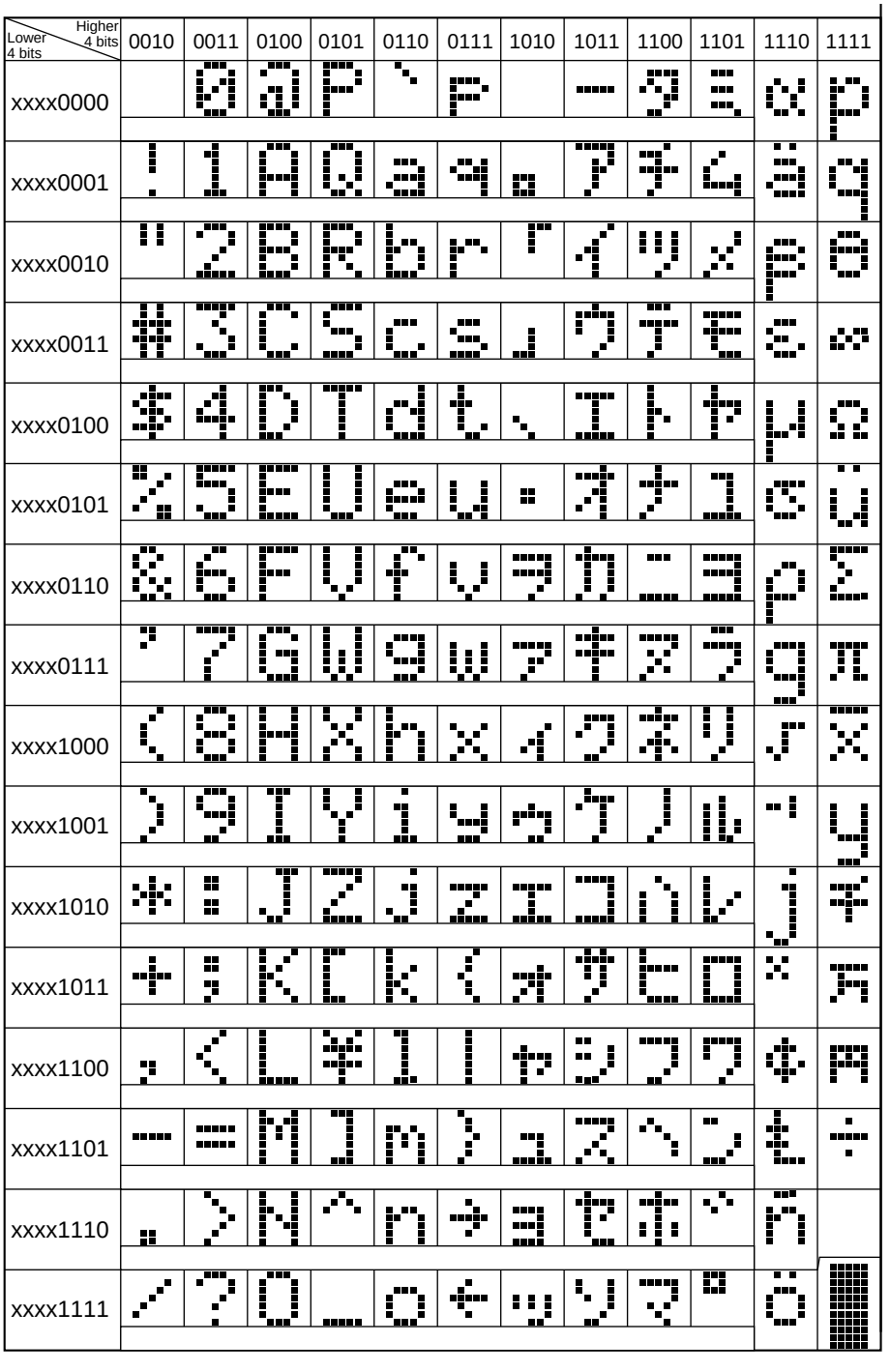
$1/m = 1/N_X$ = display duty ratio
$n = H_p \times H_N$,
m/V_p = Number of display lines
$C_p \leq V_p$

Figure 2 Display Variables

Display Mode

Display Mode	Display Data from MPU	RAM	Liquid Crystal Display Panel
Character display	Character code (8 bits)		
Graphic	Display pattern (8 bits)		

Internal Character Generator Patterns and Character Codes



Example of Correspondence between External CG ROM Address Data and Character Pattern

8 × 8 Dot Font

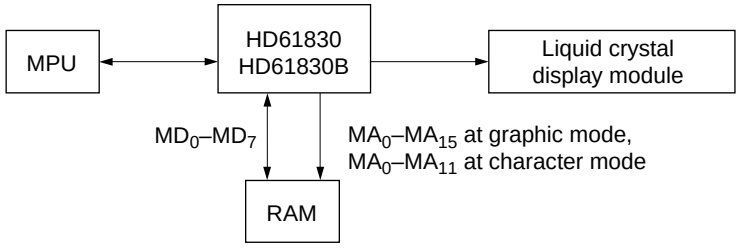
	A10	0								0								0	1
	A 9	0								0								0	1
	A 8	0								0								1	1
	A 7	0								1								0	1
A6 A5 A4 A3	A2 A1 A0	0_0	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_0	0_1	0_2	0_3	0_4	0_5	0_6	0_7		
0 0 0 0	0 0 0	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0		
	0 0 1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		
	0 1 0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		
	0 1 1	1	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0		
	1 0 0	1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	0		
	1 0 1	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0		
	1 1 0	1	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0		
	1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0 0 0 1	0 0 0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0		
	0 0 1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0		
	0 1 0	1	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1		
	0 1 1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0		
	1 0 0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	
	1 0 1	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0		
	1 1 0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0		
	1 1 1	1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0		
0 0 1 0	0 0 0																		

8 × 16 Dot Font

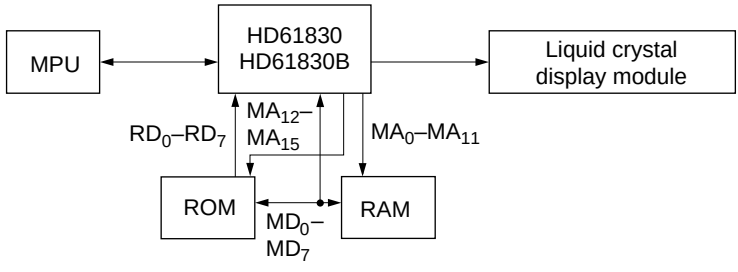
	A11	0								0								0
	A10	0								0								0
	A 9	0								0								1
	A 8	0								1								0
A7 A6 A5 A4	A3 A2 A1 A0	0_0	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_0	0_1	0_2	0_3	0_4	0_5	0_6	0_7	
0 0 0 0	0 0 0 0					0	0	0	0	0	0	0	0	0	0	0	0	
	0 0 0 1		0	0	0		0	0	0	0	0	0	0	0	0	0	0	
	0 0 1 0		0	0	0		0	0	0	0	0	0	0	0	0	0	0	
	0 0 1 1					0	0	0	0		0	0	0	0	0		0	
	0 1 0 0		0		0	0	0	0	0	0		0	0	0		0	0	
	0 1 0 1		0	0		0	0	0	0	0	0		0		0	0	0	
	0 1 1 0		0	0	0		0	0	0	0	0	0		0	0	0	0	
	0 1 1 1	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	
	1 0 0 0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	
	1 0 0 1	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	
	1 0 1 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 0 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 0 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 1 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1 1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Example of Configuration

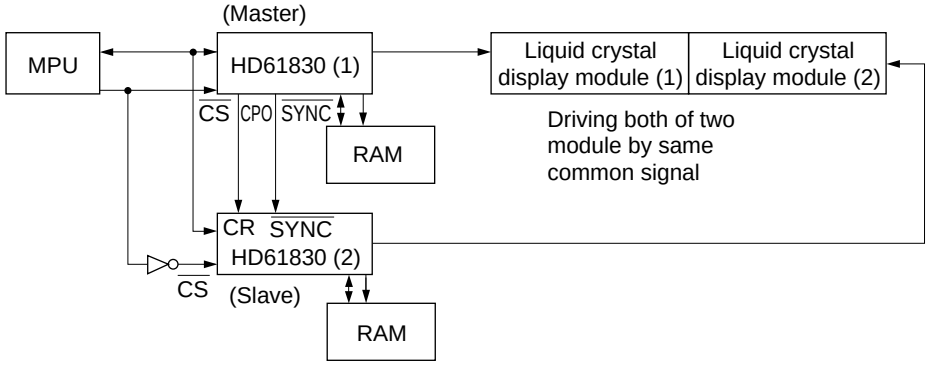
Graphic Mode or Character Mode (1) (Internal Character Generator)



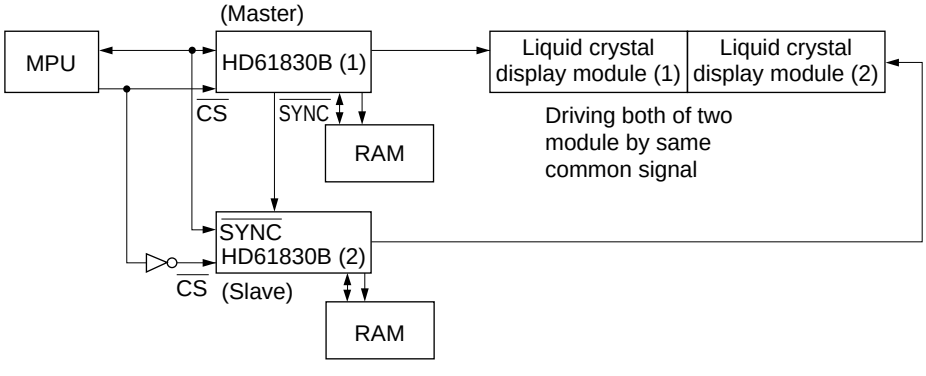
Character Mode (2) (External Character Generator)



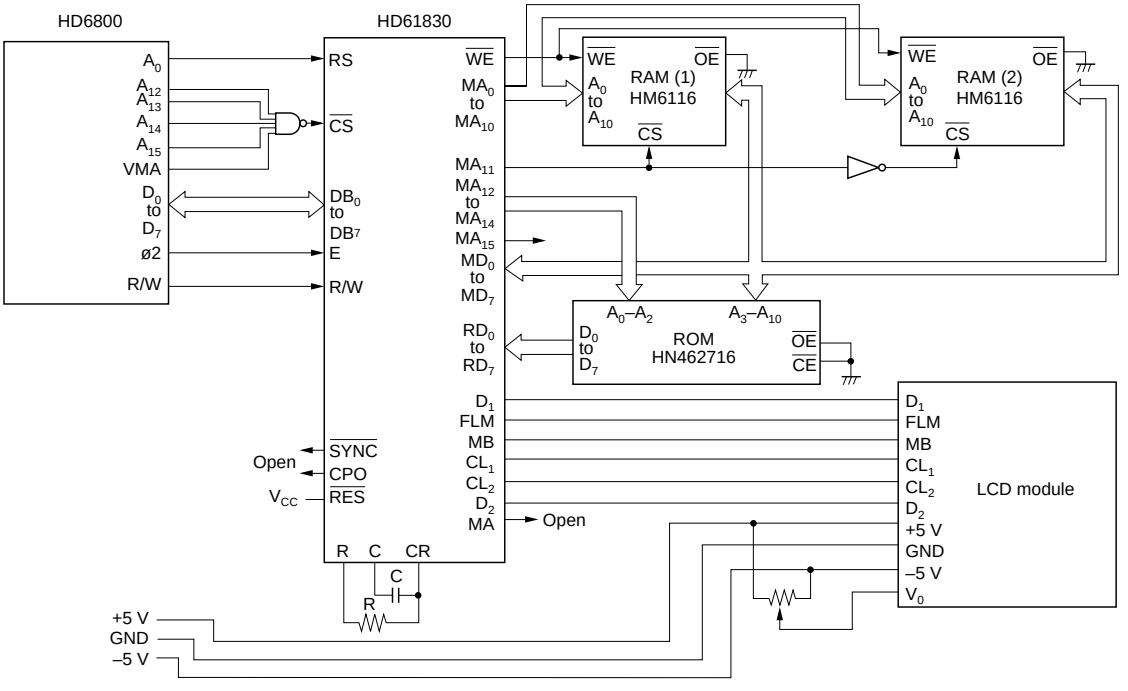
Parallel Operation (HD61830)



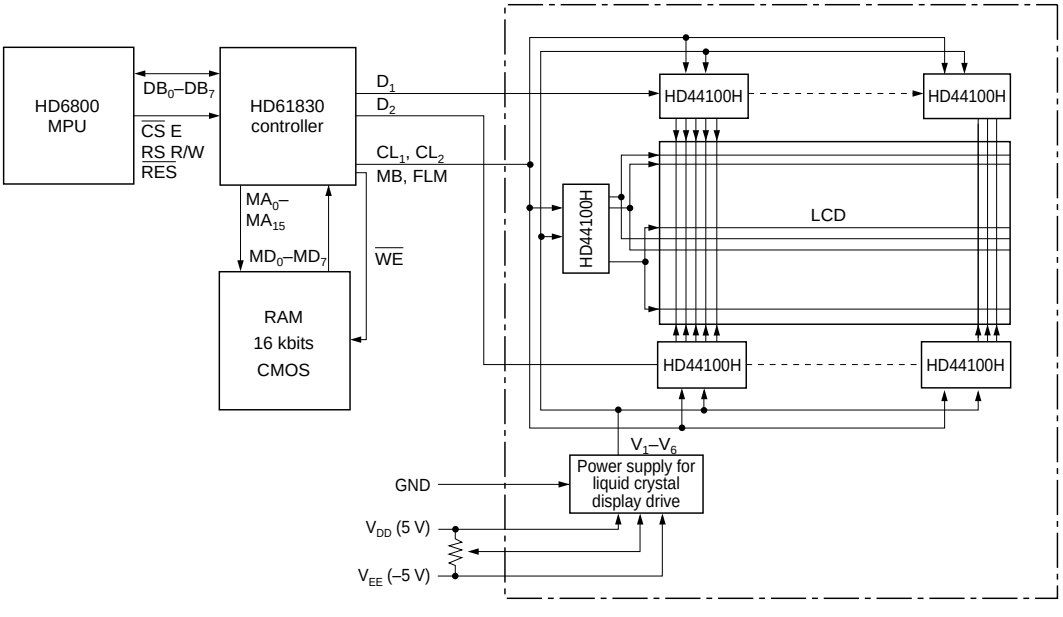
Parallel Operation (HD61830B)



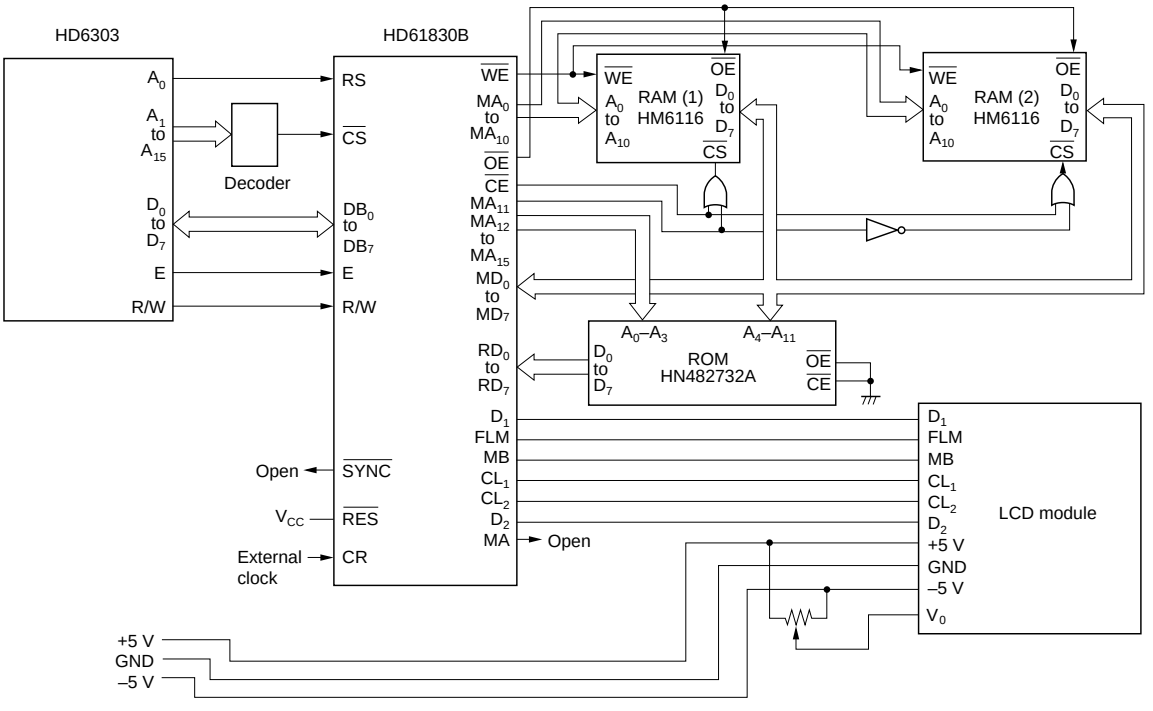
HD61830 Application (Character Mode, External CG, Character Font 8 × 8)



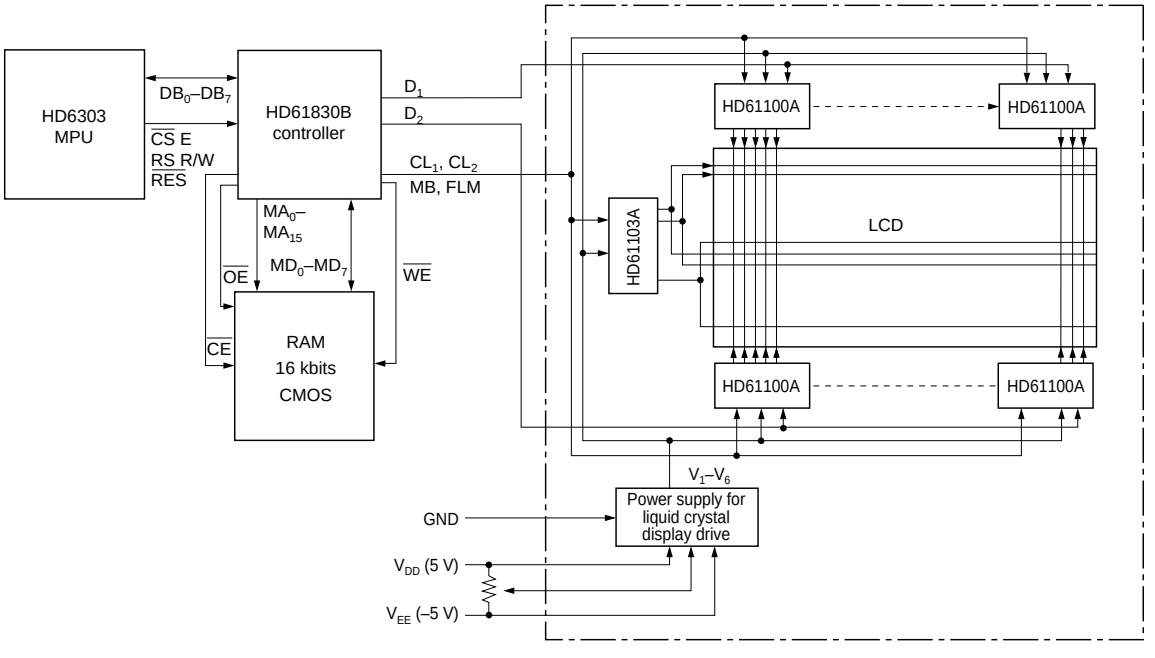
HD61830 Application (Graphic Mode)



HD61830B Application (Character Mode, External CG, Character Font 8 × 8)



HD61830B Application (Graphic Mode)



HD61830 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +0.7	V	1, 2
Terminal voltage	V_T	–0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. All voltages are referenced to GND = 0 V.

2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

HD61830 Electrical Characteristics (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

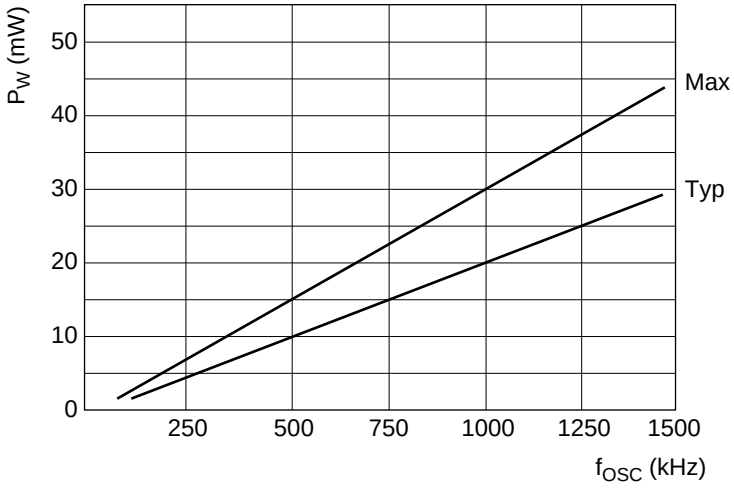
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (TTL)	V_{IH}	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	V_{IL}	0	—	0.8	V		2
Input high voltage	V_{IHR}	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	V_{IHC}	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	V_{OH}	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	V_{OL}	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	V_{OHC}	V_{CC} – 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	V_{OLC}	0	—	0.4	V	I_{OL} = 0.6 mA	6
Input leakage current	I_{IN}	–5	—	5	µA	V_{IN} = 0 – V_{CC}	7
Three-state leakage current	I_{TSL}	–10	—	10	µA	V_{OUT} = 0 – V_{CC}	8
Power dissipation (1)	P_W1	—	10	15	mW	CR oscillation f_{osc} = 500 kHz	9
Power dissipation (2)	P_W2	—	20	30	mW	External clock f_{cp} = 1 MHz	9
Internal clock operation (Clock oscillation frequency)	f_{osc}	400	500	600	kHz	C_f = 15 pF ±5% R_f = 39 kΩ ±2%	10
External clock operation (External clock operating frequency)	f_{cp}	100	500	1100	kHz		11
External clock duty	Duty	47.5	50	52.5	%		11
External clock rise time	t_{rcp}	—	—	0.05	µs		11
External clock fall time	t_{fcp}	—	—	0.05	µs		11
Pull-up current	I_{PL}	2	10	20	µA	V_{IN} = GND	12

Notes: The I/O terminals have the following configuration:

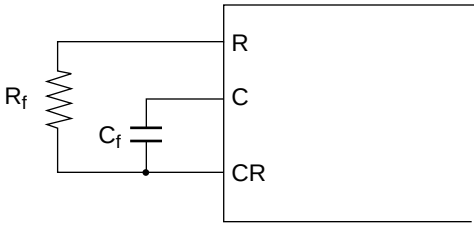
1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB_0–DB_7, $\overline{WE}$, MA_0–MA_{15}, and MD_0–MD_7.
6. Applied to terminals $\overline{SYNC}$, CP0, FLM, CL_1, CL_2, D_1, D_2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

9. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

   The relationship between the operating frequency and the power dissipation is given below.

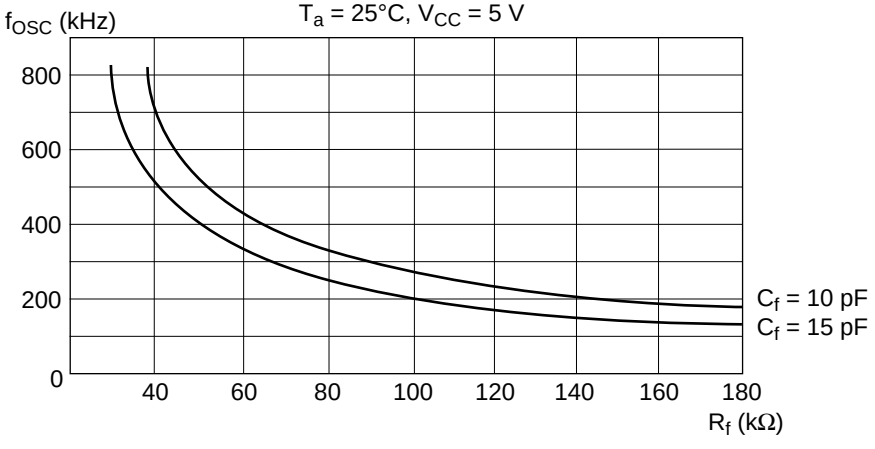


10. Applied to the operation of the internal oscillator when oscillation resistor R_f and oscillation capacity C_f are used.

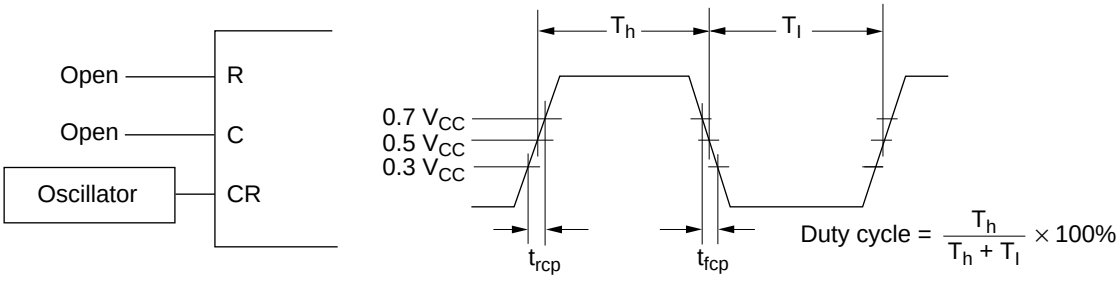


C_f = 15 pF ±5%
R_f = 39 kΩ ±2%
(when f_{OSC} = 500 kHz typ)

The relationship among oscillation frequency, R_f and C_f is given below.



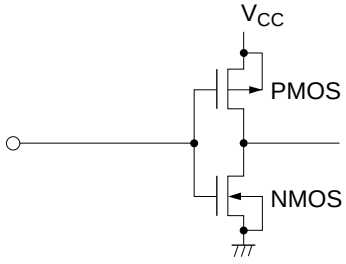
11. Applied to external clock operation.



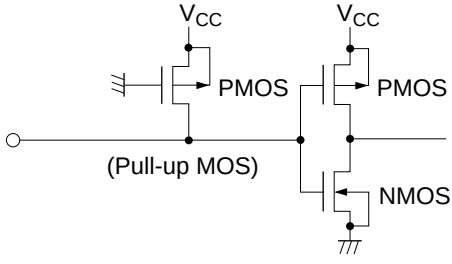
12. Applied to $\overline{SYNC}$, DB_0–DB_7, and RD_0–RD_7.

Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (without pull-up MOS)

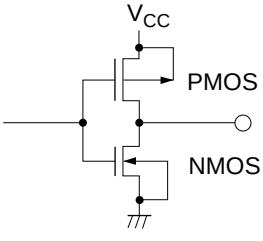


Applicable terminal: RD_0–RD_7 (with pull-up MOS)



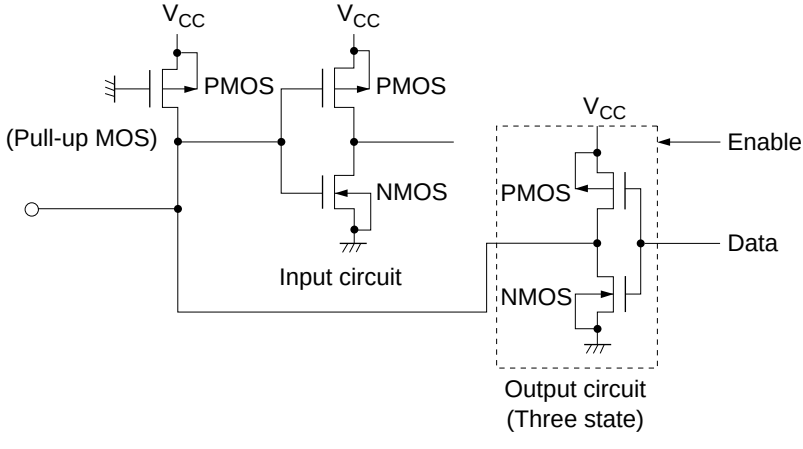
Output Terminal

Applicable terminal: CL_1, CL_2, MA, MB, FLM, D_1, D_2, $\overline{WE}$, CPO, MA_0–MA_{15}



I/O Common Terminal

Applicable terminal: DB_0–DB_7, $\overline{SYNC}$, MD_0–MD_7 (MD_0–MD_7 have no pull-up MOS)

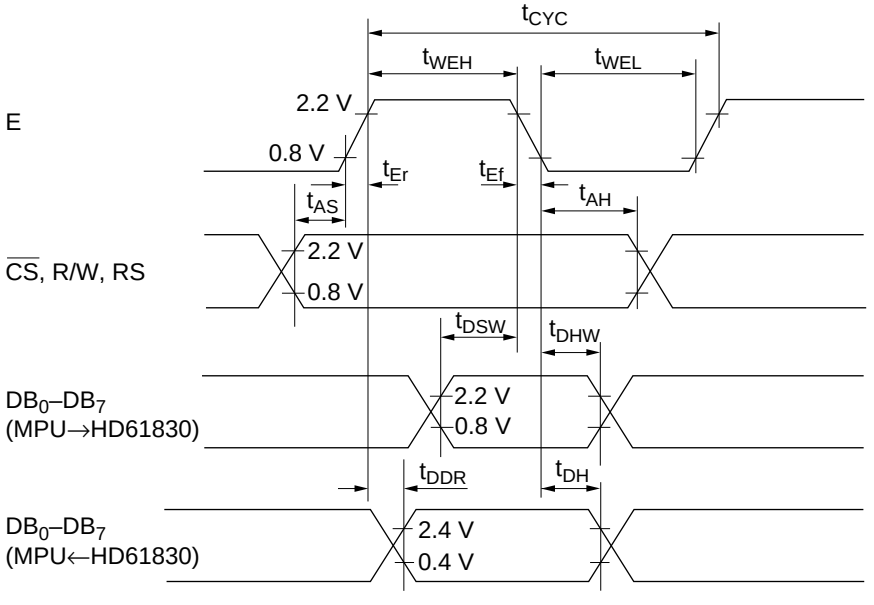


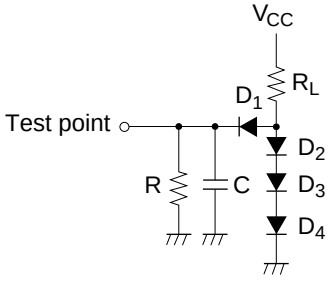
Timing Characteristics

HD61830 MPU Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	µs
Enable pulse width	High level	t_{WEH}	0.45	—	—	µs
	Low level	t_{WEL}	0.45	—	—	µs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns *
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Output data hold time		t_{DH}	20	—	—	ns

Note: * The following load circuit is connected for specification:

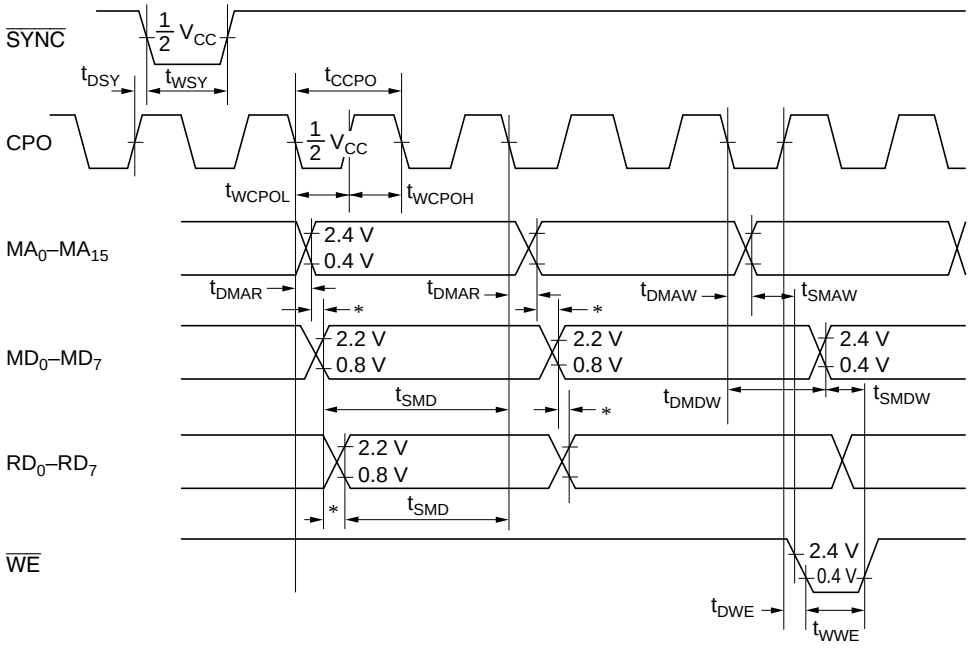




R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

HD61830 External RAM and ROM Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
$\overline{SYNC}$ delay time		t_{DSY}	—	—	200	ns
$\overline{SYNC}$ pulse width	Low level	t_{WSY}	900	—	—	ns
CPO cycle time		t_{CCPO}	900	—	—	ns
CPO pulse width	High level	t_{WCPOH}	450	—	—	ns
	Low level	t_{WCPOL}	450	—	—	ns
MA_0 to MA_{15} refresh delay time		t_{DMAR}	—	—	200	ns
MA_0 to MA_{15} write address delay time		t_{DMAW}	—	—	200	ns
MD_0 to MD_7 write data delay time		t_{DMDW}	—	—	200	ns
MD_0 to MD_7, RD_0 to RD_7 setup time		t_{SMD}	900	—	—	ns
Memory address setup time		t_{SMAW}	250	—	—	ns
Memory data setup time		t_{SMDW}	250	—	—	ns
$\overline{WE}$ delay time		t_{DWE}	—	—	200	ns
$\overline{WE}$ pulse width (low level)		t_{WWE}	450	—	—	ns

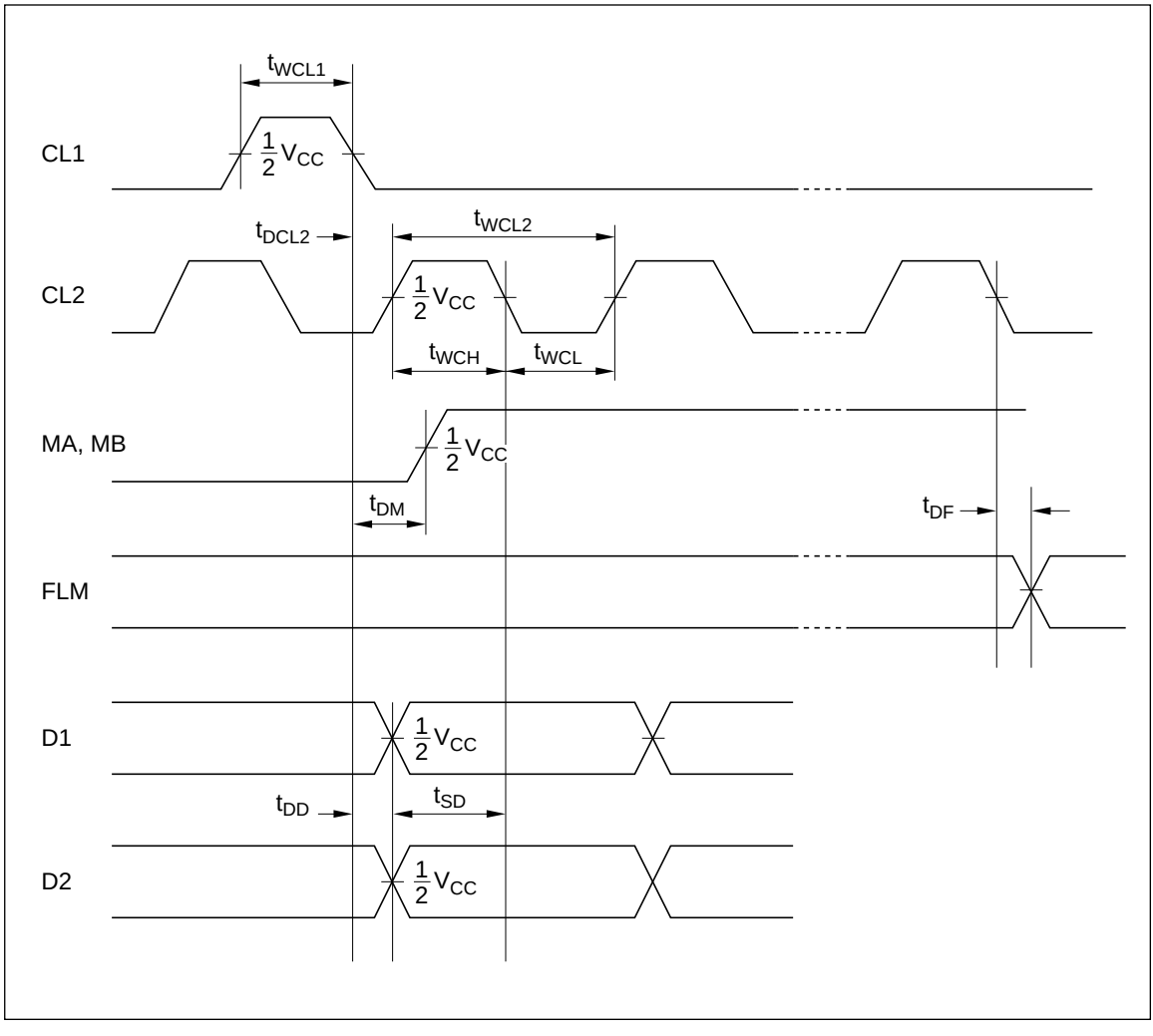


Notes: 1. No load is applied to all the output terminals.
2. "*" indicates the delay time of RAM and ROM.

HD61830 LCD Driver Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Clock pulse width (high level)		t_{WCL1}	450	—	—	ns
Clock delay time		t_{DCL2}	—	—	200	ns
Clock cycle time		t_{WCL2}	900	—	—	ns
Clock pulse width	High level	t_{WCH}	450	—	—	ns
	Low level	t_{WCL}	450	—	—	ns
MA, MB delay time		t_{DM}	—	—	300	ns
FLM delay time		t_{DF}	—	—	300	ns
Data delay time		t_{DD}	—	—	200	ns
Data setup time		t_{SD}	250	—	—	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D_1, and D_2).



HD61830B Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +0.7	V	1, 2
Terminal voltage	V_T	–0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. All voltage is referred to GND = 0 V.

2. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend that you use the LSIs within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

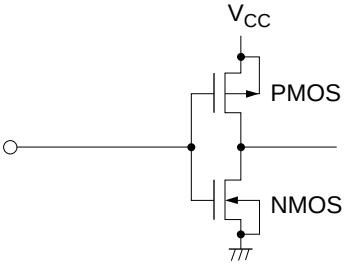
HD61830B Electrical Characteristics (V_{CC} = 5V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (TTL)	V_{IH}	2.2	—	V_{CC}	V		1
Input low voltage (TTL)	V_{IL}	0	—	0.8	V		2
Input high voltage	V_{IHR}	3.0	—	V_{CC}	V		3
Input high voltage (CMOS)	V_{IHC}	0.7 V_{CC}	—	V_{CC}	V		4
Input low voltage (CMOS)	V_{ILC}	0	—	0.3 V_{CC}	V		4
Output high voltage (TTL)	V_{OH}	2.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	5
Output low voltage (TTL)	V_{OL}	0	—	0.4	V	I_{OL} = 1.6 mA	5
Output high voltage (CMOS)	V_{OHC}	V_{CC} – 0.4	—	V_{CC}	V	$-I_{OH}$ = 0.6 mA	6
Output low voltage (CMOS)	V_{OLC}	0	—	0.4	V	I_{OI} = 0.6 mA	6
Input leakage current	I_{IN}	–5	—	5	µA	V_{IN} = 0 – V_{CC}	7
Three-state leakage current	I_{TSL}	–10	—	10	µA	V_{OUT} = 0 – V_{CC}	8
Pull-up current	I_{PL}	2	10	20	µA	V_{in} = GND	9
Power dissipation	P_W	—	—	50	mW	External clock f_{cp} = 2.4 MHz	10

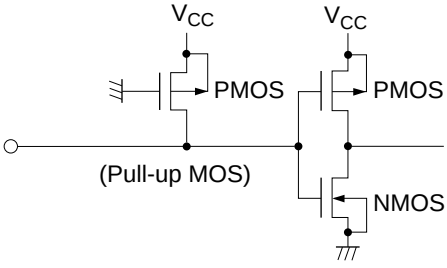
Notes:
1. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR, and $\overline{RES}$.
2. Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.
3. Applied to terminal $\overline{RES}$.
4. Applied to terminals $\overline{SYNC}$ and CR.
5. Applied to terminals DB_0–DB_7, $\overline{WE}$, MA_0–MA_{15}, $\overline{OE}$, $\overline{CE}$, and MD_0–MD_7.
6. Applied to terminals $\overline{SYNC}$, FLM, CL_1, CL_2, D_1, D_2, MA, and MB.
7. Applied to input terminals.
8. Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.
9. Applied to $\overline{SYNC}$, DB_0–DB_7, and RD_0–RD_7.
10. The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (without pull-up MOS)

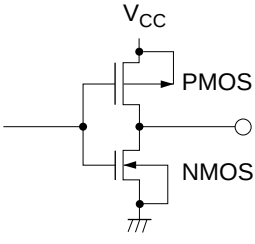


Applicable terminal: RD_0–RD_7 (with pull-up MOS)



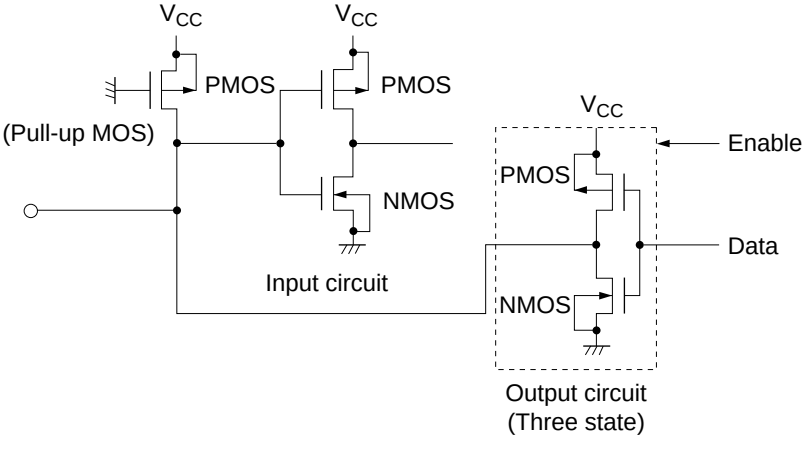
Output Terminal

Applicable terminal: CL_1, CL_2, MA, MB, FLM, D_1, D_2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA_0–MA_{15}



I/O Common Terminal

Applicable terminal: DB_0–DB_7, $\overline{SYNC}$, MD_0–MD_7 (MD_0–MD_7 have no pull-up MOS)

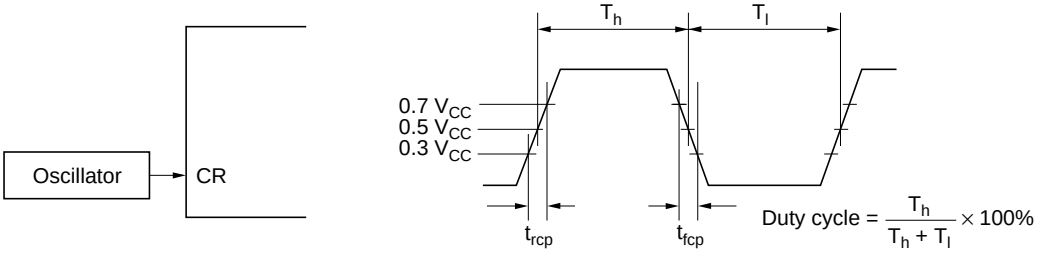


Timing Characteristics

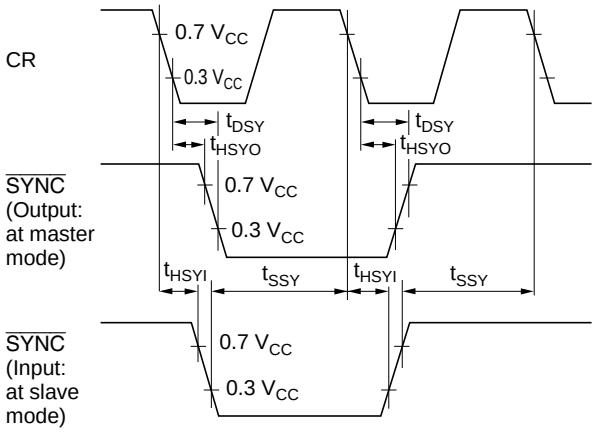
HD61830B Clock Operation (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
External clock operating frequency	f_{cp}	100	—	2400	kHz	1
External clock duty	Duty	47.5	50	52.5	%	1
External clock rise time	t_{rcp}	—	—	25.0	ns	1
External clock fall time	t_{fcp}	—	—	25.0	ns	1
$\overline{\text{SYNC}}$ output hold time	t_{HSYO}	30	—	—	ns	2, 3
$\overline{\text{SYNC}}$ output delay time	t_{DSY}	—	—	210	ns	2, 3
$\overline{\text{SYNC}}$ input hold time	t_{HSYI}	10	—	—	ns	2
$\overline{\text{SYNC}}$ input set-up time	t_{SSY}	—	—	180	ns	2

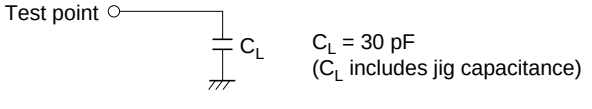
Notes: 1. Applied to external clock input terminal.



2. Applied to $\overline{\text{SYNC}}$ terminal.



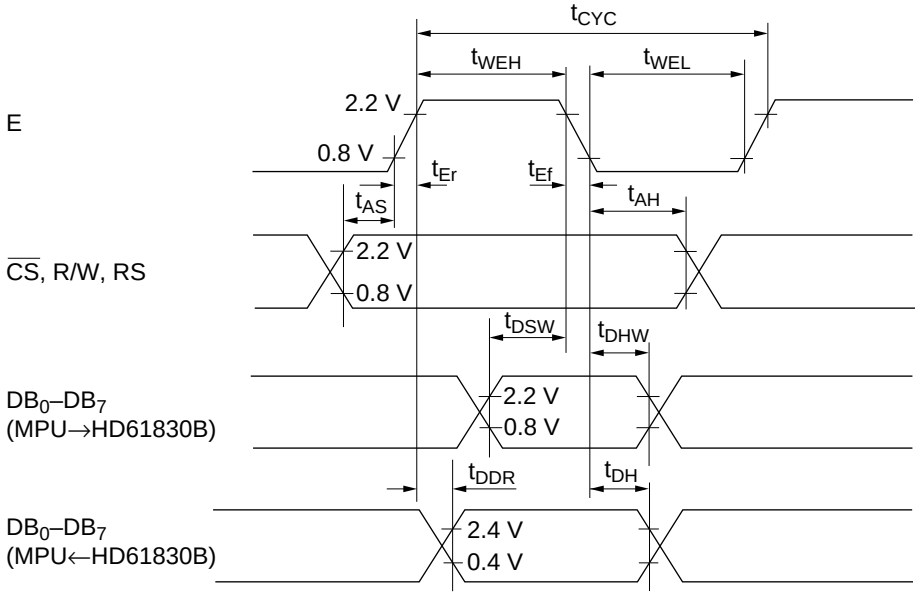
3. Testing load circuit.

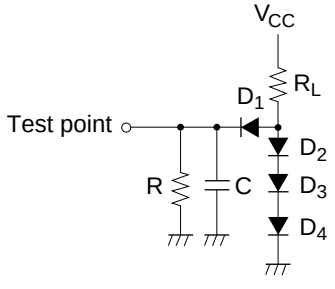


HD61830B MPU Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time		t_{CYC}	1.0	—	—	µs
Enable pulse width	High level	t_{WEH}	0.45	—	—	µs
	Low level	t_{WEL}	0.45	—	—	µs
Enable rise time		t_{Er}	—	—	25	ns
Enable fall time		t_{Ef}	—	—	25	ns
Setup time		t_{AS}	140	—	—	ns
Data setup time		t_{DSW}	225	—	—	ns
Data delay time		t_{DDR}	—	—	225	ns *
Data hold time		t_{DHW}	10	—	—	ns
Address hold time		t_{AH}	10	—	—	ns
Output data hold time		t_{DH}	20	—	—	ns

Note: * The following load circuit is connected for specification:



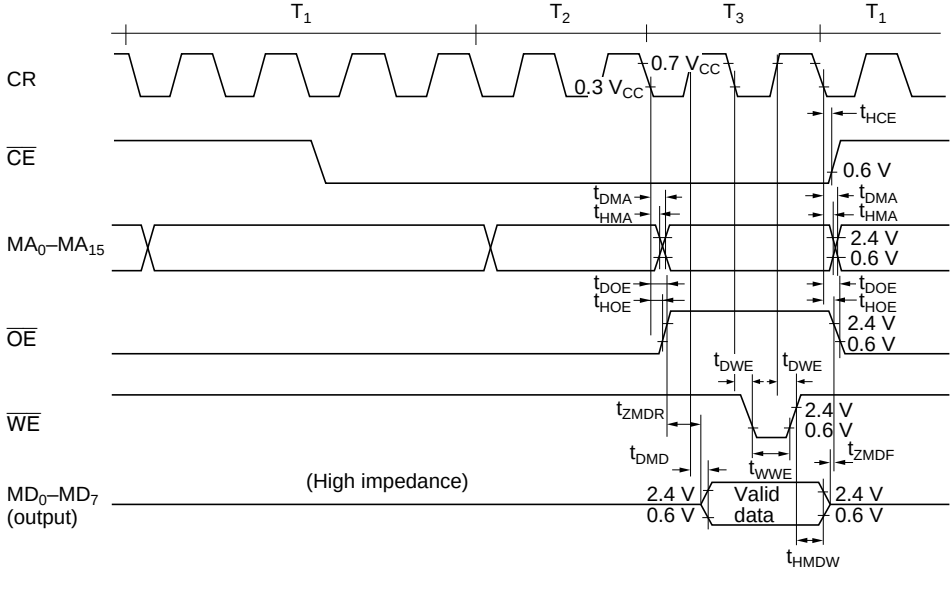


R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

HD61830B External RAM and ROM Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

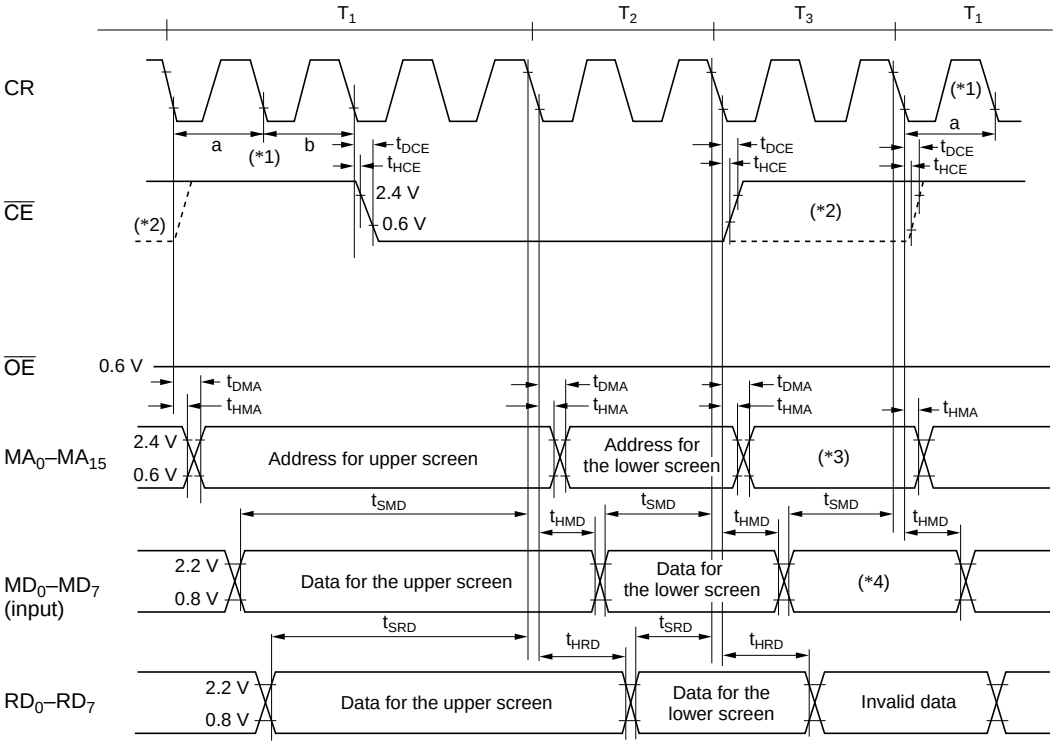
Item	Symbol	Min	Typ	Max	Unit	Notes
MA_0–MA_{15} delay time	t_{DMA}	—	—	300	ns	1, 2, 3
MA_0–MA_{15} hold time	t_{HMA}	40	—	—	ns	1, 2, 3
$\overline{CE}$ delay time	t_{DCE}	—	—	300	ns	1, 2, 3
$\overline{CE}$ hold time	t_{HCE}	40	—	—	ns	1, 2, 3
$\overline{OE}$ delay time	t_{DOE}	—	—	300	ns	1, 3
$\overline{OE}$ hold time	t_{HOE}	40	—	—	ns	1, 3
MD output delay time	t_{DMD}	—	—	150	ns	1, 3
MD output hold time	t_{HMDW}	10	—	—	ns	1, 3
$\overline{WE}$ delay time	t_{DWE}	—	—	150	ns	1, 3
$\overline{WE}$ clock pulse width	t_{WWE}	150	—	—	ns	1, 3
MD output high impedance time (1)	t_{ZMDF}	10	—	—	ns	1, 3
MD output high impedance time (2)	t_{ZMDR}	50	—	—	ns	1, 3
RD data set-up time	t_{SRD}	50	—	—	ns	2
RD data hold time	t_{HRD}	40	—	—	ns	2
MD data set-up time	t_{SMD}	50	—	—	ns	2
MD data hold time	t_{HMD}	40	—	—	ns	2

Notes: 1. RAM write timing



T1: Memory data refresh timing for upper screen
T2: Memory data refresh timing for lower screen
T3: Memory read/write timing

2. ROM/RAM read timing



*1 This figures shows the timing for H_p = 8.

For H_p = 7, time shown by “b” becomes zero. For H_p = 6, time shown by “a” and “b” become zero.

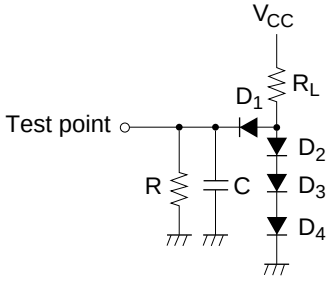
Therefore, the number of clock pulses during T1 become 4, 3, or 2 in the case of H_p = 8, H_p = 7, or H_p = 6 respectively.

*2 The waveform for instructions with memory read is shown with a dash line. In other cases, the waveform shown with a solid line is generated.

*3 When an instruction with RAM read/write is executed, the value of cursor address is output. In other cases, invalid data is output.

*4 When an instruction with RAM read is executed, HD61830B latches the data at this timing. In other cases, this data is invalid.

3. Test load circuit

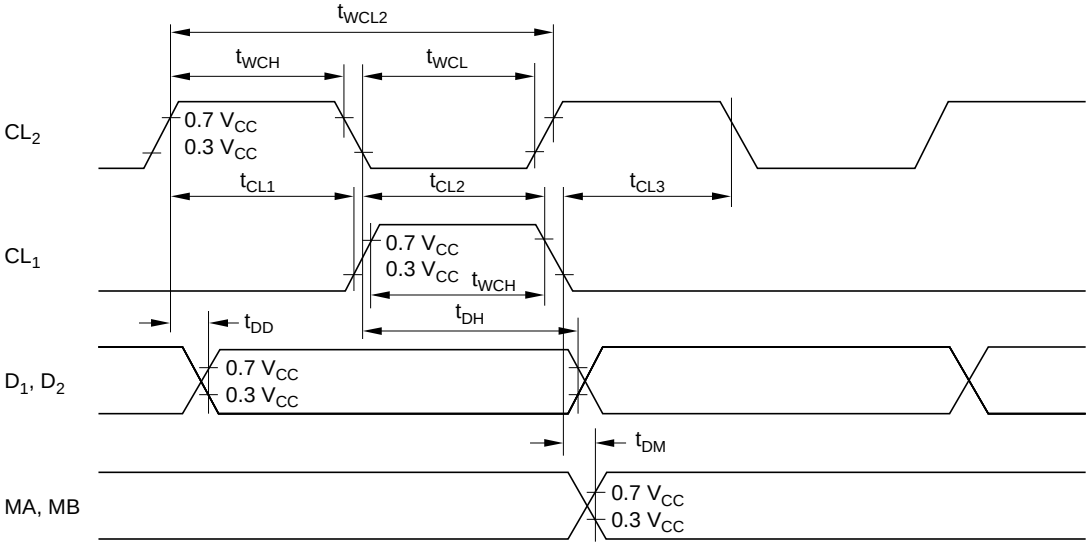


R_L = 2.4 kΩ
R = 11 kΩ
C = 50 pF (C includes jig capacitance)
Diodes D_1 to D_4: 1S2074Ⓗ

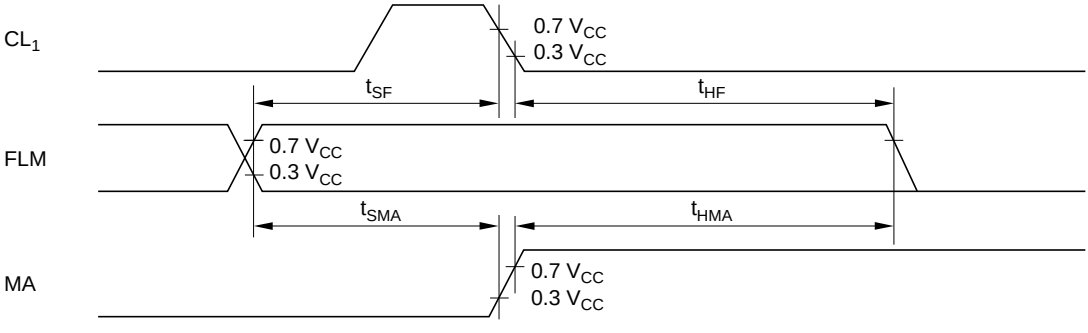
HD61830B LCD Driver Interface (V_{CC} = 5 V ±10%, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{WCL2}	416	—	—	ns	1, 3
Clock pulse width (high level)	t_{WCH}	150	—	—	ns	1, 3
Clock pulse width (low level)	t_{WCL}	150	—	—	ns	1, 3
Data delay time	t_{DD}	—	—	50	ns	1, 3
Data hold time	t_{DH}	100	—	—	ns	1, 3
Clock phase difference (1)	t_{CL1}	100	—	—	ns	1, 3
Clock phase difference (2)	t_{CL2}	100	—	—	ns	1, 3
Clock phase difference (3)	t_{CL3}	100	—	—	ns	1, 3
MA, MB delay time	t_{DM}	–200	—	200	ns	1, 3
FLM set-up time	t_{SF}	400	—	—	ns	2, 3
FLM hold time	t_{HF}	1000	—	—	ns	2, 3
MA set-up time	t_{SMA}	400	—	—	ns	2, 3
MA hold time	t_{HMA}	1000	—	—	ns	2, 3

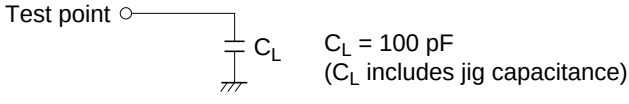
Notes: 1.



2.



3. Test load circuit



HD63645/HD64645/HD64646

LCTC (LCD Timing Controller)

HITACHI

Description

The HD63645/HD64645/HD64646 LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The HD64646 LCTC is a modified version of the HD64645 LCTC with different LCD interface timing.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD66204 (column driver) and the HD66205 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Features

- Software compatible with the HD6845 CRTC
- Programmable screen size
  - — Up to 1024 dots (height)
  - — Up to 4096 dots (width)
- High-speed data transfer
  - — Up to 20 Mbits/s in character mode
  - — Up to 40 Mbits/s in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font
  - — 1-32 dots (height)
  - — 8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical Smooth Scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver
  - — HD66204, HD66214T, HD66224T and HD66110ST (column)
  - — HD66205 and HD66215T (common)
  - — HD66106F and HD66107T (column/common)
- CPU interface
  - — 68 family HD63645
  - — 80 family HD64645, HD64646
- CMOS process
- Single +5 V ±10%

Hitachi semiconductor

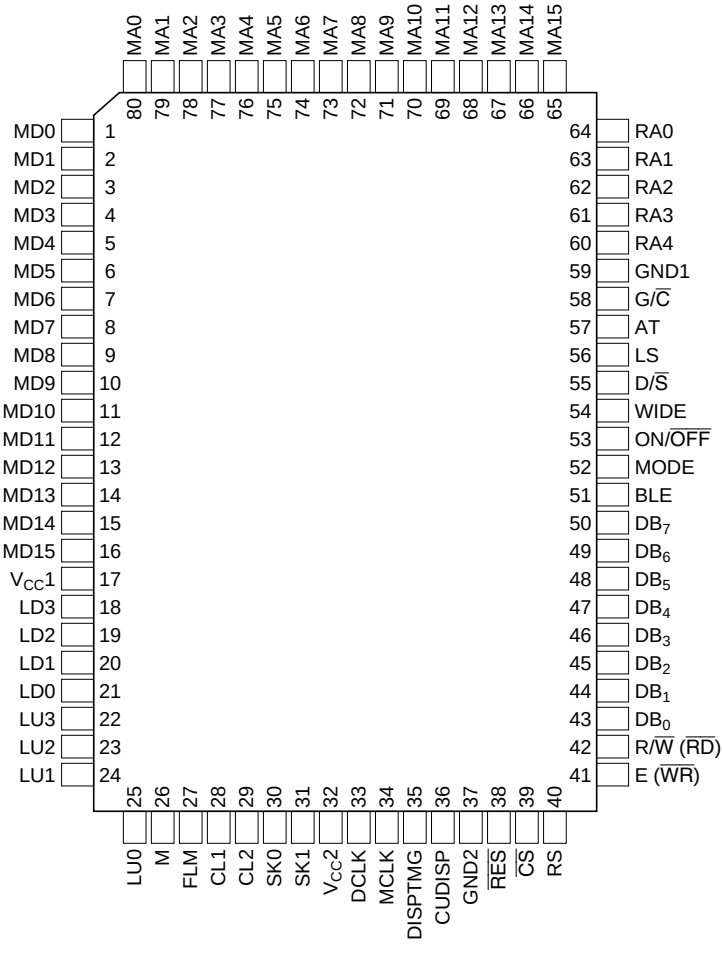
Differences between Products HD63645, HD64645 and HD64646

	HD63645	HD64645	HD64646
CPU interface	68 family	80 family	80 family
Bus timing	2 MHz	4 MHz	4 MHz
Pin arrangement and signal name	Pin 41: R/W Pin 42: E	Pin 41: $\overline{RD}$ Pin 42: $\overline{WR}$	Pin 41: $\overline{RD}$ Pin 42: $\overline{WR}$
Other	—	—	Modified LCD driver interface timing

Ordering Information

Type No.	CPU Interface	Package
HD63645F	68 family 2 MHz bus	80-pin plastic QFP (FP-80)
HD64645F	80 family 4 MHz bus	
HD64646FS	80 family 4 MHz bus	80-pin plastic QFP (FP-80B)

Pin Arrangement



(Top view)

Note: ( ) is for HD64645 and HD64646

Pin Description

Symbol	Pin Number	I/O	Name
$V_{CC}1$, $V_{CC}2$	17, 32	—	V_{CC}
GND1, GND2	37, 59	—	Ground
LU0–LU3	22–25	O	LCD up panel data 0–3
LD0–LD3	18–21	O	LCD down panel data 0–3
CL1	28	O	Clock one
CL2	29	O	Clock two
FLM	27	O	First line marker
M	26	O	M
MA0–MA15	65–80	O	Memory address 0–15
RA0–RA4	60–64	O	Raster address 0–4
MD0–MD7	1–8	I	Memory Data 0–7
MD8–MD15	9–16	I	Memory Data 8–15
DB_0–DB_7	43–50	I/O	Data bus 0–7
$\overline{CS}$	39	I	Chip select
E	41	I	Enable (HD63645 only)
R/$\overline{W}$	42	I	Read/write (HD63645 only)
$\overline{WR}$	41	I	Write (HD64645 and HD64646)
$\overline{RD}$	42	I	Read (HD64645 and HD64646)
RS	40	I	Register select
$\overline{RES}$	38	I	Reset
DCLK	33	I	D clock
MCLK	34	O	M clock
DISPTMG	35	O	Display timing
CUDISP	36	O	Cursor display
SK0	30	I	Skew 0
SK1	31	I	Skew 1
ON/$\overline{OFF}$	53	I	On/off
BLE	51	I	Blink enable
AT	57	I	Attribute
G/$\overline{C}$	58	I	Graphic/character
WIDE	54	I	Wide
LS	56	I	Large screen
D/$\overline{S}$	55	I	Dual/single
MODE	52	I	Mode

Pin Functions

Power Supply ($V_{CC}1$, $V_{CC}2$, GND)

Power Supply Pin (+5 V): Connect $V_{CC}1$ and $V_{CC}2$ with +5 V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0 V.

LCD Interface

LCD Up Panel Data (LU0–LU3), LCD Down Panel Data (LD0–LD3): LU0–LU3 and LD0–LD3 output LCD data as shown in table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0–MA15): MA0–MA15 supply the display memory address.

Raster Address (RA0–RA4): RA0–RA4 supply the raster address.

Memory Data (MD0–MD7): MD0–MD7 receive the character dot data or bit-mapped data.

Memory Data (MD8–MD15): MD8–MD15 receive attribute code data or bit-mapped data.

MPU Interface

Data Bus (DB0–DB7): DB0–DB7 send/receive data as a three-state I/O common bus.

Chip Select (CS): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock (HD63645 only).

Read/Write (R/$\overline{W}$): R/$\overline{W}$ enables MPU read of the LCTC internal registers when R/$\overline{W}$ is high, and MPU write when low (HD63645 only).

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write strobe (HD64645 and HD64646).

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read strobe (HD64645 and HD64646).

Register Select (RS): RS selects registers. (Refer to table 4.)

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Table 1 LCD Up Panel Data and LCD Down Panel Data

	Single Screen		
Pin Name	**4-Bit Data**	**8-Bit Data**	**Dual Screen**
LU0–LU3	Data output	Data output	Data output for upper screen
LD0–LD3	Disconnected	Data output	Data output for lower screen

Cursor Display (CUDISP): CUDISP supplies cursor display timing; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to table 2.

Mode Select

The mode select pins ON/$\overline{\text{OFF}}$, BLE, AT, G/$\overline{\text{C}}$, and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{\text{OFF}}$): ON/$\overline{\text{OFF}}$ switches display on and off (high = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{\text{C}}$): G/$\overline{\text{C}}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to table 10.

Dual/Single (D/$\overline{\text{S}}$): D/$\overline{\text{S}}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to table 8.)

Table 2 Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Prohibited combination

Function Overview

LCD and CRT Display Systems

Figure 1 shows a system using both LCD and CRT displays.

Main Features of HD63645/HD64645/HD64646

Main features of the LCTC are:

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3 Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen format	• Programmable horizontal scanning cycle by the character clock period • Programmable multiplexing duty ratio from static up to 1/512 • Programmable number of vertical displayed characters • Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor control	• Programmable cursor display position, corresponding to RAM address • Programmable cursor height by setting display start/end rasters • Programmable blink rate, 1/32 or 1/64 frame rate
	Memory rewriting	• Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory addressing	• 16-bit memory address output, up to 64 kbytes × 2 memory accessible • DRAM refresh address output
	Paging and scrolling	• Paging by updating start address • Horizontal scrolling by the character, by setting horizontal virtual screen width • Vertical smooth scrolling by updating display start raster
	Character attributes	• Reverse video, blinking, nondisplay (white or black), display ON/OFF
Application	CRTC compatible	• Facilitates system replacement of CRT display with LCD
	OR function	• Enables superimposing display of character screen and graphic screen
Configuration	LCTC configuration	• Single 5 V power supply • I/O TTL compatible except $\overline{\text{RES}}$, MODE, SK0, SK1 • Bus connectable with 6800 family (HD63645) • Bus connectable with 80 family (HD64645 and HD64646) • CMOS process • Internal logic fully static • 80-pin flat plastic package

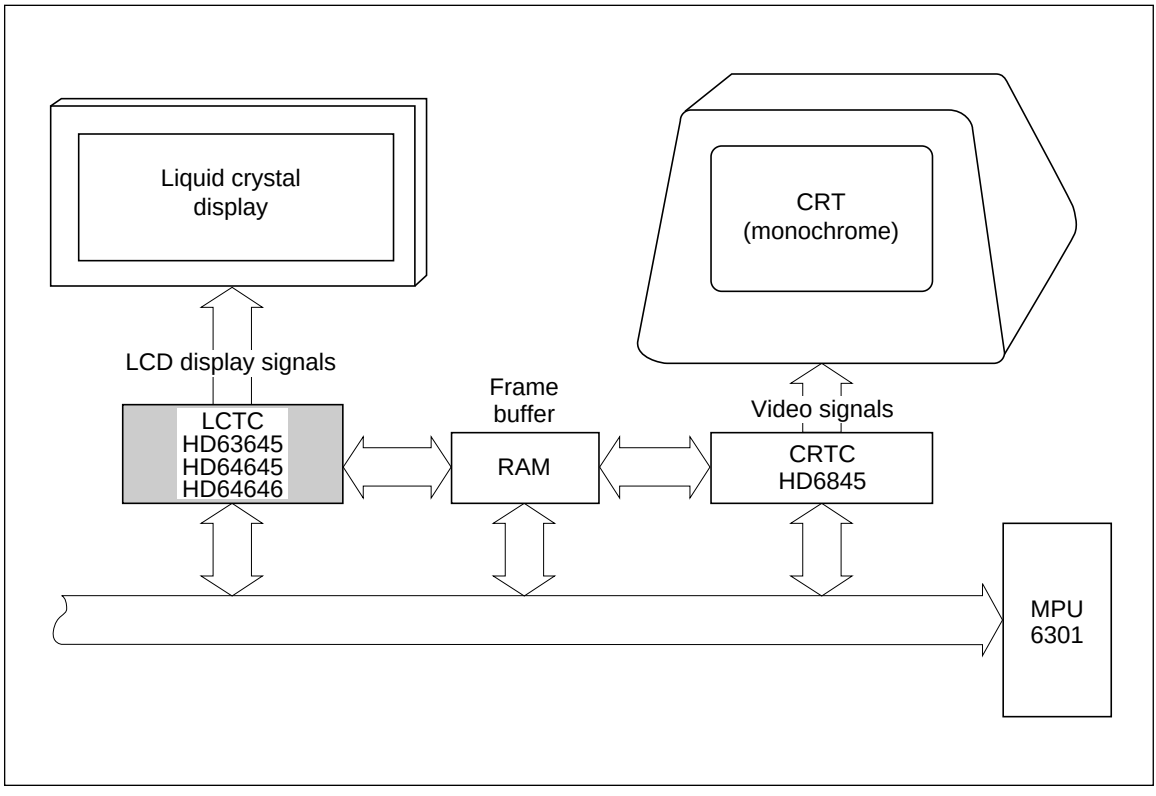

Liquid crystal
display
CRT
(monochrome)
LCD display signals
Frame
buffer
Video signals
LCTC
HD63645
HD64645
HD64646
RAM
CRTC
HD6845
MPU
6301

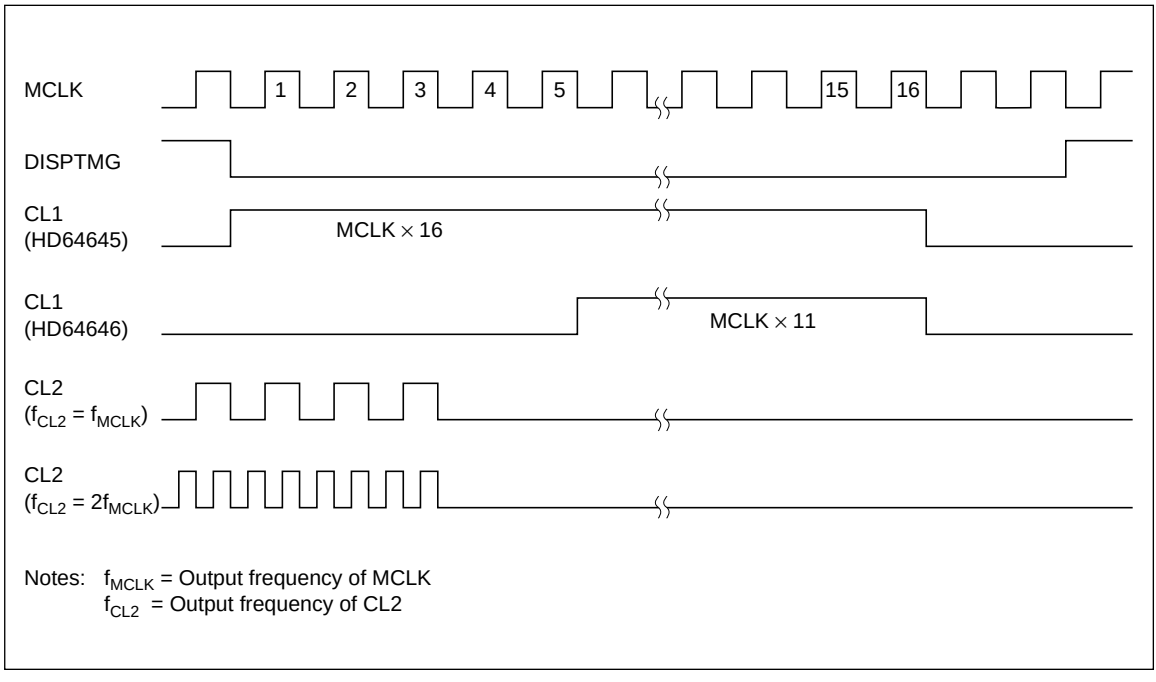
Figure 1 LCD and CRT Displays

Differences between HD64645 and HD64646

Figure 2 and figure 3 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Figure 2 shows the case without skew function and figure 3 shows the case with skew function.

In figure 2, high period between CL2 and CL1 of HD64645 overlap. HD64646 has no overlap like HD64645, and except for this overlap. HD64646 is the same as HD64645 functionally.

Also for the skew function, phase relation between CL1 and CL2 changes. As figure 3 shows, data transfer period and CL1 high period of HD64646 never overlap with the skew function.



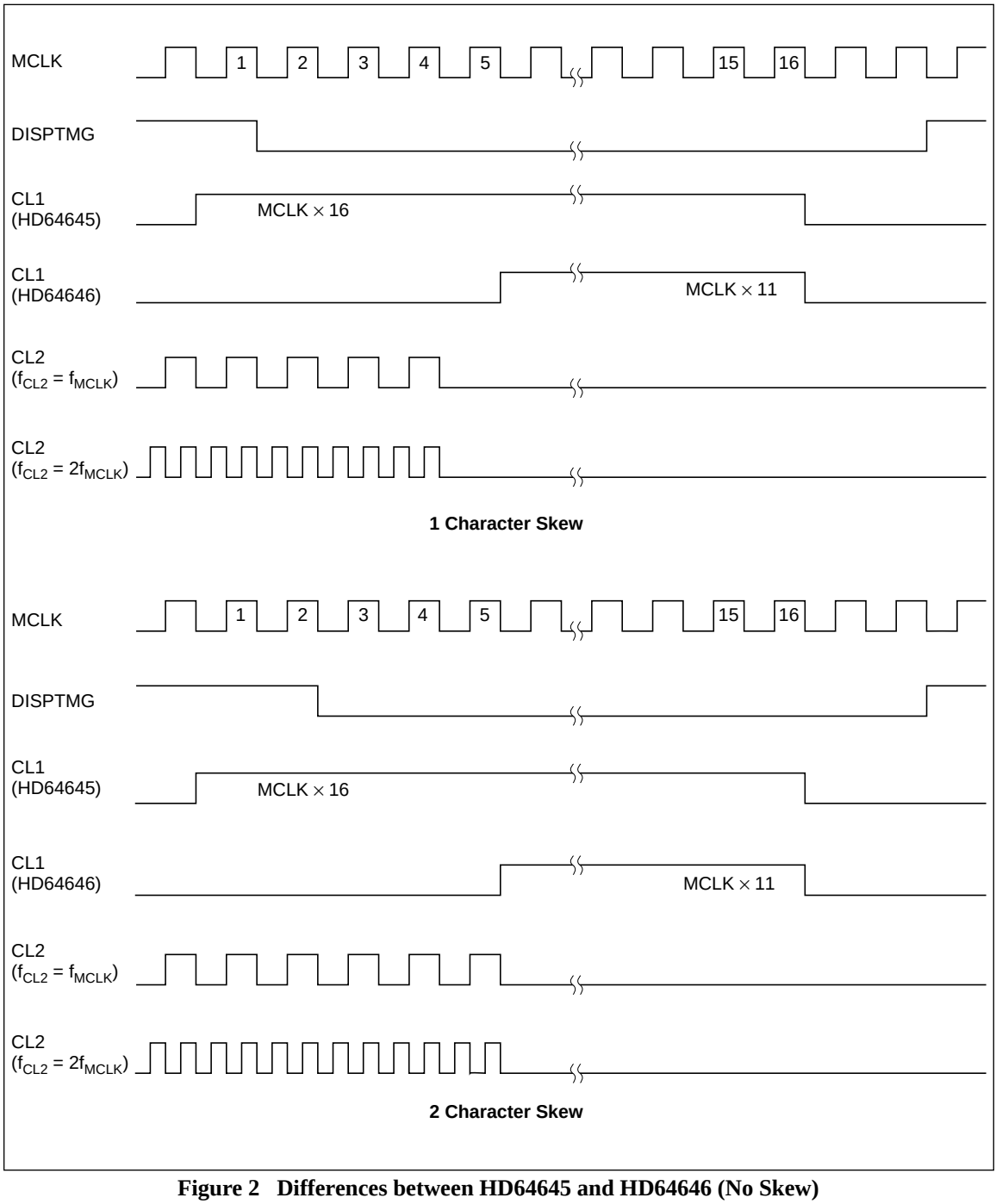
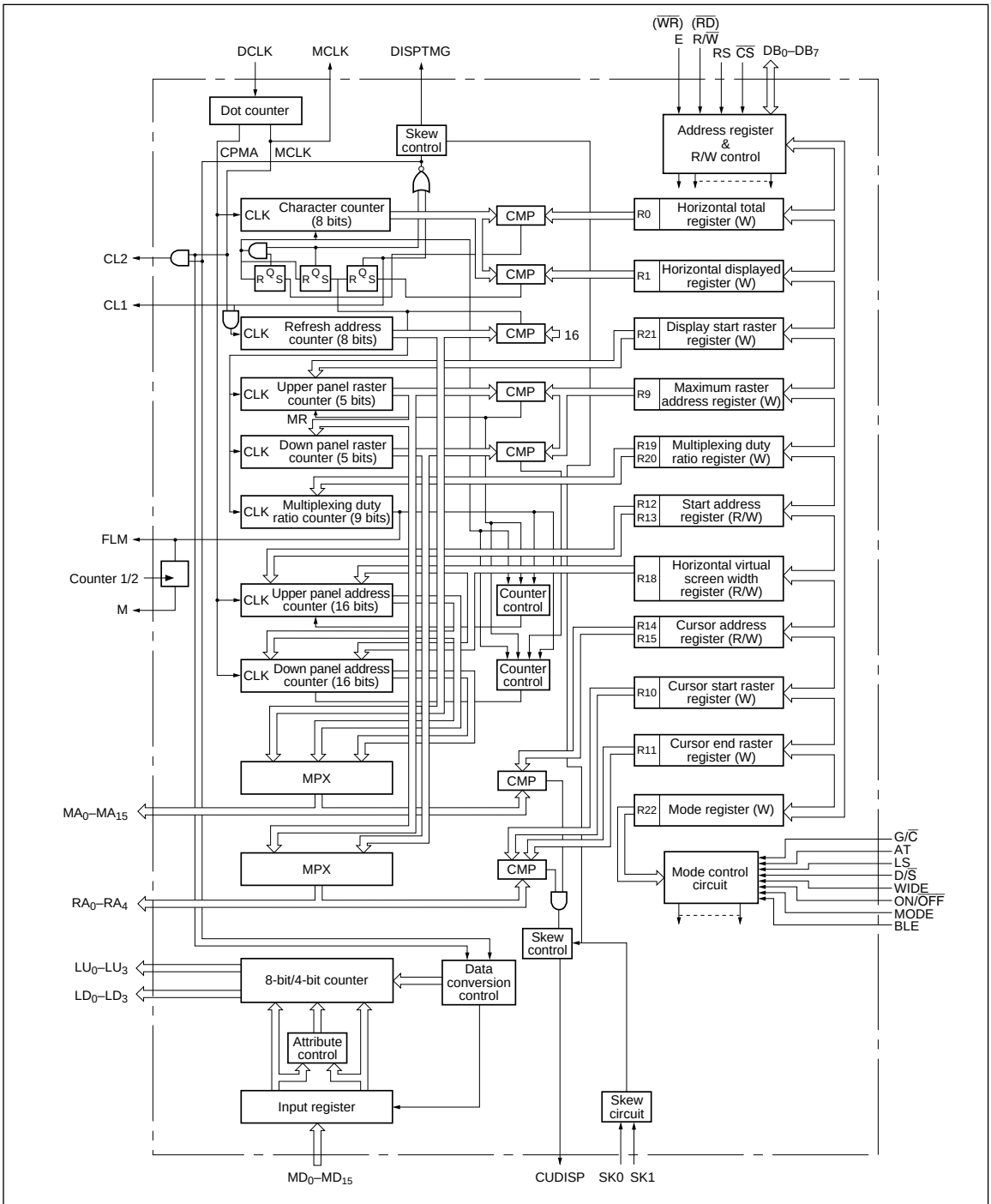


Figure 2 Differences between HD64645 and HD64646 (No Skew)

Figure 3 Differences between HD64645 and HD64646 (Skew)

Internal Block Diagram

Figure 4 is a block diagram of the LCTC.

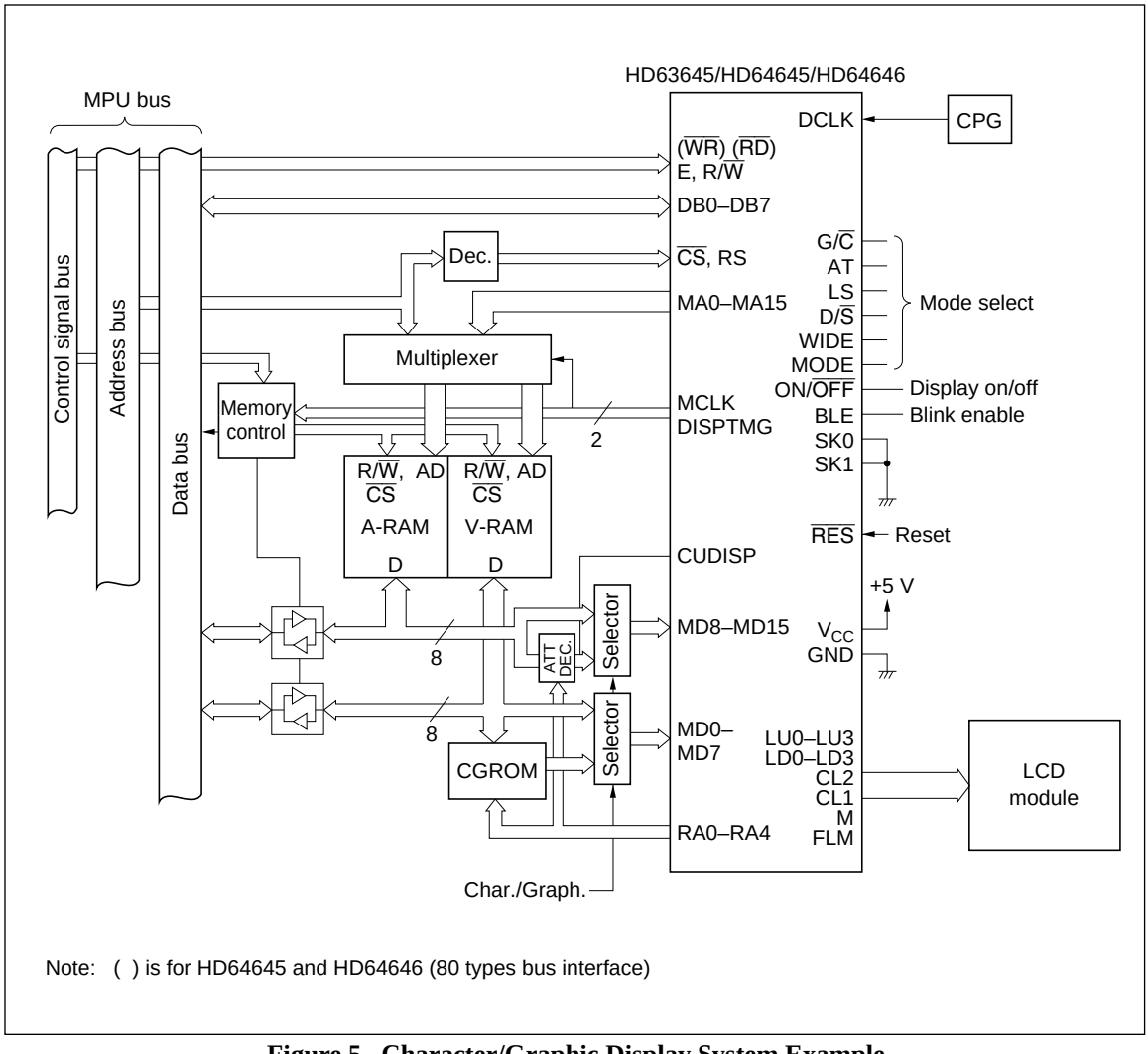


Note: ( ) is for HD64645 and HD64646 (80 types bus interface)

Figure 4 LCTC Block Diagram

System Block Configuration Examples

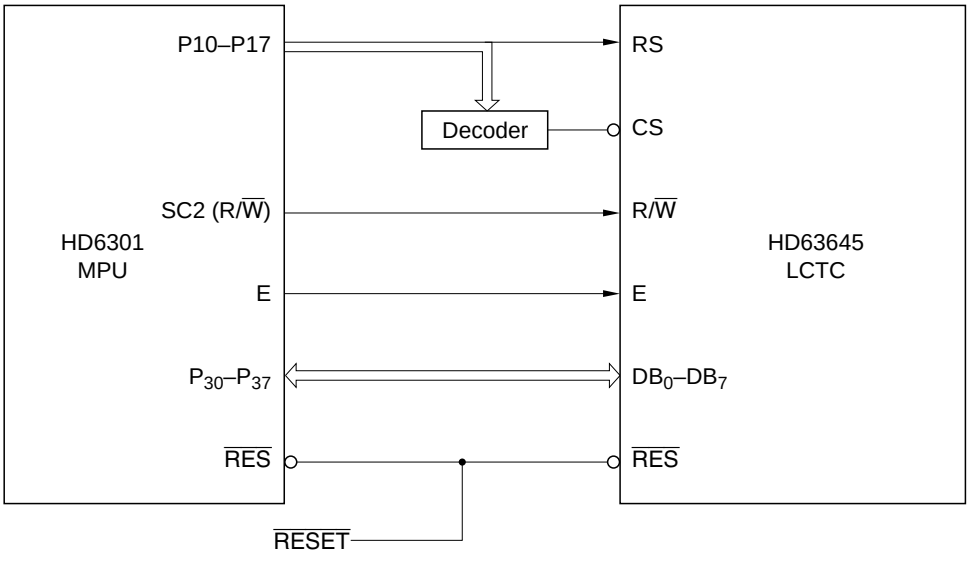
Figure 5 is a block diagram of a character/graphic display system. Figure 5 shows two examples using LCD drivers.



Note: ( ) is for HD64645 and HD64646 (80 types bus interface)

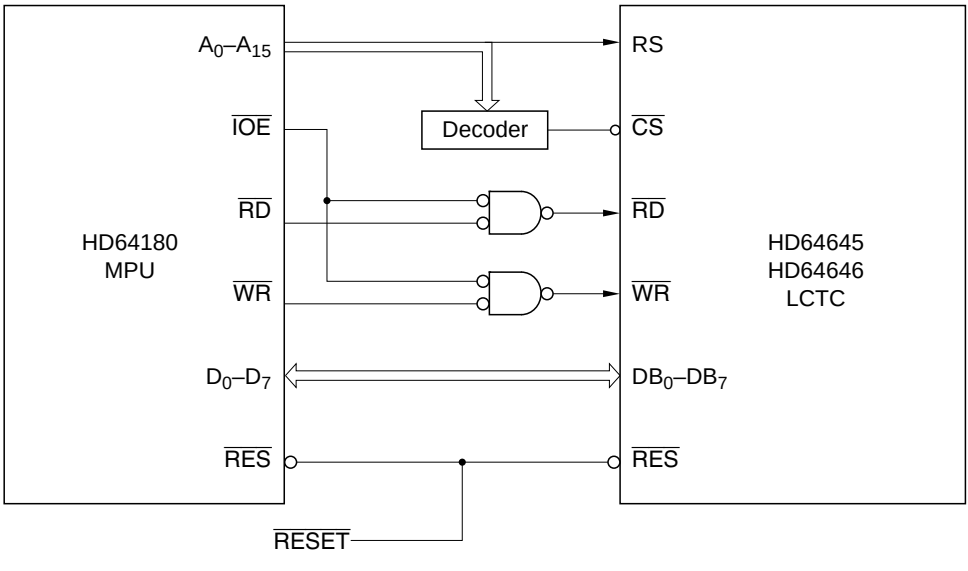
Figure 5 Character/Graphic Display System Example

Interface to MPU



Note: HD6301 is set in mode 5. P10–P17 are used as output ports, and P30–P37 as data buses. SC2 outputs R/$\overline{W}$ here.

Interface between HD6301 and HD63645



Note: In 80 family MPUs, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ORed signals of the interface signals and IOE. So $\overline{IOE}$ and $\overline{RD}$, and $\overline{IOE}$ and $\overline{WR}$ should be ORed to satisfy t_{AS}, the timing of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

Interface between HD64180, HD64645 and HD64646

Figure 6 Interface to MPU

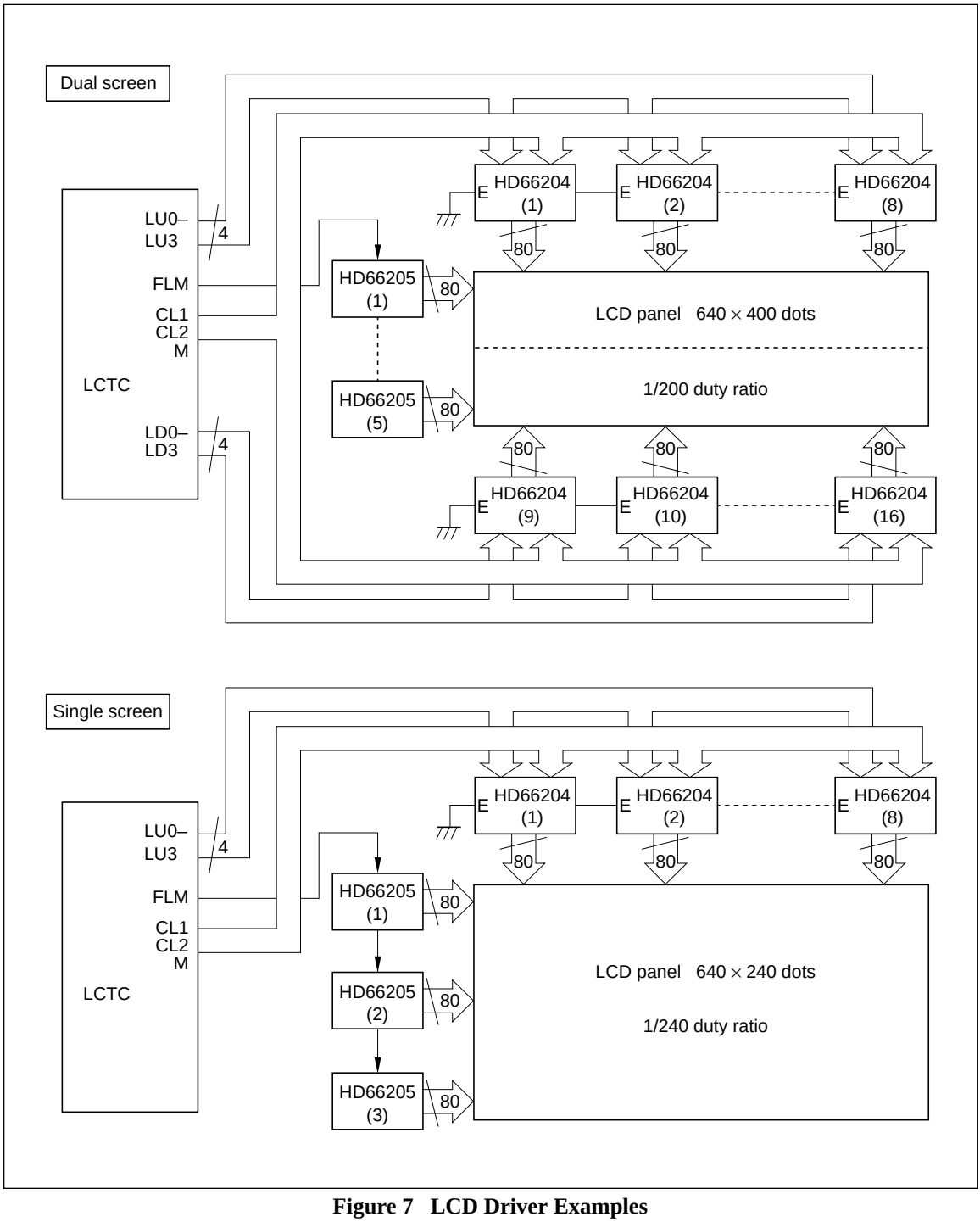


Figure 7 LCD Driver Examples

Registers

Table 4 shows the register mapping. Table 5 describes their function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4 Registers Mapping

		Address Register								Data Bit							
$\overline{CS}$	RS	4	3	2	1	0	Reg. No.	Register Name	Program Unit	Symbol	R/W	7	6	5	4	3	2	1	0
1	—	—	—	—	—	—		Invalid	—	—	—								
0	0	—	—	—	—	—	AR	Address Register	—	—	W								
0	1	0	0	0	0	0	R0	Horizontal total characters	Character*3	Nht	W								
0	1	0	0	0	0	1	R1	Horizontal displayed char.s	Character	Nhd	W								
0	1	0	1	0	0	1	R9	Maximum raster address	Raster	Nr	W								
0	1	0	1	0	1	0	R10	Cursor start raster	Raster*4	Ncs	W		B	P					
0	1	0	1	0	1	1	R11	Cursor end raster	Raster	Nce	W								
0	1	0	1	1	0	0	R12	Start address (H)	Memory address	—	R/W								
0	1	0	1	1	0	1	R13	Start address (L)	Memory address	—	R/W								
0	1	0	1	1	1	0	R14	Cursor address (H)	Memory address	—	R/W								
0	1	0	1	1	1	1	R15	Cursor address (L)	Memory address	—	R/W								
0	1	1	0	0	1	0	R18	Horizontal virtual screen width	Character	Nir	W								
0	1	1	0	0	1	1	R19	Multiplexing duty ratio (H)	Raster*3	Ndh	W								
0	1	1	0	1	0	0	R20	Multiplexing duty ratio (L)	Raster*3	Ndl	W								
0	1	1	0	1	0	1	R21	Display start raster	Raster	Nsr	W								
0	1	1	0	1	1	0	R22	Mode register	—*5	—	W				ON/OFF	G/C	WIDE	BLE	AT

Notes: 1. : Invalid data bits

2. R/W indicates whether write access or read access is enabled to/from each register.
   W: Only write accessible
   R/W: Both read and write accessible
3. The “value to be specified minus 1” should be programmed in these registers: R0, R1 and R20.
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below (for more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2–R8, R16, and R17 are not assigned for the LCTC. Programming to these registers will be ignored.

Table 5 Internal Register Description

Reg. No.	Register Name	Size (Bits)	Description
AR	Address register	5	Specifies the internal control registers (R0, R1, R9–R15, R18–R22) address to be accessed
R0	Horizontal total characters	8	Specifies the horizontal scanning period
R1	Horizontal displayed characters	8	Specifies the number of displayed characters per character row
R9	Maximum raster address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor start raster	5 + 2	Specifies the cursor start raster address and its blink mode
R11	Cursor end raster	5	Specifies the cursor end raster address
R12 R13	Start address (H) Start address (L)	16	Specify the display start address
R14 R15	Cursor address (H) Cursor address (L)	16	Specify the cursor display address
R18	Horizontal virtual screen width	8	Specifies the length of one row in memory space for horizontal scrolling
R19 R20	Multiplexing duty ratio (H) Multiplexing duty ratio (L)	9	Specify the number of rasters for one screen
R21	Display start raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode register	5	Controls the display mode

Note: For more details of registers, refer to “Internal Registers.”

Table 6 Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD63645/HD64645/HD64646	Comparison	CRTC HD6845
AR	Address register	Equivalent to CRTC	Address register
R0	Horizontal total characters		Horizontal total characters
R1	Horizontal displayed characters		Horizontal displayed characters
R2	—	Particular to CRTC; unnecessary for LCTC	Horizontal sync position
R3			Sync width
R4			Vertical total characters
R5			Vertical total adjust
R6			Vertical displayed characters
R7			Vertical sync position
R8			Interface and skew
R9	Maximum raster address	Equivalent to CRTC	Maximum raster address
R10	Cursor start raster		Cursor start raster
R11	Cursor end raster		Cursor end raster
R12	Start address (H)		Start address (H)
R13	Start address (L)		Start address (L)
R14	Cursor address (H)		Cursor (H)
R15	Cursor address (L)		Cursor (L)
R16		Particular to CRTC; unnecessary for LCTC	Light pen (H)
R17			Light pen (L)
R18	Horizontal virtual screen width	Additional registers for LCTC	
R19	Multiplexing duty ratio (H)		
R20	Multiplexing duty ratio (L)		
R21	Display start raster		
R22	Mode register		

Functional Description

Programmable Screen Format

Figure 8 illustrates the relation between LCD display screen and registers. Figure 9 shows a timing chart of signals output from the LCTC in mode 5 as an example.

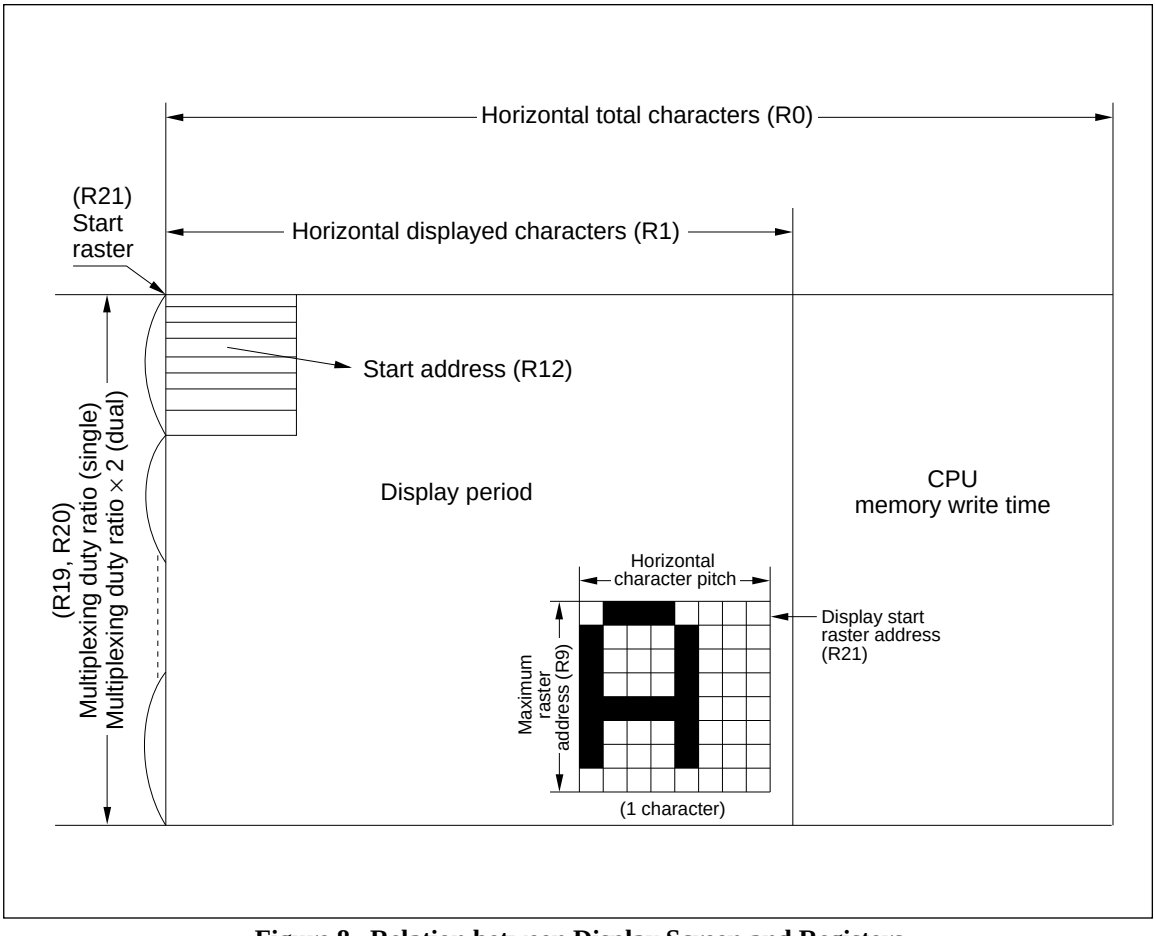
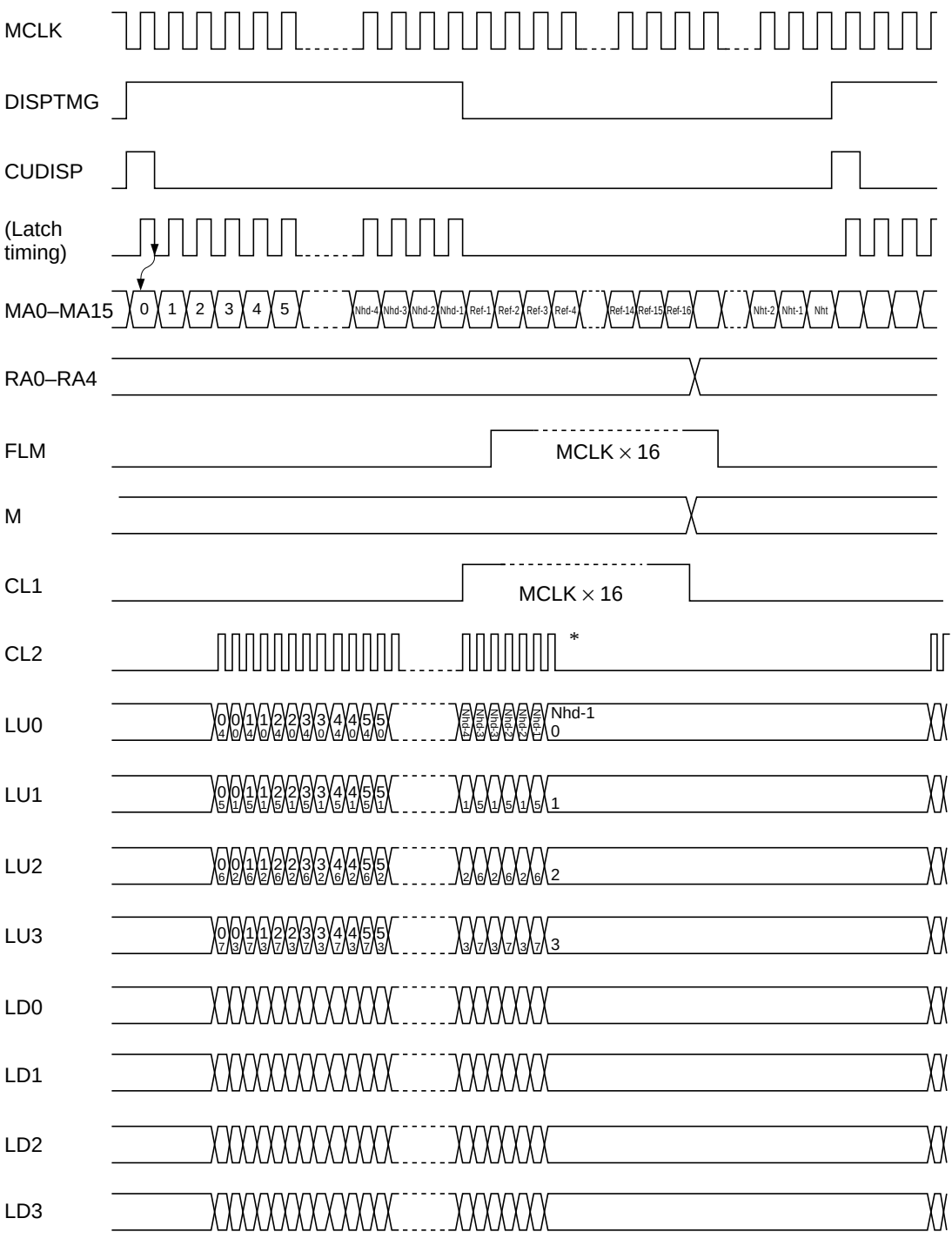


Figure 8 Relation between Display Screen and Registers



Note: * Relation between CL1 and CL2 in the case of HD64646 is difference from one shown in this chart. Refer to “Difference between HD64645 and HD64646.”

Figure 9 LCTC Timing Chart (In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (figure 10) can be controlled by programming specific registers.

- Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

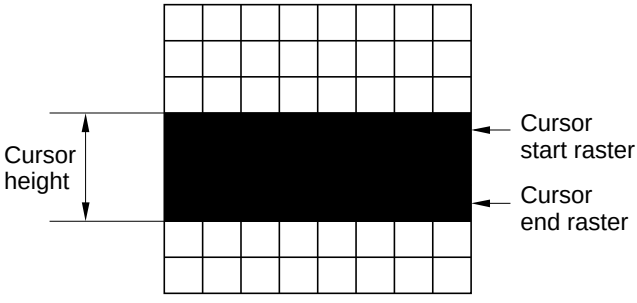


Figure 10 Cursor Display

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for a system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode: character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black), by storing the attribute data in attribute RAM (A-RAM).

Figure 11 illustrates the relation between character display screen and memory contents.

Graphic Mode 1: Graphic mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 12 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2: Graphic mode 2 utilizes software for a system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly the number of times specified by maximum raster register (R9). The raster address is output in the same way as in character mode.

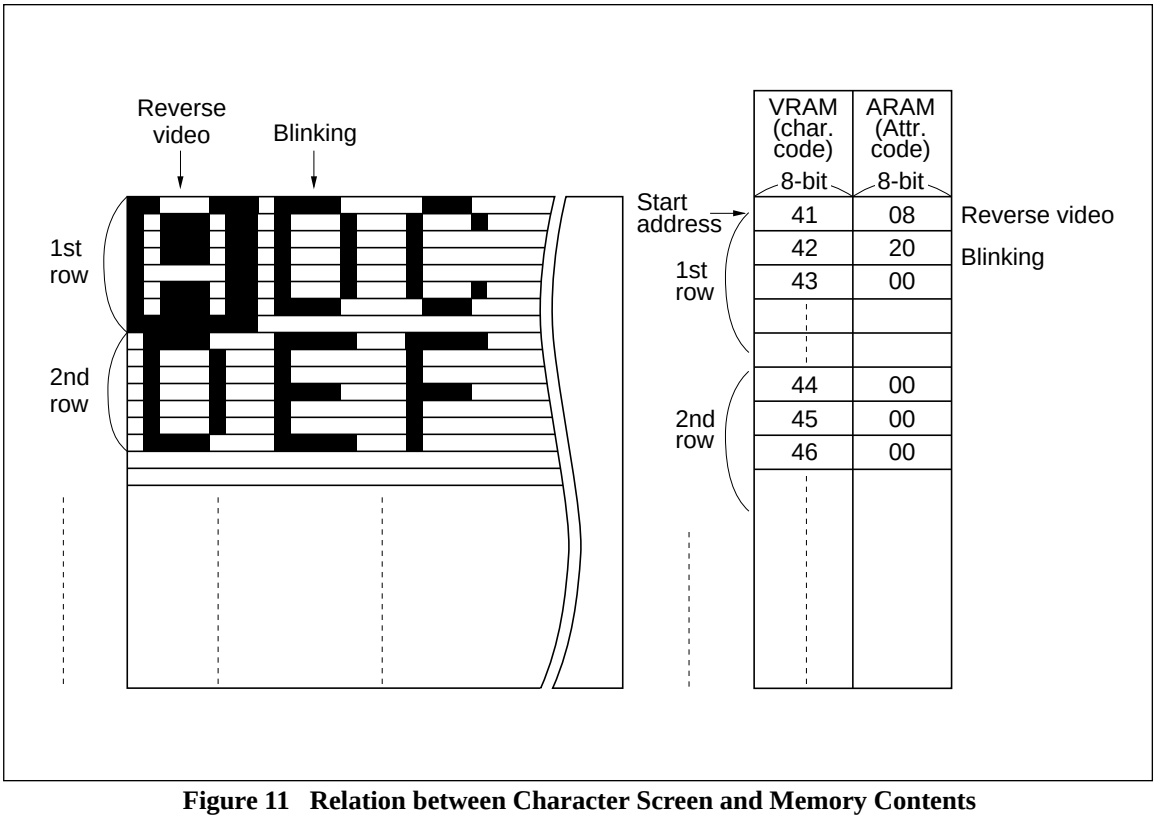


Figure 11 Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (figure 13).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 14 shows an example.

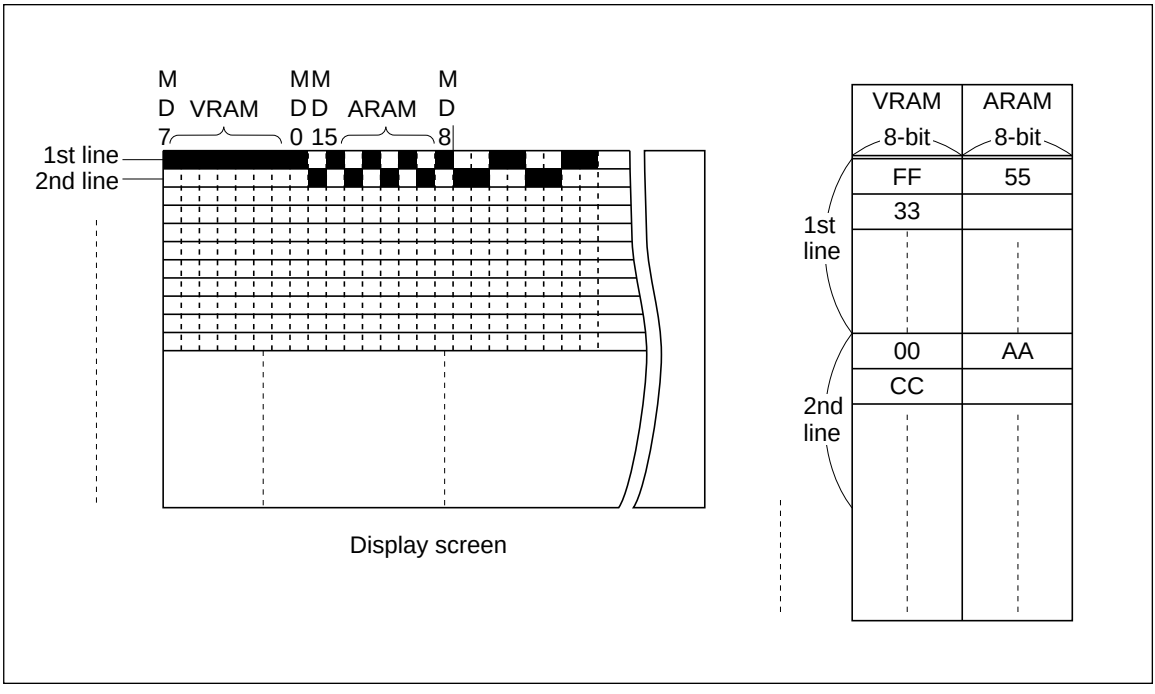


Figure 12 Relation between Graphic Screen and Memory Contents

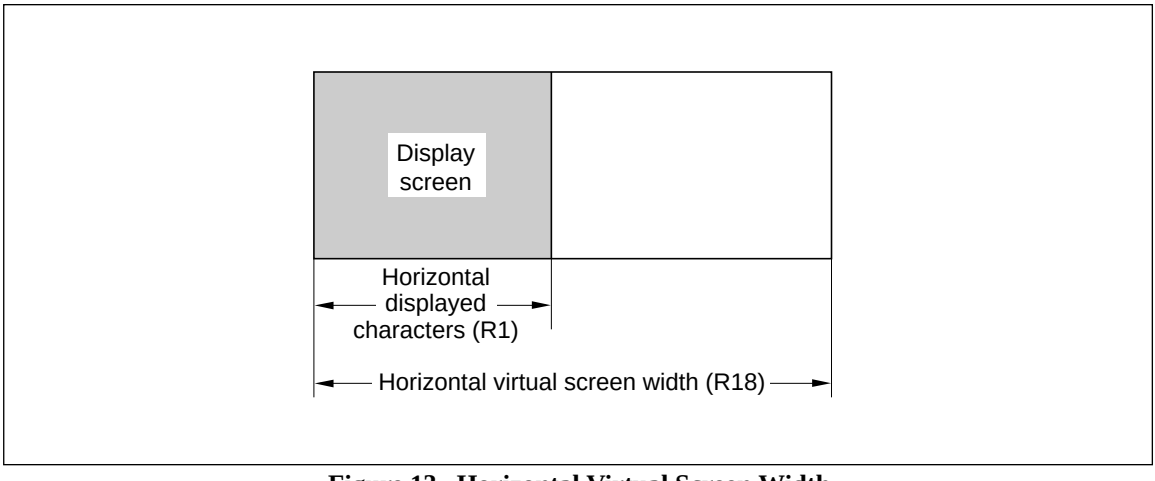


Figure 13 Horizontal Virtual Screen Width

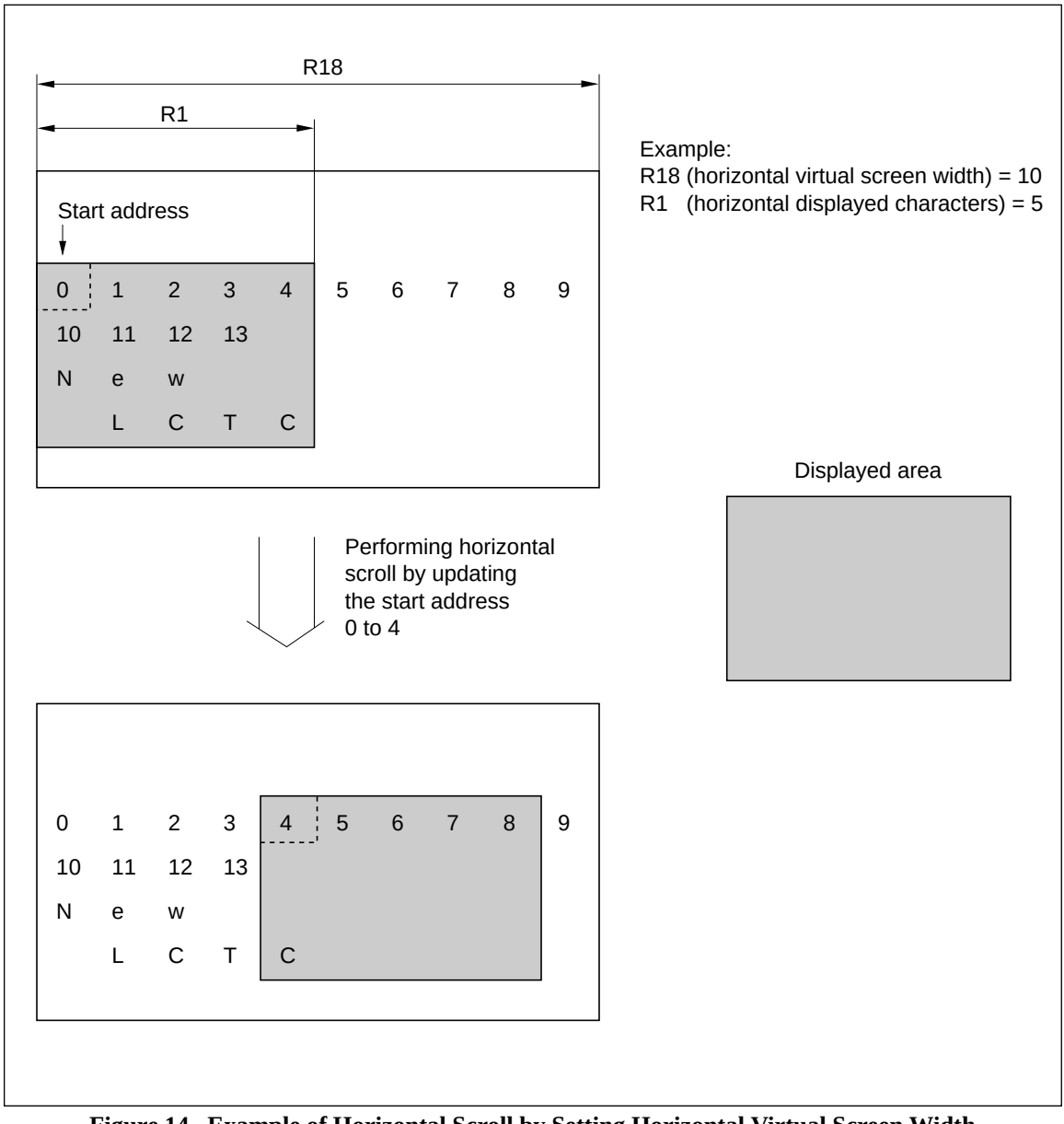


Figure 14 Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (figure 15) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (figure 16). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

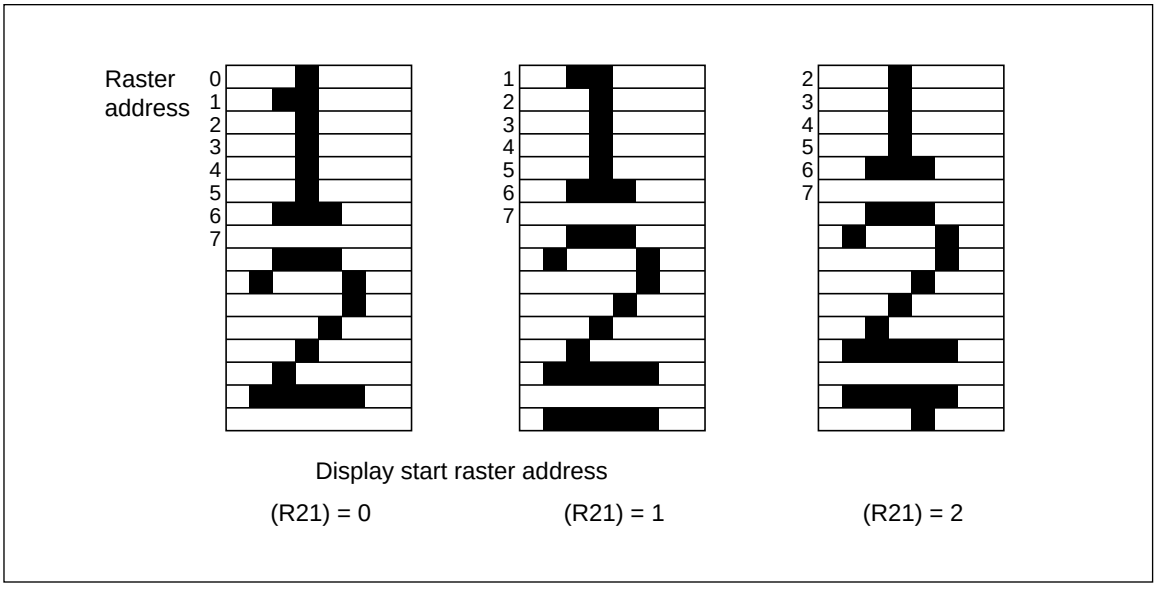


Figure 15 Example of Smooth Scroll by Setting Display Start Raster Address

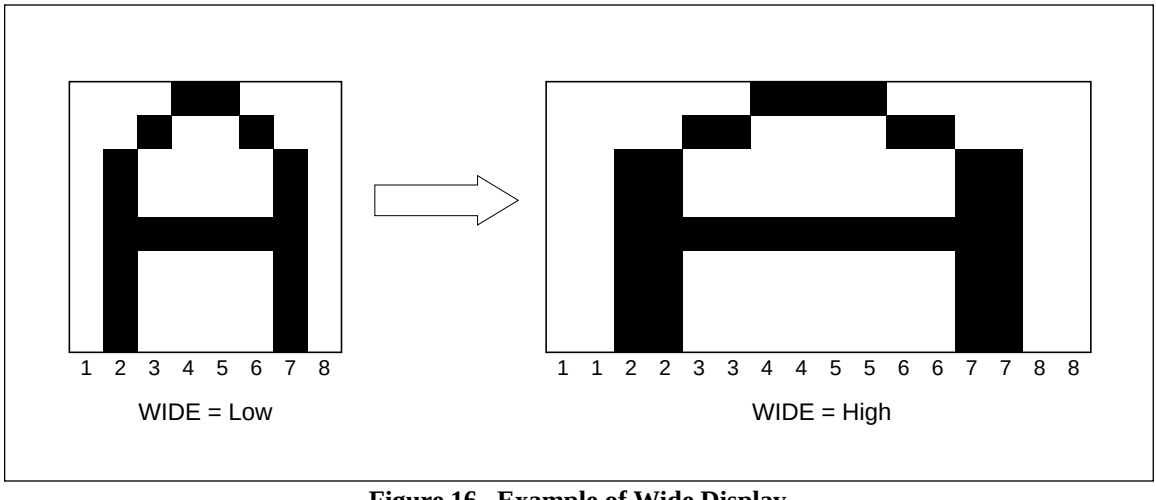


Figure 16 Example of Wide Display

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 17 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (R22) or the AT pin. As shown in figure 18, a character attribute can be specified by placing the character code on MD0–MD7, and the attribute code on MD11–MD15. MD8–MD10 are invalid.

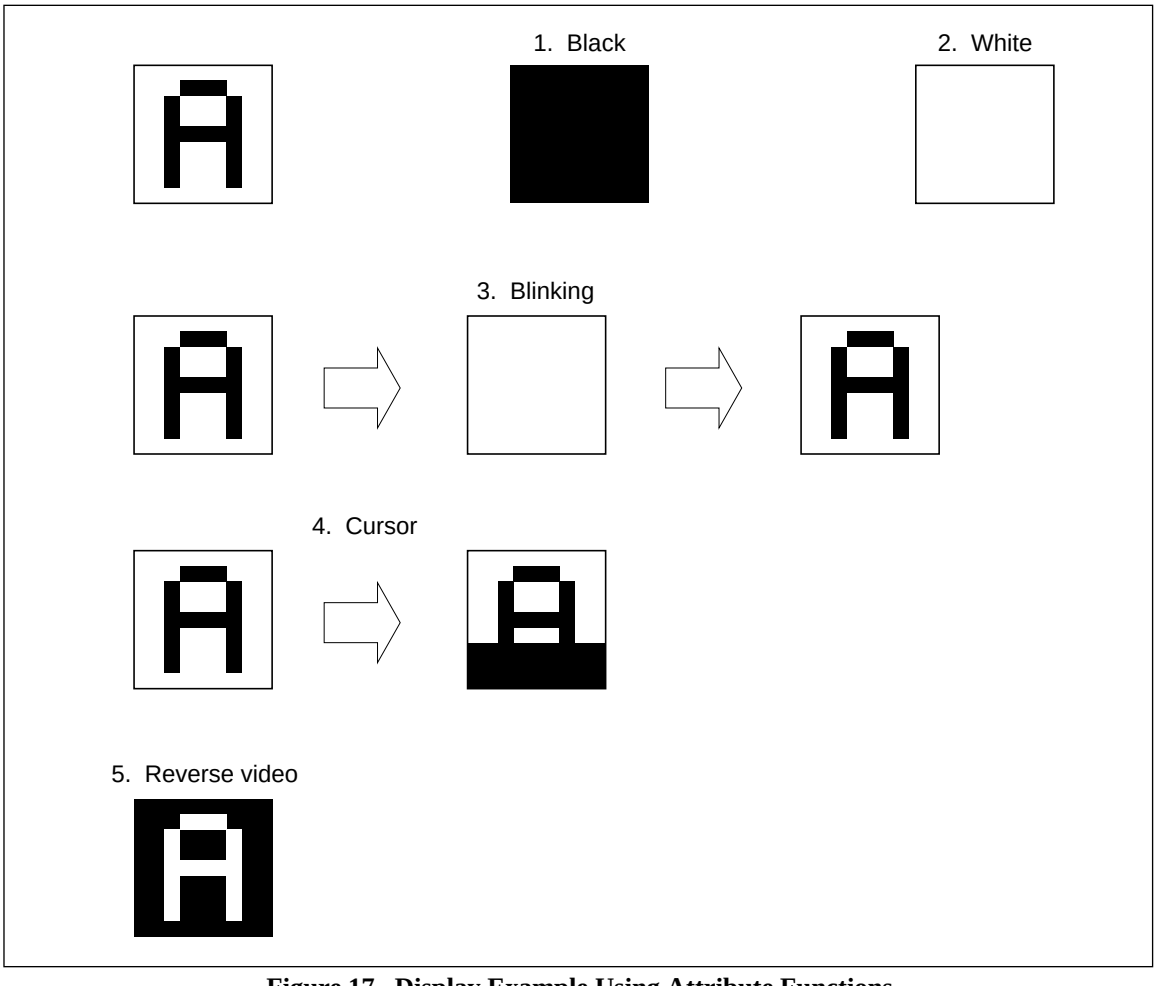


Figure 17 Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10–8	7–0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	***	Character code

Note: *** Invalid

Figure 18 Attribute Code

OR Function — Superimposing Characters and Graphics

The OR function (figure 19) generates the OR of the data entered into MD0–MD7 (e.g. character data) and the data into MD8–MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

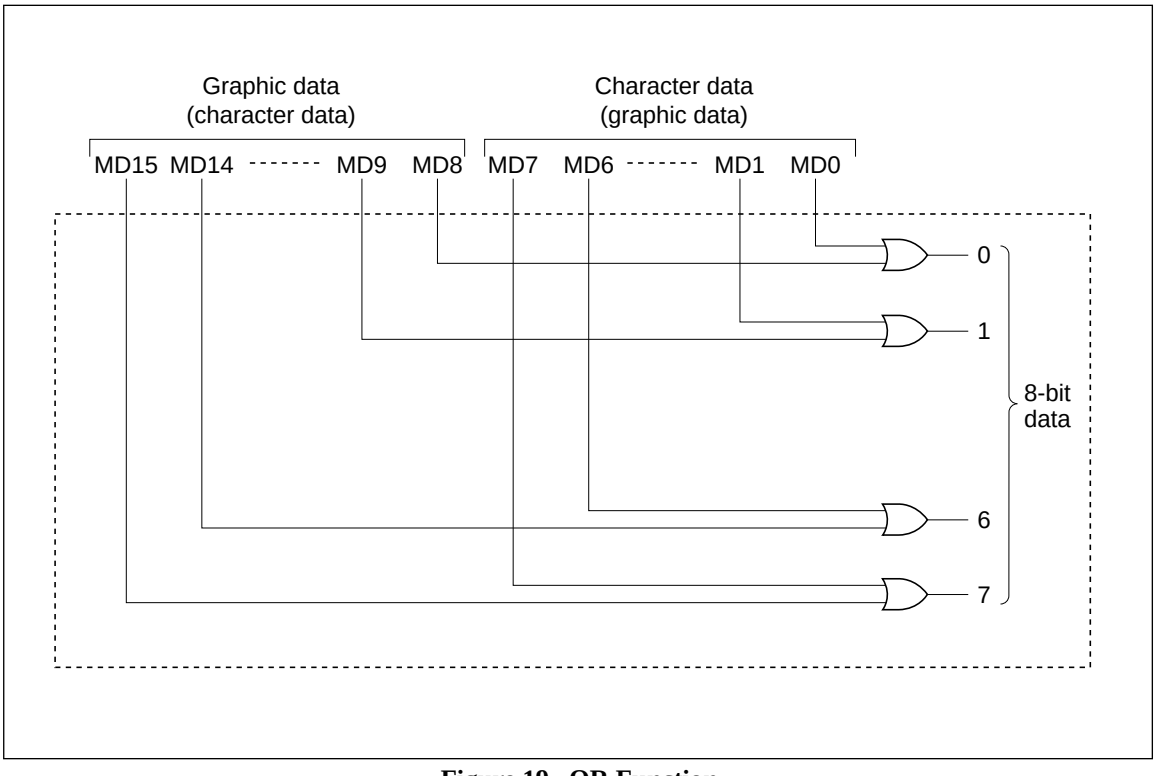


Figure 19 OR Function

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in figure 20. The 16 refresh addresses per scanned line are output 16 times, from $00–$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in table 7.

Table 7 Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

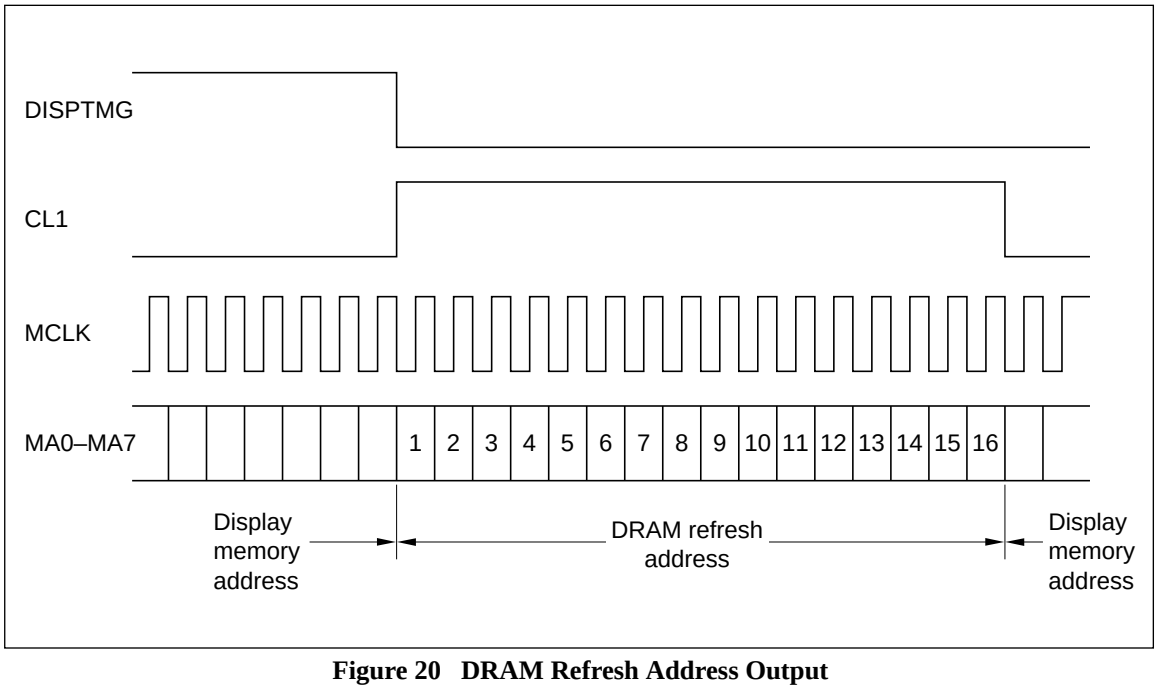


Figure 20 DRAM Refresh Address Output

Easy Mode

This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Raster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of a display spread over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See figure 21.)

Table 8 Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (Decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

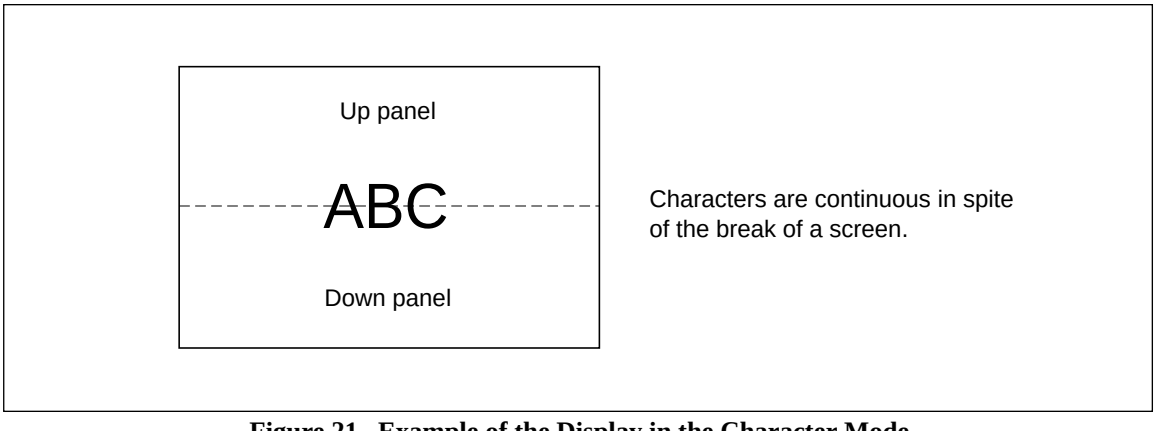


Figure 21 Example of the Display in the Character Mode

System configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (figure 22).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column drivers is smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations:

- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format:

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.

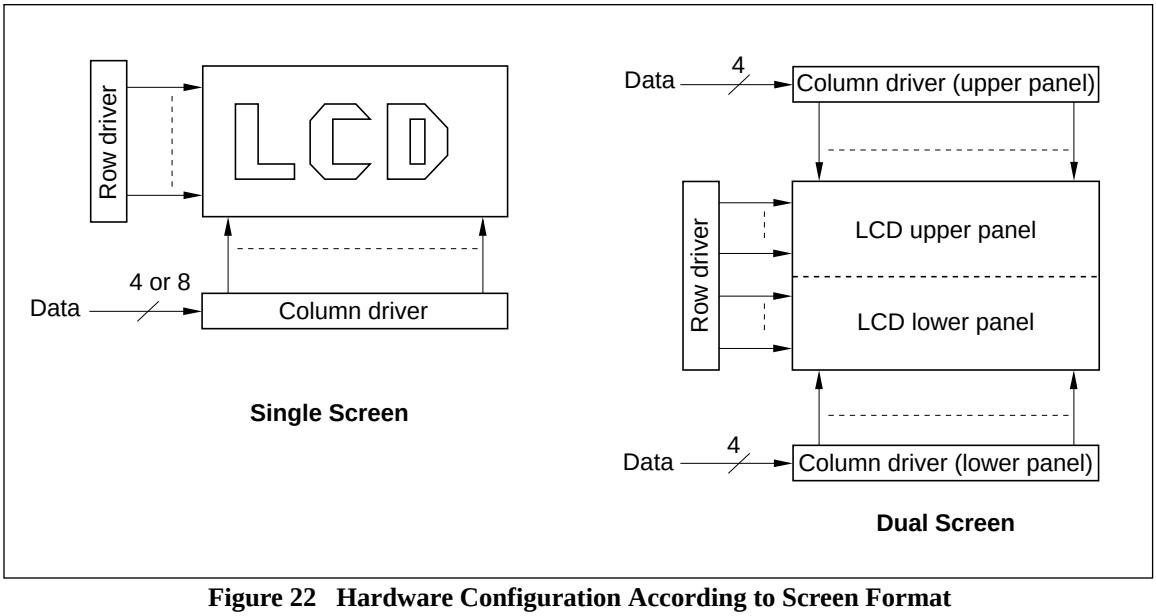


Figure 22 Hardware Configuration According to Screen Format

Table 9 Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configu-ration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum Data Transfer Speed (Mbps)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	5
				Wide	$\frac{AT}{OR}$	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	$\frac{AT}{OR}$	20	1
				Wide	$\frac{AT}{OR}$	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	9
				Wide	$\frac{AT}{OR}$	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note: Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

Mode List

Table 10 Mode List

No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Config.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic		—	—
4	Dual-screen graphic 2	1	1	0	0	0					
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic		—	—
8	Single-screen graphic 2	0	1	0	0	0					
9	8-bit character	0	0	1	0	0	Single screen	Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic		—	—
12	8-bit graphic 2	0	1	1	0	0					
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note: The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are prohibited, because they may cause malfunctions. If you set an prohibited combination, set the right combination again.

Internal Registers

The HD63645/HD64645/HD64646 has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2–R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (figure 23) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (figure 24) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. Nht indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its units are, then, converted from time into the number of characters. This value should be specified according to the specification of the LCD system to be used.

Note the following restrictions

$$Nhd + \frac{16}{m} \leq Nht + 1$$

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

Horizontal Displayed Characters Register (R1)

R1 register (figure 25) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

Nhd must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (figure 26) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	
—	—	—	Register address						W

Figure 23 Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nht (total characters – 1)								Character	W

Figure 24 Horizontal Total Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nhd (displayed characters)								Character	W

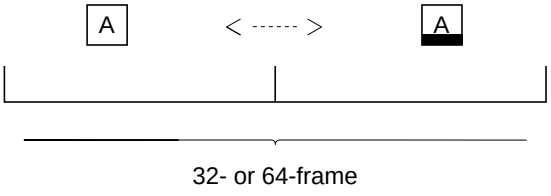
Figure 25 Horizontal Displayed Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nr					Raster	W

Figure 26 Maximum Raster Address Register

Cursor Start Raster Register (R10)

R10 register (figure 27) specifies the cursor start raster address and its blink mode. Refer to table 11.



Cursor End Raster Register (R11)

R11 register (figure 28) specifies the cursor end raster address.

Start Address Register (H/L) (R12/R13)

R12/R13 register (figure 29) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from the MPU.

Cursor Address Register (H/L) (R14/R15)

R14/R15 register (figure 30) specifies a cursor display address. Cursor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Horizontal Virtual Screen Width Register (R18)

R18 register (figure 31) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Table 11 Cursor Blink Mode

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	B	P	Ncs (raster address)					Raster	W

Figure 27 Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (raster address)					Raster	W

Figure 28 Cursor End Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R12)								Memory address	R/W
Memory address (L) (R13)									

Figure 29 Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R14)								Memory address	R/W
Memory address (L) (R15)									

Figure 30 Cursor Address Register

Multiplexing Duty Ratio Register (H/L) (R19/R20)

R19/R20 register (figure 32) specifies the number of vertical dots of the display screen. The programmed value differs according to the LCD screen configuration.

In single screen configuration:

$$\text{(Programmed value)} = \text{(Number of vertical dots)} - 1$$

In dual screen configuration:

$$\text{(Programmed value)} = \frac{\text{(Number of vertical dots)}}{2} - 1$$

Display Start Raster Register (R21)

R21 register (figure 33) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode Register (R22)

The Or of the data bits of R22 (figure 34) register and the external terminals of the same name determines a particular mode (figure 35).

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 31 Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters – 1) (R20)									

Note: * Number of rasters

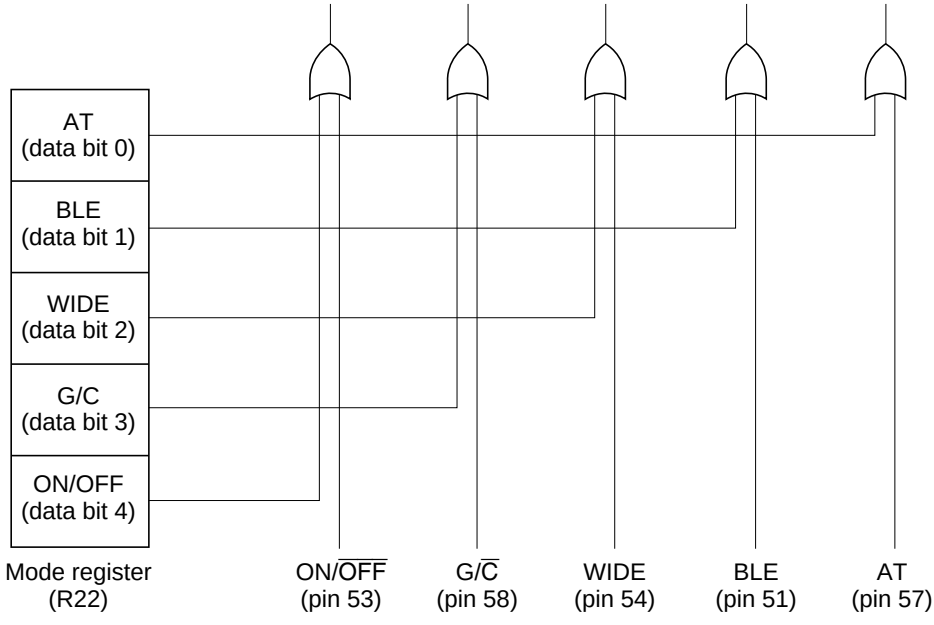
Figure 32 Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Raster address					Raster	W

Figure 33 Display Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	ON/OFF	G/C	WIDE	BLE	AT	—	W

Figure 34 Mode Register



Notes: 1. AT (valid only when G/$\overline{C}$ is low (character mode))
AT = High: Attribute functions enabled, OR function disabled.
AT = Low: OR function enabled, attribute functions disabled.

2. BLE (valid only when G/$\overline{C}$ is low (character mode))
BLE = High: Blinking enable on the character specified by attribute RAM
BLE = Low: No blinking

3. WIDE (valid only when G/$\overline{C}$ is low (character mode))
WIDE = High: Wide display enabled
WIDE = Low: Normal display

4. G/$\overline{C}$
G/$\overline{C}$ = High: Graphic 1 display (when AT = low) or graphic 2 display (when AT = high)
G/$\overline{C}$ = Low: Character display

5. ON/$\overline{OFF}$
ON/$\overline{OFF}$ = High: Display on state
ON/$\overline{OFF}$ = Low: Display off state

Figure 35 Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers are restricted as shown in table 12.

Table 12 Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display format	$1 < Nhd < Nht + 1 \leq 256$	R0, R1
	$Nhd + \frac{16}{m}^{*1} \leq Nht + 1$	
	(No. of vertical dots) × (No. of horizontal dots) × (frame frequency; f_{FRM}) ≤ (data transfer speed; V)	R1, R19, R20
	$\left\{\begin{matrix}1\\2\end{matrix}\right\}^{*2} \times (Nd + 1) \times Nhd \times \left\{\begin{matrix}8\\16\end{matrix}\right\}^{*3} f_{FRM} \leq V$	
	$Nhd \leq Nir$	R1, R18
	$0 \leq Nd \leq 511$	R19, R20
Cursor control	$0 \leq Ncs \leq Nce$	R10, R11
	$Nce \leq Nr$	R10, R9
Smooth scroll	$Nsr \leq Nr$	R21, R9
Memory width set	$0 \leq Nir \leq 255$	R18

Notes: 1. m varies according to the modes. See the following table.

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

2. Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5, 6, 7, 8, 9, 10, 11, 12	1
1, 2, 3, 4, 13	2

3. Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1, 5, 9	8
2, 3, 4, 6, 7, 8, 10, 11, 12, 13	16

Reset

$\overline{RES}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

Reset is defined as follows (figure 36):

- At reset: the time when $\overline{RES}$ goes low
- During reset: the period while $\overline{RES}$ remains low
- After reset: the period on and after the $\overline{RES}$ transition from low to high
- Make sure to hold the reset signal low for at least 1 µs

$\overline{RES}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{RES}$ pin does not basically control output pins, and operates regardless of other input pins.

1. Preserve states before reset

   LU0–LU3, LD0–LD3, FLM, CL1, RA0–RA4

2. Fixed at high level

   MLCK

3. Preserve states before reset or fixed at low level according to the timing when the reset signal is input

   DISPTMG, CUDISP, MA0–MA15

4. Fixed at high or low according to mode

   CL2

5. Unaffected

   DB_0–DB_7

Reset State of Registers

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD63645/HD64645/HD64646

1. The HD63645/HD64645/HD64646 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.

2. At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

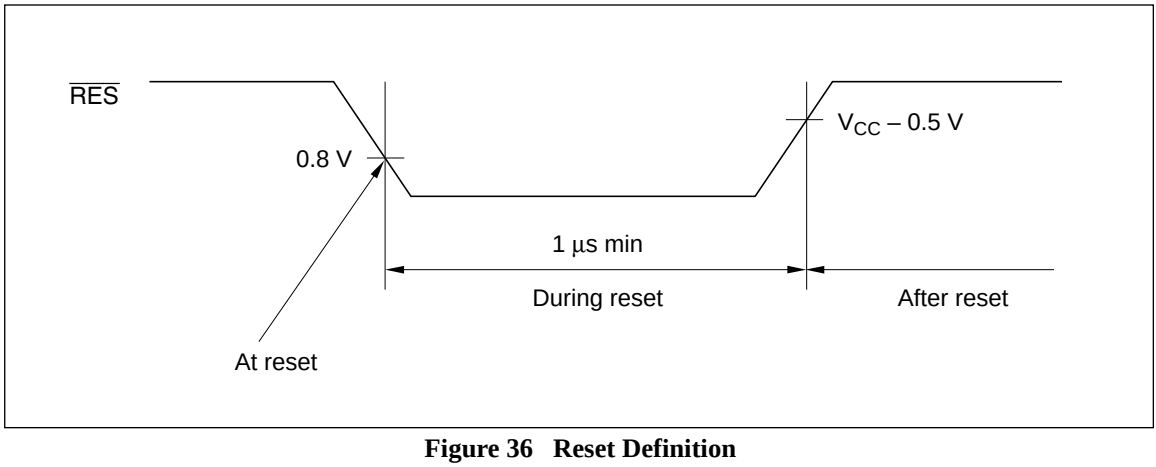


Figure 36 Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	–0.3 to +7.0 V	2
Terminal voltage	V_{in}	–0.3 to V_{CC} + 0.3 V	2
Operating temperature	T_{opr}	–20°C to +75°C	
Storage temperature	T_{stg}	–55°C to +125°C	

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.

2. With respect to ground (GND = 0 V)

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC} – 0.5		V_{CC} + 0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC} + 0.3	V	
	All others		2.0		V_{CC} + 0.3	V	
Input low voltage	All others	V_{IL}	–0.3		0.8	V	
Output high voltage	TTL interface*1	V_{OH}	2.4			V	I_{OH} = –400 µA
	CMOS interface*1		V_{CC} – 0.8			V	I_{OH} = –400 µA
Output low voltage	TTL interface	V_{OL}			0.4	V	I_{OL} = 1.6 mA
	CMOS interface				0.8	V	I_{OL} = 400 µA
Input leakage current	All inputs except DB_0–DB_7	I_{IL}	–2.5		+2.5	µA	
Three state (off-state) leakage current	DB_0–DB_7	I_{TSL}	–10		+10	µA	
Current dissipation*2		I_{CC}			10	mA	

Notes: 1. TTL Interface; MA0–MA15, RA0–RA4, DISPTMG, CUDISP, DB0–DB7, MCLK
C-MOS Interface; LU0–LU3, LD0–LD3, CL1, CL2, M, FLM

2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.

3. If the capacitive loads of LU0–LU3 and LD0–LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0–LU3 and LD0–LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface (HD63645—68 Family) (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500			ns	37
Enable pulse width (high)	P_{WEH}	220			ns	
Enable pulse width (low)	P_{WEL}	220			ns	
Enable rise time	t_{Er}			25	ns	
Enable fall time	t_{Ef}			25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70			ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10			ns	
DB_0–DB_7 setup time	t_{DS}	60			ns	
DB_0–DB_7 hold time	t_{DHW}	10			ns	
DB_0–DB_7 output delay time	t_{DDR}			150	ns	
DB_0–DB_7 output hold time	t_{DHR}	20			ns	

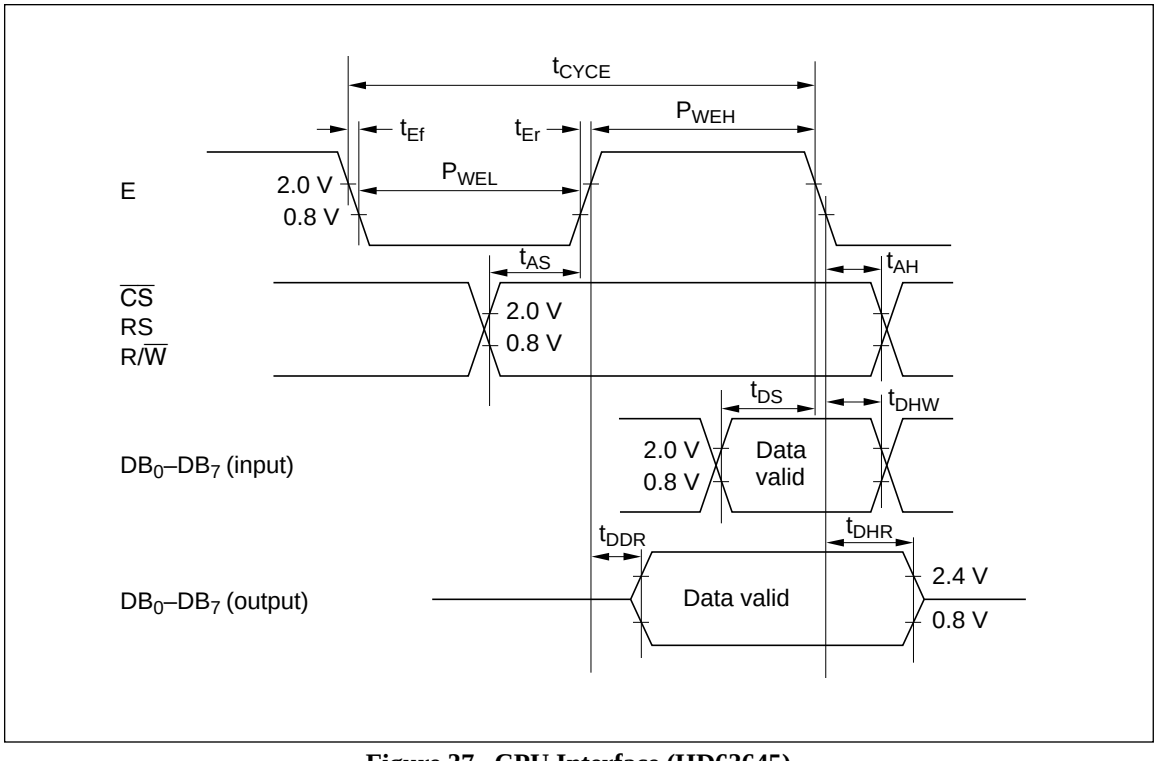


Figure 37 CPU Interface (HD63645)

CPU Interface (HD64645 and HD64646—80 Family) (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	38
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0–DB_7 setup time	t_{DSW}	100			ns	
DB_0–DB_7 hold time	t_{DHW}	0			ns	
DB_0–DB_7 output delay time	t_{DDR}			150	ns	
DB_0–DB_7 output hold time	t_{DHR}	20			ns	

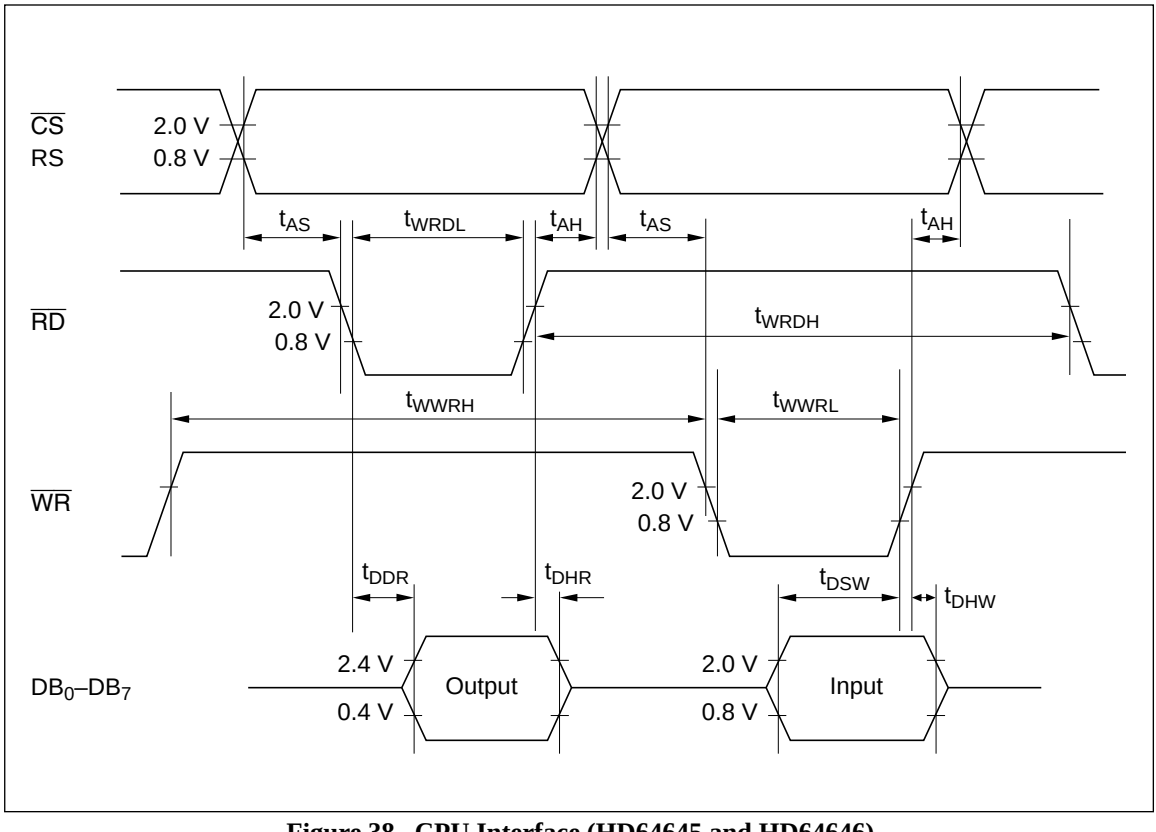


Figure 38 CPU Interface (HD64645 and HD64646)

Memory Interface (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100	—	—	ns	39
DCLK high level width	t_{WDH}	30	—	—	ns	
DCLK low level width	t_{WDL}	30	—	—	ns	
DCLK rise time	t_{Dr}	—	—	20	ns	
DCLK fall time	t_{Df}	—	—	20	ns	
MCLK delay time	t_{DMD}	—	—	60	ns	
MCLK rise time	t_{Mr}	—	—	30	ns	
MCLK fall time	t_{Mf}	—	—	30	ns	
MA0–MA15 delay time	t_{MAD}	—	—	150	ns	
MA0–MA15 hold time	t_{MAH}	10	—	—	ns	
RA0–RA4 delay time	t_{RAD}	—	—	150	ns	
RA0–RA4 hold time	t_{RAH}	10	—	—	ns	
DISPTMG delay time	t_{DTD}	—	—	150	ns	
DISPTMG hold time	t_{DTH}	10	—	—	ns	
CUDISP delay time	t_{CDD}	—	—	150	ns	
CUDISP hold time	t_{CDH}	10	—	—	ns	
CL1 delay time	t_{CL1D}	—	—	150	ns	
CL1 hold time	t_{CL1H}	10	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
MD0–MD15 setup time	t_{MDS}	30	—	—	ns	
MD0–MD15 hold time	t_{MDH}	15	—	—	ns	

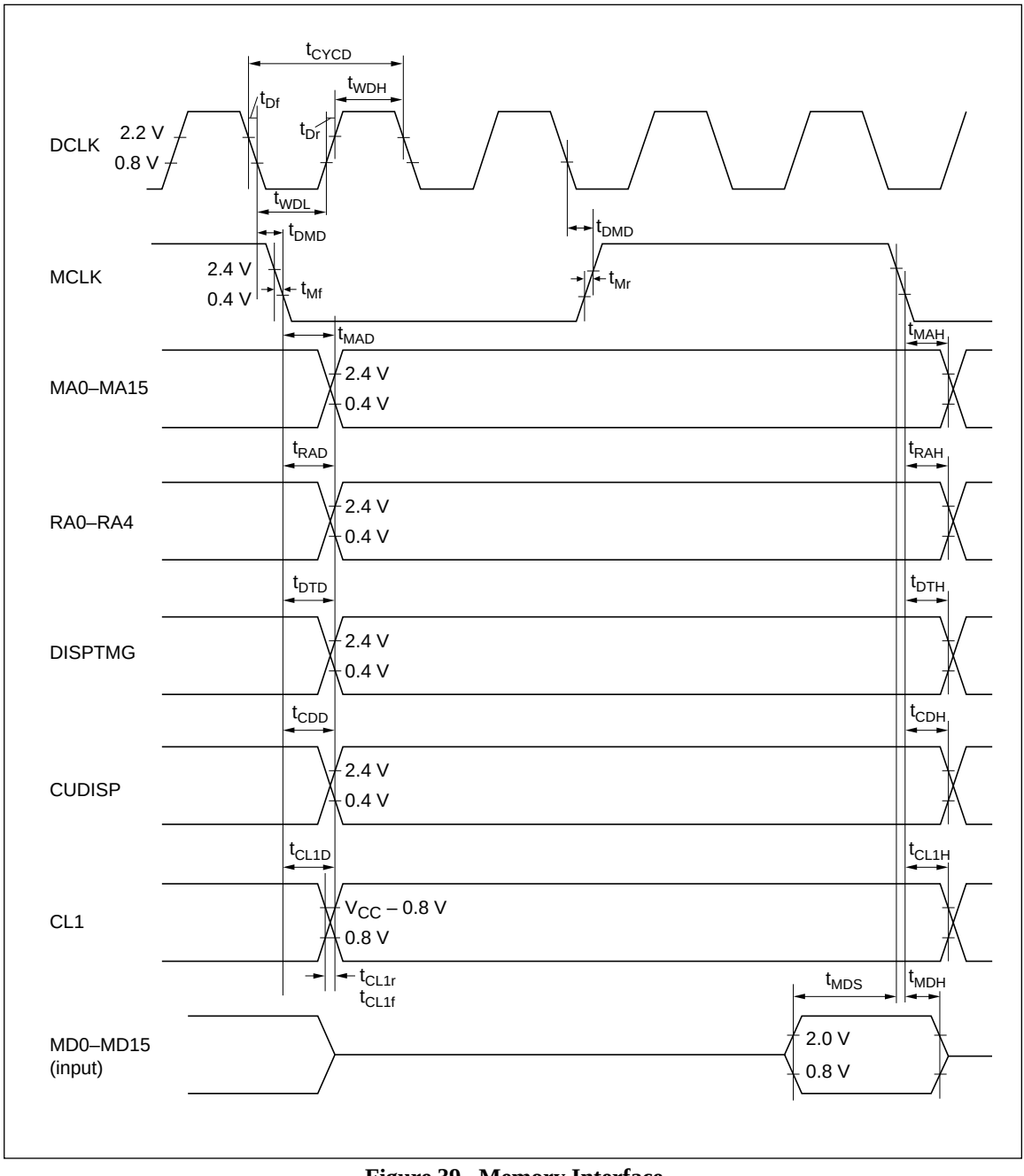


Figure 39 Memory Interface

LCD Interface 1 (HD63645 and HD64645) (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50	—	—	ns	40
Display data hold time	t_{LDH}	100	—	—	ns	
CL2 high level width	t_{WCL2H}	100	—	—	ns	
CL2 low level width	t_{WCL2L}	100	—	—	ns	
FLM setup time	t_{FS}	500	—	—	ns	
FLM hold time	t_{FH}	300	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	

Note: At fCL2 = 3 MHz

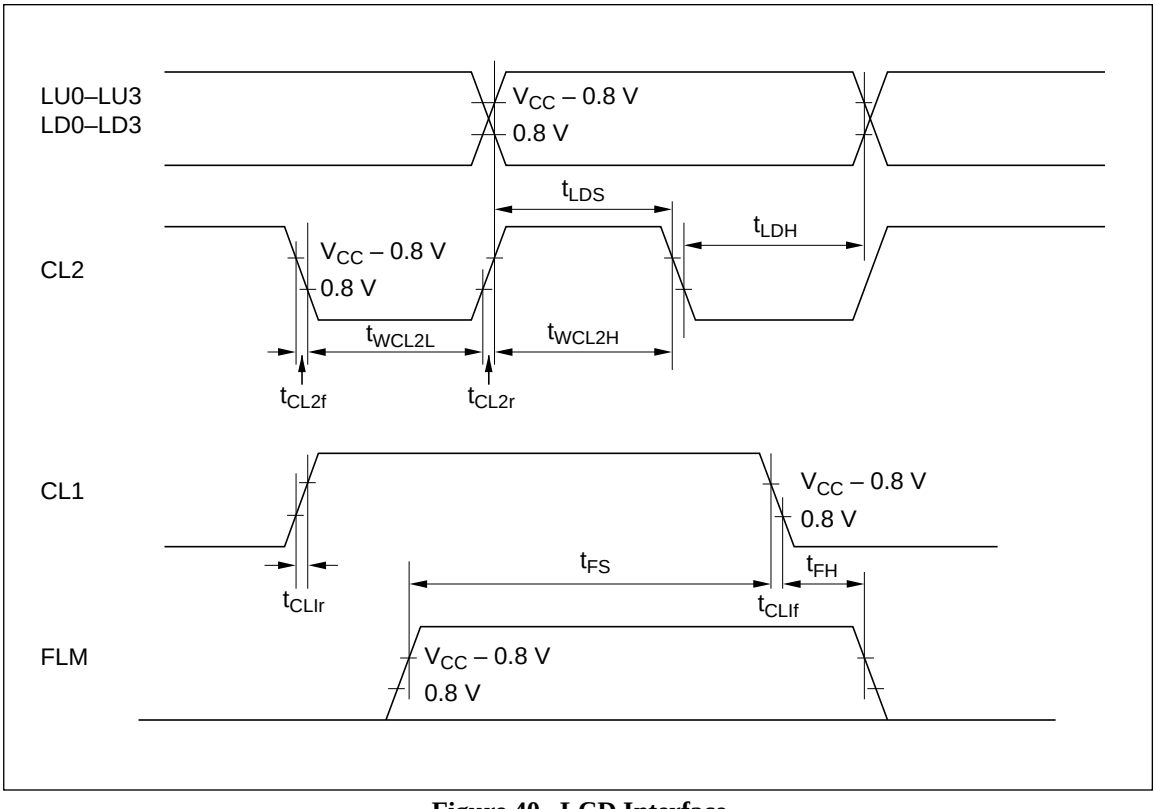


Figure 40 LCD Interface

LCD Interface 2 (HD64646 at f_{CL2} = 3 MHz) (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	—	—	ns	41
FLM hold time	t_{FH}	300	—	—	ns	
M delay time	t_{DM}	—	—	200	ns	
CL1 high level width	t_{CL1H}	300	—	—	ns	
Clock setup time	t_{SCL}	500	—	—	ns	
Clock hold time	t_{HCL}	100	—	—	ns	
Phase difference 1	t_{PD1}	100	—	—	ns	
Phase difference 2	t_{PD2}	500	—	—	ns	
CL2 high level width	t_{CL2H}	100	—	—	ns	
CL2 low level width	t_{CL2L}	100	—	—	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	
Display data setup time	t_{LDS}	80	—	—	ns	
Display data hold time	t_{LDH}	100	—	—	ns	
Display data delay time	t_{LDD}	—	—	30	ns	

LCD Interface 3 (HD64646 at f_{CL2} = 5 MHz) (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	—	—	ns	41
FLM hold time	t_{FH}	200	—	—	ns	
M delay time	t_{DM}	—	—	200	ns	
CL1 high level width	t_{CL1H}	300	—	—	ns	
Clock setup time	t_{SCL}	500	—	—	ns	
Clock hold time	t_{HCL}	100	—	—	ns	
Phase difference 1	t_{PD1}	70	—	—	ns	
Phase difference 2	t_{PD2}	500	—	—	ns	
CL2 high level width	t_{CL2H}	50	—	—	ns	
CL2 low level width	t_{CL2L}	50	—	—	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	
Display data setup time	t_{LDS}	30	—	—	ns	
Display data hold time	t_{LDH}	30	—	—	ns	
Display data delay time	t_{LDD}	—	—	30	ns	

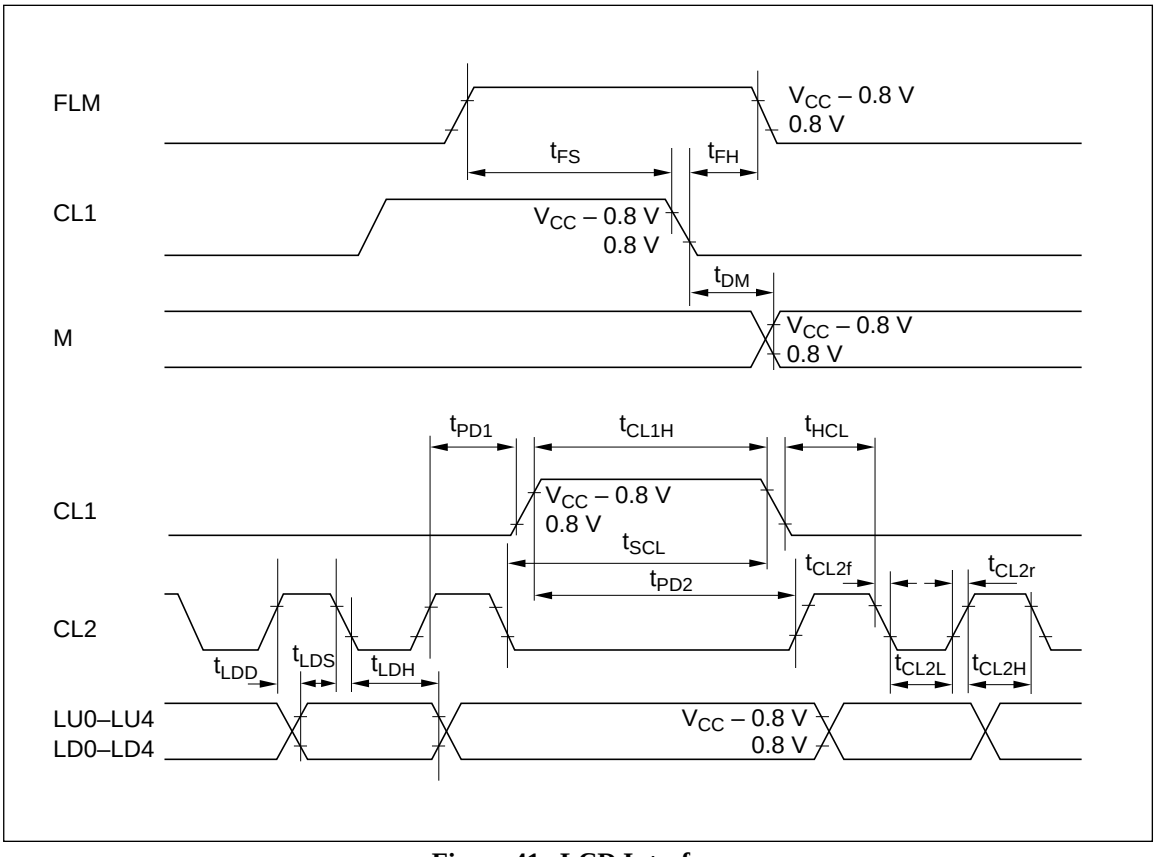
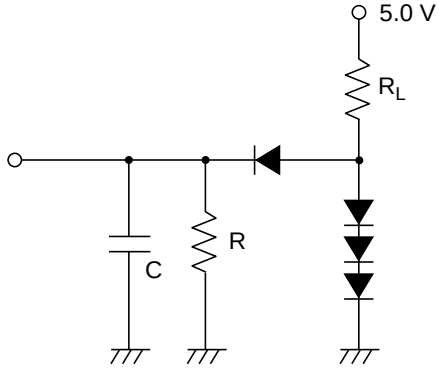


Figure 41 LCD Interface

Load Circuit

TTL Load

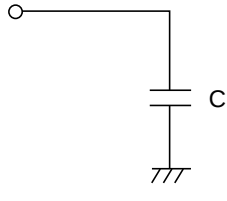
Terminal	R_L	R	C	Remarks
DB_0–DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf: Not specified
MA0–MA15, RA0–RA4, DISPTMG, CUDISP	2.4 kΩ	11 kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf: Specified



All diodes: 1S2074Ⓗ

Capacitive Load

Terminal	C	Remarks
CL2	150 pF	tr, tf: Specified
CL1	200 pF	
LU0–LU3, LD0–LD3, M	150 pF	tr, tf: Not specified
FLM	50 pF	



Refer to user's manual (No. 68-1-160) and application note (No. ADE-502-003) for detail of this product.

HD66840/HD66841

LVIC/LVIC-II
(LCD Video Interface Controller)

HITACHI

Description

The HD66840/HD66841 LCD video interface controller (LVIC/LVIC-II) converts standard RGB video signals for CRT display into LCD data. It enable a CRT display system to be replaced by an LCD system without any changes, and it also enables software originally intended for CRT display to control an LCD.

Since the LVIC/LVIC-II can control TFT-type LCDs in addition to current TN-type or STN-type LCDs, it can support 8-color display as well as monochrome, 8-level gray-scale display. It can program screen size and can control a large-panel LCD of 720 × 512 dots.

The LVIC-II thanks to a gray-scale palette, any 8-levels can be selected from 13 gray-scale levels, depending on the LCD panel used.

Features

- Conversion of RGB video signals used for CRT display into LCD data
  - — Monochrome display data
  - — 8-level gray-scale data
  - — 8-color display data
- Selectable LVIC/LVIC-II control method
  - — Pin programming method
  - — Internal register programming method (either with MPU or ROM)
- Programmable screen size
  - — 640 or 720 dots (80 or 90 characters) wide by 200, 350, 400, 480, 512, or 540 dots (lines) high, using the pin programming method
  - — 32 to 4048 dots (4 to 506 characters) wide by 4 to 1024 dots (lines) high, using internal register programming method
- Double-height display capability
- Generation of display timing signal (DISPTMG) from horizontal synchronization (HSYNC) and vertical synchronization (VSYNC) signals
- Control of TN-type, STN-type LCDs and TFT-type LCDs
- Internal PLL circuit capable of generating a CRT display dot clock (DOTCLK) (external charge pump, low pass filter (LPF), and voltage controlled oscillator (VCO) required)
- Gray-scale level selection from gray-scale palette HD66841 (LVIC-II) only
- Maximum operating frequency (dot clock for CRT display)
  - — HD66840 (LVIC) 25 MHz
  - — HD66841 (LVIC-II) 30 MHz
- LCD driver interface
  - — 4-, 8-, or 12-bit (4 bits each for R, G, and B) parallel data transfer
- Recommended LCD drivers
  - — HD66204, HD66214T, HD66224T and HD66110ST (column)
  - — HD66205, HD66205T, HD66215T and HD66115T (common)
  - — HD66106 and HD66107T (column/common)
- 1.3 µm CMOS process
- Single power supply
  - — +5 V ±10%

Hitachi semiconductor

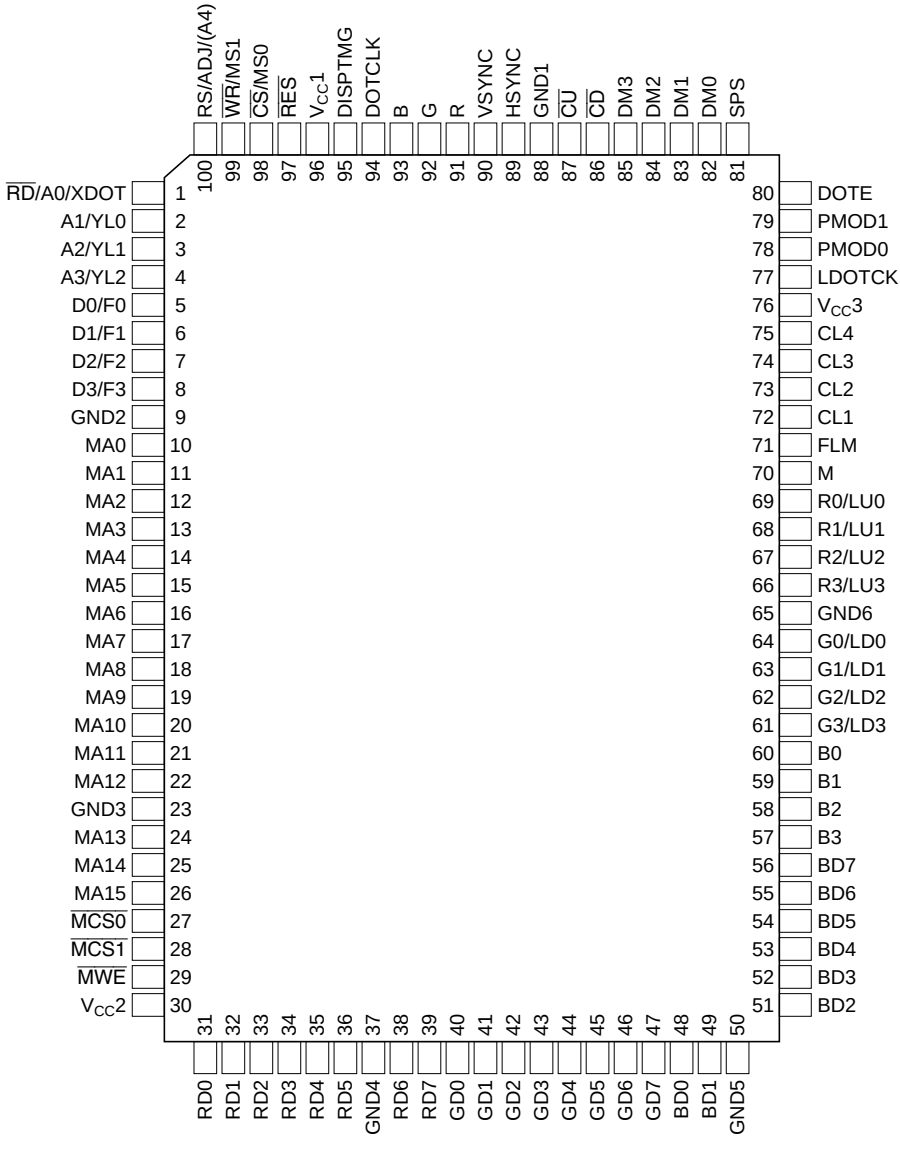
Differences between Products HD66840 and HD66841

	HD66840	HD66841
Dot clock	25 MHz	30 MHz
Frame-based thinning control	Each line	Each dot and each line
Display mode 16	Single screen Both sides X/Y driver Horizontal stripe	Dual screen One sides X/Y driver Vertical stripe
Gray-scale palette	No	8 registers
Pin arrangement and signal name	Pin 100: RS/ADJ	Pin 100: RS/ADJ/A4

Ordering Information

Type No.	Dot Clock	Package
HD66840FS	25 MHz	100-pin plastic QFP (FP-100A)
HD66841FS	30 MHZ	

Pin Arrangement



(Top view)

Note: ( ) is for HD66841

Pin Description

The HD66840 and HD66841's pins are listed in table 1 and their functions are described below.

Table 1 Pin Description

Classification	Symbol	Pin Number	I/O	Pin Name	Notes
Power supply	$V_{CC}1$–$V_{CC}3$	96, 30, 76	—	$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	
	GND1–GND6	88, 9, 23, 37, 50, 65	—	Ground 1 to ground 6	
Video signal interface	R, G, B	91, 92, 93	I	Red, green, and blue serial data	1
	HSYNC	89	I	Horizontal synchronization	
	VSYNC	90	I	Vertical synchronization	
	DISPTMG	95	I	Display timing	2
	DOTCLK	94	I	Dot clock	
LCD interface	R0–R3	69–66	O	LCD red data 0–3	3
	LU0–LU3	69–66	O	LCD upper panel data 0–3	4
	G0–G3	64–61	O	LCD green data 0–3	3, 5
	LD0–LD3	64–61	O	LCD lower panel data 0–3	4, 5
	B0–B3	60–57	O	LCD blue data 0–3	3, 6
	CL1	72	O	LCD data line select clock	
	CL2	73	O	LCD data shift clock	
	CL3	74	O	Y-driver shift clock 1	7
	CL4	75	O	Y-driver shift clock 2	7
	FLM	71	O	First line marker	
	M	70	O	LCD driving signal alternation	
	LDOTCK	77	I	LCD dot clock	
Buffer memory interface	$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$	27, 28	O	Memory chip select 0, 1	8
	$\overline{\text{MWE}}$	29	O	Memory write enable	8
	MA0–MA15	10–22, 24–26	O	Memory address 0–15	8
	RD0–RD7	31–36, 38, 39	I/O	Memory red data 0–7	8
	GD0–GD7	40–47	I/O	Memory green data 0–7	8, 9
	BD0–BD7	48, 49, 51–56	I/O	Memory blue data 0–7	8, 9

Table 1 Pin Description (cont)

Classification	Symbol	Pin Number	I/O	Pin Name	Notes
Mode setting	PMOD0, PMOD1	78, 79	I	Program mode 0, 1	
	DOTE	80	I	Dot clock edge change	
	SPS	81	I	Synchronization polarity select	
	DM0–DM3	82–85	I	Display mode 0–3	
	MS0, MS1	98, 99	I	Memory select 0, 1	10, 11
	XDOT	1	I	X-dot	10
	YL0–YL2	2–4	I	Y-line 0–2	10, 12
	ADJ	100	I	Adjust	10
	F0–F3	5–8	I	Fine adjust 0–3	10
MPU interface	$\overline{CS}$	98	I	Chip select	10, 11
	$\overline{WR}$	99	I	Write	10, 11, 13
	$\overline{RD}$	1	I	Read	10, 13
	RS	100	I	Register select	10
	D0–D3	5–8	I/O	Data 0–3	10
	$\overline{RES}$	97	I	Reset	14
ROM interface	A0–A3, A4	1–4, 100	O	Address 0–4	10, 15
	D0–D3	5–8	I	Data 0–3	10
PLL interface	$\overline{CD}$	86	O	Charge down	
	$\overline{CU}$	87	O	Charge up	

Notes:
1. Fix G and B pins low if CRT display data is monochrome.
2. Fix high or low if the display timing signal is generated internally.
3. For 8-color display modes.
4. For monochrome or 8-level gray-scale display modes.
5. Leave disconnected in 4-bit/single-screen data transfer modes.
6. Leave disconnected in monochrome or 8-level gray-scale display modes.
7. Leave disconnected in TN-type LCD modes.
8. Leave disconnected if no buffer memory is used.
9. Pull up with a resistor of about 20-kΩ in monochrome display modes.
   The HD66840/HD66841 writes the OR of RGB signals into R-plane RAM, so no RAM is required for the G and B planes in these modes. (If G- or B-plane RAM is connected in monochrome display modes, the HD66840/HD66841 writes G or B signals into each RAM. However, this does not affect the display or the contents of R-plane RAM.)
10. Multiplexed pins.
11. Fix high or low when using the ROM programming method.
12. Fix high or low when using the MPU programming method.
13. Do not set pins $\overline{WR}$ and $\overline{RD}$ low simultaneously.
14. A reset signal must be input after power-on.
15. HD66840 use address 0 to 3, HD66841 use address 0 to 4.

Pin Functions

Power Supply

$V_{CC}1$–$V_{CC}3$: Connect $V_{CC}1$–$V_{CC}3$ with +5 V.

GND1–GND6: Ground GND1–GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYNC: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0–R3: R0–R3 output R data for the LCD.

LU0–LU3: LU0–LU3 output LCD up panel data.

G0–G3: G0–G3 output G data for the LCD.

LD0–LD3: LD0–LD3 output LCD down panel data.

B0–B3: B0–B3 output B data for the LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see “LCD System Configuration”).

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see “LCD System Configuration”).

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$: $\overline{\text{MCS0}}$ and $\overline{\text{MCS1}}$ output the buffer memory chip select signal.

$\overline{\text{MWE}}$: $\overline{\text{MWE}}$ outputs the write enable signal of buffer memories.

MA0–MA15: MA0–MA15 output buffer memory addresses.

RD0–RD7: RD0–RD7 transfer data between R data buffer memory and the LVIC.

GD0–GD7: GD0–GD7 transfer data between G data buffer memory and the LVIC.

BD0–BD7: BD0–BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0–PMOD1 input signals select a programming method (table 6).

DOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G and B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0–DM3: The DM0–DM3 input signals select a display mode (table 8).

MS0–MS1: The MS0-MS1 input signals select the kind of buffer memories (table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0–YL2: The YL0–YL2 input signals specify the number of vertical displayed lines (table 3).

ADJ: The ADJ input signal determines whether F0–F3 pins adjust the number of vertical displayed lines or the display timing signal. F0–F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0–F3: F0–F3 input data for adjusting the number of vertical displayed lines (table 4), or the display timing signal (see "Fine Adjustment of Display Timing Signal").

MPU Interface

$\overline{\text{CS}}$: The MPU selects the LVIC when $\overline{\text{CS}}$ is low.

$\overline{\text{WR}}$: The MPU inputs the $\overline{\text{WR}}$ write signal to write data into internal registers of the LVIC. The MPU can write data when $\overline{\text{WR}}$ is low and cannot write data when high.

$\overline{\text{RD}}$: The MPU inputs the $\overline{\text{RD}}$ read signal to read data from internal registers of the LVIC. The MPU can read data when $\overline{\text{RD}}$ is low and cannot read data when high.

RS: The MPU inputs the RS signal together with $\overline{\text{CS}}$ to select internal registers. The MPU selects data registers (R0–R15) when RS is high and $\overline{\text{CS}}$ is low, and selects the address register (AR) when RS is low and $\overline{\text{CS}}$ is low.

D0–D3: D0–D3 transfer internal register data between the MPU and LVIC.

$\overline{\text{RES}}$: $\overline{\text{RES}}$ inputs the external reset signal.

ROM Interface

A0–A3: A0–A3 output address 0 to address 3 to an external ROM. (HD66840)

A0–A4: A0–A4 output address 0 to address 4 to an external ROM. (HD66841)

D0–D3: D0–D3 input data from an external ROM to internal registers.

PLL Circuit Interface

$\overline{\text{CD}}$: $\overline{\text{CD}}$ outputs the charge down signal to an external charge pump.

$\overline{\text{CU}}$: $\overline{\text{CU}}$ outputs the charge up signal to an external charge pump.

Table 2 Programming Method Selection

PMOD 1	PMOD 0	Programming Method	
0	0	Pin programming	
0	1	Internal register programming	MPU
1	0		ROM
1	1	Inhibited*	

Note: * This combination is for test mode: it disables display.

Table 3 Memory Type Selection

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes memory
1	0	32-kbytes memory
1	1	64-kbytes memory

Table 4 Number of Vertical Displayed Lines

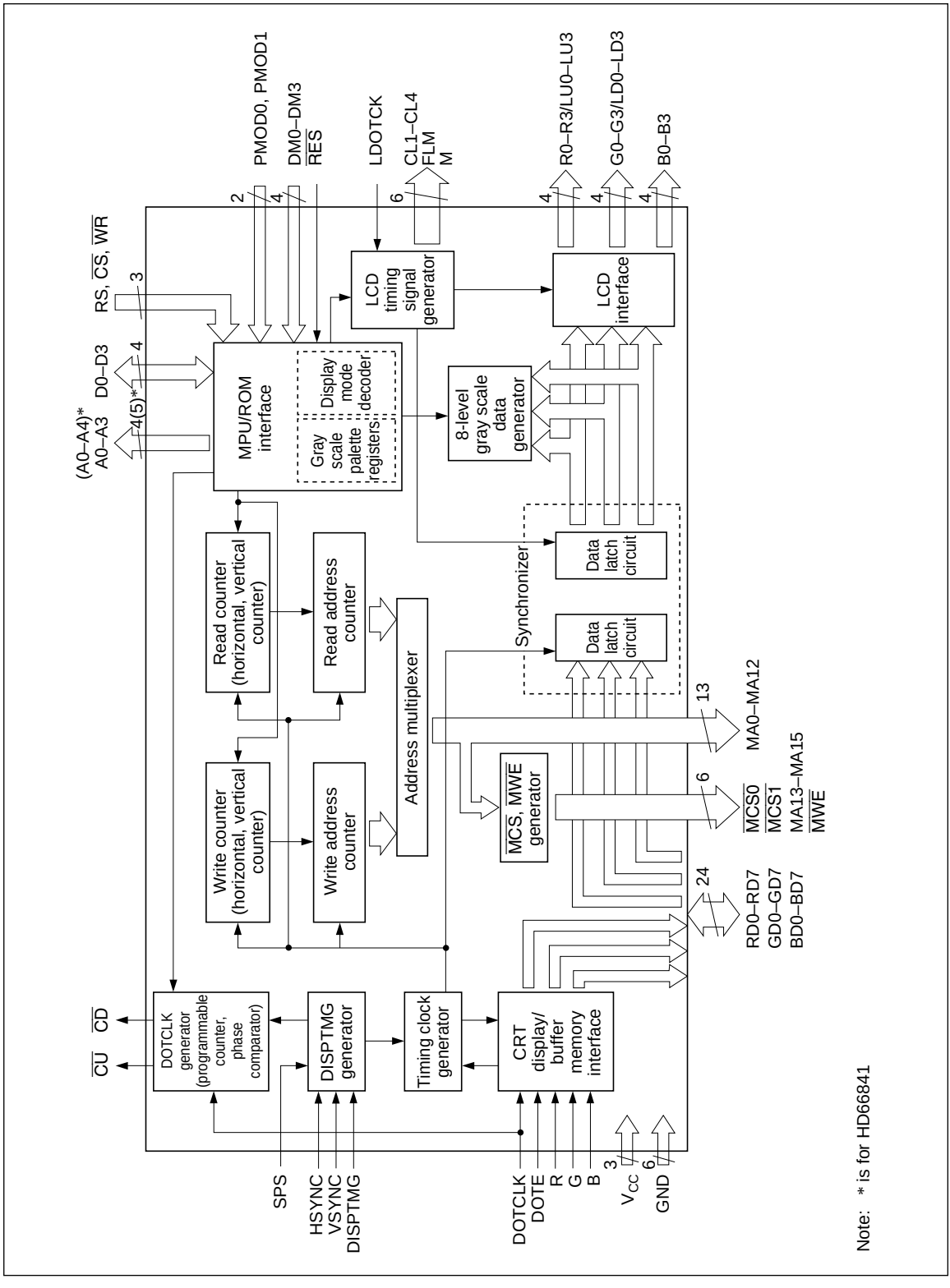
YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Inhibited*
1	1	1	

Note: * 480 lines are displayed, but they are practically indistinguishable.

Table 5 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Adjusted Lines
0	0	0	0	±0
0	0	0	1	+1
0	0	1	0	+2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+14
1	1	1	1	+15

Block Diagram



Registers

The HD66840 and HD66841's registers are listed in table 6 and the bit assignments within the registers are shown in figure 1 for HD66840, figure 2 for HD66841.

Table 6 Register List (HD66840 and HD66841)

			Reg. Address									
$\overline{CS}$	RS	PS*1	3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write*2	Notes
1	—		—	—	—	—	—	—	—	—	—	
0	0		—	—	—	—	AR	Address register	—	—	W	3
0	1	0	0	0	0	0	R0	Control register 1	—	—	R/W	
0	1	0	0	0	0	1	R1	Control register 2	—	—	R/W	
0	1	0	0	0	1	0	R2	Vertical displayed lines register (middle-order)	Line	Nvd	R/W	4
0	1	0	0	0	1	1	R3	Vertical displayed lines register (low-order)	Line	Nvd	R/W	4
0	1	0	0	1	0	0	R4	Vertical displayed lines register (high-order)/ CL3 period register (high-order)	Line/Chars.	Nvd/Npc	R/W	4, 5, 6
0	1	0	0	1	0	1	R5	CL3 period register (low-order)	Chars.	Npc	R/W	4, 5, 6
0	1	0	0	1	1	0	R6	Horizontal displayed characters register (high-order)	Chars.	Nhd	R/W	6
0	1	0	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Chars.	Nhd	R/W	6
0	1	0	1	0	0	0	R8	CL3 pulse width register	Chars.	Npw	R/W	6
0	1	0	1	0	0	1	R9	Fine adjust register	Dots	Nda	R/W	7
0	1	0	1	0	1	0	R10	PLL frequency-division ratio register (high-order)	—	N_{PLL}	R/W	8
0	1	0	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)	—	N_{PLL}	R/W	8
0	1	0	1	1	0	0	R12	Vertical backporch register (high-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	0	1	R13	Vertical backporch register (low-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	1	0	R14	Horizontal backporch register (high-order)	Dots	Nchbp	R/W	4, 9
0	1	0	1	1	1	1	R15	Horizontal backporch register (low-order)	Dots	Nchbp	R/W	4, 9

Table 6 Register List (HD66841 Only)

$\overline{CS}$	RS	PS*1	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write*2	Notes
0	1	1	0	0	0	1	P1	Black palette register	—	—	R/W	
0	1	1	0	0	1	0	P2	Blue palette register	—	—	R/W	
0	1	1	0	0	1	1	P3	Red palette register	—	—	R/W	
0	1	1	0	1	0	0	P4	Magenta palette register	—	—	R/W	
0	1	1	0	1	0	1	P5	Green palette register	—	—	R/W	
0	1	1	0	1	1	0	P6	Cyan palette register	—	—	R/W	
0	1	1	0	1	1	1	P7	Yellow palette register	—	—	R/W	
0	1	1	1	0	0	0	P8	White palette register	—	—	R/W	
0	1	1	1	0	0	1		Reserved				
.	.	.	.	.	.	.		.				
.	.	.	.	.	.	.		.				
.	.	.	.	.	.	.		.				
0	1	1	1	1	1	1		Reserved				

Notes:
1. Corresponds to bit 2 of control register 1 (R0) (HD66841 only)
2. W indicates that the register can only be written to; R/W indicates that the register can both be read from and written to. (HD66841 only)
3. Attempting to read data from this register when RS = 0 drives the bus to high-impedance state; output data becomes undefined.
4. Write (the specified value—1) into this register.
5. Valid only in 8-color display modes with horizontal stripes.
6. One character consists of eight horizontal dots.
7. Valid only if the display timing signal is supplied externally.
8. Valid only if the dot clock signal is generated internally.
9. Valid only if the display timing signal is generated internally.

Register No.	Data Bit				
	3	2	1	0	
—					
AR		Address register			
R0			DSP	DCK	←Control register 1
R1	MC	DON	MS1	MS0	←Control register 2
R2	Vertical displayed				
R3	lines register				
R4					
R5	CL3 period register				
R6	Horizontal displayed				
R7	characters register				
R8	CL3 pulse width register				
R9	Fine adjust register				
R10	PLL frequency-				
R11	dividing ratio register				
R12	Vertical backporch				
R13	register				
R14	Horizontal backporch				
R15	register				

Note: indicates invalid bits. Attempting to read data from these register bits returns indefinite output data.

Figure 1 Register Bit Assignment of HD66840

$\overline{CS}$	RS	PS*1	Reg. Address 3	2	1	0	Reg. No.	Data Bit 3	2	1	0	
1	—	—	—	—	—	—	—	*2				
0	0	—	—	—	—	—	AR					← Address register
0	1	—	0	0	0	0	R0	DIZ	PS	DSP	DCK	← Control register 1
0	1	0	0	0	0	1	R1	MC	DON	MS1	MS0	← Control register 2
0	1	0	0	0	1	0	R2					← Vertical displayed lines register
0	1	0	0	0	1	1	R3					
0	1	0	0	1	0	0	R4					
0	1	0	0	1	0	1	R5					← CL3 period register
0	1	0	0	1	1	0	R6*3					← Horizontal displayed characters
0	1	0	0	1	1	1	R7					register
0	1	0	1	0	0	0	R8					← CL3 pulse width register
0	1	0	1	0	0	1	R9					← Fine adjust register
0	1	0	1	0	1	0	R10					← PLL frequency-division ratio
0	1	0	1	0	1	1	R11					register
0	1	0	1	1	0	0	R12					← Vertical backporch register
0	1	0	1	1	0	1	R13					
0	1	0	1	1	1	0	R14					← Horizontal backporch register
0	1	0	1	1	1	1	R15					
0	1	1	0	0	0	1	P1*4	0	0	0	0	← Black palette register
0	1	1	0	0	1	0	P2*4	0	0	1	0	← Blue palette register
0	1	1	0	0	1	1	P3*4	0	1	0	1	← Red palette register
0	1	1	0	1	0	0	P4*4	0	1	1	0	← Magenta palette register
0	1	1	0	1	0	1	P5*4	0	1	1	1	← Green palette register
0	1	1	0	1	1	0	P6*4	1	0	0	0	← Cyan palette register
0	1	1	0	1	1	1	P7*4	1	0	1	0	← Yellow palette register
0	1	1	1	0	0	0	P8*4	1	0	0	0	← White palette register
0	1	1	1	0	0	1	—	*5				← Reserved register
⋮	⋮	⋮		⋮								
0	1	1	1	1	1	1	—					

Notes: 1. Corresponds to bit 2 of control register 1 (R0).
2. Invalid bits. Attempting to read data from these bits returns undefined data.
3. The most significant bit is invalid in dual-screen configuration modes.
4. Bit values shown are default values at reset.
5. Reserved bits. Any Uttempt to write data into the register is invalid, although it has no affect on LSI operations. Any attempt to read data from the register returns undefined data.

Figure 2 Register Bit Assignment of HD66841

System Configuration

Figure 3 is a block diagram of a system in which the HD66840 and HD66841 is used outside a personal computer.

The HD66840 and HD66841 converts the RGB serial data sent from the personal computer into parallel data and temporarily writes it to the buffer memorie. It then reads out the data in order and outputs it to LCD drivers to drive the LCD. In this case, the CRT display dot clock (DOTCLK), which is a latch clock for serial data, is generated by the PLL circuit from the horizontal synchronization signal (HSYNC). The DOTCLK signal frequency is specified by the PLL frequency-division ratio register (R10, R11).

The system can be configured without a VCO and LPF if the DOTCLK signal is supplied externally, and it can be configured without an MPU if the LVIC-II is controlled by the pin programming method.

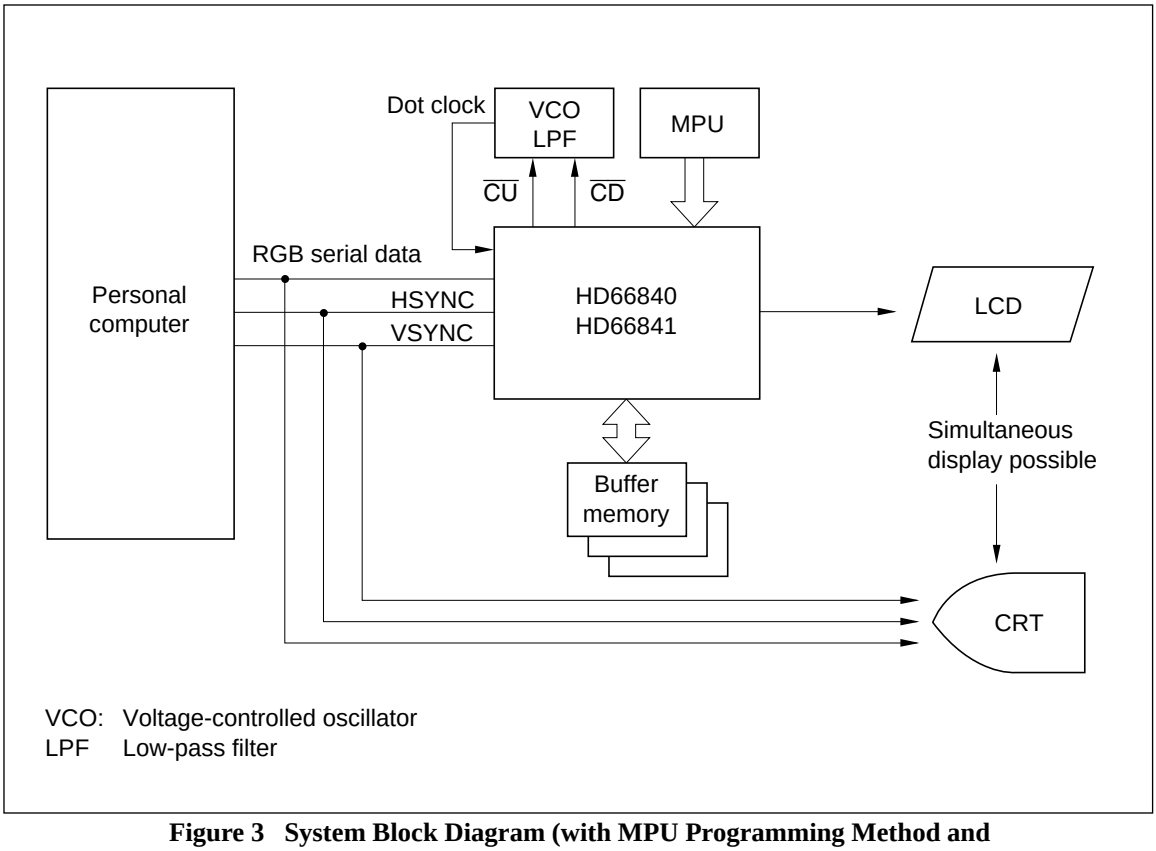


Figure 3 System Block Diagram (with MPU Programming Method and DOTCLK Generated Internally)

Functional Description

Programming Method

The user may select one of two methods to control the HD66840/HD66841 functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 7 lists the relation between programming method and pins.

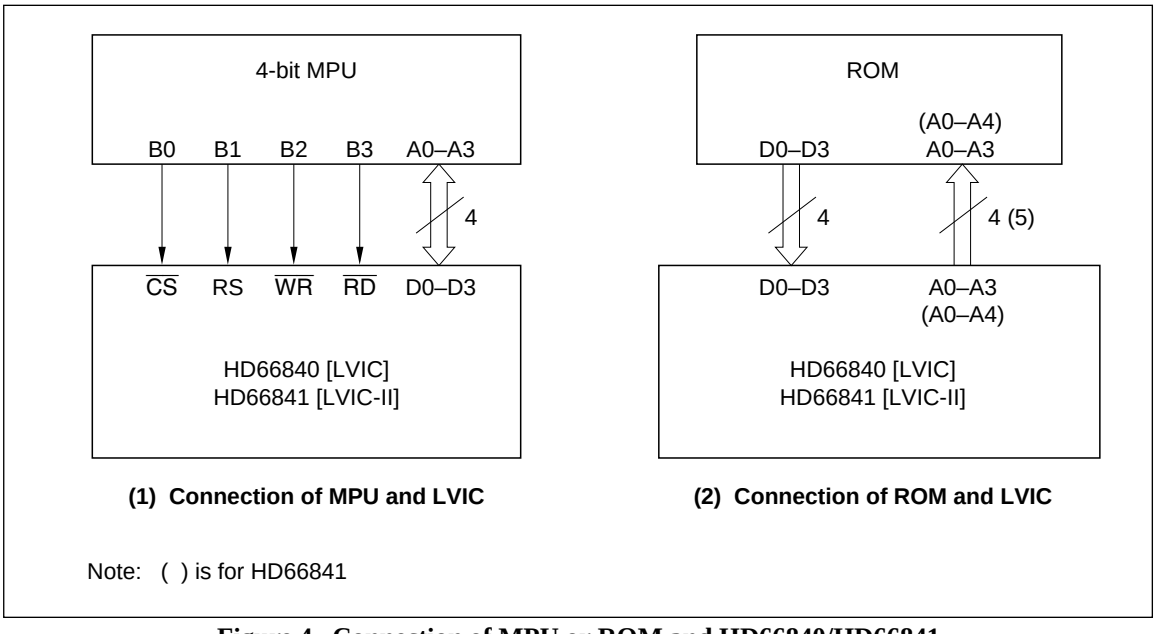
Pin Programming Method: HD66840/HD66841 mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 4 illustrates the connections of MPU or ROM and the LVIC. Figure 3 (1) is an example of using a 4-bit microprocessor, but since the HD66840/HD66841 MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 7 Programming Method Selection

Pins			
PMOD1	**PMOD0**	**Programming Method**	
0	0	Pin programming	
0	1	Internal register programming	With MPU
1	0		With ROM
1	1	Prohibited*	

Note: * This combination is for a test mode and disables display.



(1) Connection of MPU and LVIC

(2) Connection of ROM and LVIC

Note: ( ) is for HD66841

Figure 4 Connection of MPU or ROM and HD66840/HD66841

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, either 640 dots or 720 dots (80 characters or 90 characters) can be selected with the XDOT pin as the number of horizontal displayed characters, and either 200, 350, 400, 480, 512, or 540 lines can be selected with the YL2–YL0 pins as the number of vertical displayed lines. The number of vertical displayed lines can be adjusted by from +0 to +15 lines with the ADJ and F3–F0 pins.

In the internal register programming method, any even number of characters from 4 to 506 (from 32 to 4048 dots) can be selected with the horizontal displayed characters register (R6, R7), and any even number of lines from 4 to 1028 can be selected with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, note that an odd number of lines can also be selected if the screen configuration is single-screen and Y-driver (scan drivers) are positioned on one side of the LCD screen.

The relationship between the LCD screen and the pins and internal registers controlling screen size is shown in figure 5.

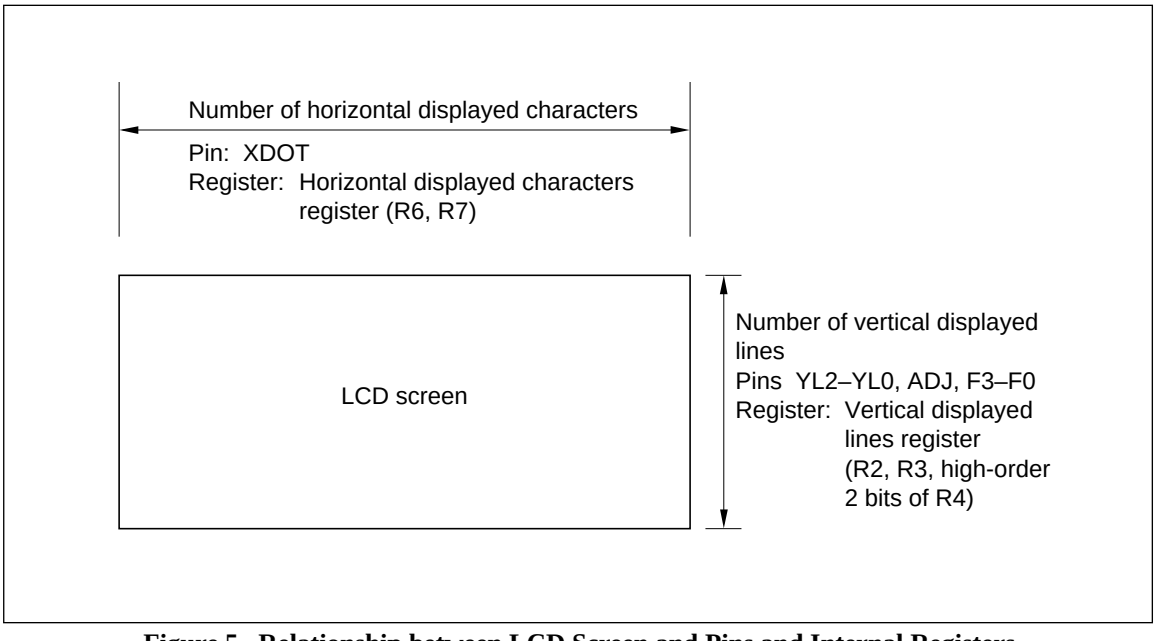


Figure 5 Relationship between LCD Screen and Pins and Internal Registers

Memory Selection

8-, 32-, or 64-kbyte SRAMs can be selected as buffer memory for the HD66840/HD66841. Since the HD66840/HD66841 has a chip select circuit for memory, no external decoder is required. The memory type can be selected with the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1). Memory types and corresponding pin address assignments are listed in table 8.

The memory capacity required depends on screen size and can be obtained from the following expression:

$$\text{Memory capacity (bytes)} = \text{Nhd} \times \text{Nvd}$$

Nhd: Number of horizontal displayed characters (where one character consists of 8 horizontal dots)

Nvd: Number of vertical displayed lines

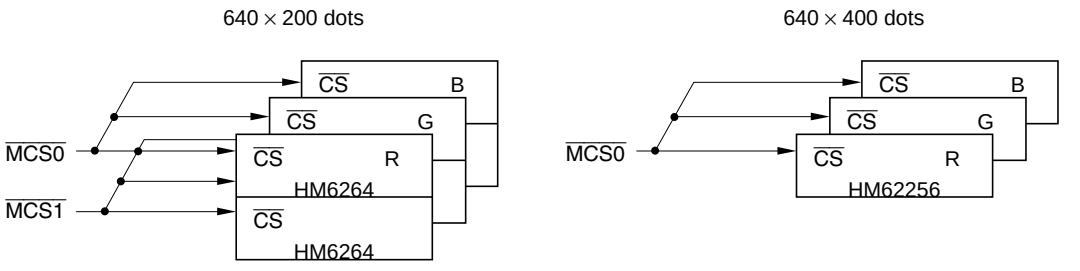
For example, a screen of 640 × 200 dots requires 16-kbytes memory capacity since 80 characters × 200 lines is 16 kbytes. Consequently, each plane requires two HM6264s (8-kbytes memories) in 8-level gray-scale display modes. The $\overline{\text{MCS0}}$ pin must be connected to the $\overline{\text{CS}}$ pin of one of the memory chips in each plane, and the $\overline{\text{MCS1}}$ pin must be connected to the $\overline{\text{CS}}$ pin of the remaining memory chip in each plane. (Figure 6 (a))

A screen of 640 × 400 dots requires a 32-kbytes (256-kbit) memory capacity, so each plane requires an HM62256, which is a 32-kbytes memory. In this case, the $\overline{\text{MCS0}}$ pin must be connected to the $\overline{\text{CS}}$ pin of each memory chip. (Figure 6 (b))

Table 8 Memories and Pin Address Assignments

Pins or Bits					
MS1	**MS0**	**Memory**	**Address Pins**	**Chip Select Pins**	**Address Assignment**
0	0	No memory*	—	—	—
0	1	8-kbyte	MA0-MA12	$\overline{\text{MCS0}}$	$0000–$1FFF
				$\overline{\text{MCS1}}$	$2000–$3FFF
				MA13	$4000-$5FFF
				MA14	$6000-$7FFF
				MA15	$8000-$9FFF
1	0	32-kbyte	MA0–MA14	$\overline{\text{MCS0}}$	$00000–$07FFF
				$\overline{\text{MCS1}}$	$08000-$0FFFF
				MA15	$10000–$17FFF
1	1	64-kbyte	MA0–MA15	$\overline{\text{MCS0}}$	$00000–$0FFFF
				$\overline{\text{MCS1}}$	$10000–$1FFFF

Note: * There are some limitations if no memory is used. Refer to the User Notes section for details.



(a) 16-kbyte Memory Configuration

(b) 32-kbyte Memory Configuration

Figure 6 Screen Size and Memories Configuration

Display Modes

The HD66840/HD66841 supports 16 display modes, depending on the state of the DM3–DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 9 lists display modes.

Table 9 Modes List

Mode No.	Pins				Display Color	LCD Data Output		LCD Driver Setting		Stripe*4	Alternating
	DM3	DM2	DM1	DM0		Data Transfer	Screen Config.	X-Driver*2	Y-Driver*3		
1	0	0	0	0	Monochrome	4-bits	Dual	One side	One side	—	Every frame
2	0	0	0	1			Single				
3*1	0	0	1	0					Both sides		
4	0	0	1	1		8-bits			One side		
5*1	0	1	0	0					Both sides		
6	0	1	0	1	8-level gray scale	4-bits	Dual		One side		
7	0	1	1	0			Single				
8	0	1	1	1		8-bits					
9*1	1	0	0	0	8-color	12-bits (4 bits for R,G,B each)				Vertical	Every line
10*1	1	0	0	1					Both sides		
11*1	1	0	1	0				Both sides	One side		
12*1	1	0	1	1					Both sides		
13*1	1	1	0	0				One side	One side	Horizontal	
14*1	1	1	0	1					Both sides		
15*1	1	1	1	0				Both sides	One side		
16*1,5	1	1	1	1					Both sides		
16*6	1	1	1	1			Dual	One side	One side	Vertical	Every frame

Notes: 1. For TFT-type LCD
2. Data output driver
3. Scan driver
4. Refer to “Display Color, 8-Color Display”
5. Declare to HD66840
6. Declare to HD66841

Display Color

The HD66840/HD66841 converts the RGB color data normally used for CRT display into monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to 5): The HD66840/HD66841 displays two colors: black (display on) and white (display off). As shown in table 10, the CRT display RGB data is ORed to determine display on/off.

8-Level Gray Scale Display (Mode 6 to 8): The HD66840/HD66841 thins out data on certain lines or dots to provide an 8-level gray-scale display based on CRT display color (luminosity). The relationship between CRT display color (luminosity) and LCD gray scale (contrast) is shown in table 11.

This relationship corresponds to the default values in palette registers; the correspondence between color and gray scale can be changed by writing data into palette registers.

Table 10 Monochrome Display

CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White

Table 11 8-Level Gray Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Color	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow			
0	1	1	Cyan			
0	1	0	Green			
1	0	1	Magenta			
1	0	0	Red			
0	0	1	Blue			
0	0	0	Black	Low	White	Weak

8-Color Display (Mode 9 to 16): The HD66840/HD66841 displays 8 colors through red (R), green (G), and blue (B) filters placed on liquid-crystal cells. The eight colors are the same as those provided by a CRT display. As shown in figure 7, 8-color display has two stripe modes: horizontal stripe mode in which the HD66840/HD66841 arranges RGB data horizontally for horizontal filters and vertical stripe mode in which it arranges RGB data vertically for vertical filters. Three cells express one dot in both modes.

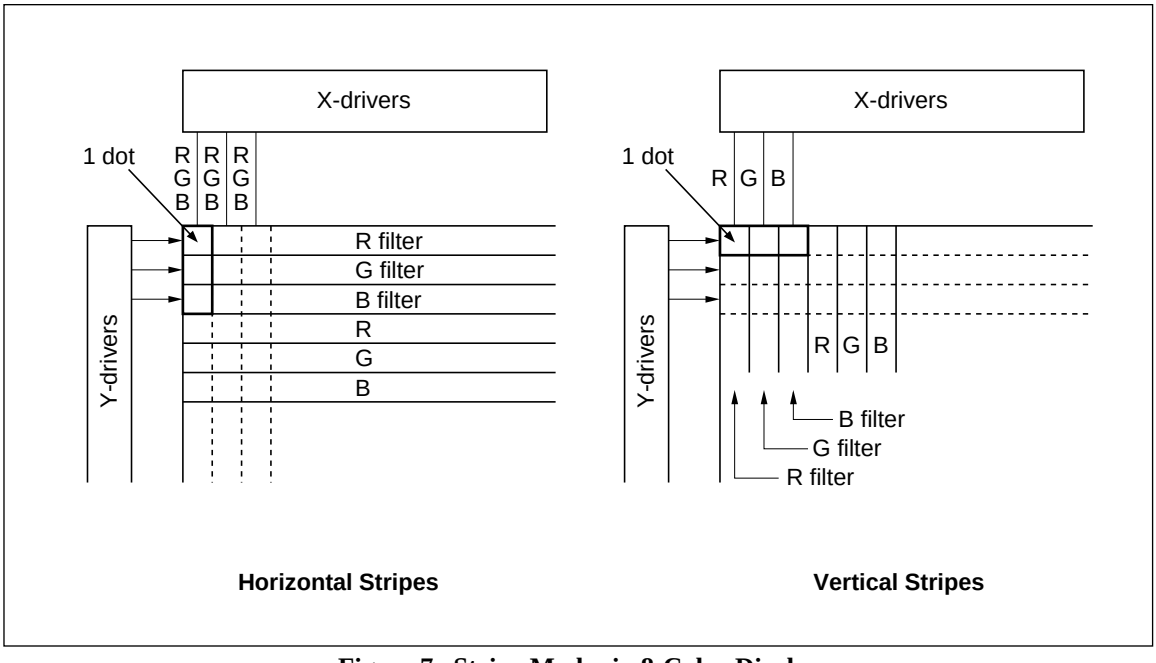


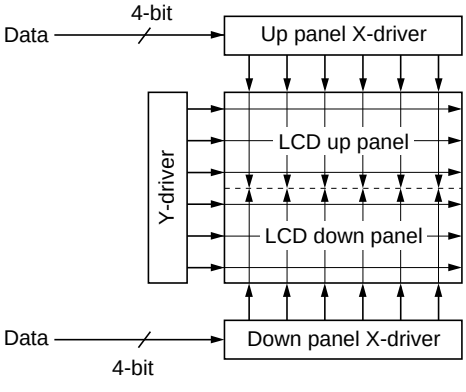
Figure 7 Stripe Modes in 8-Color Display

LCD System Configuration

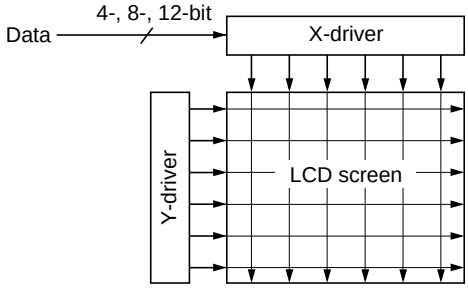
The LVIC-II supports the following LCD system configurations:

- Types of LCD data output
  - — Data transfer: 4-bit, 8-bit, or 12-bits (4 bits each for R, G, and B)
  - — Screen configuration: Single or dual
- LCD driver positions around LCD screen
  - — X-drivers: On one side or on both sides
  - — Y-drivers: On one side or on both sides

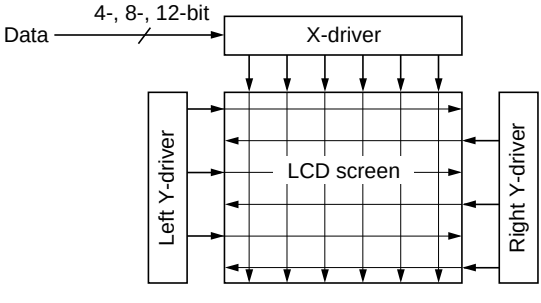
System configurations for different modes are shown in figure 8, and configurations of X- and Y-drivers positioned on both sides an LCD screen are shown in figure 9.



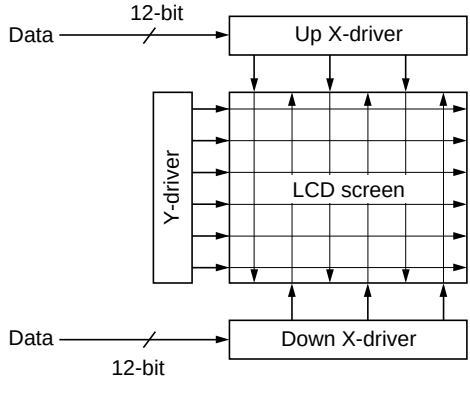
System Configuration for Mode 1 and Modes 6 (4-Bits Data Transfer, Dual Screen, X-Driver and Y-Driver Each One Side)*



System Configuration for Modes 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-Bits Data Transfer, Single Screen, X-Driver and Y-Driver Each on One Side)



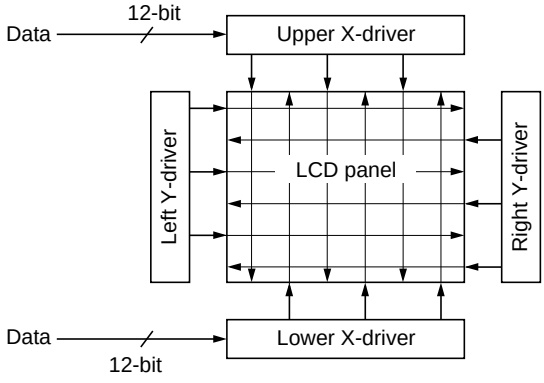
System Configuration for Modes 3, 5, 10, and 14 (4-, 8-, or 12-Bits Data Transfer, Single Screen, X-Driver on One Side and Y-Driver on Both Sides)



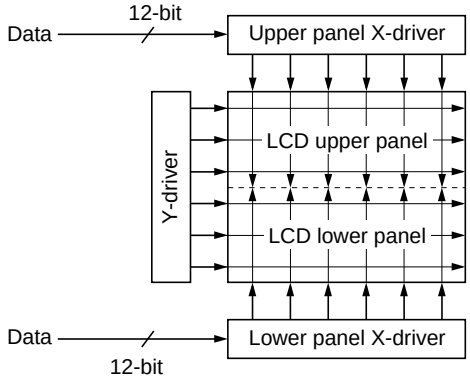
System Configuration for Mode 11 and Mode 15 (12-Bits Data Transfer, Single Screen, X-Driver on Both Sides and Y-Driver on One Side)

Note: * Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 8 System Configurations by Mode



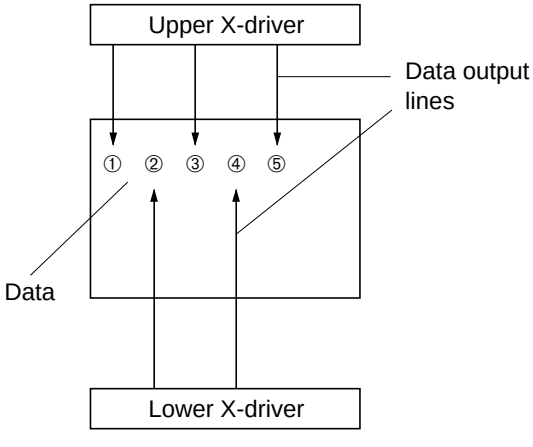
System Configuration for Mode 12 and Mode 16 of HD66840 (12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on Both Sides Each)



System Configuration for Mode 16 of HD66841 (12-Bit Data Transfer, Dual Screen, X-Driver and Y-Driver Each on One Side)*

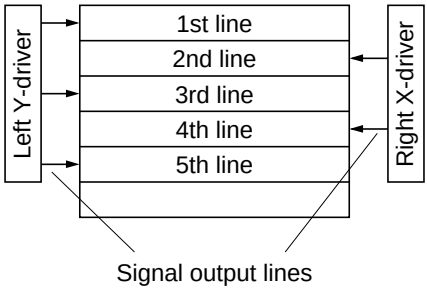
Note: * Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 8 System Configurations by Mode (cont)



(1) X-Drivers Set on Both Sides

Data output lines run alternately from upper and lower X-drivers, increasing the pitch of the lines to twice that for X-drivers positioned on one side.



(2) Y-Drivers Set on Both Sides

Line select signal output lines run alternately from right and left Y-drivers, increasing the pitch of the lines to twice that for Y-drivers positioned on one side.

Figure 9 X- and Y-Drivers Set on Both Sides

LDOTCK Frequency Calculation

The frequency f_L of the LCD dot clock (LDOTCK) can be obtained from the following equation:

$$f_L = (Nhd + 6/m) \times 8 \times Nvd \times f_F$$

Nhd: Number of horizontal characters displayed on LCD
Nvd: Number of vertical lines displayed on LCD
m: Parameter which decided by LCD mode

Screen Configuration	Mode No.	m
Dual	1, 6	2
Single	Other modes	1

f_F: FLM frequency

In this case, f_L must satisfy the following relation, where f_D is the frequency of the dot clock for CRT display (DOTCLK):

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (The phase of LDOTCK must be same to that of DOTCLK when DOTE is high, the phase of LDOTCK must be opposite to that of DOTCLK when DOTE is low. Condition of timing between LDOTCK and DOTCLK must be observed are shown in figure 10.)

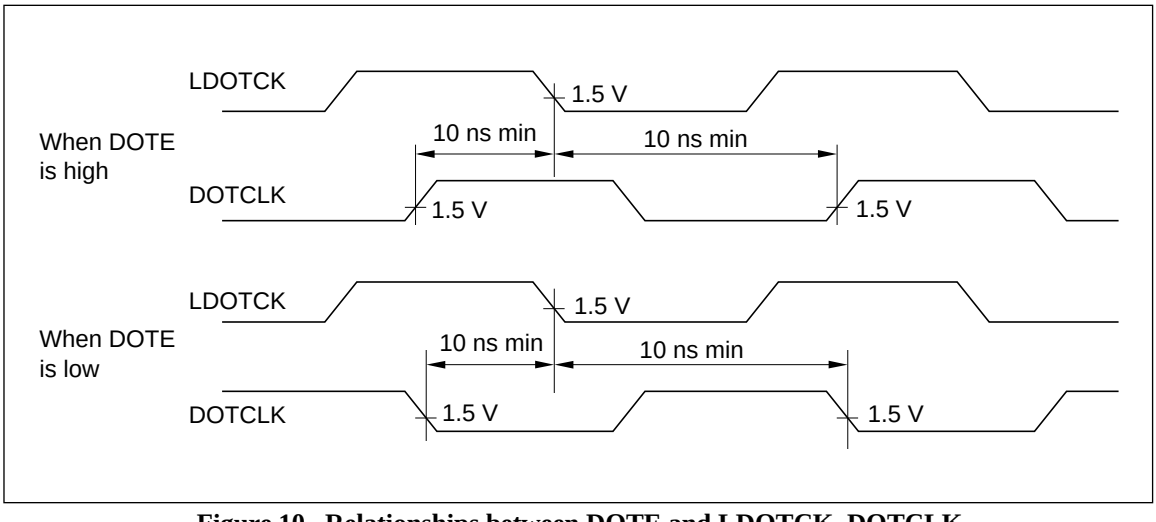


Figure 10 Relationships between DOTE and LDOTCK, DOTCLK

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the HD66840/HD66841 needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The HD66840/HD66841 can generate the display timing signal from HSYNC and V-SYNC. Figure 11 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal back-porch register (R14, R15) respectively.

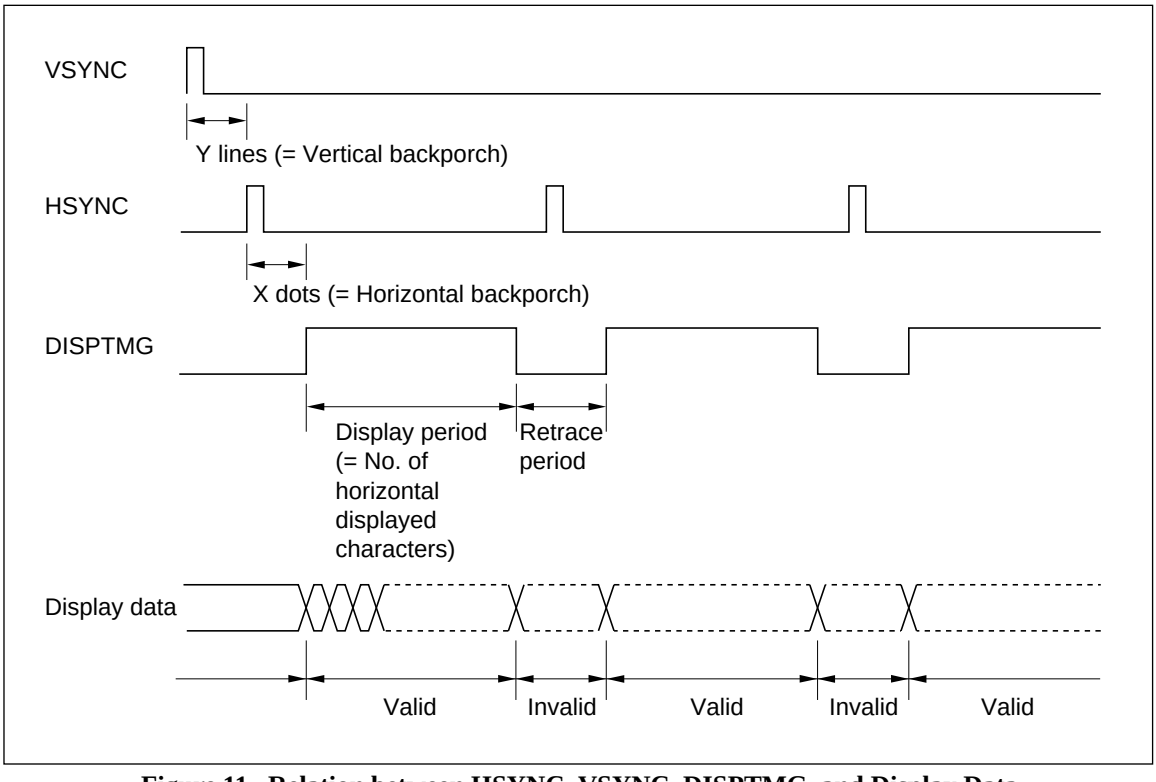


Figure 11 Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal, so it is not usually output from the CRT display plug. Therefore, the HD66840/HD66841 must generate it. The HD66840/HD66841 has a programmable counter and a phase comparator which are parts of a phase-locked lopp (PLL) circuit, and it can generate the dot clock from the H-SYNC signal if a charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

A block diagram of the PLL circuit is shown in figure 12. A PLL circuit is a feedback controller that generates a clock whose frequency and phase are the same as those of a basic clock. The basic clock is the HSYNC signal in this case.

At power-on, the VCO outputs to the programmable counter a signal whose frequency is determined by the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock pulses and the HSYNC signal pulses and output the $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs the $\overline{CU}$ signal if the frequency of the clock is lower than that of the HSYNC signal or if the phase of the clock is behind that of the HSYNC, signal; otherwise it outputs the $\overline{CD}$ signal. The charge pump and LPF apply a voltage to the VCO according to the $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and frequency of the frequency-divided clock match those of the HSYNC signal, making it a stable dot clock.

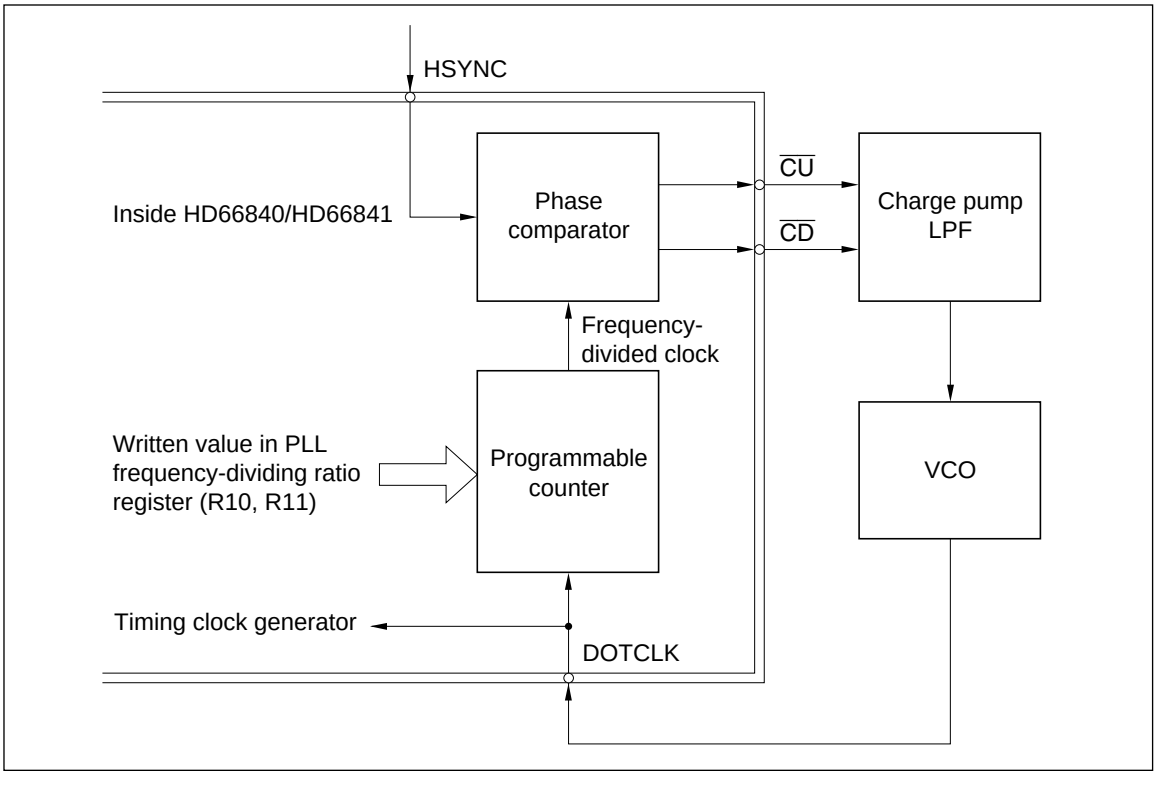


Figure 12 PLL Circuit Block Diagram

Gray-Scale Palette (HD66841 Only)

The HD66841 thins out LCD data on certain dots or lines of an LCD panel every frame, changing integral voltages applied to liquid-crystal cells, to generate intermediate levels of luminosities. Consequently the difference in depth between adjacent gray-scale shades may not be uniform in some cases since voltage-transmittance characteristics vary with different panels. To allow for this, the HD66841 is designed to generate 13 gray-scale levels and provide palette registers that assign desired levels to certain of the eight CRT display colors.

The relationships between gray scales and corresponding effective applied voltages are shown in figure 13 (a). Each gray scale is displayed according to the characteristics of its effective applied voltage and the optical transmittance of the panel (figure 13 (b)). Using the palette registers to select any 8 out of 13 levels of applied voltages enables an optimal gray-scale display conforming to the characteristics of the LCD panel. The palette registers can also be used to provide 4-level grayscale display and reverse display.

Table 12 Default Values of Palette Registers

	CRT Display Data							
Register No.	**R**	**G**	**B**	**Register Name**	**Default Value**			
P1	0	0	0	Black palette	0	0	0	0
P2	0	0	1	Blue palette	0	0	1	0
P3	1	0	0	Red palette	0	1	0	1
P4	1	0	1	Magenta palette	0	1	1	0
P5	0	1	0	Green palette	0	1	1	1
P6	0	1	1	Cyan palette	1	0	0	0
P7	1	1	0	Yellow palette	1	0	1	0
P8	1	1	1	White palette	1	1	0	0

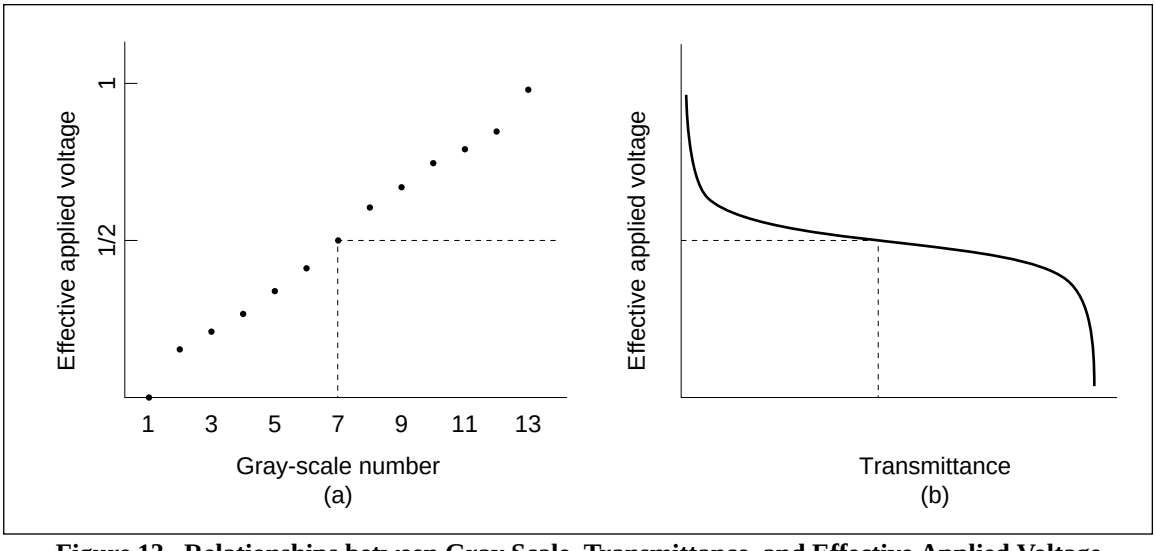


Figure 13 Relationships between Gray Scale, Transmittance, and Effective Applied Voltage

Pin Programming Method

The palette registers cannot be used in the pin programming method.

MPU Programming Method

To change the contents of palette registers in the MPU programming method, set bit 2 (the PS bit) of control register 1 (R0), to 1. Since data registers (M1–R15) cannot be accessed while this bit is 1, set in to 0 before accessing the data registers again. However, note that control register 1 (R0) can be accessed regardless of the setting of the PS bit if $0 is set in the address register (AR).

ROM Programming Method

In the ROM programming method, the HD66841 accesses ROM sequentially from address $0000 to $001F. In this case, write 0 to bit 2 of address $0000 (PS bit) before writing data register values to addresses $0001–$000F, and write 1 to bit 2 of address $0010 (PS bit) before writing palette register values to addresses $0011–$0018.

DIZ Function

The HD66841 thins out data on certain lines or dots every frame to enable gray-scale display. If a checker-board pattern consisting of alternately arranged gray scales of different levels (figure 14) is displayed by a simple dot-basis gray-scale display control method. The display might sometimes seem to “flow” horizontally, depending on the gray-scale and LCD panel characteristics.

The HD66841 automatically checks for such a checker-board section and changes the gray-scale display control method of dot-based data thinning to that of frame-based data thinning, to reduce display flow. Setting bit 3 (DIZ) of control register 1 (R0) to 1 enables this function. In frame-based data thinning, however, flickering might appear with some LCD panels; in that case, select the control method that generates the better display.

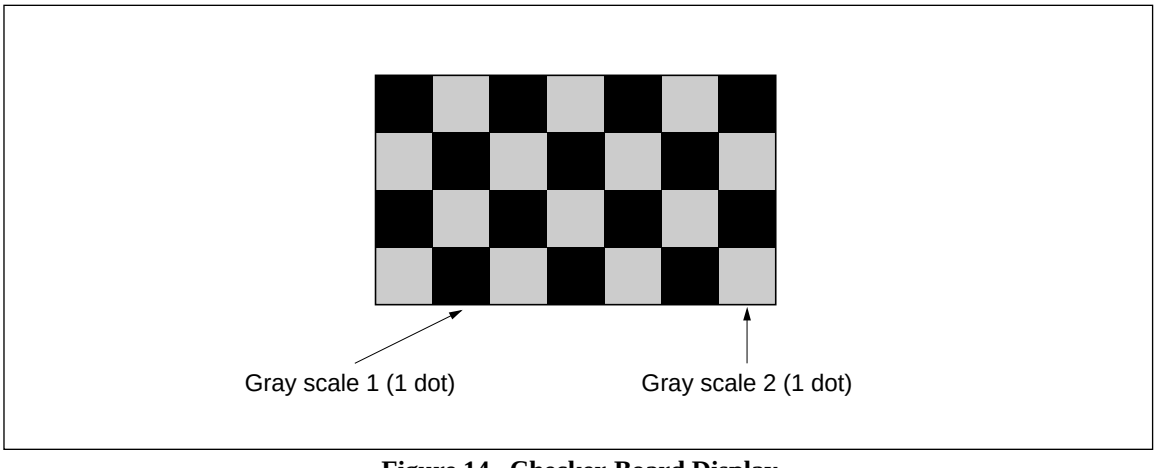


Figure 14 Checker-Board Display

Double-Height Display

The HD66840/HD66841 provides double-height display which doubles the vertical size of characters and pictures (figure 15).

In the TN-type LCD modes (display modes 1, 2, 4, and 6–8), the CL3 signal period is half as long as the CL1 signal period, as shown in figure 16. Consequently, using the CL3 signal instead of the CL1 signal (figure 17) as a line shift clock enables two lines to be selected while X-drivers (data output drivers) are outputting identical data, thus realizing double-height display. However, it should be noted that this display requires the following procedure since the HD66840/HD66841 displays twice as many lines as specified by pins or internal registers:

1. Have the LCD dot clock (LDOTCK) frequency calculated from the number of vertical displayed lines of the LCD panel.

2. Specify half the number of vertical displayed lines of the LCD panel as the number of vertical displayed lines. (For instance, if the number of vertical displayed lines of the LCD panel is 400, specify 200 with the YL2–YL0 pins or the vertical displayed lines register.)

This function is available only in the TN-type LCD modes; it is disabled in the TFT-type LCD modes.

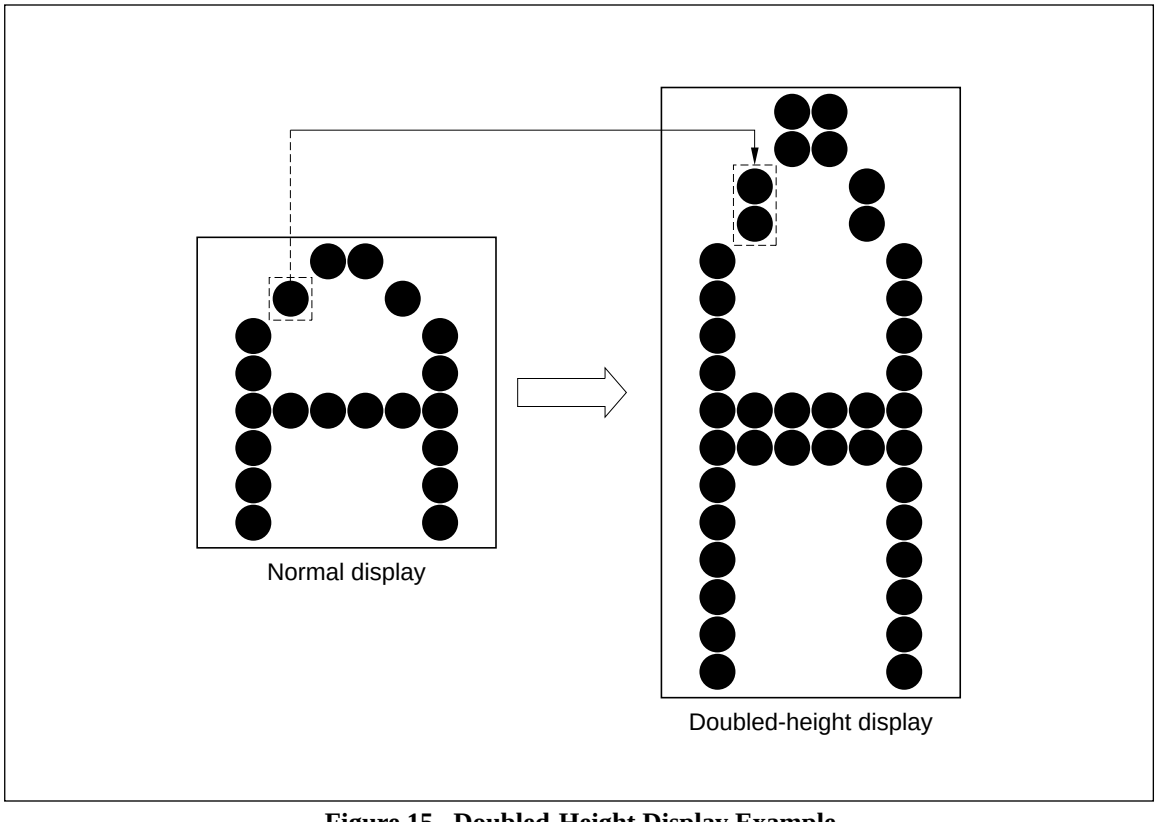


Figure 15 Doubled-Height Display Example

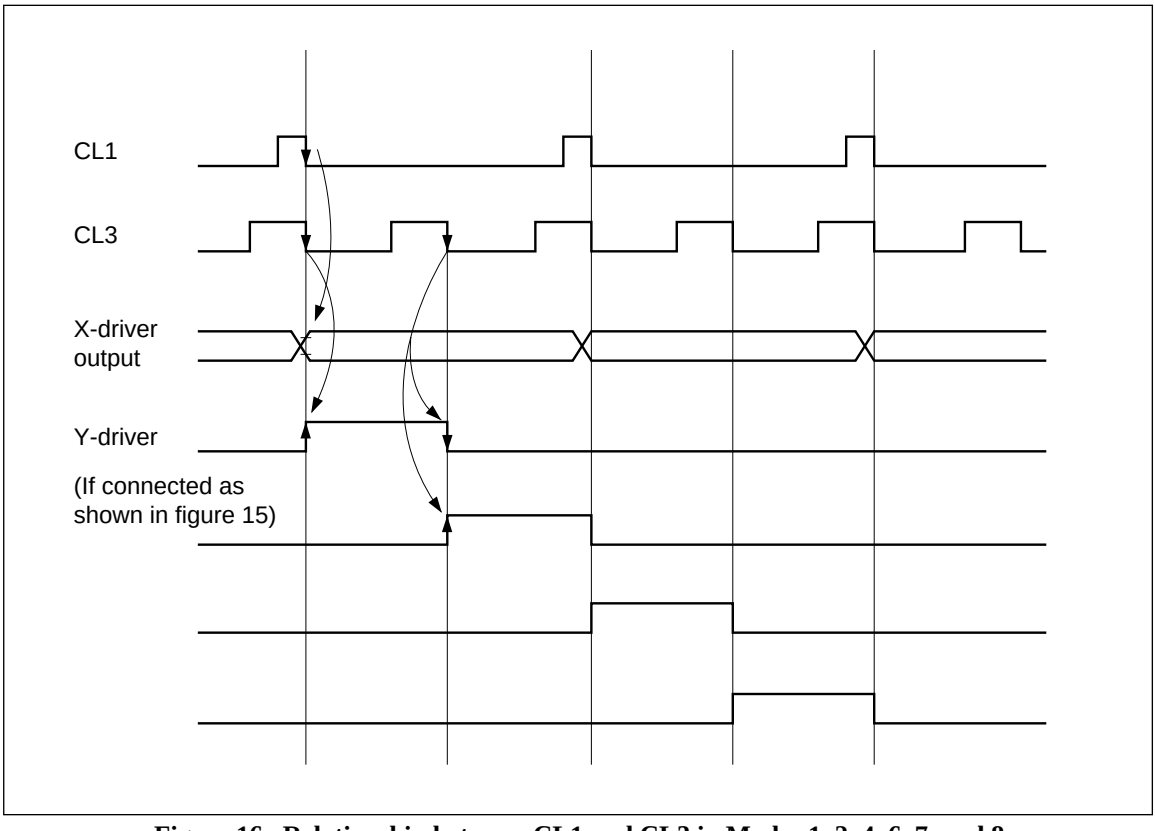


Figure 16 Relationship between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

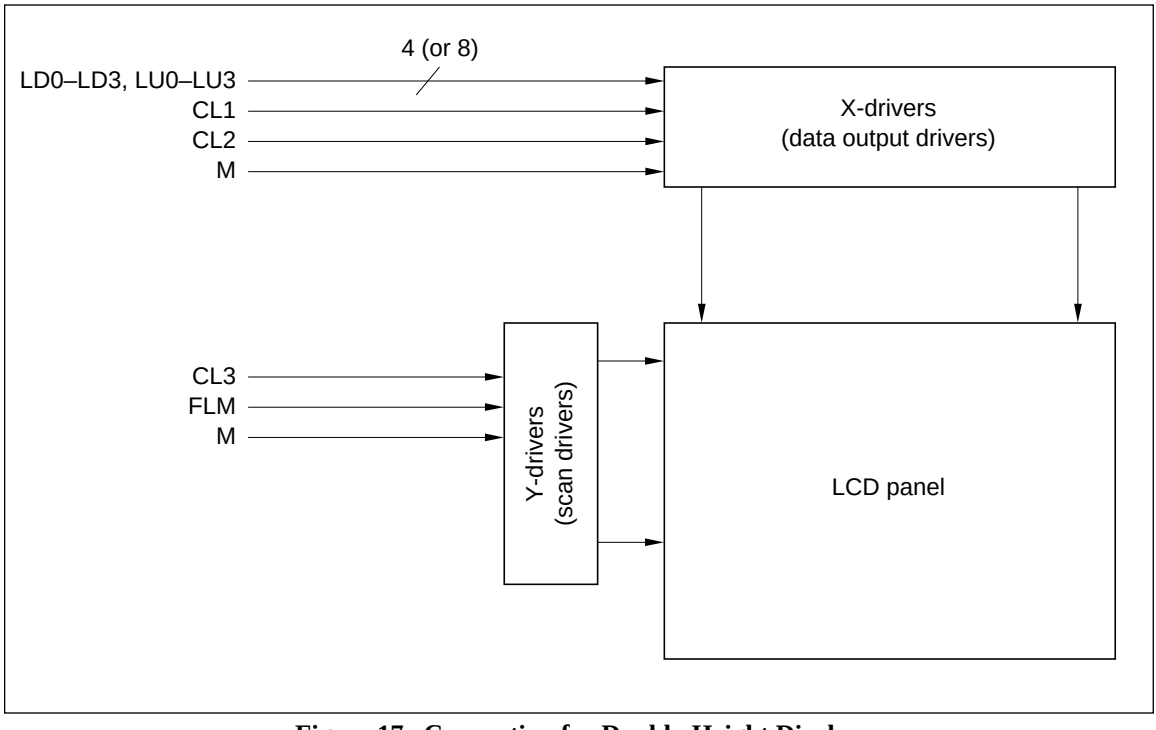


Figure 17 Connection for Double-Height Display

Display Timing Signal Fine Adjustment

If the display timing signal is supplied externally, a phase shift between CRT data and the display timing signal may appear. This is because each signal has its own specific lag. The HD66840/HD66841 can adjust the display timing signal according to pins F0–F3 or the fine adjust register (R9) to correct the phase shift.

The relationships between pins F3–F0, data bits 3 to 0 of the fine adjust register, and the resultant fine adjustments are shown in table 13. The polarity of the number of dots adjusted is given by – (minus) indicates advancing the phase of the display timing signal or + (plus) indicating delaying it. Pin F3 or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Examples of adjusting the display timing signal are shown in figure 18. Since the signal is two dots ahead of the display start position in case (1), F3, F2, F1, and F0 or data bits 3, 2, 1, and 0 of R9 should be set to (1, 0, 1, 0) to delay the signal by two dots. Conversely, since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal by two dots. If there is no need to adjust the signal, a settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 13 Pins, Data Bits of R9, and Fine Adjustment

Pin:	F3	F2	F1	F0	Number of Dots
R9 Bit:	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	–1
		⋮	⋮	⋮	⋮
		1	1	0	–6
		1	1	1	–7
	1	0	0	0	0
		0	0	1	+1
		⋮	⋮	⋮	⋮
		1	1	0	+6
		1	1	1	+7

Note: To use pins to adjust the display timing signal, set the ADJ pin to 1.

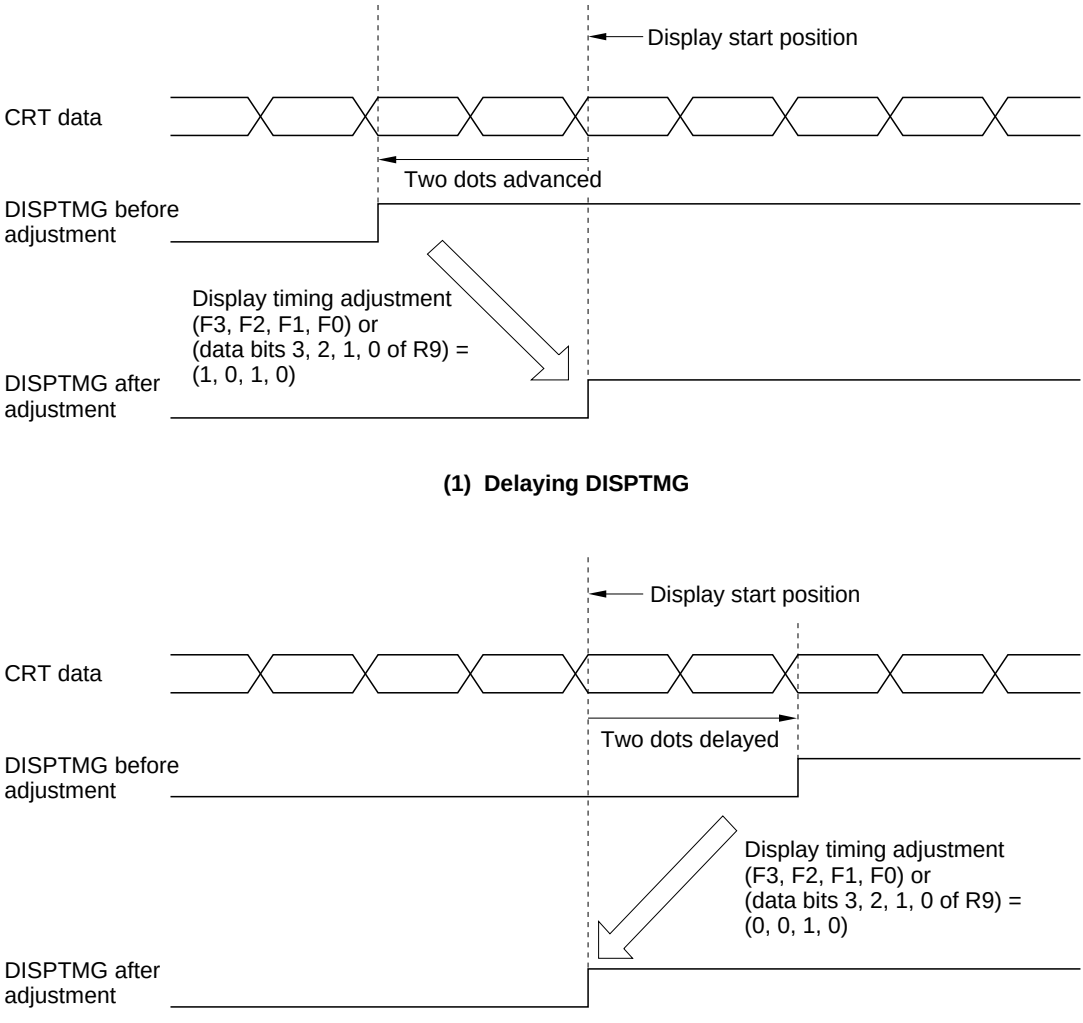


Figure 18 Adjustment of Display Timing Signal

Internal Registers

The HD66840/HD66841 has an address register (AR) and 16 data registers (R0–R15), HD66841 has 8 palette registers (P1–P8). Write the address of a register to be used into the address register (AR). (HD66841: but only after setting the PS bit of control register 1 (R0) to 0 for a data register or 1 for a palette register.)

The MPU transfers data to the register corresponding to the written address.

Registers are valid only in the internal register programming method, they are invalid (don't care) in the pin programming method.

1. Address Registers (AR)

The address register (figure 19) is used to select one of the 16 data registers (or 8 palette registers: HD66841). It can select any data register (or palette register) according to the register address written to it by the MPU. The address register itself is selected if the RS signal is set low.

2. Control Registers 1 (R0)

Control register (figure 20) is composed of 4 bits whose functions are described below. HD66840 has two invalid bits. Reading from and writing into invalid bits are possible. However, these operations do not affect the LSI function.

- DCK bit

  DCK = 1: The DOTCLK signal generated internally.
  DCK = 0: The DOTCLK signal is supplied externally.

- DSP bit

  DSP = 1: The DISPTMG signal is generated internally.
  DCK = 0: The DSPTMG signal is supplied externally. (However, note that if DCK is 1, the DISPTMG signal is generated internally even if DSP is 0.)

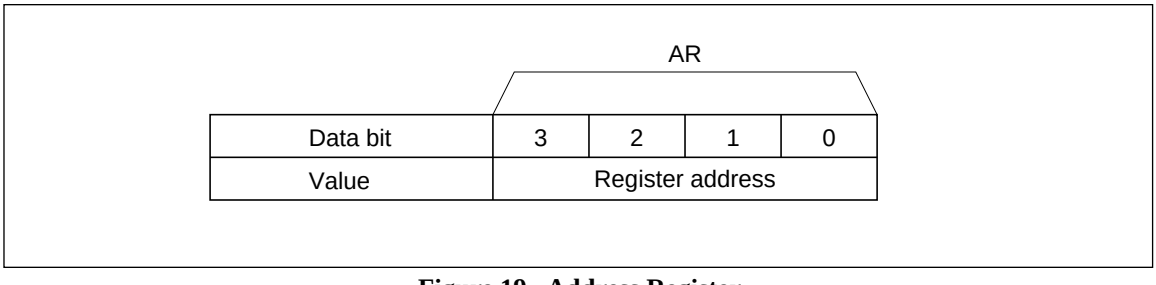


Figure 19 Address Register

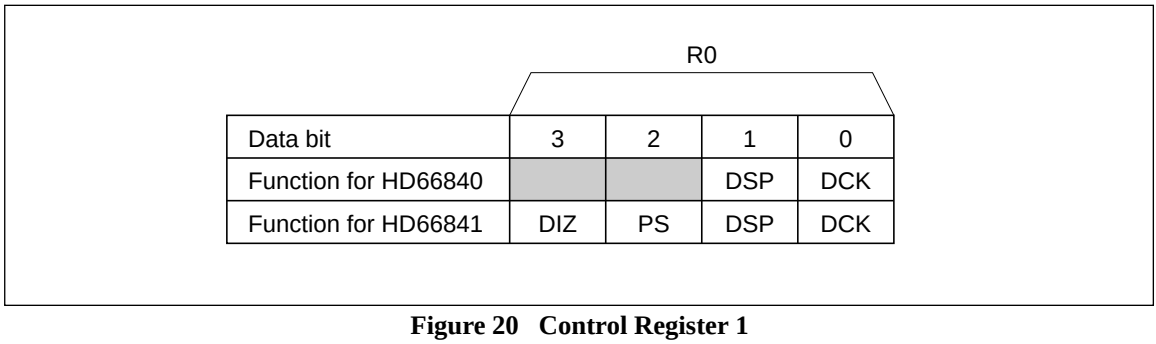


Figure 20 Control Register 1

- PS bit (HD66841's function)

  Specifies access to data registers (R0–R15) or palette registers (P1–P8).

  — In MPU programming mode

  PS = 0: Specifies access to data registers (R0–R15)

  PS = 1: Specifies access to palette registers (P1–P8)

  This register can be always accessed regardless of the PS bit setting, but it cannot be read after the PS bit is set to 1. Read it when PS is 0.

  — In ROM programming mode

  Data for HD66841 internal data registers can be written into $0001 to $000F when bit 2 (the PS bit) of $0000 is set to 0. Data be set into pallete registers can be written into $0011 to $0018 when the PS bit of $0010 is set to 1 (figure 21).

- DIZ bit (HD66841's function)

  Changes the method used to control the gray-scale display of a checker-board pattern.

  DIZ = 0: Data thinned out on a dot basis every frame

  DIZ = 1: Data thinned out on a frame basis every frame

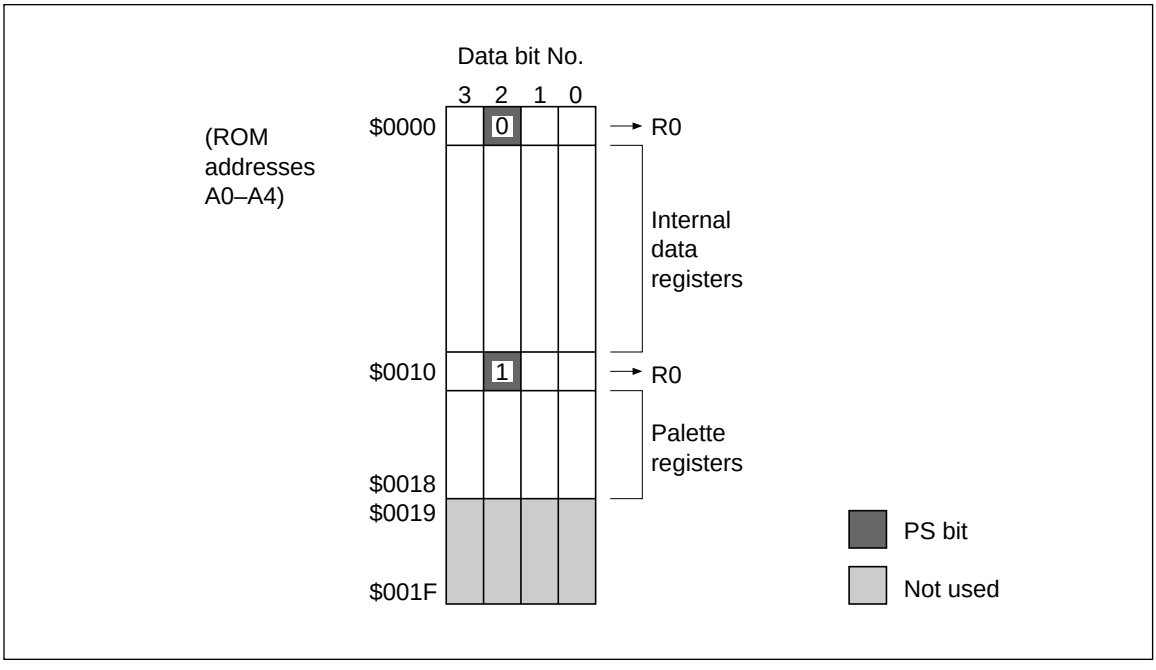


Figure 21 PS Bit Functions in ROM Programming Method

3. Control Register 2 (R1)

Control register 2 (figure 22) is composed of four bits whose functions are described below.

- MC bit

  Specifies M signal alternation.

  MC = 1: The M signal alternates every line.
  MC = 0: The M signal alternates every frame.

- DON bit

  Specifies whether the LCD is on or off.

  DON = 1: LCD on
  DON = 0: LCD off

- MS1, MS0 bits

  Specify buffer memory type.

  (MS1, MS0) = (0, 0): No memory
  (MS1, MS0) = (0, 1): 8-kbytes memory
  (MS1, MS0) = (1, 0): 32-kbytes memory
  (MS1, MS0) = (1, 1): 64-kbytes memory

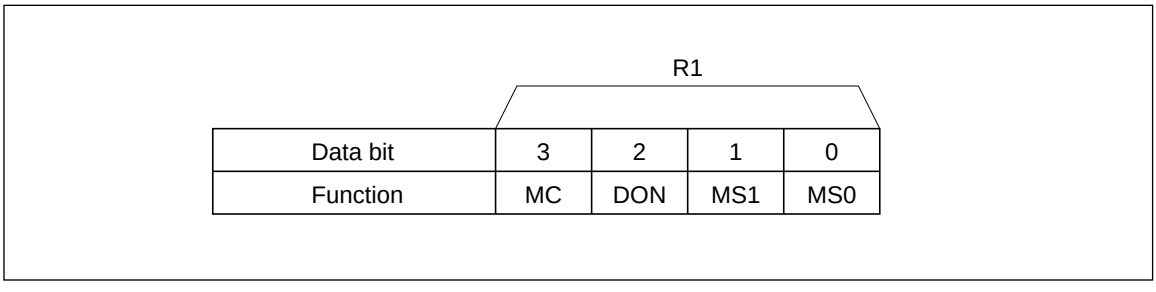


Figure 22 Control Register 2

4. Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4)

The vertical displayed lines register (figure 23) is composed of ten bits (R2, R3, and the high-order two bits of R4). It specifies the number of lines displayed from top to bottom of the screen, called the number of vertical displayed lines. This register can specify both even and odd numbers in single screen modes with Y-drivers positioned on one side, i.e., in display modes 2, 4, and 7-9, but can specify only even numbers in other modes. The value to be written into this register is Nvd – 1, where Nvd is the number of vertical displayed lines.

5. CL3 Period Register (Low-Order 2 Bits of R4, R5)

The CL3 period register (figure 23), is composed of six bits (R5 and the low-order two bits of R4). It specifies the CL3 signal period in 8-collar display modes with horizontal stripes (display modes 13–15), so it is invalid in other modes. CL3 is the clock signal used by the HD66840/HD66841 to output RGB data separately to LCD drivers. The value to be written into this register is Npc – 1, i.e., (Nhd + 6) × 1/3 – 1, where Nhd is the number of horizontal displayed dots × 1/8. If (Nhd + 6) is not divisible by 3, rounded it off.

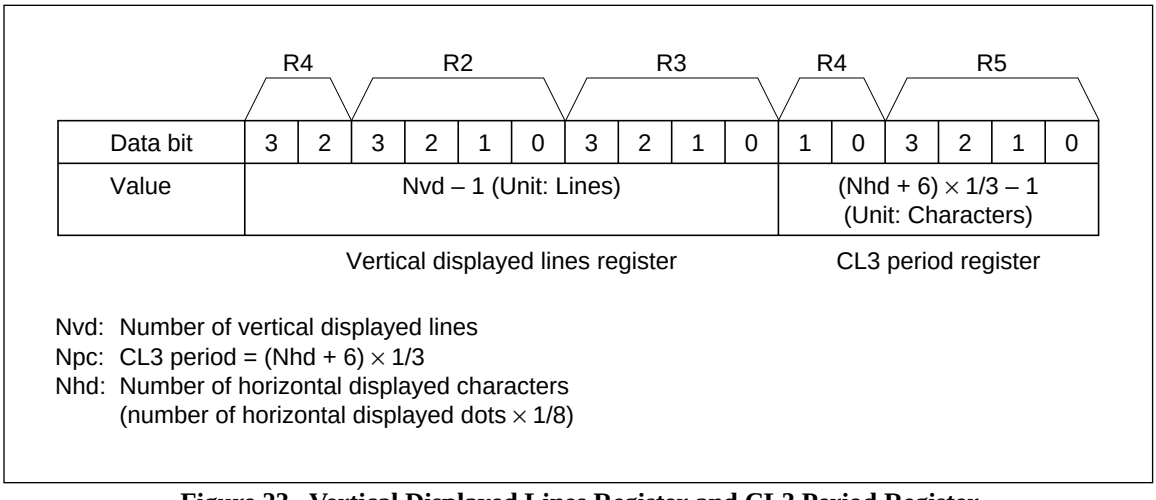


Figure 23 Vertical Displayed Lines Register and CL3 Period Register

6. Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 24) is composed of eight bits (R6, R7). It specifies the number of characters displayed on one horizontal line, called the number of horizontal line, called the number of horizontal displayed characters.

This register can specify even numbers only. In dual-screen modes (display modes 1, 6, and 16), the most significant bit of this register is invalid. When writing into this register, shift (Nhd – 1) in the low-order direction for one bit to cut off the least significant bit. Figure 25 shows how to write a value into the register when Nhd = 90.

7. CL3 Pulse Width Register (R8)

The 4-bit CL3 pulse width register (figure 26) specifies the high-level pulse width of the CL3 signal. In TFT-type LCD modes, a data hold time is necessary and it is determined by the high-level pulse width of the CL3 signal. The CL3 signal is output with the high-level pulse width specified by this register even when the HD66840/HD66841 is not in a TFT-type LCD mode.

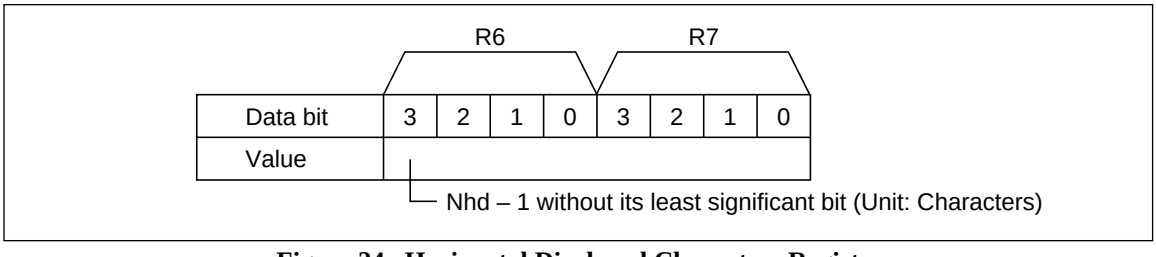


Figure 24 Horizontal Displayed Characters Register

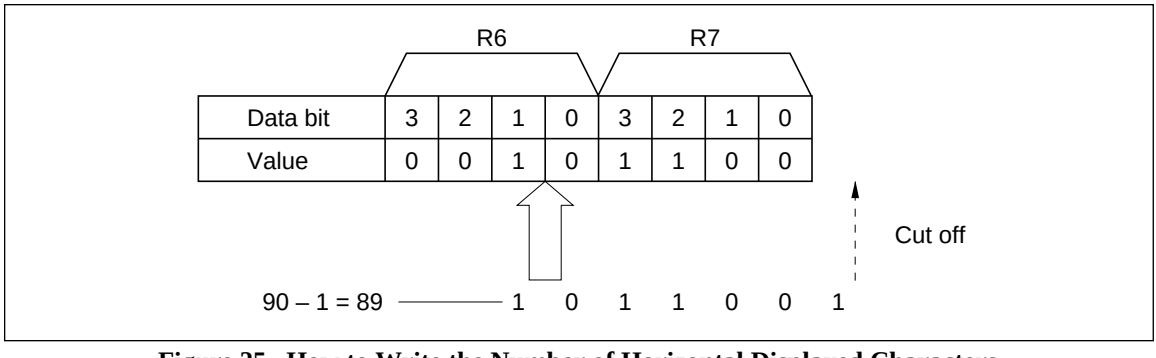


Figure 25 How to Write the Number of Horizontal Displayed Characters

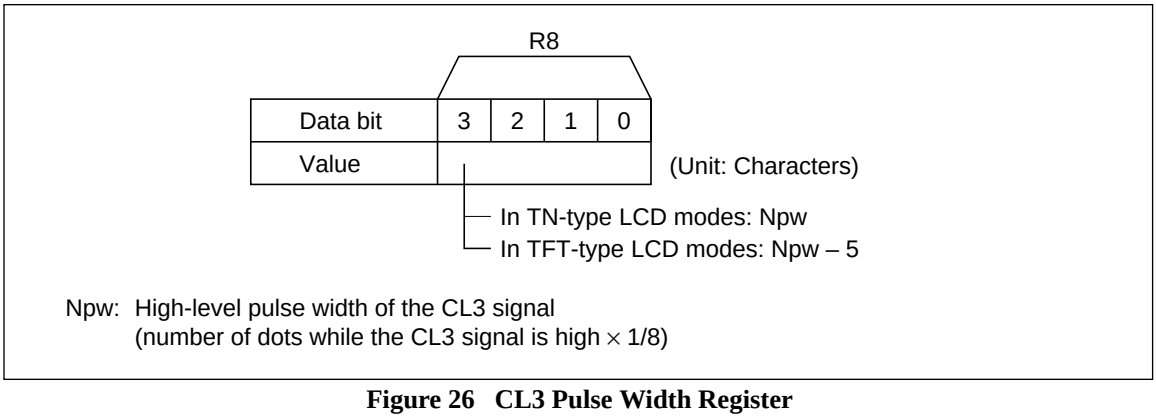


Figure 26 CL3 Pulse Width Register

8. Fine Adjust Register (R9)

The 4-bit fine adjust register (figure 27) adjusts the externally supplied display timing signal (DISPTMG) to synchronize its phase with that of LCD data. The value to be written into this register depends on the interval between the rising edge of the DISPTMG signal and the display start position. For more details, refer to the Display Timing Signal Fine Adjustment section and table 13. This register is invalid if the DISPTMG signal is generated internally, that is, if either the DCK bit or the DSP bit of control register 1 (R0) is 1.

9. PLL Frequency-Division Ratio Register (R10, R11)

The 8-bit PLL frequency-dividing ratio register (figure 28) specifies the PLL frequency-division ratio used for generating dot clock pulses by a PLL circuit. The PLL frequency-division ratio is the ratio of the DOTCLK signal's frequency to the horizontal synchronization signal's (HSYNC) frequency. The LVIC-II generates the DOTCLK signal according to this ratio. This register is invalid if the DOTCLK signal is supplied externally, i.e., it is valid only in the internal register programming method when the DCK bit of control register 1 (R0) is 0.

The value to be written into this register is N_{PLL} – 731, where N_{PLL} is the PLL frequency-division ratio which can be obtained from the following expression:

$$N_{PLL} - 731 = Ncht \times n - 731$$

Ncht: Total number of horizontal characters on CRT (total number of horizontal dots on CRT × 1/n)

n: Horizontal character pitch (number of horizontal dots making up a character)

Ncht can be also obtained from the CRT monitor specifications as follows:

$$Ncht = 1/n \times (\text{DOTCLK frequency} / \text{HSYNC frequency})$$

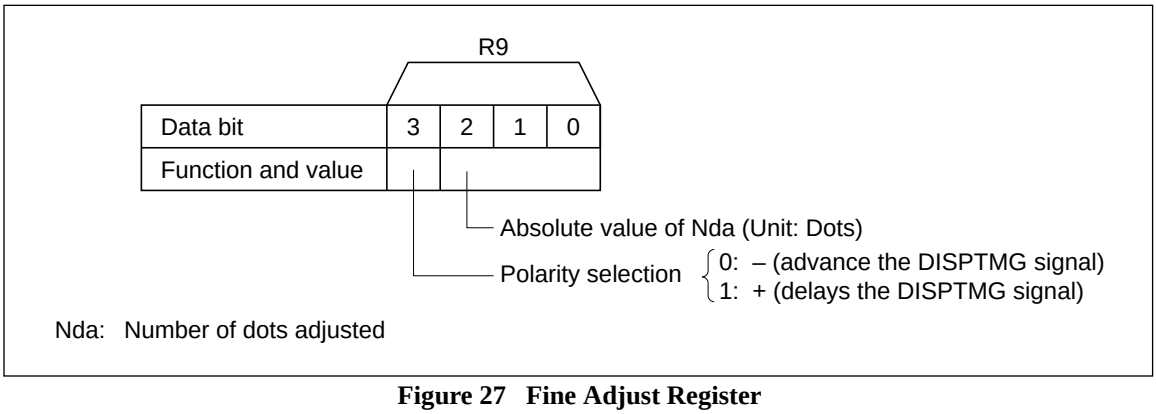


Figure 27 Fine Adjust Register

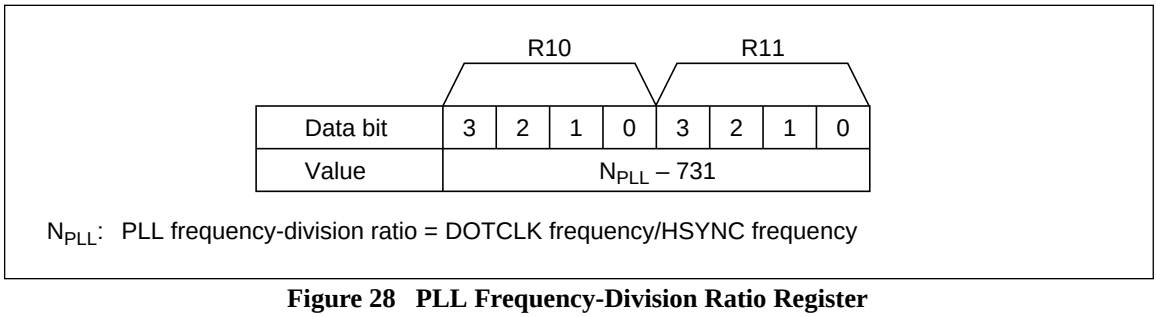


Figure 28 PLL Frequency-Division Ratio Register

10. Vertical Backporch Register (R12, R13)

The 8-bit vertical backporch register (figure 29) specifies the vertical backporch which is the number of lines between the active edge of the vertical synchronization signal (V-SYNC) and the rising edge of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the vertical backporch, refer to the Display Timing Signal Generation section and figure 11.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be regenerated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

11. Horizontal Backporch Register (R14, R15)

The 8-bit horizontal backporch register (figure 30) specifies the horizontal backporch which is the number of dots between the rising edge of the HSYNC signal and that of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the horizontal backporch, refer to Display Timing Signal Generations section and figure 11.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

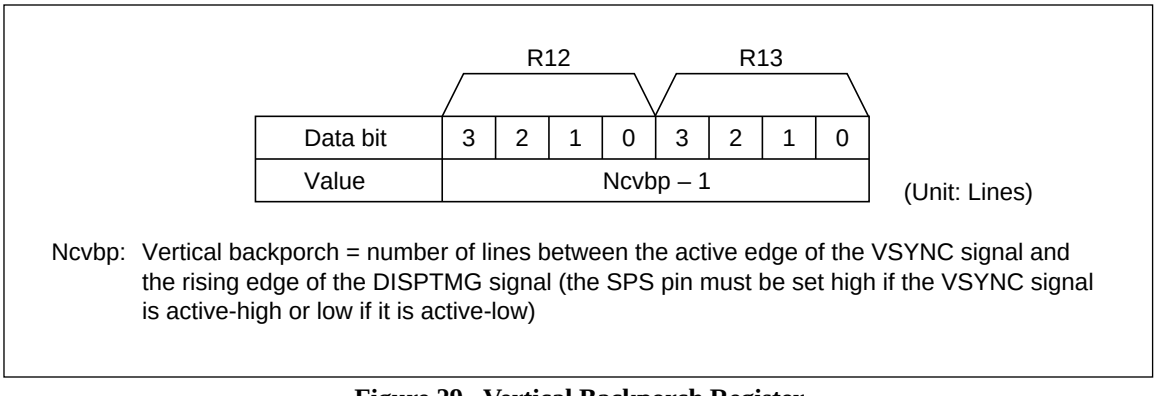


Figure 29 Vertical Backporch Register

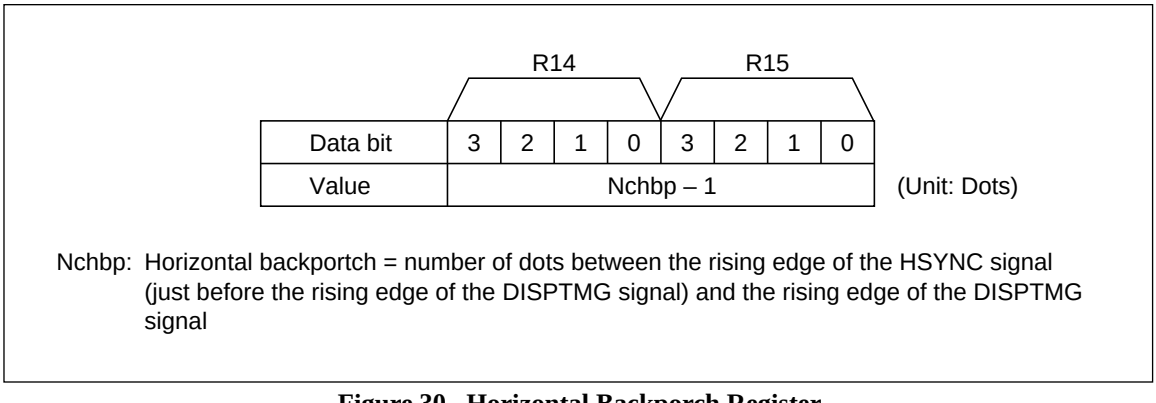
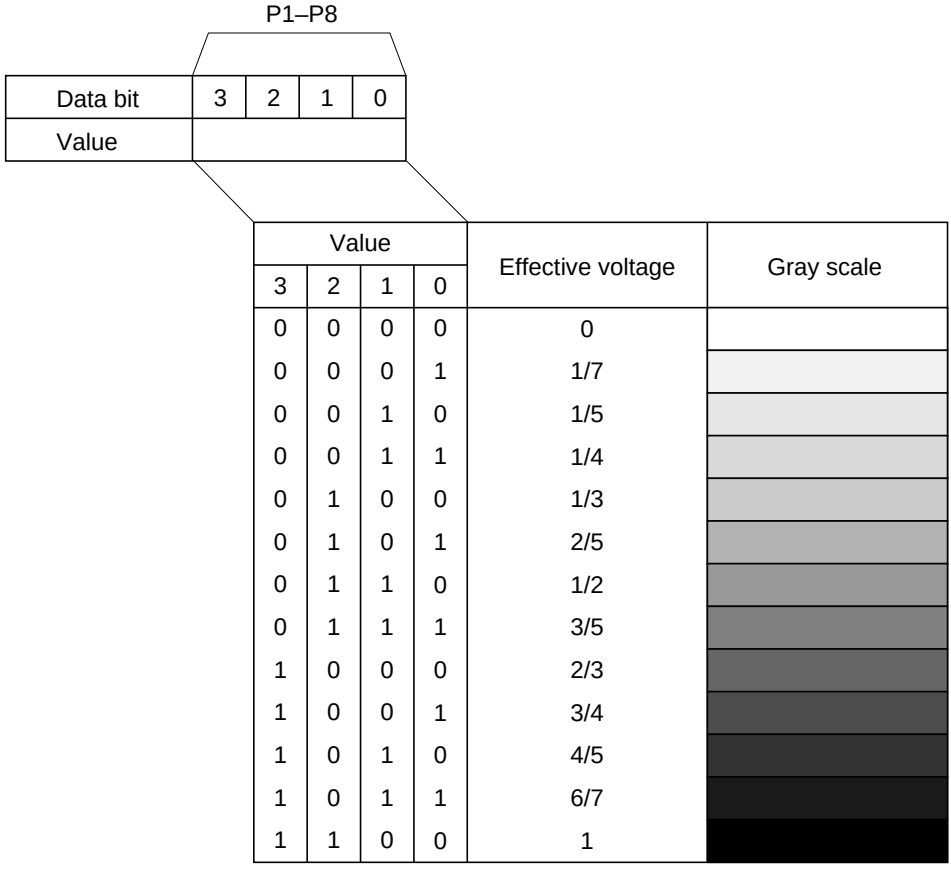


Figure 30 Horizontal Backporch Register

12. Palette Registers (P1–P8) (for HD66841)

The eight 4-bit palette registers (figure 31) each specify one of 13 gray-scale levels for one of the eight colors provided by RGB signals. Use these registers to enable an 8-level gray-scale display appropriate to the characteristics of the LCD panel.



Value				Effective voltage	Gray scale
3	2	1	0		
0	0	0	0	0	
0	0	0	1	1/7	
0	0	1	0	1/5	
0	0	1	1	1/4	
0	1	0	0	1/3	
0	1	0	1	2/5	
0	1	1	0	1/2	
0	1	1	1	3/5	
1	0	0	0	2/3	
1	0	0	1	3/4	
1	0	1	0	4/5	
1	0	1	1	6/7	
1	1	0	0	1	

Figure 31 Palette Registers

Reset

The $\overline{RES}$ signal resets and starts the LVIC-II. The reset signal must be held low for at least 1 µs after power-on.

Reset is defined as shown in figure 32.

State of Pins after Reset

In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. Output signals can be classified into the following five groups, depending on their reset states:

- Retains pre-reset state: CL2, A0–A4
- Driven to high-impedance state (or fixed low if no memory is used): RD0–RD7, GD0–GD7, BD0–BD7
- Fixed high: $\overline{MWE}$, CL4, M, $\overline{CU}$, $\overline{CD}$, $\overline{MCS1}$
- Fixed low: MA0–MA12, R0–R3, G0–G3, B0–B3, CL3, FLM
- Fixed high or low, depending on the memory used (table 14): MA13–MA15, $\overline{MCS0}$

State of Registers after Reset

The $\overline{RES}$ signal does not affect data register contents, so the MPU can both read from and write to data registers, even after reset. Registers will retain their pre-reset contents until they are rewritten.

The HD66841's palette registers, are usually set to their default values by a reset. For the default values, refer to the Gray-Scale Palette section and table 12.

Memory Clear Function

After a reset, the HD66840/HD66841 writes 0s in the memory area specified by pins or register bits MS0 and MS1 (table 8).

Table 14 State of Pins after Reset and Memory Type

Memory Type	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbytes memory	High	High	High	Low
32-kbytes memory	Low	Low	High	Low
64-kbytes memory	Low	Low	Low	Low

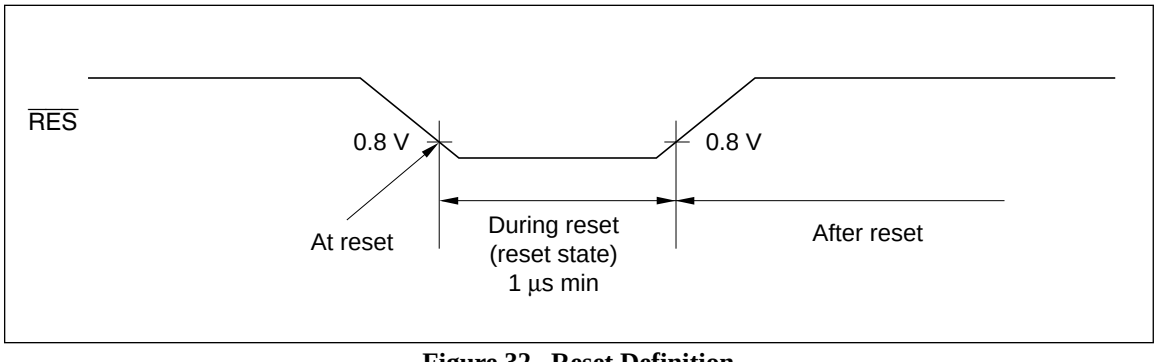


Figure 32 Reset Definition

User Notes

1. The following limitations are imposed if no memory is used (MS = 0, MS1 = 0).

   a. Dual-screen display modes are disabled.

      (HD66840: modes 1 and 6)
      (HD66841: modes 1, 6 and 16)

   b. LCD systems eith Y-drivers on both sides are disabled, even if a mode for system with Y-drivers on both sides is selected.

      (HD66840: modes 3, 5, 10, 12, 14, or 16)
      (HD66841: modes 3, 5, 10, 12, or 14)

      The HD66840/HD66841 operates in exactly the same way as in the corresponding mode for a system with Y-drivers on one side.

      (HD66840: modes 2, 4, 9, 11, 13, or 15)
      (HD66841: modes 2, 4, 9, 11, or 13)

      The CL4 pin must be left disconnected in this case.

2. With the internal register programming method, the operation of the HD66840/HD66841 after a reset cannot be guaranteed until its internal registers have been written to.

3. The memory clear function might not work normally at power-on or after a reset if the MS0 and MS1 pins or bits are not set correctly to the value corresponding to the type memory being used.

4. Since the HD66840/HD66841 are a CMOS LSI, input pins must not be left disconnected. Refer to the Pin Description and table 1 for details on pin handling.

Programming

The values written in internal registers have the limits listed in table 15. The symbols in the table are defined as shown in table 16 and figure 33.

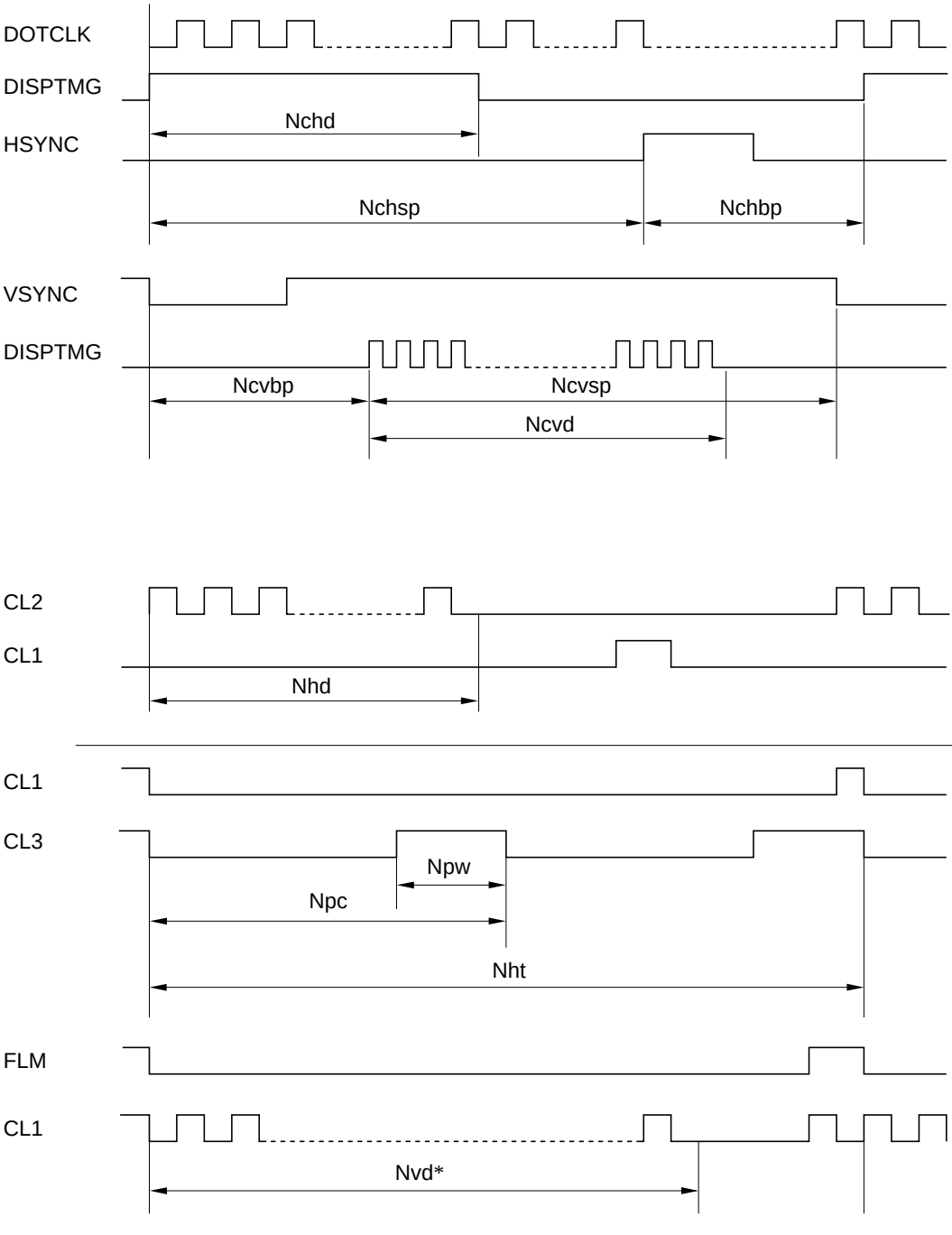
Table 15 Limits on Register Values

Item	Limits	Notes	Applicable Registers
Screen configuration	$4 \le Nvd \le (Ncvbp + Ncvsp) - 1 \le 1024$ $4 \le Nhd \le (Nchbp \times 1/n + Nchsp) - 1 \le 506$	1, 2	R2, R3, R4, R6, R7
	$(Nhd + 6) \times n \times Nvd \times f_{FLM} \le f_{DOTCLK} \le$ 25 MHz (30 MHz: HD66841)	1, 3	R2, R3, R4, R6, R7
CL3 signal control	$1 \le Npw \le (Nhd + 6)/2 - 1$ $1 \le Npw \le Nhd$ $1 \le Npw \le Npc - 1$ $Npc \le (Nhd + 6)/2 - 1$	4 5 6	R4, R5, R6, R7, R8
DISPTMG signal generation	$1 \le Nchbp \le 256$	7	R12, R13
	$1 \le Ncvbp \le 256$	7	R13, R15
No memory	$4 \le Nhd \le Nchsp - 4$	8	R2, R3, R4
	$4 \le Nvd \le Ncvsp - 1$	8	R6, R7

Notes:
1. Lowercase n indicates the horizontal character pitch which is the number of horizontal dots composing a character.
2. $Nhd \le 250$ in the dual screen modes (display modes 1, 6, and 16).
3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency.
   $f_{LDOTCK} < f_{DOTCLK} \times 15/16$ or $f_{LDOTCK} = f_{DOTCLK}$
   (f_{LDOTCK} is the LCD dot clock (LDOTCK) frequency)
4. In display modes 1, 2, 4, and 6–8
5. In display modes 3, 5, and 9–12 when Npw = (value in R8) + 5
6. In display modes 13–15 when Npw = (value in R8) + 5
7. (Value in R14 and R15) $\le (Nchsp \times n + Nchbp) - Nhd \times n - 2$
   (n = horizontal character pitch)
   (Value in R12 and R13) $\le (Ncvsp + Ncvbp) - Nvd - 2$
8. $Nht = Nchsp + (Nchbp \times 1/n)$, $Nvd < Ncvbp + Ncvsp$
   (Nht = (Nhd + 6) if buffer memory is used)
   (n = horizontal character pitch)

Table 16 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on the CRT display (number of horizontal displayed dots on the CRT display × 1/8)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal (number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal × 1/8) (= horizontal synchronization position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal backporch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical backporch)
Ncvsp	Number of lines between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical synch position)
Ncvd	Number of vertical displayed lines on the CRT display
Nhd	Number of horizontal displayed characters on the LCD (number of horizontal displayed dots on the LCD × 1/8)
Npc	Number of characters during one CL3 signal period (number of dots during one CL3 signal period × 1/8)
Npw	Number of characters while the CL3 signal is high (number of dots while the CL3 signal is high × 1/8)
Nht	Number of characters during a CN1 signal period (number of dots during a CL1 signal period × 1/8)
Nvd	Number of vertical displayed lines on the LCD



Note: For a dual screen, the Nvd period is doubled.

Figure 33 Symbol Definitions

Comparisons with HD66840 and HD66841

Gray-Scale Generation Method

The HD66840 shifts display data so that data on different lines will be thinned out in different frames, but the HD66841 shifts display data further so that data on different dots will be thinned out in different frames. This reduces deterioration of display contrast.

Display Mode

Mode 16 of the HD66840 (for 8-color display with horizontal stripes and X- and Y-drivers positioned on both sides of the LCD) has been modified into the following new mode in the HD66841:

- Mode number: 16
- Pin setting: (DM3, DM2, DM1, DM0) = (1, 1, 1, 1)
- Display colors: 8 colors
- LCD data output
  - — 12-bit-based data transfer
  - — Dual screen configuration
- LCD driver settings: X-drivers and Y-drivers set on one side
- Stripes: Vertical
- Alternation mode: Every frame

In this mode, the HD66841 outputs upper screen data and lower screen data alternately, as shown in figure 34. In this case, the CL2 frequency is one quarter of the LDOTCK frequency.

Table 17 Gray-Scale Palette

	HD66840	HD66841
Numbers of registers	16	24 (palette registers have been added to the HD66840's registers)
Selection of correspondence between CRT display colors and gray-scale levels	Impossible	Possible (any of 13 levels assignable to each of 8 colors)

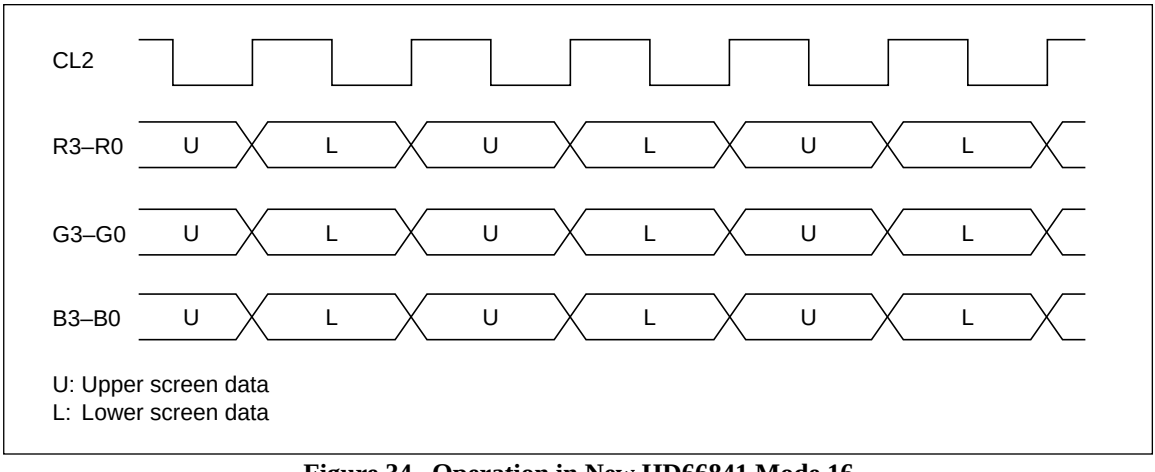


Figure 34 Operation in New HD66841 Mode 16

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C). If these conditions are exceeded, it could affect reliability of the LSI.

2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} – 0.5	V_{CC} + 0.3	V	
	TTL interface*1		2.0	V_{CC} + 0.3		
	TTL interface*4		2.2	V_{CC} + 0.3		
	CMOS interface*1		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface*1, $\overline{RES}$	V_{IL}	–0.3	0.8	V	
	TTL interface*5		–0.3	0.6		
	CMOS interface*1		–0.3	0.3 V_{CC}		
Output high voltage	TTL interface*2	V_{OH}	2.4	—	V	I_{OH} = –200 µA
	CMOS interface*2		V_{CC} – 0.8	—		I_{OH} = –200 µA
Output low voltage	TTL interface*2	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface*2		—	0.8		I_{OL} = 200 µA
Input leakage current	All inputs except I/O common pins*3	I_{IL}	–2.5	2.5	µA	
Three state (off-state) leakage current	I/O common pins*3	I_{TSL}	–10.0	10.0	µA	
Current consumption	—	I_{CC}	—	250	mW	f_{DOTCLK} = 25, 30 MHz*6 Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0–RD7, GD0–GD7, BD0–BD7, D0–D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ/A4, $\overline{CS}$/MS0

CMOS interface inputs: DM0–DM3, DOTE, PMOD0, PMD1, A1/YL0–A2/YL2

2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, MA0–MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$, $\overline{RS}$/ADJ/A4

CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0–R3/LU3, G0/LD0–G3/LD3, B0–B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7

Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0–DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

4. TTL interface: $\overline{WR}$/MS1, LDOTCK, DOTCLK
5. TTL interface: $\overline{WR}$/MS1
6. HD66840: 25 MHz, HD66841: 30 MHz

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20°C to +75°C)

Video Signal Interface

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	T_{CYCD}	40	1000	ns	HD66840
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK cycle time	t_{CYCD}	33	1000	ns	HD66841
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	HD66840/HD66841
DOTCLK fall time	t_{Df1}	—	5	ns	
RGB setup time	t_{VDS}	10	—	ns	
RGB hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Figure 35 except for DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	

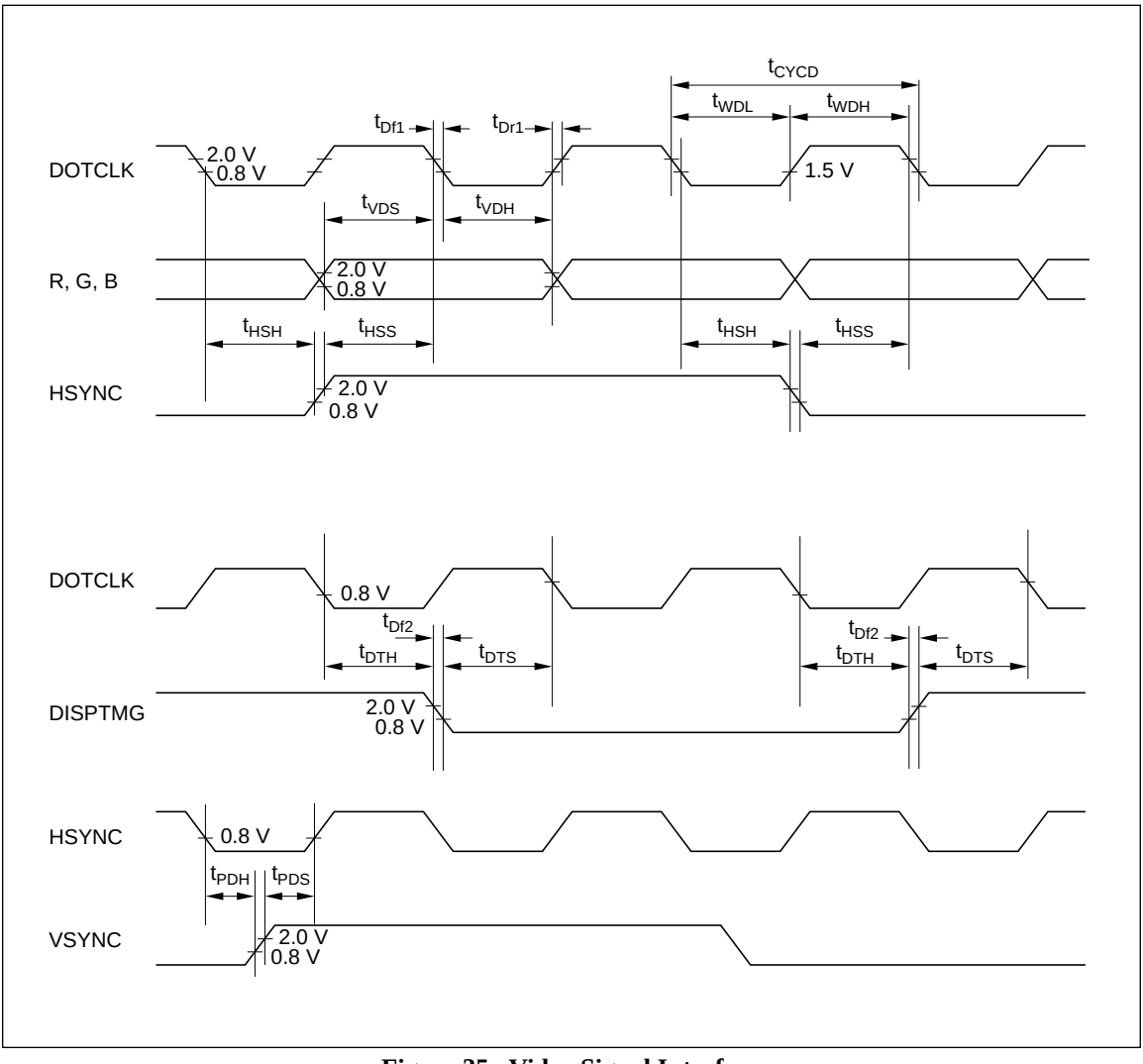


Figure 35 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	5 t_{CYCD} – 50	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 data setup time	t_{SMD}	25	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	6 t_{CYCD} – 50	—	ns
Address setup time	t_{AS}	t_{CYCD} – 30	—	ns
Address hold time	t_{WR}	t_{CYCD} – 30	—	ns
Chip select time	t_{CW}	4 t_{CYCD} – 40	—	ns
Write pulse width	t_{WP}	4 t_{CYCD} – 40	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 output setup time	T_{SMDW}	2 t_{CYCD} – 25	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 40 ns, max 1000 ns) for HD66840.
t_{CYCD} indicates DOTCLK cycle time (min 33 ns, max 1000 ns) for HD66841.

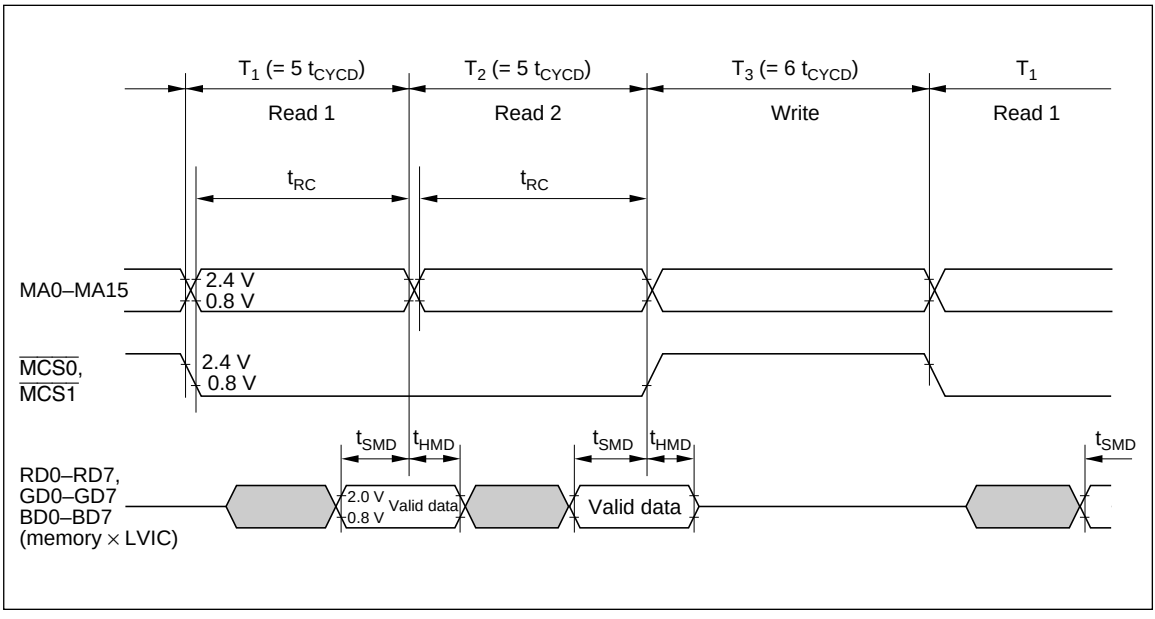


Figure 36 Buffer Memory Interface (RAM Read Timing)

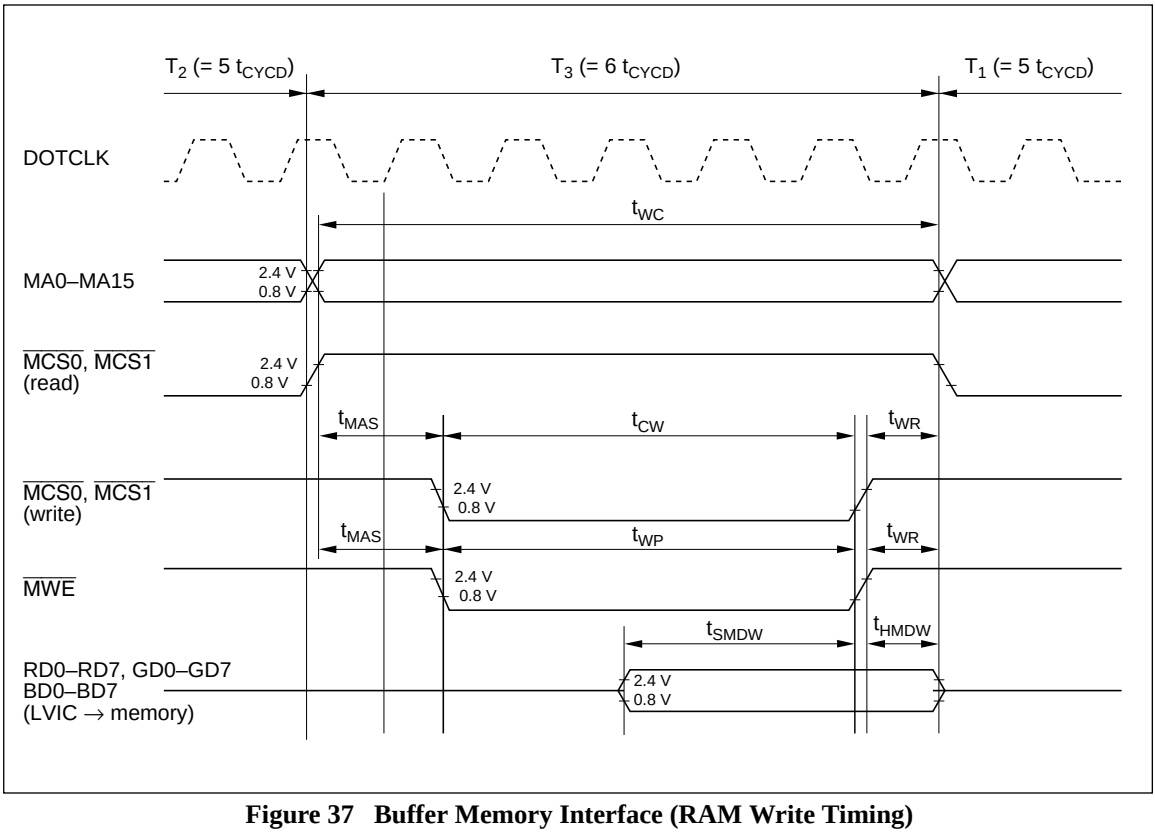


Figure 37 Buffer Memory Interface (RAM Write Timing)

LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t_{WCL2}	166	—	ns
CL2 high-level pulse width	t_{WCL2H}	50	—	ns
CL2 low-level pulse width	t_{WCL2L}	50	—	ns
CL2 rise time	t_{CL2r}	—	30	ns
CL2 fall time	t_{CL2f}	—	30	ns
CL1 high-level pulse width	t_{WCL1H}	200	—	ns
CL1 rise time	t_{CL1r}	—	30	ns
CL1 fall time	t_{CL1f}	—	30	ns
CL1 setup time	t_{SCL1}	500	—	ns
CL1 hold time	t_{HCL1}	200	—	ns
FLM hold time	t_{HF}	200	—	ns
M output delay time	t_{DM}	—	300	ns
Data delay time	t_{DD}	–20	20	ns
LDOTCK cycle time	t_{WLDOT}	41	—	ns

Note: All the values are measured at f_{CL2} = 6 MHz.

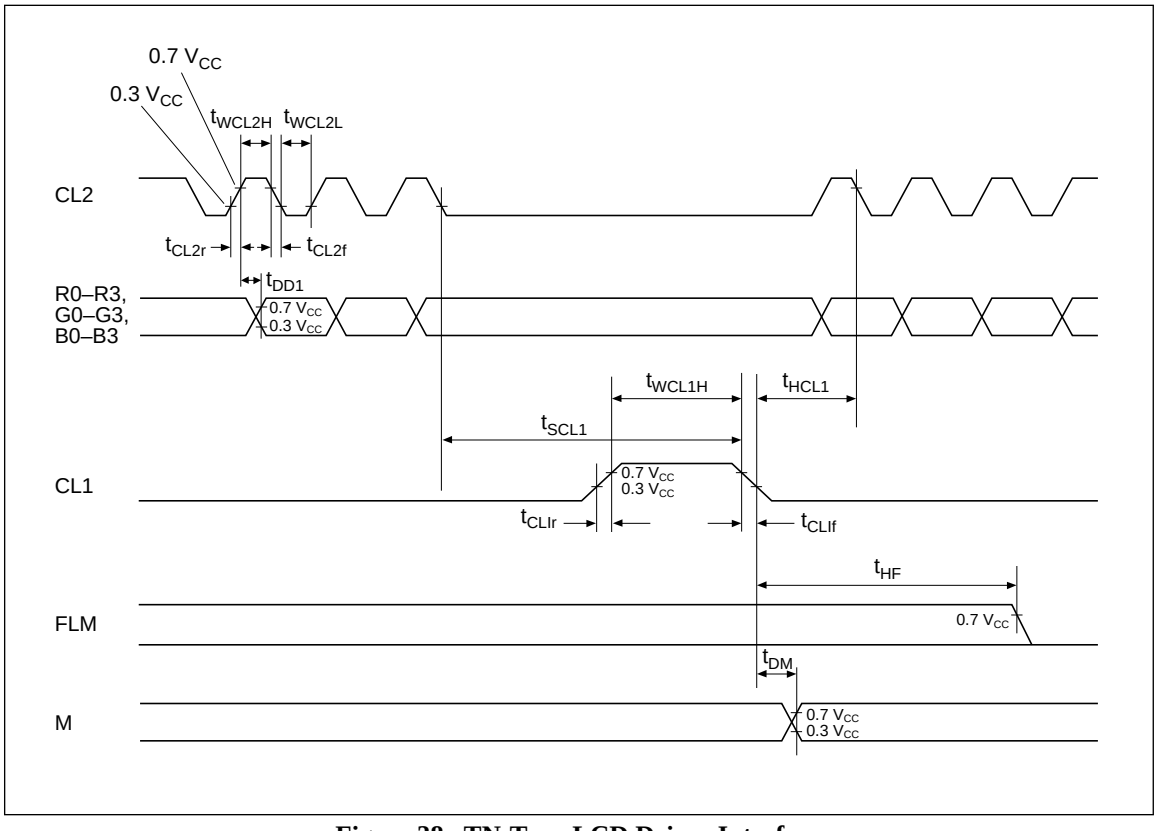


Figure 38 TN-Type LCD Driver Interface

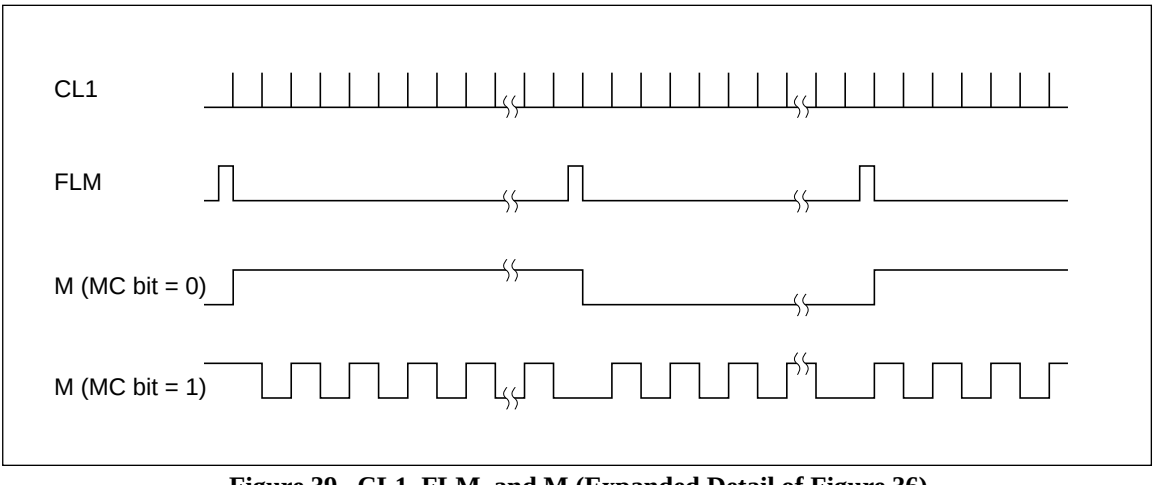


Figure 39 CL1, FLM, and M (Expanded Detail of Figure 36)

LCD Driver Interface (TFT-Type LCD Driver 1) for HD66840

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X drivers on one side)	t_{TCL2S}	160	—	ns	Figure 40, 41
CL2 high-level width (X drivers on one side)	t_{TCL2HS}	30	—	ns	
CL2 low-level width (X drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X drivers on both side)	t_{TCL2D}	320	—	ns	
CL2 high-level width (X drivers on both side)	t_{TCL2HD}	80	—	ns	
CL2 low-level width (X drivers on both side)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	–20	20	ns	
Data setup time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	40	—	ns	

LCD Driver Interface (TFT-Type LCD Driver 2) for HD66841

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X-drivers on one side)	t_{TCL2S}	133	—	ns	Figure 40, 41
CL2 high-level pulse width (X-drivers on one side)	t_{TCL2HS}	30	—	ns	
CL2 low-level pulse width (X-drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X-drivers on both sides)	t_{TCL2D}	266	—	ns	
CL2 high-level pulse width (X-drivers on both sides)	t_{TCL2HD}	80	—	ns	
CL2 low-level pulse width (X-drivers on both sides)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	–20	20	ns	
Data setup time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	33	—	ns	

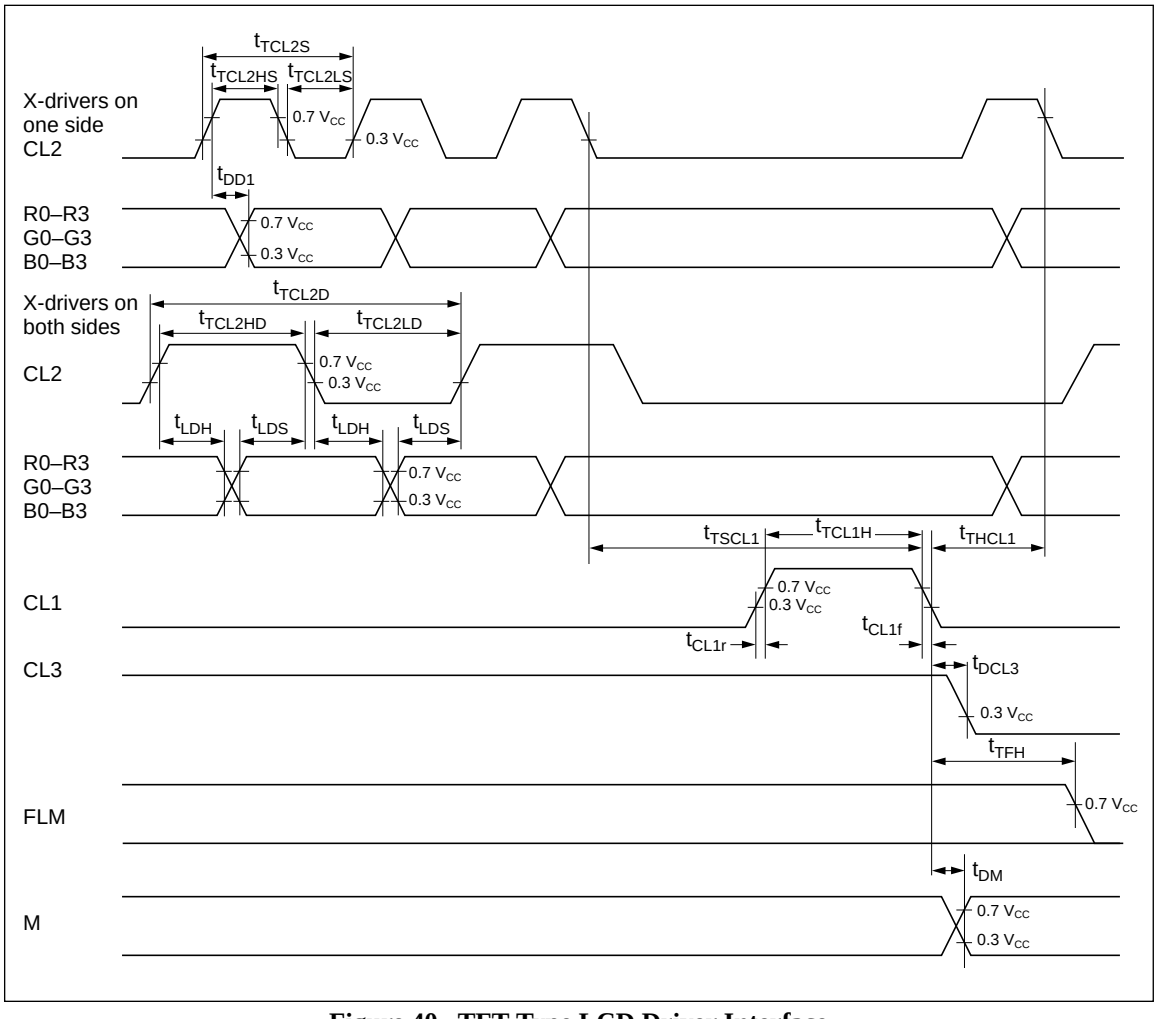


Figure 40 TFT-Type LCD Driver Interface

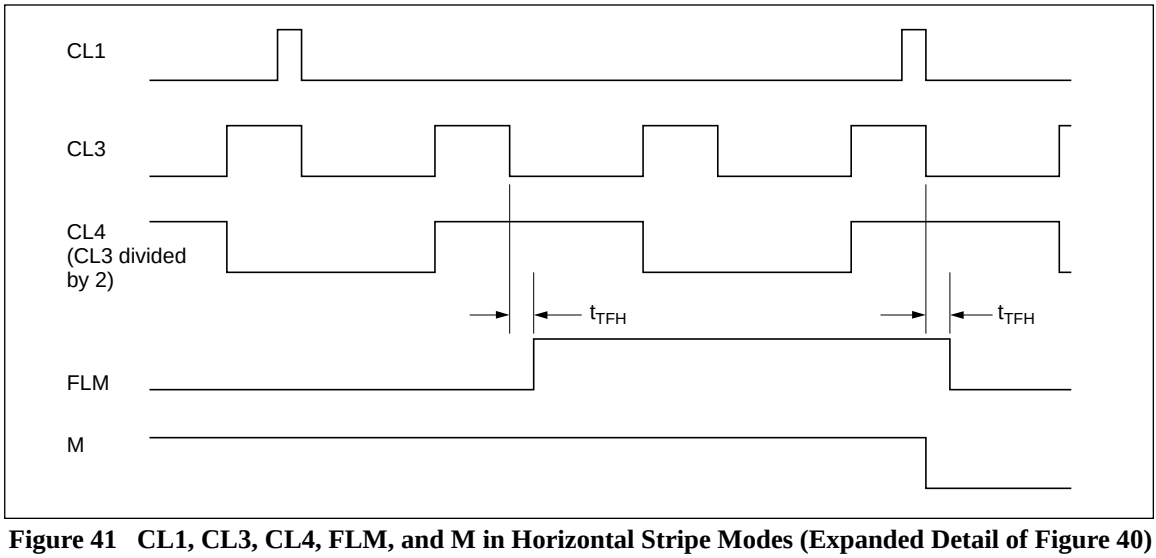


Figure 41 CL1, CL3, CL4, FLM, and M in Horizontal Stripe Modes (Expanded Detail of Figure 40)

Register Programming

MPU Interface

Item	Symbol	Min	Max	Unit	Remark
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns	Figure 42
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns	
$\overline{WR}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{WR}$ low-level pulse width	t_{WWRL}	190	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns	
D0–D3 setup time	t_{DSW}	100	—	ns	
D0–D3 hold time	t_{DHW}	0	—	ns	
D0–D3 output delay time	t_{DDR}	—	150	ns	
D0–D3 output hold time	t_{DHR}	10	—	ns	

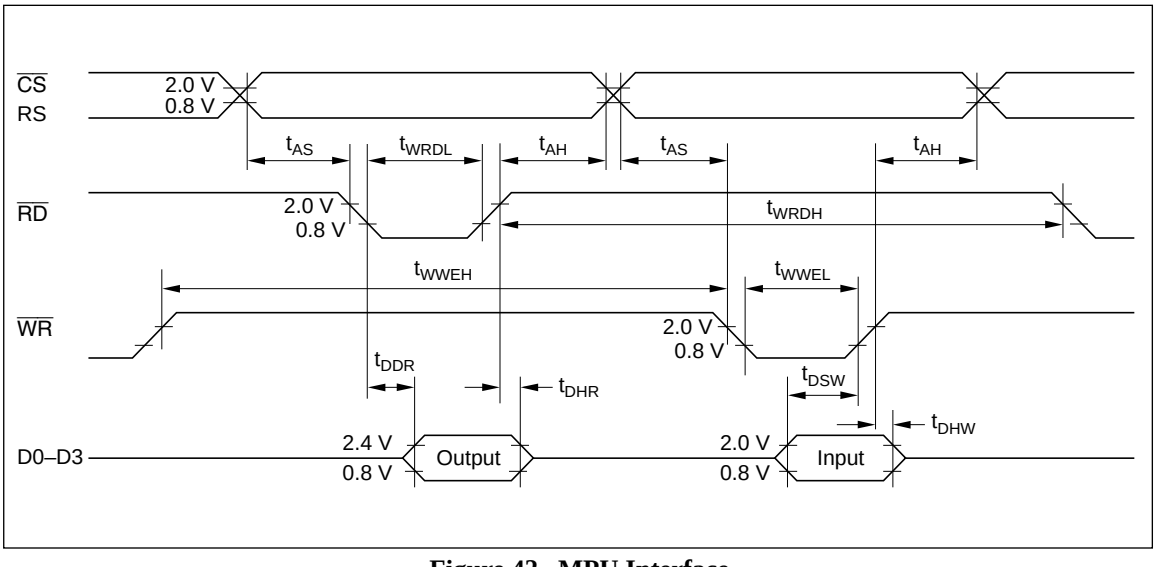


Figure 42 MPU Interface

ROM Interface

Item	Symbol	Min	Max	Unit	Remark
A signal cycle time	t_{CYCA}	528	—	ns	Figure 43
A signal rise time	t_{Ar}	—	100	ns	
A signal fall time	t_{Af}	—	100	ns	
D signal ROM data setup time	t_{DSWD}	120	—	ns	
D signal ROM data hold time	t_{DHWD}	0	—	ns	

Note: $t_{CYCA} = 16\ t_{CYCD}$ (t_{CYCD}: DOTCLK cycle time)

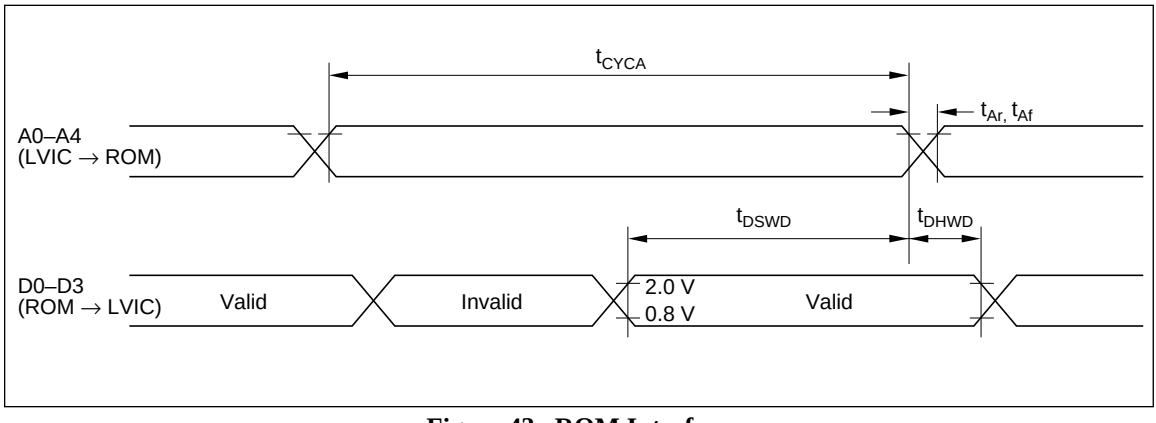


Figure 43 ROM Interface

PLL Interface

Item	Symbol	Min	Max	Unit	Remark
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns	Figure 44
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns	
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns	
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns	

Reset Input

Item	Symbol	Min	Max	Unit	Remark
$\overline{RES}$ input pulse width	$t_{\overline{RES}}$	1	—	µs	Figure 45

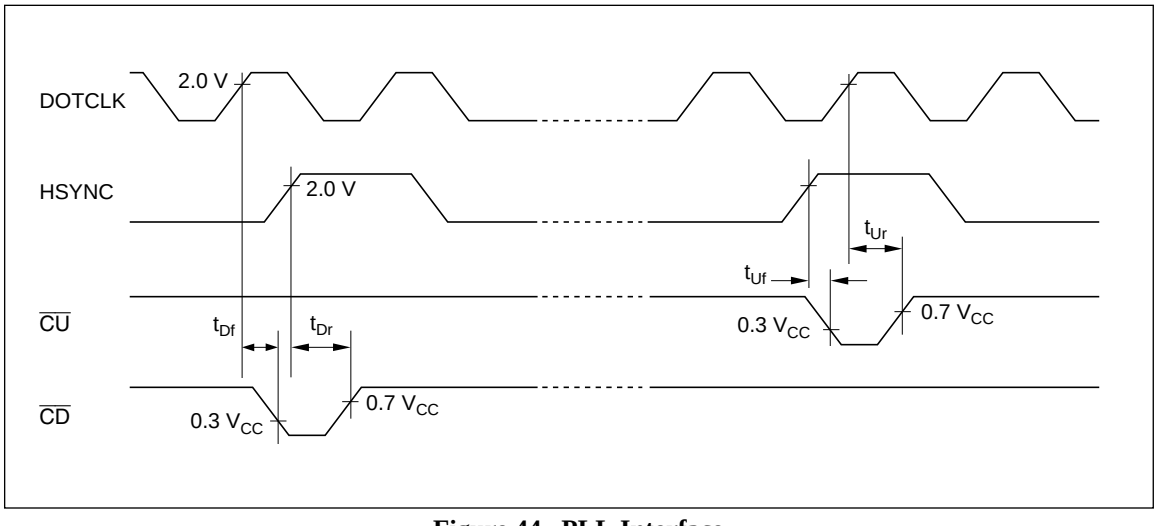


Figure 44 PLL Interface

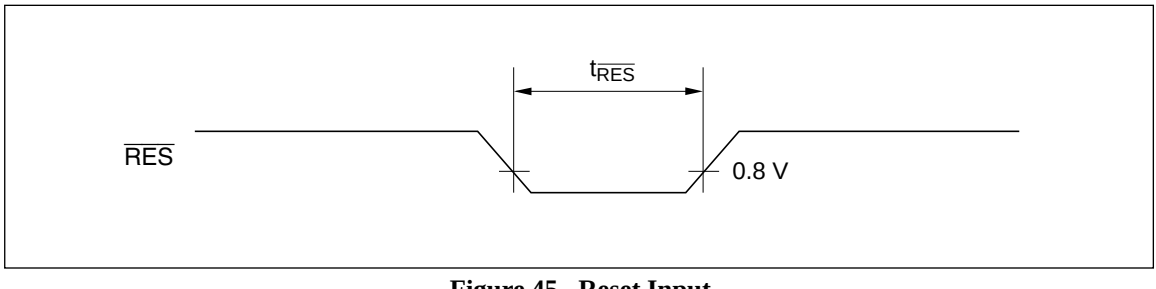


Figure 45 Reset Input

Load Circuits

TTL Load

Pin	R_L	R	C_L	Remarks
MA0–MA15, $\overline{MWE}$, $\overline{MCS0}$, $\overline{MCS1}$, RD0–RD7, GD0–GD7, BD0–BD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/RD/XDOT, A1/YL0–A3/YL2, A4/RS/ADJ	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pin	C	Remarks
CL1, CL2	40 pF	tr, tf: Specified
R0–R3, G0–G3, B0–B3 FLM $\overline{CU}$, $\overline{CD}$, M, CL3, CL4	40 pF	tr, tf: Not specified

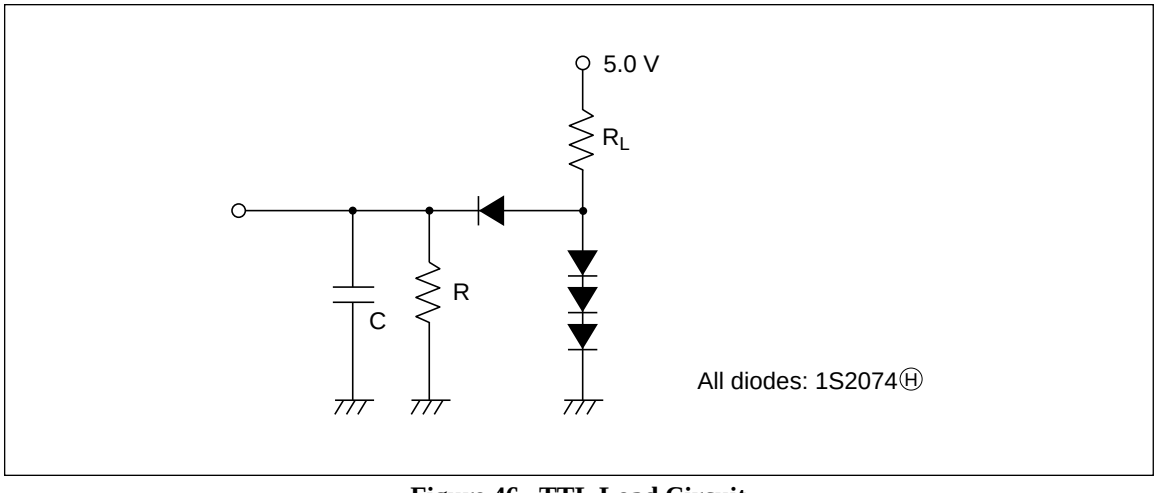


Figure 46 TTL Load Circuit

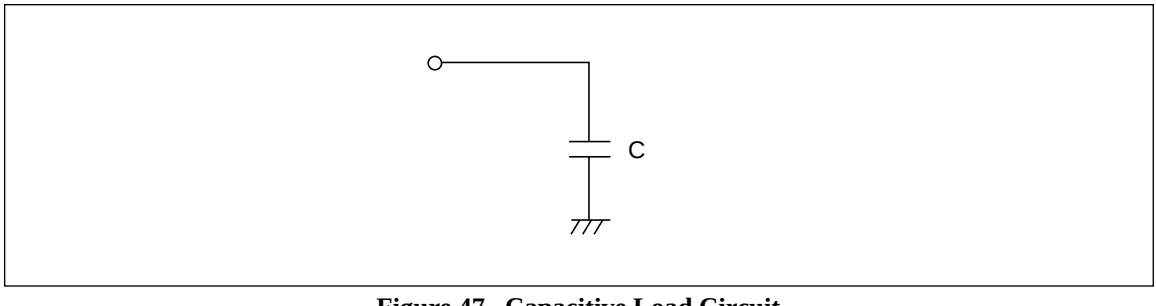


Figure 47 Capacitive Load Circuit

Refer to application note (No. ADE-502-011) for detail of HD66840 LVIC.

HD66850F

Color LCD Interface Engine (CLINE)

HITACHI

Description

The HD66850F CLINE interface controller converts multi-color video signals for CRT display into color or monochrome LCD data.

This device enables an LCD system to replace a CRT display system without any changes to the original display system. It automatically adapts to display modes of the IBM-VGA (Video Graphics Array™) system, facilitating the configuration of an LCD system.

The CLINE can control TN-type (Twisted Nematic) color and monochrome LCDs and can display a maximum of 4096 color levels or 16 gray levels.

Note: Video Graphics Array is a trademark of International Business Machines Corporation, U.S.A.

Features

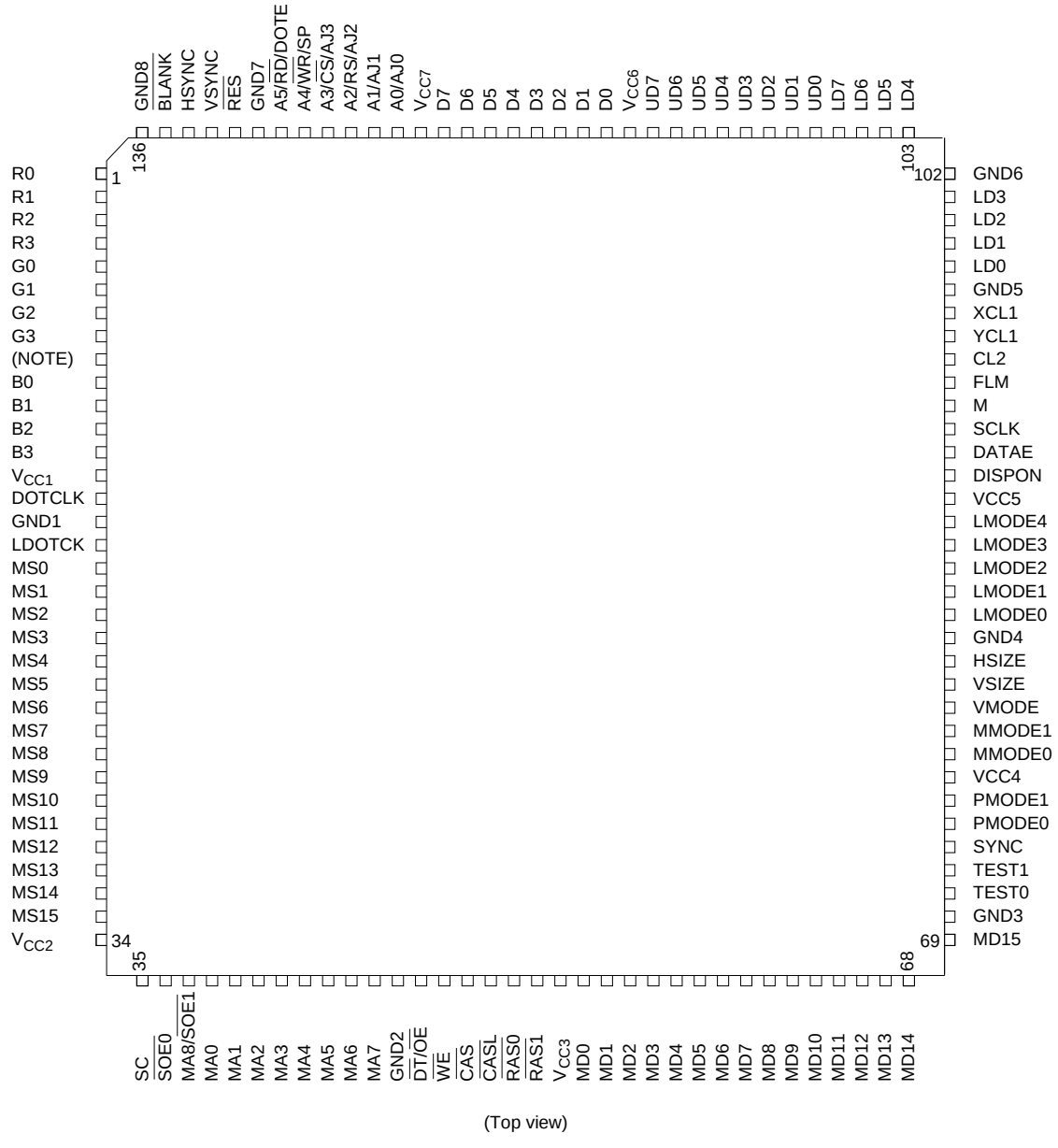
- Various LCD panel sizes supported
  - — 640 or 720 dots wide
  - — 32 to 512 lines high
- Programmable display size
  - — 32 to 720 dots wide
  - — 32 to 512 lines high
- Easy-to-see display
  - — Centering
  - — Stretching (display stretched to fill out the panel)
- Improved gradation display quality using the pulse width modulation method
- Desired gradation levels assignable to each display color through the use of internal gradation level palettes
- Changeable LCD frame frequency
  - — Through the use of a multi-port RAM frame buffer
  - — Within the range of 1/2 to 2 times of CRT display dot clock frequency
- High-speed operating frequency: 32 MHz (CRT display dot clock)
- Recommended LCD drivers: HD66110ST (column) and HD66115T (common)
- Single power supply: +5 V

Ordering Information

Type No.	Package
HD66850F	136-pin plastic QFP (FP-136)

Hitachi semiconductor

Pin Arrangement



(Top view)

Note: Pin No. 9 is not used; must be fixed low.

Pin Description

Type	Symbol	Pin No.	Pin Name	I/O	Function
Power supply	$V_{CC}1$ – $V_{CC}7$	14, 34, 53, 76, 88, 115, 124	V_{CC1} – V_{CC7}	—	All of these pins must beAll connected to a +5V supply
	GND1 – GND8	16, 46, 70, 82, 97, 102, 131, 136	GND1 – GND7	—	All of these pins must be grounded.
MPU/ROM or program interface	D0 – D7*1	(M) 116 – 123	Data 0 – 7	I/O	Transfer data between internal registers and MPU
	D0 – D7*1	(R) 116 – 123	Data 0 – 7	I	Input data to internal registers from external ROM
	DOTE	(P) 130	Dot clock edge change	I	Switches RGB data latch timing High: Data latched at the rising edge of DOTCLK pulses Low: Data latched at the falling edge of DOTCLK pulses
	$\overline{RD}$	(M) 130	Read	I	Inputs a read signal for reading data from internal registers
	A5	(R) 130	Address 5	O	Outputs external ROM address 5
	SP	(P) 129	Spread display select I	I	Selects either of the following display size modes High: Double – width display Low: Normal display
	$\overline{WR}$	(M) 129	Write	I	Inputs a write signal for writing data to internal registers
	A4	(R) 129	Address 4	O	Outputs external ROM address 4
	AJ3	(P) 128	Adjust 3	I	Adjusts the display timing signal (table 1)
	$\overline{CS}$	(M) 128	Chip select	I	Inputs a chip select signal to select the CLINE High: The CLINE not selected Low: The CLINE selected
	A3	(R) 128	Address 3	O	Outputs external ROM address 3
	AJ2	(P) 127	Adjust 2	I	Adjusts the display timing signal (table 1)
	RS	(M) 127	Register select	I	Inputs a register select signal to select either CLINE data registers or index register High: Data registers Low: The index register
	A2	(R) 127	Address 2	O	Outputs external ROM address 2
	AJ0, AJ1*2	(P) 125, 126	Adjust 0, 1	I	Adjust the display timing signal (table 1)
	A0, A1*2	(R) 125, 126	Address 0, 1	O	Output external ROM addresses 0 and 1, respectively

(M): For MPU programming method (R): For ROM programming method (P): For pin programming method
I/O: Input/Output

Type	Symbol	Pin No.	Pin Name	I/O	Function
CRT interface	R0 – R3*3	1 – 4	Red serial data 0 – 3	I	Input CRT display R data
	G0 – G3*3	5 – 8	Green serial data 0 – 3	I	Input CRT display G data or monochrome data
	B0 – B3*3	10 – 13	Blue serial data 0 – 3	I	Input CRT display B data: For monochrome display, B1 selects 16-gray-scale display and B0 indicates the type of CRT display data input. B1 = high: Prohibited B1 = low: 16-level gray scale display B0 = high: 64-color data input B0 = low: 16-level gray scale data input
	DOTCLK	15	Dot clock	I	Inputs the dot clock pulses for CRT display
	HSYNC	134	Horizontal synchronization	I	Inputs the CRT horizontal synchronization signal
	VSYNC	133	Vertical synchronization	I	Inputs the CRT vertical synchronization signal
	$\overline{\text{BLANK}}$	135	Blanking	I	Inputs a display timing siganl indicating horizontal or vertical display period, or a blank signal indicating the display period with border area period
LCD interface	UD4 – UD7*4	111 – 114	LCD upper panel data 4 – 7	O	Output LCD upper panel data or R data
	UD0 – UD3*4	107 – 110	LCD upper panel data 0 – 3	O	Output LCD upper panel data or G data
	LD4 – LD7*4	103 – 106	LCD lower panel data 4 – 7	O	Output LCD lower panel data or B data
	LD0 – LD3*4	98 – 101	LCD lower panel data 0 – 3	O	Output LCD lower panel data or I data
	XCL1*4	96	X-driver latch clock	O	Outputs the LCD data latch clock pulses for X-drivers
	YCL1	95	Y-driver shift clock	O	Outputs the LCD data line shift clock pulses for Y-drivers
	CL2	94	X-driver shift clock	O	Outputs the LCD data line shift clock pulses for X-drivers
	FLM	93	First line maker	O	Outputs the first line maker for Y-drivers

I/O: Input/Output

Type	Symbol	Pin No.	Pin Name	I/O	Function
LCD interface	M	92	M	O	Outputs a signal for converting LCD drive signals to AC
	SCLK	91	Shift clock	O	Outputs clock pulse with a frequency identical to CL2 but without a retrace period
	DATAE*4	90	Data enable	O	Indicates LCD data display period
	DISPON*4	89	Display on	O	Controls LCD on/off
	LDOTCK	17	LCD dot clock	I	Inputs LCD dot clock pulses
Buffer memory interface	MD0 – MD15*5	54 – 69	Memory data 0 – 15	O	Output data to be written to buffer memory
	MS0 – MS15*6	18 – 33	Memory serial data 0 – 15	I	Input data read from buffer memory
	MA0 – MA7*5	38 – 45	Memory address 0 – 7	O	Output buffer memory addresses 0 – 7
	MA8/ $\overline{\text{SOE1}}$*5	37	Memory address 8/ serial output enable 1	O	Outputs buffer memory address 8 when 1-Mbit RAMs are used or outputs a serial data output enable signal when 256-kbit RAMs are used
	$\overline{\text{SOE0}}$*5	36	Serial output enable 0	O	Output a serial data output enable signal for buffer memory
	$\overline{\text{WE}}$*5	48	Write enable	O	Outputs a write enable signal for buffer memory
	$\overline{\text{DT}}$/$\overline{\text{OE}}$*5	47	Data transfer/output enable	O	Outputs a data transfer signal or an output enable signal for buffer memory
	$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$*5	51, 52	Row address strobe 0, row address strobe 1	O	Outputs a row address strobe signal for buffer memory
	$\overline{\text{CAS}}$, $\overline{\text{CASL}}$*5	49, 50	Column address strobe	O	Outputs a column address strobe signal for buffer memory
	SC*5	35	Serial clock	O	Outputs serial read clock pulses for buffer memory
Mode control	PMODE0, PMODE1	74, 75	Program mode 0, Program mode 1	I	Select a CLINE programming method (table 2)
	LMODE0 – LMODE4	83 – 87	LCD mode 0 – 4	I	Select a display mode (table 9)
	MMODE0, MMODE1	77, 78	Memory mode 0, 1	I	Select a memory configuration (table 3)
	SYNC	73	Synchronization	I	Select a basic clock for LCD High: DOTCLK Low: LDOTCK

I/O: Input/Output

Type	Symbol	Pin No.	Pin Name	I/O	Function
Mode control (cont)	VMODE	79	VGA mode	I	Specifies a CRT display system High: Non-VGA system Low: VGA system
	VSIZE	80	LCD vertical size	I	Specifies the vertical size of the LCD panel High: 480 lines Low: 400 lines
	HSIZE	81	LCD horizontal size	I	Specifies the horizontal size of the LCD panel High: 720 dots Low: 640 dots
	$\overline{RES}$	132	Reset	I	Inputs an external reset signal
	TEST0, TEST1	71, 72	Test 0, 1	I	Used for tests; Must be grounded

I/O: Input/Output

Notes: 1. Must be fixed low for pin programming method.
2. Must be fixed low for MPU programming method.
3. Must be fixed low when not used.
4. Must be left disconnected when not used.
5. Must be left disconnected when buffer memory is not used.
6. Must be fixed low when buffer memory is not used.

Table 1 Display Timing Signal Fine Adjustment

Pin				Number of Dots Adjusted
AJ3	AJ2	AJ1	AJ0	
0	0	0	0	0
0	0	0	1	–1
0	0	1	0	–2
1	0	0	0	0
1	0	0	1	+1
1	0	1	0	+2
1	0	1	1	+3
1	1	0	0	+4
1	1	0	1	+5
1	1	1	0	+6

Note: – (minus) indicates advancing the phase of the display timing signal,
+ (plus) indicates delaying the phase of the display timing signal.

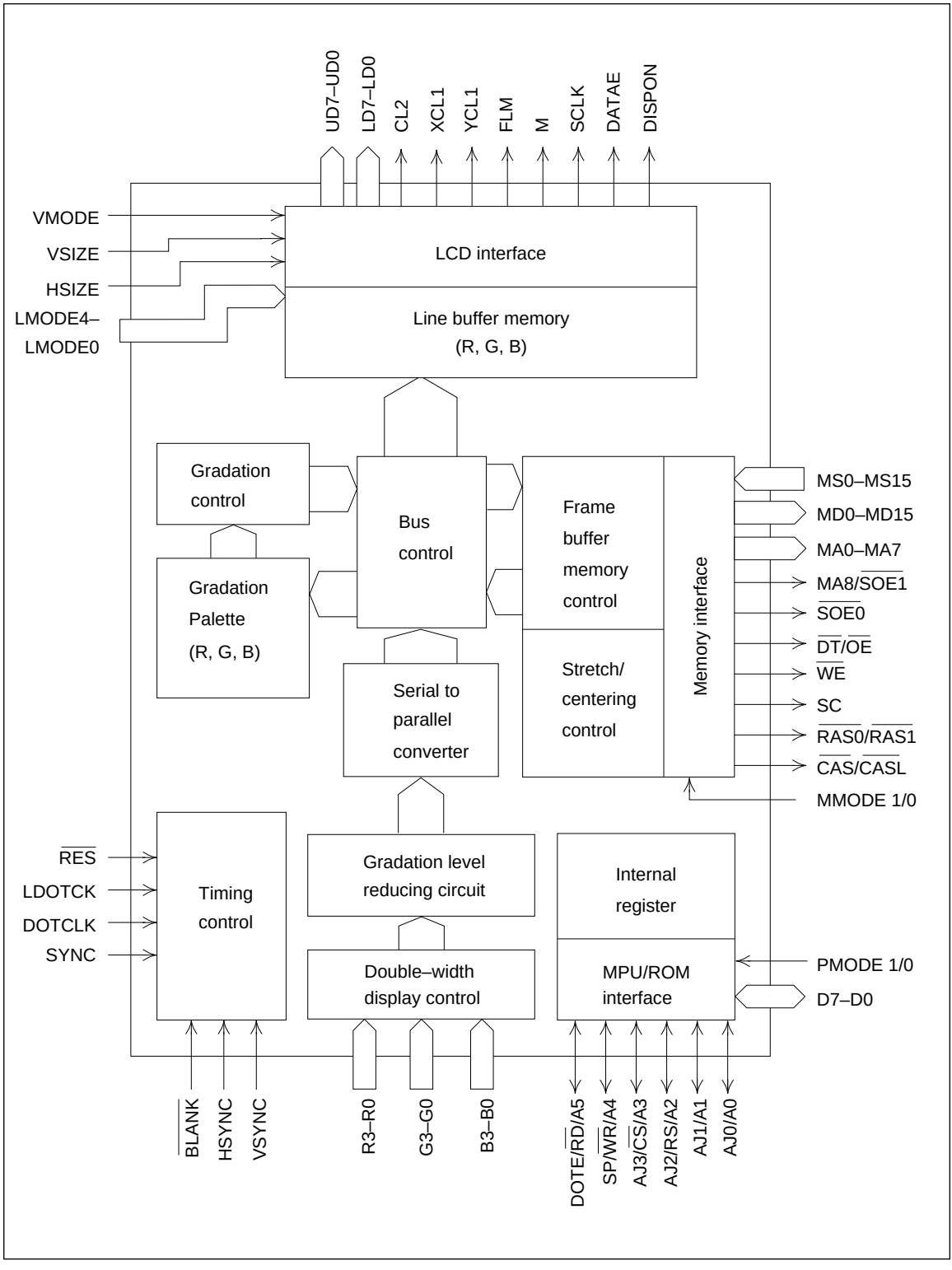
Table 2 Programming Method Selection

Pin		
PMODE1	**PMODE0**	**Programming Method**
0	0	Pin
0	1	Internal registers (MPU)
1	0	Internal registers (ROM)
1	1	Prohibited

Table 3 Memory Configuration Selection

Pin		
MMODE1	**MMODE0**	**Memory Configuration**
0	0	1-Mbit RAM
0	1	256-kbit RAM
1	0	No memory
1	1	No memory (when the CRT controller supports dual screen display)

Block Diagram



CLINE registers are summarized in table 4.

Table 4 Register List

		Index Reg				Reg.		Program	Read/	Data Bits							
$\overline{CS}$	RS	3	2	1	0	No.	Register Name	Units	Write	7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
0	0	0	0	0	0	IR	Index	—	W	—	—	—	—	IA3	IA2	IA1	IA0
0	1	0	0	0	0	R0	Control	—	R/W	—	—	—	STE	CRE	CCE	SP	DISP ON
0	1	0	0	0	1	R1	Input timing control	Dot	R/W	—	—	—	DOTE	AJ3	AJ2	AJ1	AJ0
0	1	0	0	1	0	R2	Horizontal display size	Character	R/W	—	DH6	DH5	DH4	DH3	DH2	DH1	DH0
0	1	0	0	1	1	R3	Vertical display size (high-order)	Line	R/W	—	—	—	—	—	—	—	DV8
0	1	0	1	0	0	R4	Vertical display size (low-order)	Line	R/W	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0
0	1	0	1	0	1	R5	Centering raster	Line (Raster)	R/W	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
0	1	0	1	1	0	R6	Centering character	Character	R/W	—	—	—	CC4	CC3	CC2	CC1	CC0
0	1	0	1	1	1	R7	Border color control	—	R/W	—	—	—	BM	BCI	BCR	BCG	BCB
0	1	1	0	0	0	R8	Stretching control	Line	R/W	—	—	—	—	SF3	SF2	SF1	SF0
0	1	1	0	0	1	R9	Stretching index (high-order)	Line	R/W	SI15	SI14	SI13	SI12	SI11	SI10	SI9	SI8
0	1	1	0	1	0	R10	Stretching index (low-order)	Line	R/W	SI7	SI6	SI5	SI4	SI3	SI2	SI1	SI0
0	1	1	0	1	1	R11	Gradation level palette address	—	W	—	—	PS1	PS0	PA3	PA2	PA1	PA0
0	1	1	1	0	0	R12	Gradation level palette data	—	R/W	—	—	PD5	PD4	PD3	PD2	PD1	PD0
0	1	1	1	0	1	R13	Gradation display clock period (high-order)	Dot	R/W	—	—	—	—	—	—	—	GC8
0	1	1	1	1	0	R14	Gradation display clock period (low-order)	Dot	R/W	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
0	1	1	1	1	1	R15	Reserved	—	—	—	—	—	—	—	—	—	—

Notes: 1. Bits marked with * cannot either read from or written to.
2. Bits marked with – are invalid and must be initialized to 0s; they cannot be read.

System Description

Figure 1 shows an example of a VGA-compatible display system implemented with the CLINE. In this system, a color palette HD153119 (Hitachi), which is capable of digital output, is used with a VGA-compatible CRT controller. The CLINE receives digital color data and display sychronization signals from the color pallette and the CRT controller, respectively, and displays 4096-color images on a color LCD, or 16-level grayscale images on a monochrome LCD. With minor modification of the existing CRT display system, simultaneous LCD and CRT display is possible.

Addition of an external frame buffer memory (dual-port RAM) allows the LCD frame frequency to be increased above that of a CRT. This enables easy-to-see gradation display and the control of LCDs having a dual screen configuration.

CLINE operation may be controlled by internal registers through the 80-family MPU bus or an external ROM (as shown in the figure), or simply by pins.

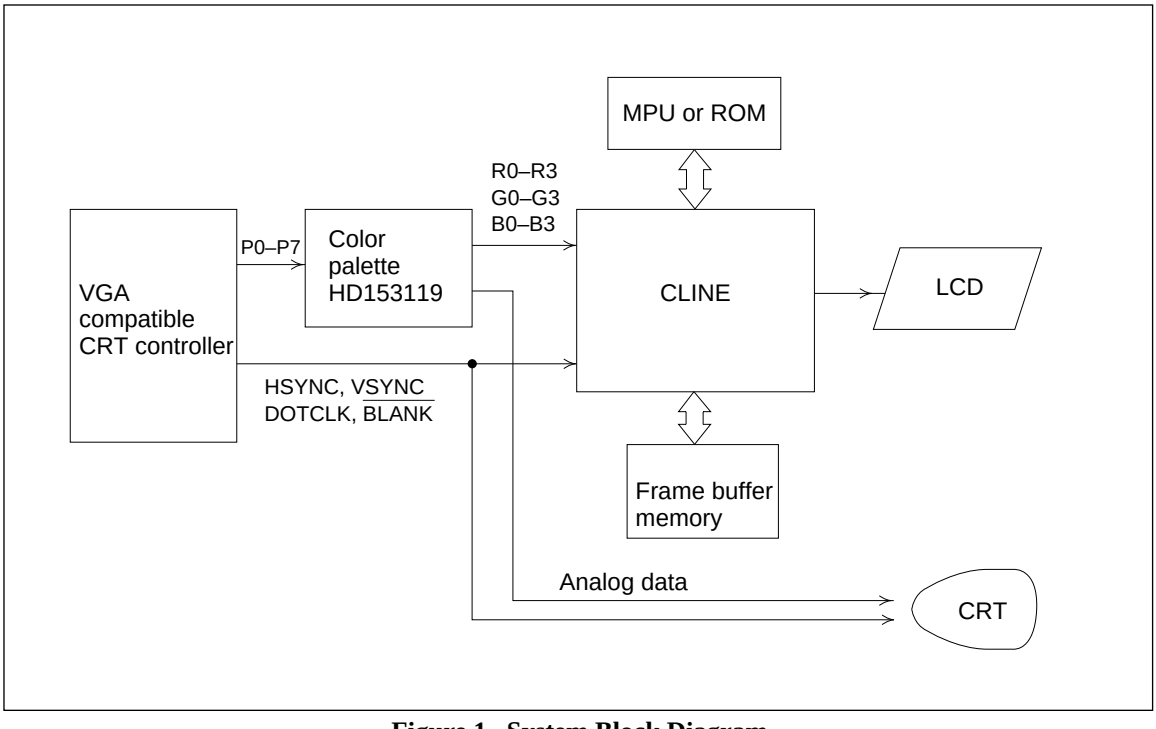


Figure 1 System Block Diagram

Functional Description

Programming Methods

To control CLINE functions, set the appropriate pins and/or internal registers according to the functions used. Controlling methods include pin and internal register programming methods. Internal register programming includes the MPU and ROM programming methods. Any of the three methods can be selected by the combined setting of pins PMODE0 and PMODE1 (table 2).

The pin programming method uses pins to control CLINE functions, and the internal register programming method uses data written to the internal registers to control the functions.

Figure 2 (a) shows a connection example of the CLINE and MPU buses for the MPU programming method. The CLINE bus, which is compatible with the 80-family microprocessor bus, can be directly connected to the host MPU bus.

Figure 2 (b) shows a connection example of the CLINE and ROM for the ROM programming method. In this case, data is automatically loaded into internal registers from the external ROM attached for this purpose. Note that with the ROM programming method, the reset signal must be applied before rewriting the internal registers or gradation level palettes.

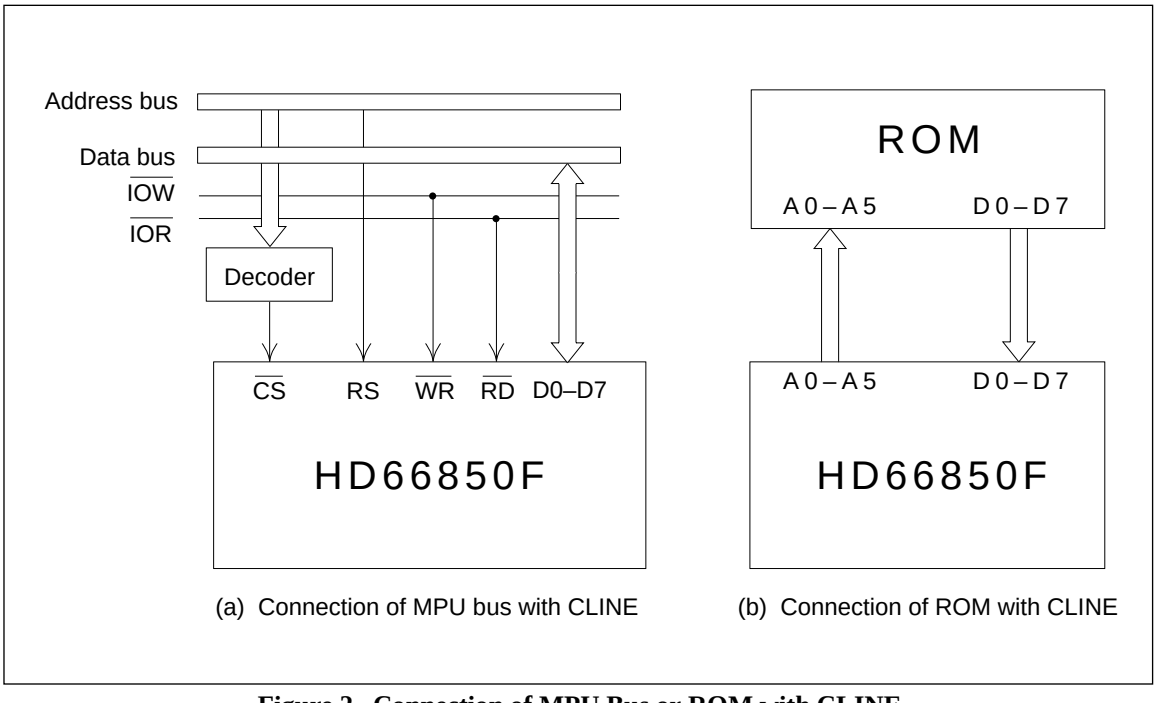


Figure 2 Connection of MPU Bus or ROM with CLINE

Automatic Adaptation to VGA Display Modes

VGA CRT display system display size varies depending on the display mode. (VGA display sizes are: 320, 360, 640, or 720 dots wide and 350, 400, or 480 lines high.) The CLINE identifies the current display mode from VSYNC and HSYNC signal polarities and the display period length, and changes the display size automatically (tables 5 and 6). This function is enabled by setting the VMODE pin low. The CLINE, based on this function, automatically sets the necessary registers (R0, R2, R3, R4, R5, R6, R8, R9, and/or R10) corresponding to the parameters of the display size, double-width display, gradation display clock, and stretching/centering display functions. (In MPU or ROM programming method, selection of vertical centering (bit 3 of R0) or stretching (bit 4 of R0) is not automatic.) Consequently, in VGA display modes, rewriting these registers is disabled.

Note that display stretching and centering are unavailable when buffer memory is not used in the system, even in VGA display modes. In these cases, a display of different vertical size would be placed in the upper section of the LCD panel, resulting in a blank area in the lower section. Centering the display in a system without memory requires external circuits or BIOS tuning.

When displaying an image 720 dots wide (9 dots × 80 characters) on an LCD panel 640 dots wide, the CLINE removes the ninth horizontal dot of each character to prevent losing the far-right portion of the image.

Table 5 Automatic Vertical Display Size Settings for VGA Display Modes

VSYNC	HSYNC	Display Size	Border Rasters	Displayed Rasters
Negative	Positive	350 lines	1-6	7-356
Positive	Negative	400 lines	1-7	8-407
Negative	Negative	480 lines	1-8	9-488

Table 6 Automatic Horizontal Display Size Settings for VGA Display Modes

BLANK Signal High Level

Pulse Width	Display Size	Border Dots	Displayed Dots
256-335 dots	320 dots (256-color)	1-5	6-325
336-359 dots	320 dots (16-color)	1-8	9-328
360-511 dots	360 dots	1-9	10-369
640-703 dots	640 dots	1-8	9-648
704-767 dots	720 dots	1-9	10-729

LCD Panel Size

LCD panel size is specified by either pins or internal registers.

For VGA modes, vertical panel size of 400 or 480 lines can be selected by the VSIZE pin and horizontal panel size of 640 or 720 lines by the HSIZE pin.

For non-VGA modes, the panel size is also specified by the VSIZE and HSIZE pins in pin programming method. In internal register programming method, vertical display size is specified by the vertical display size register (R3 and R4), within the range of 2 to 512 lines. Here, note that the vertical display size specified by R3 and R4 is the CRT display vertical size. When this size differs from the LCD panel vertical size, centering or stretching function must be used. Refer to the following equations for calculating the number of centering rasters and the stretching ratio. For the definition of the centering rasters, see figure 23, Centering Rasters,

- For centering

  LCD panel vertical size (line) =
  CRT display vertical size (line) + centering rasters (lines) $\times$ 2

- For stretching

  LCD panel vertical size (line) =
  CRT display vertical size (line) $\times$ stretching ratio

Since LCD panel horizontal size is limited to 640 or 720 dots even in internal register programming method, centering function must be used as well so that the total number of horizontal dots including the CRT display area and border areas become 640 or 720. Refer to the following equation to calculate the number of centering characters. For the definition of the border areas and centering characters, see figure 25, Centering Characters.

LCD panel horizontal size (dot) =
{number of horizontal display characters +
(number of centering characters $\times$ 2)} $\times$ 8

Double-Width Display

Some CRT display systems have a low-resolution display mode of 320 horizontal dots in addition to a high-resolution display mode of 640 horizontal dots. In this case, the CRT display system lowers the dot clock frequency to reduce one line of data to 320 dots. If such data is supplied to the LCD system of 640 horizontal dots as-is, the entire display will be placed on the left section of the panel with the right half blank. To accommodate this situation, the CLINE doubles the width of the low-resolution display. This function is enabled by the SP/WR/A4 pin in pin programming method or the SP bit (bit 1) of the control register (R0) in internal register programming method (table 7). In either method, for VGA display systems, the CLINE detects low-resolution display mode and automatically enables double-width display.

Table 7 Double-Width Display Usage

Programming Method	CRT System Mode	Setting
Pin: SP	VGA	Automatic
	Non-VGA	0: Normal display
		1: Double-width display
Internal register: Control register bit 1 (SP bit)	VGA	Automatic
	Non-VGA	0: Normal display
		1: Double-width display

Stretching and Centering Display

When the display size differs from the LCD panel size, data will be displayed on the upper-left section of the LCD panel with blank space to the right and/or below if no countermeasures are taken. To provide a user-friendly display, the CLINE can stretch a display to fill out the panel or center a display. Both stretching and centering functions are enabled by control register (R0) bits 2, 3, and 4.

Note that stretching and centering functions are available only in a system where buffer memory is used. This is because these functions are realized through adjustment of memory access. Similarly, stretching and centering functions are unavailable in non-VGA modes when the CLINE is controlled by the pin programming method. Simultaneous use of the vertical centering and stretching functions is also impossible.

In the internal register programming method, horizontal centering function is controlled by the centering character register (R6) within the range of 1 to 32 characters (8 to 256 dots), while vertical centering function is controlled by the centering raster register (R5) within the range of 1 to 256 lines.

Stretching function is controlled by the stretching control register (R8) and the stretching index register (R9 and R10) so as to double the vertical display size at most.

Figure 3 shows display examples using stretching/centering functions. In these examples, a display of 640 dots × 350 lines is displayed on an LCD panel of 720 dots × 400 lines, using stretching/centering functions.

For VGA modes, in both internal register programming and pin programming methods, necessary parameters are automatically calculated from the relationship between display size and the LCD panel size and set in the appropriate registers. Consequently, there is no need to account for display size.

However, the vertical centering or stretching function can be selected in the internal register programming method. (In pin programming method, the stretching function is automatically selected.) Table 8 describes the use of the stretching and centering function.

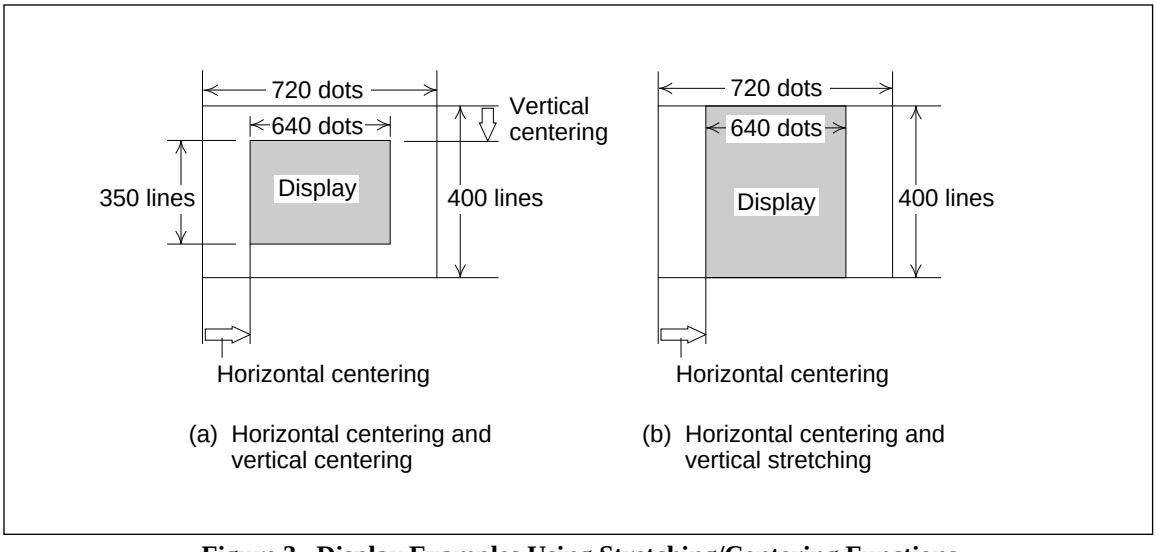


Figure 3 Display Examples Using Stretching/Centering Functions

Table 8 Stretching and Centering Function Usage

Direction	Programming Method	CRT System Mode	Display Arranging Function	Setting
Vertical	Pin	VGA	Stretching	Automatic
		Non-VGA	None	— *1
	Internal register	VGA	Stretching or centering	Automatic *2
		Non-VGA	Stretching or centering	Necessary
Horizontal	Pin	VGA	Centering	Automatic
		Non-VGA	None	— *1
	Internal register	VGA	Centering	Automatic
		Non-VGA	Centering	Necessary

Notes: 1. Display size must be LCD panel size.
2. Either stretching or centering function must be selected by the internal register.

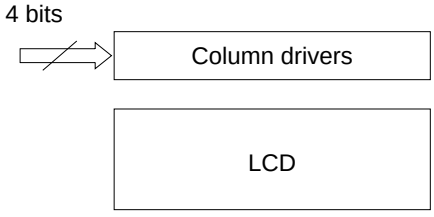
Display Modes

Display Mode Settings and LCD Module Configurations: The CLINE supports 20 display modes, depending on the settings of the LMODE4 to LMODE0 pins. The display mode includes display color mode (color or monochrome), screen configuration (single or dual), gradation display method, and width of data transfer to LCD drivers. Table 9 lists the display modes and figures 4 (a) to 4 (g) show the corresponding LCD module configurations.

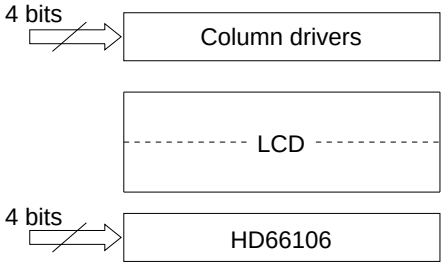
Table 9 Display Modes and LCD Module Configurations

Mode No.	Pin: LMODE 4	3	2	1	0	Display Color Mode (Gradation Display Method)	Screen Config.	Data Width	LCD Module Config.
1	0	0	0	0	0	Monochrome: black and white	Single	4	Fig. 4 (a)
2	0	0	0	0	1		Dual	4	Fig. 4 (b)
3	0	0	0	1	0		Single	8	Fig. 4 (c)
4	0	0	0	1	1		Dual	8	Fig. 4 (d)
5	0	0	1	0	0	Monochrome: 16 gray levels (Frame-based data thinning)	Single	4	Fig. 4 (a)
6	0	0	1	0	1		Dual	4	Fig. 4 (b)
7	0	0	1	1	0		Single	8	Fig. 4 (c)
8	0	0	1	1	1		Dual	8	Fig. 4 (d)
9	0	1	0	0	0	Monochrome: 16 gray levels (1/2 pulse width modulation)	Single	4	Fig. 4 (a)
10	0	1	0	0	1		Dual	4	Fig. 4 (b)
11	0	1	0	1	0		Single	8	Fig. 4 (c)
12	0	1	0	1	1		Dual	8	Fig. 4 (d)
13	1	0	0	0	0	16 colors	Single	2	Fig. 4 (e)
14	1	0	0	1	0		Single	4	Fig. 4 (f)
15	1	0	0	1	1	8 colors	Single	8	Fig. 4 (g)
16	1	0	1	0	0	4096 color (Frame-based data thinning)	Single	2	Fig. 4 (e)
17	1	0	1	1	0		Single	4	Fig. 4 (f)
18	1	0	1	1	1		Single	8	Fig. 4 (g)
19	1	1	0	1	0	4096 color (1/2 pulse width modulation)	Single	4	Fig. 4 (f)
20	1	1	0	1	1		Single	8	Fig. 4 (g)

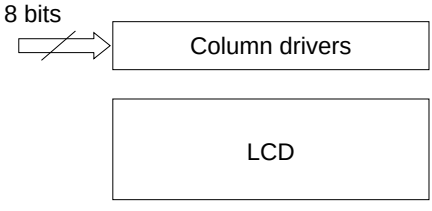
Note: Modes 15, 18, and 20 are interleaving structure modes.



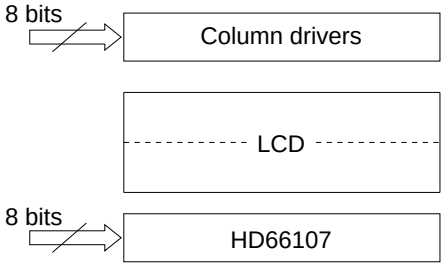
(a) Single screen, 4-bit data width



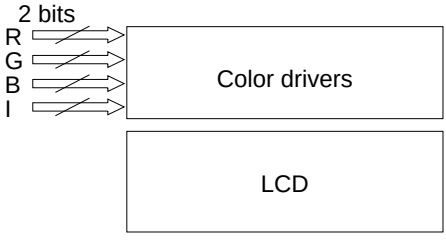
(b) Dual screen, 4-bit data width



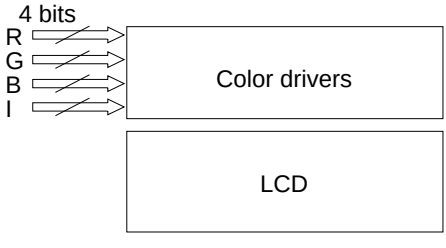
(c) Single screen, 8-bit data width



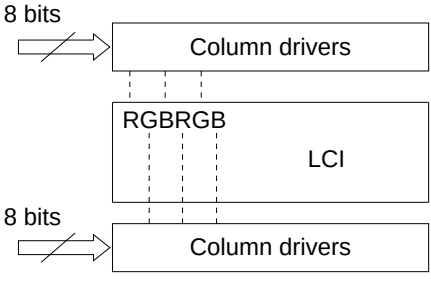
(d) Dual screen, 8-bit data width



(e) Single screen, 2-bit data width, color drivers



(f) Single screen, 4-bit data width, color drivers



(g) Single screen, 8-bit data width, interleaving structure

Figure 4 LCD Module Configurations by Display Modes

Gradation Level Reduction: Although a CRT display system can represent information for over 100,000 color levels, an LCD cannot handle so much information.

Consequently, CRT color or gradation level information must be reduced in order for the CLINE to display it. Reduction methods vary depending on the input color or gradation level information, the LCD panel (color or monochrome), and other factors. Table 10 lists gradation level reduction for CLINE modes, where "Input Bits" indicates CRT display color data and "Reduced Data" indicates input to the gradation level palettes.

Input Display Data Connection: Input display data connection and pin settings depend on the CRT input mode (color or gradation level information) and the LCD panel used.

- When monochrome LCD panel is used (LMODE4 = 0)

  — 64-color input and 16-level grayscale output (modes 5-12)

  The B0 pin must be set to 1, and the B1 pin to 0. Unused display data input pins must be fixed to 0. See figure 5 (a).

  — 16-level grayscale input and 16-level grayscale output (modes 5-12)

  Both B0 and B1 pins must be set to 0. Unused display data input pins must be fixed to 0. See figure 5 (b).

- When color LCD panel is used (LMODE4 = 1)

  — 64-color input and 16- or 8-color output (modes13-15)

  Two-bit R, G, and B data must be input to the R2-R3, G2-G3, and B2-B3 pins, respectively. Unused display data input pins must be fixed to 0). See figure 6 (a).

  — 4096-color input and 4096-color output (modes 16-20)

  Four-bit R, G, and B data must be input to the R0-R3, G0-G3, and B0-B3 pins, respectively. If the input has more than 4096 colors, use the high-order four bits of each color. See figure 6 (b).

Table 10 Gradation Level Reduction for CLINE Display Modes

Input Mode	Input Bits R	G	B	CLINE Display Mode	Reduced Data 3	2	1	0	LCD Panel	Gradation Level Reduction (Bits)
4096 colors	4	4	4	4096 color levels	D3	D2	D1	D0	Color	12 → 12
64 colors	2	2	2	16 colors	R	G	B	I	Color	6 → 4
64 colors	2	2	2	16 gray levels	D3	D2	D1	D0	Monochrome	6 → 4
16 gray levels	—	4	—	16 gray levels	D3	D2	D1	D0	Monochrome	4 → 4
16 gray levels	—	4	—	Monochrome (black & white)	All 0s or all 1s				Monochrome	4 → 1

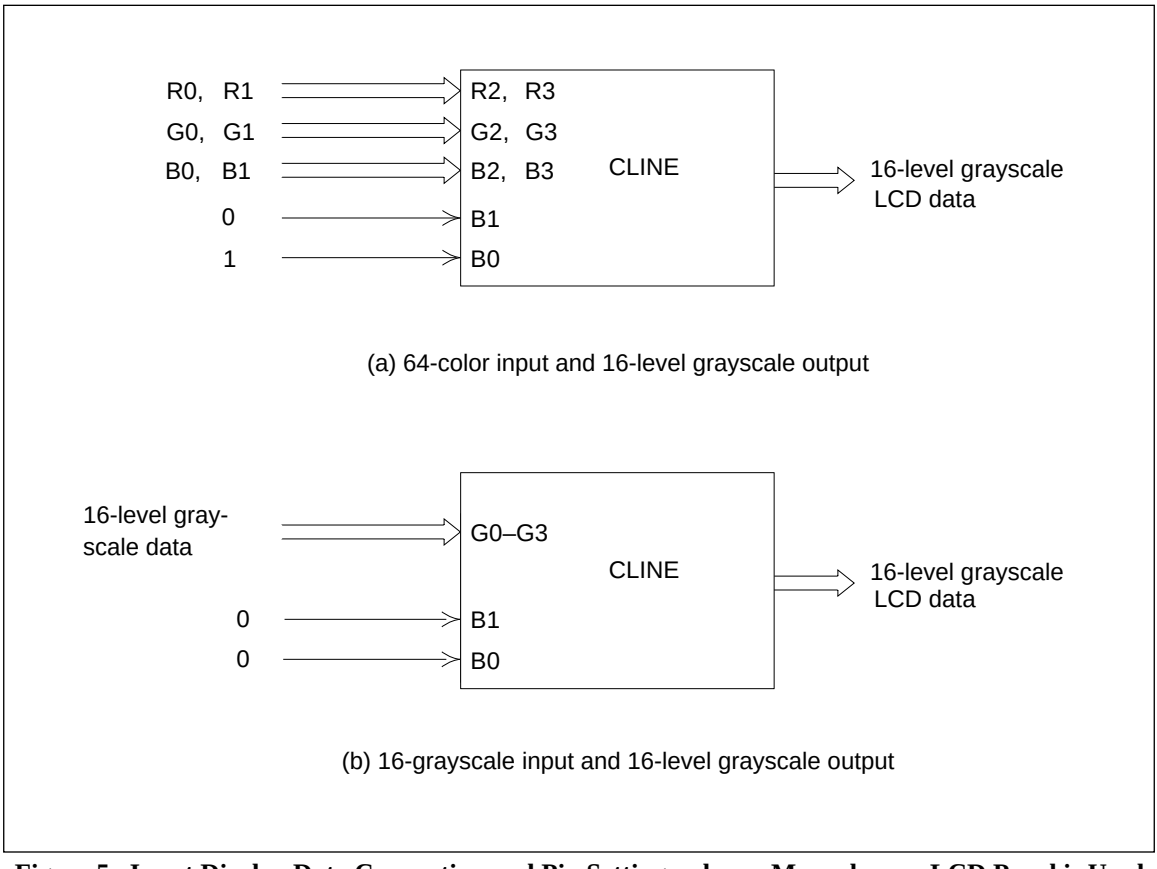
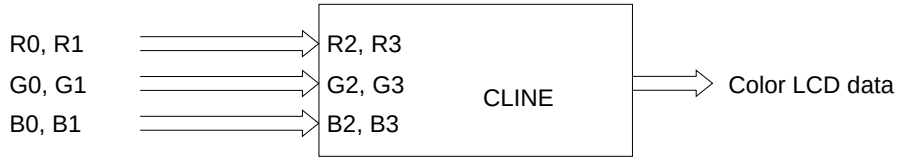
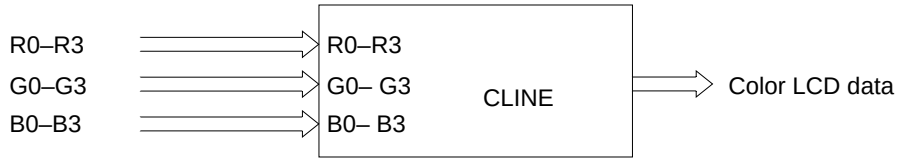


Figure 5 Input Display Data Connection and Pin Settings when a Monochrome LCD Panel is Used



(a) 64-color input and 16- or 8-color output



(b) 4096-color input and 4096-color output

Figure 6 Input Display Data Connection and Pin Settings when a Color LCD Panel is Used

LCD Data Output: The CLINE uses pins UD7–UD0 and LD7–LD0 for display data output. Output data from these pins depend on the display mode, as shown in table 11. However, data output timings are basically the same in all display modes. Display data output timing for modes 15 and 18 (8-bit color data transfer, bidirectional connection, without pulse width modulation) is shown in figure 7. Display data output timing for the LCD display modes with pulse width modulation is slightly different. This type of example is shown in figure 8. Figure 8 shows the display data output timing in mode 10 (1/2 pulse width modulation, 4-bit monochrome data transfer, and dual screen configuration).

However, LCD lower panel data LD3–LD0 are not shown in the figure.

Table 11 LCD Data Output Pins and Display Data by Display Modes

	Monochrome Modes				Color Modes				
Pin	4-Bit/ Single Screen	4-Bit/ Dual Screen	8-Bit/ Single Screen	8-Bit/ Dual Screen	2-Bit	4-Bit	8-Bit		
UD7	—	—	D7	UD7	—	R3	R15	G10	B5
UD6	—	—	D6	UD6	—	R2	B15	R9	G4
UD5	—	—	D5	UD5	R1	R1	G14	B9	R3
UD4	—	—	D4	UD4	R0	R0	R13	G8	B3
UD3	D3	UD3	D3	UD3	—	G3	B13	R7	G2
UD2	D2	UD2	D2	UD2	—	G2	G12	B7	R1
UD1	D1	UD1	D1	UD1	G1	G1	R11	G6	B1
UD0	D0	UD0	D0	UD0	G0	G0	B11	R5	G0
LD7	—	—	—	LD7	—	B3	G15	B10	R4
LD6	—	—	—	LD6	—	B2	R14	G9	B4
LD5	—	—	—	LD5	B1	B1	B14	R8	G3
LD4	—	—	—	LD4	B0	B0	G13	B8	R2
LD3	—	LD3	—	LD3	—	(I3)	R12	G7	B2
LD2	—	LD2	—	LD2	—	(I2)	B12	R6	G1
LD1	—	LD1	—	LD1	(I1)	(I1)	G11	B6	R0
LD0	—	LD0	—	LD0	(I0)	(I0)	R10	G5	B0

Notes: 1. The left bit corresponds to MSB.
2. U and L indicate upper panel and lower panel data, respectively.
3. Data in parentheses are for 16-color display.
4. — indicates that the corresponding pins are not used; must be left disconnected.

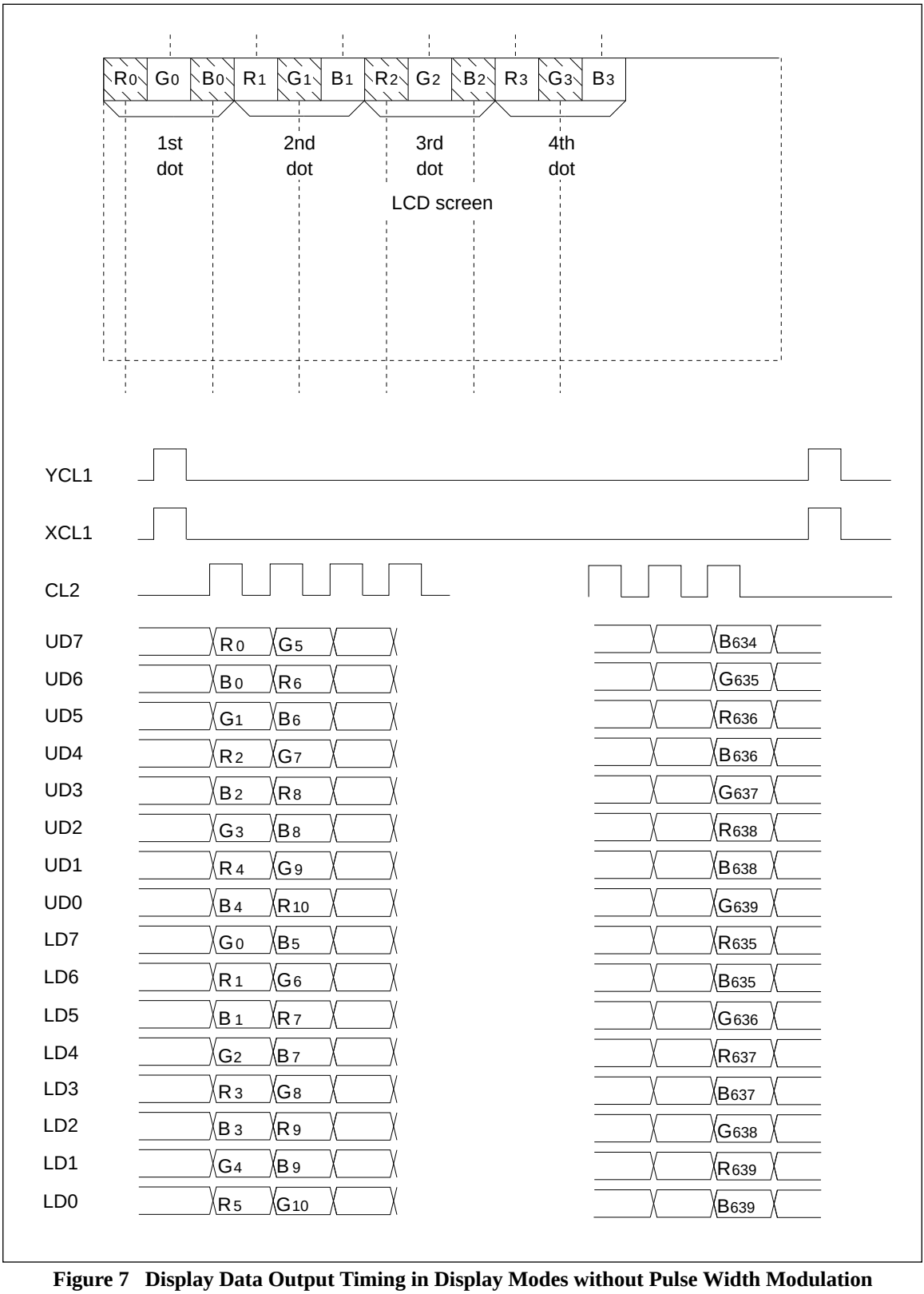


Figure 7 Display Data Output Timing in Display Modes without Pulse Width Modulation (Modes 15 and 18)

In figure 8, data P0–0, P4–0, ... P636–0 make up the first set of data for one line to be output to LCD drivers via pin UD3. Likewise, data P0–1, P4–1, ... P636–1 make up the second set of data. The combination of the first and second sets of data determines the display status as follows: (first data, second data) = (0, 0): display off; (1, 0): 1/2 pulse width modulation; and (1, 1): display on. For more details, refer to the Gradation Display Methods section.

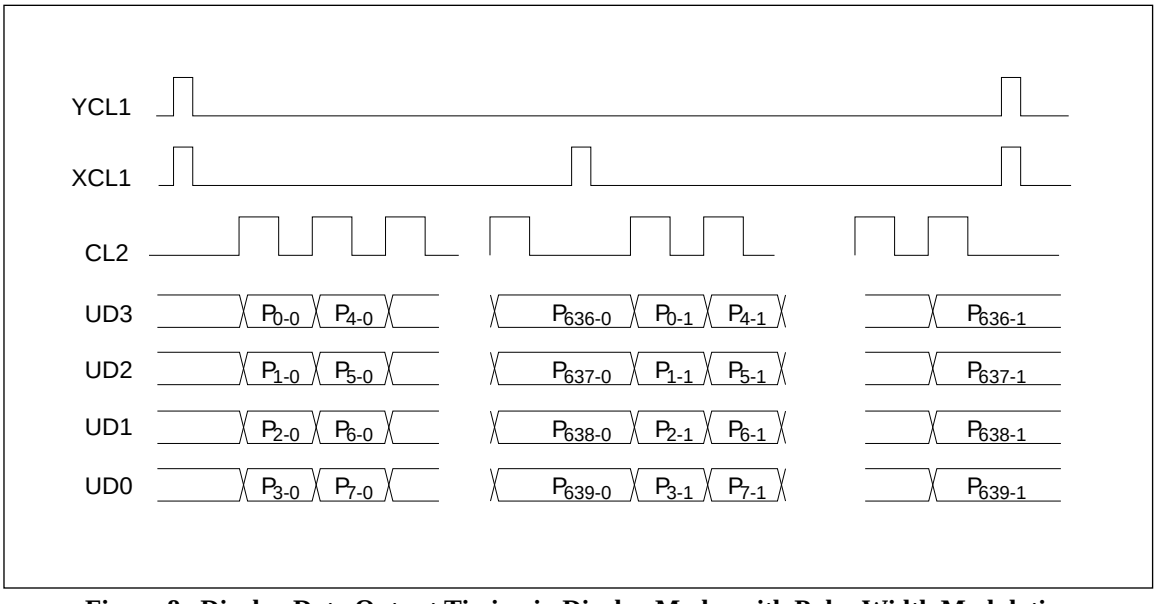


Figure 8 Display Data Output Timing in Display Modes with Pulse Width Modulation (Mode 10)

Gradation Display Methods

The CLINE supports the frame-based data thinning method and pulse width modulation method for gradation display.

Frame-Based Data Thinning Method: In the frame-based data thinning method, the CLINE thins out the display data in line or dot units in the specified frames.

Pulse Width Modulation Method: In the pulse width modulation method, the CLINE combines 1/2 pulse width modulation and frame-based data thinning. In this case, data is output from X-drivers twice in one line-selection period (figure 9).

Consequently, the X-driver latch clock must be different from the Y-driver shift clock, and a conventional LCD module configuration cannot be used. Therefore, clock XCL1 must be supplied to X-drivers and clock YCL1 to Y-drivers (figure 10).

The XCL1 period is specified by the gradation display clock period register (R13 and R14) when no buffer memory is used in non-VGA modes and in the internal register programming method. (Pulse width modulation is unavailable when buffer memory is not used in non-VGA modes, pin programming method.) In the other cases, the register is automatically set, since the YCL1 period is fixed (table 12).

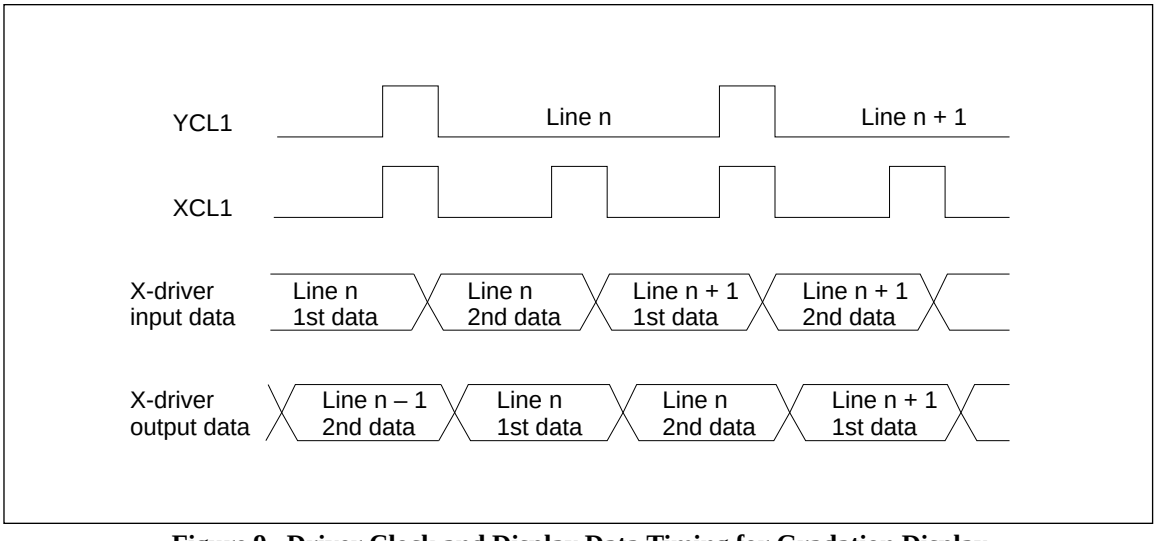


Figure 9 Driver Clock and Display Data Timing for Gradation Display with 1/2 Pulse Width Modulation

Table 12 XCL1 Period Setting

Memory Mode		XCL1 Period	Setting
With-memory		Half of YCL1 period for 1/2 pulse with modulation method	Automatic
Without-memory	VGA	Half of YCL1 period for 1/2 pulse width modulation method	Automatic (See note below)
	Non-VGA		
	Internal register programming	Conforms to gradation display clock register (R13, R14) settings	Required (R13, R14)
	Pin programming	—	

Note: Total number of horizontal dots must be 400, 450, 800, or 900 for displaying 320, 360, 640, or 720 dots, respectively.

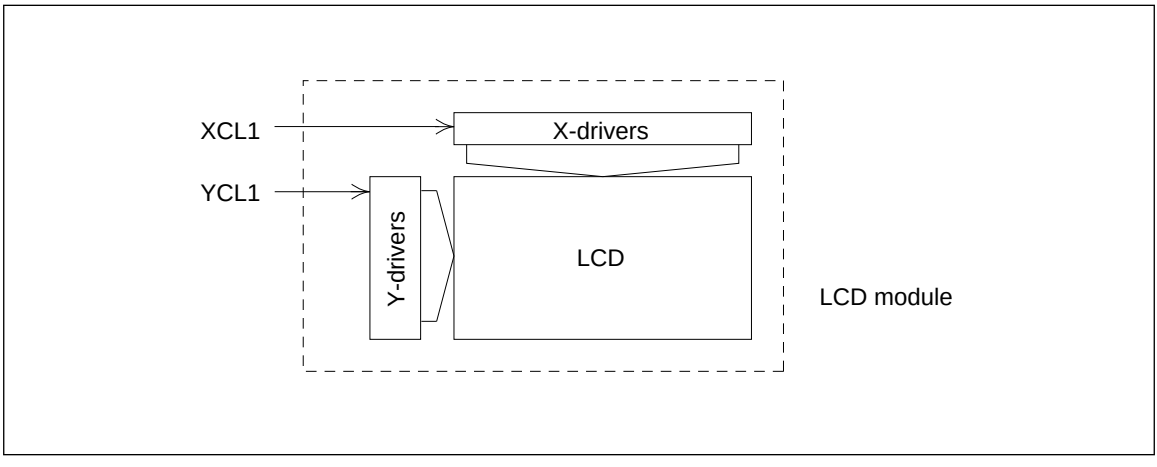


Figure 10 X- and Y-Driver Clock Connection for Pulse Width Modulation Method

Gradation Level Palettes

Gradation display quality depends greatly on LCD panel characteristics.

Consequently, uniform gradation display may be impossible for some panels. To accommodate this situation, the CLINE incorporates a set of gradation level palettes that can assign any gradation level to any CRT display color as desired.

16 levels are available for gradation display using the frame-based data thinning method and 31 levels using 1/2 pulse width modulation method. Appropriate levels can be selected for the LCD panel used.

The R-, G-, and B-palettes are used for color level display modes, while only the R-palette is used for 16-level grayscale display modes.

In pin programming and MPU programming methods, these palettes are automatically loaded after reset with appropriate data for frame-based data thinning modes and 1/2 pulse width modulation modes. The automatically set data cannot be rewritten in the pin programming method, but can be rewritten, any time after 100 µs have elapsed after reset, in MPU programming method.

By contrast, in the ROM programming method, these palettes are not automatically set. Thus writing the necessary data to the palettes is always required.

Table 13 shows the relationship between the values set in the palettes (through R12) and gradation levels. Values other than those shown here disable correct display.

Table 13 Relationship between Gradation Levels and Palette (R12) Values

(a) Frame-based data thinning modes

Gradation Level No.	Palette Data (R12 Data Bits) 5	4	3	2	1	0	Gradation Level
0	1	0	0	0	0	0	0.00
1	1	0	0	0	0	1	0.14
2	1	0	0	0	1	0	0.20
3	1	0	0	0	1	1	0.29
4	1	0	0	1	0	0	0.33
5	1	0	0	1	0	1	0.40
6	1	0	0	1	1	0	0.43
7	1	0	0	1	1	1	0.50
8	1	0	1	0	0	0	0.57
9	1	0	1	0	0	1	0.60
10	1	0	1	0	1	0	0.66
11	1	0	1	0	1	1	0.71
12	1	0	1	1	0	0	0.75
13	1	0	1	1	0	1	0.80
14	1	0	1	1	1	0	0.86
15	1	0	1	1	1	1	1.00

(b) 1/2 pulse width modulation modes

Gradation Level No.	Palette Data (R12 Data Bits) 5	4	3	2	1	0	Gradation Level
0	0	1	0	0	0	0	0.00
1	0	1	0	0	0	1	0.07
2	0	1	0	0	1	0	0.10
3	0	1	0	0	1	1	0.14
4	0	1	0	1	0	0	0.17
5	0	1	0	1	0	1	0.20
6	0	1	0	1	1	0	0.21
7	0	1	0	1	1	1	0.25
8	0	1	1	0	0	0	0.29
9	0	1	1	0	0	1	0.30
10	0	1	1	0	1	0	0.33
11	0	1	1	0	1	1	0.36
12	0	1	1	1	0	0	0.38
13	0	1	1	1	0	1	0.40
14	0	1	1	1	1	0	0.43
15	0	1	1	1	1	1	0.50
16	1	1	0	0	0	0	0.50
17	1	1	0	0	0	1	0.57
18	1	1	0	0	1	0	0.60
19	1	1	0	0	1	1	0.64
20	1	1	0	1	0	0	0.67
21	1	1	0	1	0	1	0.70
22	1	1	0	1	1	0	0.71
23	1	1	0	1	1	1	0.75
24	1	1	1	0	0	0	0.79
25	1	1	1	0	0	1	0.80
26	1	1	1	0	1	0	0.83
27	1	1	1	0	1	1	0.86
28	1	1	1	1	0	0	0.88
29	1	1	1	1	0	1	0.90
30	1	1	1	1	1	0	0.93
31	1	1	1	1	1	1	1.00

Display On/Off Control

When the LCD drivers used have an LCD on/off control pin, display can be controlled with the CLINE DISPON signal. When the LCD drivers used do not have an LCD on/off control pin, the CLINE can turn off display by transferring all-0 display data to the drivers.

Display will be turned on with the DISPON pin = 1, turns the display off while DISPON = 0. The DISPON pin is equivalent to the DISPON bit (bit 0) of the control register.

In the pin programming method, display is on except for four frames after reset. The four frame display-off time period prevents random display at power-on. In the MPU programming method, display is turned off at reset, but can be freely turned on or off after four frames after reset by rewriting the corresponding register bit. In the ROM programming method, a 1 must be written to the DISPON bit to turn on display. Like in other programming methods, display is off for four frames after reset.

LDOTCK Frequency and Data Transfer Rate

The LDOTCK frequency (f_{LDOTCK}) for asynchronous mode is calculated from the following equation:

$$f_{LDOTCK} = (Nhd + 48) \times Nvd \times f_F$$

Nhd: Number of dots contained in one horizontal line of the LCD panel
Nvd: Number of horizontal lines from the LCD panel top to bottom
f_F: Frame frequency

In this case, the following relationship must hold true:

$$1/2 \times f_{DOTCLK} < f_{LDOTCK} < 2 \times f_{DOTCLK}$$

f_{DOTCLK}: Dot clock frequency

The data transfer rate to LCD drivers depends on the mode in which the CLINE is used. Specifically, the rate depends on screen configura-tion (single or dual), data transfer width (bit count), and gradation display methods. For example, the data transfer rate will be doubled for 1/2 pulse width gradation display. This is because data must be transferred two times during one line-selection period. The data transfer rate (f_{CL2}: CL2 frequency) is calculated from the following equation ($f_{LDOTCK} = f_{DOTCLK}$ for synchronous mode):

$$f_{CL2} = \frac{f_{LDOTCK} \times l}{n \times m}$$

n: Number of panels composing one screen
— 1 for modes 1, 3, 5, 7, 9, 11, 13-20
— 2 for modes 2, 4, 6, 8, 10, 12

m: Number of bits transferred at one time
— 2 for modes 13, 16
— 4 for modes 1, 2, 5, 6, 9, 10, 14, 15, 17-20
— 8 for modes 3, 4, 7, 8, 11, 12

l: Constant for each gradation display
— 1 for modes 1-8, 13-18
— 2 for modes 9-12, 19, 20

Synchronous/Asynchronous Modes and Memory

The CLINE has two timing modes: asynchronous and synchronous.

In asynchronous mode, dot clock pulses for the CRT system (DOTCLK) are different from those for the LCD system (LDOTCK) in frequency to accommodate frame frequency conversion. This requires buffer memory as shown in figure 11 (a). In this mode, dual screen LCD panels can be used.

In synchronous mode, dot clock pulses for the CRT system are identical to those for the LCD system, thus requiring no buffer memory in principle (synchronous without-memory mode (figure 11 (b)). However, synchronous without-memory mode cannot support dual screen LCD panels.

The CLINE has another mode in which dual screen LCD panels can be used and fewer memory devices are required. This is called “synchronous with-memory mode” (figure 11 (c)). In this mode, the number of memory devices can be reduced to a half or a third that of asynchronous mode. This is because RGB data sent from the CRT system is processed for gradation display before being written into buffer memory. (In asynchronous mode, on the other hand, R, G, and B data sent from the CRT system is separately written into the R-plane, G-plane, and B-plane memories, respectively.)

Table 14 summarizes these modes.

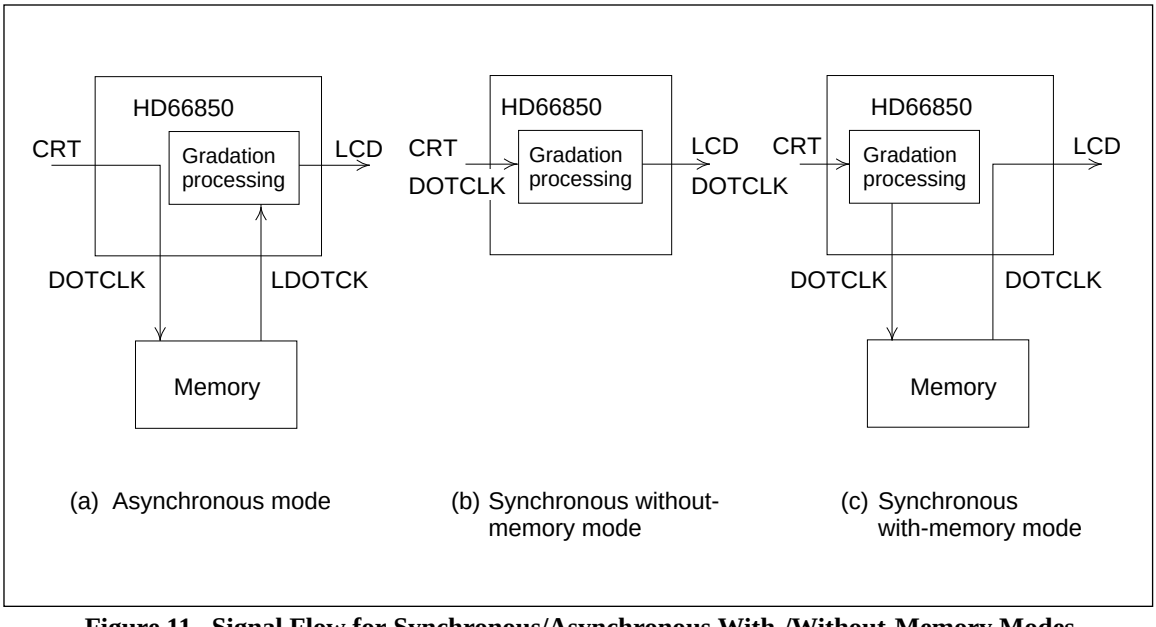


Figure 11 Signal Flow for Synchronous/Asynchronous With-/Without-Memory Modes

The CLINE uses dual port RAMs for buffer memory, enabling high-speed display and independent use of an LCD dot clock and a CRT dot clock.

The CLINE supports three types of memory configurations: 64 k × 4 bits (256 k), 256 k × 4 bits (1 M), and 128 k × 8 bits (1 M), any of which can be selected with the MMODE0 and MMODE1 pins (table 3).

The number of memory devices required depends on the LCD panel size and the display mode. However, it depends only on LCD panel vertical size and not on horizontal size since the CLINE uses memory as shown in figure 12. For example, one 256-kbit memory device is required for the panel having 256 or less lines and two for that having 257 to 512 lines. Table 15 lists the number of memory devices required for each mode.

Table 14 Memory Mode Summary

	Asynchronous With-Memory Mode	Synchronous With-Memory Mode	Synchronous Without Memory Mode
Centering/stretching	Possible	Possible	Impossible
Max number of gray levels	16	16	16
Max number of color levels	16	4096 (frame-based data thinning)	4096 (pulse width modulation)
Dual screen	Possible	Possible	Impossible
Max number of display lines	512	512	1024
Frame frequency conversion	Possible	Impossible	Impossible

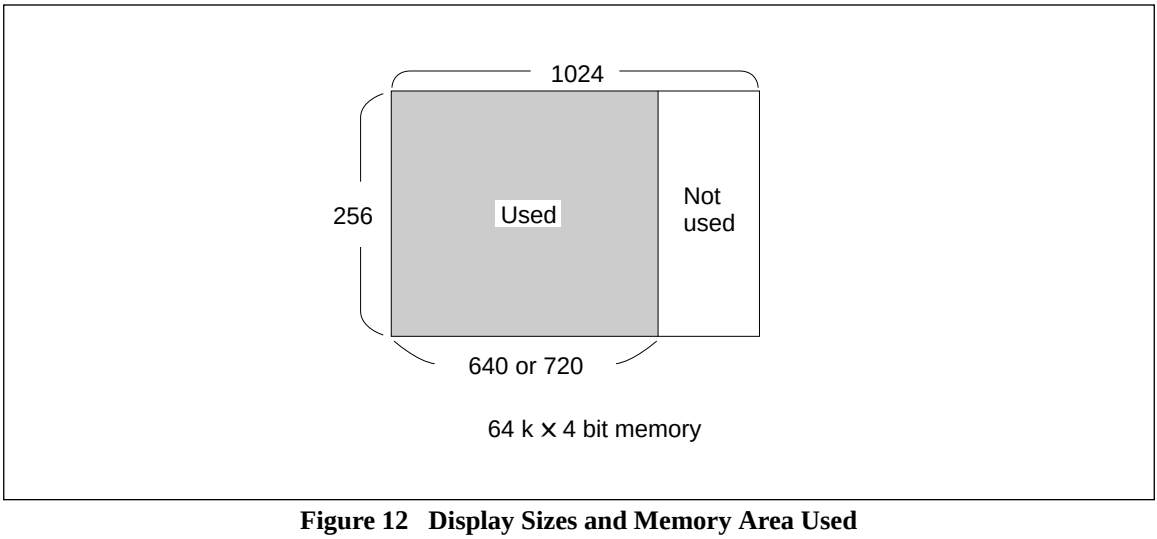


Figure 12 Display Sizes and Memory Area Used

Table 15 Number of Memory Devices for Different Display modes

	Number of Memory Devices Required					
	Asynchronous			Synchronous		
Display Mode	**64 k × 4**	**256 k × 4**	**128 k × 8**	**64 k × 4**	**256 k × 4**	**128 k × 8**
Monochrome Modes 1–4	2	1	1	2	1	1
16-level grayscale (frame-based) Modes 5–8	8	4	2	2	1	1
16-level grayscale (1/2 pulse width) Modes 9–12	8	4	2	4	2	1
8-color Mode 15	6	3	2	6	3	2
16-color Modes 13, 14	8	4	2	8	4	2
4096-color-scale (frame-based) Modes 16–18	—	—	—	6	3	2

Frame-based: Frame-based data thinning method
1/2 pulse width: 1/2 pulse width modulation method

Note: With-memory mode does not support color level display using the pulse width modulation method.

Display Timing Signal Fine Adjustment

When the display timing signal is supplied externally, a phase shift may appear between CRT data and the display timing signal, since each signal has its own peculiar lag. The CLINE can adjust the display timing signal with pins AJ3–AJ0 (in pin programming method) or with the input timing control register (R1) (in internal register programming method) to compensate the phase shift (table 1).

Figure 13 (a) shows an example of adjusting a display timing signal that is two dots ahead of the display start position. In this case, pins (AJ3, AJ2, AJ1, AJ0) or data bits (3, 2, 1, 0) of R1 must be set to (1, 0, 1, 0) to delay the signal for two dots. Conversely, they must be set to (0, 0, 1, 0) to advance the signal for two dots for the case of figure 13 (b), where the display timing signal is two dots behind.

When there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 0, 0) will work.

It should be noted that the VGA CRT system applies the BLANK signal, which includes the border area period, as the display timing signal, and that the CLINE removes the border area period. Consequently, the border area period must be considered for adjusting the display timing signal.

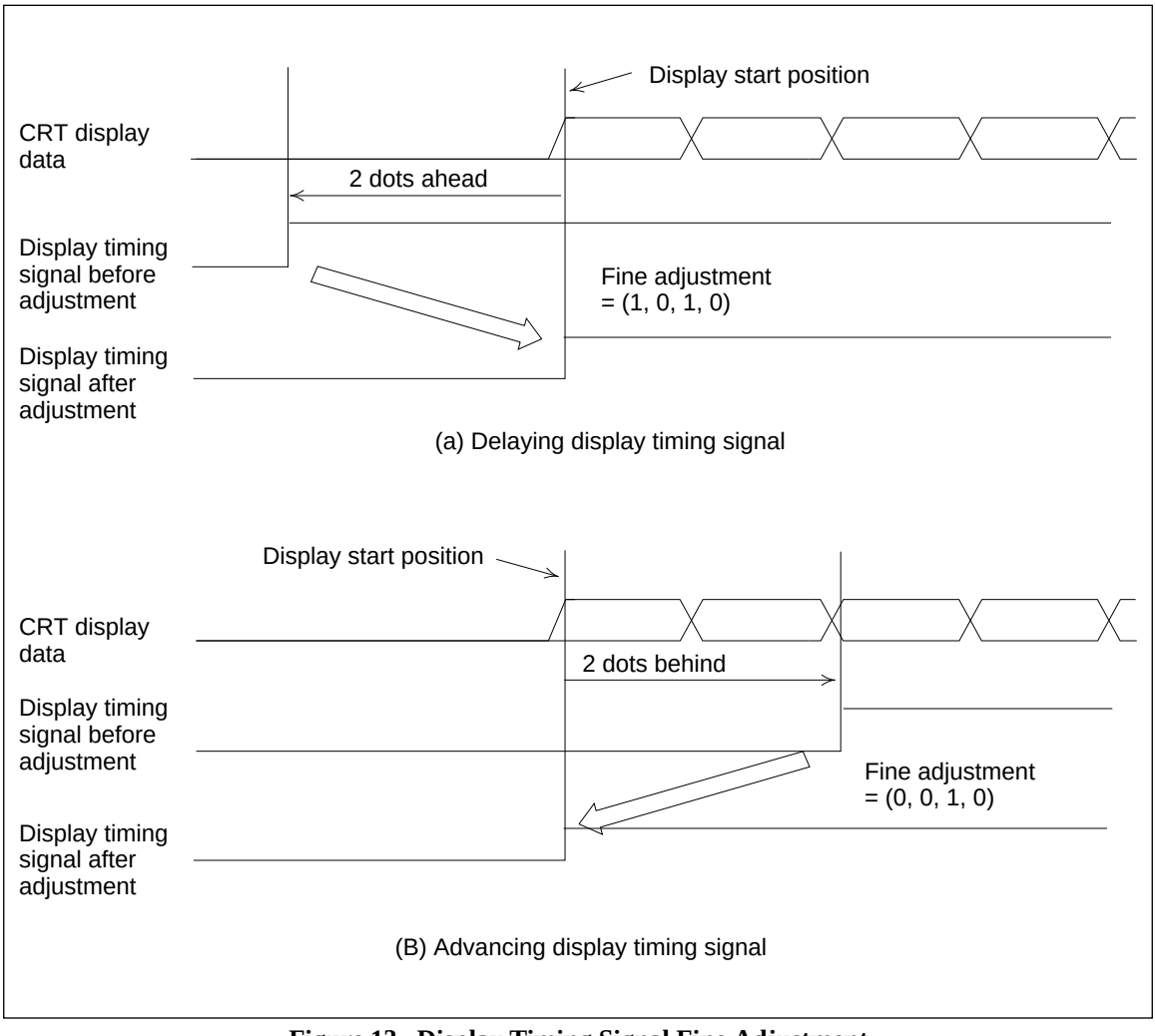


Figure 13 Display Timing Signal Fine Adjustment

Border Color Control

In the internal register programming method, the CLINE can specify the color of a blank area that is left on a centered display (figure 14). Any of 16 colors or the color of the dot immediately before the valid display data can be specified by the border color control register (R7). However, the desired color can be specified only in asynchronous mode.

In the pin programming method, the specified color is always the same color as the dot immediately before the valid display data.

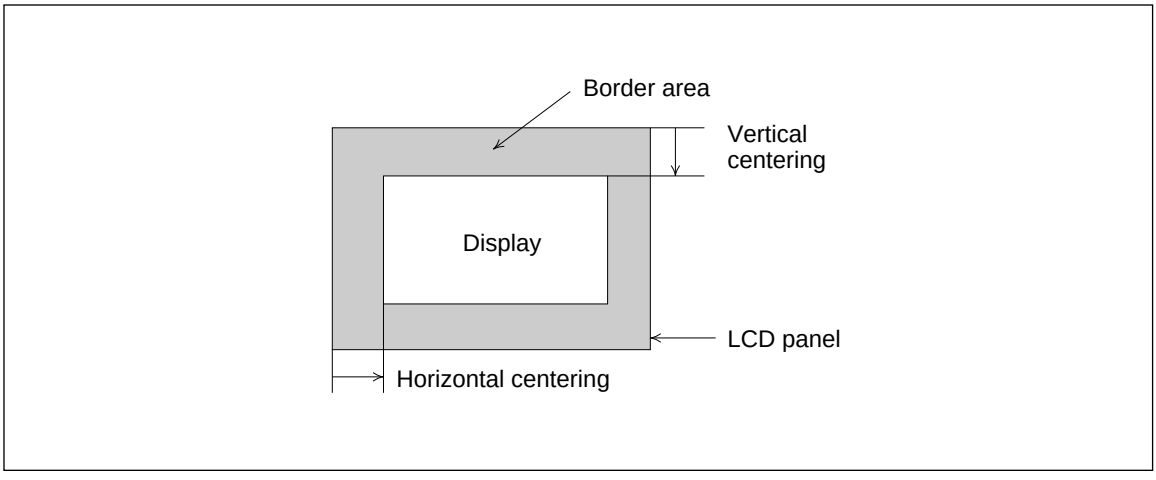


Figure 14 Border Area and an LCD Panel

Internal Registers

The CLINE has one index register (IR) and 15 data registers (R0–R14). In the MPU programming method, the desired register address must be written in one cycle into the index register before writing or reading data to/from the register in the following cycle. By contrast, in the ROM programming method, the index register is not used; the CLINE automatically reads data from the ROM, in which data has been written to the ROM addresses corresponding to the desired data registers, and writes it to the data register. Registers are valid only for the internal register programming method and are invalid (don't care) for the pin programming method. Since all data registers are reset to 0s, they must be rewritten after reset.

Register Access for MPU Programming Method

First write the desired data register address into the index register with $\overline{CS}$ = 0, RS = 0, and $\overline{WR}$ = 0, then write/read data to/from the register with $\overline{CS}$ = 0, RS = 1, and $\overline{WR}$ = 0 or $\overline{RD}$ = 0. Figure 15 shows the timing for writing data into an internal register.

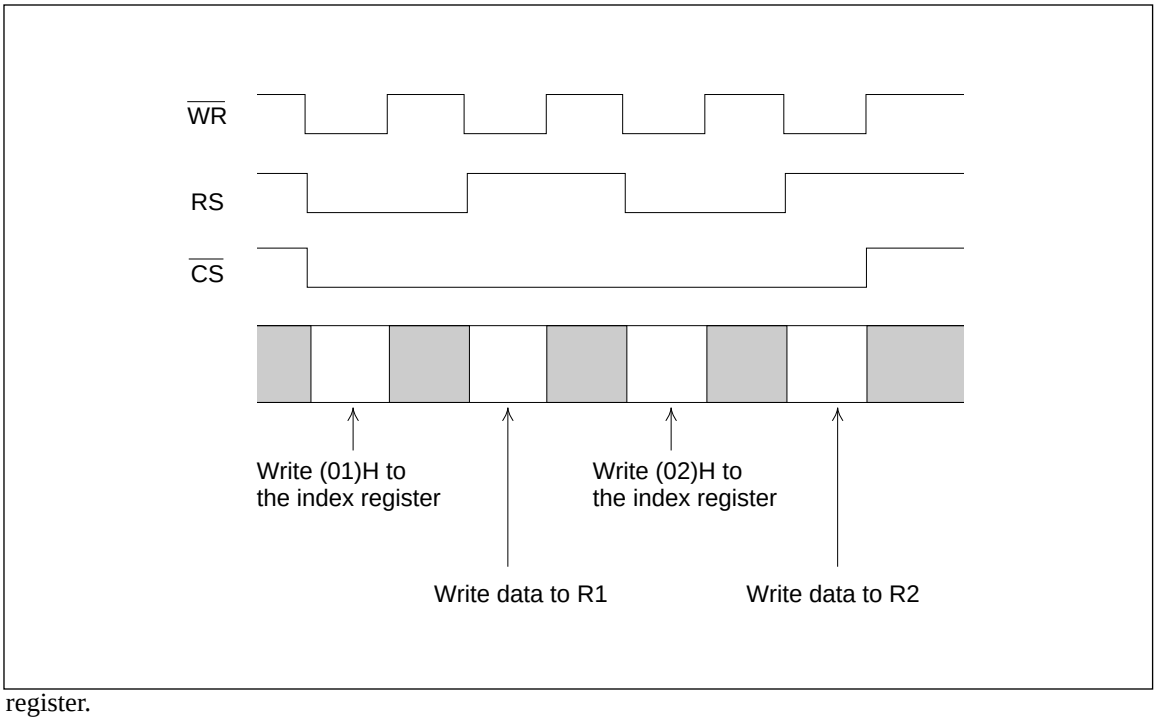


Figure 15 Internal Register Write by MPU

ROM Data Setting for ROM Programming Method

The desired data must have been previously written to the ROM addresses corresponding to the data register addresses; that is, to ROM addresses $0000–$000F. Data for the gradation level palettes must have been written to ROM addresses $0010–$003F. Consequently, data written for internal registers R11 and R12 are invalid. Figure 16 shows the ROM address map.

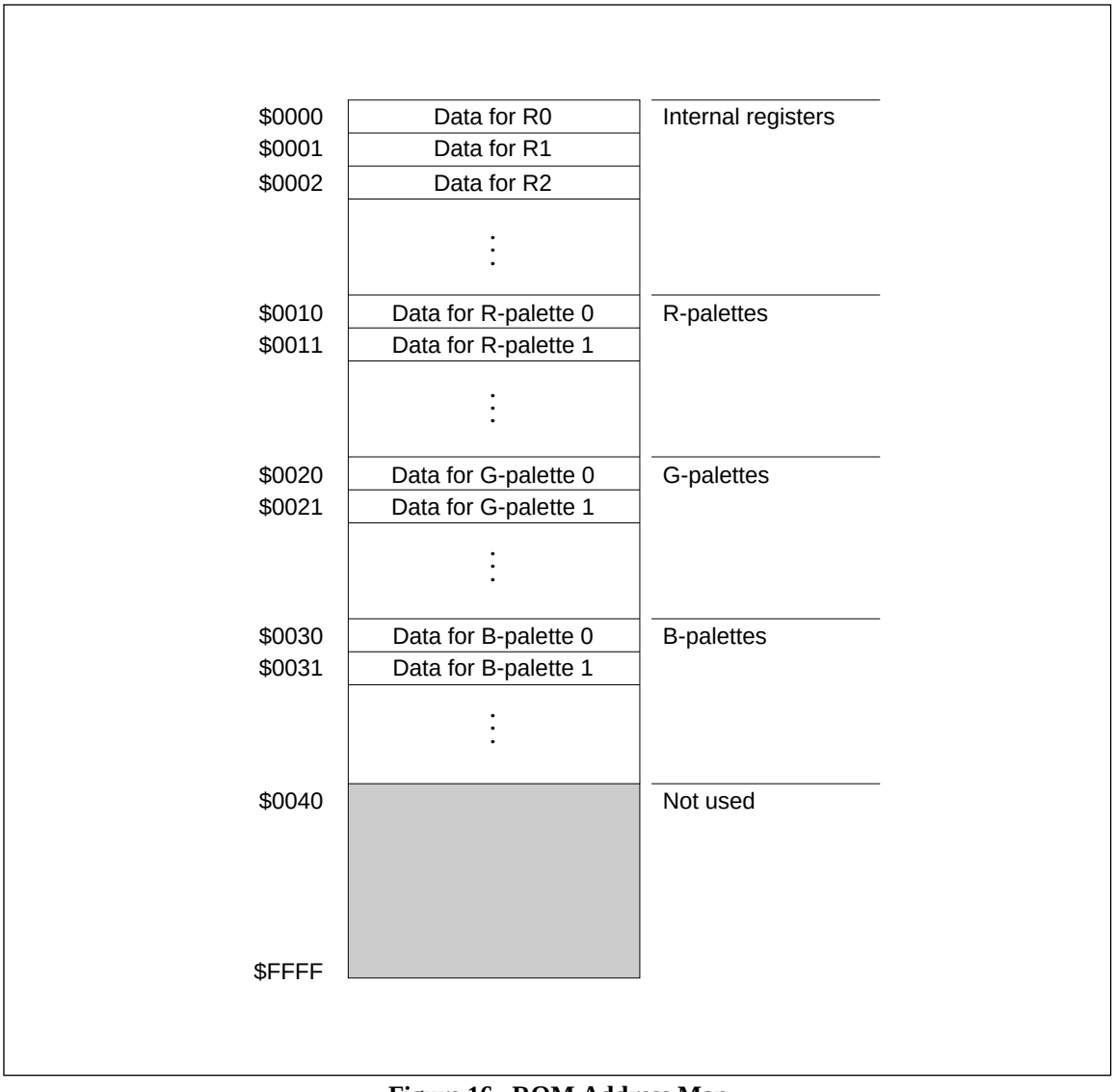


Figure 16 ROM Address Map

Register Function

Index Register (IR): The index register (figure 17), composed of four valid bits, selects one of the 15 data registers. The index register itself is selected by the MPU while the RS signal is low and selects a data register with the register address written.

Control Register (R0): The control register (figure 18) is composed of five valid bits, each with a particular function.

- STE bit
  - — STE = 1: Stretching function enabled
  - — STE = 0: Stretching function disabled
- CRE bit
  - — CRE = 1: Vertical centering function enabled
  - — CRE = 0: Vertical centering function disabled

Simultaneous use of stretching and vertical centering functions is impossible; if both the CRE and STE bits are set to 1 at the same time, correct display will be disabled.

- CCE bit
  - — CCE = 1: Horizontal centering function enabled
  - — CCE = 0: Horizontal entering function disabled
- SP bit
  - — SP = 1: Double-width display
  - — SP = 0: Normal display
- DISPON bit
  - — DISPON = 1: Display on
  - — DISPON = 0: Display off

DISPON is always cleared at reset. In the MPU programming method, rewriting this bit can always be rewritten. However, display will be off for four frames after reset, regardless of the status of this bit.

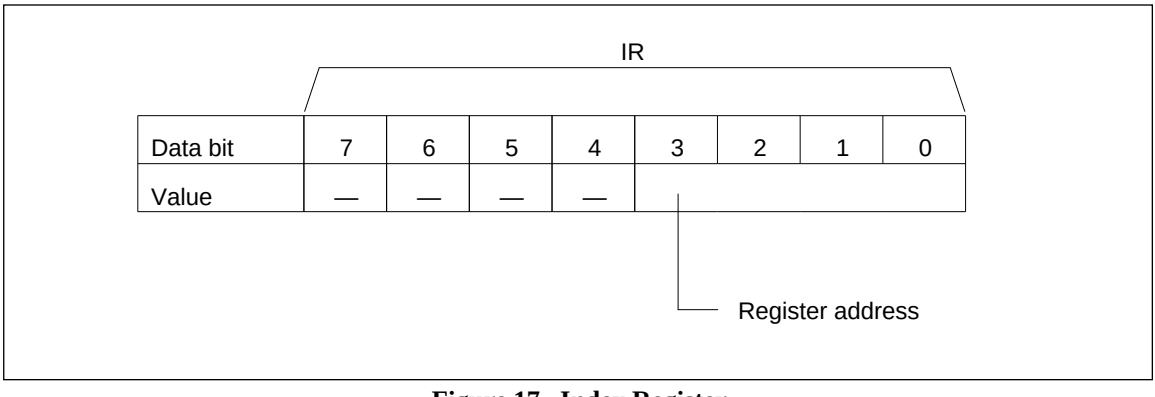


Figure 17 Index Register

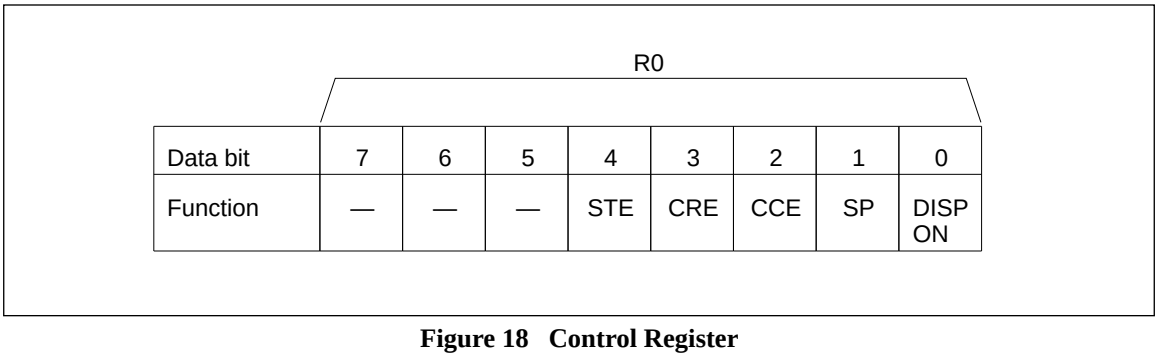


Figure 18 Control Register

Input Timing Control Register: The input timing control register (figure 19) has five valid bits, having two different functions.

- DOTE bit : Switches RGB data latch timing.
  - — DOTE = 1: Latches data at the rising edge of the dot clock pulses
  - — DOTE = 0: Latches data at the falling edge of the dot clock pulses
- AJ3-AJ0 bits: Adjust the externally supplied display timing signal to synchronize its phase with that of LCD data. Write the shift, represented in dots, between the display timing signal and the display start position to these bits. The absolute value of the number of dots to be shifted must be written to the AJ2-AJ0 bits and shift polarity to the AJ3 bit. If there is no need to adjust the display timing signal, these bits may be set to either (1, 0, 0, 0) or (0, 0, 0, 0).

R1

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	DOTE	AJ3	AJ2	AJ1	AJ0

3	2	1	0	Number of Dots Adjusted
0	0	0	0	0
	0	0	1	–1
	0	1	0	–2
1	0	0	0	0
	0	0	1	+1
	0	1	0	+2
	0	1	1	+3
	1	0	0	+4
	1	0	1	+5
	1	1	0	+6

Note: – (minus) and + (plus) in the Number of Dots Adjusted column indicate advancing and delaying the display timing signal, respectively.

Figure 19 Input Timing Control Register

Horizontal Display Size Register: The horizontal display size register (figure 20), composed of seven valid bits, specifies the horizontal display size in units of characters (eight dots). The value to write to this register is "number of characters displayed on one horizontal line – 1." A maximum of 90 characters (720 dots) can be specified.

This register is set automatically in VGA mode.

Vertical Display Size Register: The vertical display size register (figure 21), composed of nine valid bits, specifies the vertical display size in units of lines. The value to write to this register is "number of lines displayed from display screen top to bottom – 1." A maximum of 512 lines can be specified.

This register is set automatically in VGA mode.

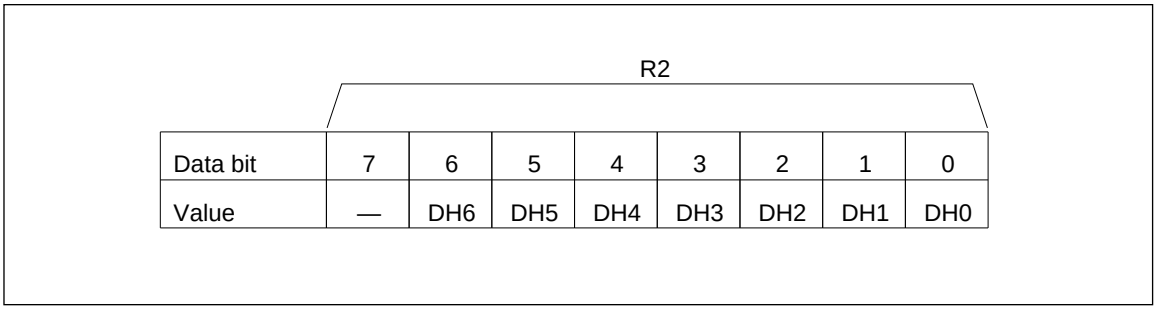


Figure 20 Horizontal Display Size Register

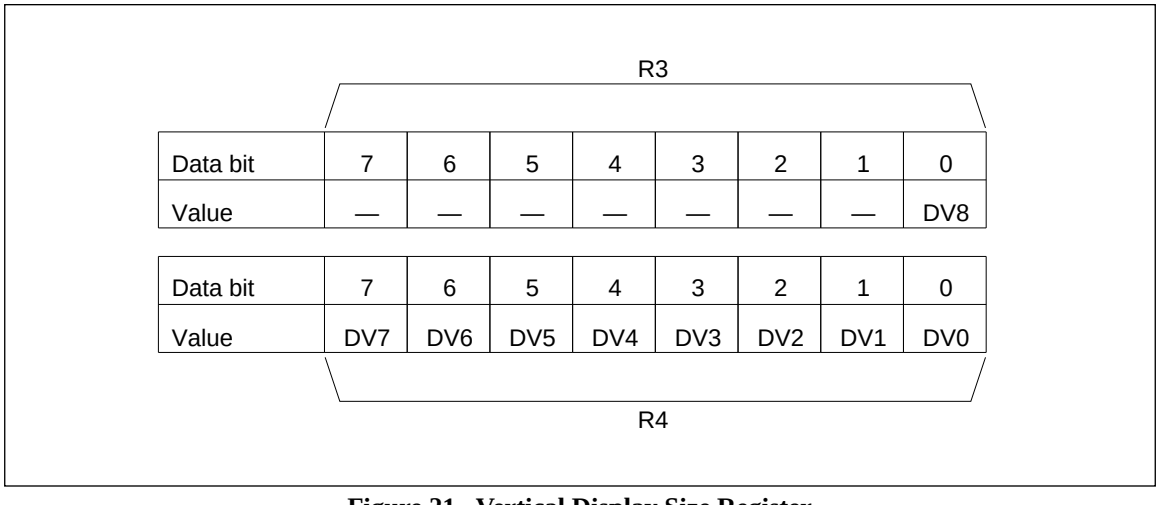


Figure 21 Vertical Display Size Register

Centering Raster Register: The centering raster register (figure 22), composed of eight bits, specifies the number of rasters for vertically centering the display within the range of 1 to 256. The value to write to this register is "number of rasters for centering – 1." As shown in figure 23, the number here indicates the number of rasters in either the upper border area or lower border area, not the total number. Since the LCD panel size is determined by this number and the display size, the number of rasters must be correctly written if the display size differs from the LCD panel size. Incorrect setting disables correct display. This register is enabled the control register's CRE bit is 1. This register is set automatically in VGA mode.

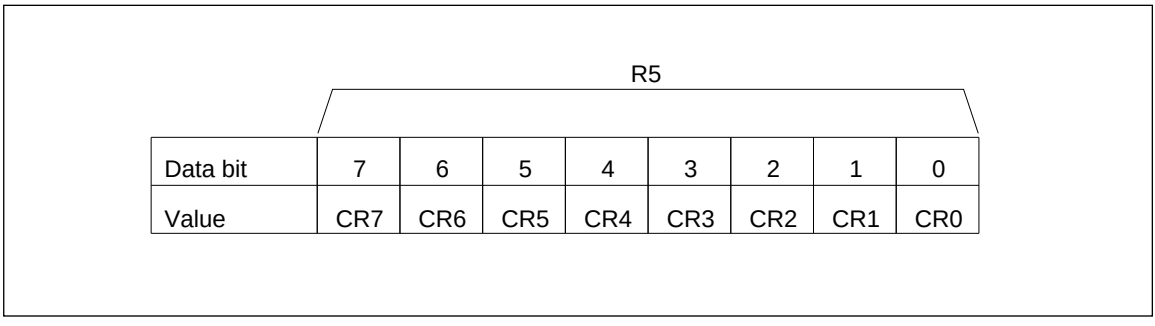


Figure 22 Centering Raster Register

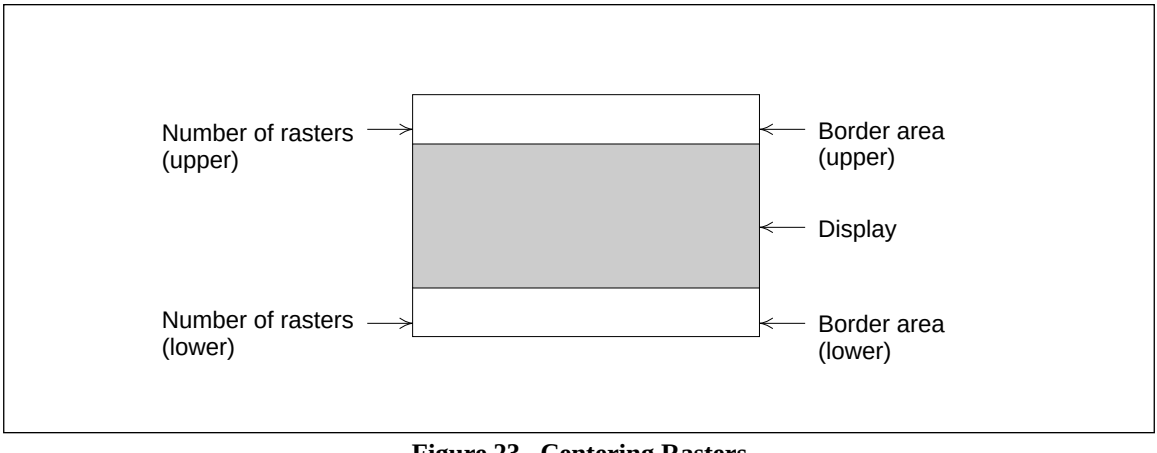


Figure 23 Centering Rasters

Centering Character Register: The centering character register (figure 24), composed of five valid bits, specifies the number of characters for horizontally centering the display within the range of 1 to 32. The value to write to this register is "number of characters for centering – 1." As shown in figure 25, the number here indicates the number of characters in either the left border area or right border area, not the total number. Since the LCD panel size is determined by this number and the display size, the number of characters must be correctly written when the display size differs from the LCD panel size. Incorrect setting disables correct display. This register is enabled when the control register's CCE bit is 1.

This register is set automatically in VGA mode.

R6

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	CC4	CC3	CC2	CC1	CC0

Figure 24 Centering Character Register

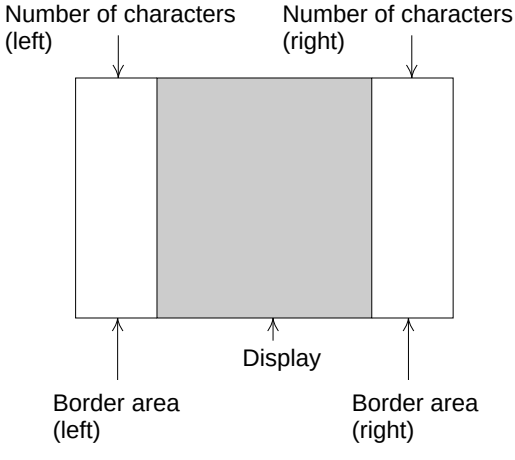


Figure 25 Centering Characters

Border Color Control Register: The border color control register (figure 26), has five valid bite having two different functions. These functions are available only in with-memory mode.

- BM bit: Specifies border control mode; reset to 0. This bit must be 1 in asynchronous mode.
  - — BM = 1: Displays the color specified by the BCI, BCR, BCG, and BCB bits in the border area (disabled in synchronous mode)
  - — BM = 0: Displays the color of the dot immediately before the display period on the border area
- BCI, BCR, BCG, and BCB bits: Specify the color to be displayed on the border area. These bits are enabled when the BM bit is 1; reset to 0s.

Stretching Control Register: The stretching control register (figure 27), composed of four valid bits, is used in combination with the stretching index register (R9 and R10). It specifies the period for stretching in units of lines. The value to write to this register is "number of lines –1." This register is enabled when the control register's STE bit is 1.

This register is set automatically in VGA mode.

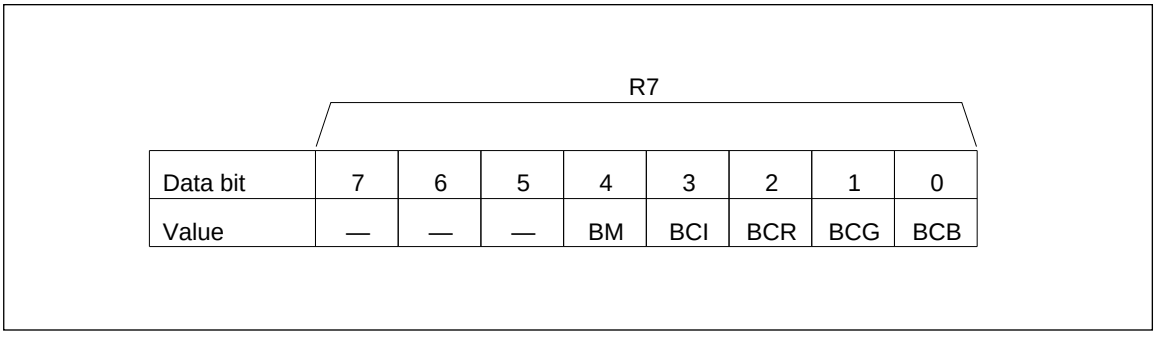


Figure 26 Border Color Control Register

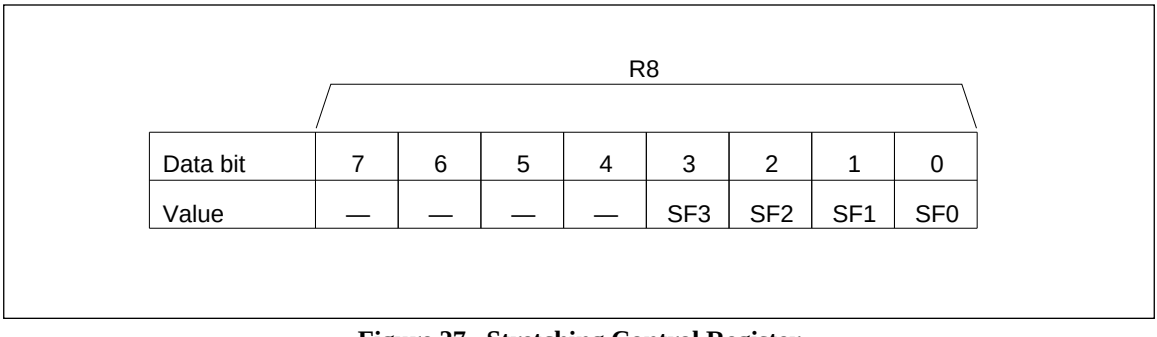


Figure 27 Stretching Control Register

Stretching Index Register: The stretching index register (figure 28), composed of 16 valid bits, is used in combination with the stretching control register (R8). It specifies the lines to be displayed twice among those specified by R8. The lines represented by the SI bits which are set to 1s will be displayed twice. Although this register has 16 bits, only the bits within the period specified by R8 are enabled. For example, when R8 is set to four, only five bits of SI0 to SI4 of this register are enabled (figure 29).

This register is set automatically in VGA mode.

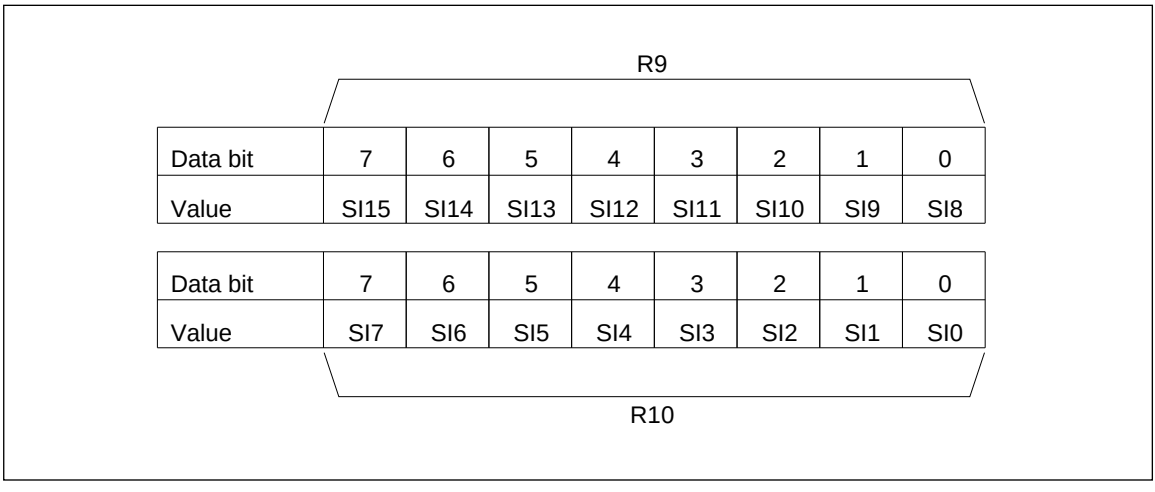


Figure 28 Stretching Index Register

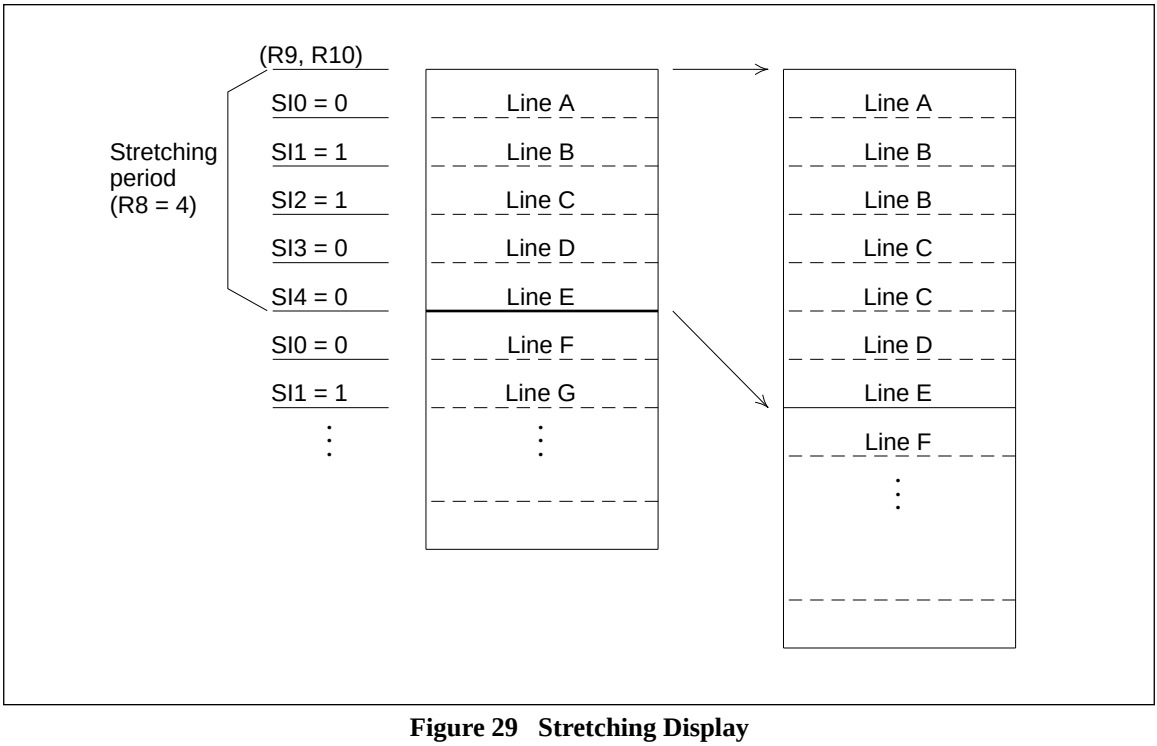


Figure 29 Stretching Display

Gradation Level Palette Address Register: The gradation level palette address register (figure 30) is composed of six valid bits with two different functions.

- PS1 and FS0 bits: Specify a method of selecting the plane of the gradation level palettes (R, G, or B).
  - — (PS1, PS0) = (0, 0): Every time the gradation level palette data register (R12) is read from or written to, either R-, G-, or B-palette is automatically selected, in that order
  - — (PS1, PS0) = (0, 1): R-palette is selected
  - — (PS1, PS0) = (1, 0): G-palette is selected
  - — (PS1, PS0) = (1, 1): B-palette is selected
- PA3–PA0 bits: Specify the desired gradation level palette using the address written to these bits. After palette address specification, data is read from or written to the specified palette and the address is automatically incremented by 1. The address increment manner depends on PS1 and PS0 settings.
  - — (PS1, PS0) = (0, 0): Gradation level palette address is automatically incremented by 1 after reading/writing data from/to R, G, and B gradation level palettes in that order, through the gradation level palette data register
  - — Other settings: Gradation level palette address is automatically incremented by 1 after reading/writing data from/to any one gradation level palette, through the gradation level palette data register

R11

Data bit	7	6	5	4	3	2	1	0
Value	—	—	PS1	PS0	PA3	PA2	PA1	PA0

Figure 30 Gradation Level Palette Address Register

Gradation Level Palette Data Register: The gradation level palette data register (figure 31), composed of six valid bits, contains data which is read from or written to the gradation level palette specified with the gradation level palette address register (R11).

Gradation level palettes must be set according to the display mode used (16-level grayscale display or 4096-color-scale display); the R-palette must be used for 16-level grayscale display, and R-, G-, and B-palettes for 4096-color-scale display. PD5 bit must be 1 and PD4 bit must be 0 in frame-based data thinning mode. PD4 bit must be 1 in 1/2 pulse width modulation mode. Show table 13.

In the MPU programming method, the gradation level palettes must be read/written after 100 ms have elapsed after reset. Note that display is scattered during palette read/write.

In the MPU programming method, gradation level palettes are not directly read from, but are read from via this register. Consequently, any data that happens to be in this register at that time is read out in the first read cycle, and then data corresponding to the specified address is transferred to this register and read from this register in the following read cycle. The address is incremented (or R-, G-, and B-palettes are switched) at the same time. In other words, after address setting, the first data read is incorrect, and the second data read is correct. Consequently, one dummy read is required after setting a gradation level palette address. Figure 32 shows the timing for reading a gradation level palette.

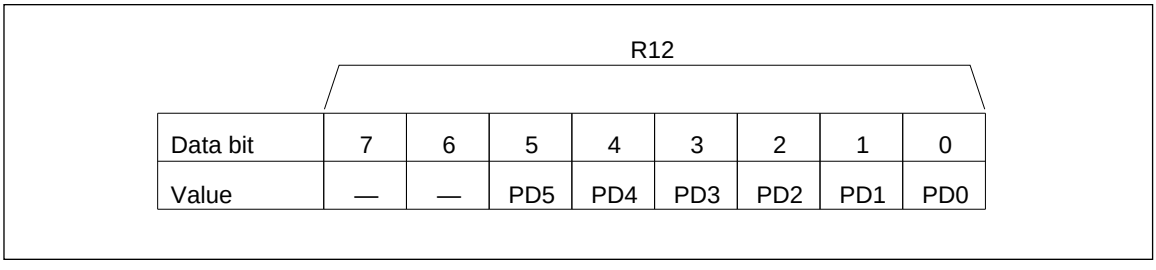


Figure 31 Gradation Level Palette Data Register

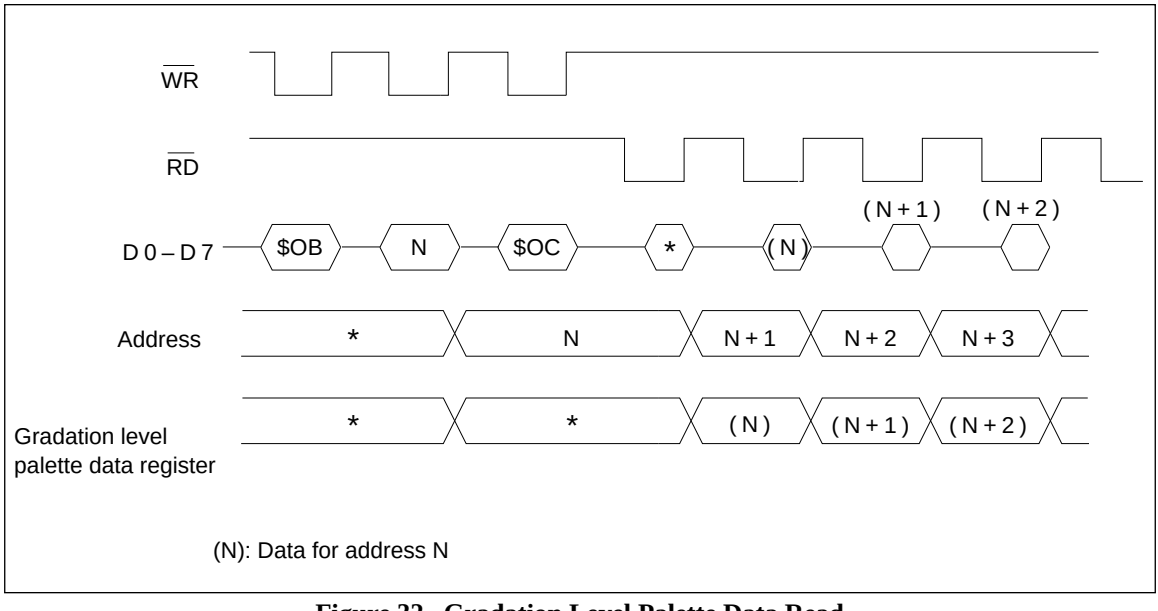


Figure 32 Gradation Level Palette Data Read

Gradation Display Clock Period Register: The gradation display clock period register (figure 33), composed of nine valid bits, specifies the period of XCL1, the LCD data latch clock, when pulse width modulation method is used for gradation display. The value to write to this register is "specified number – 1," in units of dots. Eight through 512 dots can be specified. Note that this register is invalid in with-memory mode.

This register is set automatically in VGA mode.

- GC8–GC0 bits: Specify the number of dots for T1; T1 is the period of XCL1 for 1/2 pulse width gradation display. When the total number of dots for one period of the YCL1 clock pulse cannot be divided by two for 1/2 pulse width gradation display, the remainder is added to T1 as T1', where T1' = T_L – T1 (figure 34).

R13

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	—	—	—	—	GC8

Data bit	7	6	5	4	3	2	1	0
Value	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

R14

Figure 33 Gradation Display Clock Period Register

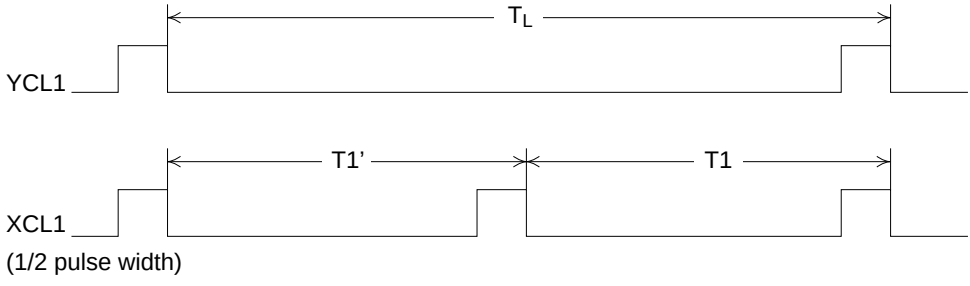


Figure 34 T_L, T1, and T'

Reset Description

The $\overline{RES}$ signal resets and starts the CLINE. The $\overline{RES}$ signal must be supplied at each power-on. Reset is defined as shown in figure 35.

Pin: In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. The reset states of input/output pins are described below.

- D0–D7: Not affected by reset. These pins output data even during the reset state when $\overline{RD}$ = 0, $\overline{CS}$ = 0, RS = 1, and $\overline{WR}$ = 1, in the MPU programming method.
- A0–A5: Always output 0s during the reset state in the ROM programming method. Otherwise, these pins serve as input pins.

Registers: The contents of all internal registers are lost and cleared; the desired data must be rewritten after reset.

Palettes: Palettes are automatically loaded after reset with the appropriate data according to the display mode. When data different from the automatically set data is needed, the data must be overwritten 100 µs or more after reset. (100 µs is required for automatic data setting.)

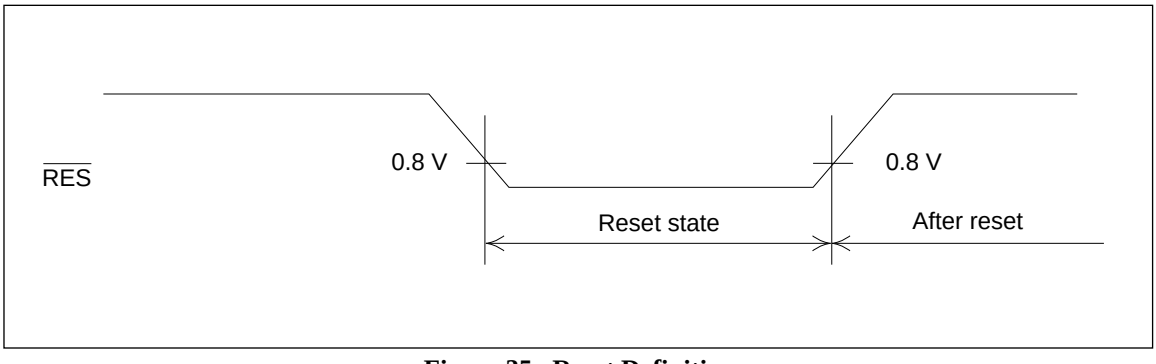


Figure 35 Reset Definition

There are some restrictions and notices in the HD66850F. Please check the following content, and use it.

Input Signal Timing

HSYNC, VSYNC Asserted Width: The HSYNC and VSYNC input signals have the minimum asserted width to operate correctly, please keep the asserted width with the below value or more.

HSYNC to VSYNC, HSYNC to $\overline{\text{BLANK}}$ Phase Shift: There are some restrictions between HSYNC and VSYNC, and HSYNC and $\overline{\text{BLANK}}$. Don't input them within the restricted phase shift.

Table 16 HSYNC, VSYNC Asserted Width

Condition	Item	Symbol	Minimum Dots
All mode	Asserted HSYNC	a	12 dots or more
	Asserted VSYNC	b	2 rasters or more

Table 17 VSYNC, $\overline{\text{BLANK}}$ Phase Shift

Condition	Item	Symbol	Available Dots
All mode	VSYNC	c	3 dots or less, 16 dots or more
	BLANK	d	1 dot or more

Note: In VGA mode, the polarities of HSYNC and VSYNC depend on the display resolution on CRT, but we will explain them as the active-high input in this document.

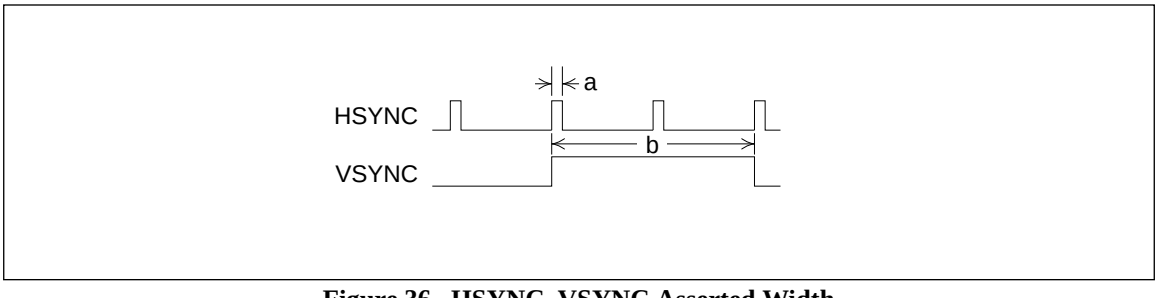


Figure 36 HSYNC, VSYNC Asserted Width

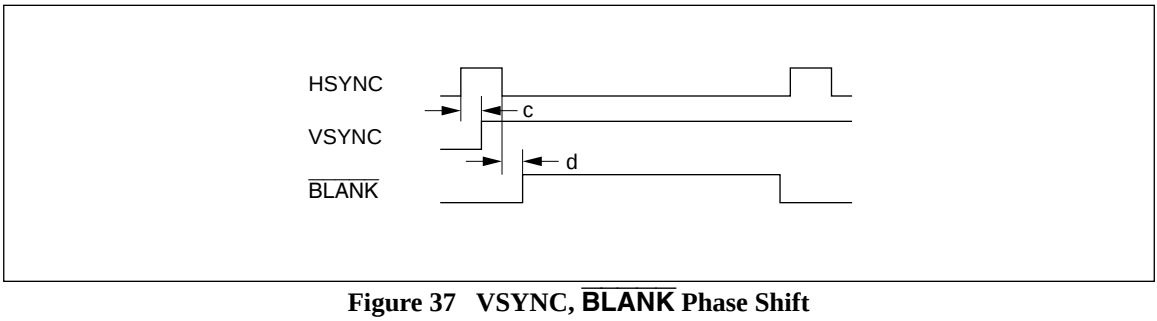


Figure 37 VSYNC, $\overline{\text{BLANK}}$ Phase Shift

Total Horizontal Dots: HD66850F needs 48 dots for the horizontal retrace period, and the HSYNC period must be 688 dots or more when 640 dots display, 768 dots or more when 720 dots display.

Horizontal Front Porch: There is a restriction about the horizontal front porch (from negated $\overline{\text{BLANK}}$ to asserted HSYNC) as the below in VGA mode. Please input them with the minimum value or more. Especially in 320 or 360 dots wide, period of the front porch is usually just 3 or 4 dots. Please delay HSYNC asserted timing, and hold the minimum value. Otherwise the first line on a panel will be incorrect.

Table 18 Total Horizontal Dots

Condition	Symbol	Minimum Dots
All mode	e	688 dots (when 640 dots display)
		768 dots (when 720 dots display)

Table 19 Horizontal Front Porch

			Dot Adjust								
Condition	Symbol	Item	–2	–1	±0	+1	+2	+3	+4	+5	+6
VGA mode	f	Horizontal 320 or 640 dots display	1 dot or more				3 dots or more				7 dots or more
		Horizontal 360 or 720 dots display	1 dot or more					5 dots or more			

Note: The BLANK 'High' width (g) must be 328 or 336 dots in 320 dots display, 376 dots in 360 dots display, 656 dots in 640 dots display, and 738 dots display in 720 dots display.

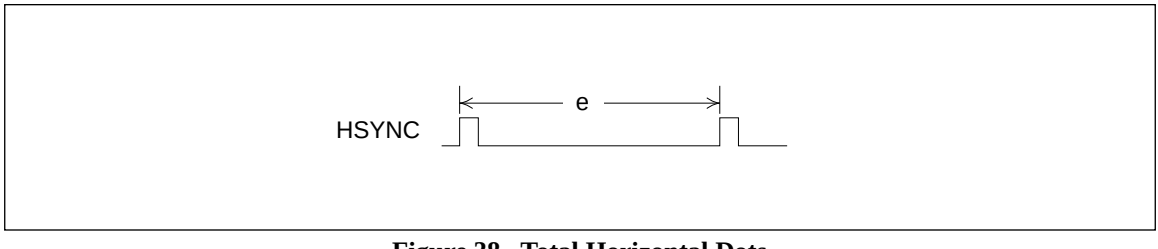


Figure 38 Total Horizontal Dots

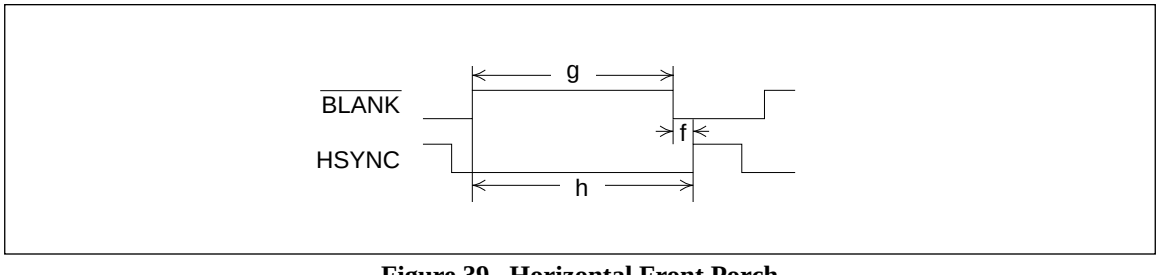


Figure 39 Horizontal Front Porch

When it displays 720 dots wide (text mode) on 640 dots panel in VGA mode, HD66850F removes 1 dot from each 9 dots. It may not display correctly according to the combination of the dot ajust and the period from negated $\overline{\text{BLANK}}$ to asserted HSYNC (h in figure 4). In this case, please change the dot adjust, or delay asserted timing of HSYNC.

This restriction causes trouble when the below equation is satisfied. When the total horizontal dot is 900 dots wide, and the period between negated $\overline{\text{BLANK}}$ to asserted HSYNC is 'h' dots,

$$4 \times [(h - 2)/4 \uparrow] = 9 \times M + A$$

($\uparrow$: revaluation, M and A: integer)

The 'A' which causes trouble depends on the dot ajust as below.

Table 20 Display Period + Horizontal Front Porch

Condition	Symbol	Item		Dot Adjust –2	–1	±0	+1	+2	+3	+4	+5	+6
VGA mode & with buffer memory mode, 720 dots display on 640 dots panel	h	Monochrome or 8/16 colors mode	743 to 746 dots	NG	ok	ok	ok	ok	NG	ok	ok	ok
			747 to 750 dots	NG	ok	ok	ok	NG	ok	ok	ok	ok
			751 to 754 dots	ok	ok	ok	ok	NG	ok	ok	ok	NG
			755 to 758 dots	ok	ok	ok	NG	ok	ok	ok	ok	NG
			759 to 762 dots	ok	ok	ok	NG	ok	ok	ok	NG	ok
			763 to 766 dots	ok	ok	NG	ok	ok	ok	ok	NG	ok
		64/512/4096 colors mode	743 to 764 dots	ok	NG	ok	ok	ok	ok	NG	ok	ok
			747 to 750 dots	ok	NG	ok	ok	ok	NG	ok	ok	ok
			751 to 754 dots	NG	ok	ok	ok	ok	NG	ok	ok	ok
			755 to 758 dots	NG	ok	ok	ok	NG	ok	ok	ok	ok
			759 to 762 dots	ok	ok	ok	ok	NG	ok	ok	ok	NG
			763 to 766 dots	ok	ok	ok	NG	ok	ok	ok	ok	NG

Note: The total horizontal dot must be 900 dots wide.

Parameter	Item	Dot Adjust –2	–1	±0	+1	+2	+3	+4	+5	+6
A	Monochrome or 8/16 colors mode	1	2	3	4	5	6	7	8	0
		6	7	8	0	1	2	3	4	5
	64/512/4096 colors mode	0	1	2	3	4	5	6	7	8
		5	6	7	8	0	1	2	3	4

Automatic Judgement of VGA Display Resolution: In VGA mode, HD66850 judges the current display resolution from the polarities of VSYNC, and HSYNC, and the width of $\overline{\text{BLANK}}$ 'H' automatically. Please input these signals as below to judge the correct resolution.

Table 21 $\overline{\text{BLANK}}$ 'High' Level Width

Condition	Symbol	VGA Mode No.	Horizontal Resolution	$\overline{\text{BLANK}}$ H Width
VGA mode	j	0/1	360 wide	378 dots
		2/3, 7	720 wide	738 dots
		4/5	320 wide	336 dots
		6, F, 10, 11, 12	640 wide	656 dots
		13 (256 col)	320 wide	328 dots

Table 22 Polarities of HSYNC and VSYNC

Condition	VGA Mode No.	Vertical Resolution	HSYNC	VSYNC
VGA mode	F, 10	350 raster high	Positive	Negative
	0/1, 2/3, 4/5, 6, 7, 13	400 raster high	Negative	Positive
	11, 12	480 raster high	Negative	Negative

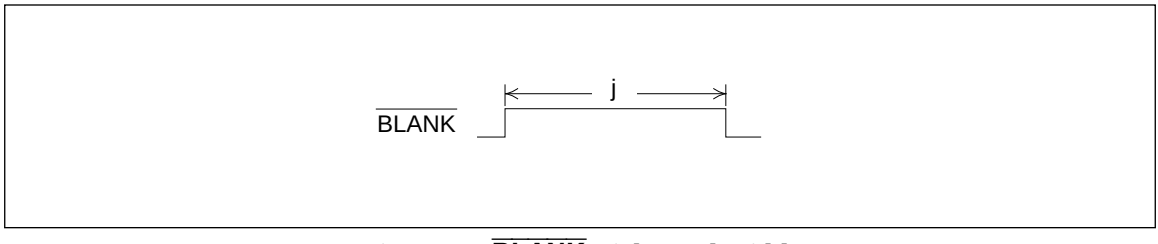


Figure 40 $\overline{\text{BLANK}}$ High Level Width

Border Area: In VGA mode, there is border area around display area. When the border and display area is scanned, $\overline{\text{BLANK}}$ is 'high' level. HD66850 internally generates the display timing which indicates just the display area from $\overline{\text{BLANK}}$ input. So, please input the $\overline{\text{BLANK}}$ with the horizontal border dot wide and vertical border high raster as below.

Table 23 Number of Horizontal Border Dot

Condition	Symbol	VGA Mode No.	Resolution	Border
VGA mode	k	0/1	360	9 dots
		2/3, 7	720	9 dots
		4/5	320	8 dots
		6, F, 10, 11, 12	640	8 dots
		13 (256 col)	320	4 dots

Table 24 Number of Vertical Border Raster

Condition	Symbol	VGA Mode No.	Resolution	Border
VGA mode	m	F, 10	350	6 rasters
		0/1, 2/3, 4/5, 6, 7, 13	400	7 rasters
		11, 12	480	8 rasters

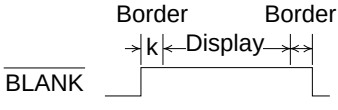


Figure 41 Number of Horizontal Border Dot

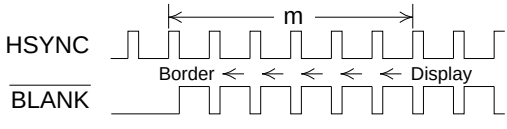


Figure 42 Number of Vertical Border Raster

When 64 k × 4 bit (256 k) or 128 k × 8 (1M) bit memory is attached for buffer memory, please satisfy the below relationship about vertical display and border raster.

$$\left[\begin{array}{l}\text{Vertical}\\ \text{display raster}\end{array}\right] + \left[\begin{array}{l}\text{Vertical border}\\ \text{raster after display}\end{array}\right] \leq \begin{array}{l}512\\ \text{raster}\end{array}$$

Usually, the vertical 480 rasters mode (VGA mode 11, 12) has 6 or 7 border rasters, so this limitation will be no problem.

Table 25 Vertical Display Raster + Vertical Border Raster After Display

Condition	Symbol	Vertical Display Raster + Vertical Border Raster after Display
VGA and with memory mode	n	512 rasters or less

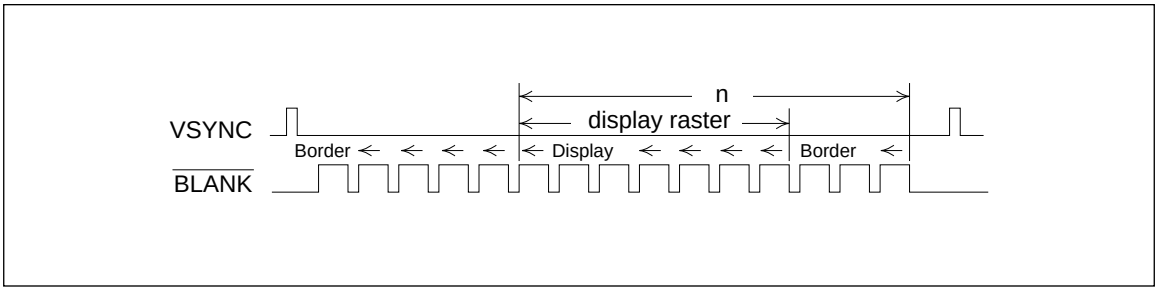


Figure 43 Vertical Display Raster

Asynchronous Mode

In asynchronous mode, the set data in the gradation palette is broken owing to the dot adjust during display. To avoid this problem, in MPU and ROM programming method, please write '1' to bit 4 (BM mode) of the border control register (R7), and all '0' to bit 3-0 (border color) of R7. The register R7 must be '10H'. In pin programming method, please adjust display timing with AJ3-AJ0 pins, and start to display just from left edge on an LCD panel without border dot, rise the $\overline{\text{BLANK}}$ input at same DOTCLK edge as change of the video data (R/G/B).

In 8/16 colors mode, this restriction is no problem in any mode because HD66850F does not access the gradation palette. In 64 / 512 / 4096 colors mode, it does not support asynchronous mode.

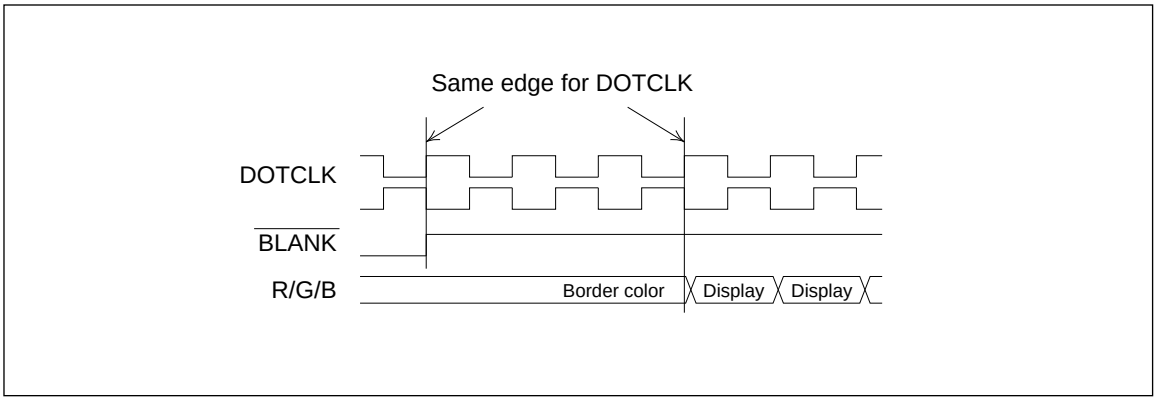


Figure 44 Countermeasure in the Pin Programming Method

Frame Period

In synchronous with-memory mode, DOTCLK and frame period for CRT are same as one for LCD. When it displays on a full screen with stretching or centering function, HD66850F needs to extend the frame period for displaying on LCD. If this frame period for LCD were longer than one for CRT, HD66850F can not work correctly.

HD66850F needs 48 dots period for the horizontal retrace, and number of the total horizontal dot for LCD is number of the horizontal display dot + 48 dots. This minimum frame period which is necessary to display on LCD is shown as below.

$$\text{Minimum frame period for LCD} = (\text{Number of horizontal display dot} + 48) \times \text{Vertical panel size [dots]}$$

The frame period for CRT must be longer than the above minimum one for LCD.

For example, when HD66850F stretchs CRT resolution with 640 × 350 dots to the LCD panel with 640 × 480 dots, the minimum frame period for LCD is (640 + 48) × 480 = 330, 240 dots.

On the other hand, when number of the total horizontal dot for CRT is 800 dots wide, 330, 240/800 = 412.8 rasters, so HD66850F needs 413 or more rasters high as the total vertical raster for CRT.

In asynchronous mode, HD66850F separates LCD clock (LDOTCK) from CRT clock (DOTCK), and the both frame period are different. So, this limitation is no problem.

LCD Alternating Signal M

When LCD alternating signal M is changed at same line in each frame, brightness of the line differs from one of another line. To avoid this problem, the signal M is ususally controlled to change at different line in each frame. But period of the signal M may synchronize with the frame period according to the total vertical raster. In this case, adjust period of the M, and don't synchronize them.

Especially, it is easy to synchronize them in VGA 720 × 400 dots mode. For example, when it displays 720 × 400 dots in synchronous with-memory mode, usaually number of the total horizontal dot for CRT is 900 dots wide, and number of the total vertical raster is 448 rasters high, so the frame period for CRT is 900 × 448 = 403,200 [dots]. On the other hand, number of the total horizontal dot for LCD is 720 + 48 = 768 dots wide, and the frame period (403,200 dots) divided by a total horizontal dot for LCD (768 dots) is 512 which is interger. So, when line number of period of the M equals to the following divisor of 512:

[1, 3, 5, 7, 15, 21, 25, 35, 75, 105, 175] (lines),

period of the M synchronizes with the frame period, and a horizontal bright line is appeared when the M is changed.

Vertical Centering

Number of vertical centering line depends on 'the value in register (R5) + 1' in non-VGA mode, or on the VSIZE pin and display resolution in VGA mode. But when '0' is written in the register (R5) and the vertical centering is enabled, HD66850F can not works correctly. Don't set '0' in the register (R5). And when number of vertical display raster is same as the vertical panel size (VSIZE), the vertical centering enable bit (bit 3 in R0) must be cleared. Especially in VGA mode, please update the enable bit according to selected VGA display mode.

When stretching function is selected, there is no restriction about setting '0' in the stretching registers (R8, R9, R10).

Table 26 Notes on VGA Mode Usage by LCD Panel Size

Horizontal Size (dots)	Vertical Size (lines)	Notes
640	—	• In VGA text modes (0/1, 2/3, 7), there is no space between characters.
720	—	• In VGA graphic modes (4/5, 6, F, 10, 11, 12, 13), horizontal centering is necessary. (Display is automatically centered horizontally in with-memory mode. See note below.)
—	400	• Data on line 401 through line 480 in VGA 640-by-480 graphic modes (11, 12) are not displayed. • Vertical centering or stretching is necessary for VGA 640-by-350 graphic modes (F, 10). (Display is automatically stretched in with-memory mode. See note below.)
—	480	• Vertical centering or stretching is necessary for VGA text modes (0/1, 2/3, 7). (Display is automatically stretched in with-memory mode. See note below.) • Vertical centering or stretching is necessary for VGA 640-by-200 or 320-by-200 graphic modes (4/5, 6, 13). (Display is automatically stretched in with-memory mode. See note below.) • Vertical centering or stretching is necessary for VGA 640-by-350 graphic modes (F, 10). (Display is automatically stretched in with-memory mode. See note below.)

Note: For without-memory mode, external circuits or BIOS tuning are required.

Table 27 Notes on Internal Register Settings

Register No.	Bits	Register or Bit Function	Notes	
			VGA	Non-VGA
R0	STE	Stretching enable	1	1
R0	CRE	Vertical centering enable	2	2
R0	CCE	Horizontal centering enable	3	4
R0	SP	Double-width display set	5	4
R0	DISPON	Display on	6	6
R1	DOTE	Dot clock phase select	4	4
R1	AJ3–AJ0	Display timing adjust	4	4
R2	DH6–DH0	Display horizontal size set	7	4
R3–R4	DV8–DV0	Display vertical size set	8	4
R5	CR7–CR0	Centering raster set	8	4
R6	CC4–CC0	Centering character set	3	4
R7	BM	Border control mode select	9	9
R7	BCI, BCR, BCG, BCB	Border color select	10	10
R8	SF3–SF0	Stretching period	8	4
R9–R10	SI15–SI0	Stretching index set	—	—
R11	PS1–PS0	Gradation display palette select	11	11
R11	PA3–PA0	Gradation display palette address set		
R12	PD5–PD0	Gradation level palette data set		
R13–R14	GC8–GC0	Gradation display clock period set	7	12

Notes:
1. Simultaneous use with vertical centering function is impossible.
2. Simultaneous use with stretching function is impossible.
3. Automatically set for a 640- or 320-dot-wide display on a 720-dot-wide LCD panel; cannot be rewritten.
4. Must be set after reset.
5. Automatically set for a middle-resolution display; cannot be rewritten.
6. Display will turn on four frames after reset. Display will not turn on during four frames after reset.
7. Automatically set according to the horizontal panel size and number of displayed horizontal dots; cannot be rewritten.
8. Automatically set according to the vertical panel size and polarity of HSYNC and VSYNC signals; cannot be rewritten.
9. Available only in with-memory mode.
10. Available only in asynchronous with-memory mode.
11. In the MPU programming method, automatically set for 16-level display after reset; can be rewritten 100 µs after reset. In ROM programming method, appropriate data must be written.
12. In with-memory mode, automatically set according to the horizontal panel size and number ofdisplayed horizontal dots; cannot be rewritten. For without-memory mode, appropriate data must be written after reset.

Table 28 Limits on Register Values

Register Function	Applied to	Limits
Horizontal display size control	R2	$4 \le Nchd \le (R2 + 1) \le 90$ (HSIZE = 1) $4 \le Nchd \le (R2 + 1) \le 80$ (HSIZE = 0)
Vertical display size control	R3, R4	$4 \le Ncvd \le (R3, R4 + 1) \le 512$
Vertical centering	R3, R4, R5	$2 \le (R5 + 1) \le 256$ $(R5 + 1) \times 2 + Ncvd = (R3, R4 + 1)$
Horizontal centering	R2, R6	$2 \le (R6 + 1) \le 32$ $(R6 + 1) \times 2 + Nchd = (R2 + 1)$
Gradation display clock period control	R13, R14	$(R13, R14 + 1) = (Ncht \times 8)/n$ (MMODE1 = 1) n: 2 for 1/2 pulse width gradation display $(R2 + 1) + 8 \le Ncht$ (NMODE1 = 0)
Miscellaneous	R2, R3, R4	$1/2f_{DOTCLK} \le \{(R + 1) + 6\} \times 8 \times (R3, R4 + 1) \times f_{FLM} \le 2f_{DOTCLK}$ (SYNC = 0)

Ncht: Total number of characters on a CRT horizontal line
(total number of dots on a CRT horizontal line × 1/8)

Nchd: Number of characters displayed on a CRT horizontal line
(number of dots displayed on a CRT horizontal line × 1/8)

Ncvd: Number of lines displayed from screen top to bottom on the CRT display

f_{LDOTCK}: LCD dot clock frequency

f_{DOTCLK}: CRT dot clock frequency

f_{FLM}: Frame frequency

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to 7.0	V
Input voltage	Vin	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded.
Normal operation should be under recommended operating conditions (V_{CC} = 5.0 ± 10%, GND = 0V, Ta = –20°C to +75°C. (If these conditions are exceeded, LSI reliability may be affected.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20 to +75°C, unless otherwise specified)

Item		Symbol	Min	Max	Unit	Test Condition
Input high-level voltage	$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	—	V	
	DOTE/$\overline{RD}$/A5, SP/$\overline{WR}$/A4		2.2	—	V	
	Other input pins*1		2.0	—	V	
Input low-level voltage		V_{IL}	—	0.8	V	
Output high-level voltage	TL interface pins*2	V_{OH}	2.4	—	V	I_{OH} = –200 µA
	CMOS interface pins*3		V_{CC} –0.8	—	V	I_{OH} = –200 µA
Output low-level voltage	TTL interface pins*2	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface pins*3		—	0.8	V	I_{OL} = 200 µA
Input leakage current		I_{TL}	–2.5	+2.5	µA	
Three-state leakage current		I_{TSL}	–10.0	10.0	µA	
Current consumption		I_{CC}	—	100	mA	Output pins open

Notes: 1. Other input pins: DOTCLK, HSYNC, VSYNC, $\overline{BLANK}$, MS0–MS15, LDOTCK, D0–D7, AJ3/$\overline{CS}$/A3, AJ2/RS/A2, AJ1/A1, AJ0/A0, R0–R3, G0–G3, B0–B3, PMODE1, PMODE0, LMODE0–LMODE4, MMODE1, MMODE0, SYNC, VMODE, VSIZE, HSIZE, TEST1, TEST0
2. TTL interface output pins: D0–D7, DOTE/$\overline{RD}$/A5, SP/$\overline{WR}$/A4, AJ3/$\overline{CS}$/A3, AJ2/RS/A2, AJ1/A1, AJ0/A0, MD0–MD15, MA0–MA7, MA8/$\overline{SOE1}$, $\overline{SOE0}$, $\overline{WE}$, DT/$\overline{OE}$, $\overline{RAS1}$, $\overline{RAS0}$, $\overline{CAS}$, $\overline{CASL}$, SC
3. CMOS interface output pins: UD0–UD7, LD0–LD7, XCL1, YCL1, CL2, FLM, M, SCLK, DISPON, DATAE

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20 to +75°C, unless otherwise specified)

Video interface

No.	Item	Symbol	Min	Max	Unit	Reference
1	DOTCLK cycle time	T_{CYCD}	31.2	62.5	ns	Figure 45
2	DOTCLK low-level pulse width	t_{WDL}	15	—	ns	
3	DOTCLK high-level pulse width	t_{WDH}	15	—	ns	
4	DOTCLK rise time	t_{Dr}	—	5	ns	
5	DOTCLK fall time	t_{Df}	—	5	ns	
6	Video data setup time	t_{VDS}	10	—	ns	
7	Video data hold time	t_{VDH}	10	—	ns	
8	$\overline{\text{BLANK}}$ setup time	t_{BLS}	10	—	ns	
9	$\overline{\text{BLANK}}$ hold time	t_{BLH}	10	—	ns	
10	$\overline{\text{BLANK}}$ low-level pulse width	t_{BLW}	—	12	µs	
11	$\overline{\text{BLANK}}$ phase shift	t_{BLPD}	2Tc	—	ns	
12	Phase shift setup time	t_{PDS}	2Tc	—	ns	
13	Phase shift hold time	t_{PDH}	2Tc	—	ns	

Tc: DOTCLK cycle time

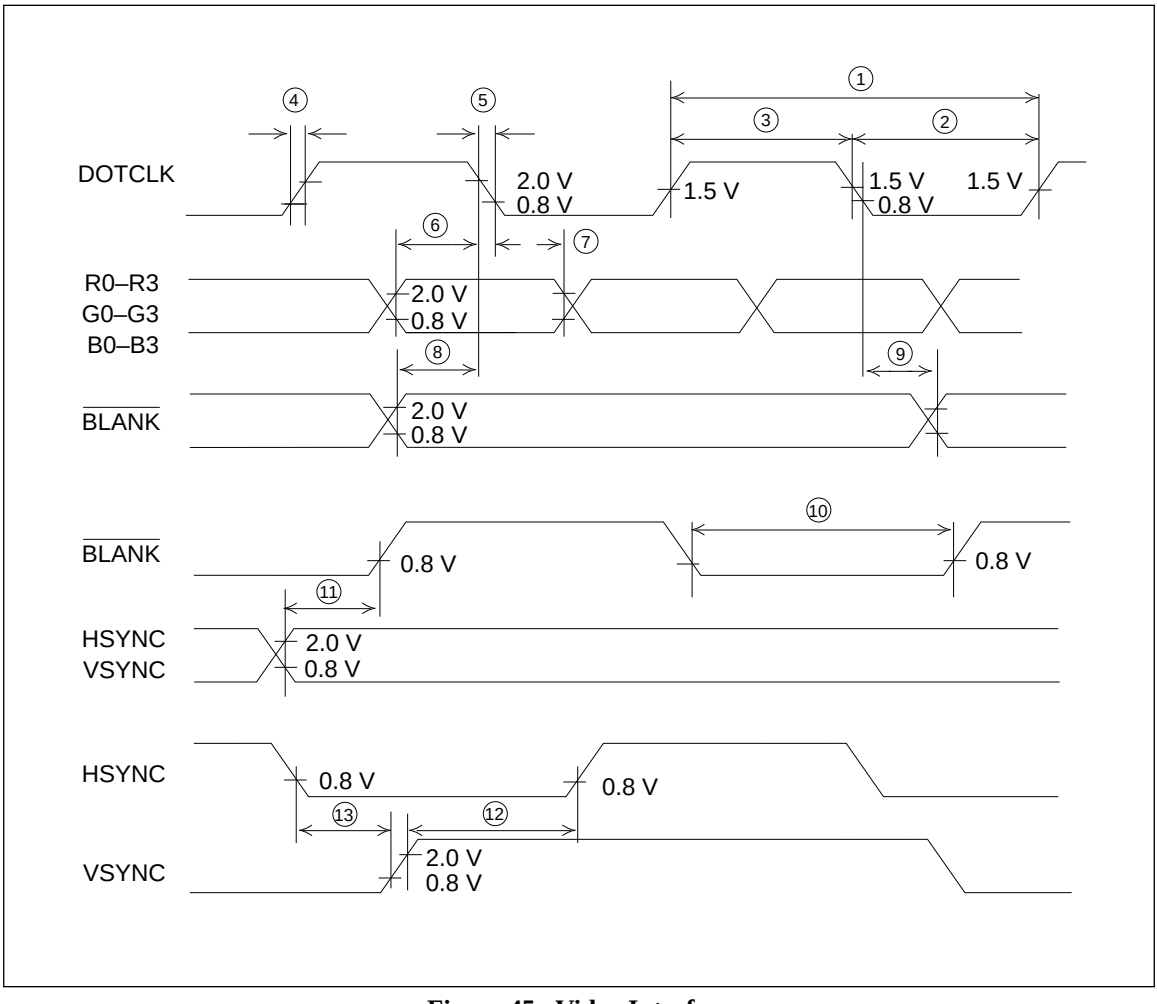


Figure 45 Video Interface

Memory Interface

No.	Item	Symbol	Min	Max	Unit	Reference
14	$\overline{RAS}$ cycle time	t_{RC}	12Tc – 10	—	ns	Figure 46
15	$\overline{RAS}$ low-level pulse width	t_{RAS}	5Tc	128Tc – 20	ns	
16	$\overline{RAS}$ high-level pulse width	t_{RP}	4Tc – 40	—	ns	
17	$\overline{CAS}$ hold time	t_{CSH}	6Tc – 50	—	ns	
18	$\overline{RAS}$, $\overline{CAS}$ delay time	t_{RCD}	3Tc – 40	—	ns	
19	$\overline{CAS}$ low-level pulse width	t_{CAS1}	3Tc – 35	—	ns	
20	$\overline{CASL}$ low-level pulse width	t_{CAS2}	2Tc – 30	—	ns	
21	$\overline{CAS}$ high-level pulse width	t_{CP1}	1Tc – 20	—	ns	
22	$\overline{CASL}$ high-level pulse width	t_{CP2}	2Tc – 20	—	ns	
23	$\overline{CAS}$ cycle time	t_{PC}	4Tc – 20	—	ns	
24	$\overline{RAS}$ hold time	t_{RSH}	4Tc – 40	—	ns	
25	Row address setup time	t_{ASR}	2Tc – 50	—	ns	
26	Row address hold time	t_{RAH}	2Tc – 30	—	ns	
27	Column address setup time	t_{ASC}	1Tc – 30	—	ns	
28	Column address hold time	t_{CAH}	2Tc – 40	—	ns	
29	$\overline{WE}$ setup time	t_{WS}	2Tc – 50	—	ns	
30	$\overline{WE}$ hold time	t_{WH}	2Tc – 40	—	ns	
31	Memory data setup time	t_{MDS}	1Tc – 30	—	ns	
32	Memory data hold time	t_{MDH}	2Tc – 35	—	ns	
33	Data transfer $\overline{DT}/\overline{OE}$ setup time	t_{DTS}	2Tc – 50	—	ns	Figure 47
34	Data transfer $\overline{DT}/\overline{OE}$ hold time	t_{DTH}	6Tc – 50	—	ns	
35	Phase shift between $\overline{CAS}$ and $\overline{DT}/\overline{OE}$	t_{CDH}	2Tc – 40	—	ns	
36	Phase shift between $\overline{CAS}$ and $\overline{DT}/\overline{OE}$	t_{DTR}	2Tc – 50	—	ns	
37	$\overline{CAS}$ setup time	t_{CSR}	2Tc – 50	—	ns	Figure 48
38	$\overline{CAS}$ hold time	t_{CHR}	6Tc – 50	—	ns	
39	Phase shift between $\overline{RAS}$ and $\overline{CAS}$	t_{RPC}	2Tc – 50	—	ns	
40	SC cycle time	t_{SCC}	$4T_L$ – 10	—	ns	Figure 49
41	SC high-level pulse width	t_{SC}	$2T_L$ – 50	—	ns	
42	SC low-level pulse width	t_{SCP}	$2T_L$ – 50	—	ns	
43	Memory data read setup time	t_{RDS}	40	—	ns	
44	Memory data read hold time	t_{RDH}	5	—	ns	
45	Phase shift between $\overline{SOE}$ and SC	t_{DSE}	20	—	ns	

T_C: DOTCLK cycle time
T_L: LDOTCK cycle time (= T_C for synchronous mode)

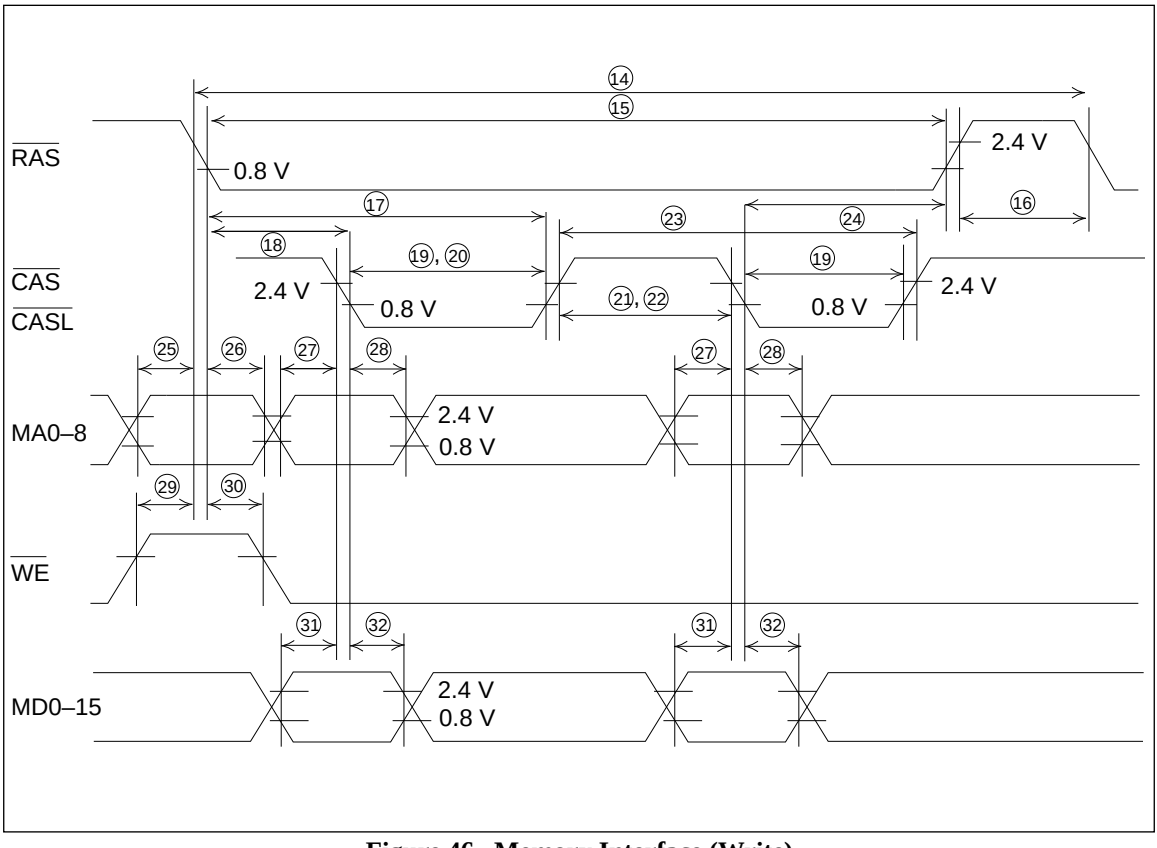


Figure 46 Memory Interface (Write)

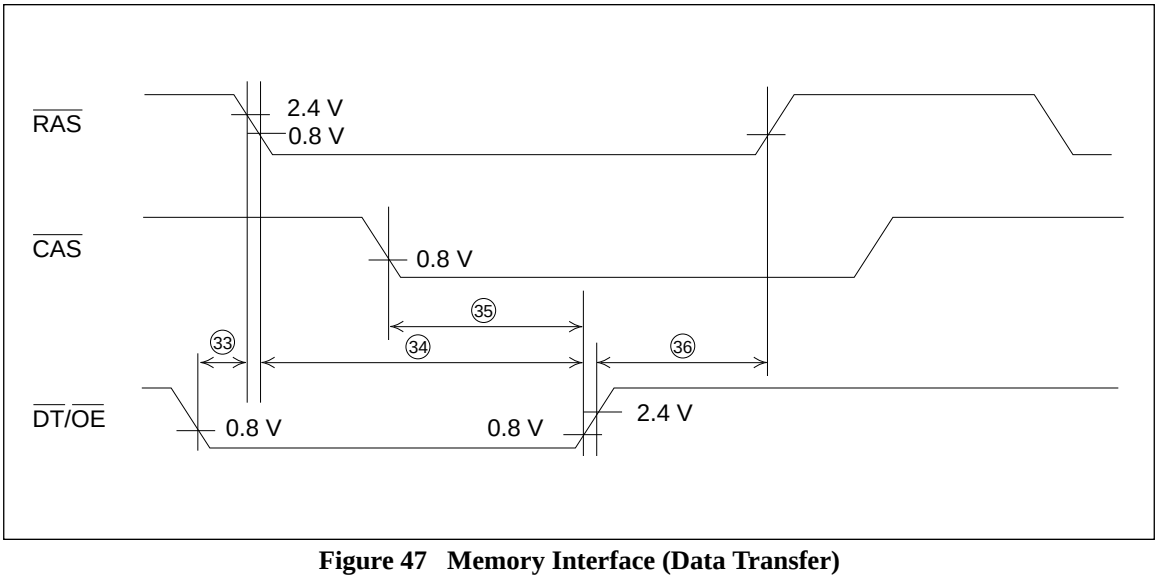


Figure 47 Memory Interface (Data Transfer)

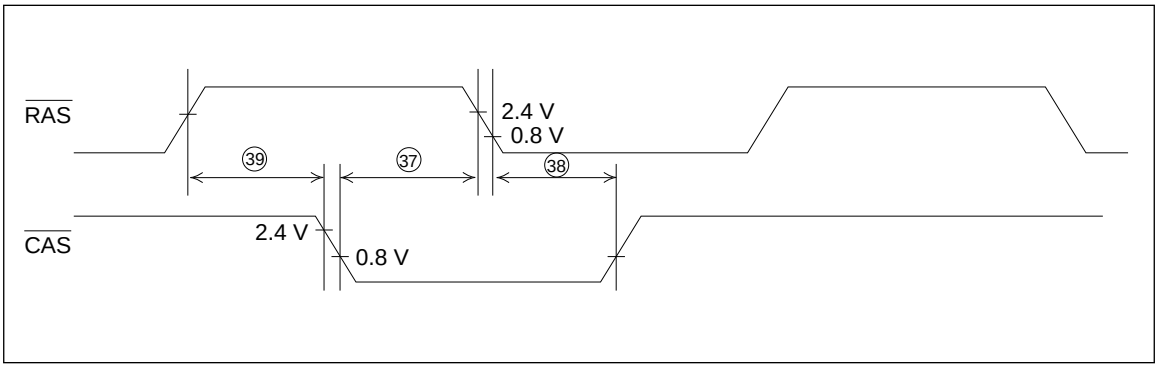


Figure 48 Memory Interface (Refresh)

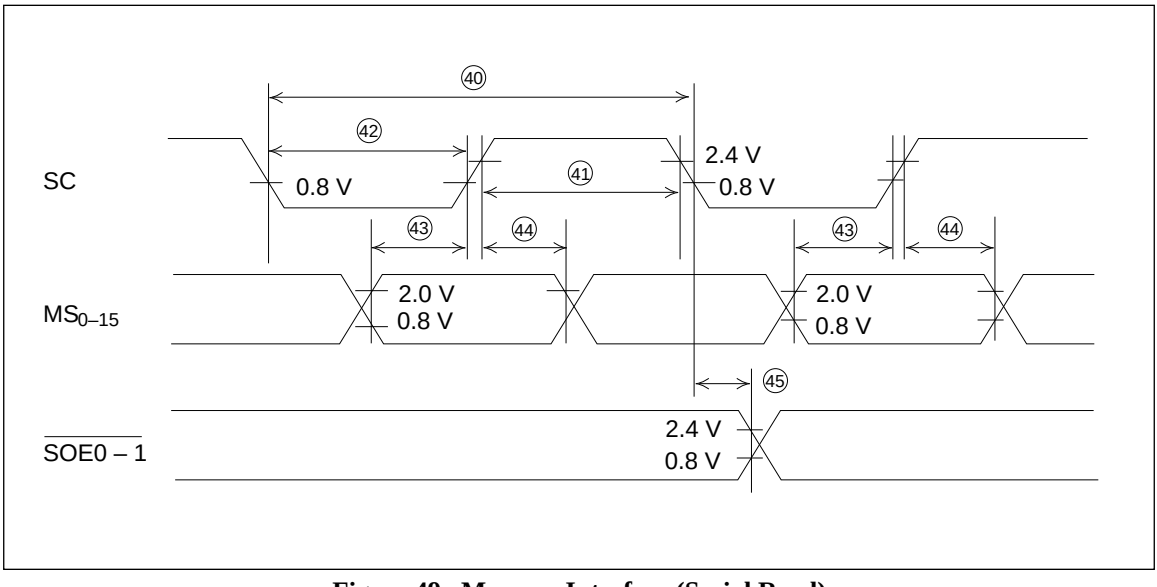


Figure 49 Memory Interface (Serial Read)

LCD Driver Interface

No.	Item	Symbol	Min	Max	Unit	Reference
46	CL2 cycle time	t_{WCL2}	$2T_L - 10$*1	—	ns	Figure 50
			$4T_L - 10$*2			
			$8T_L - 10$*3			
			$16T_L - 10$*4			
47	CL2 high-level pulse width	t_{WCL2H}	$1T_L - 40$*1	—	ns	
			$2T_L - 40$*2			
			$4T_L - 40$*3			
			$8T_L - 40$*4			
48	CL2 low-level pulse width	t_{WCL2L}	$1T_L - 40$*1	—	ns	
			$2T_L - 40$*1			
			$4T_L - 40$*2			
			$8T_L - 40$*4			
49	CL1 high-level pulse width	t_{WCL1h}	150	—	ns	
50	LCD data delay time	t_{DD}	—	30	ns	
51	CL1 setup time	t_{SCL1}	200	—	ns	
52	CL1 hold time	t_{HCL1}	200	—	ns	
53	M output delay time	t_{DM}	—	100	ns	
54	FLM setup time	t_{HF}	100	—	ns	
55	LDOTCK cycle time	t_{CYCL}	31.2	100	ns	
56	LDOTCK high-level pulse width	t_{WLH}	15	—	ns	
57	LDOTCK low-level pulse width	t_{WLL}	15	—	ns	
58	LDOTCK rise time	t_{Lr}	—	5	ns	
59	LDOTCK fall time	t_{Lf}	—	5	ns	

T_L: LDOTCK cycle time (= T_C for synchronous mode)

Notes: 1. For display modes 9, 13, 16, 19, and 20
2. For display modes 1, 5, 10, 11, 14, 15, 17, and 18
3. For display modes 2, 3, 6, 7, and 12
4. For display modes 4 and 8

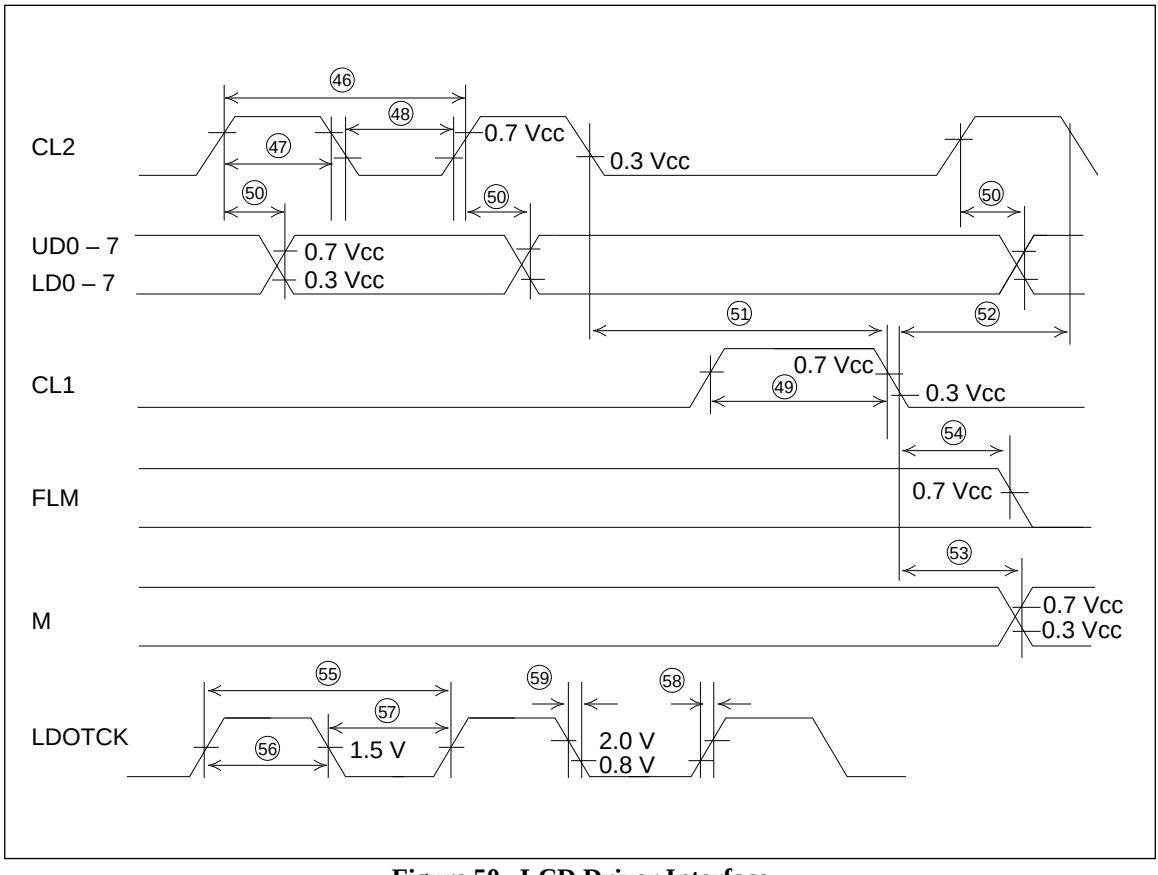


Figure 50 LCD Driver Interface

MPU Interface

No.	Item	Symbol	Min	Max	Unit	Reference
60	$\overline{RD}$ low-level pulse width	t_{WRDL}	$4T_C + 10$	—	ns	Figure 51
61	$\overline{RD}$ high-level pulse width	t_{WRDH}	$4T_C + 10$	—	ns	
62	$\overline{WR}$ low-level pulse width	t_{WWRL}	$4T_C + 10$	—	ns	
63	$\overline{WR}$ high-level pulse width	t_{WWRH}	$4T_C + 10$	—	ns	
64	$\overline{RD}$ input inhibited time	t_{RIH}	$4T_C + 10$	—	ns	
65	$\overline{WR}$ input inhibited time	t_{WIH}	$4T_C + 10$	—	ns	
66	Address setup time	t_{AS}	0	—	ns	
67	Address hold time	t_{AH}	0	—	ns	
68	Data delay time	t_{DDR}	—	100	ns	
69	Data output hold time	t_{DHR}	10	—	ns	
70	Data setup time	t_{DSW}	0	—	ns	
71	Data hold time	t_{DHW}	0	—	ns	

T_C: DOTCLK cycle time

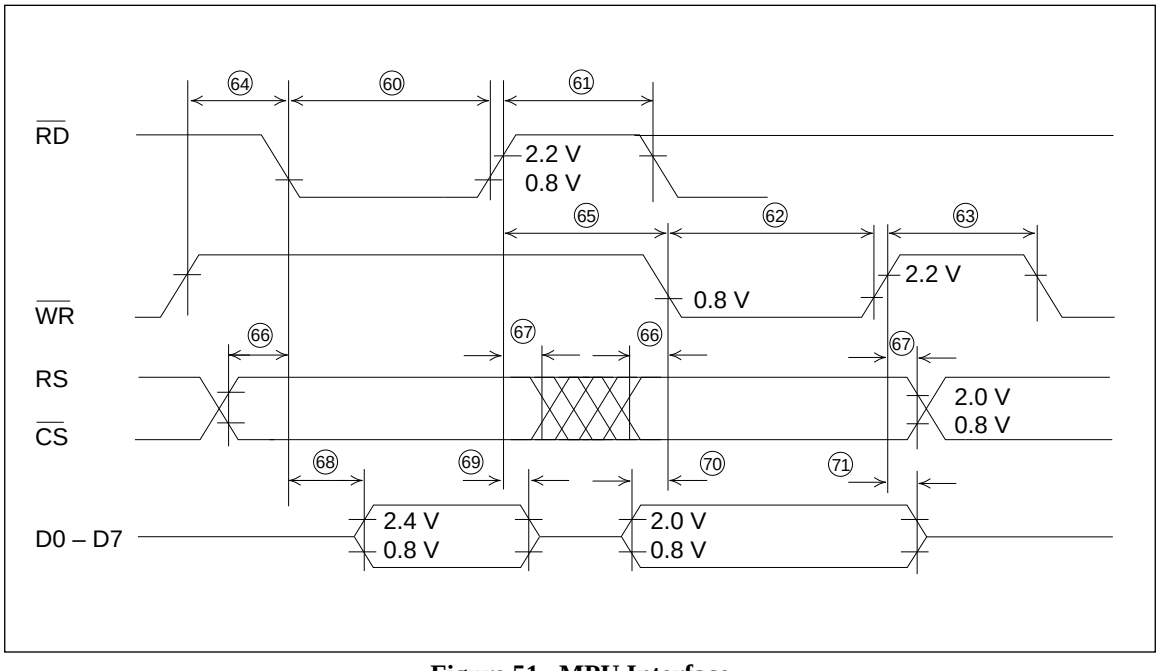


Figure 51 MPU Interface

ROM Interface

No.	Item	Symbol	Min	Max	Unit	Reference
72	ROM address cycle time	t_{CYCA}	$16T_C - 20$	—	ns	Figure 52
73	ROM data setup time	t_{DSWD}	150	—	ns	
74	ROM data hold time	t_{DHWD}	10	—	ns	

T_C: DOTCLK cycle time

RES Timing

No.	Item	Symbol	Min	Max	Unit	Reference
75	$\overline{RES}$ low-level pulse width	t_{RES}	1	—	µs	Figure 53

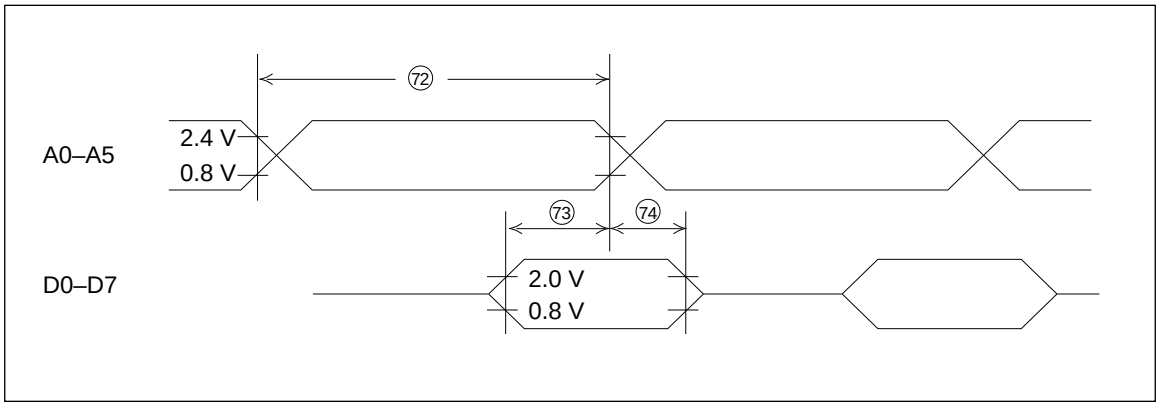


Figure 52 ROM Interface

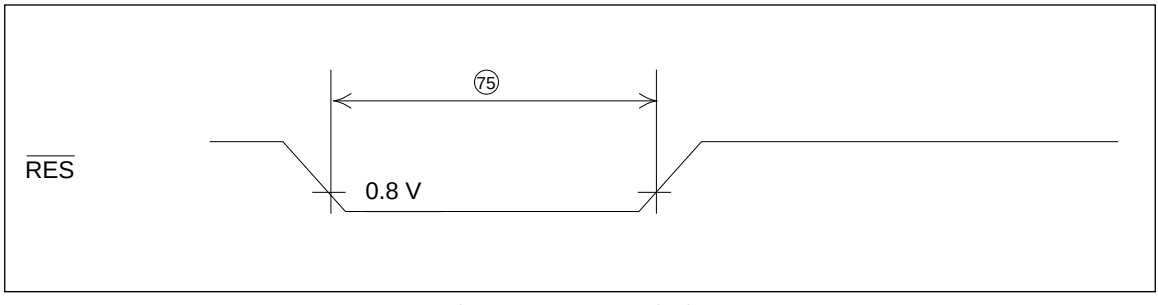
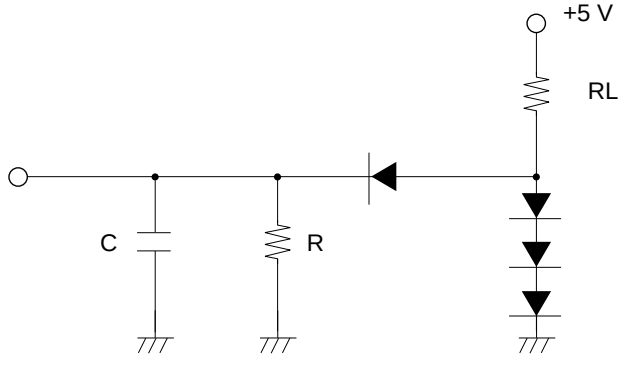


Figure 53 Reset Timing

Load Circuit

Pins	R_L	R	C	Reference
MA0 – MA7, MA8/$\overline{SOE1}$, $\overline{DT}$/$\overline{OE}$, $\overline{WE}$, $\overline{CAS}$, $\overline{CASL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{SOE0}$, MD0 – MD15, D0 – D7, A0/AJ0, A1/AJ1, A2/RS/AJ2, A3/$\overline{CS}$/AJ3, A4/$\overline{WR}$/SP, A5/$\overline{RD}$/DOTE	2.4 kΩ	11 kΩ	40 pF	Figure 54
DISPON, DATAE, SCLK, M, FLM, CL2, YCL1, XCL1, LD0 – LD7, UD0 – UD7	—	—	40 pF	Figure 55



C: 40 pF
R: 11 kΩ
RL: 2.4 kΩ

All diodes are 1S2074 (H)

Applicable pins: MA0–MA7, MA8/$\overline{SOE1}$, $\overline{DT}$/$\overline{OE}$, $\overline{WE}$, $\overline{CAS}$, $\overline{CASL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{SOE0}$, MD0–MD15, D0-D7, A0/AJ0, A1/AJ1, A2/RS/AJ2, A3/$\overline{CS}$/AJ3, A4/$\overline{WR}$/SP, A5/$\overline{RD}$/DOTE

Figure 54 TTL Load Circuit

Applicable pins: DISPON, DATAE, SCLK, M, FLM, CL2, YCL1, XCL1, LD0 – LD7, UD0 – UD7

Figure 55 Capacitive Load Circuit

HD66300T

(Horizontal Driver for TFT-Type LCD Color TV)

HITACHI

Description

The HD66300T is a horizontal driver used for TFT-type (Thin Film Transistor) LCD color TVs. Specifically, it drives the drain bus signals of a TFT-type LCD panel.

The HD66300T receives as input three video signals R, G, B, and their inverted signals $\overline{R}$, $\overline{G}$ and $\overline{B}$. Internal sample and hold circuitry then samples and holds these signals before outputting them via voltage followers to drive an TFT-type LCD panel.

The HD66300T can drive LCD panels from 480 × 240 pixels middle-resolution up to 720 × 480 pixels high-resolution. It has 120 LCD drive outputs and enables design of a compact LCD TV due to TCP (Tape Carrier Package) technology.

Features

- LCD drive outputs: 120
- Internal sample and hold circuits: 480 (4 circuits per output)
- Support of single-rate sequential drive mode and double-rate sequential drive mode
- Support of various types of color filter arrangements through an internal color sequence controller
- Vertical pixels: 240 (middle-resolution) or 480 (high-resolution)
- Horizontal pixels: 480 to 720
- Support of monodirectional connection mode and interleaved connection mode through a bidirectional shift register
- Dynamic range: 15 V_{PP}
- Power supply: +5 V and –15 V
- CMOS process

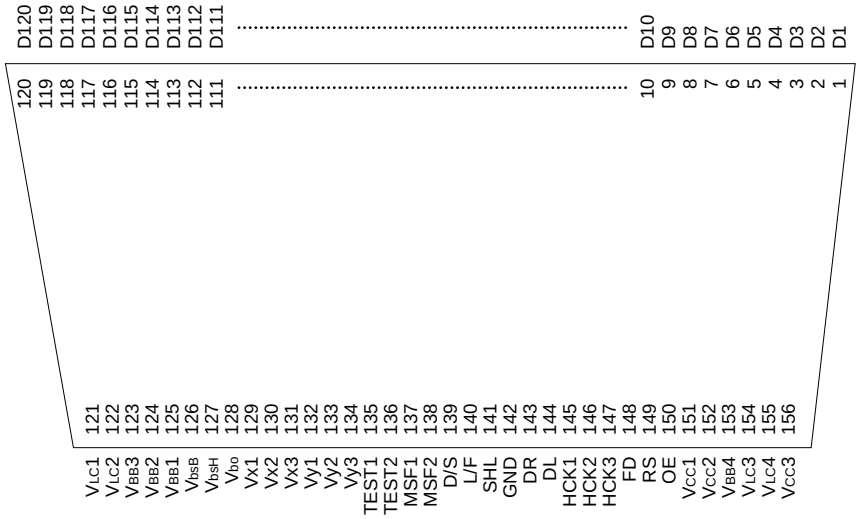
Ordering Information

Type No.	Package
HD66300T00	156-pin TCP

Note: The details of TCP pattern are shown in "The Information of TCP."

Hitachi semiconductor

Pin Arrangement



(Top view)

Note : This boes not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Connected to	Functions (Refer to)
D1 to D120	120	O	LCD panel	1
HCK1, HCK2, HCK3	3	I	Controller	2
DL, DR	2	I/O	Controller or next HD66300T	3
FD	1	I	Controller	4
RS	1	I	GND	5
OE	1	I	Controller	6
SHL	1	I	V_{CC} or GND	7
D/S	1	I	V_{CC} or GND	8
L/F	1	I	V_{CC} or GND	9
MSF1, MSF2	2	I	V_{CC} or GND	10
TEST1, TEST2	2	I	GND	11
Vx1, Vx2, Vx3, Vy1, Vy2, Vy3	6	I	Inverter	12
V_{bo}	1	I	Power source	13
V_{bsB}, V_{bsH}	2	I	Power source	14
$V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$	4	—	Power source	15
$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	3	—	Power source	16
GND	1	—	Power source	17
$V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$	4	—	Power source	18

Pin Functions

1. D1 to D120: These pins output LCD drive signals.

2. HCK1, HCK2, HCK3: These pins input three-phase clock pulses, which determine the signal sampling timing for sample and hold circuits.

3. DL, DR: These pins input or output data into or from the internal bidirectional shift register. The state of pin SHL determines whether these pins input or output data.

SHL	DL	DR
V_{CC}	Output	Input
GND	Input	Output

4. FD: This pin inputs the field determination signal, which allows the sample and hold circuitry and the shift matrix circuit to operate synchronously with TV signals, at its rising and falling edge.

FD = high: First field
FD = low: Second field

When a non-interlace signal is applied, it must be inverted every field.

When an interlace signal is applied in double-rate sequential drive mode with per-line inversion (mode 1, 2, 3), the signal must be set high in both fields. The signal must be set low, however, in each field's horizontal retrace period.

5. RS: This pin inputs a test signal and should be connected to pin GND.

6. OE: This pin inputs the signal which controls the controller of the shift matrix circuit; it changes the selection of a sample and hold circuit and the shift matrix (combination of color data), at its rising edge. It also switches the bias current of the output buffer, as shown in the following table.

OE	Bias Current of Output Buffer
High	Large current (determined by VbsB)
Low	Small current (determined by VbsH)

7. SHL: This pin selects the shift direction of the shift register.

SHL	Shift Direction
High	DL ← DR
Low	DL → DR

8. D/S: This pin selects the LCD drive mode.

D/S	Mode
High	Double-rate sequential drive mode
Low	Single-rate sequential drive mode

9. L/F: This pin selects the inversion mode of LCD drive signals.

L/F	Mode
High	Per-line inversion mode
Low	Per-field inversion mode

10. MSF1, MSF2: These pins select the function of the shift matrix circuit; they should be set according to both the type of color filter arrangement on a TFT-type LCD panel and the drive mode.

Filter Arrangement	Drive Mode	MSF1	MSF2
Diagonal mosaic pattern	Single-rate	GND	V_{CC}/GND*
	Double-rate	GND	V_{CC}/GND*
Vertical stripe pattern	Single-rate	V_{CC}	V_{CC}
	Double-rate	V_{CC}	V_{CC}
Unicolor triangular pattern	Single-rate	V_{CC}	V_{CC}
	Double-rate	V_{CC}	GND
Bicolor triangular pattern	Single-rate	V_{CC}	GND
	Double-rate	V_{CC}	GND

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

Note: * Refer to table 2 and timing charts of each mode.

11. TEST1, TEST2: These pins input test signals and should be connected to pin GND.

12. Vx1, Vx2, Vx3, Vy1, Vy2, Vy3: Video signals are applied to these pins; positive video signals are connected to pins Vxi and negative video signals to pins Vyi.

13. V_{bo}: Bias voltage is applied to this pin for the differential amplifier in the sample and hold circuitry.

14. V_{bsB}, V_{bsH}: Bias voltage is applied to this pin for the two power sources of the output buffer.

VbsB: The voltage for driving a capacitive load
VbsH: The voltage for holding the output voltage

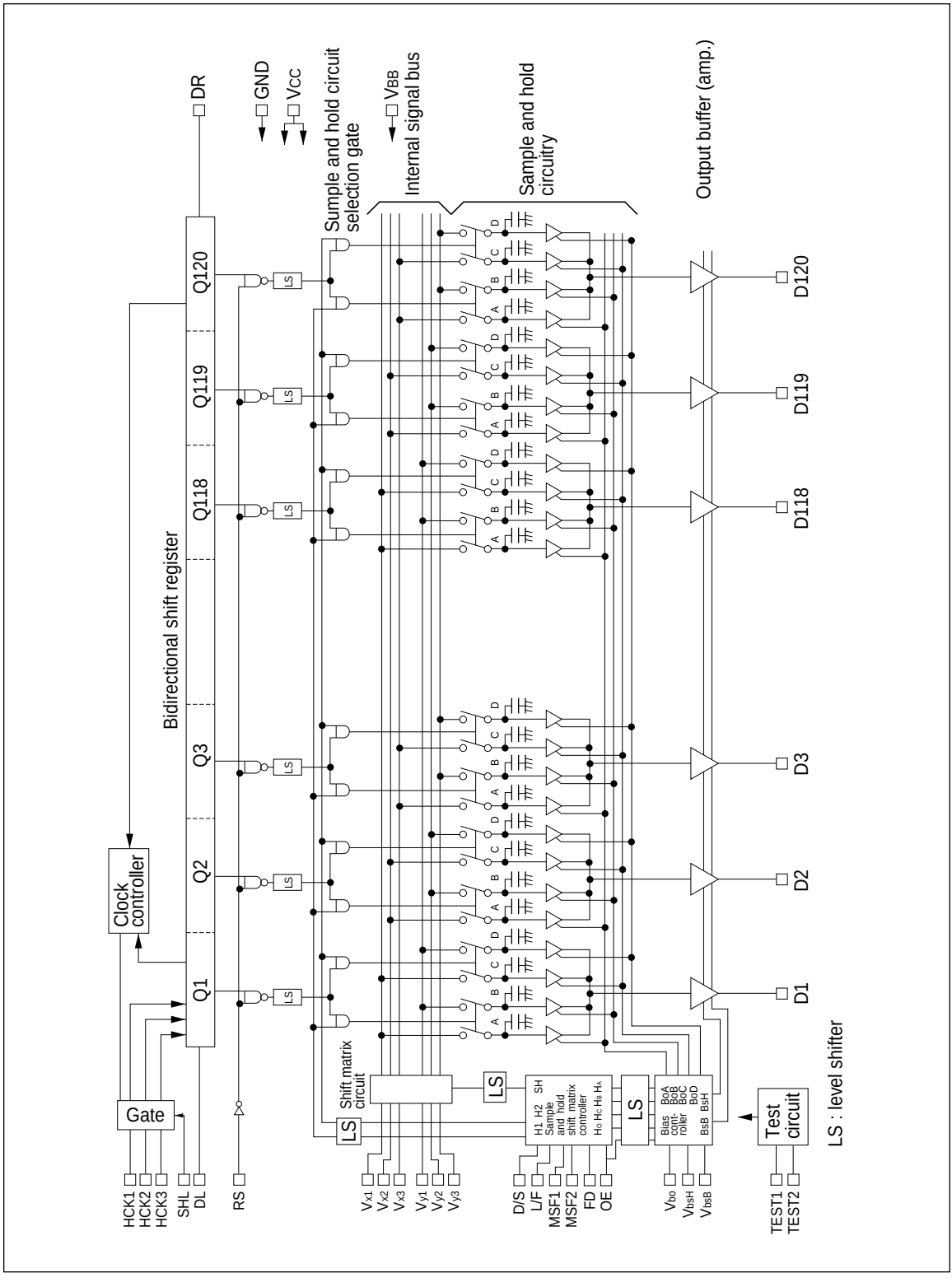
15. $V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$: +5 V LCD drive voltage is applied to these pins.

16. $V_{CC}1$, $V_{CC}2$, $V_{CC}3$: +5 V is applied to these pins for the logic and the analog units.

17. GND: 0 V is applied to this pin for the logic unit.

18. $V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$: –15 V is applied to these pins for the LCD drive unit.

Internal Block Diagram



Block Functions

Shift Register: The shift register generates the sampling timing for video signals. It is driven by three-phase clocks HCK1, HCK2, and HCK3, whose phases are different from each other by 120°; each clock determines the sampling timing for one color signal so that three clocks support the three color signals R, G, and B. The shift direction of this register can be changed.

Level Shifter: The level shifter changes 5-V signals into 20-V signals.

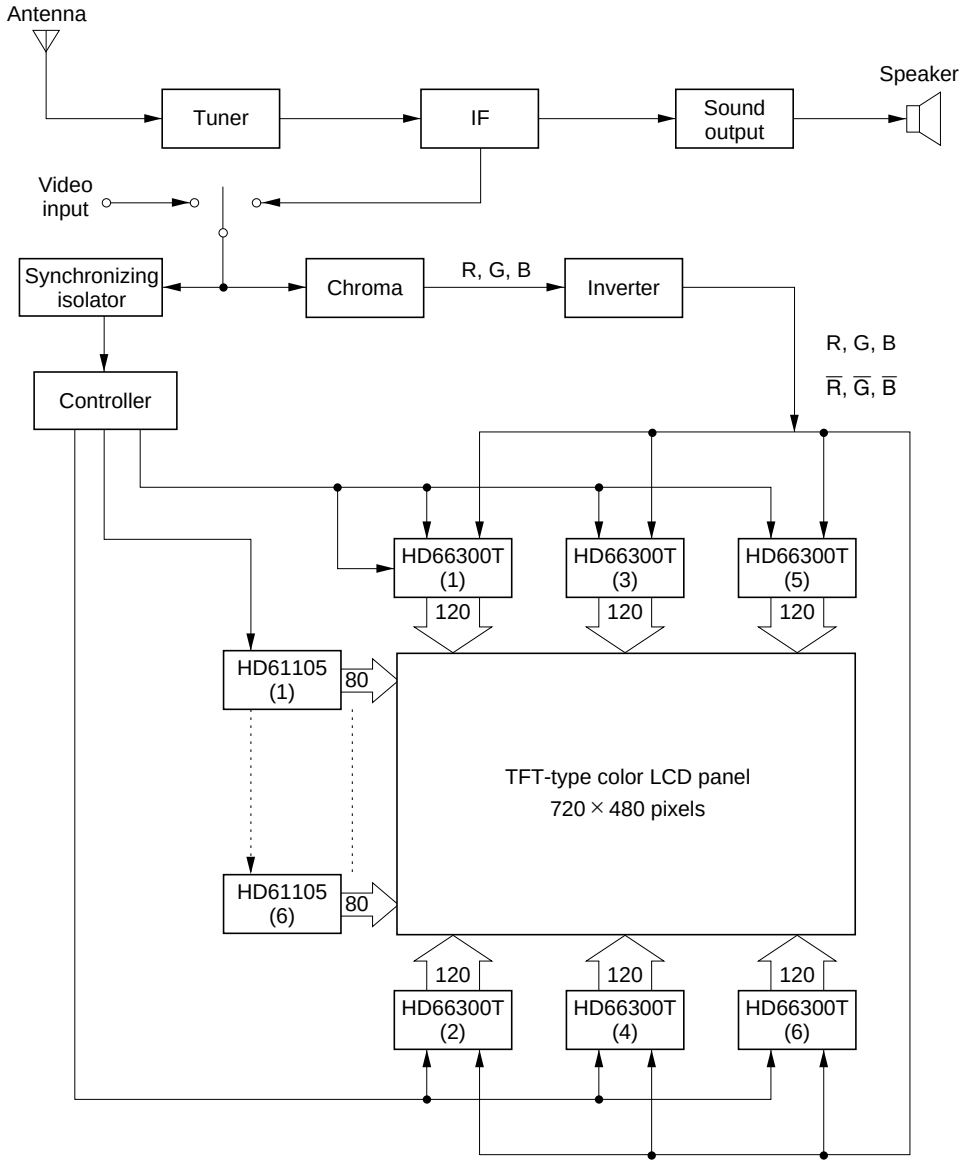
Sample and Hold Circuitry: In double-rate sequential drive mode, two sample and hold circuits are selected to sample video signals during one horizontal scanning period out of the four circuits attached to one LCD drive signal. One of the two selected circuits is read out in the first half of the following horizontal scanning period, and the other selected circuit is read out in the second half. While the two circuits are being read out, the other two circuits sample signals and are alternately read out in the same procedure mentioned above.

In single-rate sequential drive mode, one sample and hold circuit samples a signal during one horizontal scanning period, and is read out in the following horizontal scanning period. While it is being read out, one circuit out of the other three samples a signal.

Shift Matrix Circuit: The shift matrix circuit, a color sequence controller, changes over the sampled video signal every horizontal scanning period.

Output Buffer: The output buffer consists of a source follower circuit and can change the through-rate of an output signal by changing the external bias voltage.

System Block Configuration Example



Example of HD66300T Connection to LCD Panel

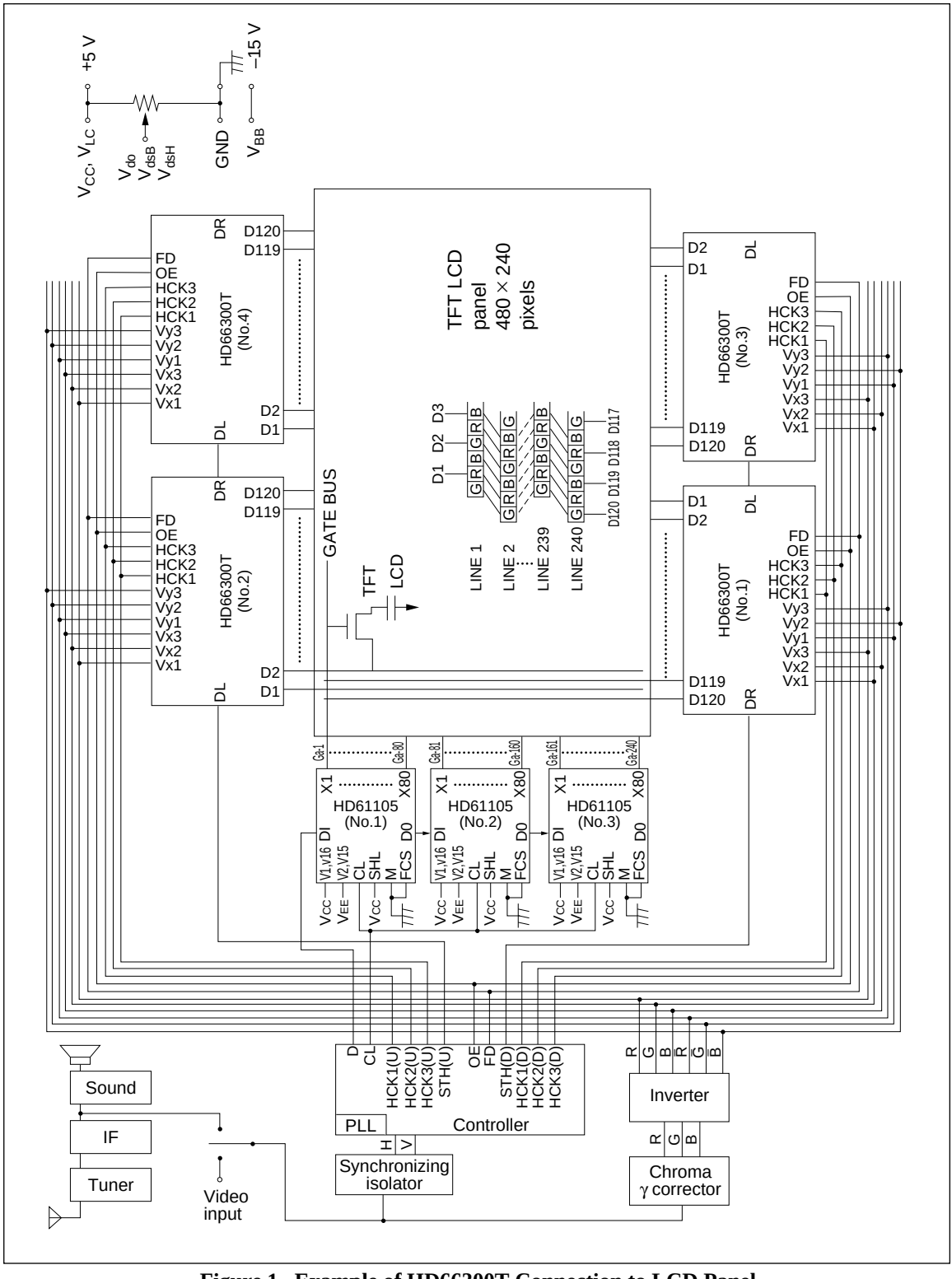
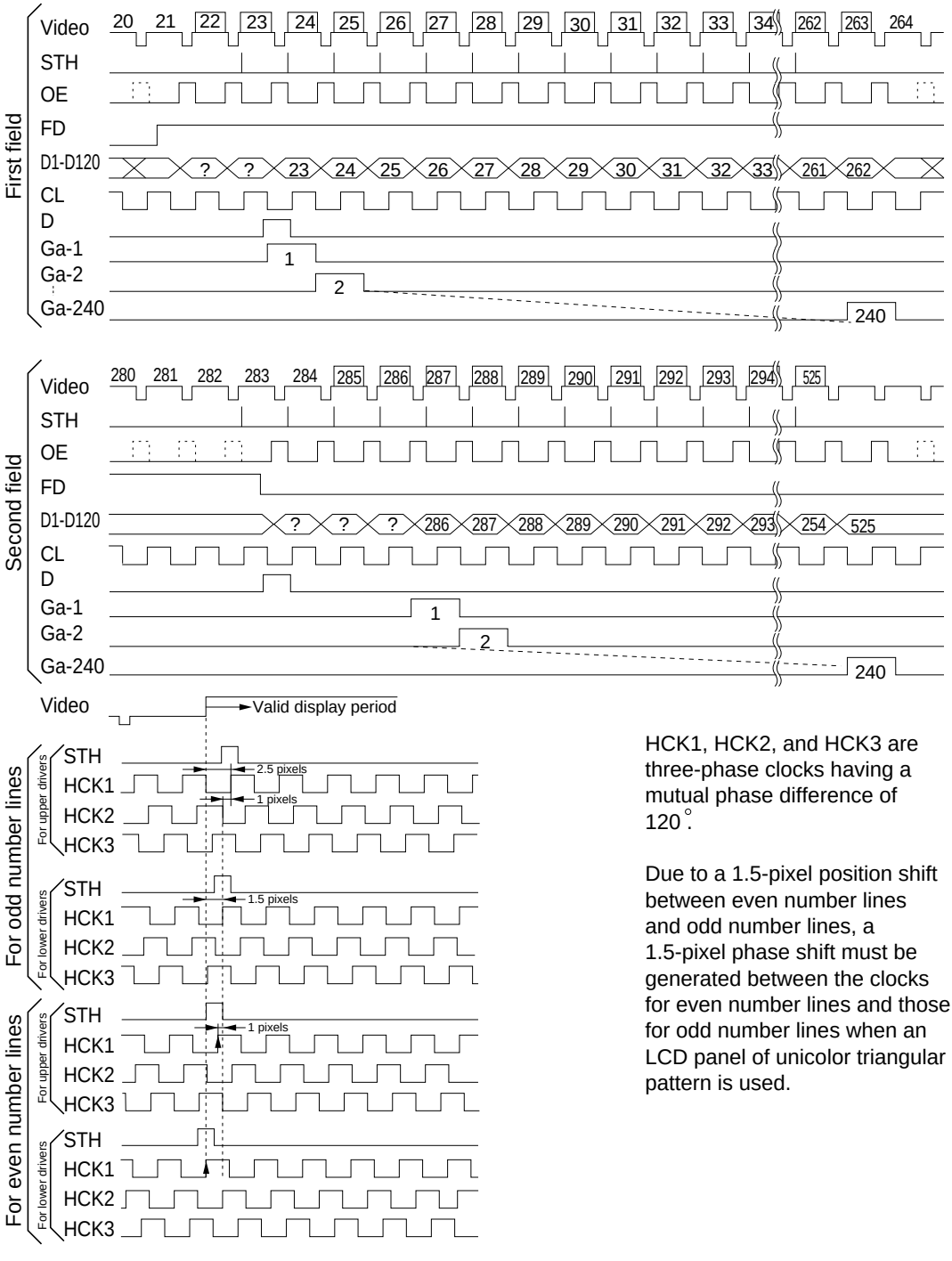


Figure 1 Example of HD66300T Connection to LCD Panel



HCK1, HCK2, and HCK3 are three-phase clocks having a mutual phase difference of 120°.

Due to a 1.5-pixel position shift between even number lines and odd number lines, a 1.5-pixel phase shift must be generated between the clocks for even number lines and those for odd number lines when an LCD panel of unicolor triangular pattern is used.

Figure 2 Timing Chart

Functional Description

Screen Size

Number of horizontal pixels:

- 120, 240, 360, 600, and 720 in monodirectional connection mode
- 240, 480, and 720 in bidirectional connection mode

Number of vertical pixels:

- 240 in single-rate sequential drive mode
- 480 in double-rate sequential drive mode

Single-Rate Sequential Drive Mode and Double-Rate Sequential Drive Mode

Single-Rate Sequential Drive Mode: A typical TV signal* has 525 scanning lines, 480 of which are part of the valid display period. In interlace scanning mode, 480 scanning lines are equally divided into a first field and a second field.

In single-rate sequential drive mode, a 240-pixel-high LCD panel is used. 240 scanning lines of the first and second fields of the TV signal are respectively assigned to the 240 lines of the LCD panel.

One line of an LCD panel is driven every horizontal scanning period in this mode.

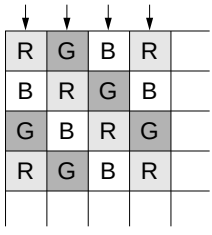
Double-Rate Sequential Drive Mode: To obtain a high-resolution display, a 480-pixel-high LCD panel is used. If 480 scanning lines are respectively assigned to the 480 lines of the LCD panel, the LCD alternating frequency becomes 15 Hz, which causes flickering and degrades display quality. To avoid this problem, the following method is employed. In the first field, the first scanning line is assigned to the first and second lines of the LCD panel, the second scanning line is assigned to the third and fourth lines, and so on. In the second field, the first scanning line is assigned to the second and third lines, the second scanning line is assigned to the fourth and fifth lines, and so on.

Two lines of an LCD panel are driven every horizontal scanning period in this mode.

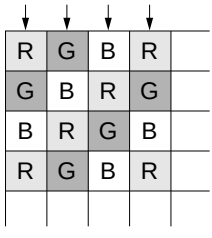
Note: * Refer to the index for the further information of NTSC TV system signals and LCD.

Supportable Types of Color Filter Arrangements

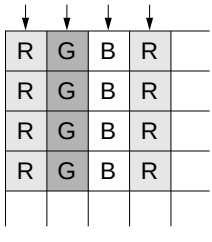
The order and timing for the HD66300T to output color signals depend on the color filter arrangement on a TFT-type LCD panel. The HD66300T can support TFT-type LCD panels having the following color filter arrangements by specifying the operation of the internal color sequence controller and by changing the external signals to be supplied.



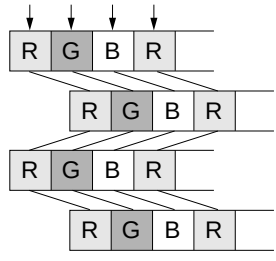
(a) Diagonal from top-left to bottom-right mosaic pattern



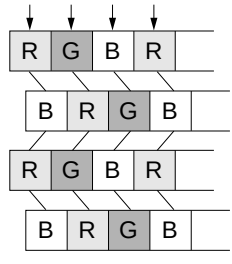
(b) Diagonal from top-left to bottom-left mosaic pattern



(c) Vertical stripe pattern



(d) Unicolor triangular pattern



(e) Bicolor triangular pattern

Figure 3 Supportable Types of Color Filter Arrangements

Mode Setting Pins

Mode setting pins MSF1, MSF2, and D/S must be set according to both the type of color filter arrangement on the TFT-type LCD panel and the drive mode (single-rate sequential drive mode or double-rate sequential drive mode). These pins activate the internal color sequence controller, which changes the sequence of color video signals corresponding to each sample and hold circuit and allows the LSI to output color data in the right order for the LCD panel being used.

Per-Field Inversion and Per-Line Inversion

The inversion mode of LCD drive signals can be selected by pin L/F.

Per-Field Inversion (Available with L/F = Low)

In a certain field, all LCD drive signals have one polarity and in the following field, they all have the inverted polarity.

Per-Line Inversion (Available with L/F = High)

In a certain field, all LCD drive signals have positive polarity in odd number lines and negative polarity in even number lines, while in the following field, the situation is reversed, that is, negative polarity in odd number lines and positive polarity in even number lines.

Table 1 Mode Setting Pins

Filter Arrangement	Drive Mode	D/S	MSF1	MSF2	Referential Timing Charts
Diagonal mosaic pattern	Single-rate	GND	GND	V_{CC}, GND	MODES 15, 16, 18, and 19
	Double-rate	V_{CC}	GND	V_{CC}, GND	MODES 1, 2, 5, 6, 8, 9, 12, and 13
Vertical stripe pattern	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
	Double-rate	V_{CC}	V_{CC}	V_{CC}	MODES 3, 7, 10, and 14
Unicolor triangular pattern	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11
Bicolor triangular pattern	Single-rate	GND	V_{CC}	GND	MODE 17
	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

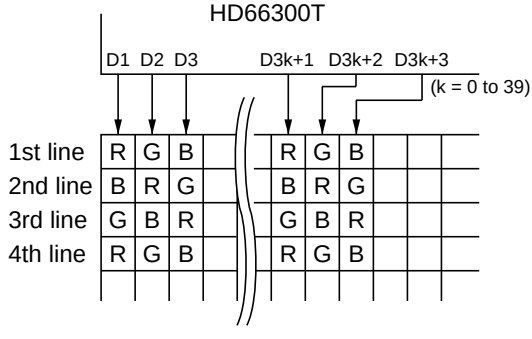
Interface

Video Signals Connection

Video signals must be connected to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3; in principle, positive video signals R, G, and B signals must be input to pins Vx1, Vx2, and Vx3, and negative video signals $\overline{R}$, $\overline{G}$, and $\overline{B}$ to pins Vy1, Vy2, and Vy3. For actual connection between an LCD panel and the LCD drive signal output pins, refer to the following example.

In the Case of Diagonal from Top-Left to Bottom-Right Mosaic Pattern

This example describes the case in which an LCD panel having a diagonal from top-left to bottom-right mosaic pattern is driven in double-rate sequential drive mode and monodirectional connection mode.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R → B → G → R →
D2 (= D3k + 2)	G → R → B → G →
D3 (= D3k + 3)	B → G → R → B →

The Signal Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	Vx1 → Vx3 → Vx2 → Vx1 →
D2 (= D3k + 2)	Vx2 → Vx1 → Vx3 → Vx2 →
D3 (= D3k + 3)	Vx3 → Vx2 → Vx1 → Vx3 →

(Refer to MODE 5)

The Connection of Signals

Signal	Color
Vx1	R
Vx2	G
Vx3	B
Vy1	$\overline{R}$
Vy2	$\overline{G}$
Vy3	$\overline{B}$

In the Case of Diagonal from Top-Right to Bottom-Left Mosaic Pattern, Vertical Stripe Pattern

The same procedure for video signal connection applies to the case in which a TFT-type LCD panel having a diagonal from top-right to bottom-left mosaic pattern or a vertical stripe pattern is used, as well as to the cases where a panel of any pattern is used through the bidirectional connection mode.

Triangular Pattern, Single-Rate Sequential Drive Mode

The following procedures are required when a panel of unicolor or bicolor triangular pattern is used:

1. Unicolor Triangular Pattern, Single-Rate Sequential Drive Mode

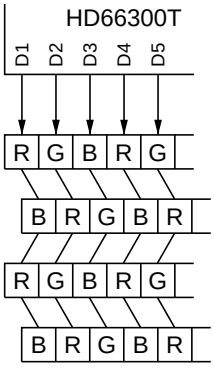
   The clock phase must be changed every line because of the 1.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)

   The connection of signals here is the same as that described above.

2. Bicolor Triangular Pattern, Single-Rate Sequential Drive Mode

   The clock phase must be changed every line because of the 0.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)

   The connection of video signals in the second field must be changed from that in the first field. See the following tables.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R → B → R → B →
D2 (= D3k + 2)	G → R → G → R →
D3 (= D3k + 3)	B → G → B → G →

The Signal Sequence for Each Output Pin

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (= D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (= D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to Mode 17)

The Connection of Signal in Each Field

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	R	$\overline{B}$	R	B
Vx2	G	$\overline{R}$	G	R
Vx3	B	$\overline{G}$	B	G
Vy1	B	$\overline{R}$	$\overline{B}$	$\overline{R}$
Vy2	R	$\overline{G}$	$\overline{R}$	$\overline{G}$
Vy3	G	$\overline{B}$	$\overline{G}$	$\overline{B}$

Triangular Pattern, Double-Rate Sequential Drive Mode

Changing the phase of the sampling clocks is sufficient when the panel is driven in single-rate sequential drive mode. However, when the panel is driven in double-rate sequential drive mode, the above countermeasure does not work, since the display data for two lines is sampled at one time here. Consequently, delaying the input video signal for a time period corresponding to the shift between pixels is required.

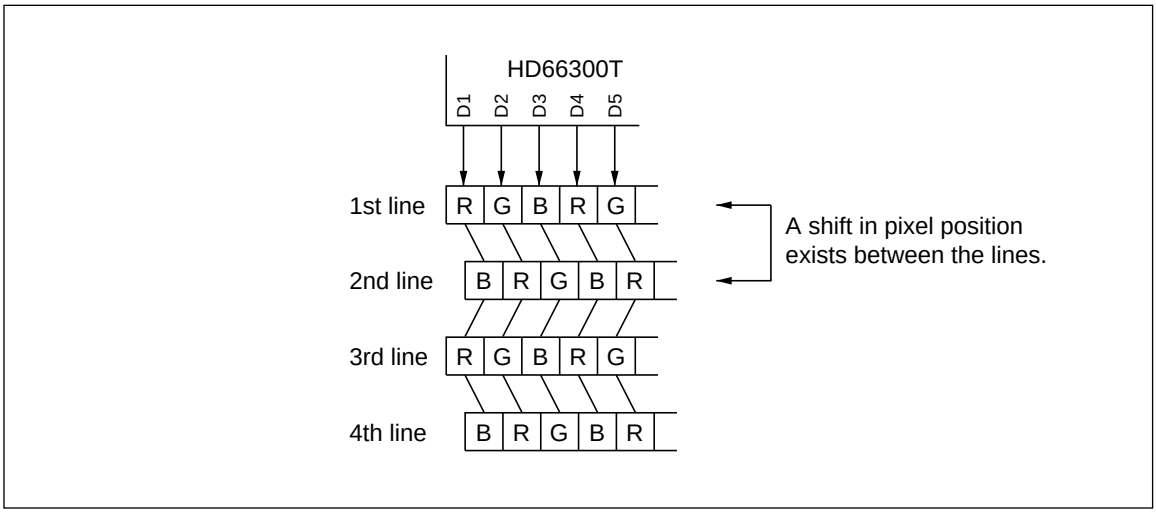


Figure 4 Pixel Position Shift (Triangular Pattern, Double-Rate Sequential Drive Mode)

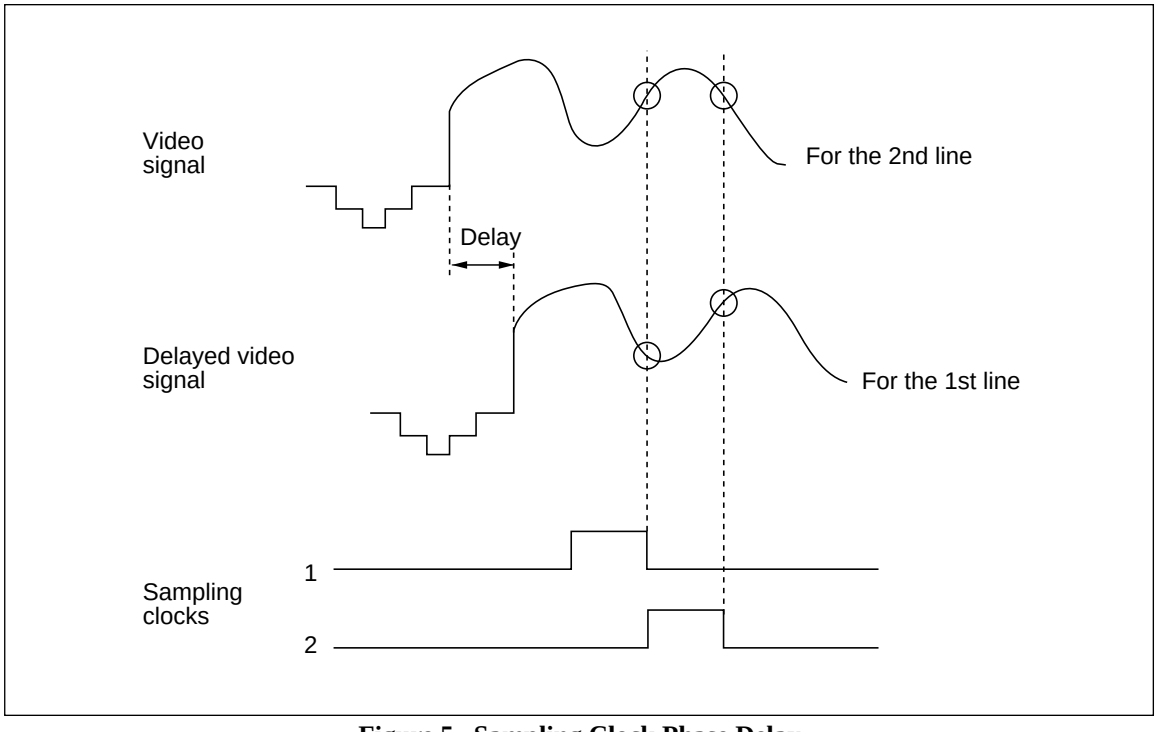
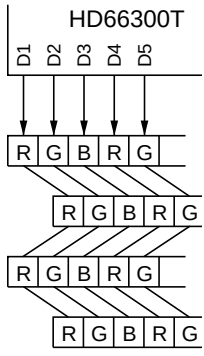


Figure 5 Sampling Clock Phase Delay

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R → R → R → R →
D2 (= D3k + 2)	G → G → G → G →
D3 (= D3k + 3)	B → B → B → B →

The Signal Sequence for Each Output Pin (In Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (= D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (= D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In Non-Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

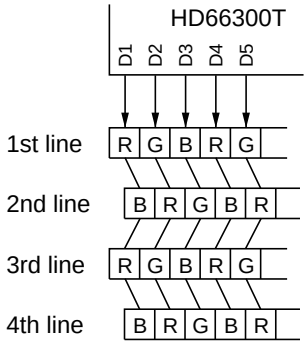
The Connection of Signals in Each Field (In Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	$\overline{R}$	Delayed R	R
Vx2	Delayed G	$\overline{G}$	Delayed G	G
Vx3	Delayed B	$\overline{B}$	Delayed B	B
Vy1	R	Delayed $\overline{R}$	$\overline{R}$	Delayed $\overline{R}$
Vy2	G	Delayed $\overline{G}$	$\overline{G}$	Delayed $\overline{G}$
Vy3	B	Delayed $\overline{B}$	$\overline{B}$	Delayed $\overline{B}$

The Connection of Signals in Each Field (In Non-Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	R	$\overline{R}$	$\overline{R}$	R
Vy2	G	$\overline{G}$	$\overline{G}$	G
Vy3	B	$\overline{B}$	$\overline{B}$	B

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R →R →R →R →
D2 (= D3k + 2)	G→R →G →R →
D3 (= D3k + 3)	B →G →B →G →

The Signal Sequence for Each Output Pin (In Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (= D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (= D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In Non-Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

The Connection of Signals in Each Field (in Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	$\overline{B}$	Delayed R	B
Vx2	Delayed G	$\overline{R}$	Delayed G	R
Vx3	Delayed B	$\overline{G}$	Delayed B	G
Vy1	B	Delayed $\overline{R}$	$\overline{B}$	Delayed $\overline{R}$
Vy2	R	Delayed $\overline{G}$	$\overline{R}$	Delayed $\overline{G}$
Vy3	G	Delayed $\overline{B}$	$\overline{G}$	Delayed $\overline{B}$

The Connection of Signals in Each Field (in Non-Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	B	$\overline{B}$	$\overline{B}$	B
Vy2	R	$\overline{R}$	$\overline{R}$	R
Vy3	G	$\overline{G}$	$\overline{G}$	G

Connection to LCD Panels

There are two modes of connecting HD66300T chips to an LCD panel:

1) monodirectional connection mode
2) bidirectional connection mode

In the former mode, the HD66300Ts are set on either the upper side or lower side of the panel, while in the latter mode, the HD66300Ts are set on both sides and the upper drivers and the lower drivers are alternately connected to each pixel-column.

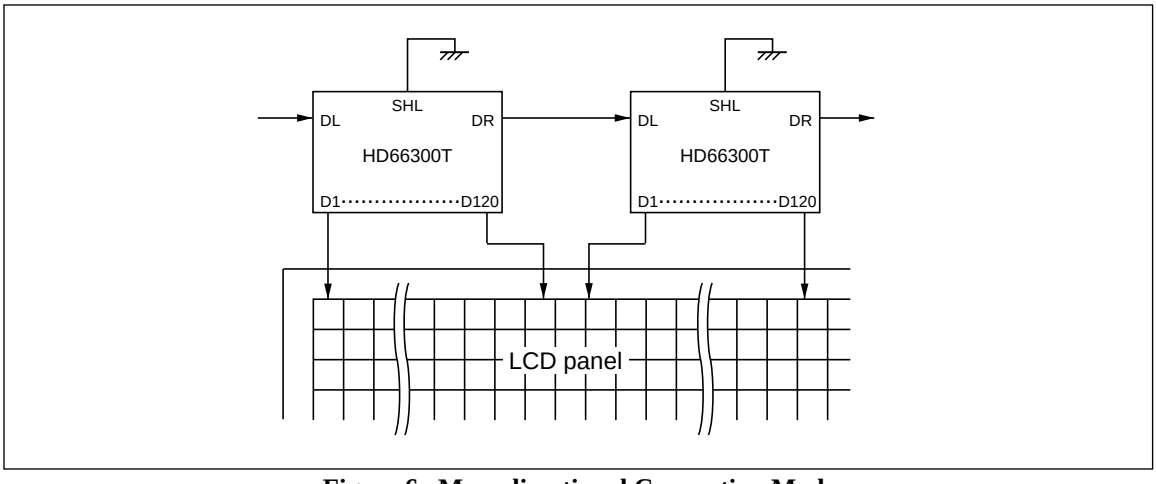


Figure 6 Monodirectional Connection Mode

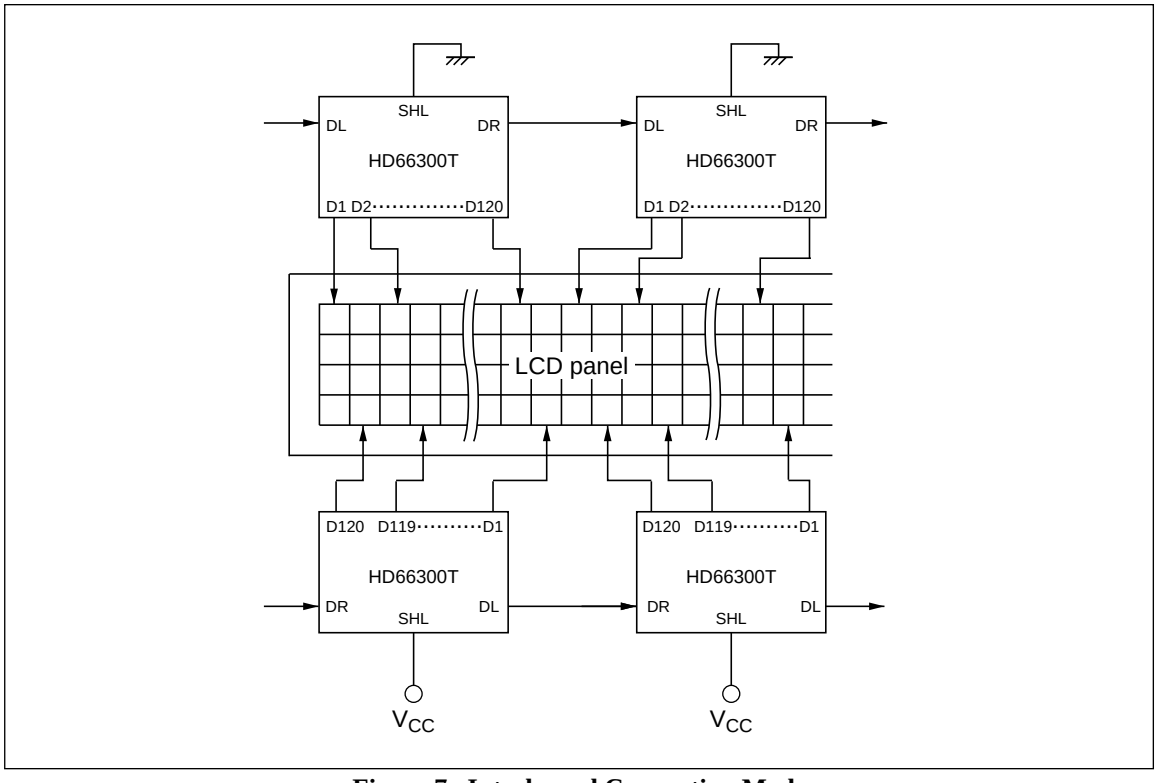


Figure 7 Interleaved Connection Mode

Internal Operation

The HD66300T has four sample and hold circuits for each outputs as shown in the block diagram, and its internal bidirectional shift register controls which circuits to sample data.

It has three-phase shift clocks with mutual phase difference of 120° to drive the shift register, which enables driving an LCD panel with mosaic pattern and triangular pattern.

The operation of sample and hold circuits and sampling operation are described below followed by the description of the relationship between three-phase shift clock phases and frequencies.

After the above description, determination of bias voltage is described; bias voltage controls driving characteristics of a differential amplifier and output buffer of the sample and hold circuits.

Finally, the OE and FD signals are described; they determine the operation of the sample and hold shift matrix circuit. Timing charts for each mode follow the description.

Sample and Hold Circuitry

Operation of Sample and Hold Circuitry

The HD66300T has four sample and hold circuits A, B, C, and D per LCD drive signal output. Sample and hold circuit pair A and B is supplied with the same sampling clock pulses as circuit pair C and D. One of the signals output by these circuits is connected to an output driver.

These sample and hold circuits repeat sampling and outputting of signals alternately to drive an TFT-type LCD panel.

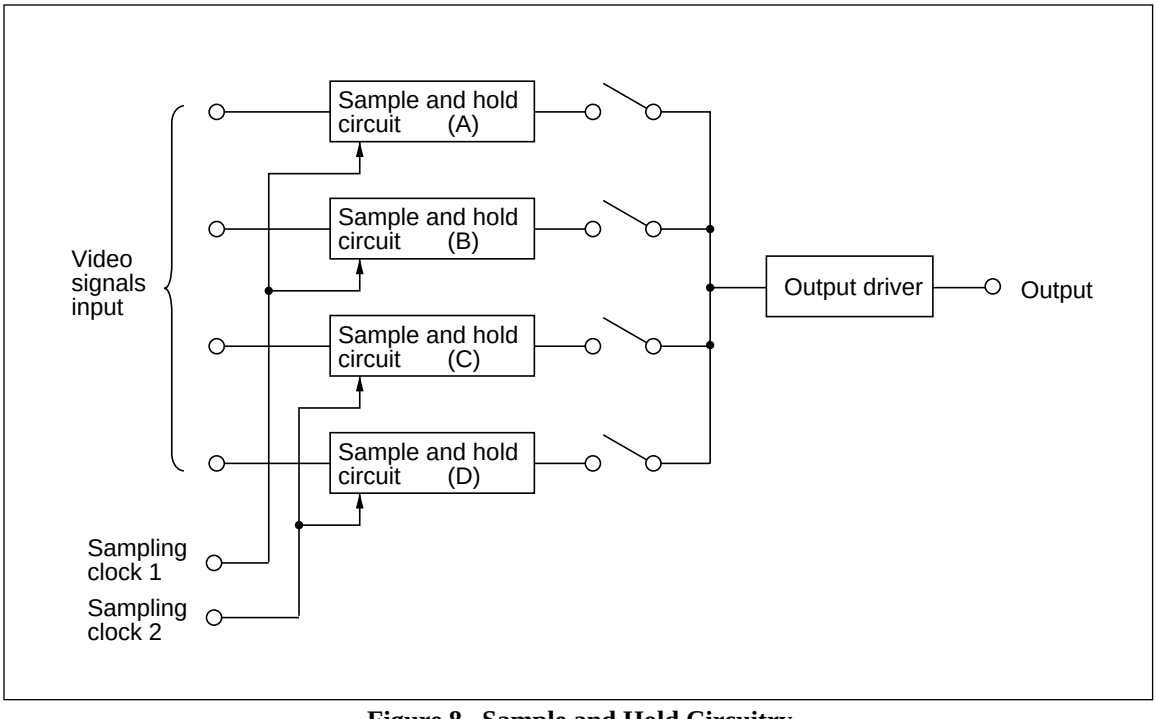


Figure 8 Sample and Hold Circuitry

In single-rate sequential drive mode, sample and hold circuits A and D are alternately used; circuits B and C perform sampling operation, but are not used since they are not connected to the output driver.

In single-rate sequential drive mode, one sample and hold circuit samples the signal during one horizontal scanning period, and outputs it as an LCD drive signal in the following horizontal scanning period.

In double-rate sequential drive mode, all sample and hold circuits A, B, C, and D are alternately used.

In double-rate sequential drive mode, two sample and hold circuits sample two signals during one horizontal scanning period, and output one of them as an LCD drive signal in the first half of the following horizontal scanning period, and output the other signal in the second half.

The following shows the timing charts of sampling and outputting operation.

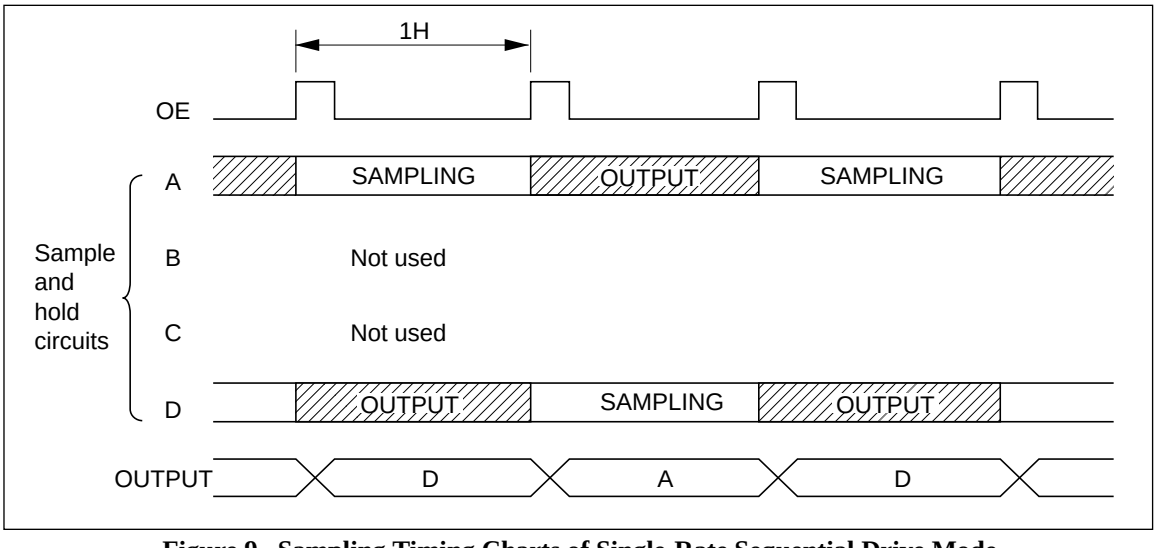


Figure 9 Sampling Timing Charts of Single-Rate Sequential Drive Mode

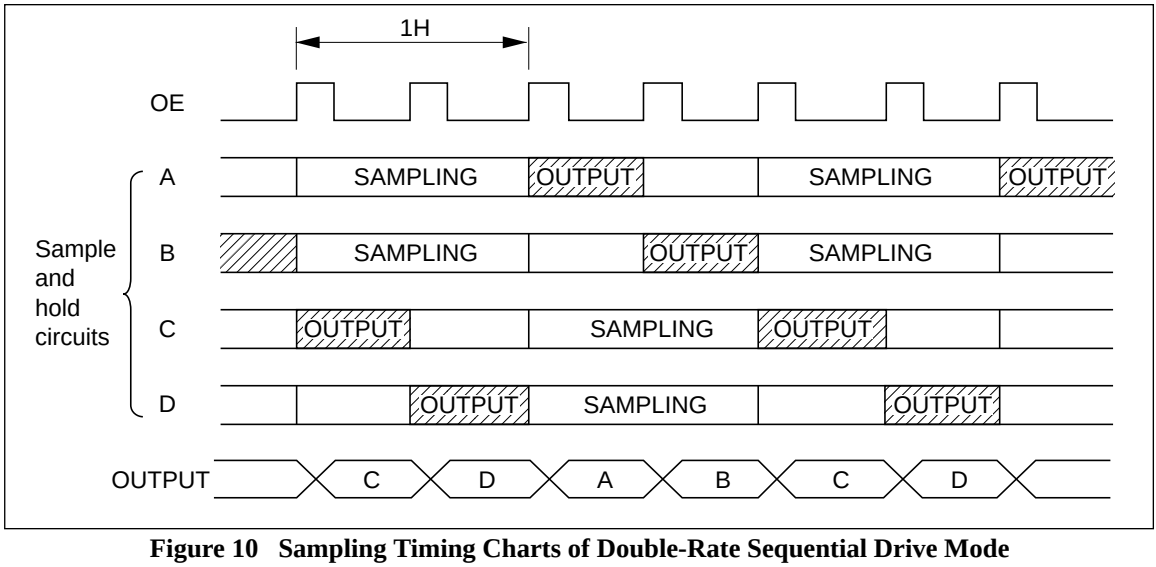


Figure 10 Sampling Timing Charts of Double-Rate Sequential Drive Mode

Sampling Operation

The HD66300T has a bidirectional shift register composed of 120 bits and each bit of the shift register generates the sampling pulses to control the sampling operation of the four sample and hold circuits connected to each LCD drive signal output pin. When a bit of the shift register is 1, the corresponding sample and hold circuits are in the sampling state; when it is 0, the corresponding sample and hold circuits are in the hold state. Consequently, shifting a 1 into the shift register activates in turn the sample and hold circuits corresponding to each LCD drive signal output pin.

Figure 11 is a shift register sketch illustrating the relationship between the shift register and the shift clocks HCK1, HCK2, and HCK3. Note that the order of sampling pulse generation depends on the state of pin SHL. D1 corresponds to DL and D120 to DR.

Figure 12 is a timing chart of sampling pulses generated by the shift register.

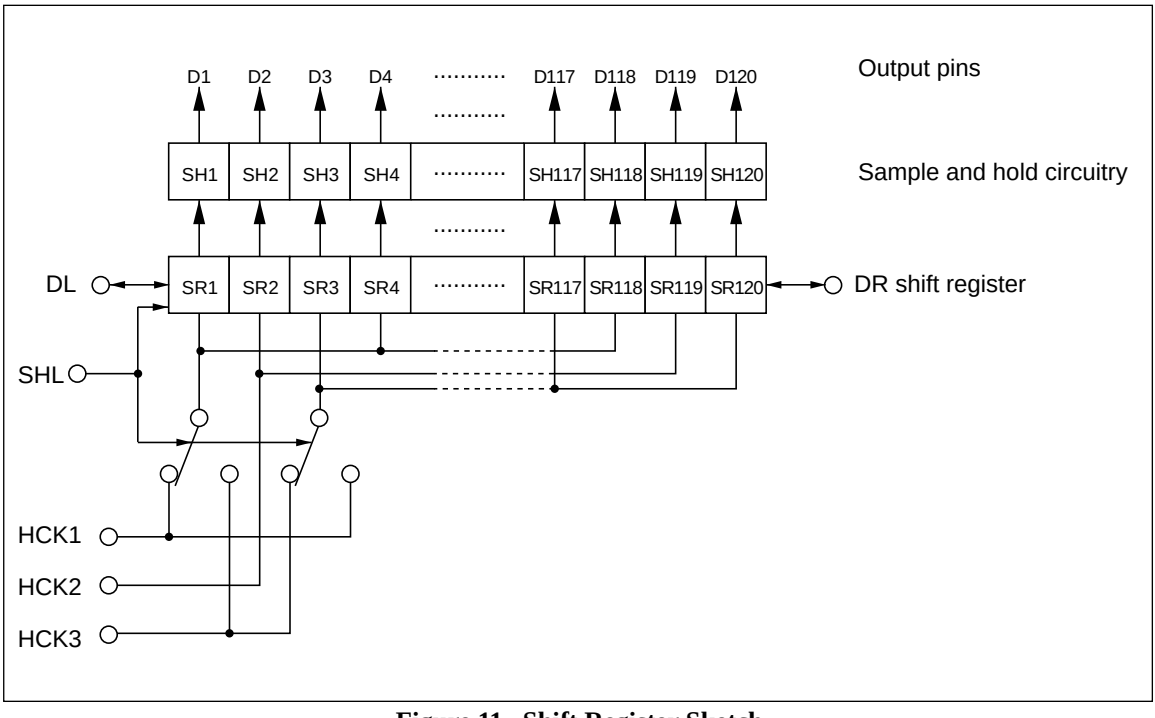
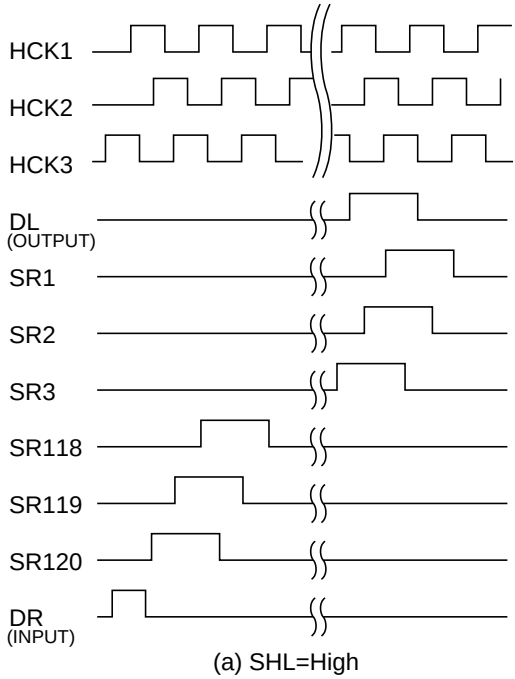
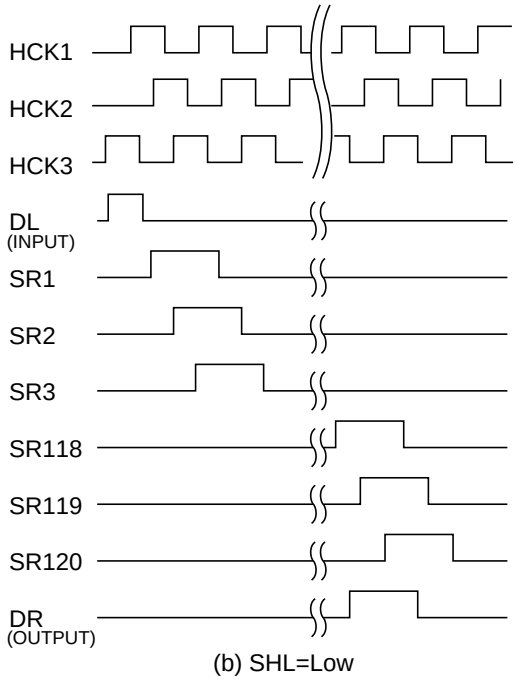


Figure 11 Shift Register Sketch



(a) SHL=High



(b) SHL=Low

Figure 12 Sampling Pulse Timing Chart

Three-Phase Shift Clocks

Three-Phase Shift Clocks and Sample Start Signal: Shift clocks HCK1, HCK2, and HCK3, which are operation clocks for the shift register, must be three-phase clocks with 50-percent duty. The HCK2 clock must be generated 120° after the HCK1 clock, and the HCK3 clock 240° after the HCK1 clock. Sampling operation starts when 1 is input from pin DL or DR at a rising edge of the HCK1 clock pulse.

In monodirectional connection mode, all the HD66300T chips must be supplied with the same three-phase shift clock pulses. In interleaved connection mode, the frequency of the three-phase shift clocks must be half of that in monodirectional connection mode, and the phase shift between the upper drivers clocks and the lower drivers clocks must be one pixel.

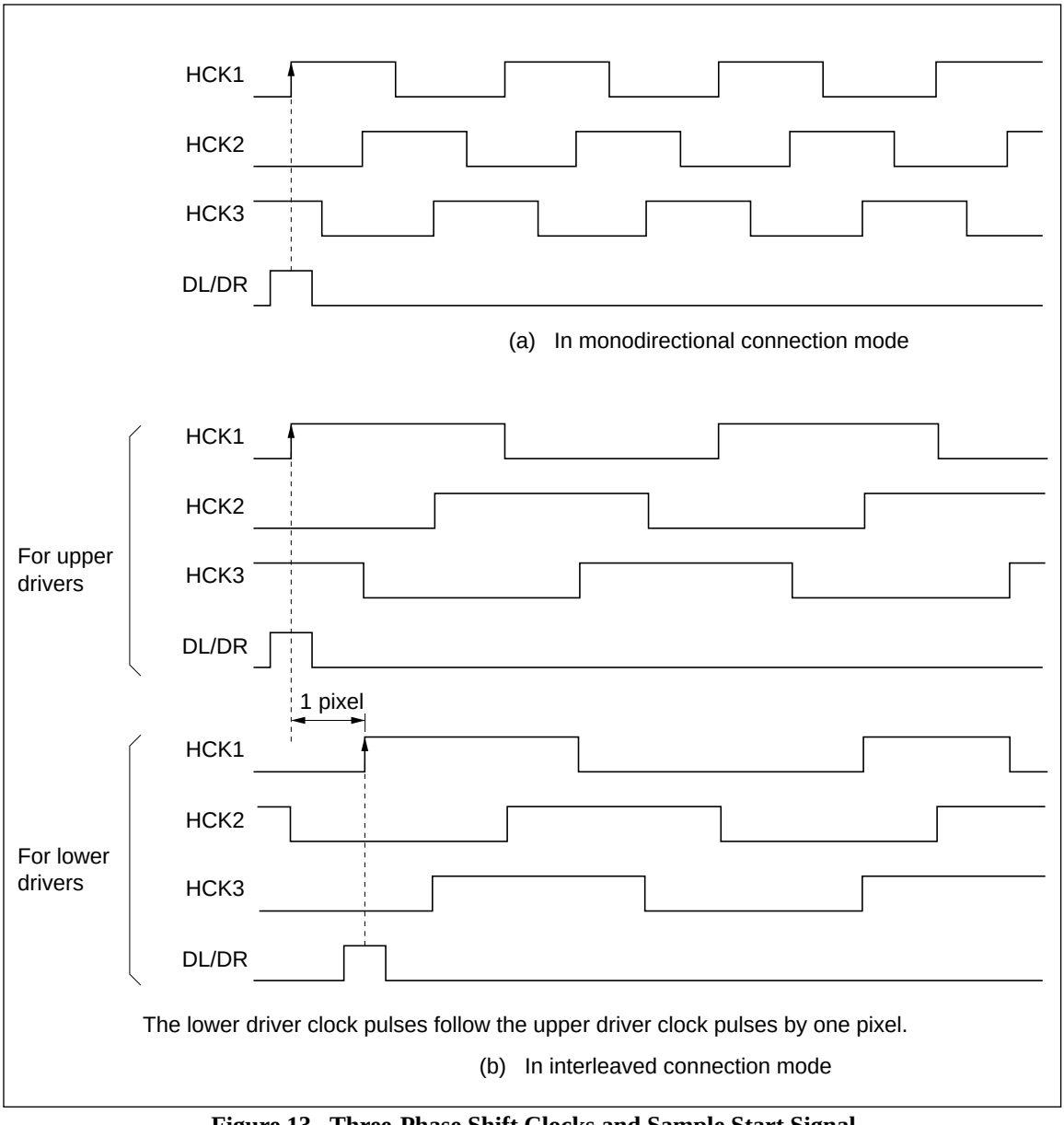


Figure 13 Three-Phase Shift Clocks and Sample Start Signal

Some position shift exists between the pixels of even number lines and those of odd number lines for LCD panels having triangular patterns. This requires generating a phase shift between the three-phase clocks for even number lines and those for odd number lines. The required phase shift is 1.5 pixels for LCD panels having a unicolor triangular pattern, while it is 0.5 pixels for those having a bicolor triangular pattern.

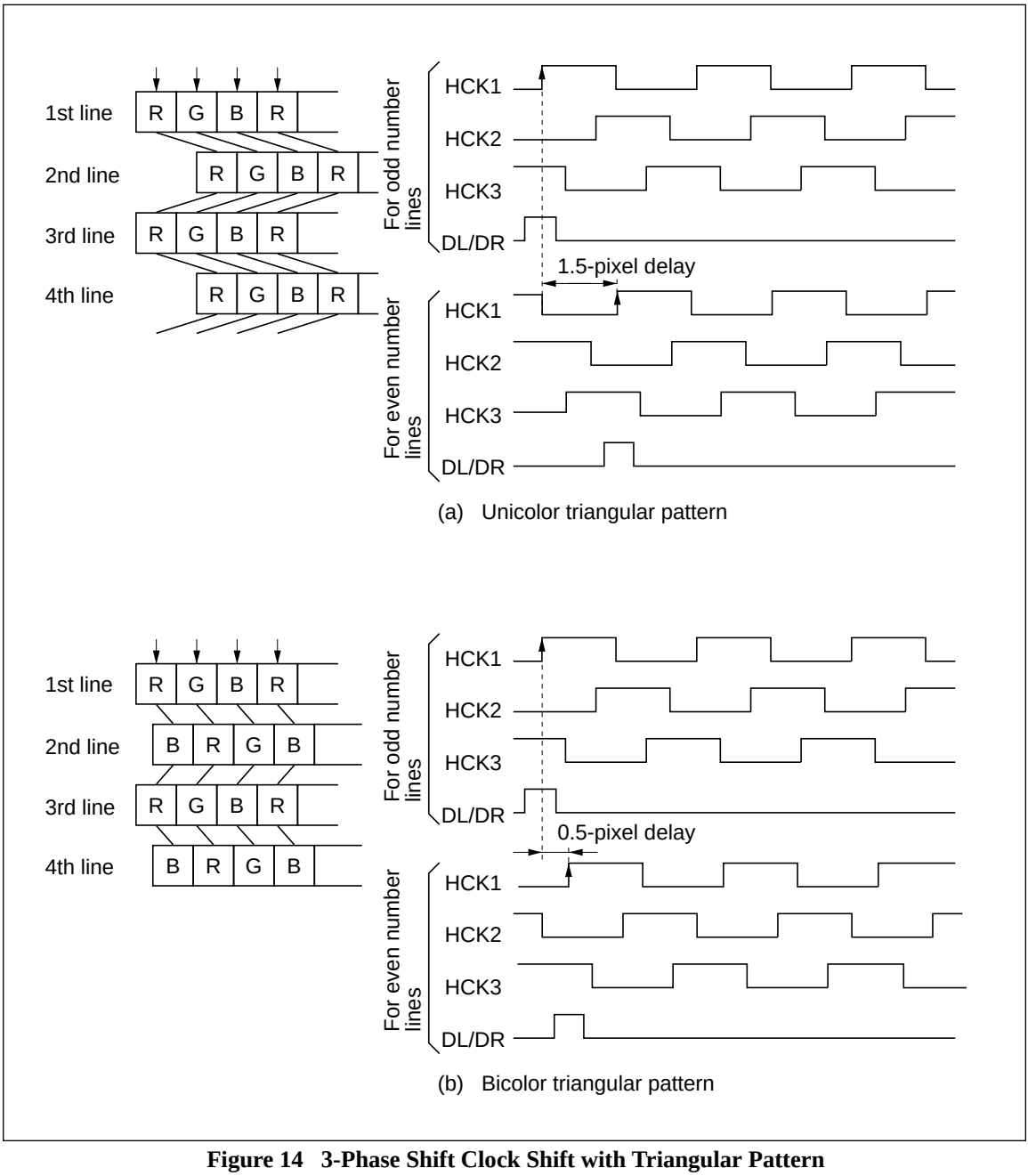


Figure 14 3-Phase Shift Clock Shift with Triangular Pattern

How to Generate Three-Phase Shift Clocks: Three-phase shift clocks can be generated by dividing the base clock, which is generated from a horizontal synchronizing clock, through the use of a frequency multiplier such as a PLL circuit.

The number of horizontal pixels of the LCD panel and the valid display ratio determines the base clock frequency f.

If the number of horizontal pixels is 480 and the valid display ratio is 95% in the NTSC system, the base clock frequency f is about 9.59 MHz according to the following equation.

$$\begin{aligned} f &= (1/\text{valid display period}) \times (\text{no. of horizontal pixels/valid display ratio}) \\ &= 480/(52.7\ \mu\text{sec} \times 0.95) \\ &= 9.59\ (\text{MHz}) \end{aligned}$$

The three-phase clocks can be generated by dividing f by 3 (in the monodirectional connection mode) or 6 (in the bidirectional connection mode).

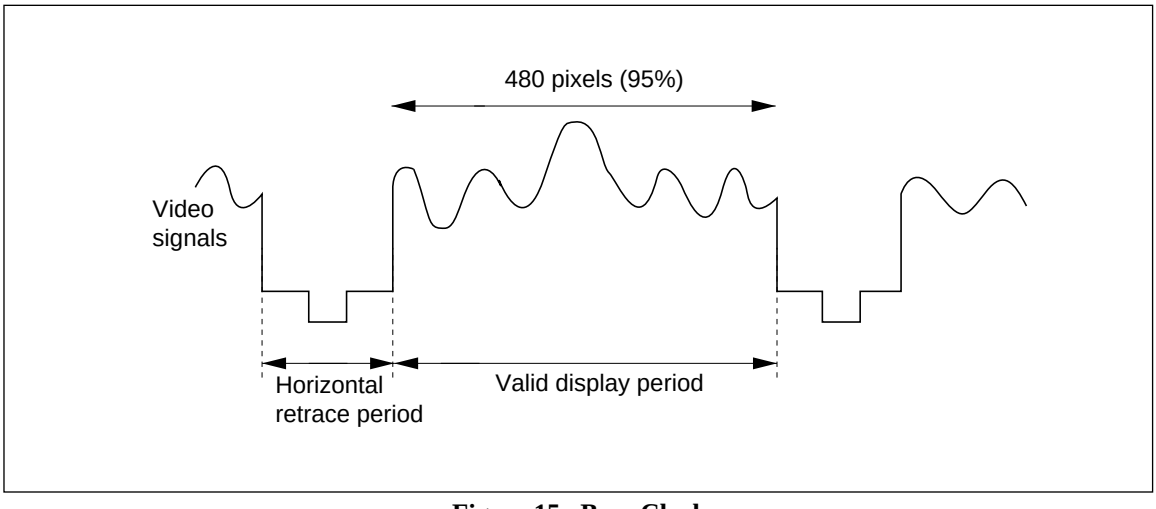


Figure 15 Base Clock

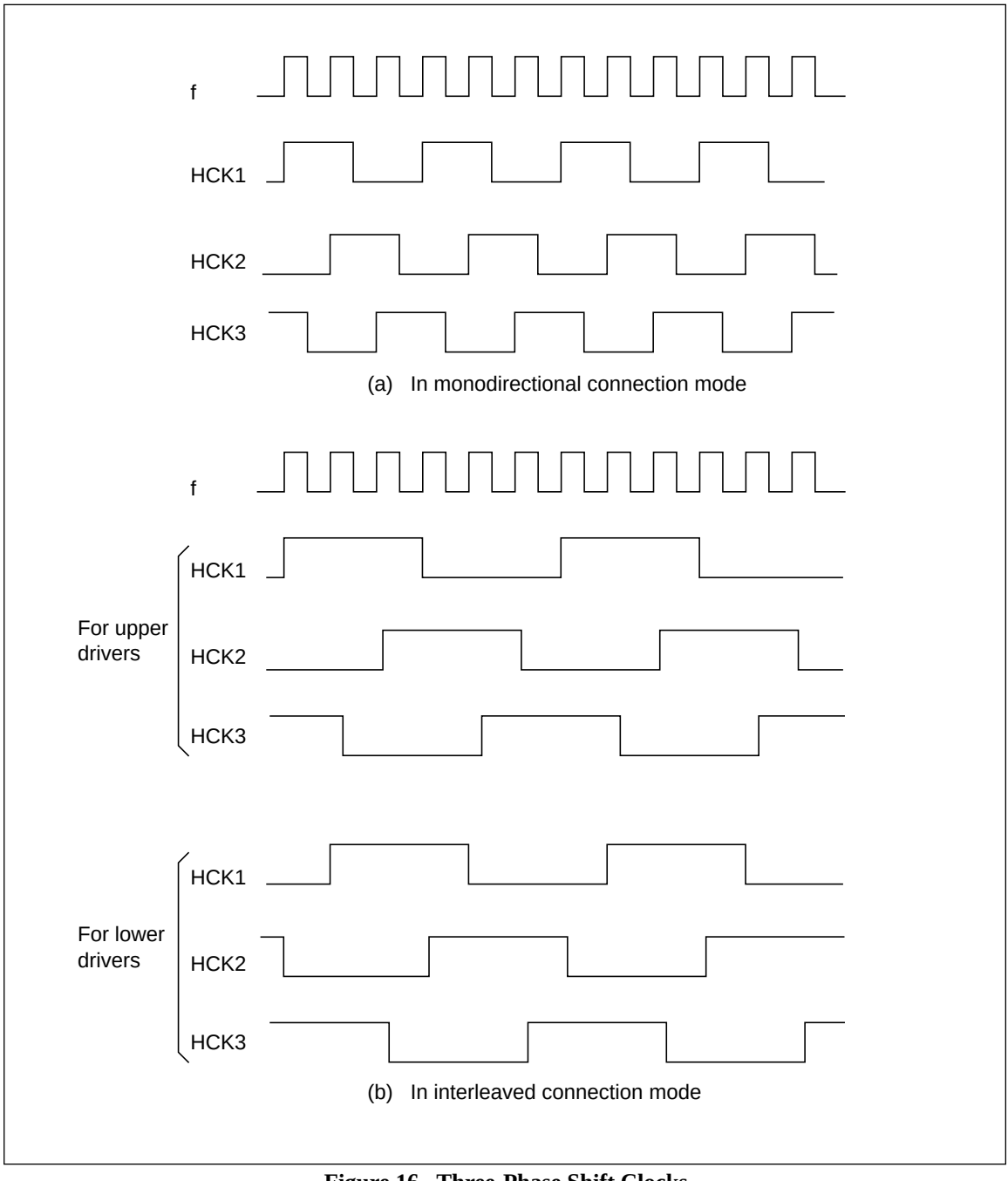


Figure 16 Three-Phase Shift Clocks

Bias Voltage

Voltages V_{bsB} , V_{bsH}, and V_{bo} control the drive capability of the output buffer and differential amplifier. Here the LSI must be used in the range of

$$V_{CC} - 4.0\ V \le V_{bsB}\ ,\ V_{bsH}\ ,\ V_{bo} \le V_{CC} - 2.0\ V$$

V_{bsB} controls the drive current capability of the output buffer when OE is high (IV_{sB}) and V_{bsH} controls the leakage correction current of when OE is low (IV_{sH}). Figure 17 and figure 18 show the relationship between IV_{sB} and V_{bsB} and the relationship between IV_{sH} and V_{bsH}, respectively.

V_{bsB} and V_{bsH} should be to an appropriate level for the electrical characteristics of the LCD panel used.

The rise time (t_{DDR}) and the fall time (t_{DDF}) of the output buffer depend on the input level of V_{bsB}.

Figure 19 shows the relationship between t_{DDR}, t_{DDF} and V_{bsB}.

V_{bo} controls the bias current of the differential amplifier (IV_{bo}).

Figure 20 shows the relationship between the rise and fall times (t_{DDR}, t_{DDF}) of the output buffer and V_{bo}.

V_{bo} should be adjusted to an appropriate level for the electrical characteristics of the LCD panel used.

The increase of total current consumption is 120 times larger than that of IV_{bsB}, IV_{bsH} and IV_{bo}, because figure 17, 18 and 21 each shows the case of one output and HD66300T has 120 outputs.

Figure 17, 18, 19, 20 and 21 are just for reference and do not guarantee the characteristics.

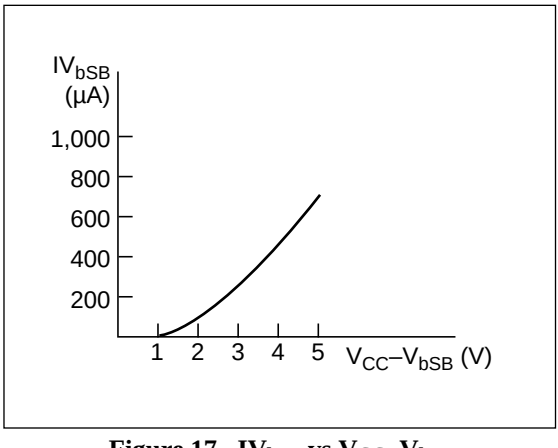


Figure 17 IV_{bsB} vs V_{CC}–V_{bsB}

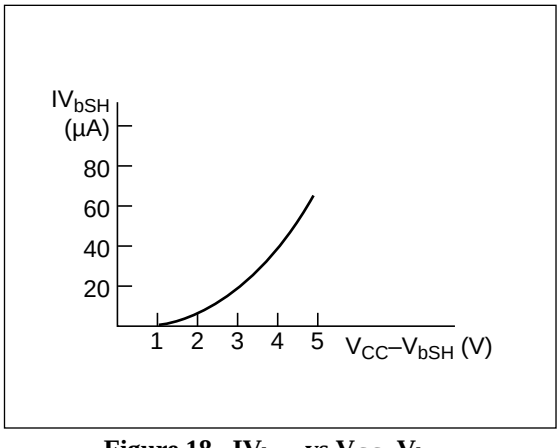


Figure 18 IV_{bsH} vs V_{CC}–V_{bsH}

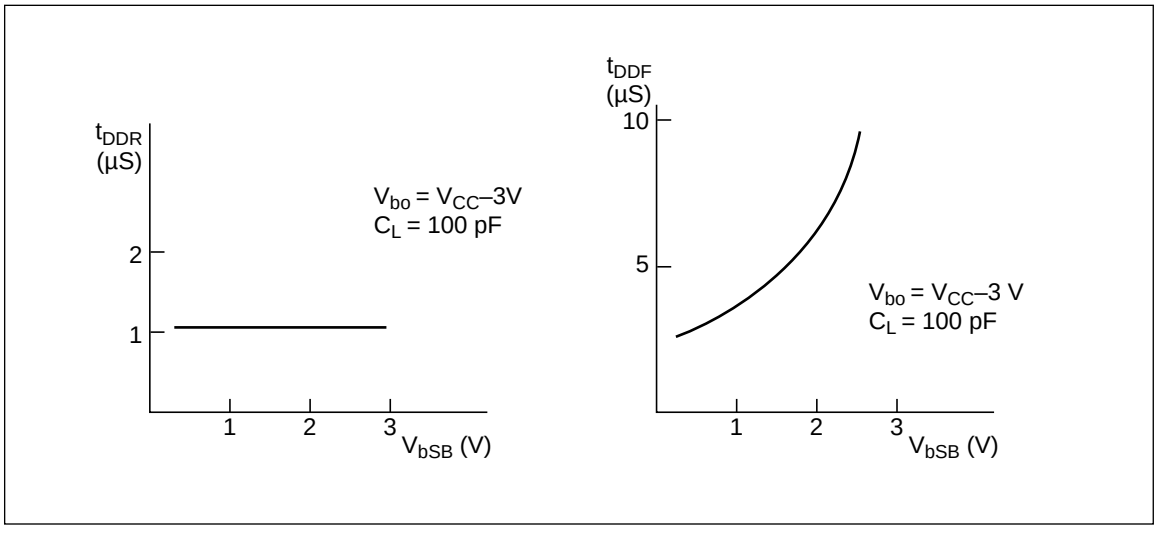


Figure 19 t_{DDR}, t_{DDF} vs V_{bsB}

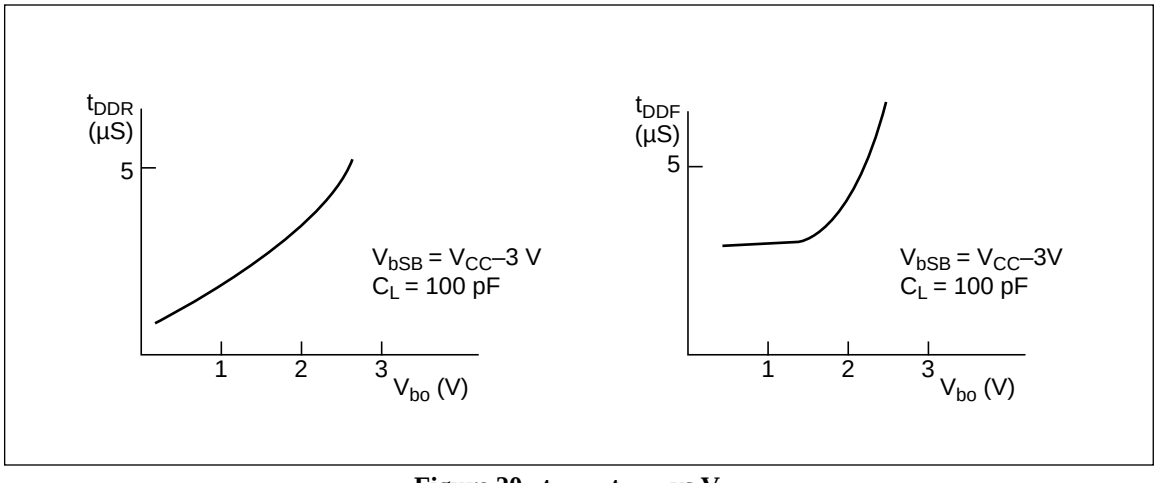


Figure 20 t_{DDR}, t_{DDF} vs V_{bo}

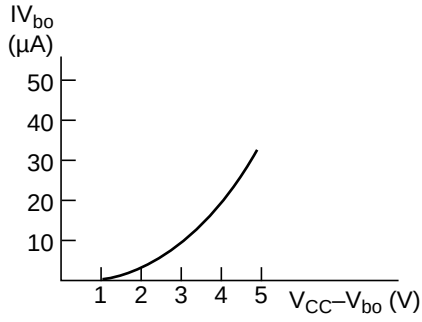


Figure 21 IV_{bo} vs V_{CC}–V_{bo}

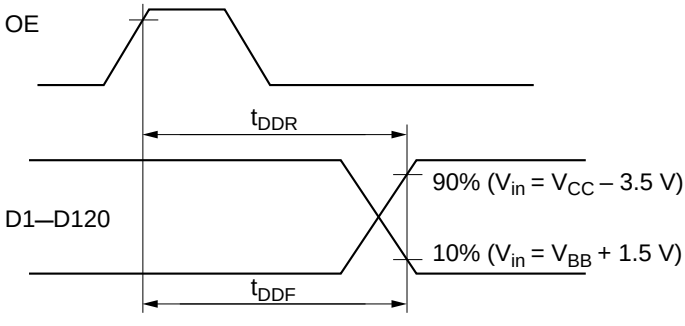


Figure 22 Definition of t_{DDR} and t_{DDF}

OE Signal

The OE signal has the following functions:

Clock for Internal Circuits: Controls the sample and hold circuitry and the controller of the shift matrix circuit, and switches the output signal at the OE signal rising edge.

Switching of Drive Capability of the Output Buffer: Determines the current drive capability of the output buffer;

OE = high: Drives with large current (300 µA, typ)
OE = low: Drives with small current (20 µA, typ)

This function allows the output buffer to operate with large current during the transition of an output signal, thus shortening its falling time. At the same time it allows the output buffer to operate with small current while an output signal is stable, lowering current consumption.

The drive current is controlled by bias voltages V_{bsB} (large current) and V_{bsH} (small current).

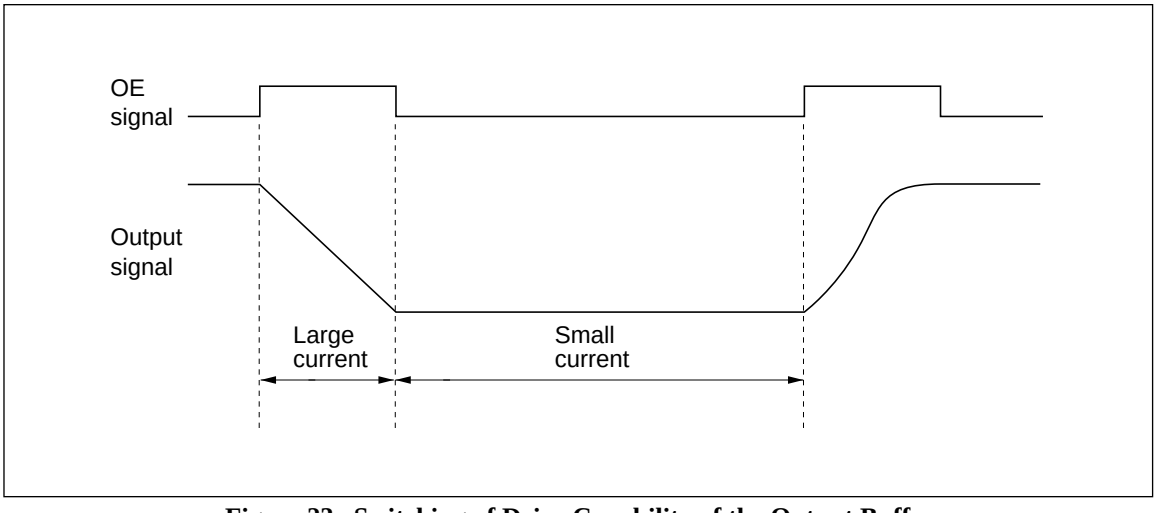


Figure 23 Switching of Drive Capability of the Output Buffer

FD Signal

The FD signal is the field determination signal; a field is determined by the state of this signal at the rising edge of the OE signal. This signal synchronizes the internal controllers with TV signals.

The order of outputting signals is determined at the fourth rising edge of the OE signal after the rising or falling edge of the FD signal in double-rate sequential drive mode, while it is determined at the third rising edge in single-rate sequential drive mode; herein after, as long as the FD signal is not changed, signals will be output in the determined order at most every 12 pulses of the OE signal in double-rate sequential drive mode, while at most every 6 pulses in single-rate sequential drive mode.

The FD signal should usually be high in the first field and low in the second field. In some modes, however, it should be high in both fields, but low for at least one-pulse time period of the OE signal during the horizontal scanning period.

The order of outputting signals and the timing of inputting the FD signal vary depending on the mode. For more details, refer to the appropriate timing charts.

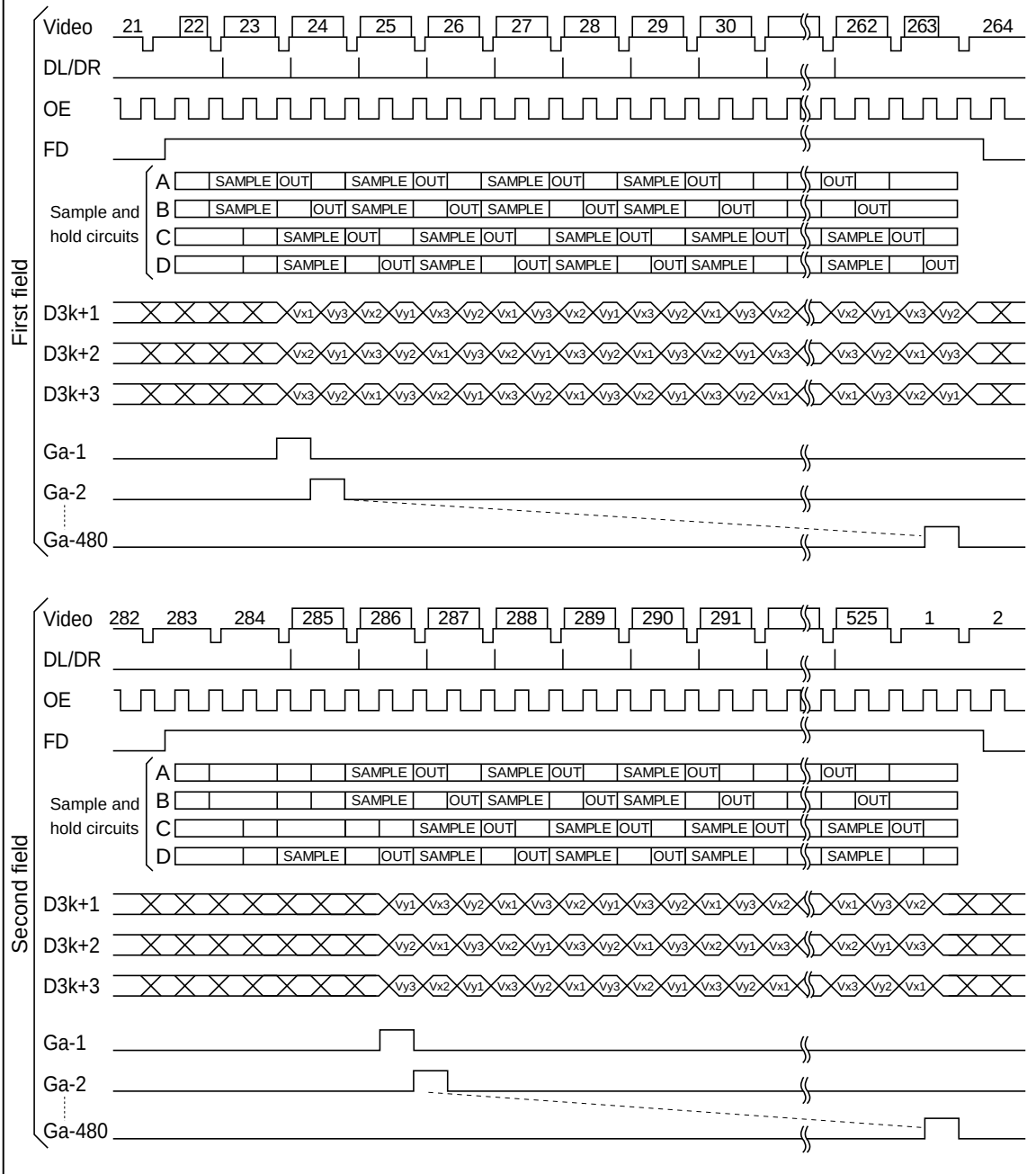
Timing Charts for Each Mode

Table 2 Reference Timing Charts for Each Mode

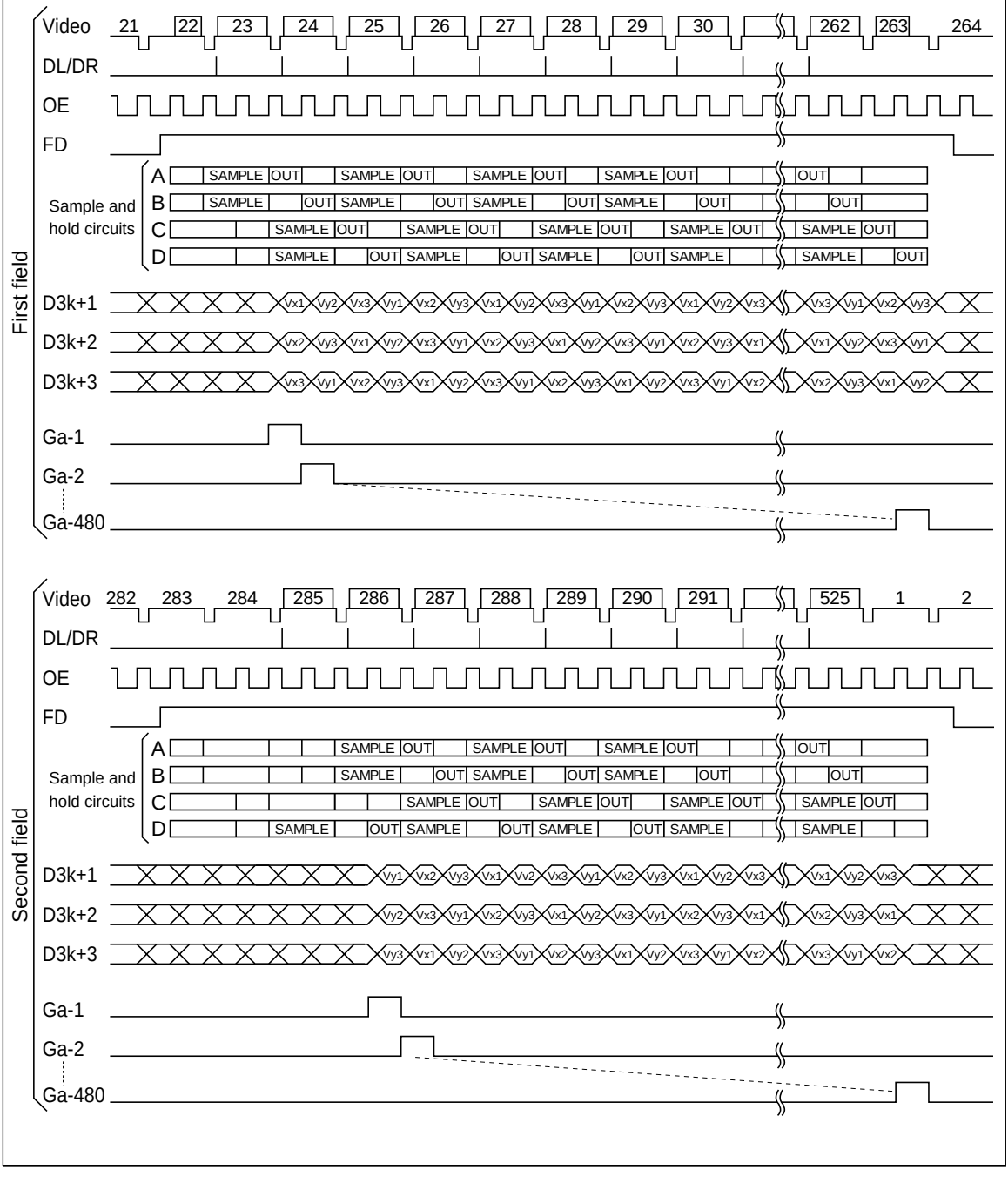
Filter Arrangement			Single (D/S = Low)		Double (D/S = High)			
					Interlace		Non-Interlace	
			Per-Line	Per-Field	Per-Line	Per-Field	Per-Line	Per-Field
Mosaic	Top-left to bottom-right	Inter-leaved	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
		Mono-directional	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
	Top-right to bottom-left	Inter-leaved	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
		Mono-directional	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
Vertical stripe			MODE 17	MODE 20	MODE 3	MODE 7	MODE 10	MODE 14
Unicolor triangular			MODE 17	MODE 20	MODE 4	MODE 4	MODE 11	MODE 11
Bicolor triangular			MODE 17	MODE 17	MODE 4	MODE 4	MODE 11	MODE 11

Single: Single-rate sequential drive mode
Double: Double-rate sequential drive mode
Per-Line: Per-line inversion mode
Per-Field: Per-field inversion mode
Interleaved: Interleaved connection mode
Monodirectional: Monodirectional connection mode

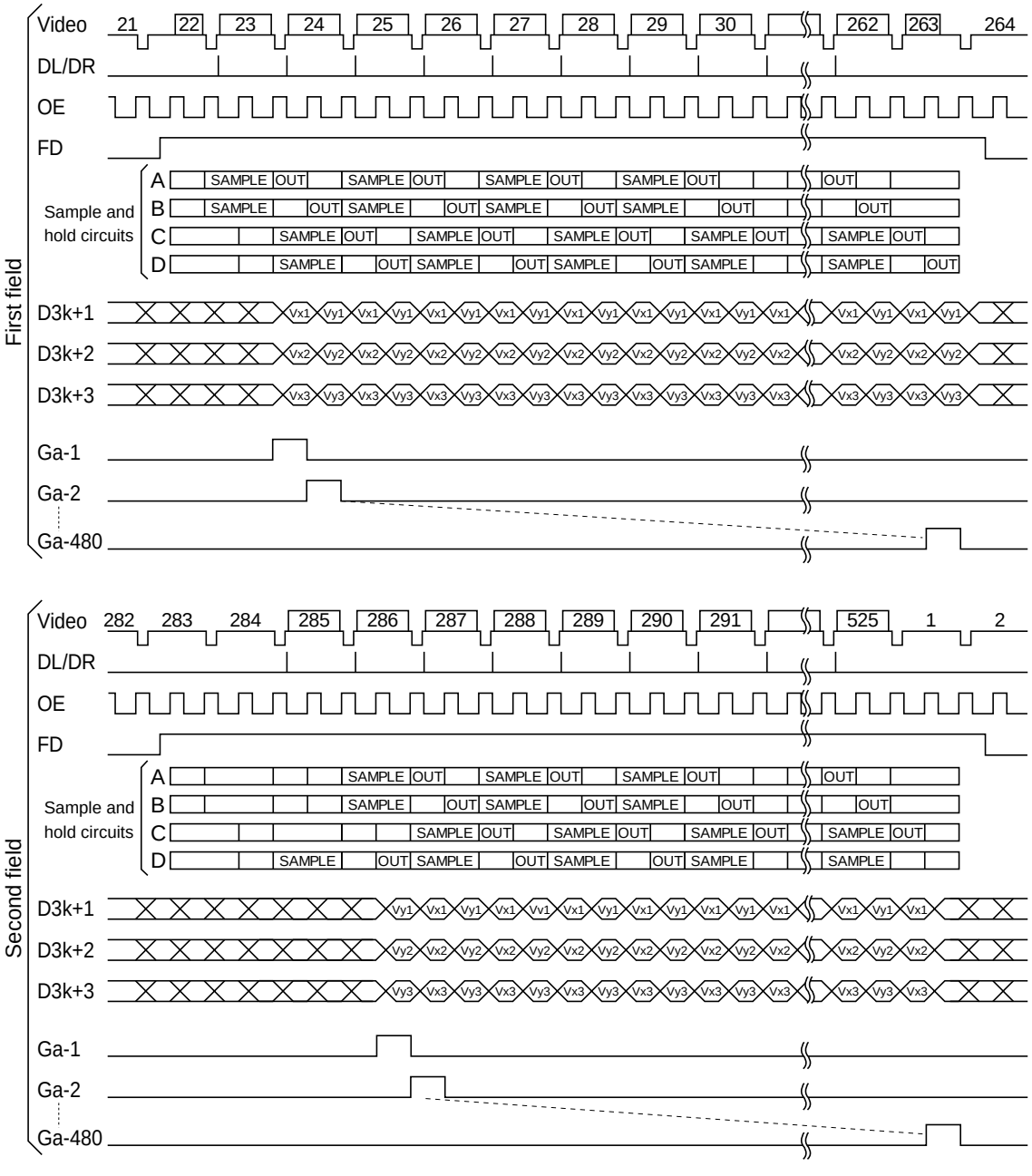
MODE 1	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



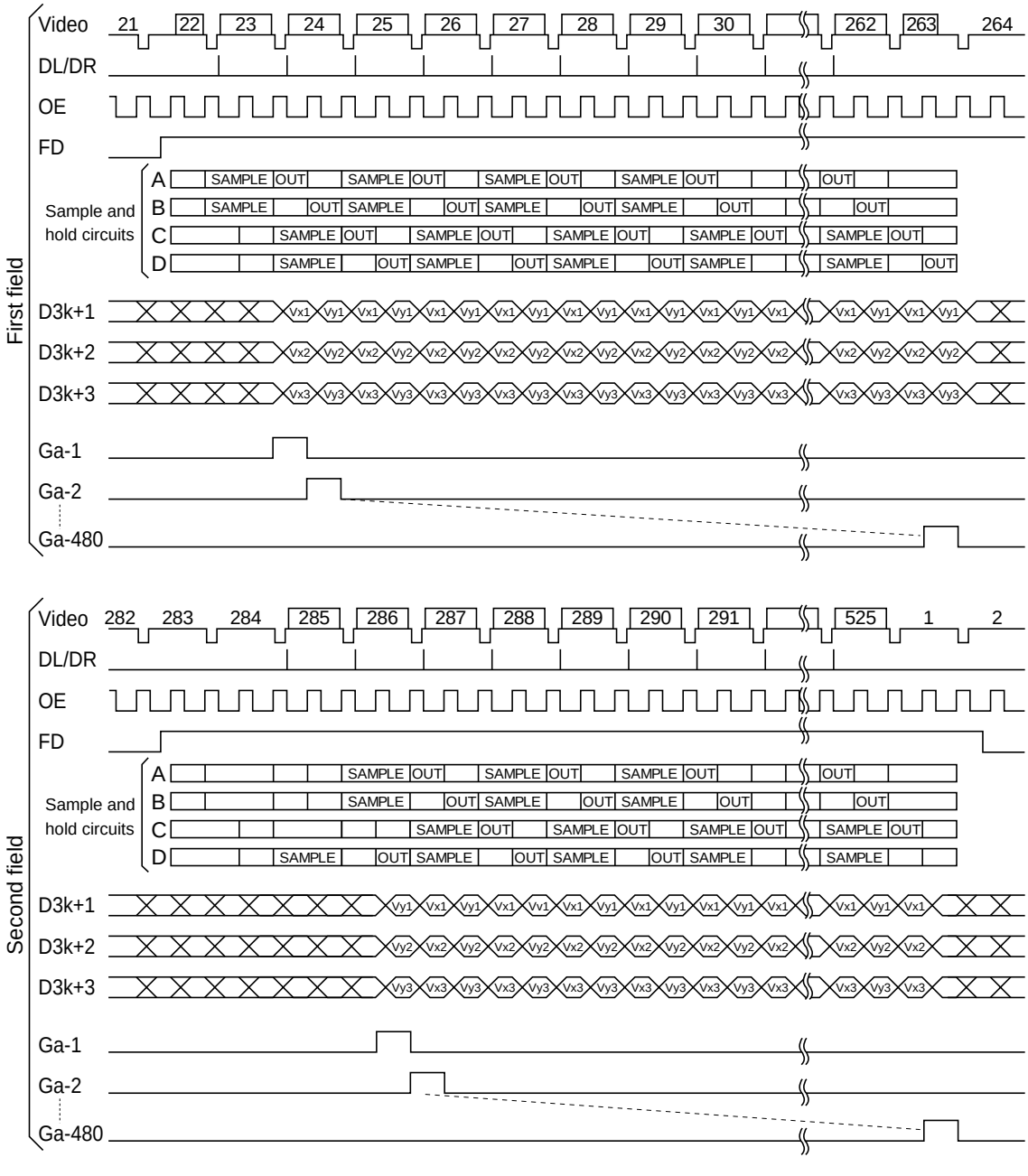
MODE 2	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	GND



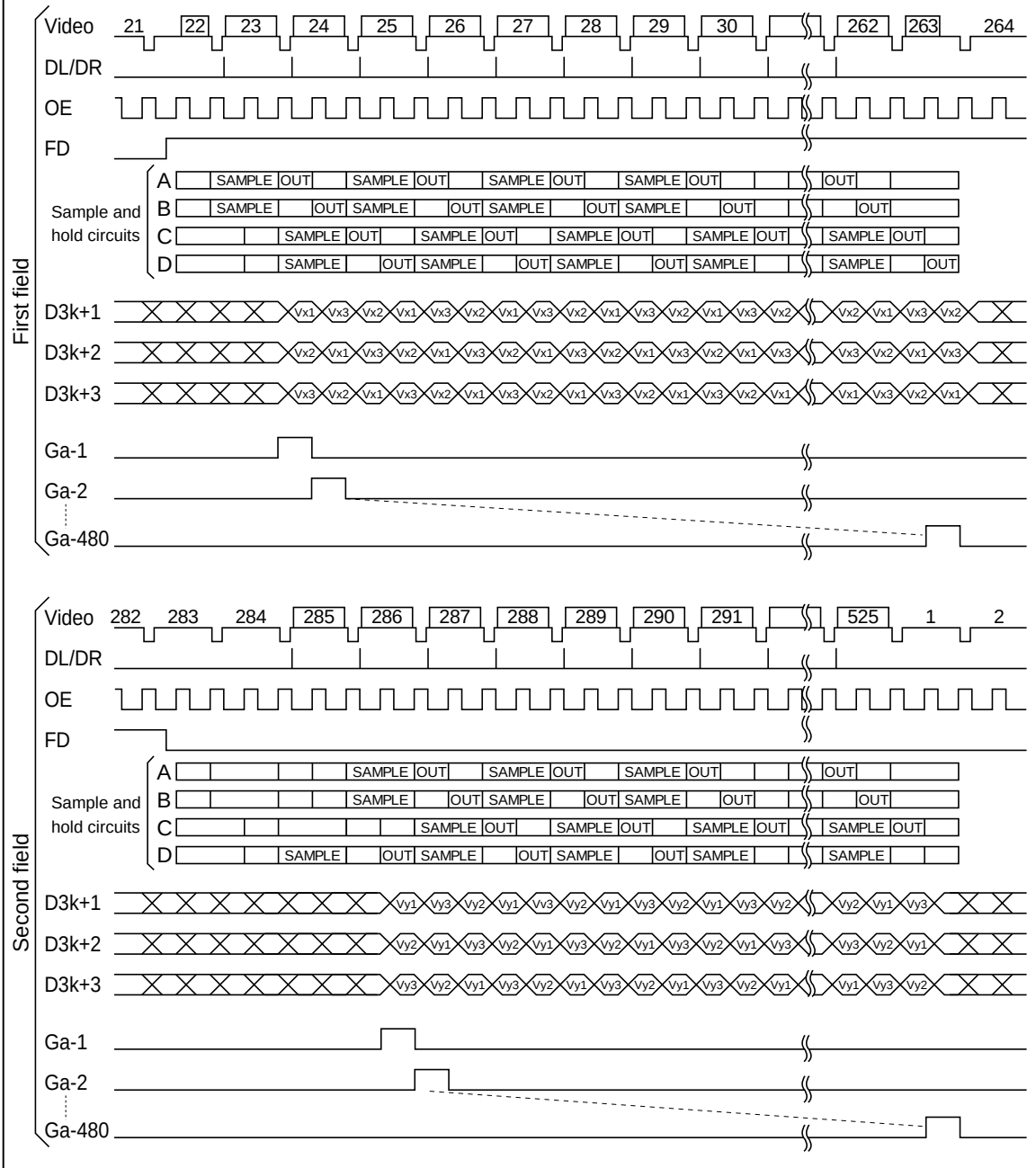
MODE 3	
D/S	V_{CC}
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



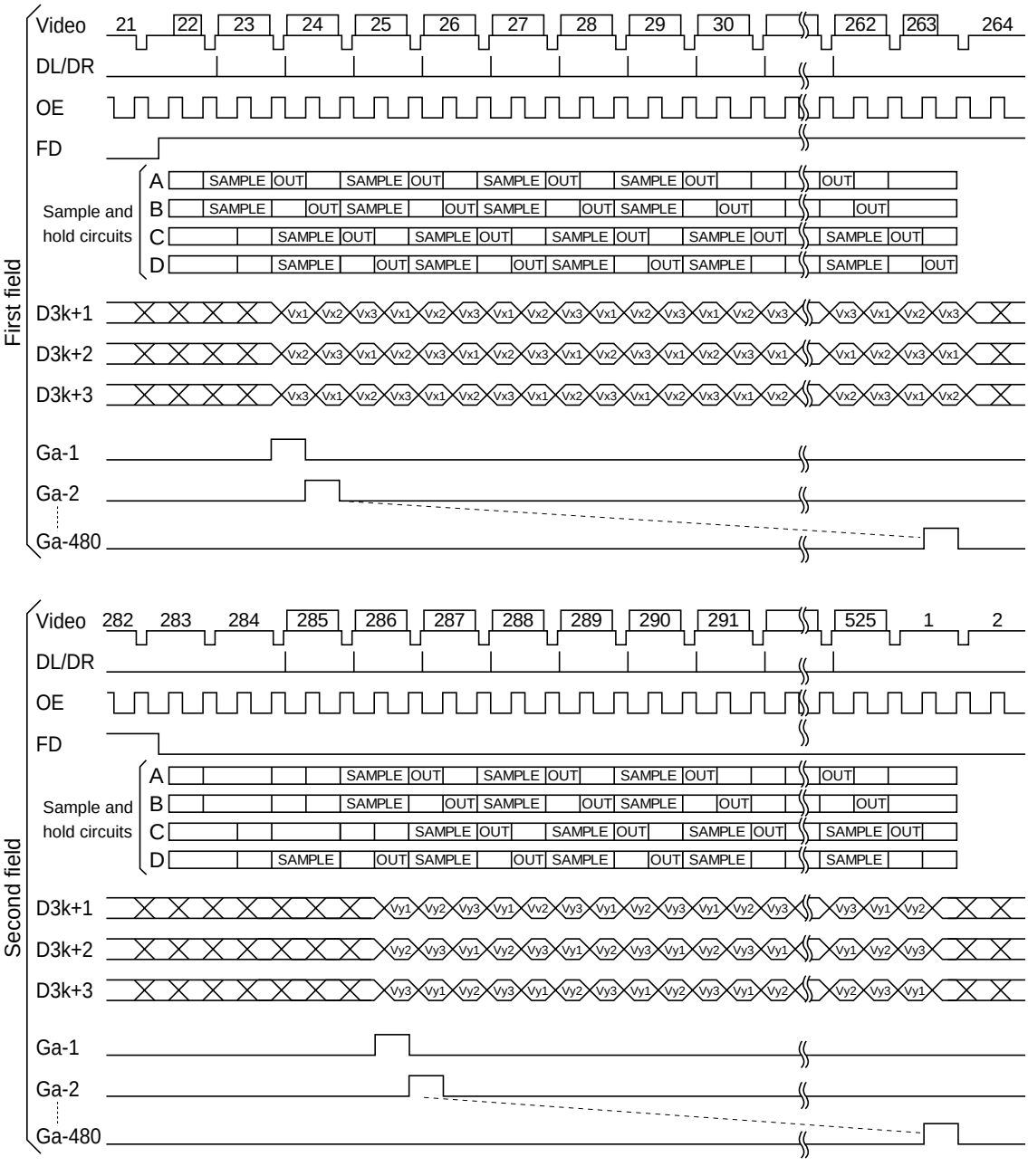
MODE 4	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND



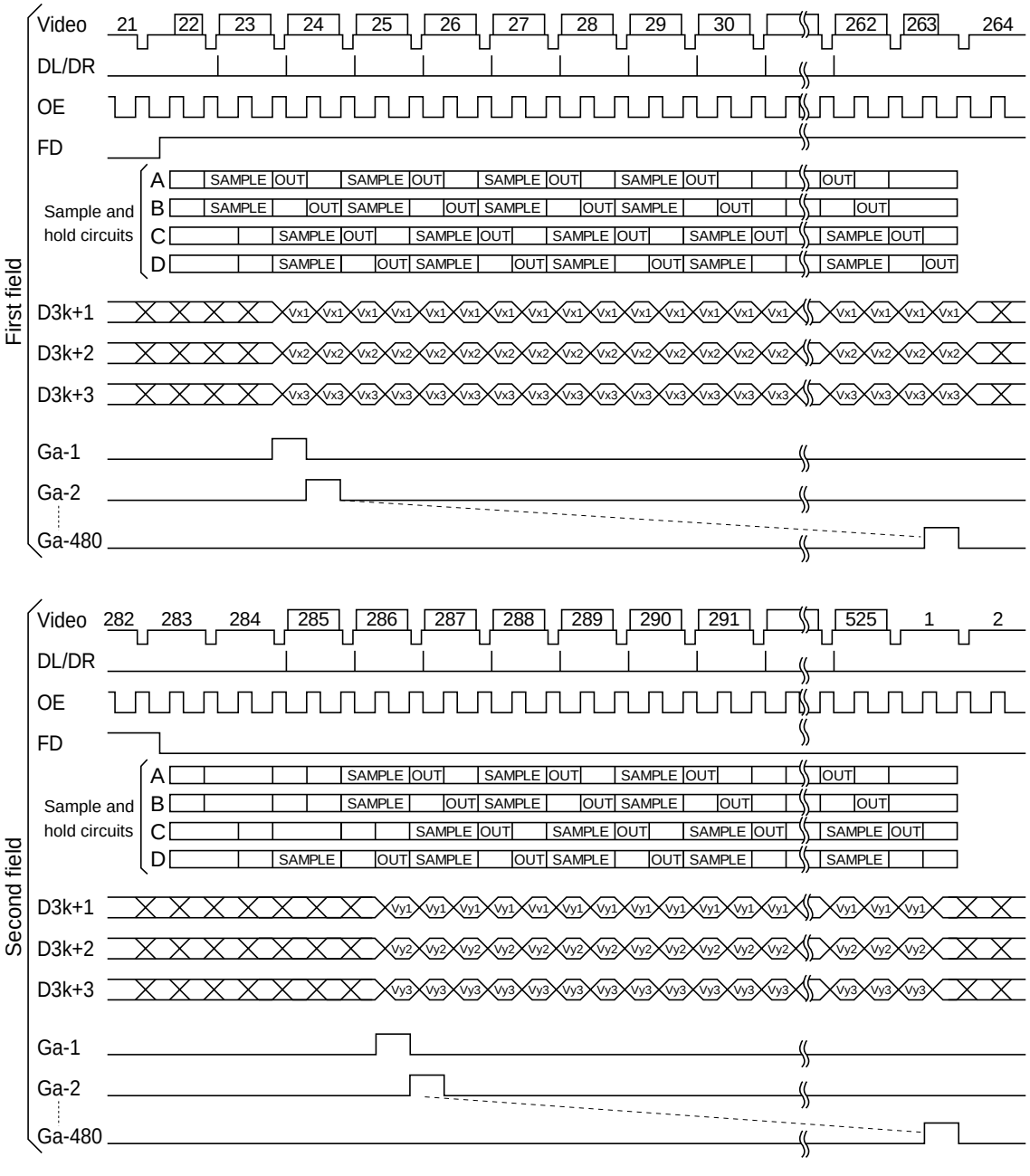
MODE 5	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	V_{CC}



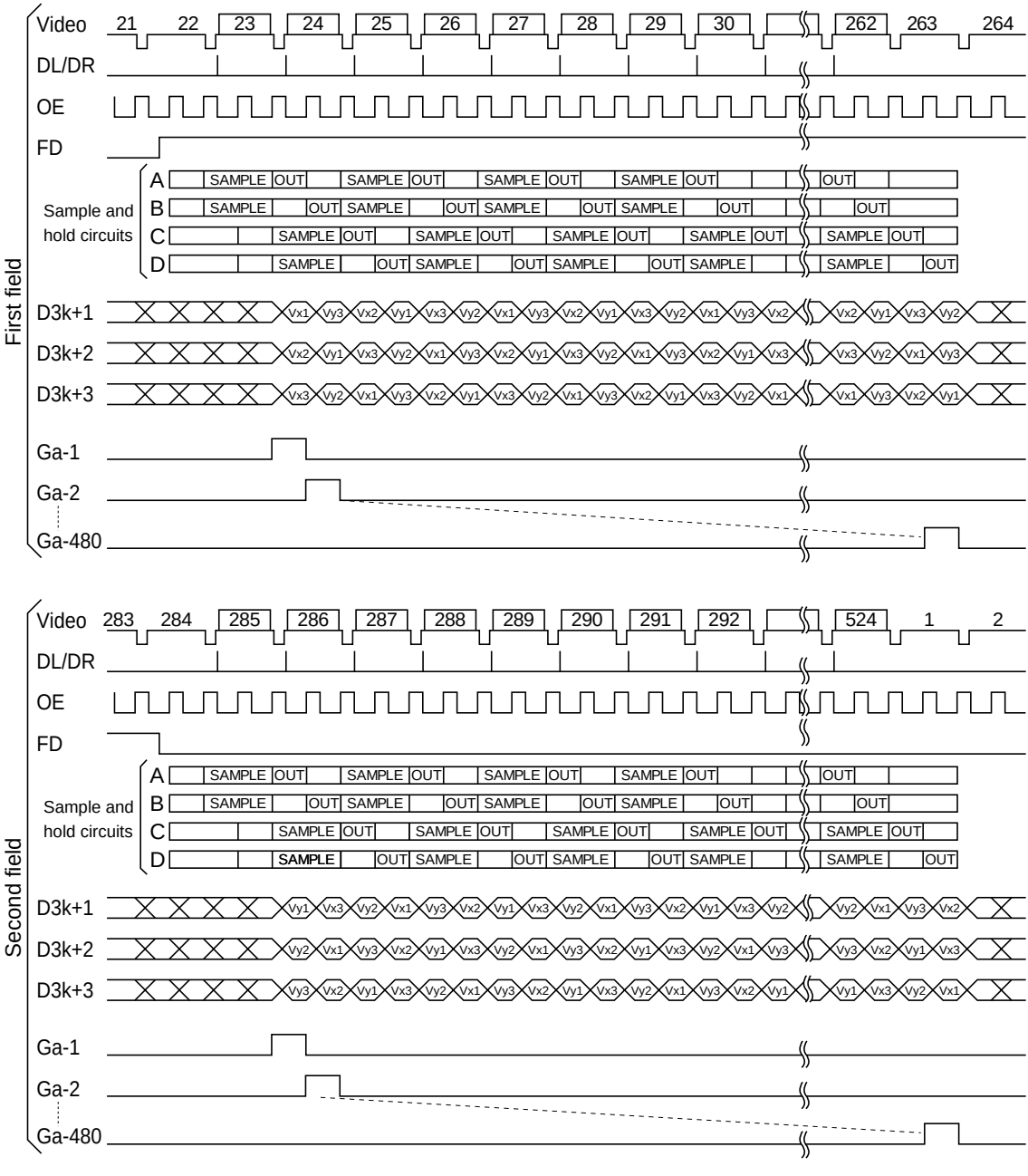
MODE 6	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND



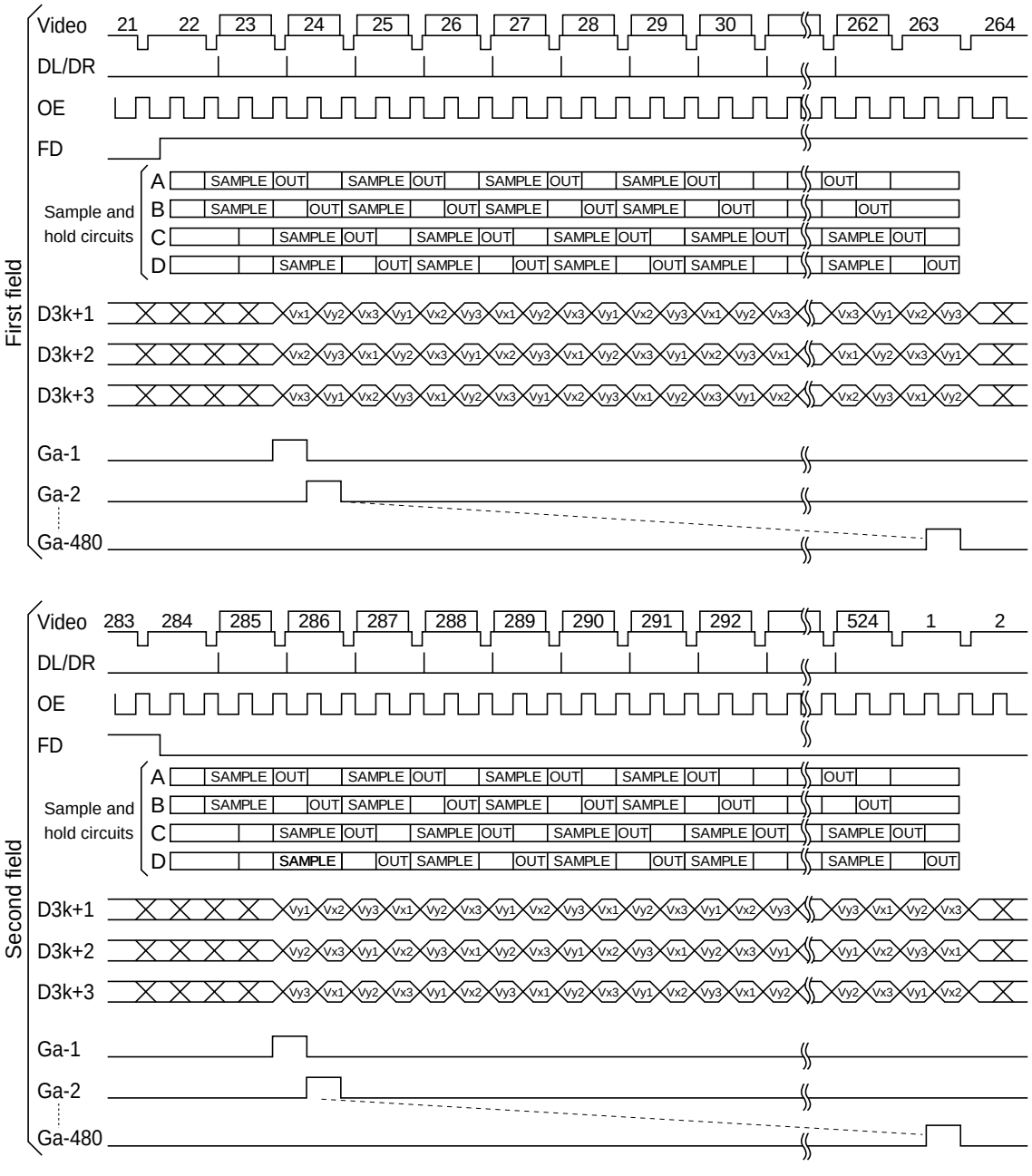
MODE 7	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



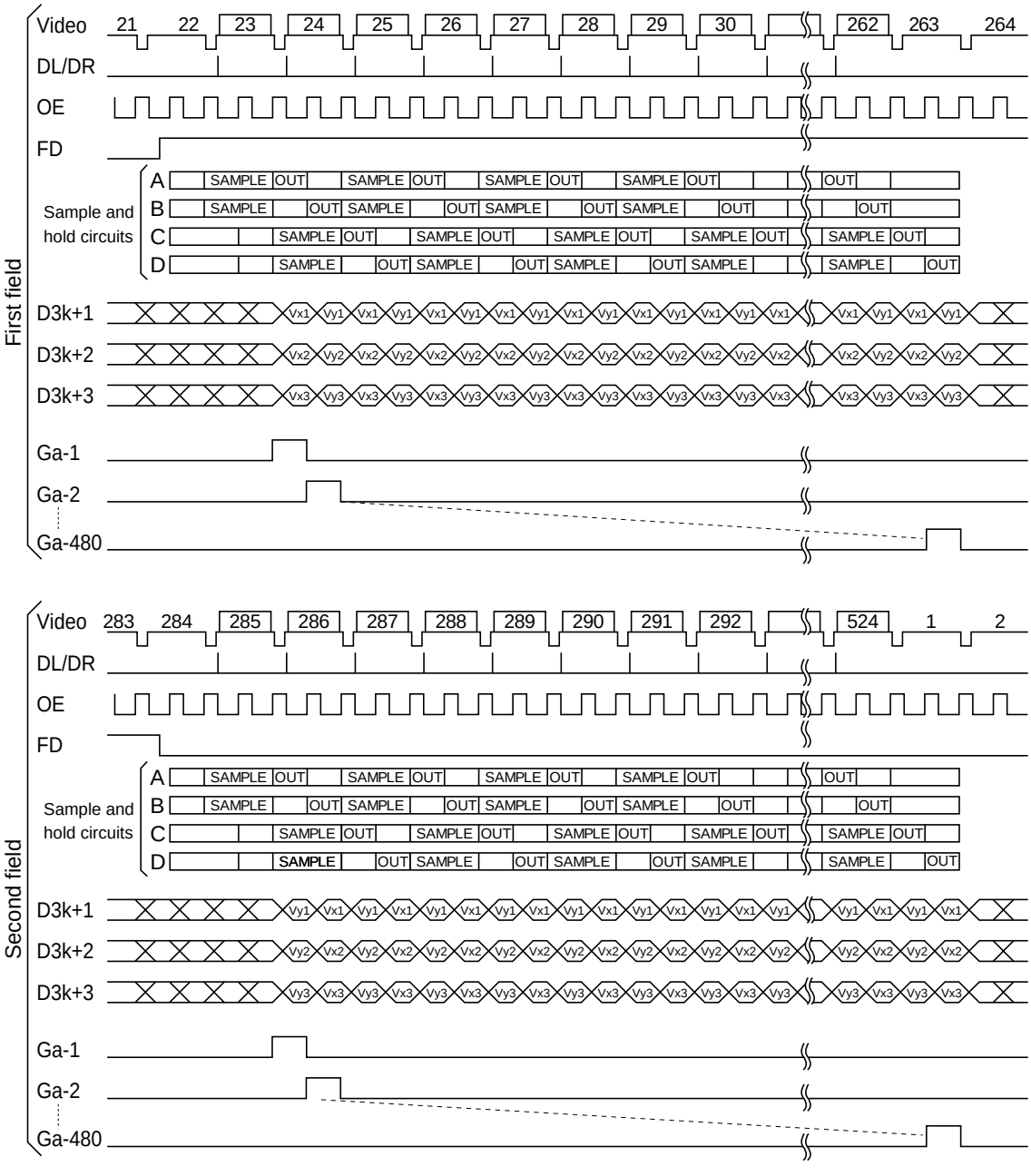
MODE 8	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



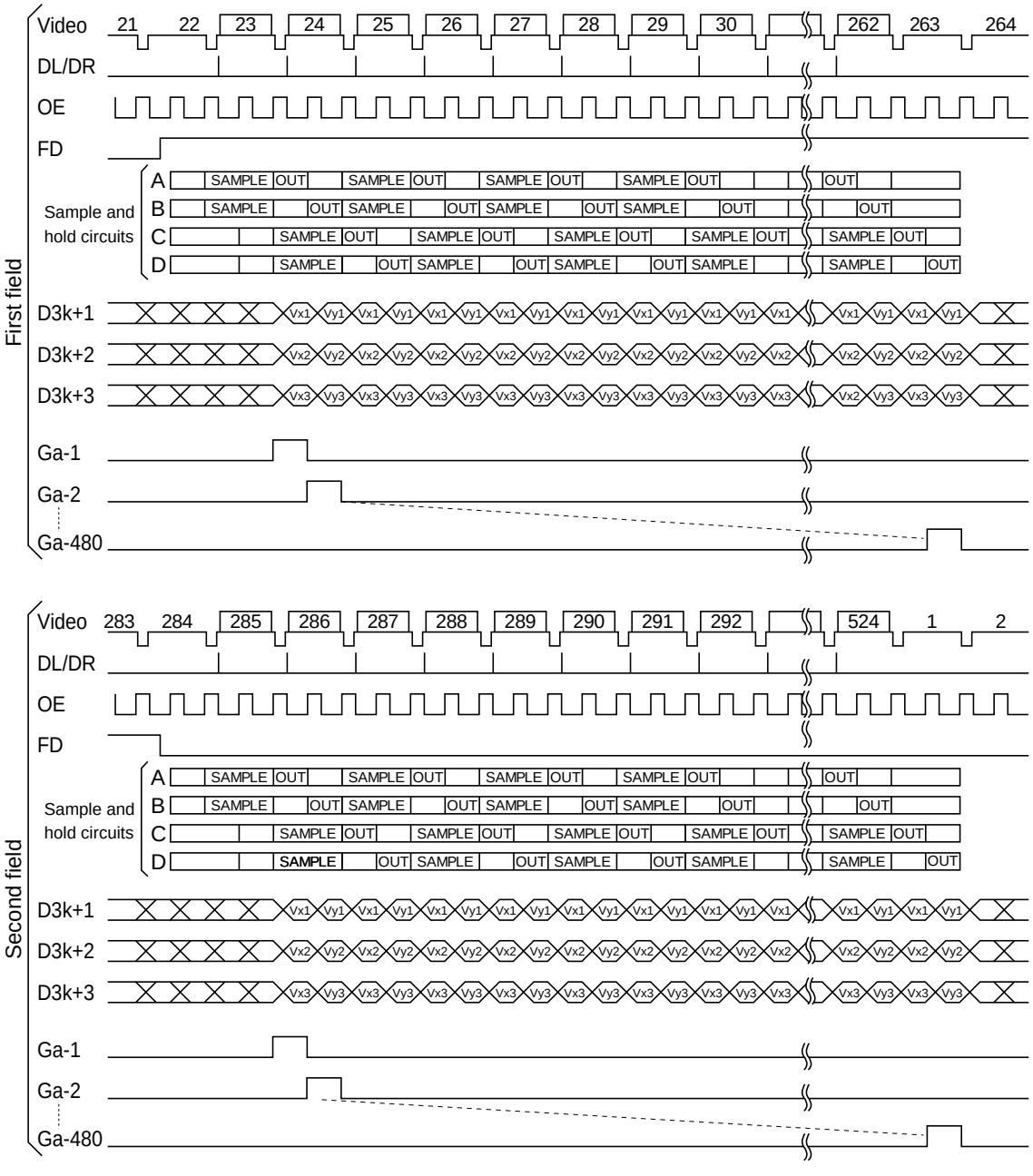
MODE 9	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	GND



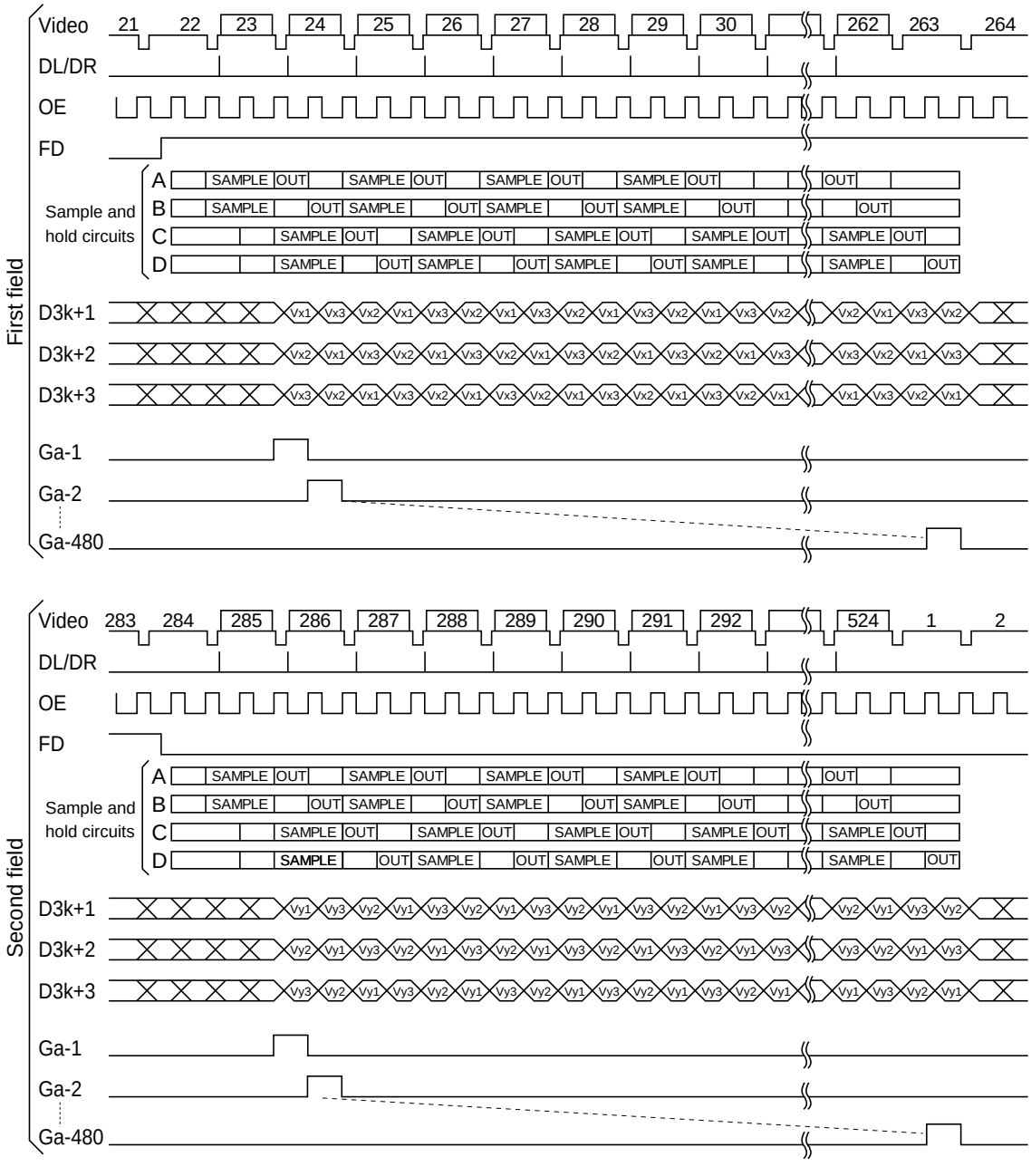
MODE 10	
D/S	V_{CC}
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



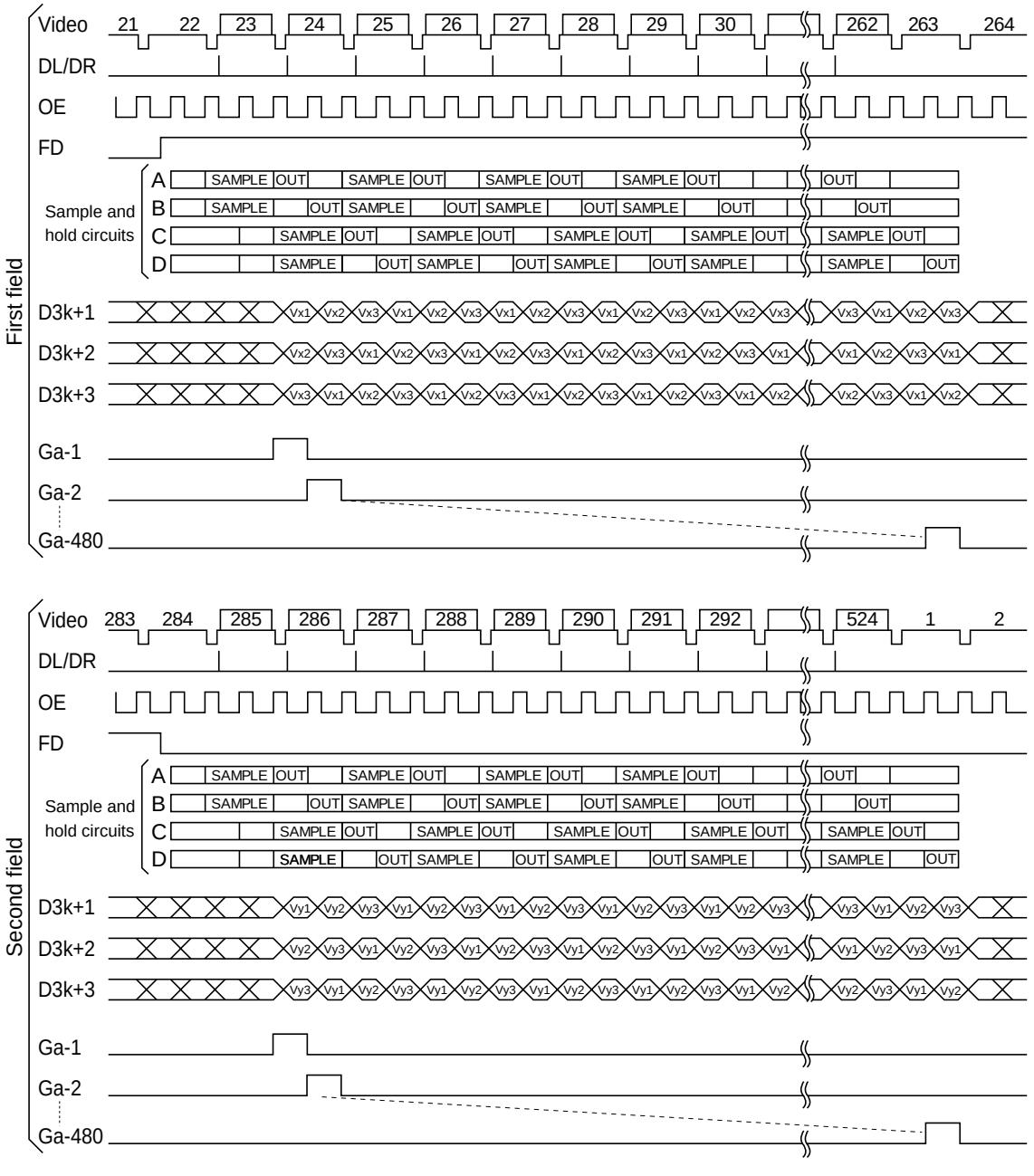
MODE 11	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND



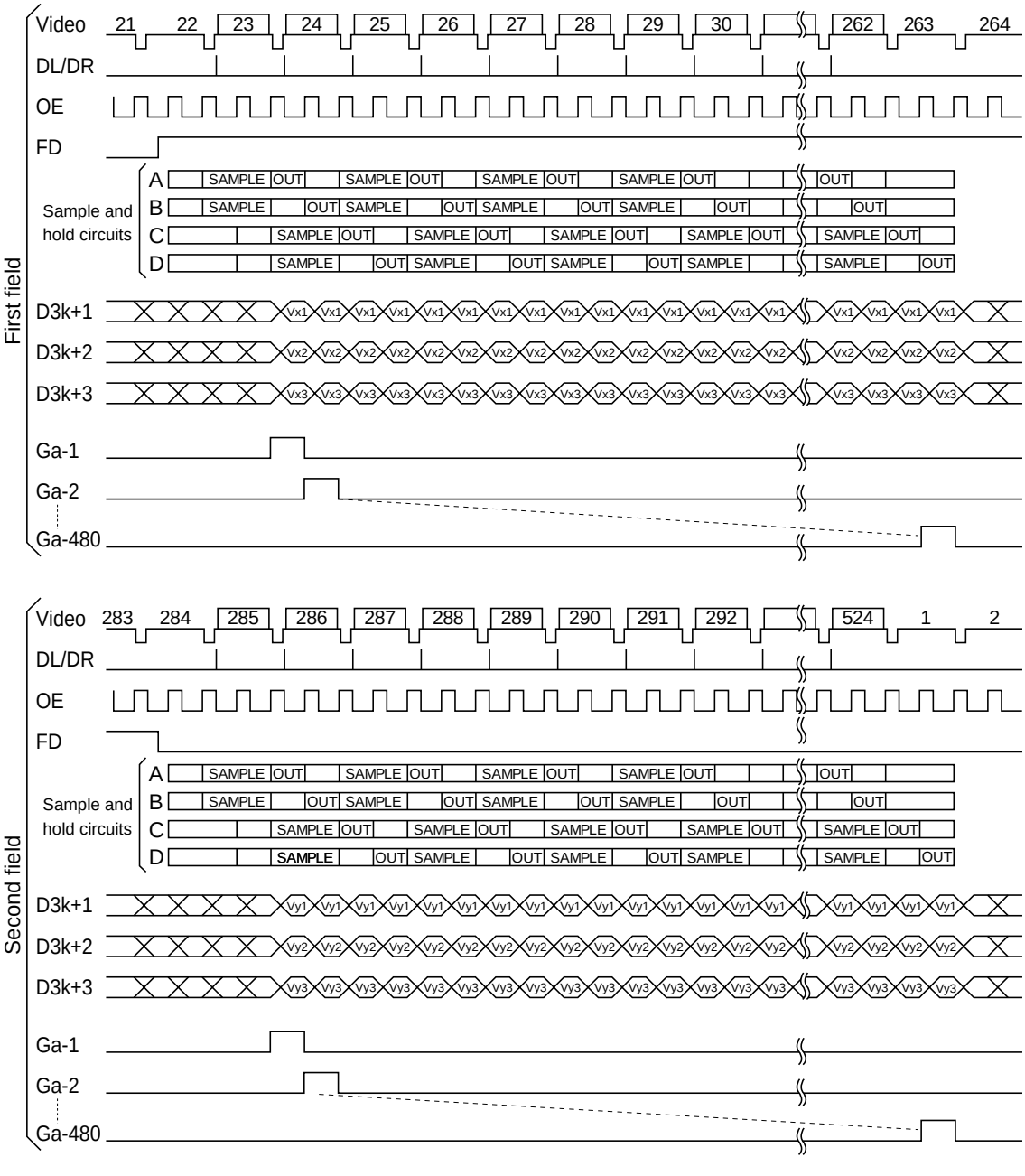
MODE 12	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	V_{CC}



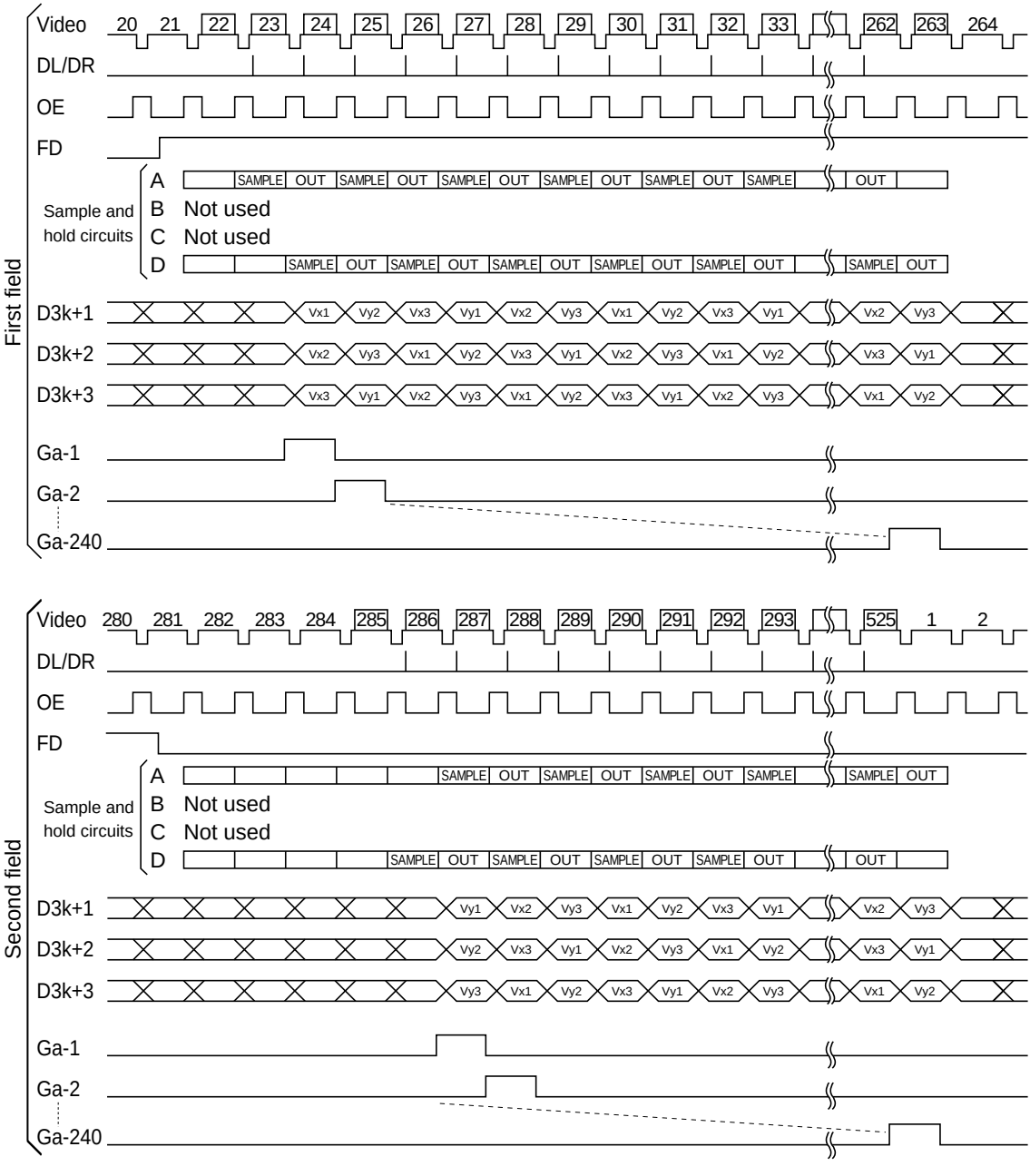
MODE 13	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND



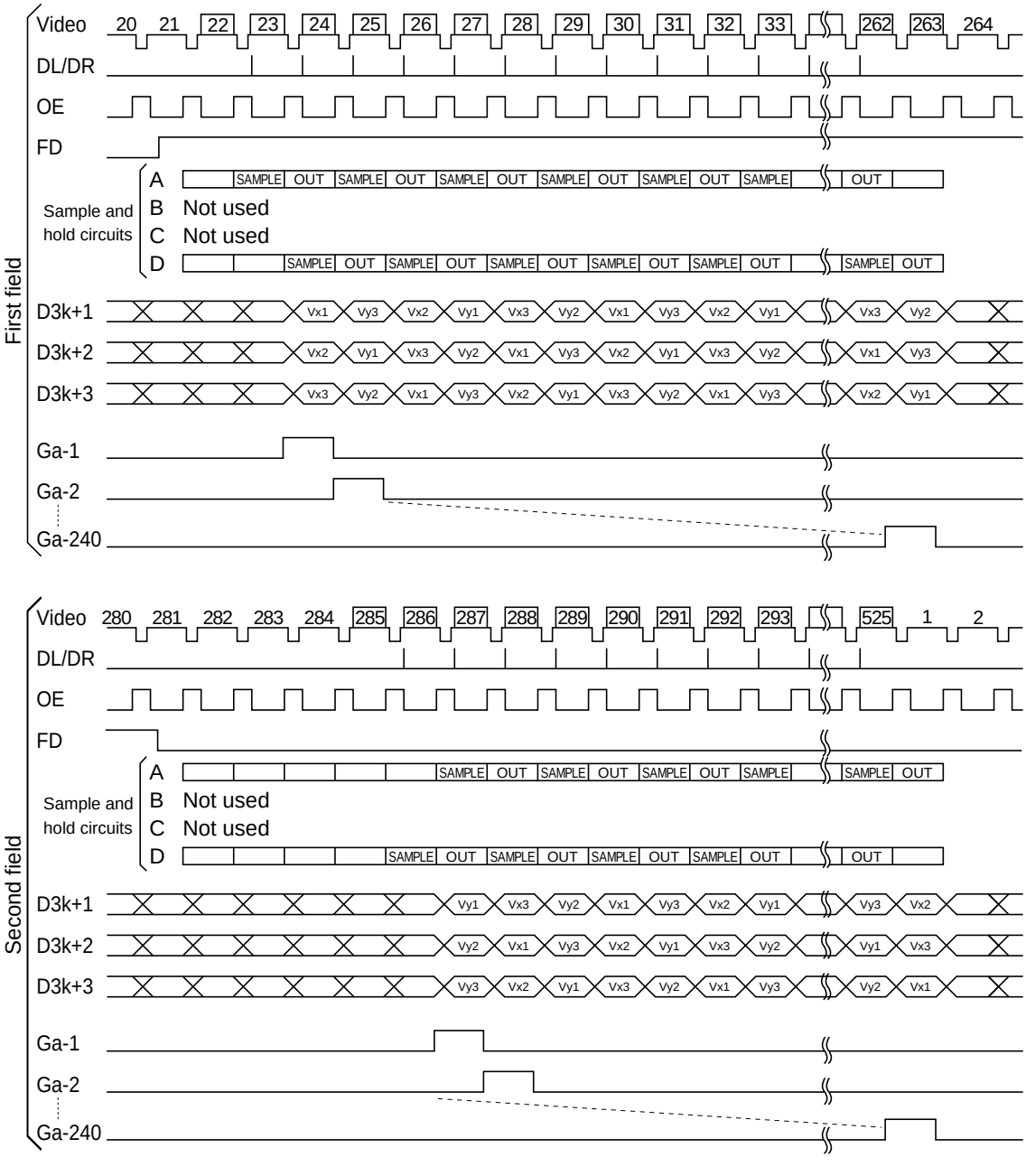
MODE 14	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



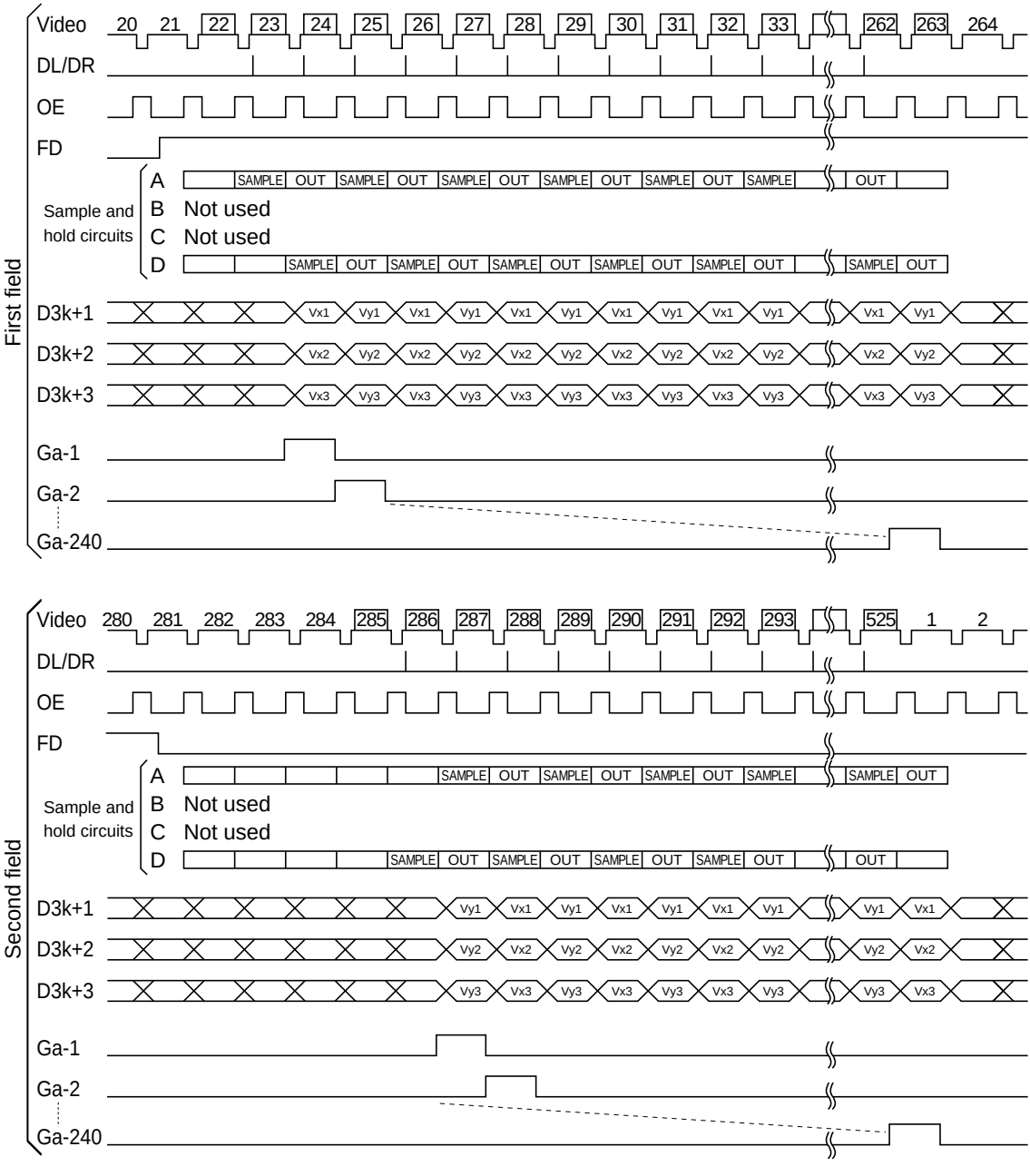
MODE 15	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



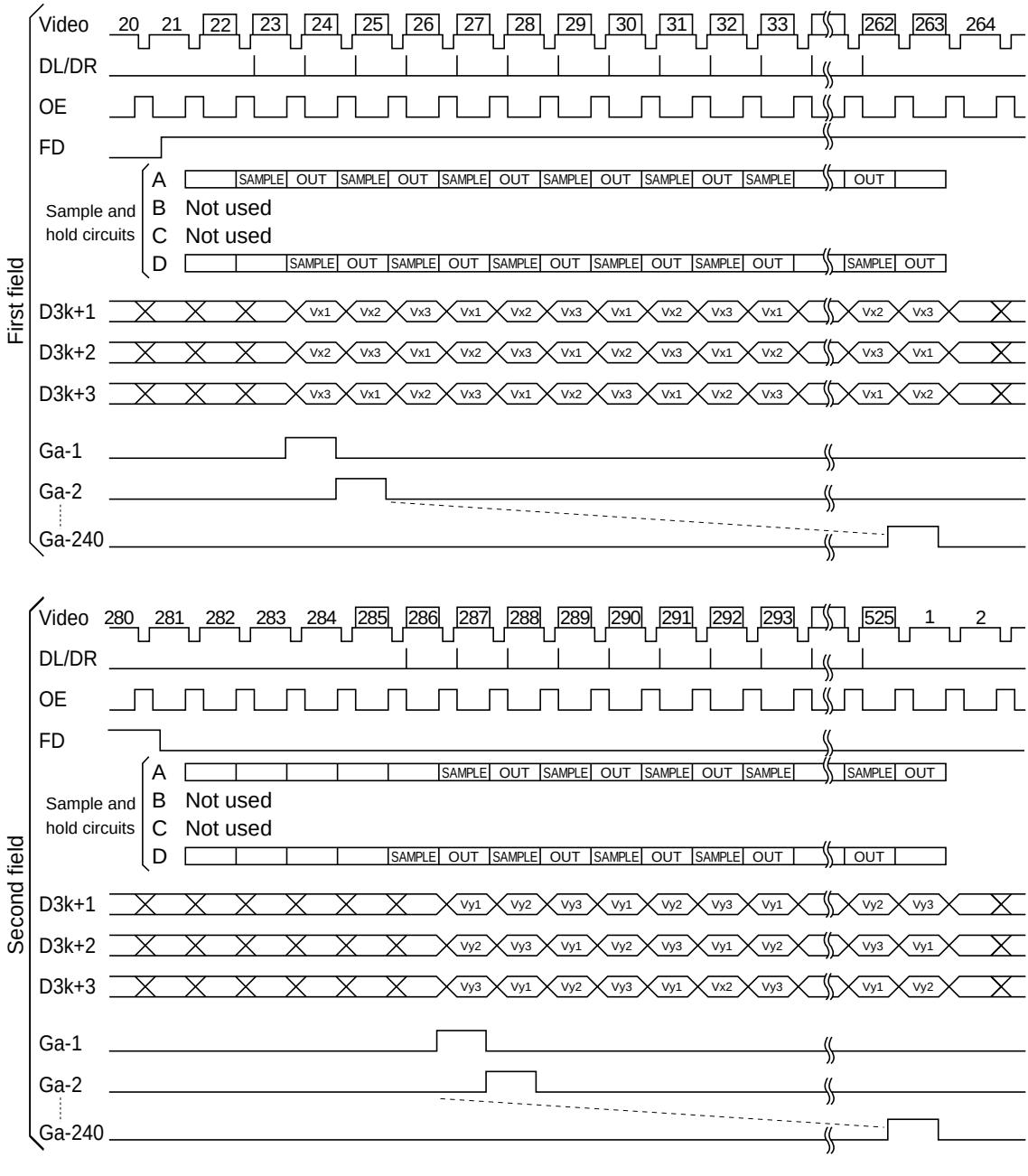
MODE 16	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	GND



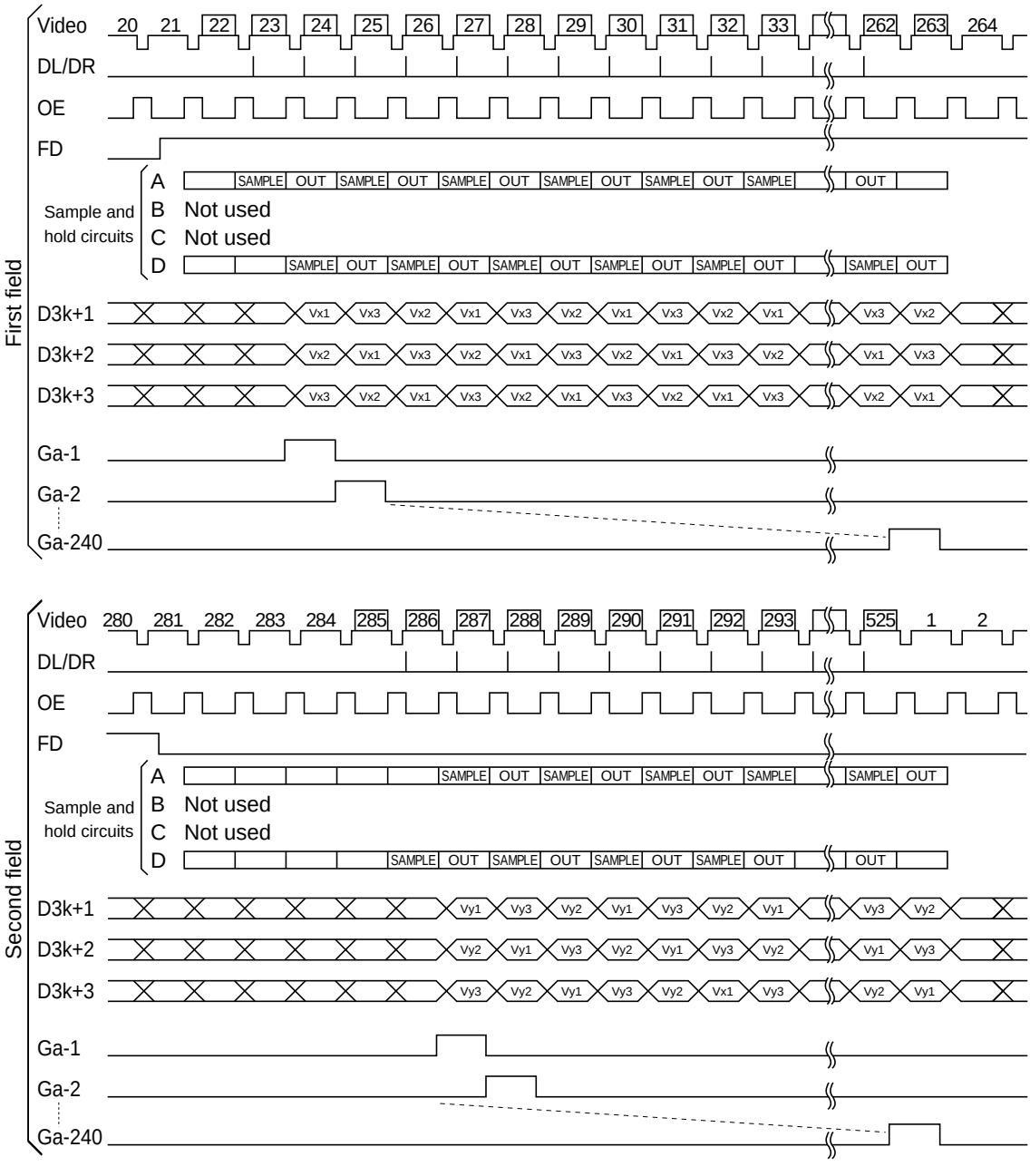
MODE 17	
D/S	GND
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



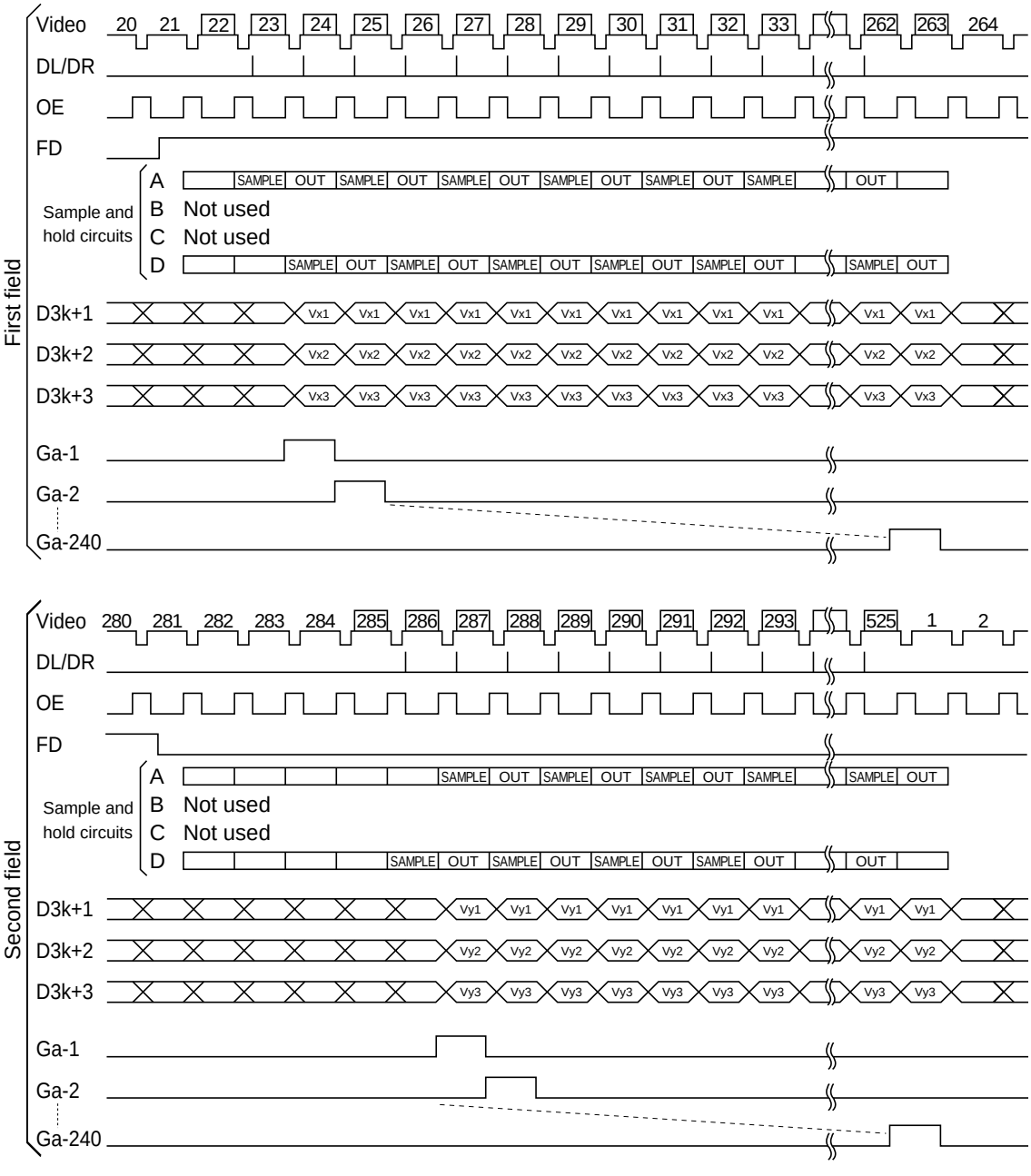
MODE 18	
D/S	GND
L/F	GND
MSF1	GND
MSF2	V_{CC}



MODE 19	
D/S	GND
L/F	GND
MSF1	GND
MSF2	GND



MODE 20	
D/S	GND
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



NTSC System TV Signals and LCD

A TV screen display, which is updated 30 times per second, is called a “frame” and is composed of 525 scanning lines. One frame contains two fields; scanning lines 1 to 262.5 scan the display in the first field, and scanning lines 262.5 to 525 scan the display in the second field to fill the gaps which are left unscanned in the first field. This scanning mode is called an “interlace scan.”

The time period in which one scanning line scans the display is called a “horizontal scanning period” and is about 63.5 µs. Within the horizontal scanning period, the time period that display operation is actually performed is called the “valid display period.” The other period is called the “horizontal retrace period.”

There are two modes for displaying a TV screen image on an LCD panel. In the first mode, each scanning line in the two fields is assigned to one line of the LCD panel; thus, each of the 240 lines of the panel are driven by the positive signal in the first field and by the negative signal in the second field. Here, 30-Hz alternating frequency is available, but the number of vertical pixels is limited to 240.

(Single-rate sequential drive mode)

In the second mode, every other line of the LCD panel can be driven by the first field and the remaining lines can be driven likewise by the second field. In this case, if one pixel of the LCD panel is considered, it is recognized that the pixel is driven by signals with opposite polarity every frame. This lowers the alternating frequency to 15 MHz, which is only half of the frame frequency. Driving LCD elements with signals of such low alternating frequency causes flickering and degrades display quality. To raise the alternating frequency to 30 MHz, a method can be employed in which LCD elements are driven once every field instead of once every frame.

Specifically, in the first field, the first and second lines of the LCD panel are driven respectively during the first half and second half of the complete horizontal scanning period. The same rule is repeated for the following lines. In the second field, on the other hand, the combination of two lines is different. The first line is driven during the second half of the horizontal scanning period, and then the second and third lines are driven respectively during the first and second half of the following horizontal scanning period. The same rule is repeated for the following lines.

Employing this method enables the implementation of 480 vertical pixels.

(Double-rate sequential drive mode)

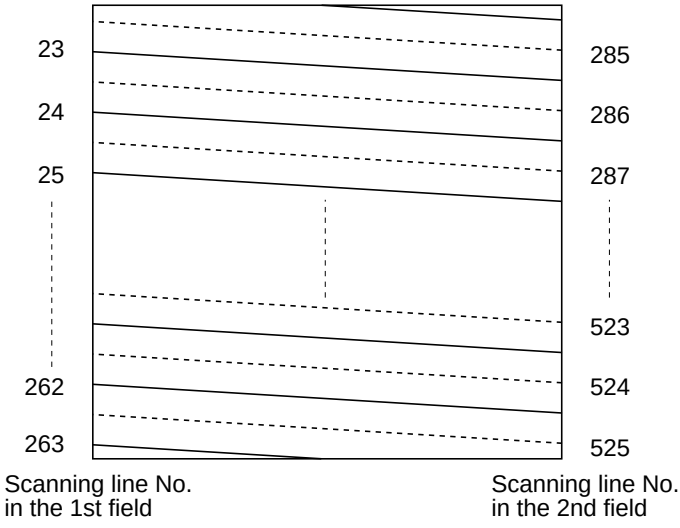


Figure 24 Example of NTSC System TV Signals Scanning

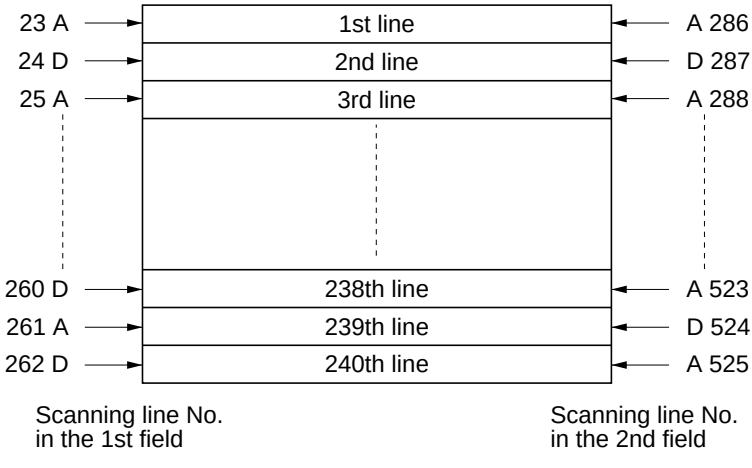


Figure 25 Middle-Resolution Display by Single-Rate Sequential Drive Mode

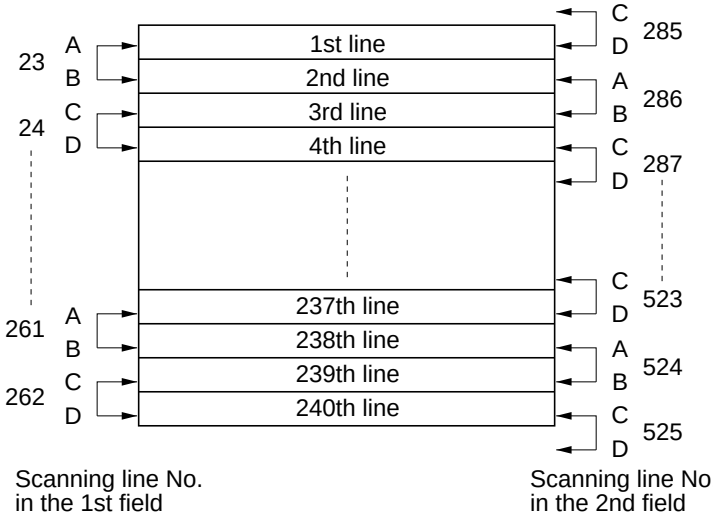


Figure 26 High-Resolution Display by Double-Rate Sequential Drive Mode

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Remarks	Notes
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V		
Power supply for analog unit	V_{BB}	V_{CC}– 23 to V_{CC} + 0.3	V		
Input voltage for logic unit	V_{TC}	–0.3 to V_{CC} + 0.3	V		3
Input voltage for analog unit	V_{TB}	V_{BB}– 0.3 to V_{CC} + 0.3	V		4
Operating temperature	T_{opr}	–20 to +75	°C	Applies to logic circuit	
		–10 to +60	°C	Applies to analog circuit	
Storage temperature	T_{stg}	–40 to +125	°C		
LCD level voltage	V_{LCD}	V_{BB} to V_{CC} + 0.3	V		

Notes: 1. Value referred to GND = 0 V.

2. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
4. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.

Electrical Characteristics

DC Characteristics ($V_{LCD} = V_{CC} = 5$ V ±10%, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, $T_a = -20$ to +75 ˚C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions			Notes
Input high-level voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V				3
Input low-level voltage	V_{IL}	GND	—	0.3V_{CC}	V				
Output high-level voltage	V_{OH}	V_{CC} – 0.4	—	—	V	$-I_{OH}$ = 0.3 mA			4
Output low-level voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.3 mA			
Input leakage current (1)	I_{LI1}	–10	—	+10	µA	V_I = 0 V, V_{CC}			1
Input leakage current (2)	I_{LI2}	–10	—	+10	µA	$V_I = V_{BB}$, V_{CC}			2
Output current (1)	I_{OUT}	—	—	–150	µA	$V_{CC} - V_{BB}$ = 20 V Apply V_{in} to Vx and Vy. $V_{in} = (V_{CC} - V_{BB})/2$ $V_{bo} = V_{CC} - 3$ V $V_{bsH} = V_{CC} - 3$ V $V_{bsB} = V_{CC} - 3$ V	Dk = V_{in} – 0.5 V	OE = V_{CC}	5
		—	—	–10	µA			OE = GND	
Output current (2)	I_{IN}	+150	—	—	µA		DK = V_{in} + 0.5 V	OE = V_{CC}	
		+10	—	—	µA			OE = GND	
Current consumption	I_{GND}	—	—	3.0	mA	f_{ck} = 2.5 MHz, $V_{bo} = V_{CC} - 3$ V $V_{bsH} = V_{CC} - 3$ V, $V_{bsB} = V_{CC} - 3$ V OE = 33 kHz, FD = 30 Hz OE duty = 7/32			6
	I_{BB}	—	15	30	mA				
Bias voltage	V_b	V_{CC} – 4.0	V_{CC} – 3.0	—	V	$V_{bo} = V_{bsH} = V_{bsB}$, C_L = 100 pF, t_{DDR} < 6.3 µs			
Dynamic range	V_{DY}	V_{BB} + 1.5	—	V_{CC} – 3.5	V	$V_{CC} - V_{BB}$ = 20 V, T_a = –10 to +60°C –0.5 V < V_{off} < +0.5 V $V_{bo} = V_{bsH} = V_{bsB} = V_{CC} - 3$ V			5, 7, 9

Item	Symbol	Min	Typ	Max	Unit	Test Conditions		Notes
Offset voltage	$V_{off\ (L)}$	–5 – 180	—	–5 + 180	mV	$V_{CC} - V_{BB}$ = 20 V Ta = –10 to + 60°C f_{ck} = 2.5 MHz $V_{bo} = V_{bsH} = V_{bsB}$ $= V_{CC} - 3$ V	V_{in} = –11 V	5, 8, 9
	$V_{off\ (H)}$	+55 – 180	—	+55 + 180	mV		V_{in} = –1 V	

Notes:
1. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
2. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, and TEST2.
4. Applies to pins DL and DR.
5. Applies to pins D1 to D120.
6. The shift register is constantly shifting one 1.
   Mode setting: L/F = V_{CC}, D/S = V_{CC}, MSF1 = GND, MSF2 = V_{CC}
   (The other input pins must be V_{CC} or GND level.)
7. The operations are the same as those when offset voltage is measured.
8. Definition of “offset voltage” is shown figure 27.
9. These characteristics are defined within the temperature which is shown in the test condition.

AC Characteristics ($V_{LCD} = V_{CC} = 5\ V \pm 10\%$, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, $T_a = -20$ to +75°C)

Item	Symbol	Min	Max	Unit	Test Condition	Notes
Three-phase clock period	t_{CKCK}	210	1000	ns		
Three-phase clock pulse width	t_{CWH} t_{CWL}	100	—	ns		
Interval between three-phase clock falling edge and rising edge	t_{fr1} t_{fr2} t_{fr3}	30	—	ns		1
Interval between three-phase clock rising edge and falling edge	t_{rf}	20	—	ns		2
Clock rise and fall times	t_{ct}	—	30	ns		
DL, DR input setup time	t_{su}	50	—	ns		
DL, DR input hold time	t_{HLI}	20	—	ns		
DL, DR output delay time	t_{pd}	—	90	ns	C_L = 15 pF	
DL, DR output hold time	t_{HLO}	5	—	ns		
OE input period	t_{CYCO}	30	80	µs		
OE input high-level pulse width	t_{OWH}	3	15	µs		
OE rise and fall times	t_{or} t_{of}	—	30	ns		
FD input setup time	t_{FS}	100	—	ns		
FD input hold time	t_{FH}	100	—	ns		

Notes: 1. Necessary for preventing the three-phase shift register from racing.

2. t_{rf} must satisfy the DR and DL input hold time (t_{HLI}) of the next horizontal driver. ($t_{rf} + t_{HLO} > t_{HLI}$)

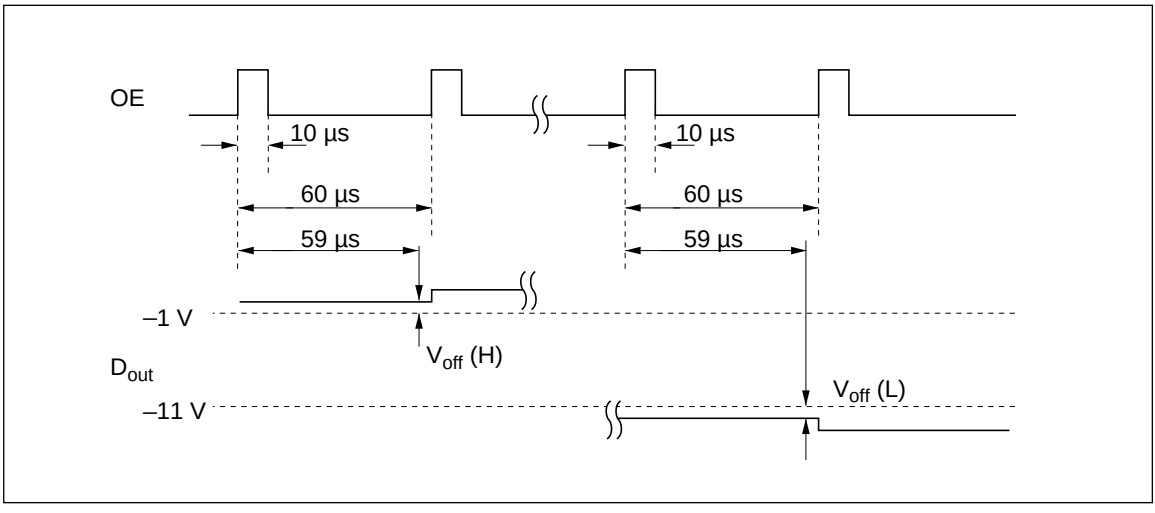


Figure 27 Offset Voltage

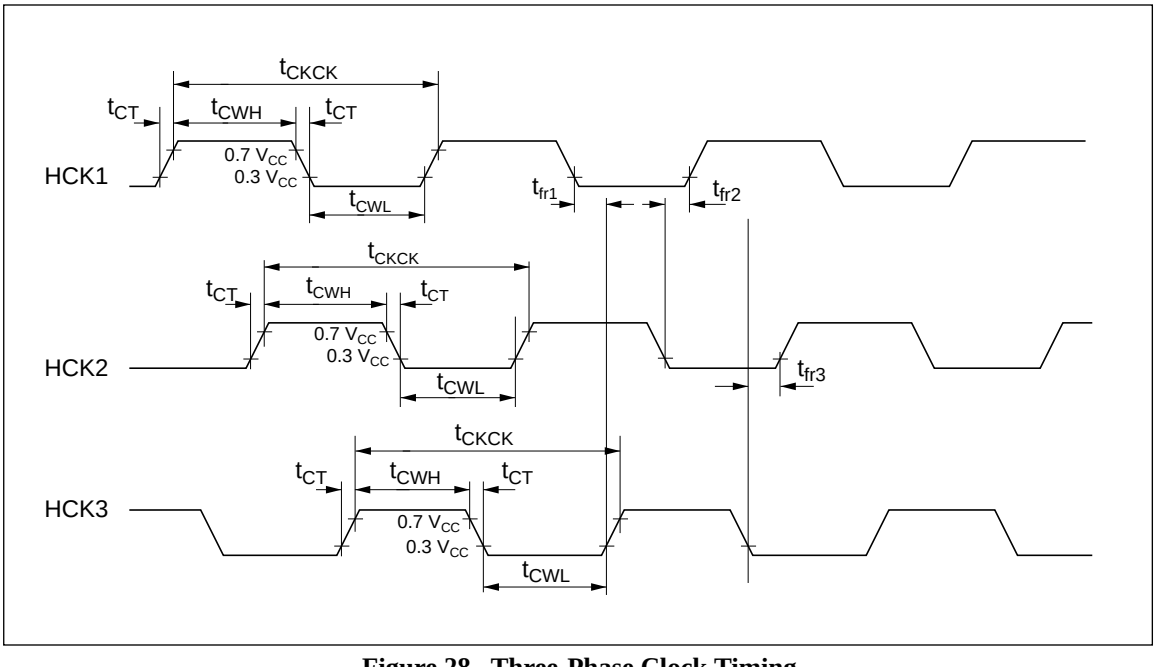


Figure 28 Three-Phase Clock Timing

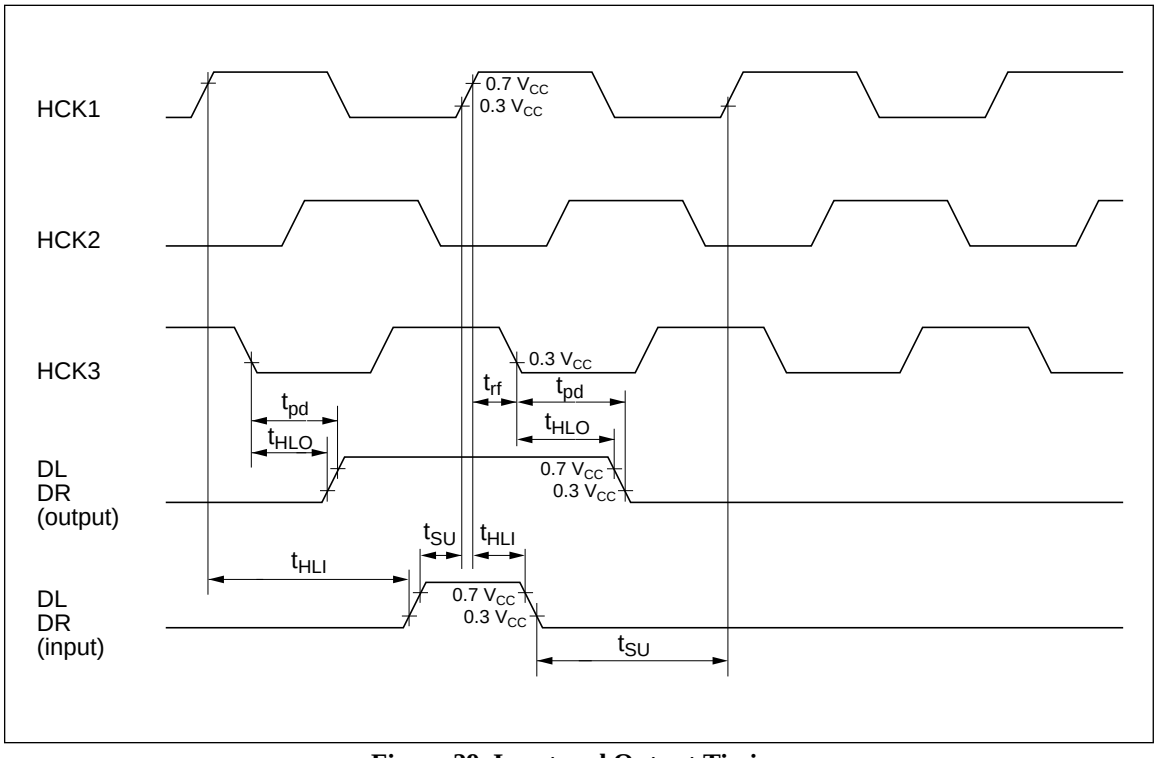


Figure 29 Input and Output Timing

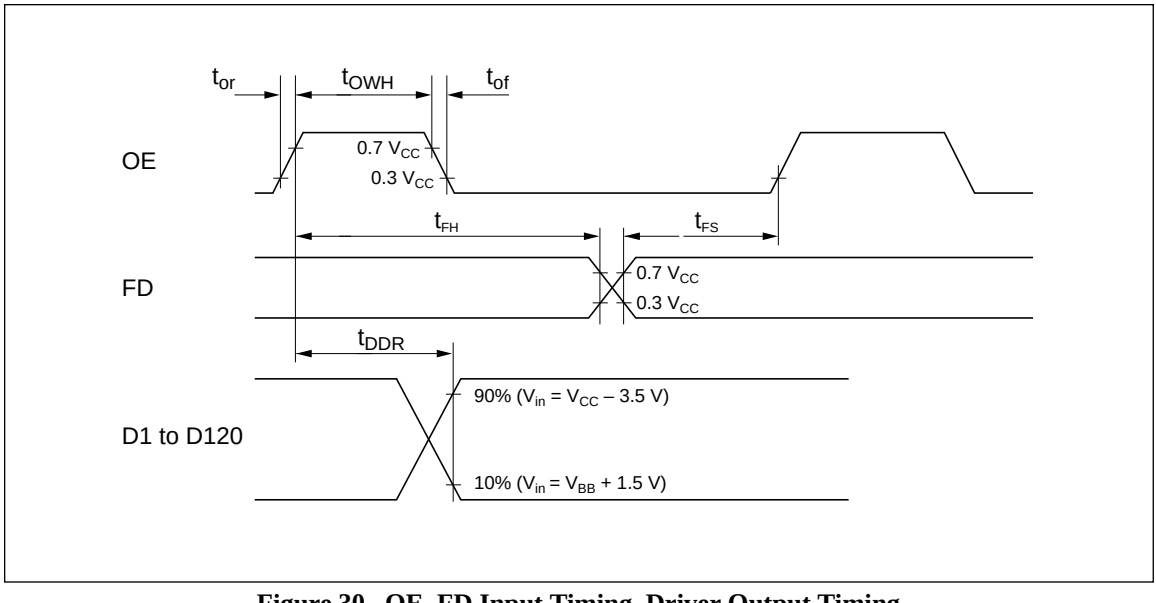


Figure 30 OE, FD Input Timing, Driver Output Timing

HD66310T

TFT-Type LCD Driver for VDT

HITACHI

Description

The HD66310T is a drain bus driver for TFT-type (thin film transistor) LCDs. It receives 3-bit digital data for one dot, selects a level from eight voltage levels, and outputs the level to an LCD.

The HD66310T can drive an LCD panel with an RGBW filter to display a maximum of 4096 colors.

Features

- Full color display: a maximum of 4096 colors
  RGB color filter: 512 colors, 8 gray scales
  RGBW color filter: 4096 colors, 8 gray scales
- High-speed operation
  Number of input data bits: 3 bits × 4
  Maximum operation clock frequency:
  — 12 MHz (HD66310T00)
  — 15 MHz (HD66310T0015)
  Maximum pixels: 480 × 640 dots
- 160 internal driver circuits
- Bidirectional shift
- Internal chip enable signal generator
- Stand-by function
- LCD driving voltage: 15 V to 23 V
- CMOS process

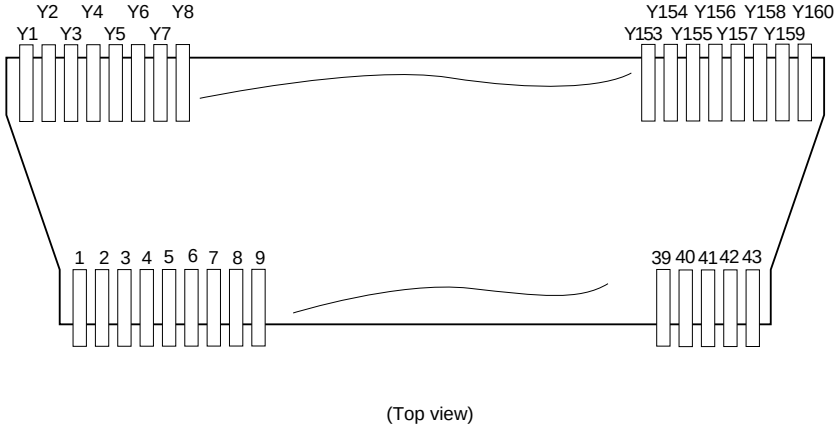
Ordering Information

Type No.	Max. Operating Clock Frequency	Power Supply for Logic Unit	Operating Temperature	Package
HD66310T00	12 MHz	5 V ± 10%	–20 to +75°C	203-pin TCP
HD66310T0015	15 MHz	5 V ± 5%	–20 to +65°C	

Note: The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Pin Arrangement



(Top view)

1	V0L	22	DMY1
2	V1L	23	D20
3	V2L	24	D21
4	V3L	25	D22
5	V4L	26	D23
6	V5L	27	DMY2
7	V6L	28	CL1
8	V7L	29	CL2
9	V_{CC1}	30	BS
10	V_{CC2}	31	SHL
11	EIO1	32	EIO2
12	$\overline{RVS}$	33	TEST
13	D00	34	GND
14	D01	35	V_{EE}
15	D02	36	V7R
16	D03	37	V6R
17	DMY0	38	V5R
18	D10	39	V4R
19	D11	40	V3R
20	D12	41	V2R
21	D13	42	V1R
		43	V0R

Note: This does not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Functions (Refer to)
$V_{CC}1$, $V_{CC}2$	2	Power supply	1.
GND	1	Power supply	
V_{EE}	1	Power supply	
V0L–V7L, V0R–V7R	16	Power supply	2.
CL1	1	Input	3.
CL2	1	Input	4.
D00, D10, D20, to D03, D13, D23	12	Input	5.
$\overline{RVS}$	1	Input	6.
SHL	1	Input	7.
EIO1, EIO2	2	Input/output	8.
TEST, BS	2	Input	9.
Y1–Y160	160	Output	10.
DMY0–DMY2	3	—	11.

Pin Functions

1. $V_{CC}1$, $V_{CC}2$, GND, V_{EE}: These pins are used for the power supply.

V_{CC}–GND: Power supply of low voltage
V_{CC}–V_{EE}: Power supply of high voltage

2. V0L–V7L, V0R–V7R: 8-level LCD driving voltage is applied to these pins. One of the eight levels is selected according to the value of the 3-bit input display data. The L and R pins of the same voltage level are connected in the driver.

3. CL1: Inputs clock pulses, which determine the output timing of the LCD driving voltage. The output changes at the CL1 rising edge.

4. CL2: Inputs clock pulses, which determine the input timing of display data. The driver samples data at the CL2 falling edge.

Table 1 Voltage Level Selection According to Display Data Value

Display Data			Voltage Level	
D2j	D1j	D0j	$\overline{RVS}$ = 1	$\overline{RVS}$ = 0
0	0	0	V0	V7
0	0	1	V1	V6
0	1	0	V2	V5
0	1	1	V3	V4
1	0	0	V4	V3
1	0	1	V5	V2
1	1	0	V6	V1
1	1	1	V7	V0

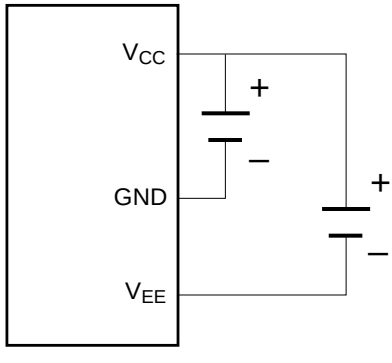


Figure 1 Power Supply for the Device

5. D00–D03, D10–D13, D20–D23: Input display data. See table 1 for the voltage level selection by the display data.

6. $\overline{\text{RVS}}$: Determines if logical I/O display data is reversed. Display data is reversed when $\overline{\text{RVS}}$ is low.

7. SHL: Selects the shift direction of display data.

8. EIO1, EIO2: Inputs/outputs chip enable signals. The SHL signal selects which pin is for input or output. When the chip enable input signal is low, data input starts. When display data corresponding to 160 outputs are input, the chip enable output signal changes from high to low.

9. TEST, BS: Used for test purposes only. Connect to a low level for normal operation.

10. Y1–Y160: Output LCD driving signals.

11. DMY0–DMY2: Reserved pins that should be left open.

Table 2 Input/Output Selection for EIO1 and EIO2

SHL	EIO1	EIO2
GND	Input	Output
V_{CC}	Output	Input

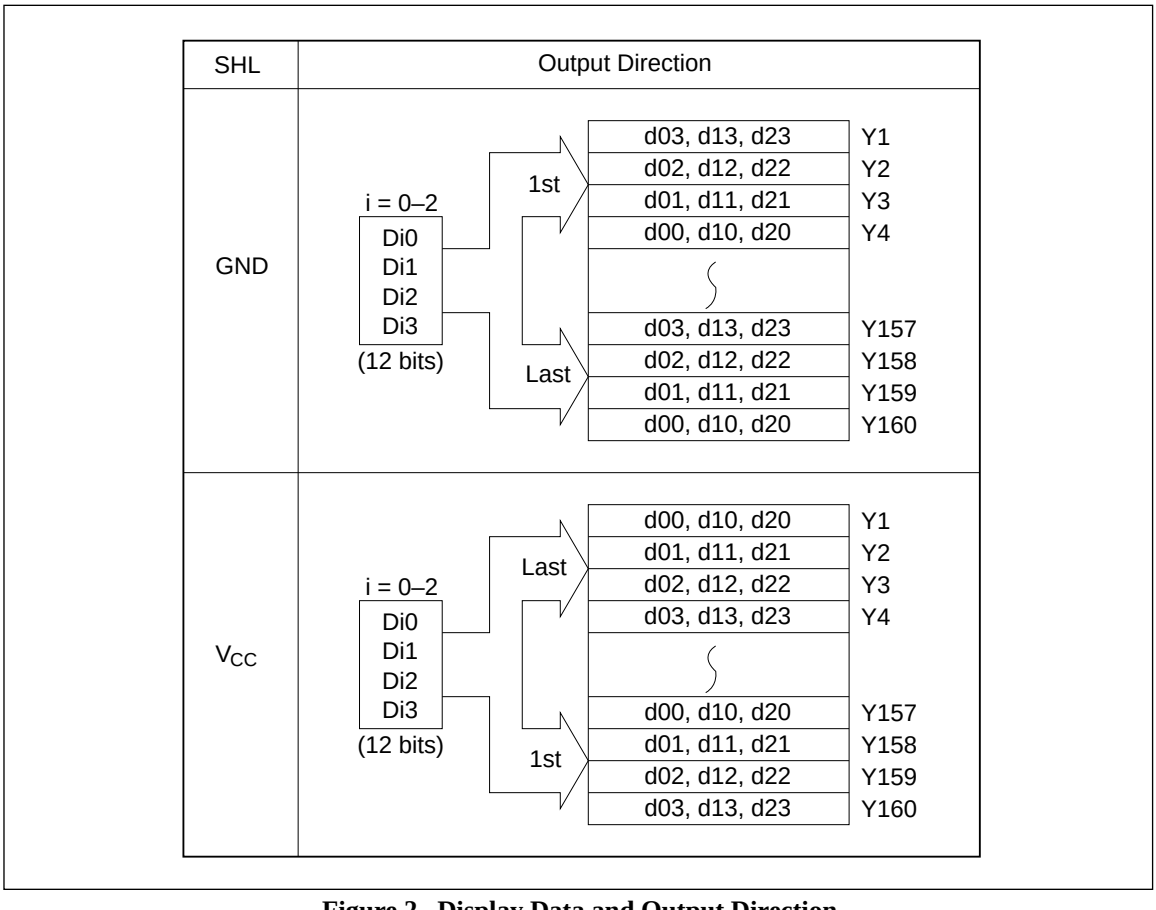
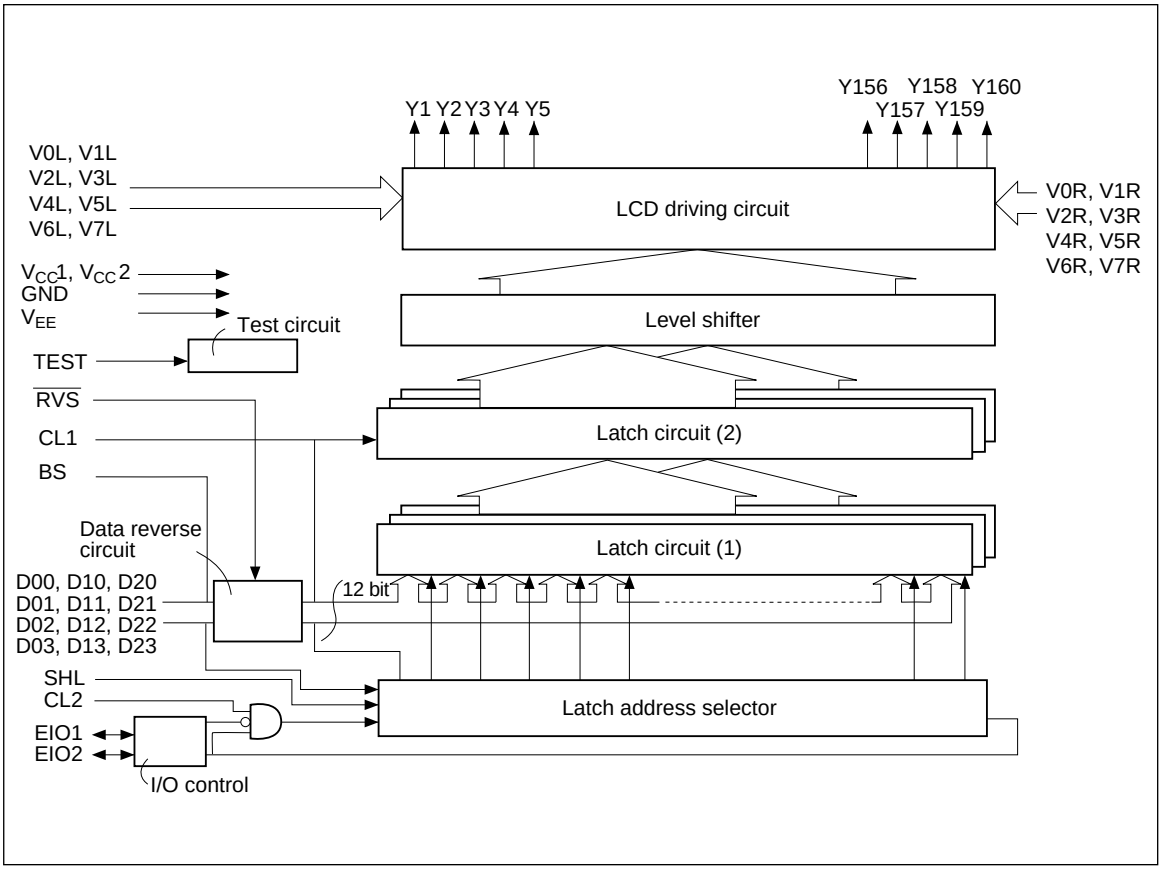


Figure 2 Display Data and Output Direction

Internal Block Diagram



Block Functions

Latch Address Selector: Contains a 6-bit up/down counter and a decoder, and sends the latch signals to latch circuit (1) at the CL2 falling edge.

Data Reverse Circuit: Reverses the input display data when $\overline{RVS}$ = 0, and does not reverse data when $\overline{RVS}$ = 1.

Latch Circuit (1): Consists of three planes of 160-bit latch circuit. Each bit of 3-bit data is separately latched in its corresponding plane depending on its significance. Each plane is divided into forty 4-bit blocks, and all four bits are latched into the block at once, as specified by the latch signal from the address selector. In total, the 3-plane circuit latches 12 bits of data at one time.

Latch Circuit (2): Consists of three planes of 160-bit latch circuit, which latches the data from latch circuit (1) at the timing determined by CL1, and holds the data for one line scanning period.

Level Shifter: Raises the driving voltage of 5 V to the appropriate LCD driving voltage.

LCD Driving Circuit: Outputs an 8-level LCD driving voltage. This circuit receives 3-bit data for one dot from latch circuit (2) and selects one level from eight voltage levels.

Test Circuit: Generates test signals.

System Configuration

A block configuration of the TFT-type color display system using the HD66310T is shown in figure 3.

The HD66310T receives 3-bit data for one pixel and selects one of the eight LCD driving voltage levels to send to the LCD. The LCD driving output circuit, which is produced by the CMOS structure, can use any LCD driving voltage level from V_{CC} to V_{EE}. When the LCD panel uses an RGB color filter (the Triad arrangement), 512 (8^3) colors can be displayed. When using an RGBW color filter (the Quad arrangement), 4096 (8^4) colors can be displayed.

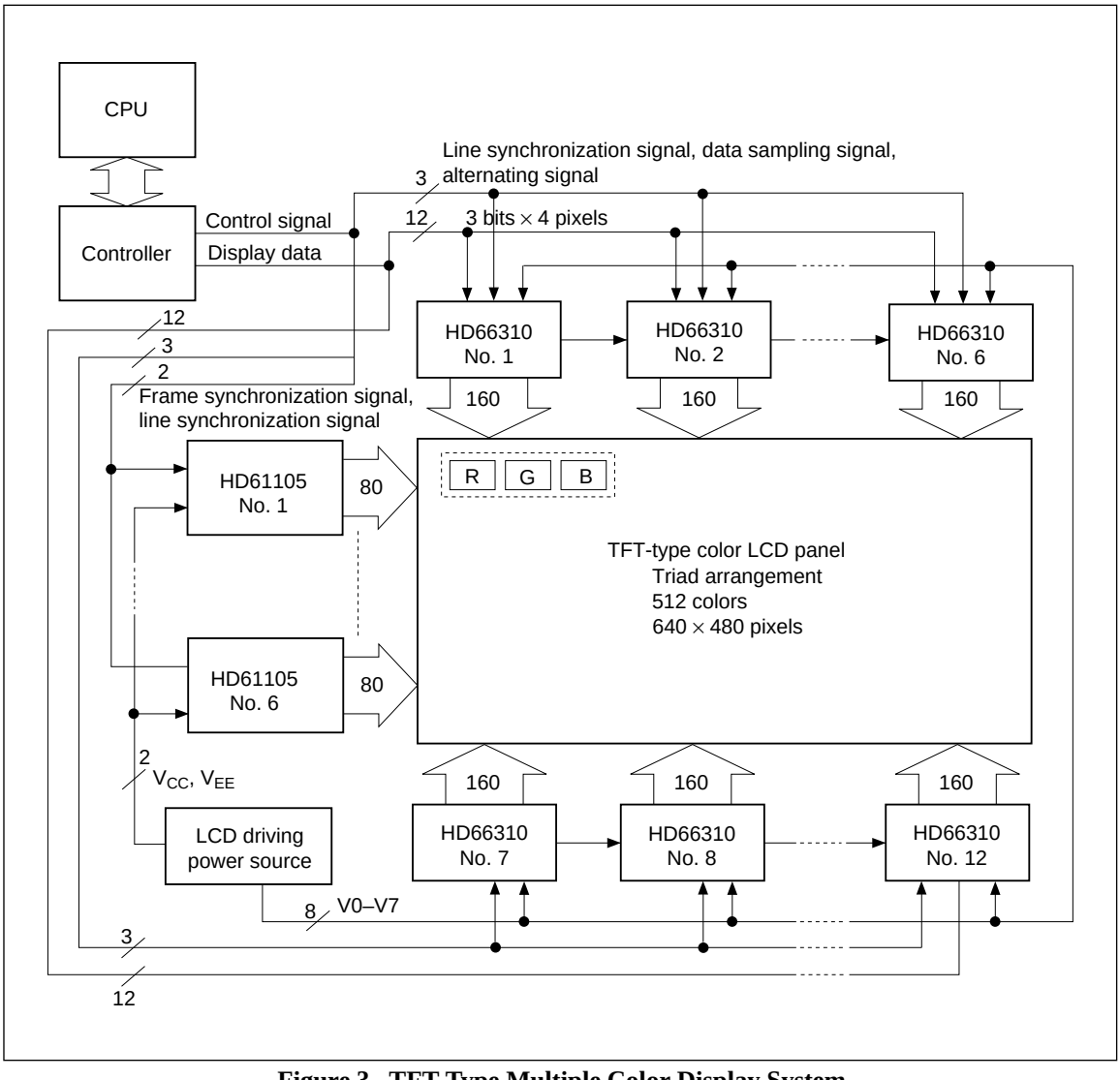


Figure 3 TFT-Type Multiple Color Display System

Internal Operation

8-Level Output

The HD66310 internal circuit unit for one data output is shown in figure 4. The circuit receives 3-bit data (D0j, D1j, D2j) and selects one of eight voltage levels (V0–V7) to output to the LCD.

The transfer gates of the output circuit are produced by the CMOS structure. Therefore, any voltage level between V_{CC} to V_{EE} can be applied to lines V0 to V7.

The HD66310 has 160 of the above circuits.

Operation Timing

The HD66310 operation timing is shown in figure 5.

When the SHL signal is at the GND level, data input is started by a low EIO1 (data input enable) signal. At the CL2 falling edge, 12 bits of data, which are for four outputs (3 bits for gray scales × 4 outputs), are input together. When the data input corresponding to 160 outputs are completed, the HD66310 automatically enters the stand-by mode, and the EIO2 signal changes to low.

The LCD driving output changes at the CL1 rising edge. The voltage level selected by data d1 is output from pin Y1, and the level selected by d160 is output from Y160. See table 1 for the voltage level selection by the input data.

When the SHL signal is at the V_{CC} level, data input is started by a low EIO2 signal. When the data input for 160 outputs are completed, the EIO1 signal changes to low. The voltage level selected by data d1 is output from pin Y160, and the level selected by d160 is output from Y1.

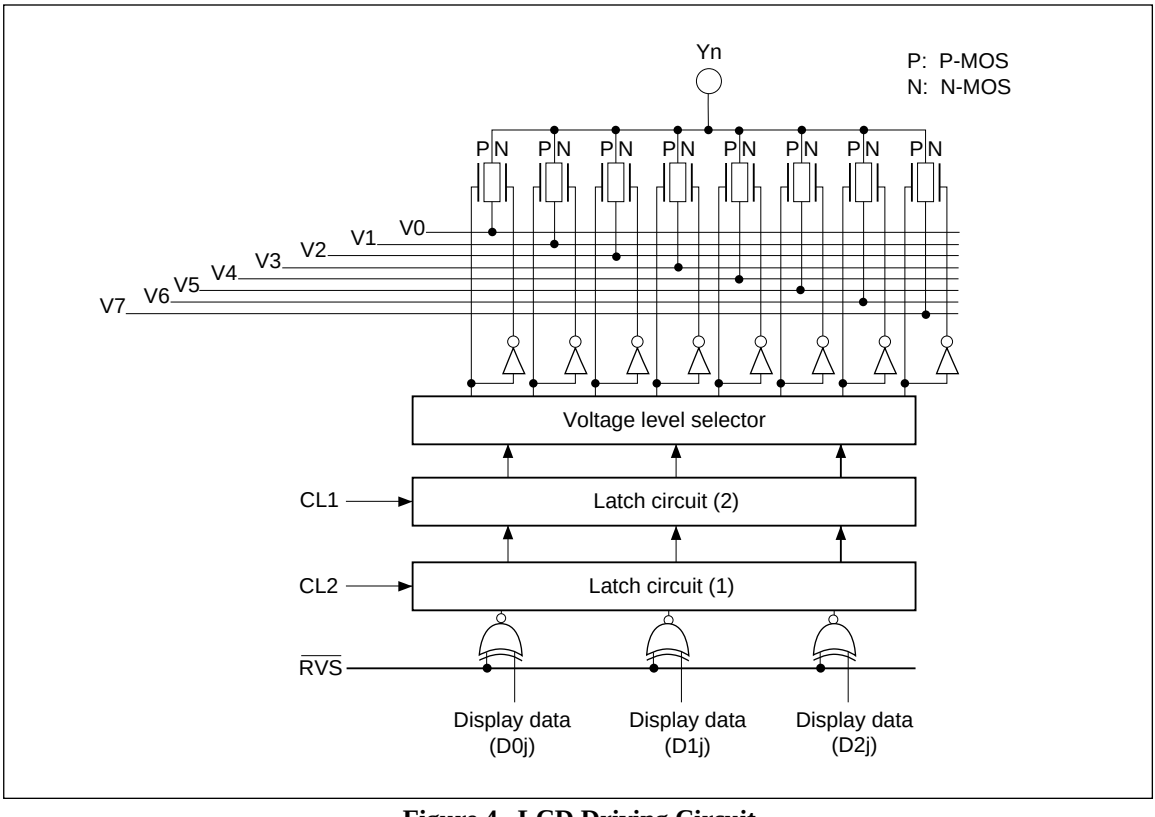


Figure 4 LCD Driving Circuit

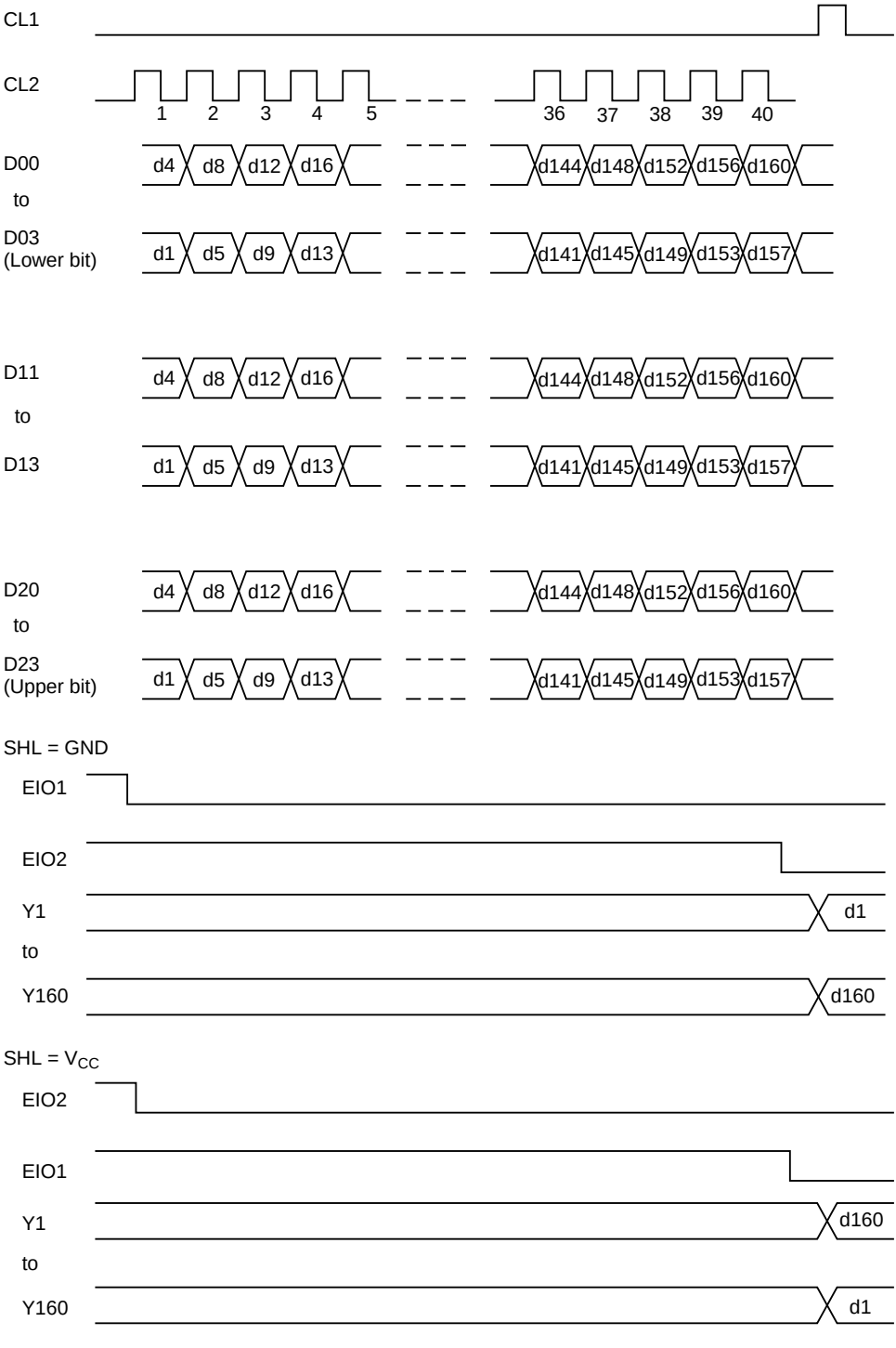


Figure 5 Basic Operation Timing Chart

Cascade Connection

When the SHL signal is at the GND level, the HD66310 begins to input data when the EIO1 signal goes low. When the data input is completed, the EIO2 signal changes to low. By connecting the EIO2 pin of the first HD66310 to the EIO1 pin of the next HD66310, the low EIO2 signal activates the next HD66310. Figure 6 shows a connection example.

When the SHL signal is at the VCC level, the EIO2 pin of the first HD66310 is connected to GND, and the EIO1 pin is connected to the next HD66310 EIO2 pin.

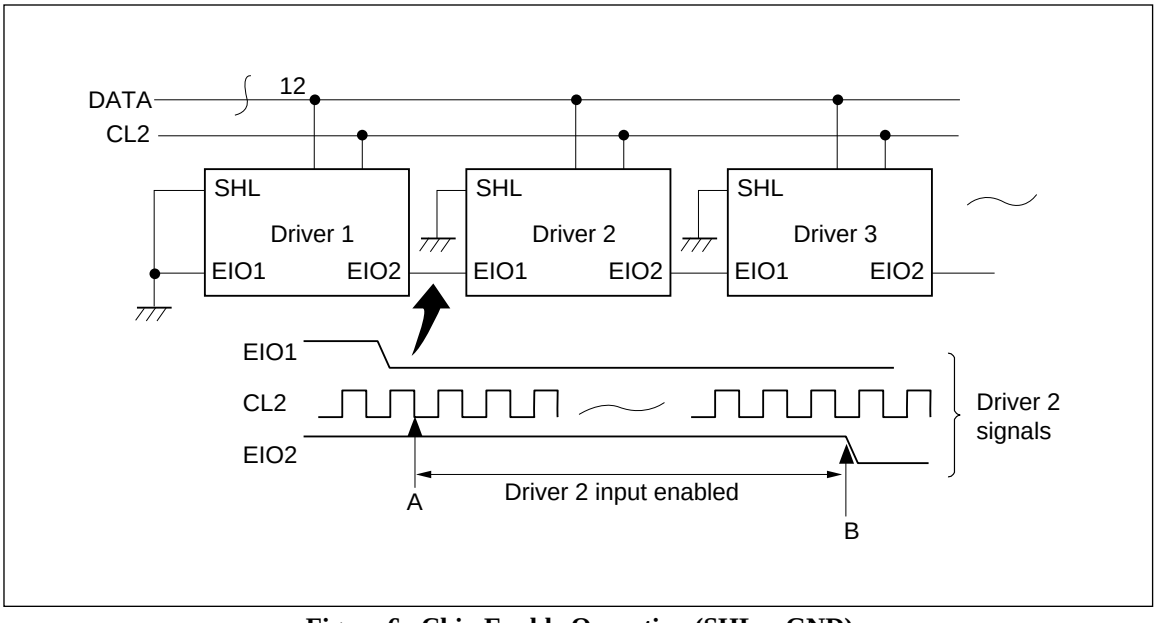


Figure 6 Chip Enable Operation (SHL = GND)

LCD Driving Power Supply Circuitry

Multiple-Level Driving Voltage Method

AC voltage must be applied to the LCD, since DC voltage deteriorates the LCD. To display eight gray scales, 16 voltage levels, shown in figure 7, must be applied.

Although the HD66310 has eight LCD driving voltage input levels, it can output 16 driving voltage levels using the level selector shown in figure 8, since the transfer gates of the output circuit are produced by the CMOS structure.

External Power Supply Circuitry

Figures 8 and 9 show the external power supply circuit when displaying 512 colors in the Triad arrangement, and figure 10 shows the circuit for displaying 64 colors in the Triad arrangement. Table 3 shows the specifications of the LCD panel and the HD66310 pins for each power supply circuit.

The circuit shown in figure 8 is the basic one used when displaying 512 colors in the Triad arrangement. However, the HD66310 can dispense with the level selector, as shown in figure 9, using the internal $\overline{RVS}$ (output reverse) pin. See table 1 for detailed $\overline{RVS}$ functions.

When displaying 64 colors in the Triad arrangement, the $\overline{RVS}$ pin functions as the alternating signal input pin, as shown in figure 10.

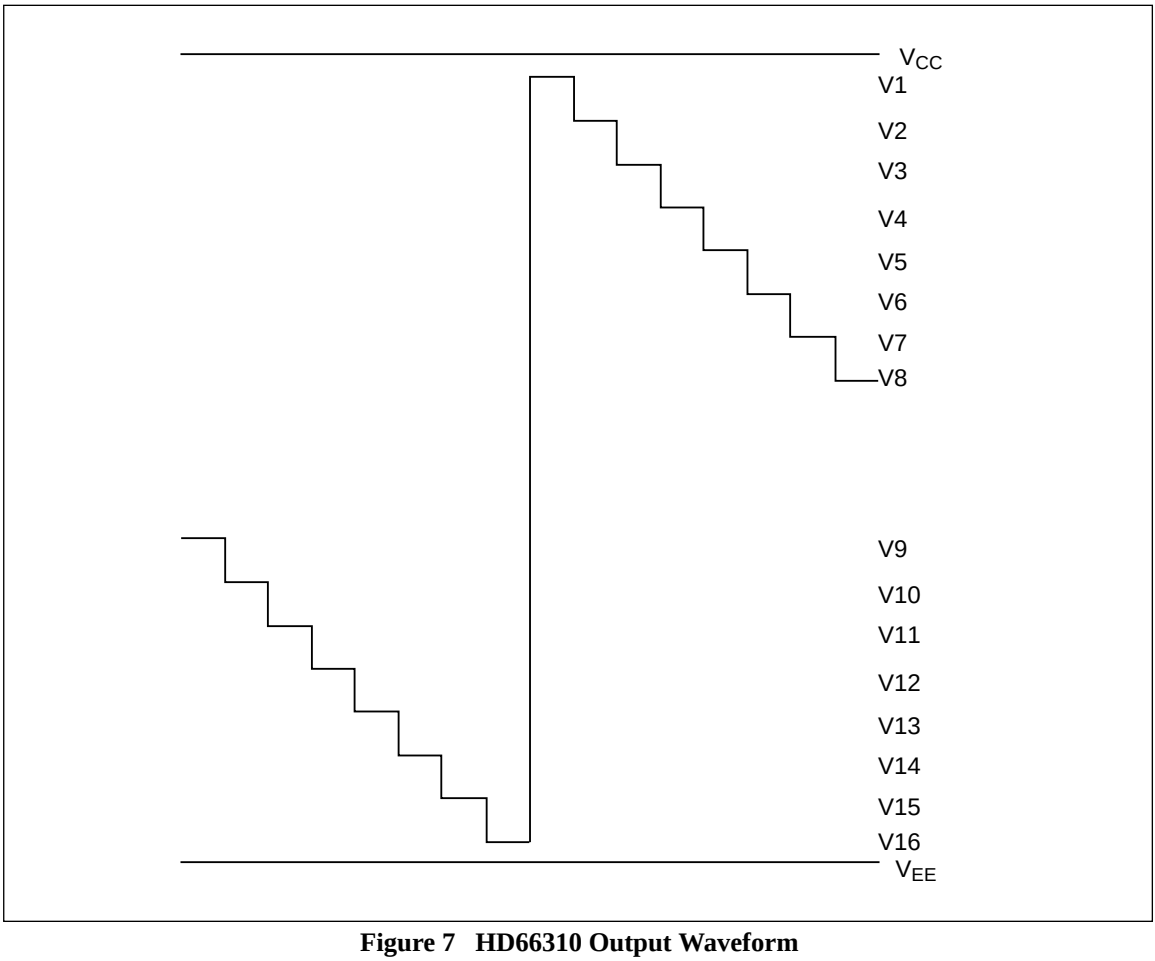


Figure 7 HD66310 Output Waveform

Table 3 Color Display and Pin Specifications

Output Level	Panel Spec.	Display Data Di2	Di1	Di0	$\overline{RVS}$ pin	Power Supply (Refer to)
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	1	Fig. 8
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	Alternating signal	Fig. 9
4 × 2 (AC)	Quad: 256 colors Triad: 64 colors	1	1/0 (upper bit)	1/0 (lower bit)	Alternating signal	Fig. 10

1: V_{CC} level voltage
0: GND level voltage

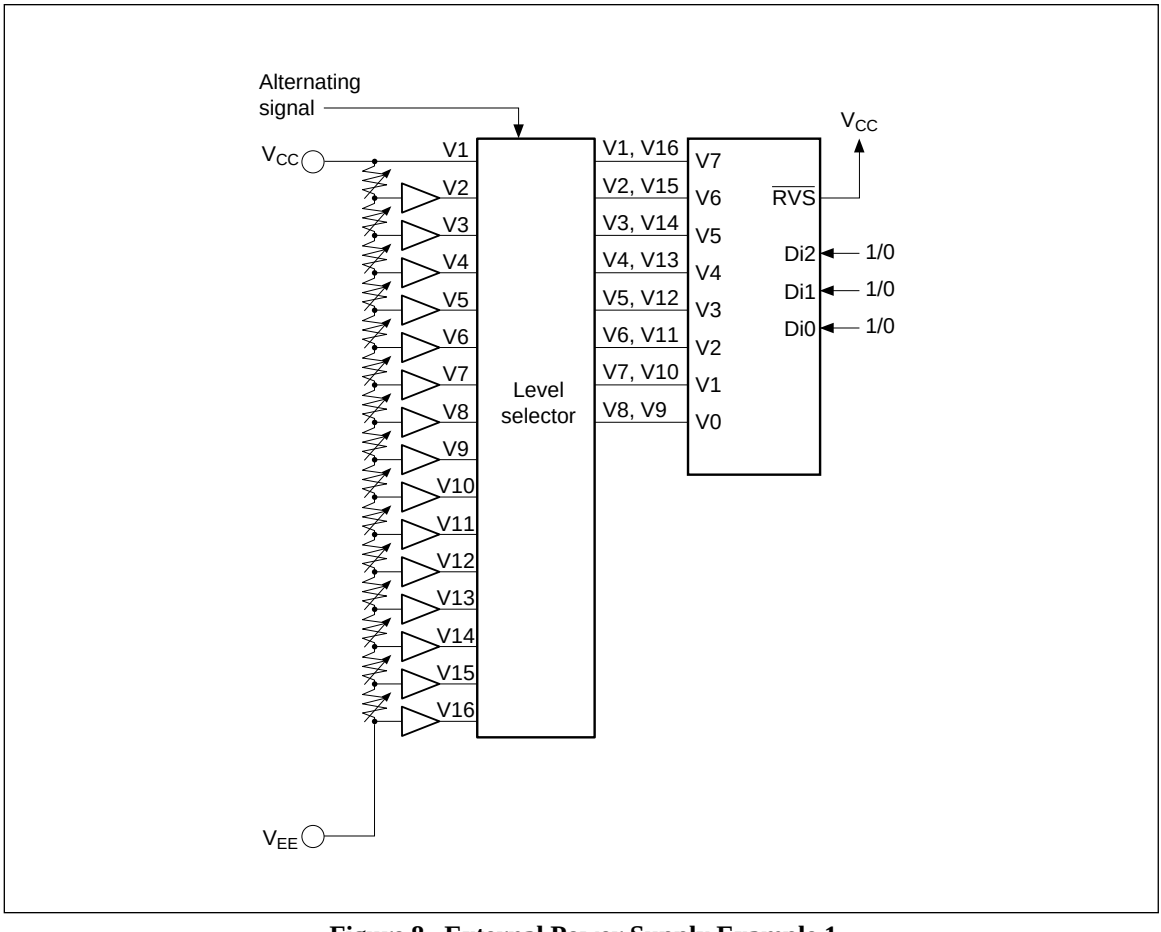


Figure 8 External Power Supply Example 1

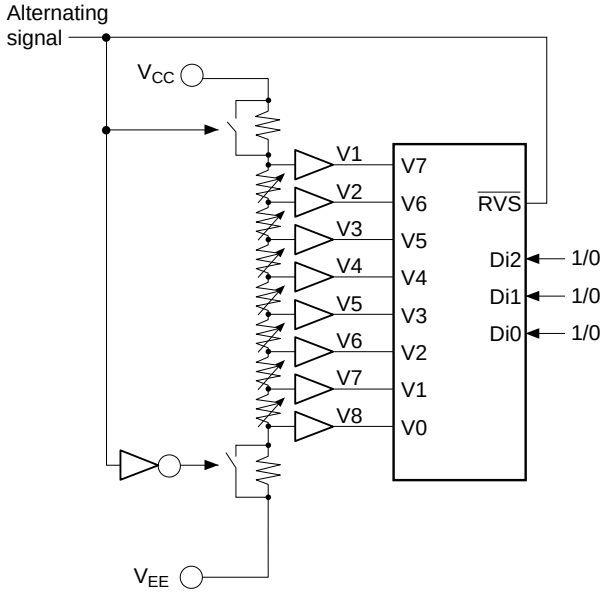


Figure 9 External Power Supply Example 2

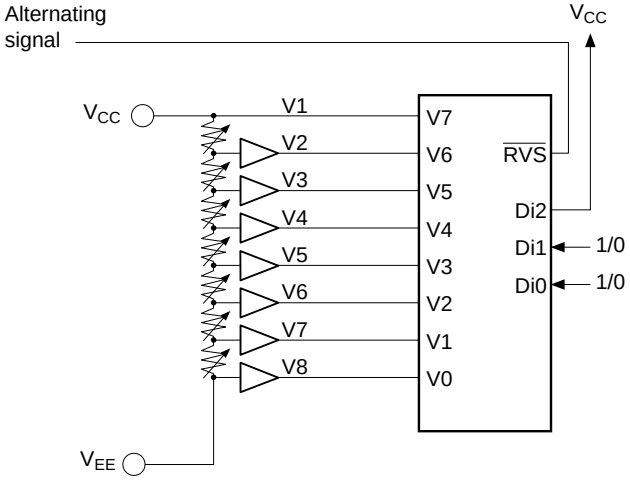


Figure 10 External Power Supply Example 3

Design for Timing

When using the RVS pins to simplify the power source, as shown in figures 9 and 10, it is recommended to add a vertical retrace period, (a scanning period in which no scan electrode is selected) at the end of a frame scanning period, as shown in figure 12, for the following two reasons.

- As shown in figure 4, the data reverse circuit is before the latch circuit (1). The LCD driving output is reversed one CL1 period after a transition of the $\overline{RVS}$ signal, as shown in figure 11. However, the power supply lines immediately reverses polarity after a transition of the $\overline{RVS}$ signal, as shown in figures 9 and 10. Therefore, the HD66310 outputs invalid data during the last CL1 of a frame period.
- In the power supply circuits shown in figures 9 and 10, voltage temporarily becomes unstable just after the $\overline{RVS}$ transition, causing the LCD display to become jumbled.

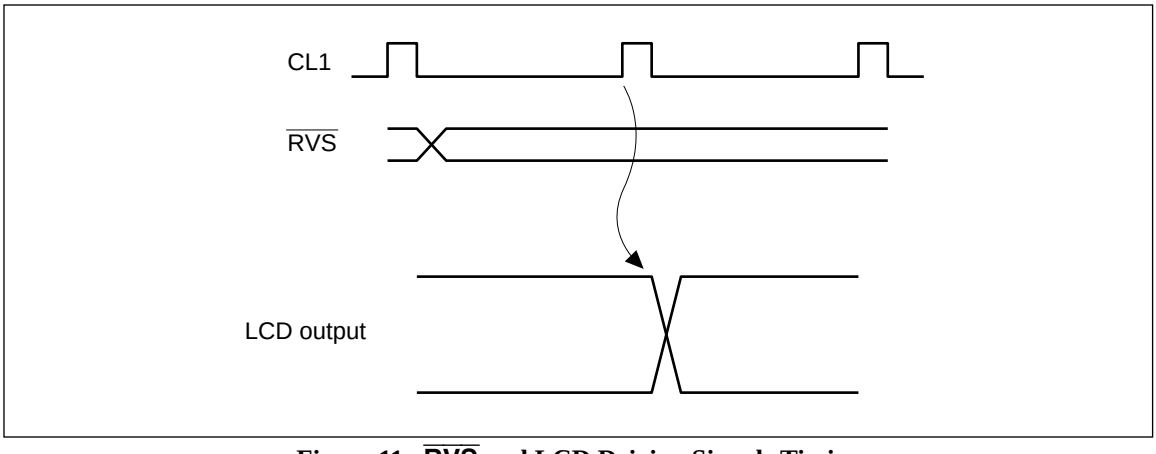


Figure 11 $\overline{RVS}$ and LCD Driving Signals Timing

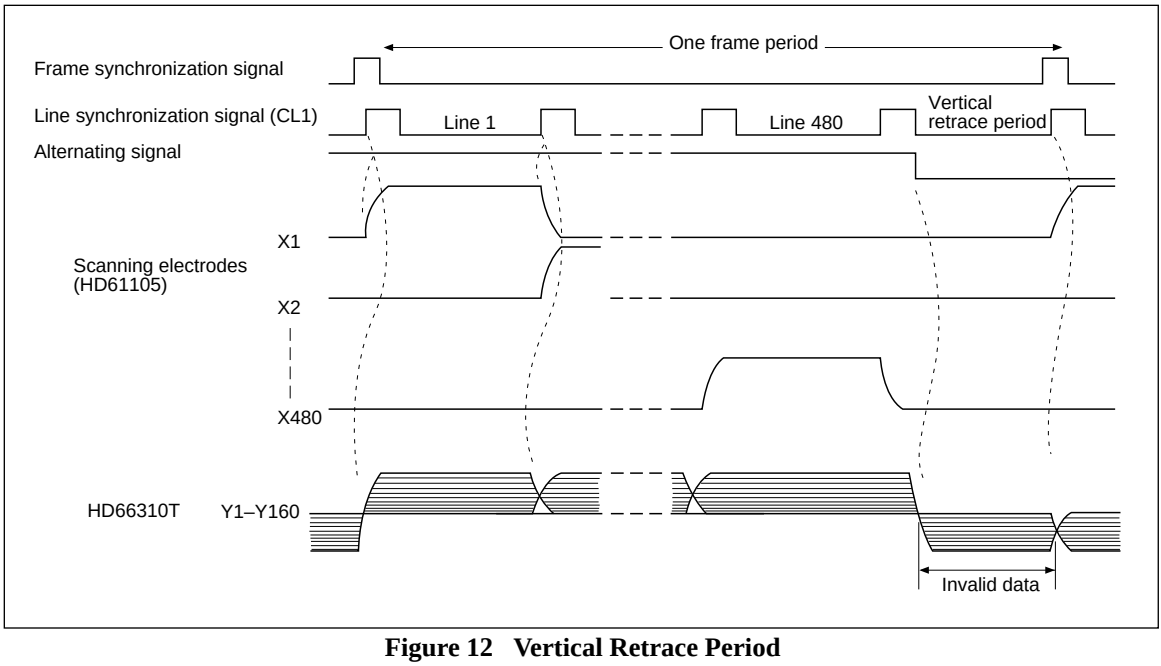


Figure 12 Vertical Retrace Period

Application

Figure 13 shows an HD66310T application for a 480 × 640-dot, 512-color LCD panel. Figure 14 shows the operation timing chart for the system.

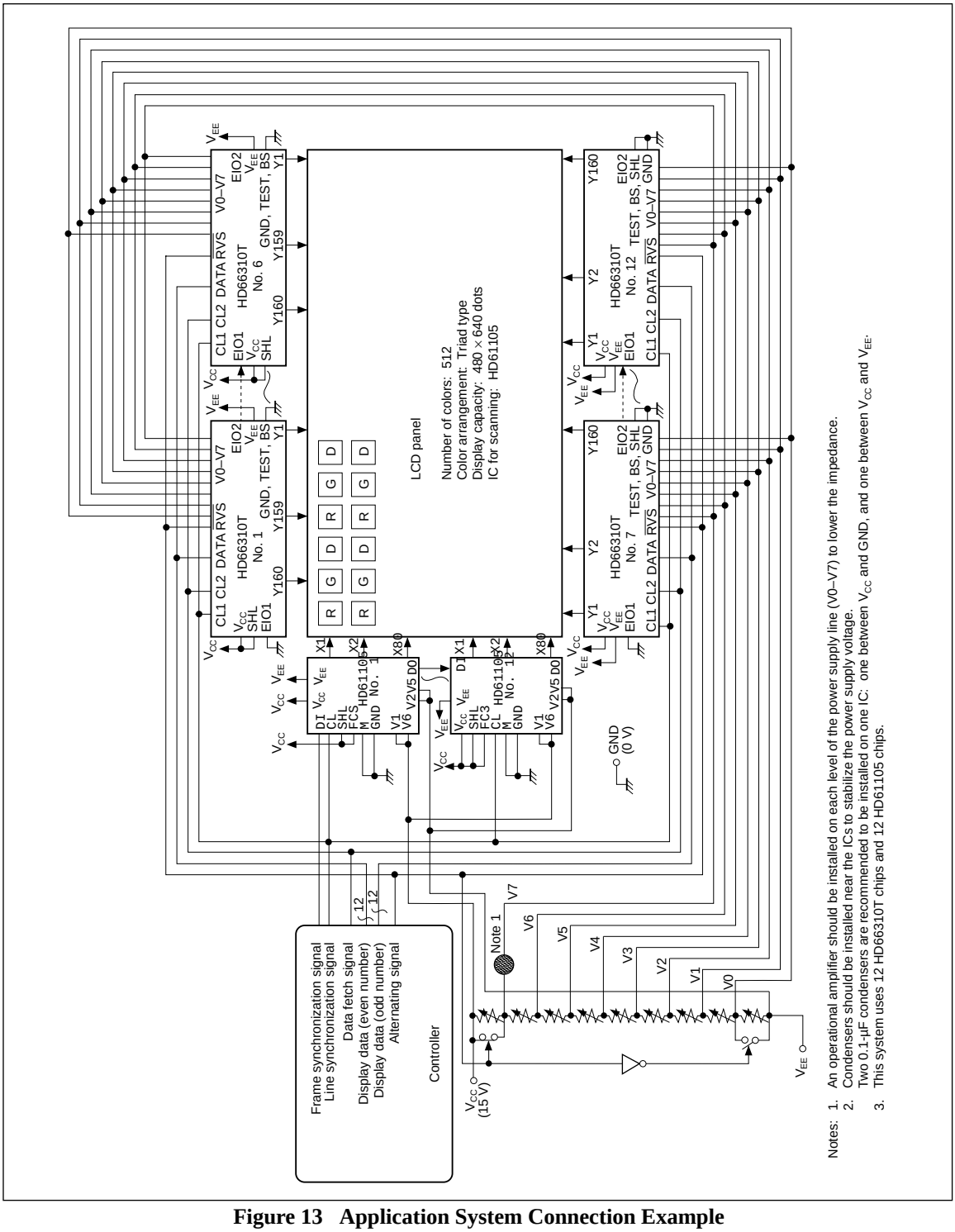


Figure 13 Application System Connection Example

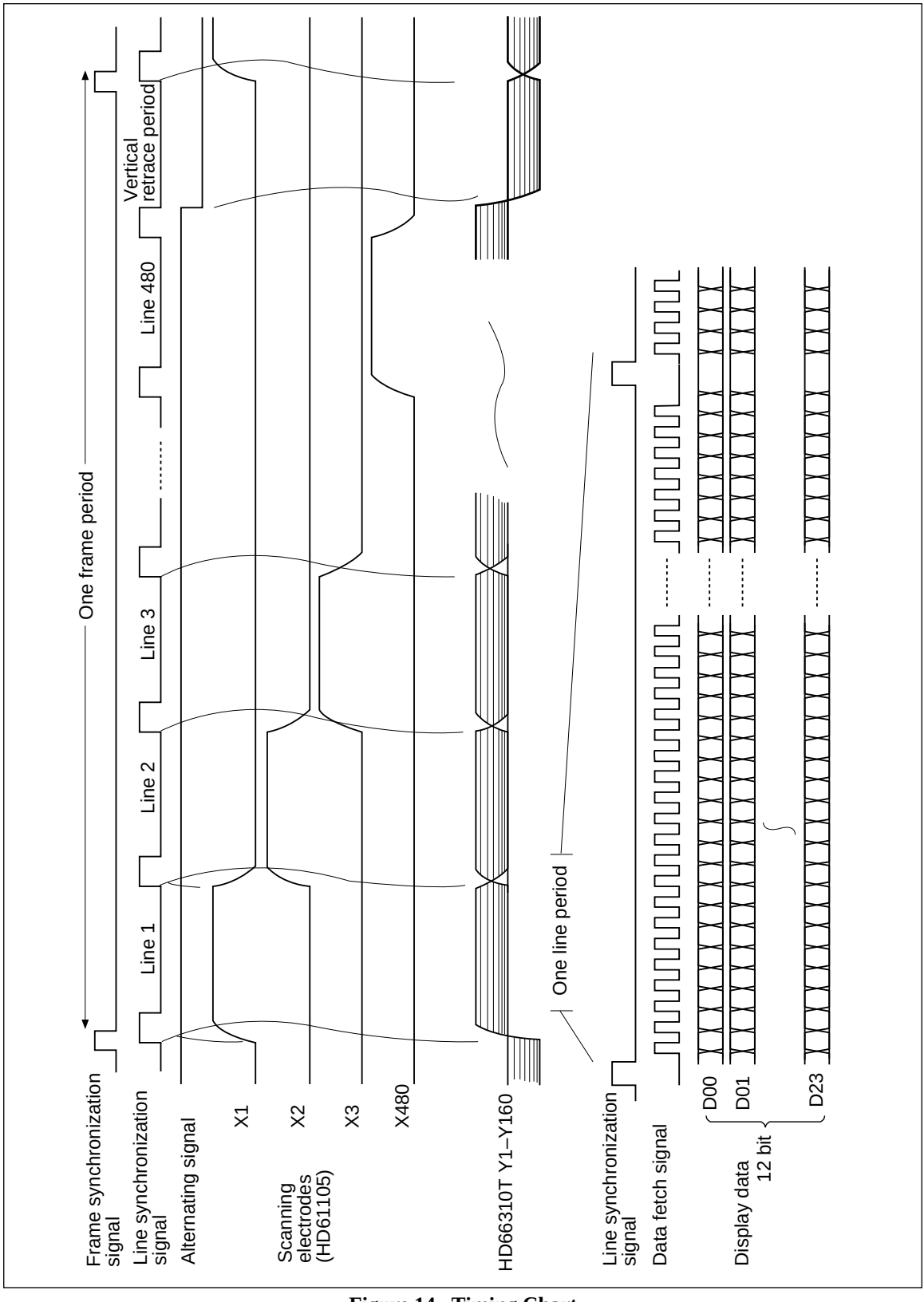


Figure 14 Timing Chart

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V	2
Power supply for LCD driving unit	V_{EE}	V_{CC} – 25 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Input voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
Operating temperature	T_{opr}	–20 to +75 (HD66310T00) –20 to +65 (HD66310T0015)	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. Exceeding the absolute maximum ratings could result in permanent damage to the LSI. The recommended operating conditions are within the electrical characteristic limits listed on the following pages. Exceeding these limits may cause malfunctions and affect reliability.

2. Values are in reference to GND = 0 V.

3. Applies to input pins SHL, CL1, CL2, BS, $\overline{RVS}$, TEST, and D00–D23. Also applies to input/output pins EIO1 and EIO2 when these pins function as input pins.

Electrical Characteristics

DC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
LCD driving power supply voltage	$V_{CC} - V_{EE}$	15		23	V		1
Input high-level voltage (1)	V_{IH1}	$0.8 \times V_{CC}$		V_{CC}	V		2
Input low-level voltage (1)	V_{IL1}	0		$0.2 \times V_{CC}$	V		2
Input high-level voltage (2)	V_{IH2}	$0.75 \times V_{CC}$		V_{CC}	V		3
Input low-level voltage (2)	V_{IL2}	0		$0.25 \times V_{CC}$	V		3
Output high-level voltage	V_{OH}	V_{CC} – 0.4			V	I_{OH} = –0.4 mA	4
Output low-level voltage	V_{OL}			0.4	V	I_{OL} = 0.4 mA	4
Input leakage current (1)	I_{L1}	–5.0		+5.0	µA	$V_{IN} = V_{CC}$ to GND	5
Input leakage current (2)	I_{L2}	–10		+10	µA	$V_{IN} = V_{CC}$ to GND	6
Input leakage current (3)	I_{L3}	–100		+100	µA	$V_{IN} = V_{CC}$ to V_{EE}	7
LCD driver on resistance	RON			2.5	kΩ	$V_{CC} - V_{EE}$ = 20 V	8
Current consumption (1)	$-I_{P1}$			25 30	mA mA	Data fetch 12 MHz Data fetch 15 MHz	9, 11, 12
Current consumption (2)	$-I_{P2}$			2 2.5	mA mA	Stand-by 12 MHz Stand-by 15 MHz	9, 11, 12
Current consumption (3)	$-I_{P3}$			3 3.7	mA mA	12 MHz 15 MHz	10, 11, 12

Notes:
1. Voltage between V_{CC} and V_{EE}.
2. Applies to CL1, CL2, SHL, Dij, $\overline{RVS}$, TEST, and BS.
3. Applies to EIO1 (input) and EIO2 (input).
4. Applies to EIO1 (output) and EIO2 (output).
5. Applies to CL1, CL2, SHL, $\overline{RVS}$, Dij, TEST, and BS.
6. Applies to EIO1 (input) and EIO2 (input).
7. Applies to V0L to V7L and V0R to V7R.
8. Applies to Y1 to Y160.
9. Current between V_{CC} and GND under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.
10. Current between V_{CC} and V_{EE} under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.

11. f_{CL2} and f_{CL1} are 15 MHz, 37.5 kHz respectively in 15 MHz version.
12. f_{CL2} and f_{CL1} are 12 MHz, 30 kHz respectively in 12 MHz version.

AC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Clock period	t_{CYC}	83 (66)			ns		1
Clock high-level pulse width	t_{CWH}	30 (23)			ns		1
Clock low-level pulse width	t_{CWL}	30 (23)			ns		1
Clock rise time	t_R			10 (10)	ns		2
Clock fall time	t_F			10 (10)	ns		2
Clock setup time	t_{SU}	100 (100)			ns		2
Clock hold time	t_H	100 (100)			ns		2
Data setup time	t_{DSU}	20 (10)			ns		3
Data hold time	t_{DH}	30 (25)			ns		3
Enable input setup time	t_{ESU}	20 (10)			ns		4
Enable output delay time	t_{ED}			53 (46)	ns	See figure 16 for test load	4
CL1 high-level pulse width	t_{WH}	100 (100)			ns		5
$\overline{RVS}$ setup time	t_{RSU}	50 (50)			ns		6
$\overline{RVS}$ hold time	t_{RH}	50 (50)			ns		6

Data in ( ) is the characteristics in 15 MHz version.

Notes: 1. Applies to CL2.
2. Applies to CL1 and CL2.
3. Applies to Dij and CL2.
4. Applies to EIO1, EIO2, and CL2.
5. Applies to CL1.
6. Applies to $\overline{RVS}$ and CL2.

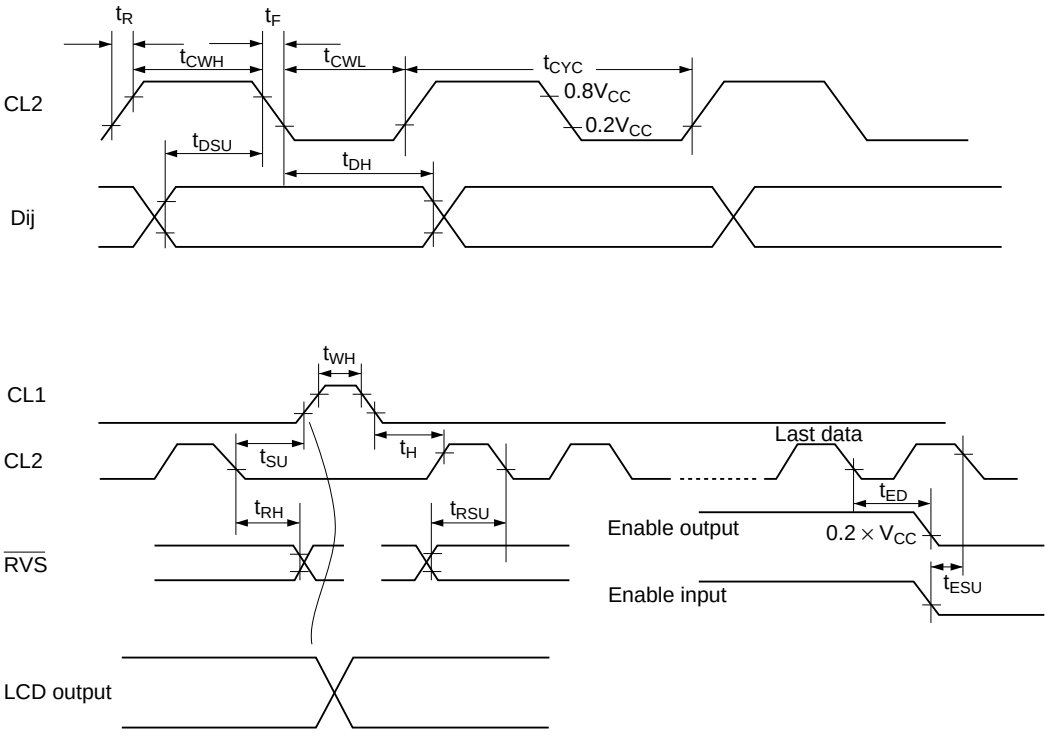


Figure 15 Timing Chart

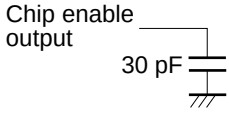


Figure 16 Test Load

HD66330T (TFT Driver)

64-Level Gray Scale Driver for TFT Liquid Crystal Display

HITACHI

Description

The HD66330T, a signal driver LSI, drives an active matrix LCD panel having TFTs (thin film transistor) in the picture element (pixel) area. The LSI receives 6-bit digital display data per dot and outputs corresponding gray scale voltage. This LSI easily achieves multicoloring of a VGA-sized color TFT LCD and is suitable for applications such as multimedia.

Features

- Multicolor display
  The HD66330T receives 6-bit digital display data per dot, and selects and outputs an LCD drive voltage among 64-level gray scale voltages. When R, G, and B color filters are added to the LCD panel, a maximum of 260,000 colors can be displayed.
- High-speed operation
  Operating clock: 35 MHz maximum
  Amount of input data: 3 dots × 6 bits (gray scale data)
- Applicable systems
  PC (640 × 480/400 dots) systems
- Internal 192-bit drive function
- Internal standby function
- Internal chip-enable signal generation circuit
- Supply voltage: 4.5 V to 5.5 V
- Bidirectional shift

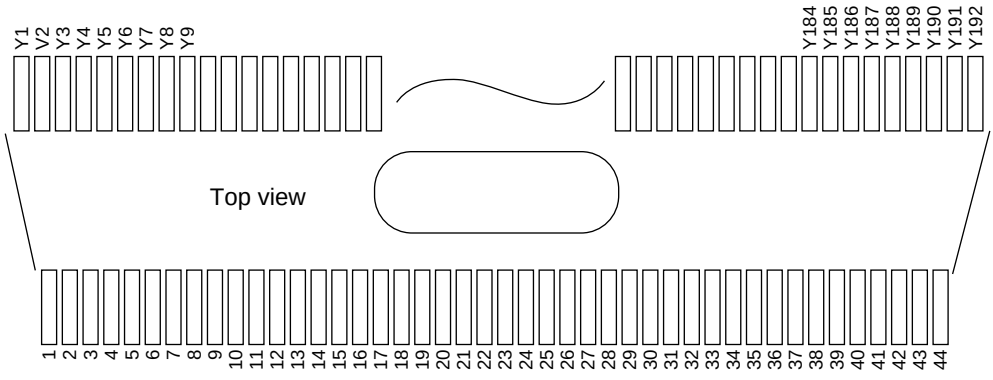
Ordering Information

Type No.	Outer Lead Pitch (µm)	Package
HD66330TA0	160	236-pin TCP

Note: The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

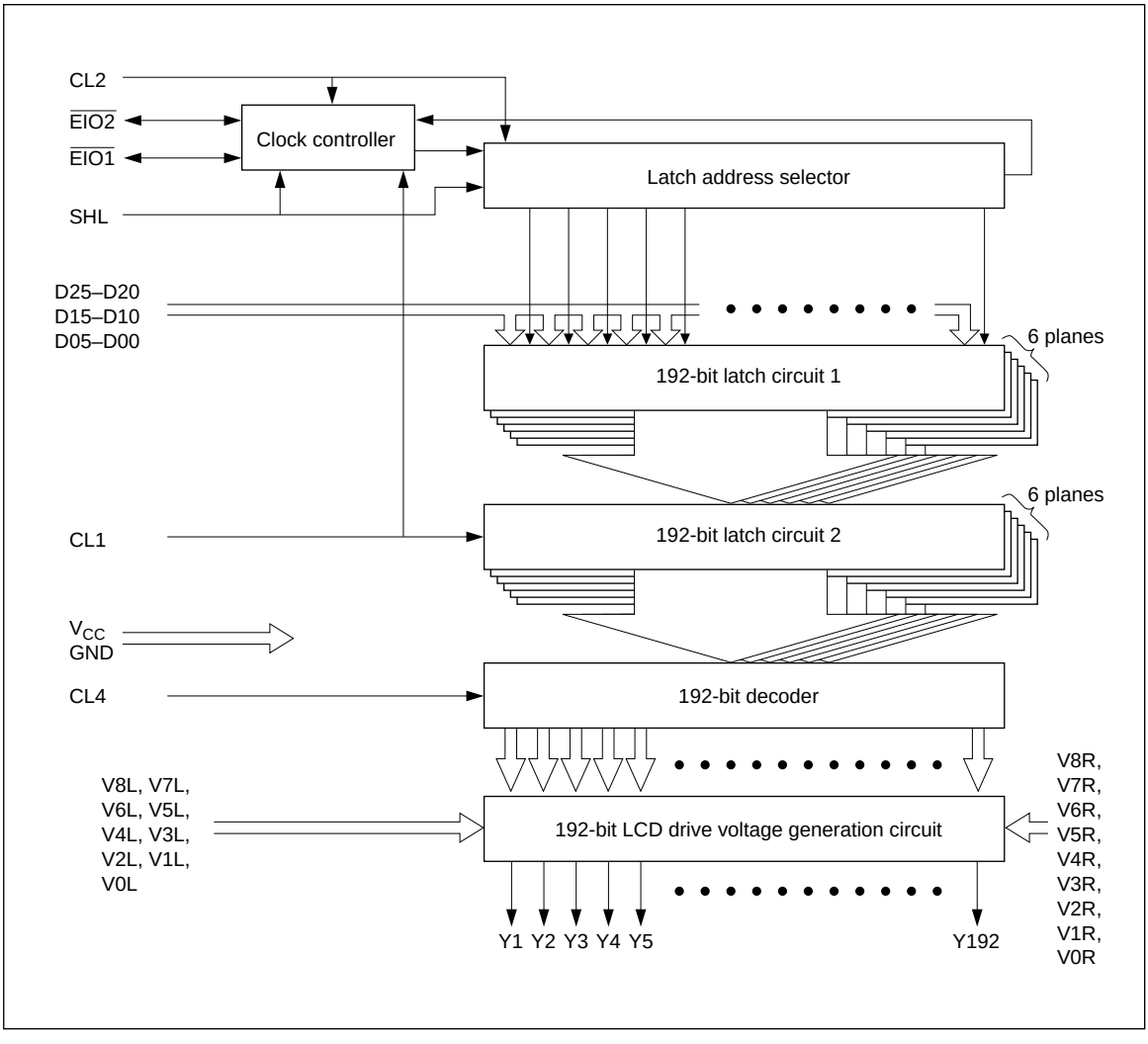
Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

1	V8L	11	D01	21	SHL	31	D21	41	V5R
2	V7L	12	D02	22	GND	32	D22	42	V6R
3	V6L	13	D03	23	$\overline{\text{EIO2}}$	33	D23	43	V7R
4	V5L	14	D04	24	E10	34	D24	44	V8R
5	V4L	15	D05	25	D11	35	D25		
6	V3L	16	$\overline{\text{EIO1}}$	26	D12	36	V0R		
7	V2L	17	CL4	27	D13	37	V1R		
8	V1L	18	CL2	28	D14	38	V2R		
9	V0L	19	CL1	29	D15	39	V3R		
10	D00	20	V_{CC}	30	D20	40	V4R		

Internal Block Diagram



Block Functions

Clock Controller: Generates chip enable signals ($\overline{EIO2}$ and $\overline{EIO1}$) and controls the internal timing signals.

Latch Address Selector: Generates latch signals, which sequentially trigger latch operation of input display data.

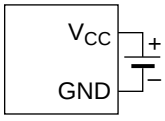
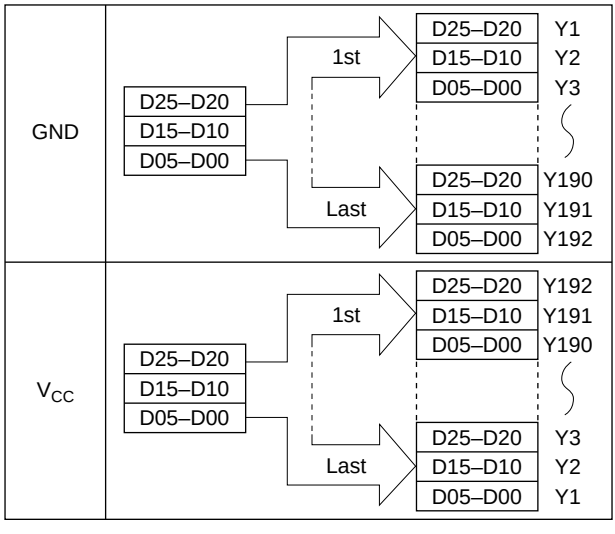
Latch Circuit 1: Latches 3-pixel × 6-bit sequentially input display data; composed of 192 × 6 bits.

Latch Circuit 2: Latches 192 × 6-bit data latched in latch circuit 1 synchronously with the CL1 signal.

Decoder: Generates a decode signal per pixel for the LCD drive voltage generation circuit using an upper 3-bit decoder and a lower 3-bit decoder.

LCD Drive Voltage Generation Circuit: Generates LCD drive voltages from LCD drive power supply voltages according to the decode signals generated by the decoder.

Pin Functions

Signal Name	Numbers	I/O	Functions
V_{CC}	1	Power supply	 V_{CC}–GND: Supplies power to the LSI.
GND	1	Power supply	
V8L–V0L, V8R–V0R	18	Power supply	Supplies power to the LCD drive voltage generation circuit. The same voltage must be applied to corresponding L- and R-power pins within a range of V_{CC} to GND.
CL1	1	Input	Inputs display data latch pulses for latch circuit 2. At the rising edge of each CL1 pulse, latch circuit 2 latches display data input from latch circuit 1 and outputs LCD drive voltages corresponding to the latched data.
CL2	1	Input	Inputs display data latch pulses for latch circuit 1. At the falling edge of each CL2 pulse, latch circuit 1 latches display data input via D25–D00 and outputs the latched data to latch circuit 2.
D25–D20, D15–D10, D05–D00	18	Input	Inputs 6-bit (gray scale data) × 3-pixel display data.
SHL	1	Input	Selects the shift direction of the display data. 
CL4	1	Input	Controls the 2-phase function. A high level period of this signal specifies the first phase period that performs high output current operation, and a low level specifies the second phase period that outputs the voltage corresponding to the display data.

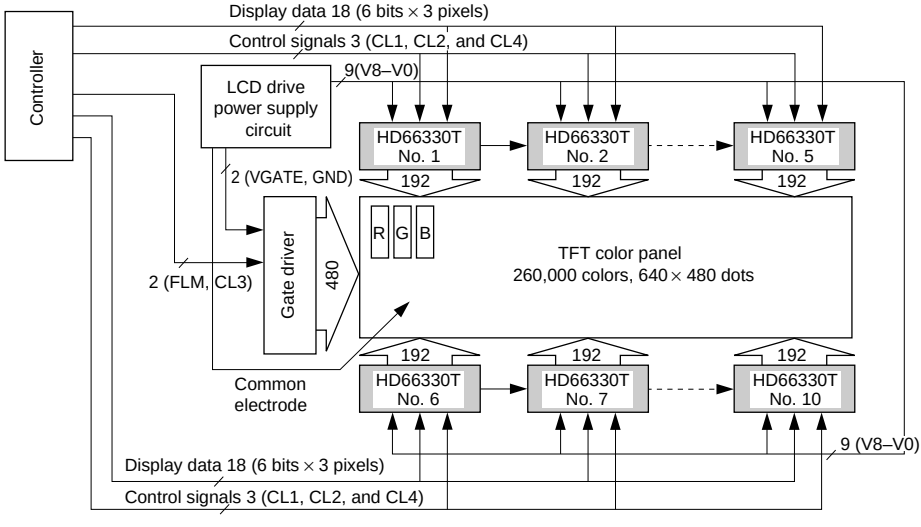
Signal Name	Numbers	I/O	Functions
$\overline{EIO1}$, $\overline{EIO2}$	2	Input/output	Provides chip-enable signals. Input or output depends on the SHL signal, as shown below. At any one time, the signal being used for input must go low to enable the LSI to latch display data, and the signal being used for output will be driven low after 192 pixels of display data have been read.
Y1–Y192	192	Output	Outputs LCD drive voltages.

SHL Level	$\overline{EIO1}$	$\overline{EIO2}$
GND	Input	Output
V_{CC}	Output	Input

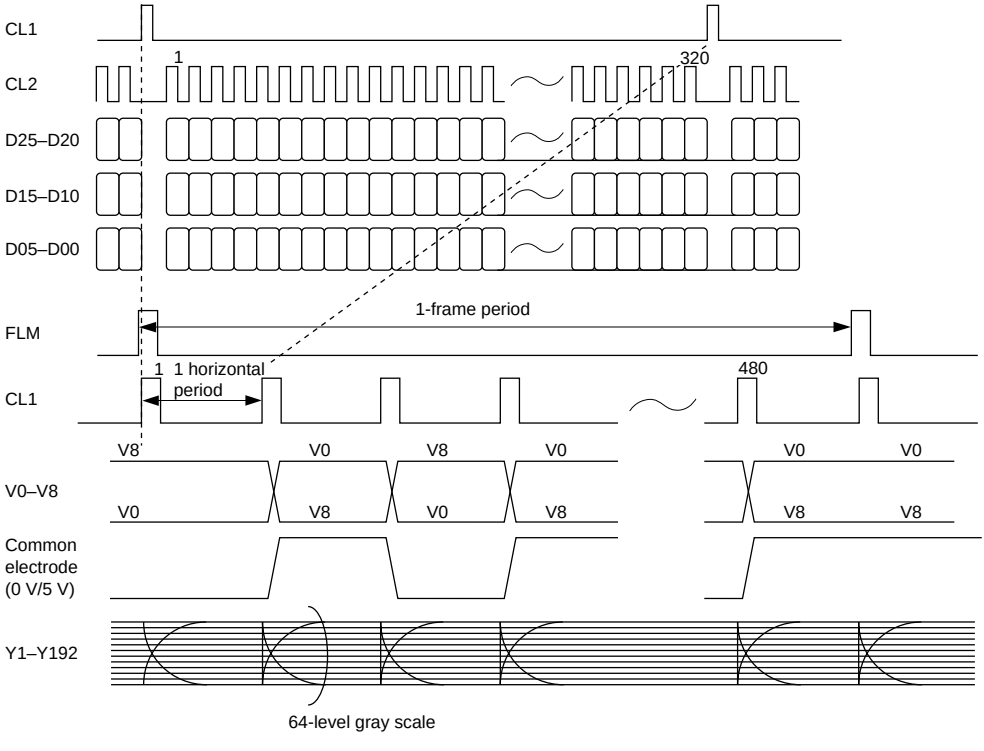
System Overview

The following shows a block diagram of a TFT color LCD system configured with multiple HD66330Ts. The HD66330Ts latch 6-bit data per dot, and selects and outputs one level among 64 internally generated LCD drive voltage levels. When the pixels are structured using R, G, and B color filters, a maximum of 260,000 colors can be displayed.

System block diagram

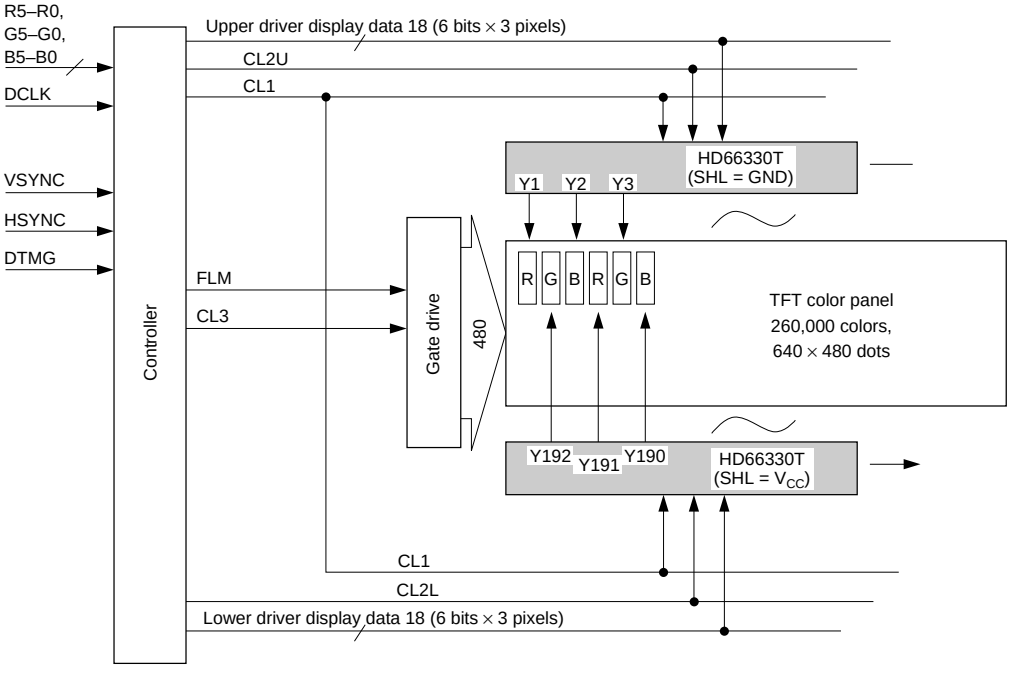


Timing chart (example of the common-voltage AC-drive method)

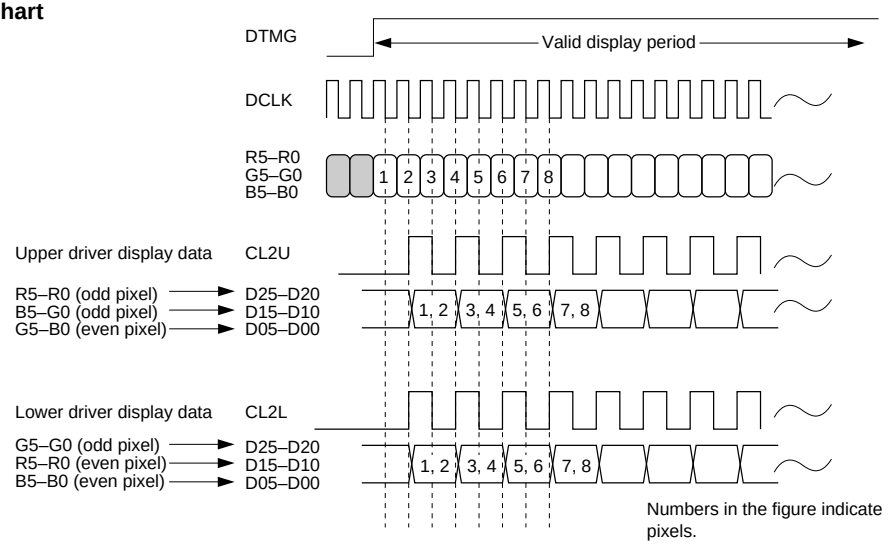


Timing Chart for Display Data

The following figures show the display data timing and hardware configuration for the TFT color LCD system configured with HD66330Ts. Since color panels usually have a narrow connection pitch with driver LSIs, the HD66330Ts should be located above (upper drivers) and below (lower drivers) the panel and alternately connected to the panel pins. In such a configuration, the RGB data and the system dot clock (DCLK) should be divided between the upper and lower drivers. Here, DCLK should be divided into two by the controller.

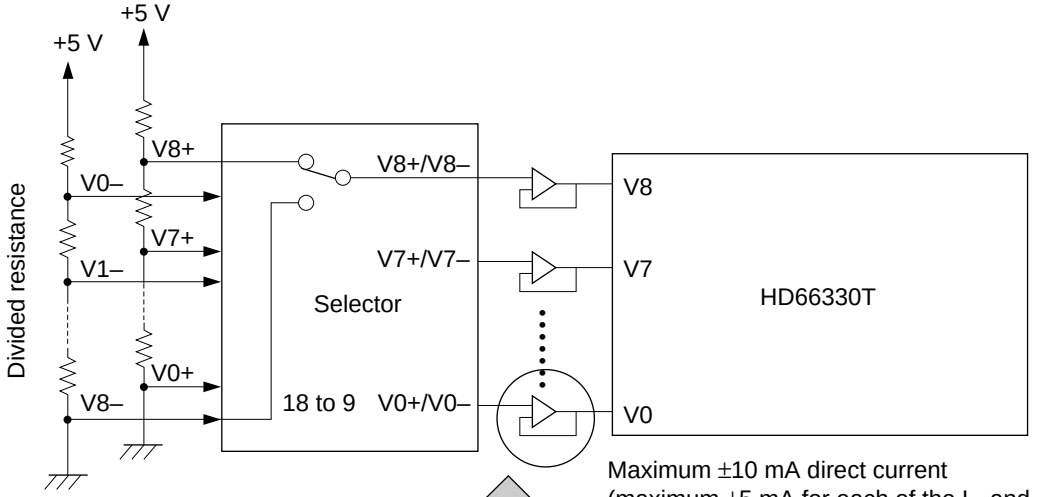


Timing chart



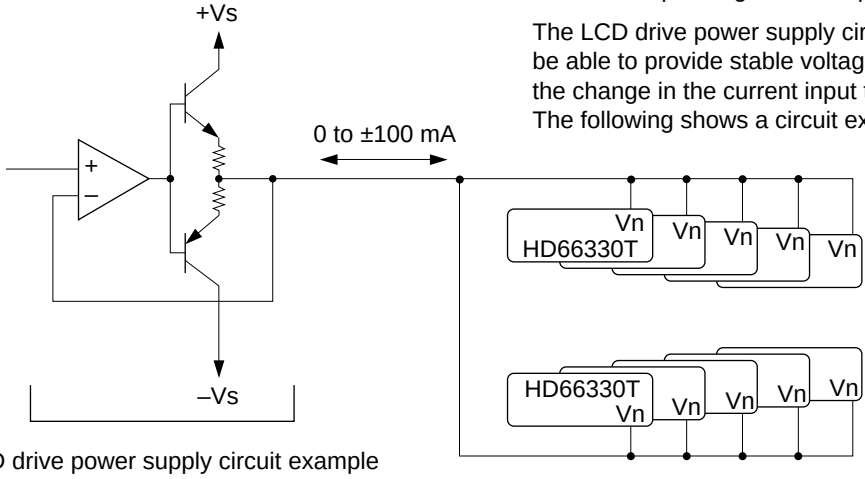
Power Supply Circuit Example

The figures below show an example of a circuit used to generate LCD drive power supply voltages V0 to V8. In this example, 18 levels of voltage are generated by divided resistance to alternate the current for the LCD panel, and either positive or negative voltages are selected and supplied to the HD66330T. To stabilize voltage, an operational amplifier should be connected to each selector output.



Maximum ±10 mA direct current (maximum ±5 mA for each of the L- and R-pins) flows in the LCD drive power supply voltage pins V0 to V8 of one HD66330T. When 10 ICs are used, the current amounts to ±100 mA maximum. The direct current changes within 0 to ±100 mA depending on the display data.

The LCD drive power supply circuit must be able to provide stable voltage despite the change in the current input to the IC. The following shows a circuit example:



LCD drive power supply circuit example
(per one voltage level)

Power Supply Voltage Examples

Voltage levels to be input to LCD drive power supply pins V0 to V8 should be determined according to panel specifications such as voltage intensity characteristics. The table below lists voltage level examples for reference:

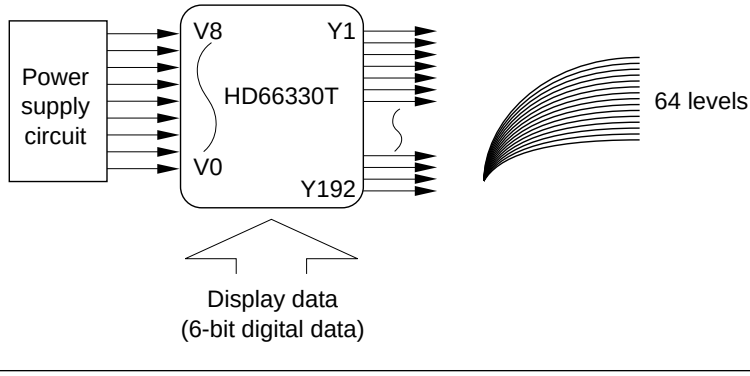
	V0	V1	V2	V3	V4	V5	V6	V7	V8	Counter Electrode
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0	0
	5.0	4.0	3.5	3.0	2.5	2.0	1.5	1.0	0	5.0

Relationship between Display Data and Output Voltage

The HD66330T outputs 64-level gray scale voltage generated by 9 levels of LCD drive power supply voltage and 6-bit digital data. The figure below shows the relationship among the input voltages from the LCD drive power supply circuit, digital codes, and output voltages.

Display Data						Output Voltage	
Di5	Di4	Di3	Di2	Di1	Di0	1st Phase	2nd Phase
0	0	0	0	0	0	V1	V0 + 1/8 × (V1–V0)
0	0	0	0	0	1	V1	V0 + 2/8 × (V1–V0)
0	0	0	0	1	0	V1	V0 + 3/8 × (V1–V0)
0	0	0	0	1	1	V1	V0 + 4/8 × (V1–V0)
0	0	0	1	0	0	V1	V0 + 5/8 × (V1–V0)
0	0	0	1	0	1	V1	V0 + 6/8 × (V1–V0)
0	0	0	1	1	0	V1	V0 + 7/8 × (V1–V0)
0	0	0	1	1	1	V1	V1
0	0	1	0	0	0	V2	V1 + 1/8 × (V2–V1)
0	0	1	0	0	1	V2	V1 + 2/8 × (V2–V1)
0	0	1	0	1	0	V2	V1 + 3/8 × (V2–V1)
0	0	1	0	1	1	V2	V1 + 4/8 × (V2–V1)
0	0	1	1	0	0	V2	V1 + 5/8 × (V2–V1)
0	0	1	1	0	1	V2	V1 + 6/8 × (V2–V1)
0	0	1	1	1	0	V2	V1 + 7/8 × (V2–V1)
0	0	1	1	1	1	V2	V2
0	1	0	0	0	0	V3	V2 + 1/8 × (V3–V2)
0	1	0	0	0	1	V3	V2 + 2/8 × (V3–V2)
0	1	0	0	1	0	V3	V2 + 3/8 × (V3–V2)
0	1	0	0	1	1	V3	V2 + 4/8 × (V3–V2)
0	1	0	1	0	0	V3	V2 + 5/8 × (V3–V2)
0	1	0	1	0	1	V3	V2 + 6/8 × (V3–V2)
0	1	0	1	1	0	V3	V2 + 7/8 × (V3–V2)
0	1	0	1	1	1	V3	V3
0	1	1	0	0	0	V4	V3 + 1/8 × (V4–V3)
0	1	1	0	0	1	V4	V3 + 2/8 × (V4–V3)
0	1	1	0	1	0	V4	V3 + 3/8 × (V4–V3)
0	1	1	0	1	1	V4	V3 + 4/8 × (V4–V3)
0	1	1	1	0	0	V4	V3 + 5/8 × (V4–V3)
0	1	1	1	0	1	V4	V3 + 6/8 × (V4–V3)
0	1	1	1	1	0	V4	V3 + 7/8 × (V4–V3)
0	1	1	1	1	1	V4	V4
1	0	0	0	0	0	V5	V4 + 1/8 × (V5–V4)
1	0	0	0	0	1	V5	V4 + 2/8 × (V5–V4)
1	0	0	0	1	0	V5	V4 + 3/8 × (V5–V4)
1	0	0	0	1	1	V5	V4 + 4/8 × (V5–V4)
1	0	0	1	0	0	V5	V4 + 5/8 × (V5–V4)
1	0	0	1	0	1	V5	V4 + 6/8 × (V5–V4)
1	0	0	1	1	0	V5	V4 + 7/8 × (V5–V4)
1	0	0	1	1	1	V5	V5
1	0	1	0	0	0	V6	V5 + 1/8 × (V6–V5)
1	0	1	0	0	1	V6	V5 + 2/8 × (V6–V5)
1	0	1	0	1	0	V6	V5 + 3/8 × (V6–V5)
1	0	1	0	1	1	V6	V5 + 4/8 × (V6–V5)
1	0	1	1	0	0	V6	V5 + 5/8 × (V6–V5)
1	0	1	1	0	1	V6	V5 + 6/8 × (V6–V5)
1	0	1	1	1	0	V6	V5 + 7/8 × (V6–V5)
1	0	1	1	1	1	V6	V6
1	1	0	0	0	0	V7	V6 + 1/8 × (V7–V6)
1	1	0	0	0	1	V7	V6 + 2/8 × (V7–V6)
1	1	0	0	1	0	V7	V6 + 3/8 × (V7–V6)
1	1	0	0	1	1	V7	V6 + 4/8 × (V7–V6)
1	1	0	1	0	0	V7	V6 + 5/8 × (V7–V6)
1	1	0	1	0	1	V7	V6 + 6/8 × (V7–V6)
1	1	0	1	1	0	V7	V6 + 7/8 × (V7–V6)
1	1	0	1	1	1	V7	V7
1	1	1	0	0	0	V8	V7 + 1/8 × (V8–V7)
1	1	1	0	0	1	V8	V7 + 2/8 × (V8–V7)
1	1	1	0	1	0	V8	V7 + 3/8 × (V8–V7)
1	1	1	0	1	1	V8	V7 + 4/8 × (V8–V7)
1	1	1	1	0	0	V8	V7 + 5/8 × (V8–V7)
1	1	1	1	0	1	V8	V7 + 6/8 × (V8–V7)
1	1	1	1	1	0	V8	V7 + 7/8 × (V8–V7)
1	1	1	1	1	1	V8	V8

Note: 1st phase: The period in which 2-phase control signal CL4 is high and high output current operation is performed.
2nd phase: The period in which 2-phase control signal CL4 is low and low output current operation is performed.



Output Offset Voltage

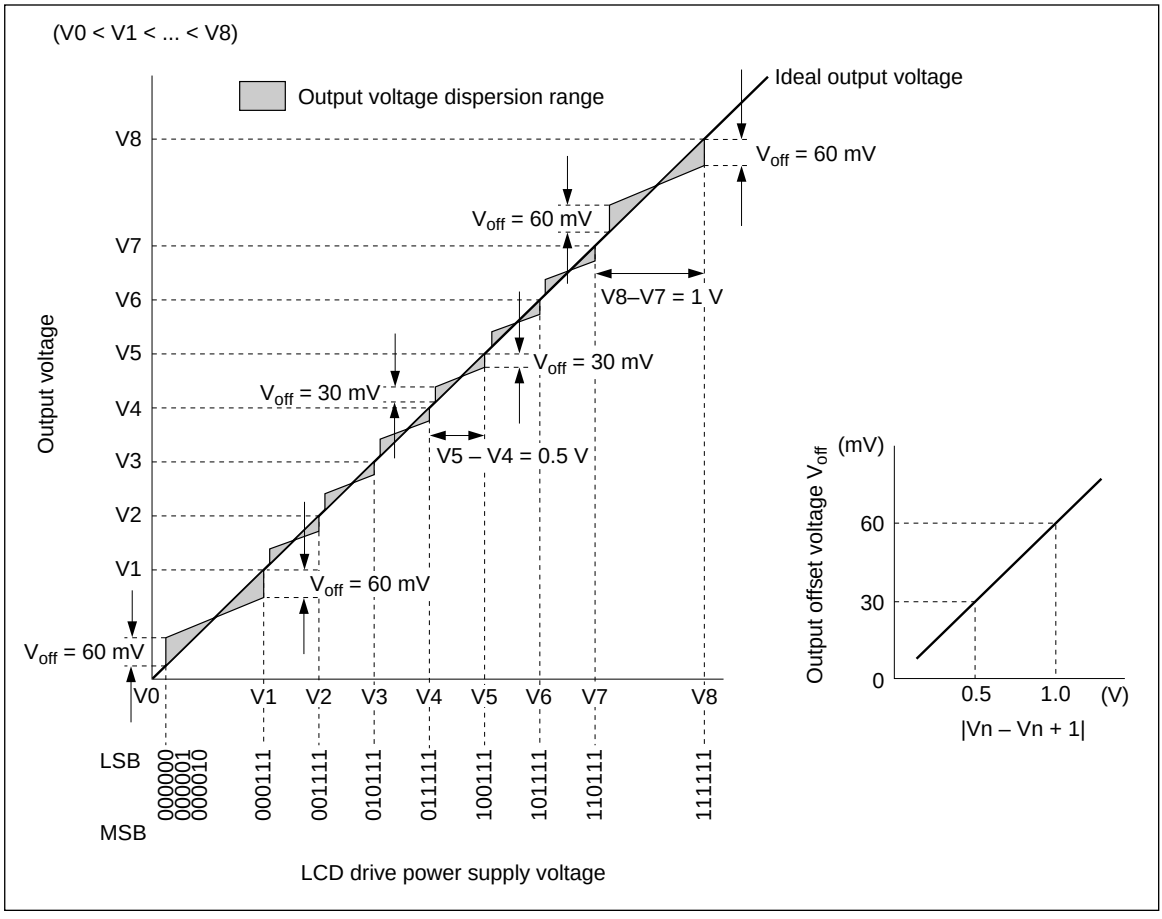
The HD66330T has an internal DA converter per output. The upper three bits of 6-bit display data select and apply the LCD drive power supply voltage level to the DA converter, and the lower three bits select and output one analog voltage level.

Output offset voltage Voff is defined as the difference between the actual output voltage and the ideal output voltage expected from the LCD drive power supply voltage and digital display data. The Voff can be considered as the total output voltage differences including the differences between LSIs, between different output pins of the same LSI, and that caused by concentrated current in a LSI due to a particular display pattern.

The figure below shows the characteristics of output voltage with respect to LCD drive power supply voltages. Since output offset voltage Voff depends on the difference between adjoining LCD drive power supply voltages |Vn – Vn + 1| (n = 0 to 7) output offset voltage will also decrease when the power supply voltage difference |Vn – Vn + 1| is decreased.

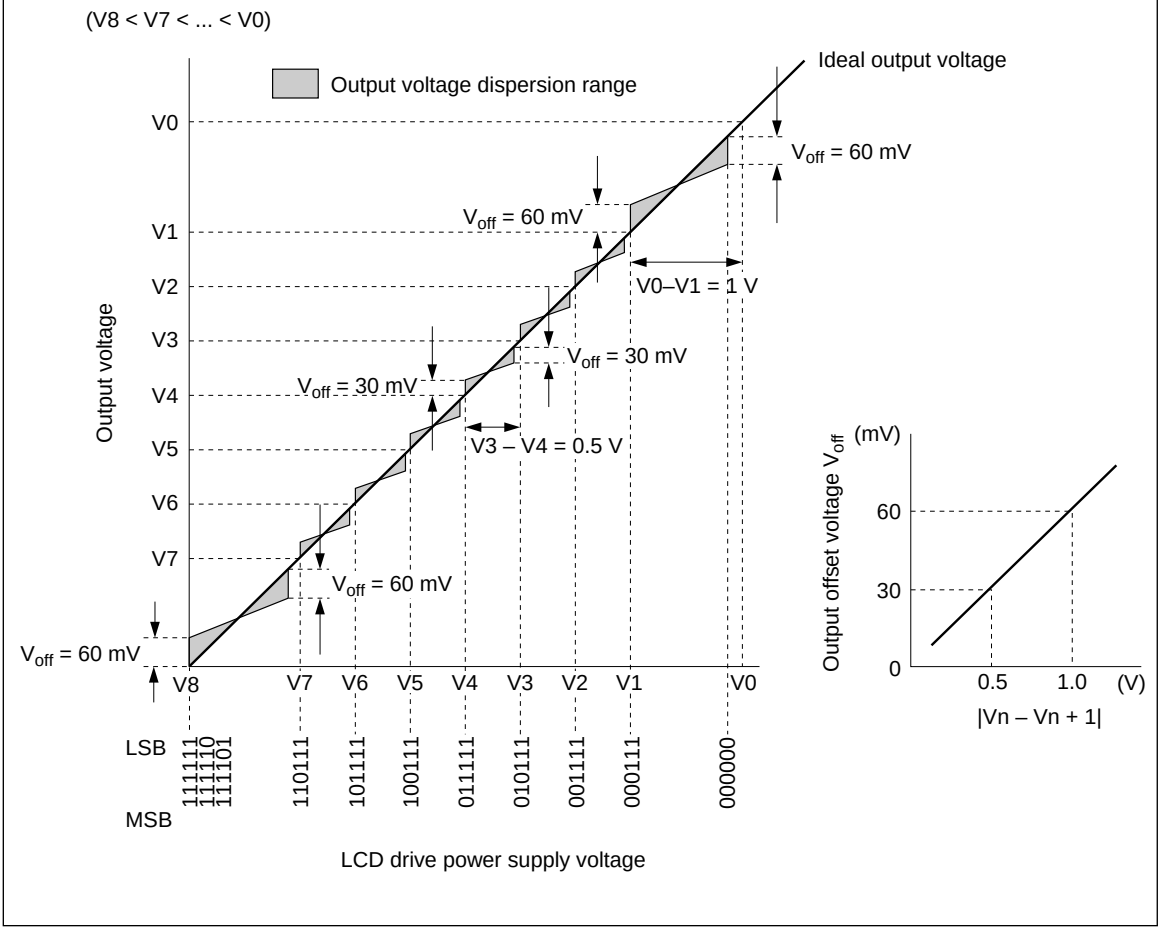
LCD Drive Power Supply Voltage Examples

	V0	V1	V2	V3	V4	V5	V6	V7	V8
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0



LCD Drive Power Supply Voltage Examples

	V8	V7	V6	V5	V4	V3	V2	V1	V0
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0



2-Phase Operation

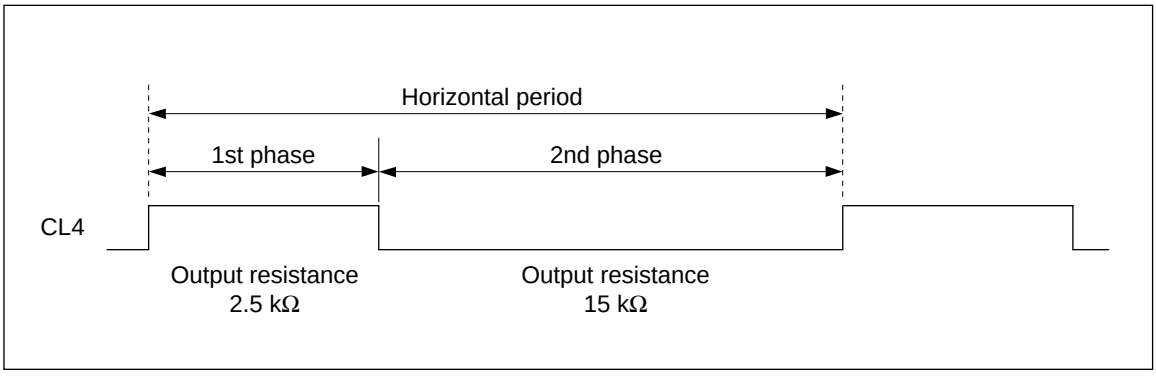
A high-speed low-power output switching function is provided by dividing the horizontal period into 1st-and 2nd-phase periods, where high output current operation and low output current operation are alternately performed.

During the 1st-phase period, the specified voltage is applied to the LCD panel quickly with a low output impedance of about 2.5 kΩ (high output current operation). Here, the applied voltage is selected by the upper three bits of display data.

During the 2nd-phase period, a voltage is applied corresponding to the display data with an output impedance of about 15 kΩ (low output current operation).

In general, since it is not required to secure the 1st phase in a 640 × 480-dot color panel (see the figure below for assumed load condition), CL4 can be fixed low.

This function is effective when the panel load is large or when a horizontal period is short and gray scale voltage must be applied quickly. For settings in the 1st-phase period, see note 4 in Electrical Characteristics.



Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	1
Input voltage (1)	V_{t1}	–0.3 to +V_{CC} + 0.3	V	1, 2
Input voltage (2)	V_{t2}	–0.3 to +V_{CC} + 0.3	V	1, 3, 4
LCD power supply input current	I_t	±20	mA	5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Notes: 1. Assuming GND = 0 V.

2. Applies to input pins CL1, CL2, CL4, SHL, and Dij, and I/O pins $\overline{EIO1}$ and $\overline{EIO2}$ when used as input.
3. Specifies voltage to be input to the LCD drive power supply pins.
   Either of the following relationships must hold:
   $V_{CC} \geq V8 \geq V7 \geq V6 \geq V5 \geq V4 \geq V3 \geq V2 \geq V1 \geq V0 \geq GND$ or
   $V_{CC} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V6 \geq V7 \geq V8 \geq GND$
4. The following relationship must hold for V0 to V8 potentials:
   $|Vn - Vn + 1| \leq 2$ V (n = 0 to 7)
5. Specifies the maximum ratings for current in the LCD drive power supply input pins V0 to V8 (total current for both L and R pins).

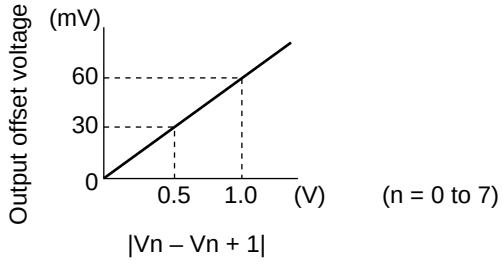
Electrical Characteristics

DC Characteristics (V_{CC} – GND = 4.5 to 5.5 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Conditions	Notes
Input high-level voltage	V_{IH}	CL1, Cl2, SHL,Dij, CL4, EIO1(I), EIO2(I)	2.2		V_{CC}	V		
Input low-level voltage	V_{IL}		0		0.8	V		
Output high-level voltage	V_{OH}	EIO1(O), EIO2(O)	V_{CC} – 0.4			V	I_{OH} = –0.4 mA	
Output low-level voltage	V_{OL}				0.4	V	I_{OL} = 0.4 mA	
Input leakage current (1)	I_{L1}	CL1, Cl2, SHL, Dij, CL4	–5		+5	µA		
Input leakage current (2)	I_{L2}	EIO1(I), EIO2(I)	–10		+10	µA		
LCD drive power supply input current	I_t	V0L–V8L, V0R–V8R	–10		+10	mA	Total of L and R pins |Vn – Vn + 1| = 1 V (n = 0 to 7)	
Output offset voltage	V_{off}	Y1–Y192	—		60	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 1 V (n = 0 to 7)	1
			—		30	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 0.5 V (n = 0 to 7)	
Difference between output pins	V_{ref}	Y1–Y192	—		±30	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 1 V (n = 0 to 7)	2
			—		±15	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 0.5 V (n = 0 to 7)	
Driver output ON resistance	R_{on1}	Y1–Y192	—		2.5	kΩ	1st phase V_{CC} – GND = 5 V	
	R_{on2}	Y1–Y192	—		15	kΩ	2nd phase V_{CC} – GND = 5 V	
Current consumption (1)	I_{p1}	Between V_{CC} and GND	—		20	mA	Data latch f_{CL2} = 15 MHz, f_{CL1} = 33 kHz	3
Current consumption (2)	I_{p2}	Between V_{CC} and GND	—		1.5	mA	Standby f_{CL2} = 15 MHz, f_{CL1} = 33 kHz	

Notes: 1. Output offset voltage V_{off} is defined as difference between the actual output voltage and output voltage expected from the LCD drive power supply voltage and digital display data.

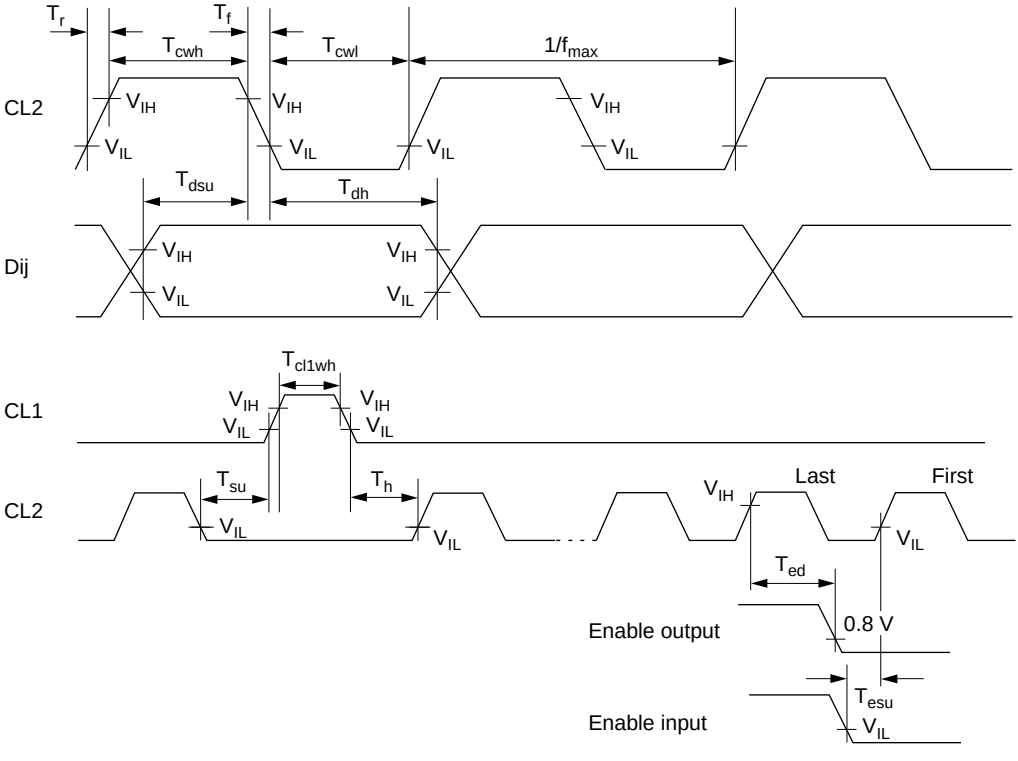
V_{off} shows the following characteristics with respect to voltage difference between adjoining LCD drive power supply pins |Vn – Vn + 1|.



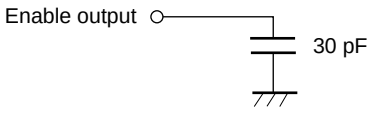
2. V_{ref} can be considered as the maximum total output voltage differences including the differences between LSIs, between output pins of the same LSI, and that caused by concentrated current in an LSI due to a particular display pattern.
3. Except for the current flowing in V0 to V8; outputs are unloaded.

AC Characteristics (V_{CC} – GND = 4.5 to 5.5 V, and T_a = –20 to +75°C, unless otherwise noted)

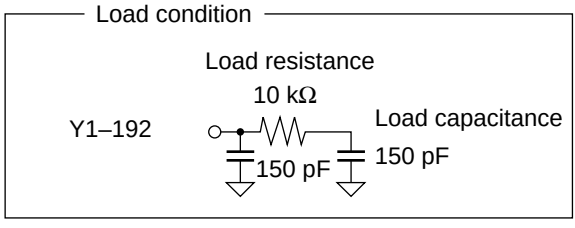
Item	Symbol	Applicable Pin	Min	Typ	Max	Unit	Test Condition	Notes
Operating frequency	f_{max}	CL2			35	MHz		
Clock high-level width	T_{cwh}	CL2	9			ns		
Clock low-level width	T_{cwl}	CL2	9			ns		
Clock rise time	T_r	CL1, CL2			5	ns		
Clock fall time	T_f	CL1, CL2			5	ns		
Clock setup time	T_{su}	CL1, CL2	50			ns		
Clock hold time	T_h	CL1, CL2	70			ns		
Data setup time	T_{dsu}	Dij, CL2	6			ns		
Data hold time	T_{dh}	Dij, CL2	6			ns		
Enable setup time	T_{esu}	EIO1, EIO2, CL2	4			ns		
Enable output delay time	T_{ed}	EIO1, EIO2, CL2			18	ns		1
CL1 high-level width	T_{cl1wh}	CL1	56			ns		
Driver output delay time	T_{dd}	CL1, Y1–Y192			20	µs		2, 3, 4

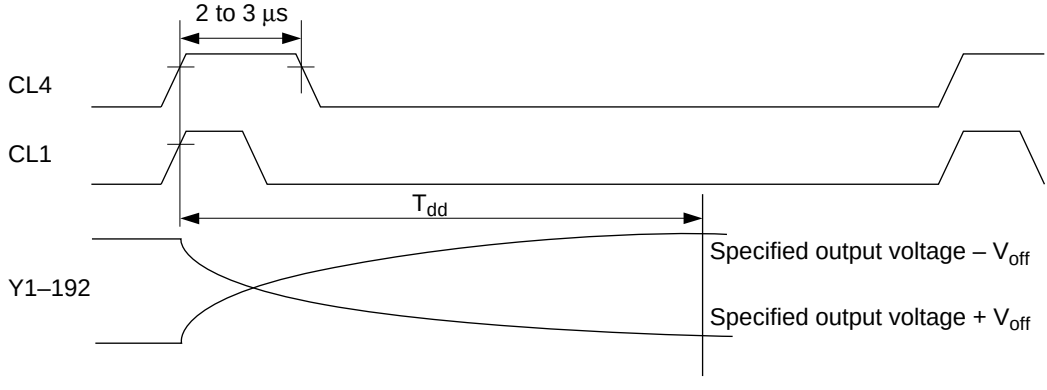


Notes: 1. The figure below shows the load condition for the enable output pins.

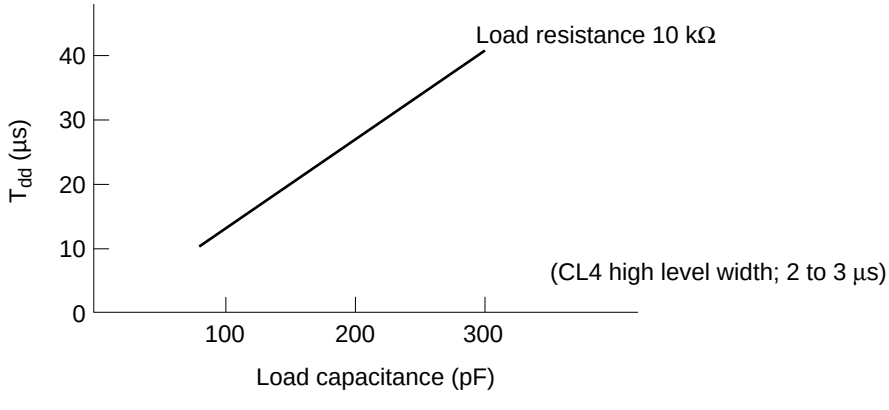


2. Specified by the following load condition and timing.





3. Driver output delay time T_{dd} has the following characteristics with respect to the load condition.



4. Driver output delay time T_{dd} has the following characteristics with respect to the CL4 high-level width.