



CSD25401Q3

SLPS211C -AUGUST 2009-REVISED APRIL 2013

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P-Channel NexFET™ Power MOSFETs

Check for Samples: CSD25401Q3

FEATURES

- Ultra Low Q_q and Q_{qd}
- Low Thermal Resistance
- Low R_{DS(on)}
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

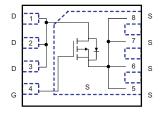
APPLICATIONS

- DC-DC Converters
- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion load management applications. The SON 3x3 package offers excellent thermal performance for the size of the package.

Figure 1. Top View



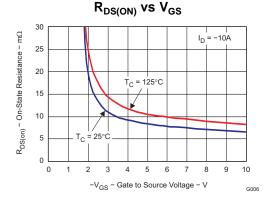


Table 1. PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	-20		V
Q_g	Gate Charge Total (4.5V) 8.8			
Q_{gd}	Gate Charge Gate to Drain	o Drain 2.1		nC
D	Drain to Course On Registeres	$V_{GS} = -2.5V$	13.5	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -4.5V	8.8	mΩ
V_{th}	Threshold Voltage	-0.85		V

ORDERING INFORMATION

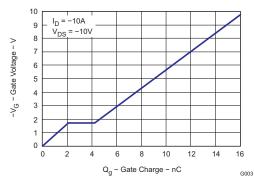
Device	Package	Media	Media Qty	
CSD25401Q3	SON 3 x 3 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 2	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	-20	٧
V_{GS}	Gate to Source Voltage	+12 / -12	٧
	Continuous Drain Current, T _C = 25°C	-60	Α
I _D	Continuous Drain Current ⁽¹⁾	-14	Α
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	-82	Α
P _D	Power Dissipation ⁽¹⁾	2.8	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1) $R_{\theta JA} = 45$ °C/W on 1inch² Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300µs, duty cycle ≤2%

Gate Charge



M

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ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static C	haracteristics				<u> </u>	
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
I _{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V$, $V_{DS} = -20V$ to $-16V$			-1	μA
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 12V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.6	-0.85	-1.2	V
	Drain to Source On Resistance	$V_{GS} = -2.5V$, $I_D = -10A$		13.5	18.2	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -10A$		8.8	11.7	mΩ
9 _{fs}	Transconductance	$V_{DS} = -15V, I_D = -10A$		43		S
Dynami	c Characteristics		•			
C _{ISS}	Input Capacitance			1070	1400	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = -10V,$ $f = 1MHz$		560	730	pF
C _{RSS}	Reverse Transfer Capacitance	1 - 111112		180	230	pF
Qg	Gate Charge Total (4.5V)			8.8	12.3	nC
Q _{gd}	Gate Charge Gate to Drain	101/ 1 100		2.1		nC
Q _{gs}	Gate Charge Gate to Source	V _{DS} = -10V, I _D = -10A		2.1		nC
Q _{g(th)}	Gate Charge at Vth			0.9		nC
Q _{OSS}	Output Charge	$V_{DS} = -10V, V_{GS} = 0V$		8.2		nC
t _{d(on)}	Turn On Delay Time			8.1		ns
t _r	Rise Time	$V_{DS} = -10V, V_{GS} = -4.5V,$		3.9		ns
t _{d(off)}	Turn Off Delay Time	$I_D = -10A$, $R_G = 5.1\Omega$		13.5		ns
t _f	Fall Time	12.6			ns	
Diode C	haracteristics		<u>.</u>		*	
V _{SD}	Diode Forward Voltage	I _S = -10A, V _{GS} = 0V		-0.7	-1	V
Q _{rr}	Reverse Recovery Charge	$V_{DD} = -12.5V, I_F = -10A,$		17.4		nC
t _{rr}	Reverse Recovery Time	di/dt = 300A/µs		21		ns

THERMAL INFORMATION

	•	CSD25401Q3	LIMITE
	I HERWAL METRIC	8 PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	42.0	
θ_{JCtop}	Junction-to-case (top) thermal resistance	20.6	
θ_{JB}	Junction-to-board thermal resistance	8.8	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.3	*C/VV
Ψ_{JB}	Junction-to-board characterization parameter	8.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.1	

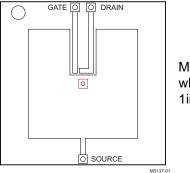
⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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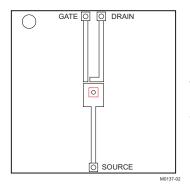
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⁽²⁾ For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

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Max $R_{\theta JA} = 57^{\circ}C/W$ when mounted on 1inch² of 2 oz. Cu.



Max $R_{\theta JA} = 158^{\circ}C/W$ when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

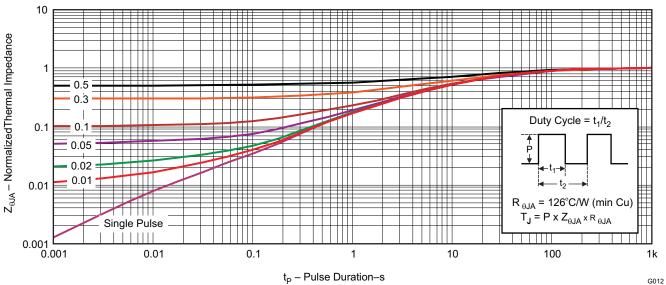


Figure 2. Transient Thermal Impedance

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

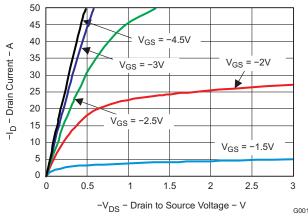


Figure 3. Saturation Characteristics

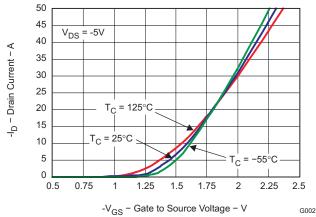
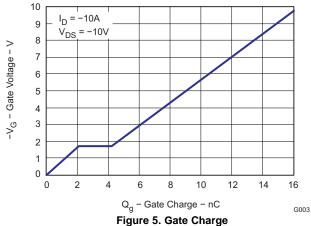
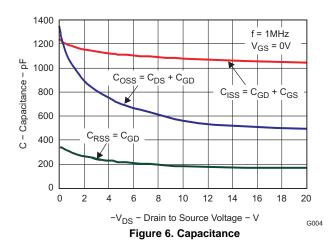


Figure 4. Transfer Characteristics





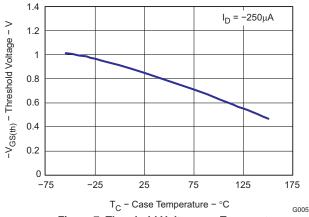


Figure 7. Threshold Voltage vs. Temperature

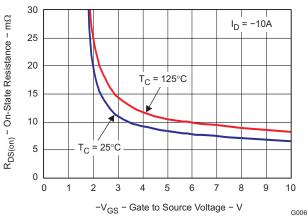


Figure 8. On Resistance vs. Gate Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

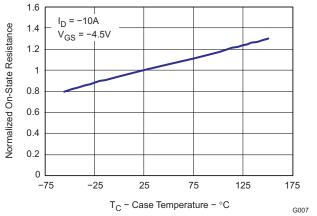


Figure 9. On Resistance vs. Temperature

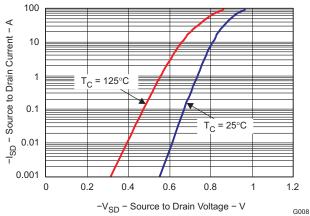


Figure 10. Typical Diode Forward Voltage

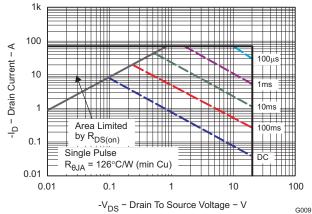


Figure 11. Maximum Safe Operating Area

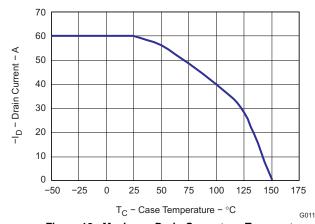


Figure 12. Maximum Drain Current vs. Temperature

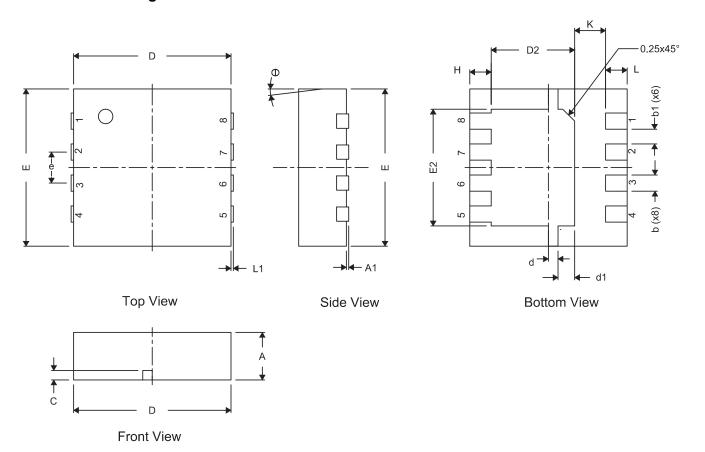
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MECHANICAL DATA

CSD25401Q3 Package Dimensions



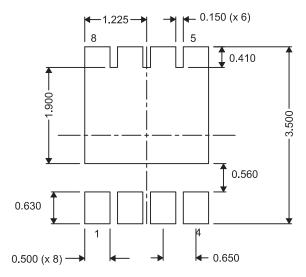
DIM		MILLIMETERS		INCHES				
	MIN	NOM	MAX	MIN	NOM	MAX		
Α	0.950	1.000	1.100	0.037	0.039	0.043		
A1	0.000	0.000	0.050	0.000	0.000	0.002		
b	0.280	0.340	0.400	0.011	0.013	0.016		
b1		0.310 NOM			0.012 NOM			
С	0.150	0.200	0.250	0.006	0.008	0.010		
D	3.200	3.300	3.400	0.126	0.130	0.134		
D2	1.650	1.750	1.800	0.065	0.069	0.071		
d	0.150	0.200	0.250	0.006	0.008	0.010		
d1	0.300	0.350	0.400	0.012	0.014	0.016		
Е	3.200	3.300	3.400	0.126	0.130	0.134		
E2	2.350	2.450	2.550	0.093	0.096	0.100		
е		0.650 TYP		0.026 TYP				
Н	0.35	0.450	0.550	0.014	0.018	0.022		
K	0.650 TYP			0.026 TYP				
L	0.35	0.450	0.550	0.014	0.018	0.022		
L1	0		0	0		0		
θ	0		0	0		0		

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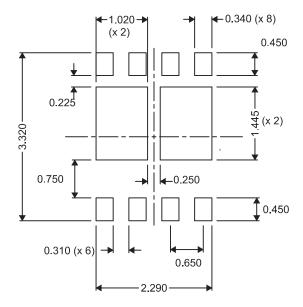
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Recommended PCB Pattern



Recommended Stencil Opening

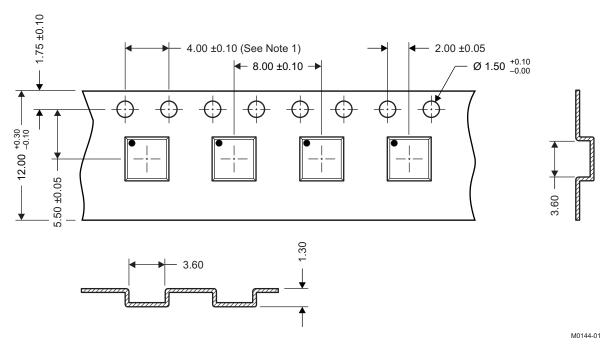


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Tape and Reel Information



Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- 3. Material:black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. Thickness: 0.30 ±0.05mm
- 6. MSL1 260°C (IR and Conection) PbF Reflow Compatible



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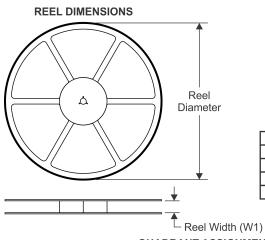
REVISION HISTORY

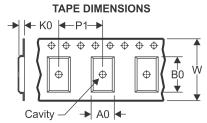
Changes from Original (August 2009) to Revision A	Page
Changed 300s to 300µs in Note 2 of the Abs Max Ratings table	
Changed Q _g Gate Charge Total (4.5V) - max value From: 2.3 To: 12.3	2
Changes from Revision A (October 2009) to Revision B	Page
Deleted the Package Marking Information section	8
Changes from Revision B (October 2010) to Revision C	Page
Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table	2
Changed the CSD25401Q3 Package Dimensions section	6
Changed the Recommended PCB Pattern section	7

PACKAGE MATERIALS INFORMATION

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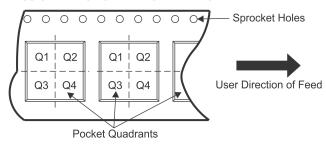
TAPE AND REEL INFORMATION





A0	
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

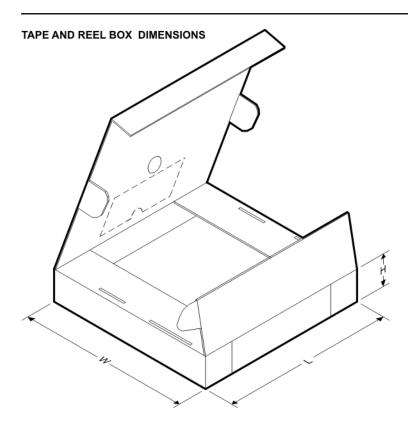
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25401Q3	VSON- CLIP	DQG	8	2500	330.0	12.8	3.6	3.6	1.2	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25401Q3	VSON-CLIP	DQG	8	2500	335.0	335.0	32.0

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