QorIQ Multicore Processor Development

P3041 Development System

BUILT ON Power

Overview

The P3041DS is a flexible development system supporting the quad-core P3041 device. With its 1.5 GHz P3041 and rich input/output (I/O) mix, the board is intended for development of P3041 in networking and Ethernet-centric applications, such as control plane and mixed control plane/data plane in switches, routers, base station network interface cards, aerospace and defense and factory automation.

The P3041DS can help shorten your time to market. The board, which exercises most capabilities of the device, can serve as a reference for the customer's hardware development. It can also be used as a debug tool to check behaviors on the board compared to behaviors seen on customer boards. It can be used for software development and performance evaluation before the customer's board is ready.

The P3041 processor is based upon the e500mc core, built on Power Architecture® technology, offering speeds of 1200–1500 MHz. It has a three-level cache hierarchy with 32 KB of instruction and data cache per core, 128 KB of unified backside L2 cache per core and 1 MB of shared frontside CoreNet platform cache fronting the memory controller. I/Os include 18 SerDes lanes running at up to 5 GHz, multiplexed across four PCI Express® Gen2 controllers, one 10 gigabit Ethernet (GE) XAUI interface, four 1 GE SGMII interfaces, four 2.5 Gbps SGMII interfaces, two Serial RapidIO (version 1.3 with features of version 2.1) interfaces, two SATA 2.0 interfaces and the high-speed Aurora debug interface. It has a 64-bit DDR3 and DDR3L (low power) DRAM interface with 8-bit ECC support running at a data rate up to 1333 MHz. It includes two USB 2.0 interfaces (including PHY), two dual universal asynchronous receiver/transmitters (DUARTs), an SD/MMC interface, a 32-bit local bus, four I^2C and SPI. It also includes the accelerator blocks collectively known as the Data Path Acceleration Architecture (DPAA) that offload various tasks from the core, including routine packet handling, security algorithm calculation and pattern matching.

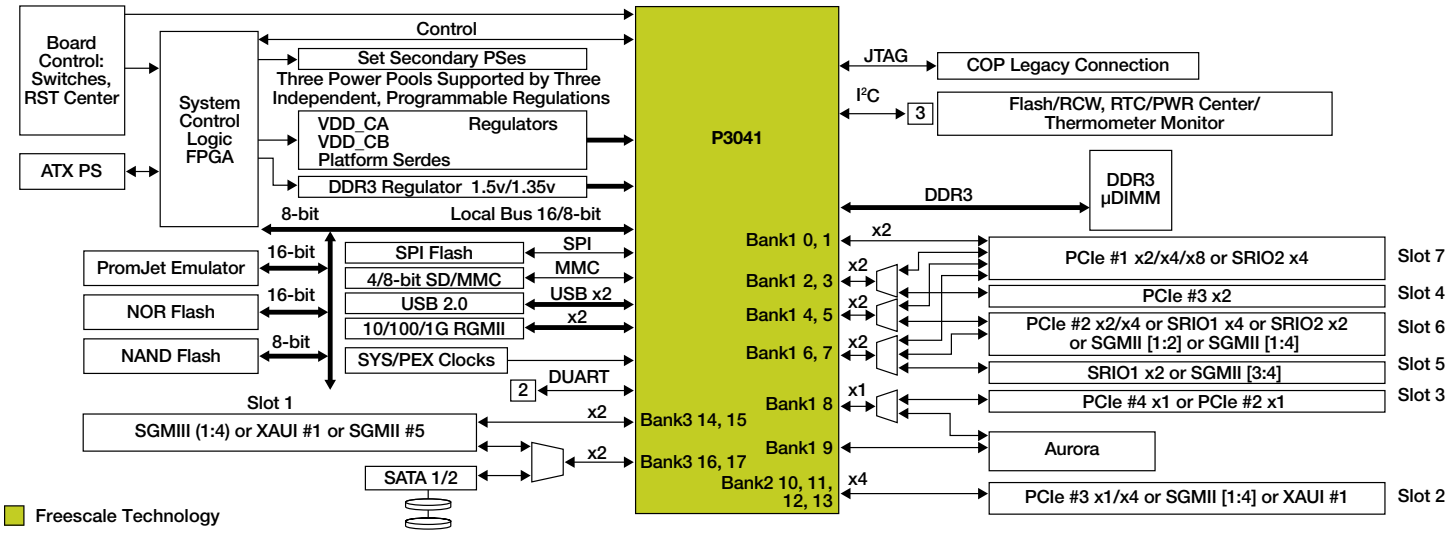
The P3041DS offers significant flexibility in allocating its 18 SerDes lanes to various functions. Its base configuration supports two RGMII ports, two PCI Express x4 slots (two lanes per slot), a x4 slot for Freescale's optional SGMII-PEX-RISER, a x4 slot for Freescale's optional XAUI-RISER, the Aurora high-speed debug port and two SATA ports. It can also be configured to support up to four PCI Express slots of widths up to x8.

The P3041DS memory system supports 2 GB of DDR3 at 1333 MHz. It has 128 MB of NOR flash, 1 GB of NAND flash, a 256 KB I^2C EEPROM as well as 16 MB of flash and 128 KB EEPROM of SPI-based memory. It also includes two USB 2.0 receptacles and an SD card slot.

The P3041DS is pre-loaded with an Embedded Linux Essentials for QorIQ Processors with Data Path Acceleration development kit. This kit includes a 2.6.x.x SMP Linux kernel, hugetlbfs for applications with a large memory footprint, user space DPAA for high-performance packet handling, u-boot, the GCC tool chain and Mentor System Builder, among many other features.

freescale™ QorIQ

P3041DS



P3041DS Board Features

Processor

- P3041, 1.5 GHz core with 1333 MHz DDR3 data rate
- Multiple SysClk inputs for generating various device frequencies

Memory

- 2 GB unbuffered DDR3 240-pin µDIMM module with ECC (72-bit bus), 1333 MHz data rate
- 128 MB NOR flash
- 1 GB NAND flash
- SPI-based 128 MB flash
- SPI-based 128 KB EEPROM
- SD connector to interface with an SD memory card

PCI Express

- Six x4 PCI Express slots
- Can support Freescale's XAUI-RISER and SGMII-PEX-RISER option cards

SATA

- Two vertical SATA connectors

USB 2.0

- Two High-Speed USB controllers
- One Type A and one MicroAB receptacle

Ethernet

- Supports two 10/100/1000 ports with no add-in cards
- dTSEC4 and dTSEC5 as RGMII to Vitesse VSC8244 PHY
- Optional SGMII-PEX-RISER expands 10/100/1000 port count to five
- 10 GE supported with optional XAUI-RISER card

DUART

- Two DUARTs

Debug

- JTAG/COP
- Aurora high-speed connector

Other

- IEEE® 1588 connector for Symmetricom option card
- Temperature sensor
- Eight general-purpose I/Os

For more information, visit freescale.com/QorIQ

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