CMOS 8–Bit Microcontrollers

TMP90P802AP/TMP90P802AM

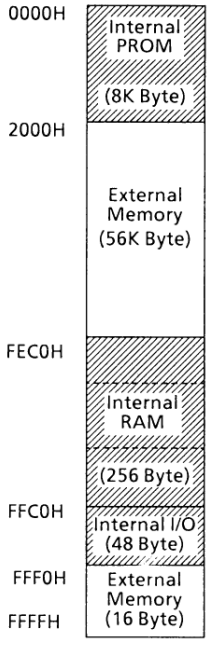
1. Outline and Characteristics

The TMP90P802A is a system evaluation LSI having a built in One-Time PROM for TMP90C802A.

A programming and verification for internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP90C802A by programming to the internal PROM.

The following are the memory map of TMP91C640 and TMP90C840A.



TMP90P802A Memory Map

Parts No.	ROM	RAM	Package	Adapter Socket No.
TMP90P802AP	OTP 8192 x 8bit	256 x 8bit	40-DIP	BM1158
TMP90P802AM			40-DIP	BM1159

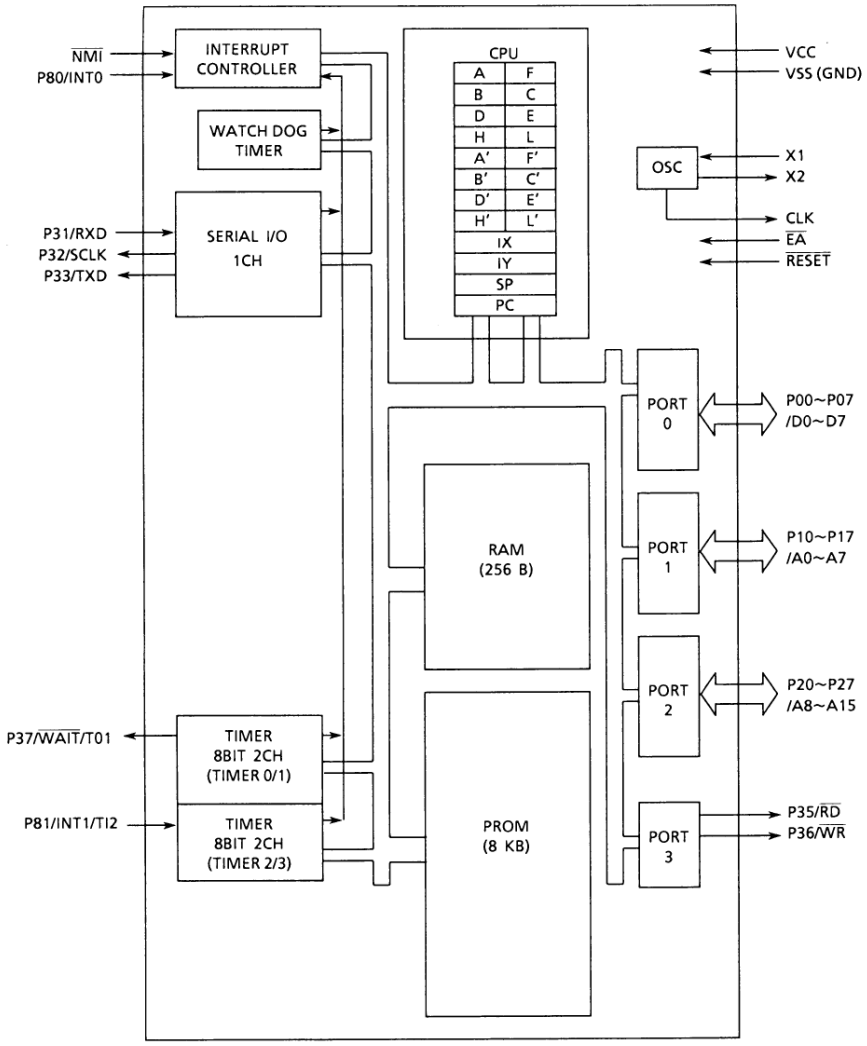


Figure 1. TMP90C802A Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP90P802A.

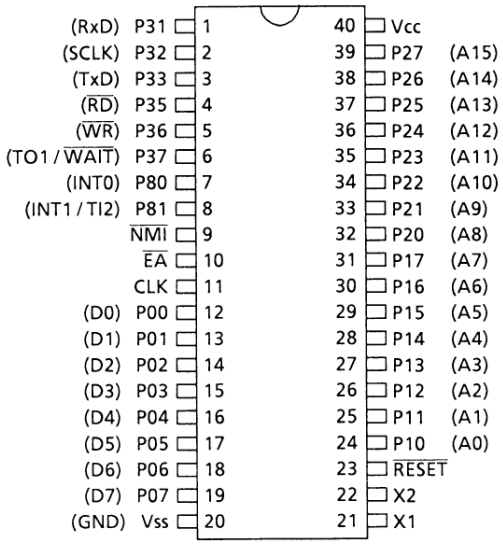


Figure 2.1 (1). Pin Assignment

Figure 2.1 (2) shows pin assignment of the TMP90P802A.

2.2 Pin Names and Functions

The TMP90P802A has MCU mode and PROM mode.

(1) MCU Mode (The TMP90P802A and the TMP90C802A are pin compatible).

Table 2.2 Pin Names and Functions

Pin Name	No. of pins	I/O 3 states	Function
P00 ~ P07 /D0 ~ D7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
		3 states	Data Bus: Also functions as 8-bit bidirectional data bus for external memory
P10 ~ P17 /A0 ~ A7	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
		Output	Addrress Bus: The lower 8 bits address bus for external memory
P20 ~ P27 /A8 ~ A 15	8	I/O	Port 2: 8-bit I/O port that allows selection on byte basis
		Output	Addrress Bus: The uppper 8 bits address bus for external memory
P31 /RxD	1	Input	Port 31: 1-bit input port
			Receives serial data
P32 /TxD /$\overline{\text{RTS}}$ /SCLK	1	Output	Port 32: 1-bit output port
			Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port
			Transmits serial data
P35 /$\overline{\text{RD}}$	1	Output	Port 35: 1-bit output port
			Read: Generates strobe signal for reading external memory
P36 /$\overline{\text{WR}}$	1	Output	Port 36: 1-bit output port
			Writes: Generates strobe signal for writing external memory
P37 /$\overline{\text{WAIT}}$	1	Input	Port 37: 1-bit input port
			Wait: Input pin for connecting slow speed memory or peripheral LSI
P80 /INT0	1	Input	Port 80: 1-bit input port
			Interrupt request pin 0: Interrupt request pin (Level/rising edge is programmable) 
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port
			Interrupt request pin 1: Interrupt request pin (Rising/falling edge is programmable) 
			Timer input 4: Counter/capture trigger signal for Timer 4
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin 
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
$\overline{\text{EA}}$	1	Input	Connects with V_{CC} pin .
$\overline{\text{RESET}}$	1	Input	Reset: Initializes the TMP90P802A (Built-in pull-up resistor)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator (1 ~ 12.5MHz)
V_{CC}	1	–	Power supply (+5V)
V_{SS} (GND)	1	–	Ground (0V)

2) PROM Mode

Table 2.2.2

Pin Function Name	No. of pins	I/O	Function	Pin Name (MCU mode)
A7 ~ A0	8	Input	Address Input	P17 ~ P10 P24 ~ P20
A12 ~ A8	5	Input		
A15 ~ A13	3	Input	Be fixed to "L" level.	P27 ~ P25
D7 ~ D0	8	I/O	Data Input/Output	P07 ~ P00
$\overline{OE}$	1	Input	Output Enable Input	P35
$\overline{CE}$	1	Input	Chip Enable Input	P36
VPP	1	Power Supply	12.5V/5V (Programming Power Supply)	$\overline{EA}$
VCC	1	Power Supply	5V	
VSS	1	Power Supply	0V	
Pin Name	**No. of pins**	**I/O**	**Pin Setting**	
P31	1	Input	Be fixed level.	
P32 ~ P34	3	Output	Open	
P37	1	Input	Be fixed level.	
P80 , P81	2	Input	Be fixed to "H" level.	
$\overline{NMI}$	1	Input	Be fixed to level.	
$\overline{RESET}$	1	Input	Be fixed to "L" level.	
CLK	1	Input	Be fixed to "L" level.	
X1	1	Input	Resonator connection pin	
X2	1	Output		

3. Operation

The TMP90P802A is the OTP version of the TMP90C802A that is replaced an internal ROM from Mask ROM to EPROM.

The function of TMP90P802A is exactly same as that of TMP90C840A.

Refer to the TMP90C802A except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in the relation to the TMP90P802A.

The TMP90P802A has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

In the MCU mode, the operation is the same as that of TMP90C802A.

(2) Memory Map

Figure 3.1 shows the memory map of TMP90P802A, and the accessing area by the respective addressing mode.

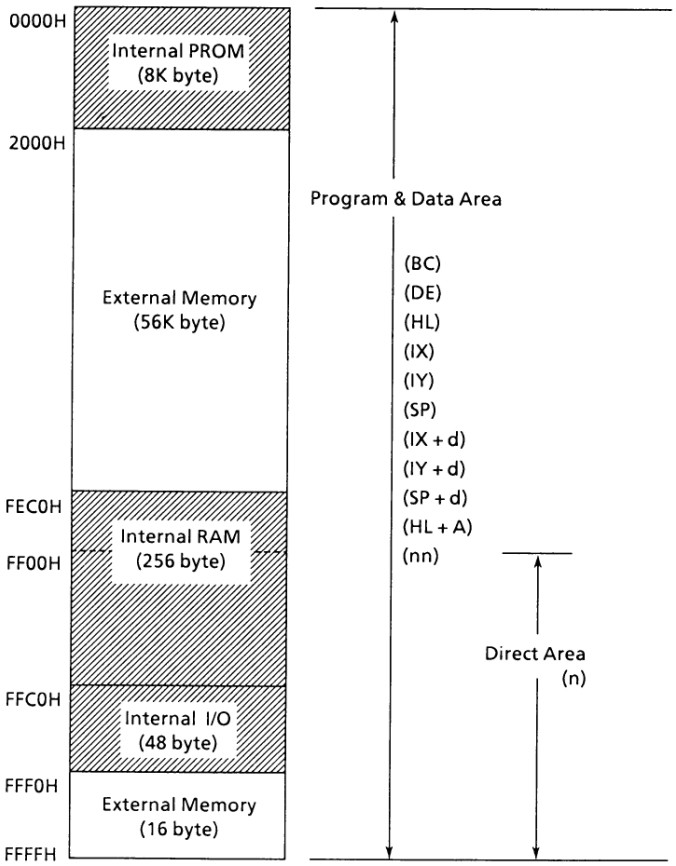


Figure 3.1. TMP90P802A Memory Map

3.2 PROM Mode

(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level.

The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket. The device selection (ROM Type) should be "27256" with following conditions.
size : 256Kbit (32K x 8-bit) VPP: 12.5V TPW: 1ms
Figure 3.2 shows the setting of pins in PROM mode.

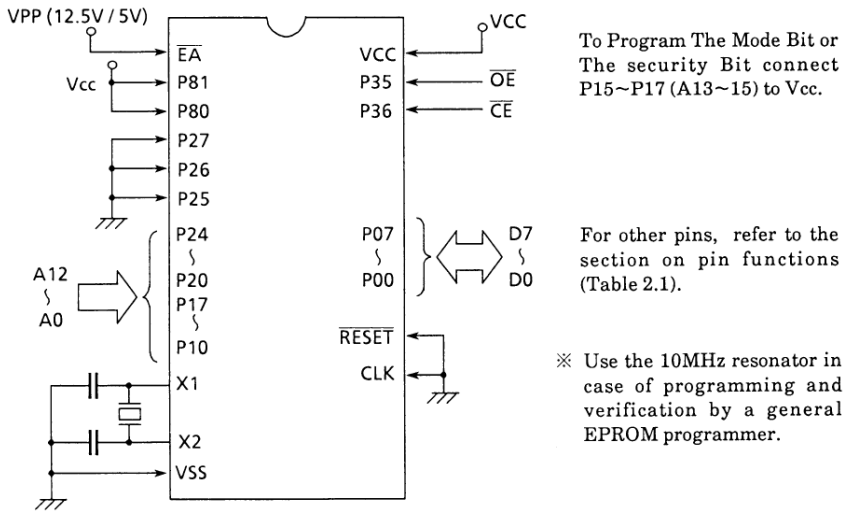


Figure 3.2. PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

(Vcc : 6.0V) *These conditions can be
($\overline{\text{RESET}}$: "L" level) obtained by using adaptor
(CLK : "L" level) socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the $\overline{\text{CE}}$ pin is set to "Low" (1ms plus is required).

General Programming procedure of an EPROM programmer is as follows,

- Write a data to a specified address for 1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writing is performed by using three times longer programming pulse width (1ms x programming times), or using three times more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of Vpp = Vcc = 5V after all data were written.

Figure 3.3 shows the programming flow chart.

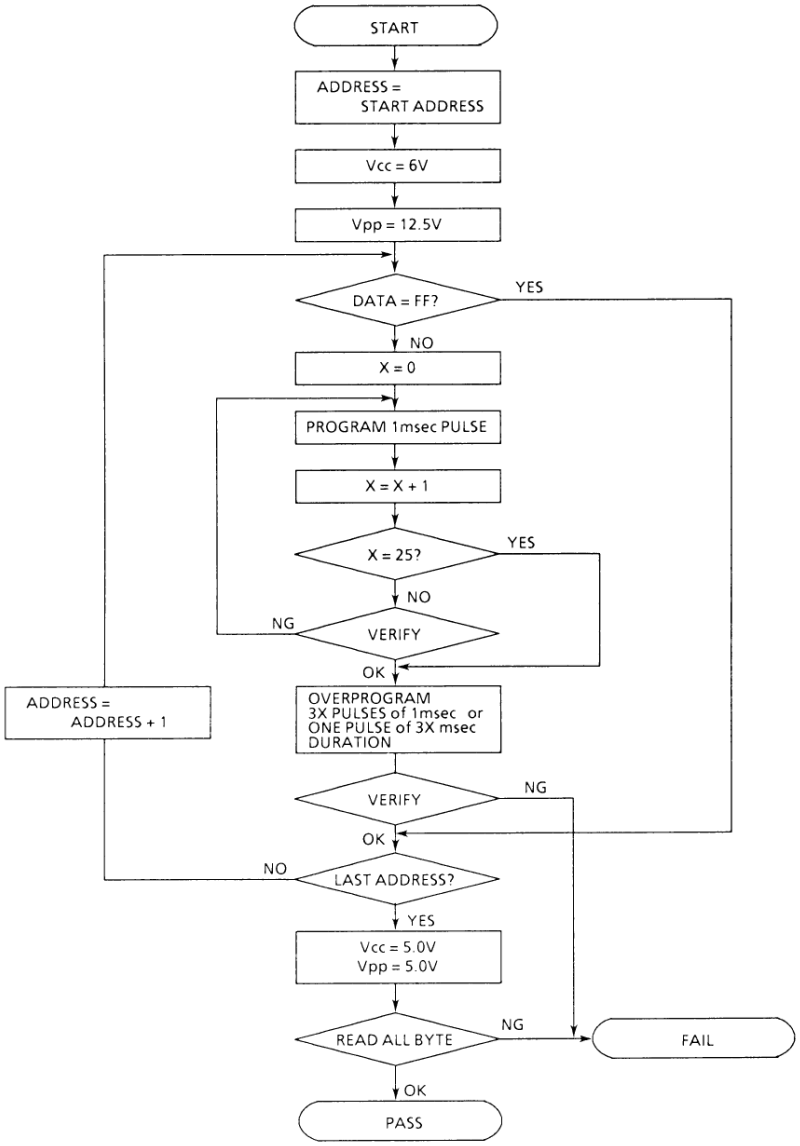


Figure 3.3. Flow Chart

(3) The Mode Bit and the Security Bit

The TMP90P802A has the Security Bit in PROM cell. If the Sercuity Bit is programmed to "0", the content of the PROM is disable to read in PROM mode.

How to Program the Security Bit.

1) Connect A15 pins to V_{CC}. [Otherwise connect them to GND to program PROM]
2) Set programming address to 0000H.
3) To program the Security Bit, set D0 to "0".
4) Set D2 ~ D7 to "1" respectively.

The following table shows the 8-bit data to program The Security Bit.

Table 3.1 Data to Program

Bit to Program	D0 ~ D7	A0 ~ A12	A13, A14, A15
The Security Bit	FEH	All "0"	A13, A14 = "0" A15 = "1"
PROM (0000H ~ 1FFFH)	–	–	All "0"

4. Electrical Characteristics

TMP90P802AP/TMP90P802AM

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 ~ + 7	V
V_{IN}	Input voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power dissipation (Ta = 85°C)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	-65 ~ 150	°C
T_{OPR}	Operating temperature	-40 ~ 85	°C

4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70° (1 ~ 16MHz)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P2, P3, P8	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, INT0, $\overline{NMI}$	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input Low Voltage (D0 ~ D7)	2.2	V_{CC} + 0.3	V	–
V_{IH1}	P1, P2, P3, P8	$0.7V_{CC}$	V_{CC} + 0.3	V	–
V_{IH2}	$\overline{RESET}$, INT0, $\overline{NMI}$	$0.75V_{CC}$	V_{CC} + 0.3	V	–
V_{IH4}	X1	$0.8V_{CC}$	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	–	V V V	I_{OH} = -400μA I_{OH} = -100μA I_{OH} = -20μA
I_{DAR}	Darlington Drive Current (8 I/O pins)	-1.0	-3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	17 (Typ) 1.5 (Typ) 6 (Typ)	30 5 15	mA mA mA	tosc = 10MHz (25% Up @ 12.5MHz)
	STOP (TA = -20 ~ 70°C) STOP (TA = 0 ~ 50°C)	0.2 (Typ)	50 10	μA μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	6	KΩ	V_{IL2} = 0.2V_{CC}, V_{IH2} = 0.8V_{CC}
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	0.4	1.0 (Typ)	V	–

Note: I_{DAR} is guaranteed for a total of up to 8 optional ports.

4.3 AC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	OSC. Period = x	80	1000	100	–	80	–	ns
t_{CYC}	CLK Period	4x	4x	400	–	320	–	ns
t_{WL}	CLK Low width	2x - 40	–	160	–	120	–	ns
t_{WH}	CLK High width	2x - 40	–	160	–	120	–	ns
t_{AC}	Address Setup to $\overline{RD}$, $\overline{WR}$	x - 45	–	55	–	35	–	ns
t_{RR}	$\overline{RD}$ Low width	2.5x - 40	–	210	–	160	–	ns
t_{CA}	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x - 30	–	20	–	10	–	ns
t_{AD}	Address to Valid Data In	–	3.5x - 95	–	255	–	185	ns
t_{RD}	$\overline{RD}$ to Valid Data In	–	2.5x - 80	–	170	–	120	ns
t_{HR}	Input Data Hold After $\overline{RD}$	0	–	0	–	0	–	ns
t_{WW}	$\overline{WR}$ Low width	2.5x - 40	–	210	–	160	–	ns
t_{DW}	Data Setup to $\overline{WR}$	2x - 50	–	150	–	110	–	ns
t_{WD}	Data Hold After $\overline{WR}$	20	90	20	90	20	90	ns
t_{CWA}	$\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$	–	1.5x - 100	–	50	–	20	ns
t_{AWA}	Address to Valid $\overline{WAIT}$	–	2.5x - 130	–	120	–	70	ns
t_{WAS}	$\overline{WAIT}$ Setup to CLK	70	–	70	–	70	–	ns
t_{WAH}	$\overline{WAIT}$ Hold After CLK	0	–	0	–	0	–	ns
t_{RV}	$\overline{RD}$/$\overline{WR}$ Recovery Time	1.5x - 35	–	115	–	85	–	ns
t_{CPW}	CLK to Port Data Output	–	x + 200	–	300	–	260	ns
t_{PRC}	Port Data Setup to CLK	200	–	200	–	200	–	ns
t_{CPR}	Port Data Hold After CLK	100	–	100	–	100	–	ns
t_{CHCL}	$\overline{RD}$/$\overline{WR}$ Hold After CLK	x - 60	–	40	–	20	–	ns
t_{CLC}	$\overline{RD}$/$\overline{WR}$ Setup to CLK	1.5x - 50	–	100	–	70	–	ns
t_{CLHA}	Address Hold After CLK	1.5x - 80	–	70	–	40	–	ns
t_{ACL}	Address Setup to CLK	2.5x - 80	–	170	–	120	–	ns
t_{CLD}	Data Setup to CLK	x - 50	–	50	–	30	–	ns

- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 – D7)
  High $0.8V_{CC}$/Low $0.2V_{CC}$ (excluding D0 – D7)

4.4 Zero - Cross Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p - p
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	KHz

4.5 Serial Channel Timing - I/O Interface Mode

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x	–	800	–	640	–	ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x - 150	–	450	–	330	–	ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x - 120	–	80	–	40	–	ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0	–	0	–	0	–	ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid	–	6x - 150	–	450	–	330	ns

4.6 8-bit Event Counter

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	TI4 clock cycle	8x + 100	–	900	–	740	–	ns
t_{VCKL}	TI4 Low clock pulse width	4x + 40	–	440	–	360	–	ns
t_{VCKH}	TI4 High clock pulse width	4x + 40	–	440	–	360	–	ns

4.7 Interrupt Operation

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level pulse width 	4x	–	400	–	320	–	ns
t_{INTAH}	$\overline{NMI}$, INT0 High level pulse width 	4x	–	400	–	320	–	ns
t_{INTBL}	INT1, INT2 Low level pulse width 	8x + 100	–	900	–	740	–	ns
t_{INTBH}	INT1, INT2 High level pulse width 	8x + 100	–	900	–	740	–	ns

4.8 Read Operation (PROM Mode)

DC Characteristic, AC Characterisc

TA = -40 ~ 85°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	VPP Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	0.7 x V_{CC}	Vcc + 0.3	V
V_{IL1}	Input Low Voltage (A ~ A15, $\overline{CE}$, $\overline{OE}$)	–	-0.3	0.3 x V_{CC}	V
t_{ACC}	Address to Output Delay	C_L = 50pf	2.25TCYC + α	∠	ns

TCYC = 400ns (10MHz Clock)
α = 200ns

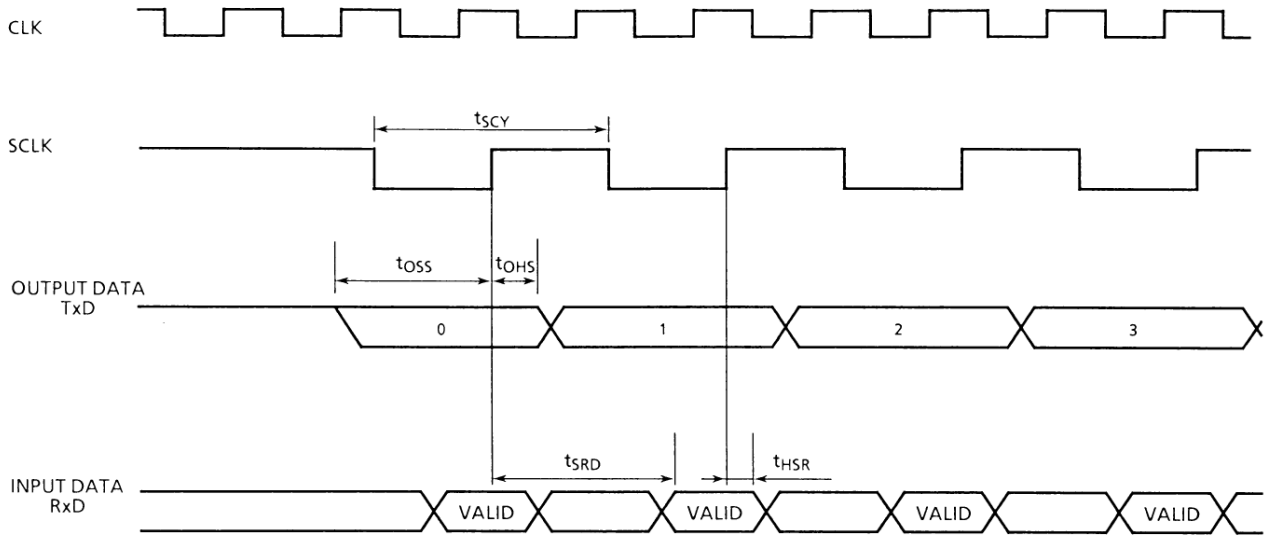
4.9 Programming Operation (PROM Mode)

DC Characteristic, AC Characteristic

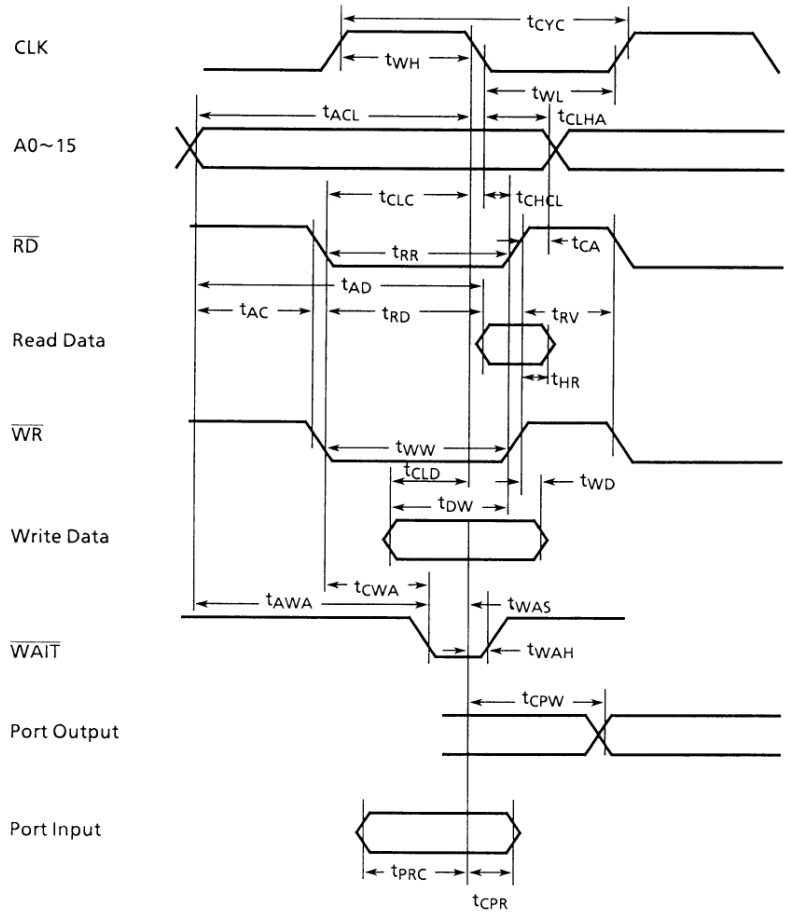
TA = 25 ± 5°C Vcc = 6V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Voltage	–	12.25	12.50	12.75	V
V_{IH}	Input High Voltage (D0 ~ D7)	–	0.2V_{CC} + 1.1		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 ~ D7)	–	-0.3		0.2V_{CC} - 0.1	V
V_{IH1}	Input High Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$)	–	-0.3		0.3V_{CC}	V
I_{CC}	V_{CC} Supply Current	t_{OSC} = 10MHz	–		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00V	–		50	mA
t_{PW}	$\overline{CE}$ Programming Pulse Width	C_L = 50p^F	0.95	1.00	1.05	ms

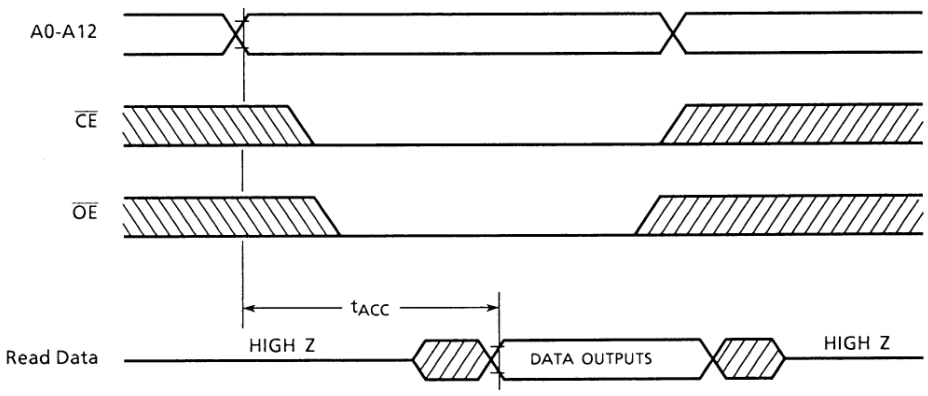
4.10 I/O Interface Mode Timing



4.11 Timing Chart



4.12 Read Operation Timing Chart (PROM Mode)



4.13 Programming Operation Timing Chart (PROM Mode)