



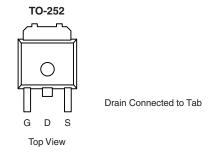
# N-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)			
100	$0.025 \text{ at V}_{GS} = 10 \text{ V}$	40			
100	$0.028$ at $V_{GS} = 4.5 \text{ V}$	38			

#### **FEATURES**

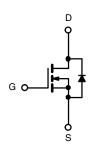
- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature
- 100 % R<sub>g</sub> Tested





Ordering Information: SUD40N10-25

SUD40N10-25-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage		$V_{DS}$	100	V		
Gate-Source Voltage			± 20			
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 25 °C	L	40			
Continuous Drain Current (1 <sub>J</sub> = 175 °C) <sup>2</sup>	T <sub>C</sub> = 125 °C	l <sub>D</sub>	23			
Pulsed Drain Current	I <sub>DM</sub>	70	Α			
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	40				
Avalanche Current	I <sub>AS</sub>	40				
Single Pulse Avalanche Energy (Duty Cycle ≤ 1 %)	L = 0.1 mH	E <sub>AS</sub>	80	mJ		
Maximum Daylar Dissination	T <sub>C</sub> = 25 °C	P <sub>D</sub>	136 <sup>b</sup>	W		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	r D	3 <sup>a</sup>	\ \v\		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C			

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Lunchion to Ambient	t ≤ 10 s	- R <sub>thJA</sub>	15	18	°C/W		
Junction-to-Ambient <sup>a</sup>	Steady State		40	50			
Junction-to-Case		R <sub>thJC</sub>	0.85	1.1			

#### Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See SOA curve for voltage derating.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply.

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static	•						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		3.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	μΑ	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	70			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		0.02	0.025	Ω	
5 h	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A, T <sub>J</sub> = 125 °C			0.05		
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A, T <sub>J</sub> = 175 °C			0.063		
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		0.022	0.028		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 40 A		70		S	
Dynamic <sup>a</sup>							
Input Capacitance	C <sub>iss</sub>			2400		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, F = 1 MHz		290			
Reverse Transfer Capacitance	C <sub>rss</sub>			120			
Total Gate Charge <sup>c</sup>	$Q_g$			40	60		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$		11		nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			9			
Gate Resistance	$R_{g}$		1		3.5	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			8	13		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V, R}_{L} = 1.25 \Omega$		40	60		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 40 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		15	25	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>			80	120		
Source-Drain Diode Ratings and Cha	racteristics 7	T <sub>C</sub> = 25 °C					
Pulsed Current	I <sub>SM</sub>				70	Α	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		1.0	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 40 A, dl/dt = 100 A/μs		75	120	ns	

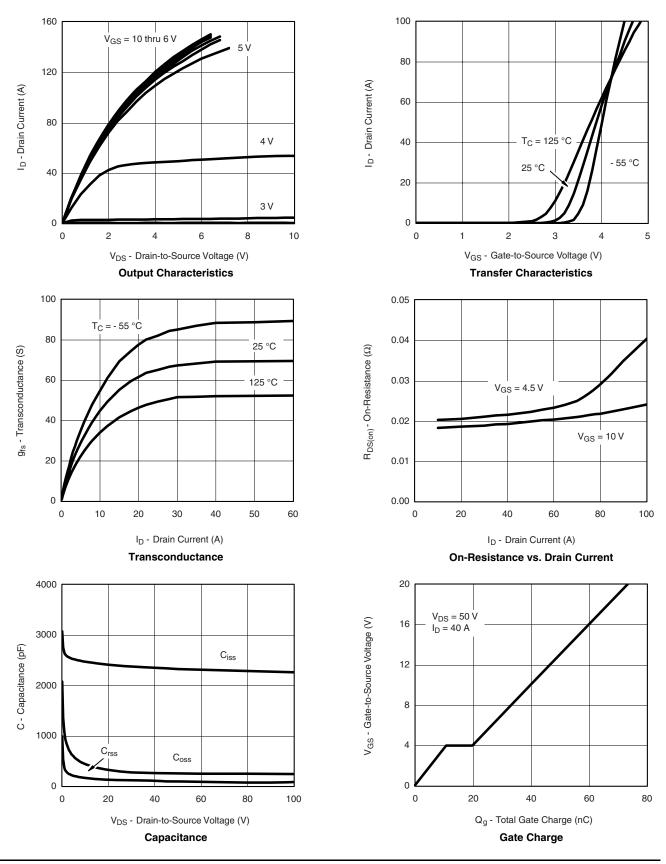
#### Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



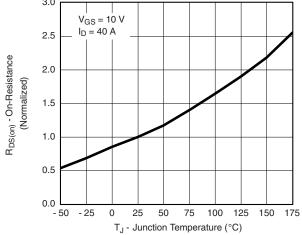
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



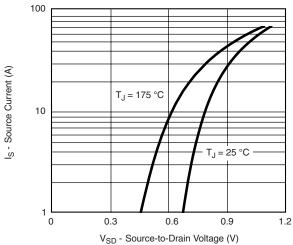
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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

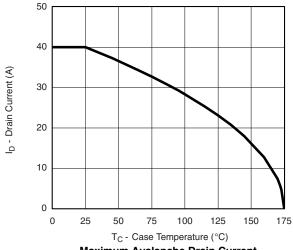


On-Resistance vs. Junction Temperature

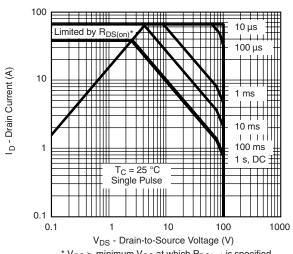


Source-Drain Diode Forward Voltage

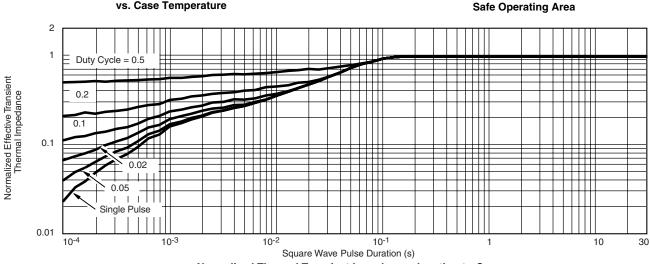
#### THERMAL RATINGS



Maximum Avalanche Drain Current vs. Case Temperature



 $^{\star}$   $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



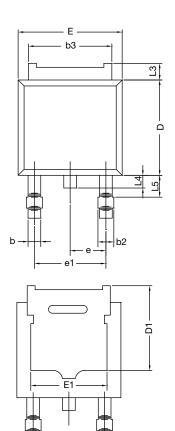
#### Normalized Thermal Transient Impedance, Junction-to-Case

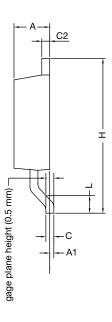
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71140.





## **TO-252AA Case Outline**



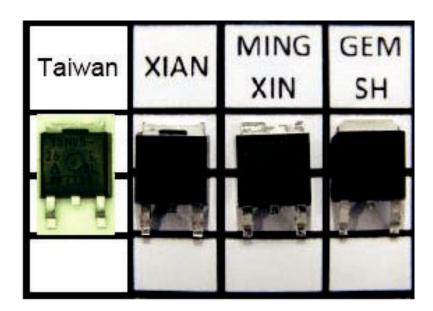


	MILLIMETERS		INC	HES		
DIM.	MIN.	MAX.	MIN.	MAX.		
Α	2.18	2.38	0.086	0.094		
A1	-	0.127	-	0.005		
b	0.64	0.88	0.025	0.035		
b2	0.76	1.14	0.030	0.045		
b3	4.95	5.46	0.195	0.215		
С	0.46	0.61	0.018	0.024		
C2	0.46	0.89	0.018	0.035		
D	5.97	6.22	0.235	0.245		
D1	4.10	-	0.161	-		
Е	6.35	6.73	0.250	0.265		
E1	4.32	-	0.170	-		
Н	9.40	10.41	0.370	0.410		
e	2.28 BSC		C 0.090 BSC			
e1	4.56	BSC	0.180 BSC			
L	1.40	1.78	0.055	0.070		
L3	0.89	1.27	0.035	0.050		
L4	-	1.02	-	0.040		
L5	1.01	1.52	0.040	0.060		
ECN: T13-0359-Rev. O, 03-Jun-13						

DWG: 5347

#### Notes

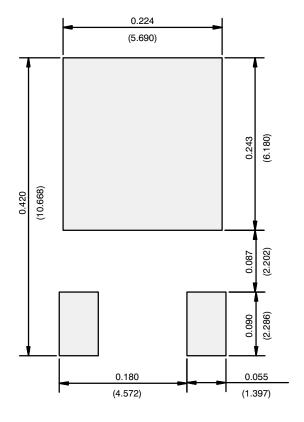
- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



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## **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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