3.3V ABT Octal bus transceiver/register (3-State) 74LVT646

FEATURES

- Combines 74LVT245 and 74LVT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6 and 200V per Machine Model

DESCRIPTION

The LVT646 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High.

Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low).

In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74LVT646.

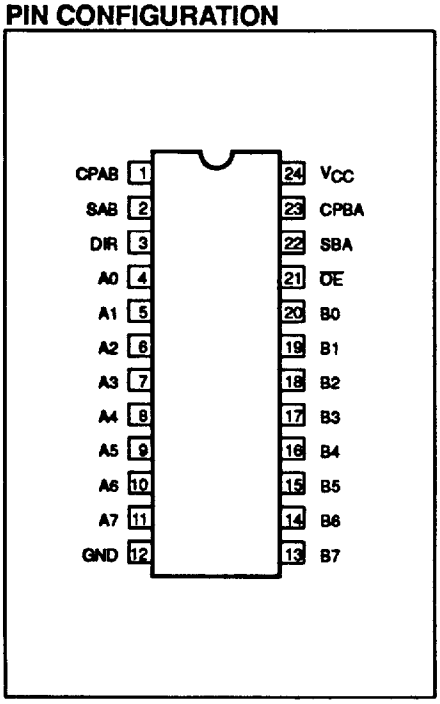
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{An}$ to $\overline{Bn}$ or $\overline{Bn}$ to $\overline{An}$	C_L = 50pF; V_{CC} = 3.3V ± 0.3V	2.8	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or 3.0V	4.5	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or 3.0V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

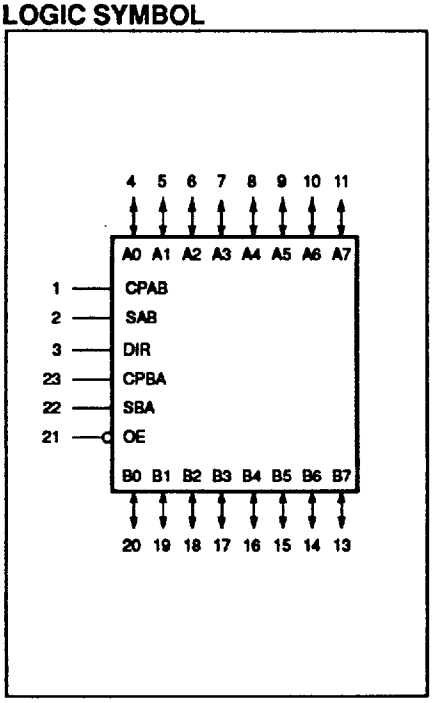
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT646D	0173D
24-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT646DB	1641A
24-Pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT646PW	TBD

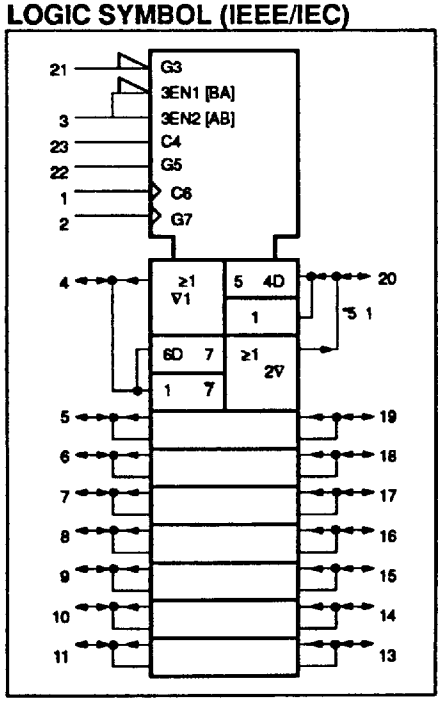
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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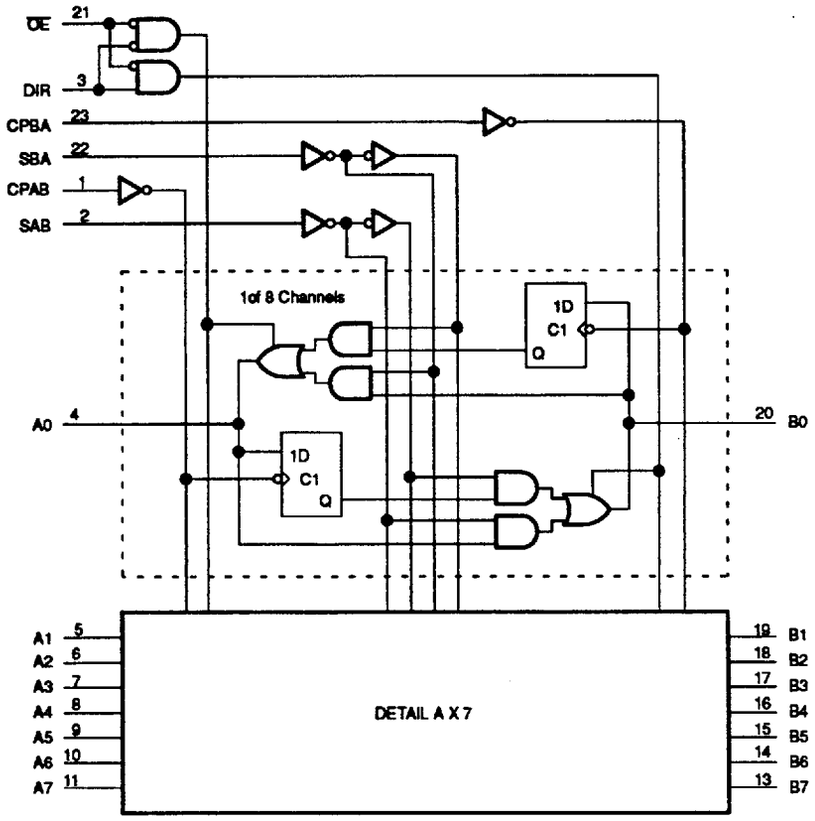
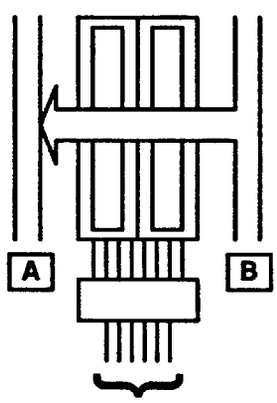
LOGIC DIAGRAM

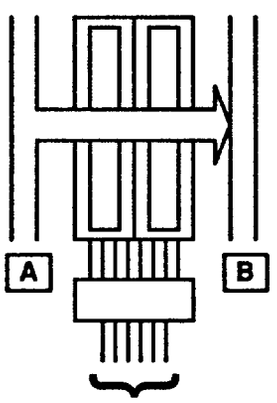


REAL TIME BUS TRANSFER BUS B TO BUS A



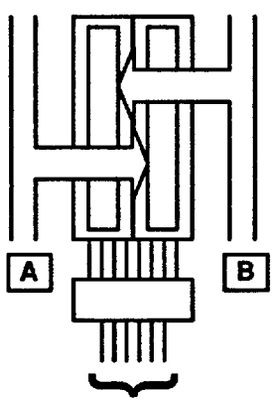
OE	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



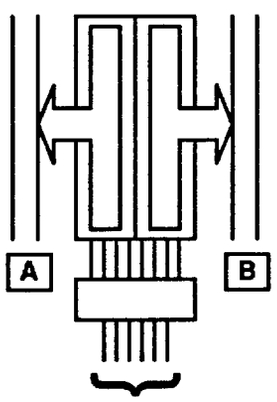
OE	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OE	DIR	CPAB	CPBA	SAB	SBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



OE	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

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ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]			20	
		V_{CC} = 3.6V; V_I = V_{CC}				1	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A or B ports	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = X				±100	µA
C_I	Input capacitance	V_I = 3V or 0			4		pF
C_O	Output capacitance	V_O = 3V or 0			11		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.3V with a transition time of up to 10msec. From V_{CC} = 1.3V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. X = Don't care.
4. Unused pins at V_{CC} or GND.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1					MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1		3.8 3.8			ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2		2.8 2.7			ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	2, 3		3.7 3.8			ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	5 6		3.0 3.2			ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	5 6		4.3 3.8			ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	5 6		3.4 3.4			ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	5 6		4.1 3.5			ns

NOTE:
1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

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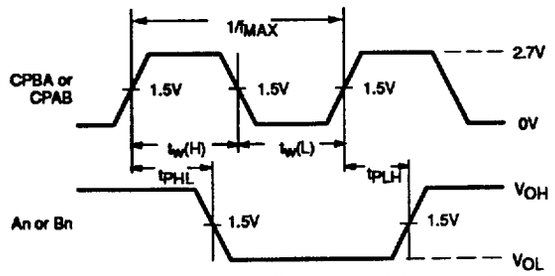
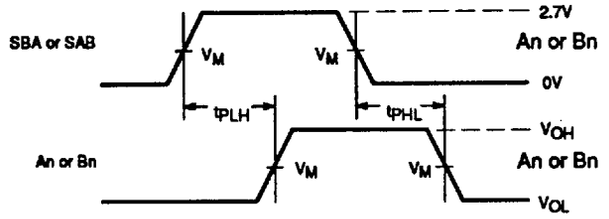
AC WAVEFORMS

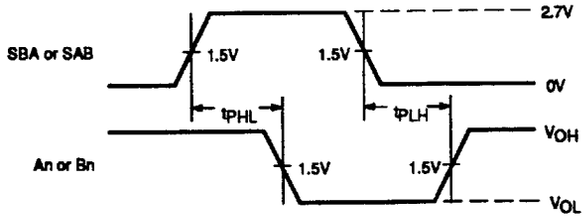
V_M = 1.5V, V_{IN} = GND to 2.7V



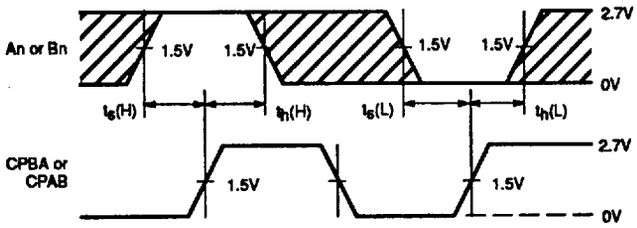
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



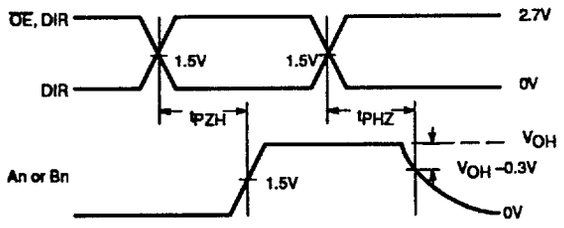
Waveform 2. Propagation Delay, SAB to Bn or SBA to An, An to Bn or Bn to An



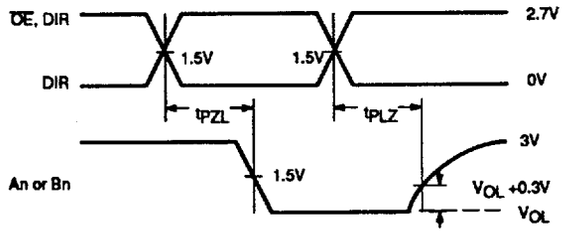
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

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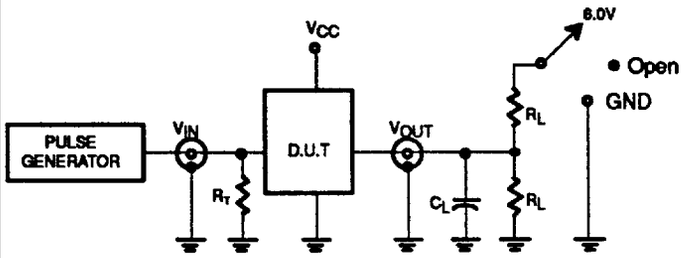
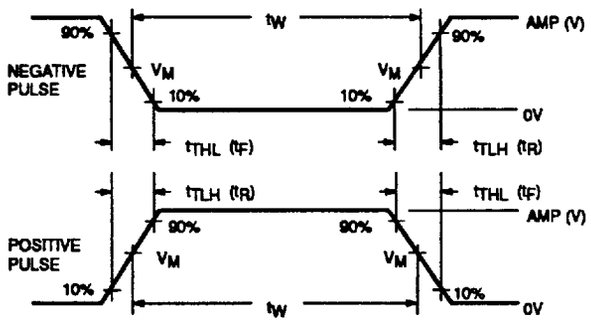
TEST CIRCUIT AND WAVEFORM



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns