

## 74ABT240

### Octal Buffer/Line Driver with 3-STATE Outputs

#### General Description

The ABT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

#### Features

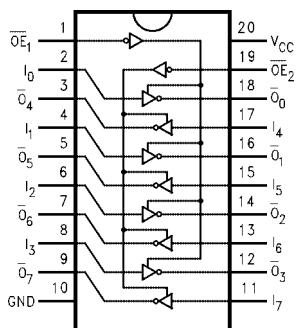
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

#### Ordering Code:

Order Number	Package Number	Package Description
74ABT240CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT240CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT240CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT240CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_1$ , $\overline{OE}_2$	3-STATE Output Enable Inputs
$I_0$ – $I_7$	Inputs
$\overline{O}_0$ – $\overline{O}_7$	Outputs

#### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings <sup>(Note 1)</sup>				Recommended Operating Conditions		
Storage Temperature	-65°C to +150°C			Free Air Ambient Temperature	-40°C to +85°C	
Junction Temperature under Bias	-55°C to +150°C			Supply Voltage	+4.5V to +5.5V	
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V			Minimum Input Edge Rate ( $\Delta V/\Delta t$ )		
Input Voltage (Note 2)	-0.5V to +7.0V			Data Input	50 mV/ns	
Input Current (Note 2)	-30 mA to +5.0 mA			Enable Input	20 mV/ns	
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V					
in the HIGH State	-0.5V to V <sub>CC</sub>					
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)					
DC Latchup Source Current (Across Comm Operating Range)	-150 mA			<b>Note 1:</b> Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.		
Over Voltage Latchup (I/O)	10V			<b>Note 2:</b> Either voltage limit or current limit is sufficient to protect inputs.		
DC Electrical Characteristics						
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	
V <sub>IL</sub>	Input LOW Voltage		0.8		V	
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.2		V	Min
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min
		2.0			V	Min
V <sub>OL</sub>	Output LOW Voltage		0.55		V	Min
I <sub>IH</sub>	Input HIGH Current		1	1	µA	Max
I <sub>BVI</sub>	Input HIGH Current Breakdown Test		7		µA	Max
I <sub>IL</sub>	Input LOW Current		-1	-1	µA	Max
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0
I <sub>OZH</sub>	Output Leakage Current		10		µA	0 - 5.5V
I <sub>OZL</sub>	Output Leakage Current		-10		µA	0 - 5.5V
I <sub>OS</sub>	Output Short-Circuit Current	-100	-275		mA	Max
I <sub>CEX</sub>	Output HIGH Leakage Current		50		µA	Max
I <sub>ZZ</sub>	Bus Drainage Test		100		µA	0.0
I <sub>CCH</sub>	Power Supply Current		50		µA	Max
I <sub>CCL</sub>	Power Supply Current		30		mA	Max
I <sub>CCZ</sub>	Power Supply Current		50		µA	Max
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input Outputs Enabled Outputs 3-STATE Outputs 3-STATE		1.5	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
				50	µA	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
					Max	Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
						All Others at V <sub>CC</sub> or Ground
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 3)	No Load		0.1	mA/ MHz	Max
						Outputs Open
						$\overline{OE}_n$ = GND, (Note 4)
						One Bit Toggling, 50% Duty Cycle

**Note 3:** Guaranteed, but not tested.**Note 4:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

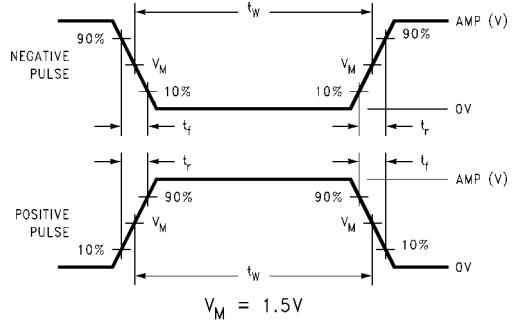
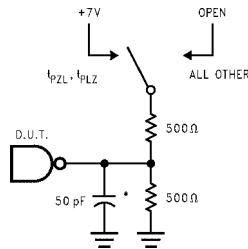
### AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ C$			$T_A = -55^\circ C$ to $+125^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$			Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay	1.0	4.8		0.8	5.5	1.0	4.8			
$t_{PHL}$	Data to Outputs	1.6	4.8		1.0	5.5	1.6	4.8			ns
$t_{PZH}$	Output Enable	1.1	6.2		0.8	7.5	1.1	6.2			
$t_{PZL}$	Time	1.1	6.2		0.8	7.7	1.1	6.2			ns
$t_{PHZ}$	Output Disable	1.8	6.4		1.0	7.5	1.8	6.4			
$t_{PLZ}$	Time	1.6	5.8		1.0	7.2	1.6	5.8			ns

### Capacitance

Symbol	Parameter	Typ	Units	Conditions	
				$T_A = 25^\circ C$	
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0V$	
$C_{OUT}$ (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$	

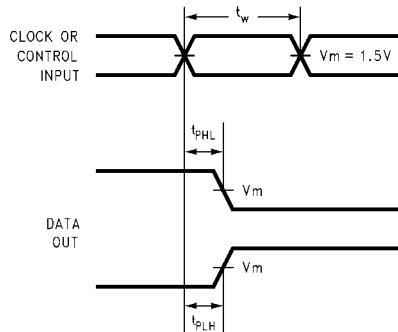
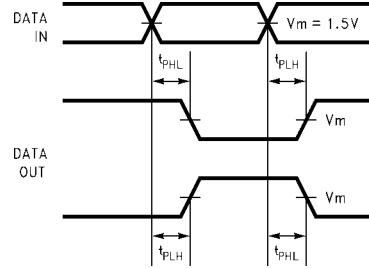
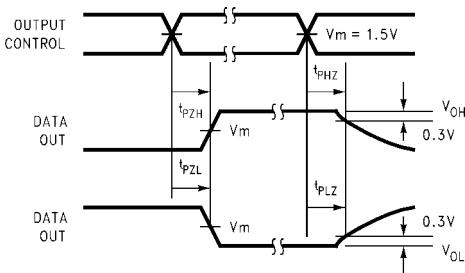
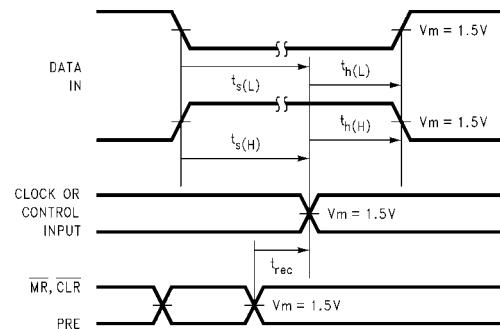
Note 5:  $C_{OUT}$  is measured at frequency  $f = 1$  MHz, per MIL-STD-883, Method 3012.

**AC Loading**

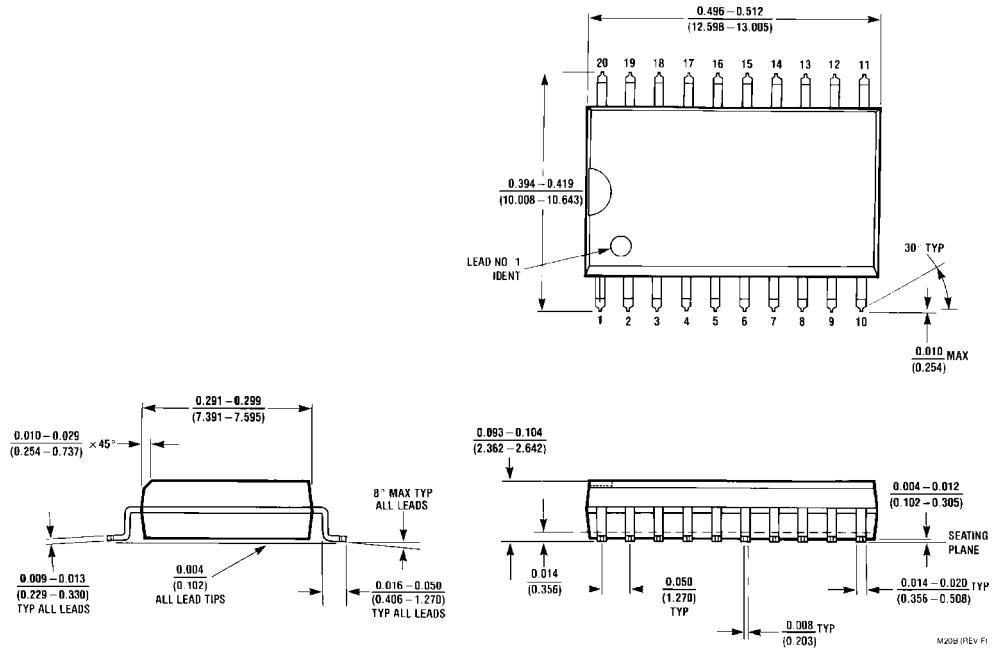
\*Includes jig and probe capacitance

**Standard AC Test Load**

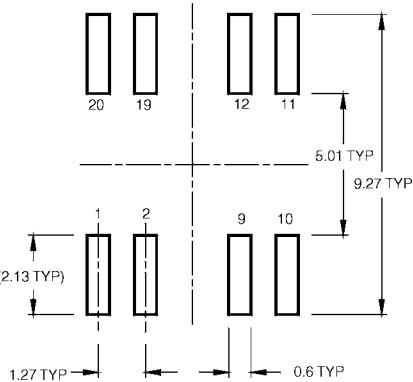
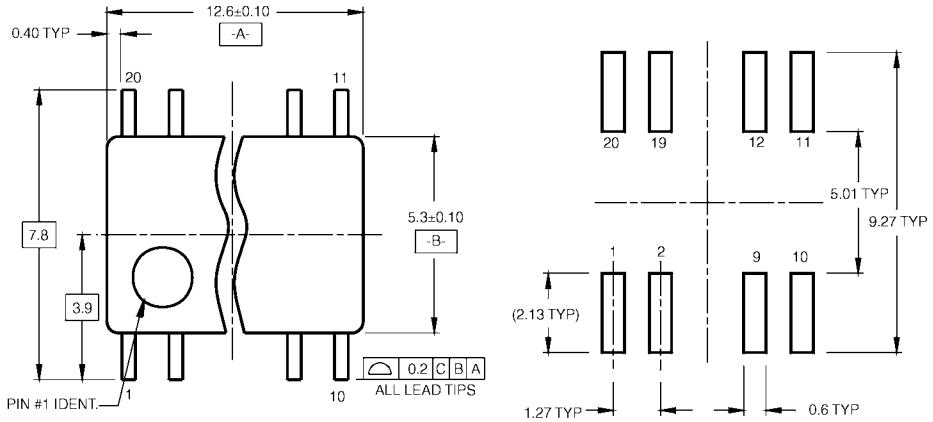
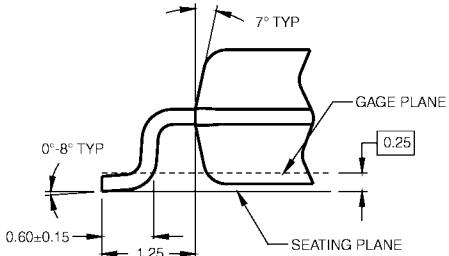
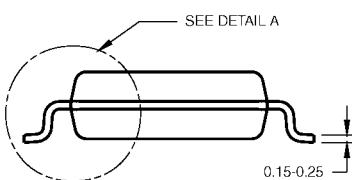
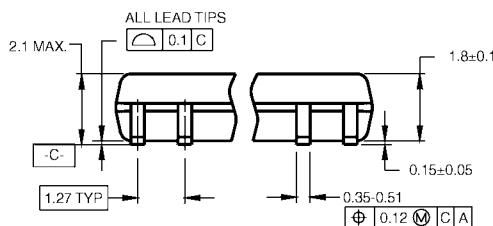
Amplitude	Rep. Rate	$t_W$	$t_f$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

**Test Input Signal Requirements****AC Waveforms****Propagation Delay,  
Pulse Width Waveforms****Propagation Delay Waveforms for  
Inverting and Non-Inverting Functions****3-STATE Output HIGH  
and LOW Enable and Disable Times****Setup Time, Hold Time  
and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

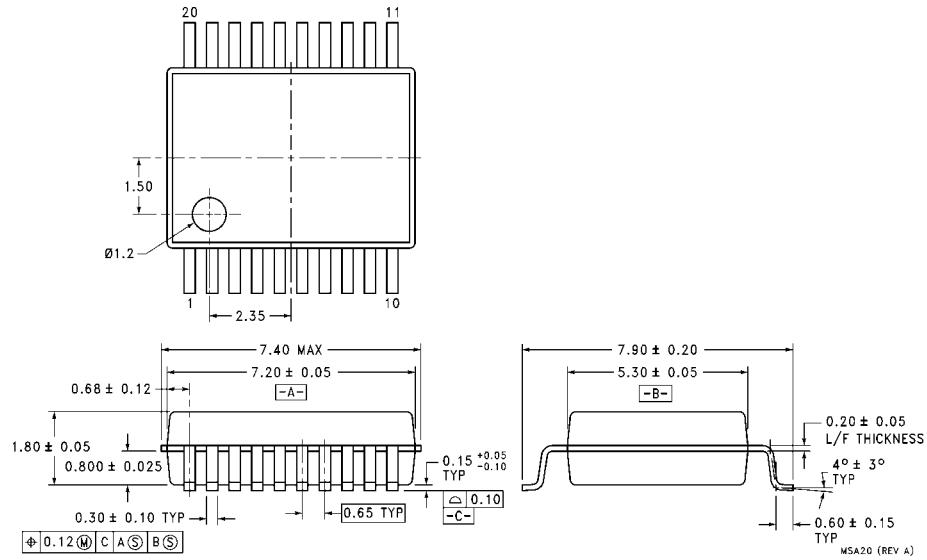
## NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

DETAIL A

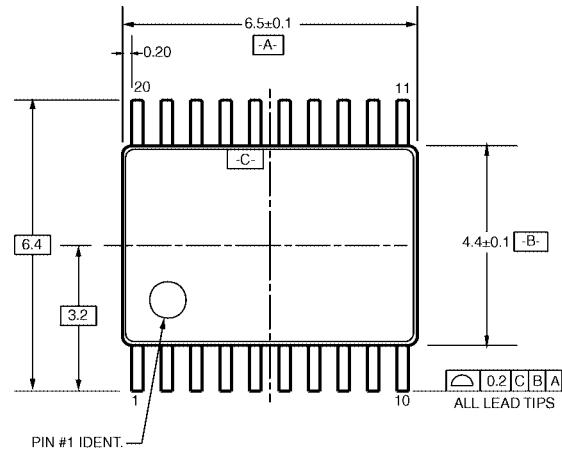
**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**  
**Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

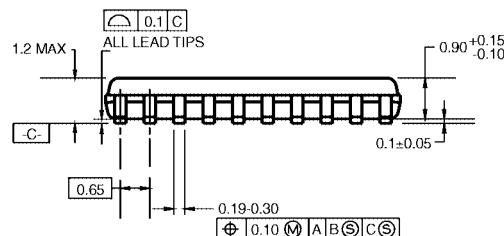
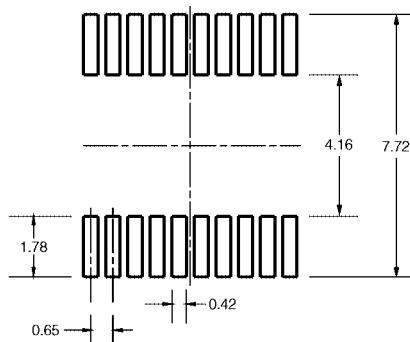
20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20

## 74ABT240 Octal Buffer/Line Driver with 3-STATE Outputs

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

#### NOTES:

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,  
REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND  
TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

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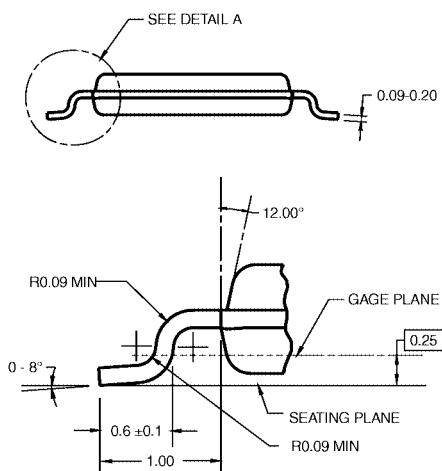
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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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#### DETAIL A