TSL1018

18 + 1 channel buffer for TFT-LCD panels

Features

- Wide supply voltage: 5.5V to 16.8V
- Low operating current: 8mA typical at 25°C
- Bandwidth at -3dB: 3.5MHz
- High output current COM amplifier: ±150mA
- Industrial temperature range: -40°C to +95°C
- Small package: TQFP48 ePad

Application

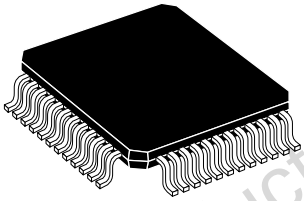
- TFT liquid crystal display (LCD)

Description

The TSL1018 is composed of 18 + 1 channel buffers which are used to buffer the reference voltage for gamma correction in thin film transistor (TFT) liquid crystal displays (LCD).

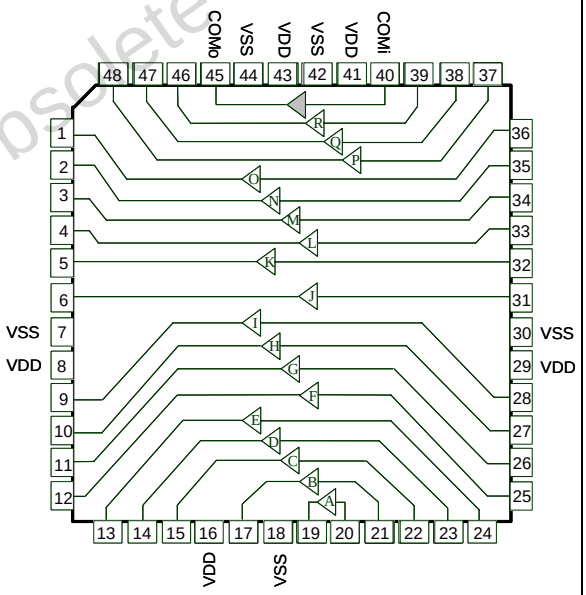
One "COM" amplifier is able to deliver high output current value, up to ±150mA. Amplifiers A and B feature positive single supply inputs for common mode voltage, thus can be used for highest gamma voltages. The amplifiers C to R inclusive, and the COM amplifier, feature negative single supply inputs and are dedicated to the lowest gamma voltages.

The TSL1018 is fully characterized and guaranteed over a wide industrial temperature range (-40 to +95°C).



7 x 7mm TQFP48 ePad

Pin connections (top view)



1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	18	V
V_{IN}	Input voltage	V_{SS} -0.5V to V_{DD} +0.5V	V
I_{OUT}	Output current (A to R buffers) Output current (COM buffer)	40 150	mA
R_{THJA}	Thermal resistance junction to ambient for TQFP48 ePad not thermally connected to PCB ePad thermally connected to PCB	 85 36	°C/W
P_D	Power dissipation(1) for TQFP48 ePad ePad not thermally connected to PCB ePad thermally connected to PCB	 1470 3470	mW
T_{LEAD}	Lead temperature (soldering 10 seconds)	260	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
ESD	Human body model (HBM)(2)	2000	V
	Machine model (MM)(3)	200	
	Charged device model (CDM) (4)	1500	

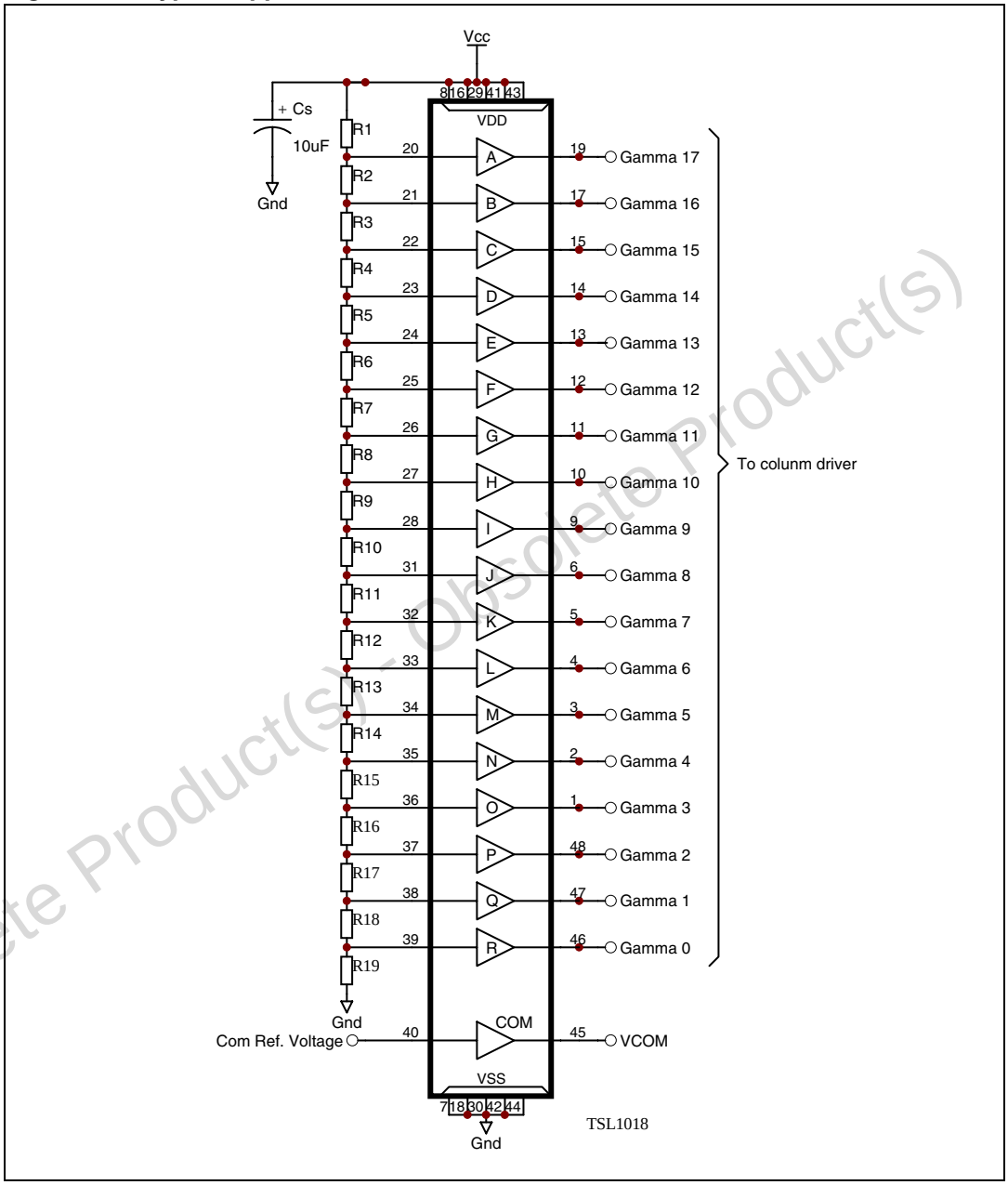
1. P_D is calculated with T_{amb} = 25°C, T_J = 150°C and R_{THJA} .
2. Human body model: a 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to the ground through only one pin.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{DD} - V_{SS})	5.5 to 16.8	V
T_{amb}	Ambient temperature	-40 to +95	°C
V_{IN}	Input voltages for buffers A & B	V_{SS} + 1.5V to V_{DD}	V
	Input voltages for buffers C to R & COM	V_{SS} to V_{DD} - 1.5V	

2 Typical application schematics

Figure 1. Typical application schematic for the TSL1018



Note that:

- Amplifiers **A** & **B** have their input voltages in the range V_{SS}+1.5V to V_{DD}. This is why they must be used for high level gamma correction voltages.
- Amplifiers **C to R** have their input voltages in the rangeV_{SS} to V_{DD}-1.5V. This is why they must be used for medium-to-low level gamma correction voltages.
- Amplifier COM has its input voltage range from V_{SS} toV_{DD}-1.5V.

3 Electrical characteristics

Table 3. Electrical characteristics for T_{amb} = 25°C , V_{DD} = +5V, V_{SS} = -5V, R_L = 10kΩ, C_L = 10pF (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	V_{ICM} = 0V			12	mV
ΔV_{IO}	Input offset voltage drift	-40°C < T_{amb} < +85°C		5		µV/°C
I_{IB}	Input bias current	V_{ICM} = 0V, buffers A & B V_{ICM} = 0V, buffers C to R & COM			140 70	nA
R_{IN}	Input impedance			1		GΩ
C_{IN}	Input capacitance			1.35		pF
V_{OL}	Output voltage low	I_{OUT} = -5mA Buffers C to P Buffers Q, R & COM		 -4.85 -4.92	 -4.80 -4.85	V
V_{OH}	Output voltage high	I_{OUT} = 5mA for buffers A & B	4.82	4.87		V
I_{OUT}	Output current	(A to R buffers)		±40		mA
		COM buffer		±150		
PSRR	Power supply rejection ratio	V_{CC}= 6.5 to 15.5V	80	100		dB
I_{CC}	Supply current	No load		8	11	mA
SR	Slew rate (rising & falling edge)	-4V < V_{OUT} < +4V 20% to 80%		1.1		V/µs
t_s	Settling time	Settling to 0.1%, V_{OUT}=2V step		5		µs
BW	Bandwidth at -3dB	R_L=10kΩ, C_L=10pF		3.5		MHz
G_m	Phase margin	R_L=10kΩ, C_L=10pF		60		degrees
C_s	Channel separation	f=1MHz		75		dB

Note: Limits are 100% production tested at 25°C. Behavior at the temperature range limits is guaranteed through correlation and by design.

Figure 2. Supply current vs. supply voltage for various temperatures

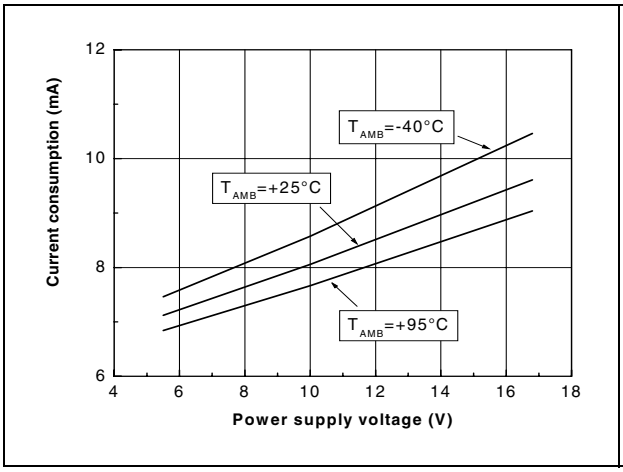


Figure 3. Output offset voltage (eq. V_{IO}) vs. temperature

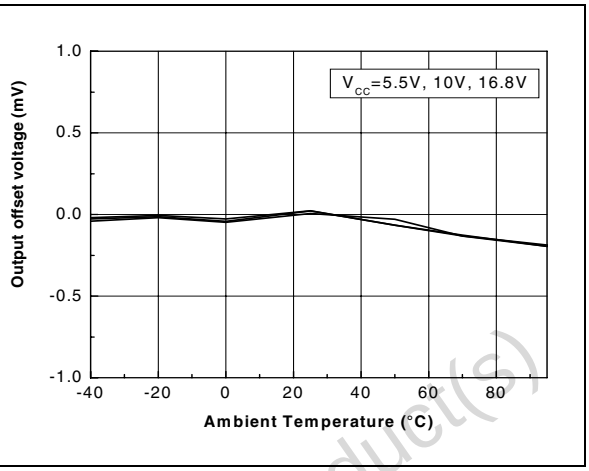


Figure 4. Input current (I_{IB}) vs. temperature

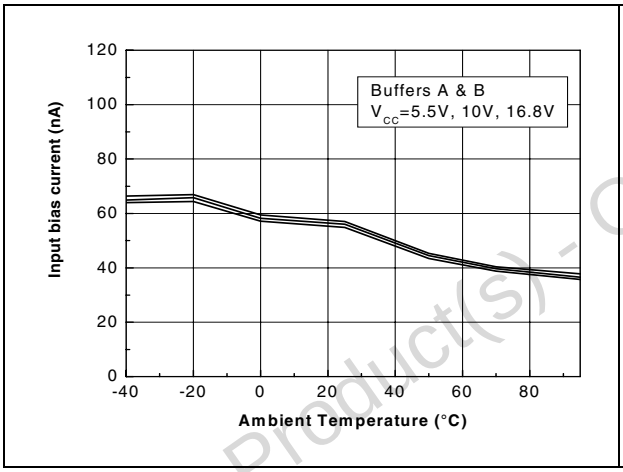


Figure 5. Input current (I_{IB}) vs. temperature

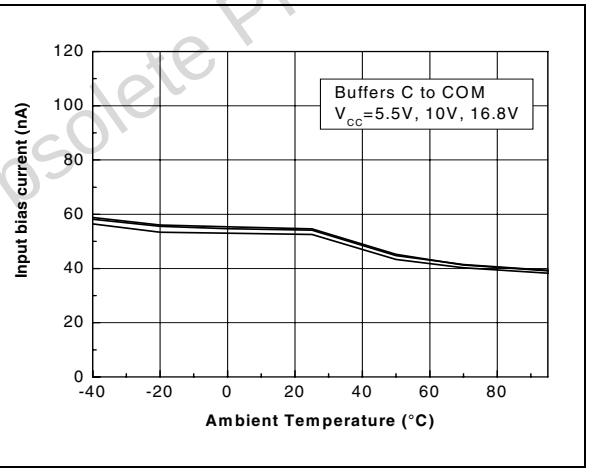


Figure 6. Output current capability vs. temperature

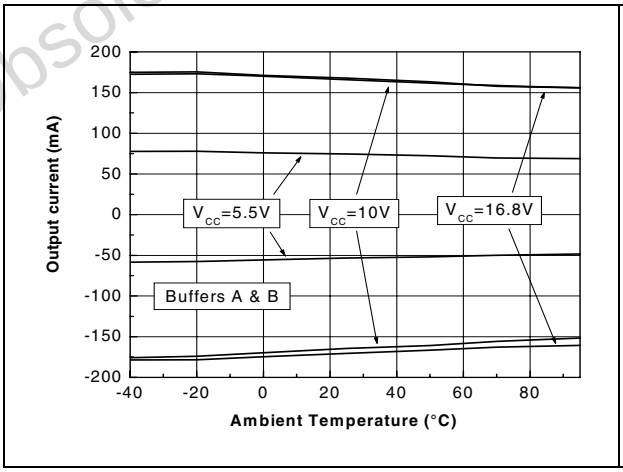


Figure 7. Output current capability vs. temperature

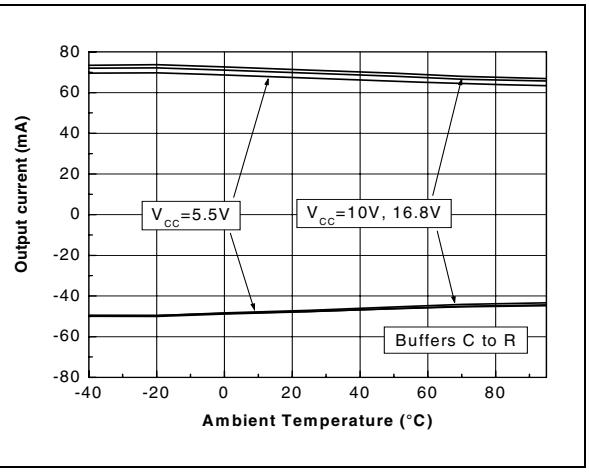


Figure 8. Output current capability vs. temperature

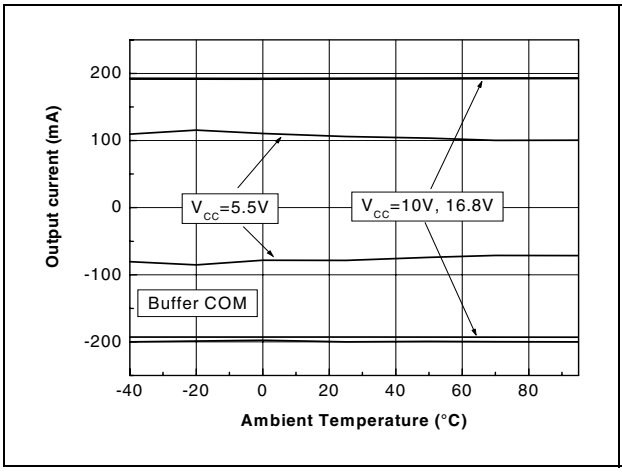


Figure 9. High level voltage drop vs. temperature

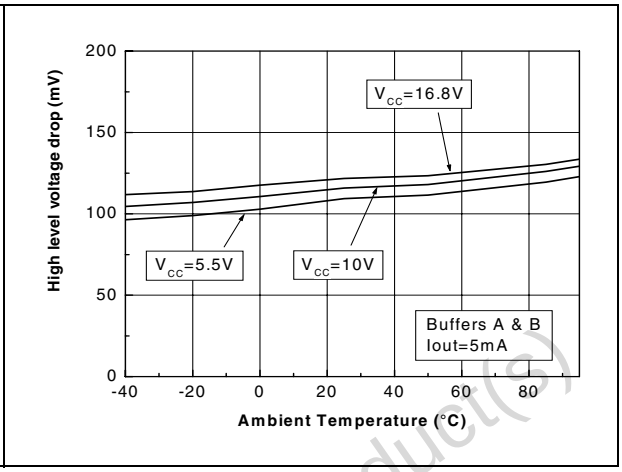


Figure 10. Low level voltage drop vs. temperature

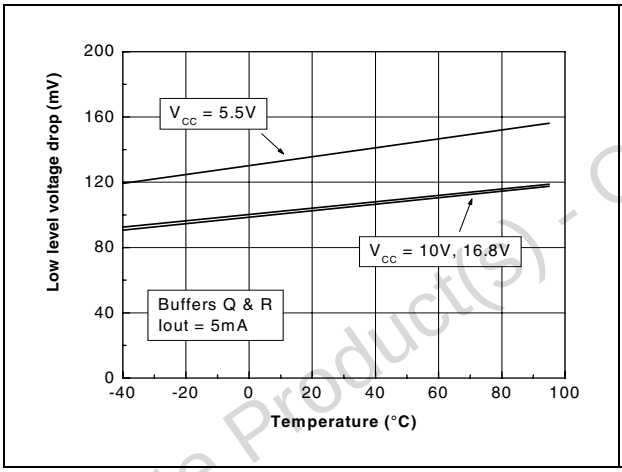


Figure 11. Low level voltage drop vs. temperature

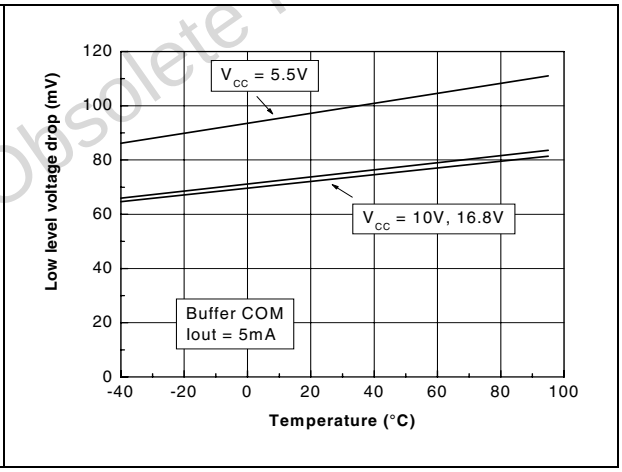


Figure 12. Voltage output high (V_{OH}) vs. output current - buffers A & B

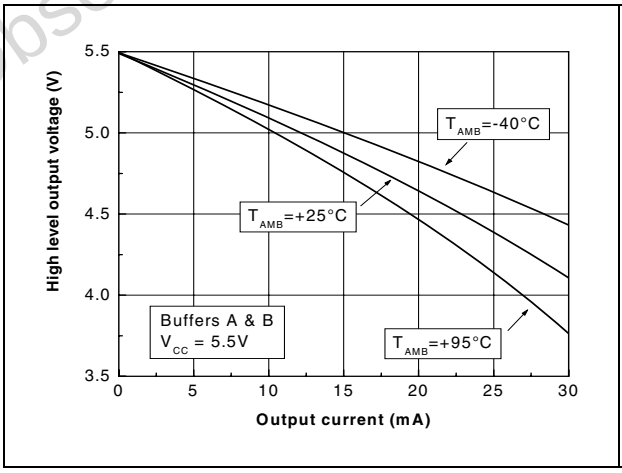


Figure 13. Voltage output high (V_{OH}) vs. output current - buffers A & B

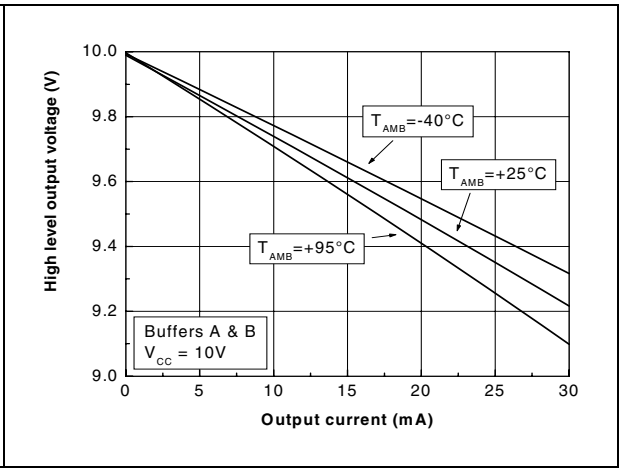


Figure 14. Voltage output high (V_{OH}) vs. output current - buffers A & B

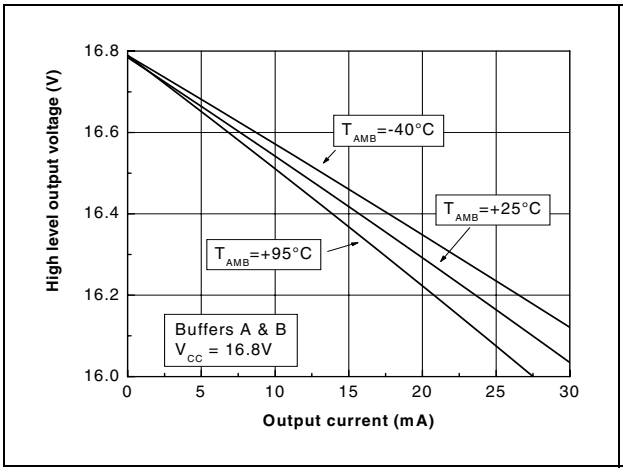


Figure 15. Voltage output low (V_{OL}) vs. output current - buffers C to P

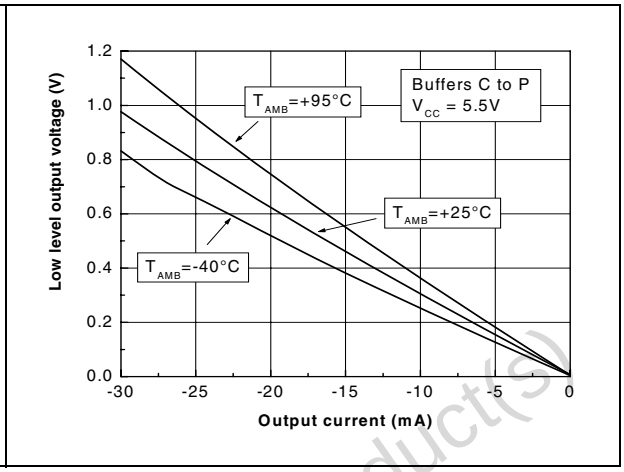


Figure 16. Voltage output low (V_{OL}) vs. output current - buffers C to P

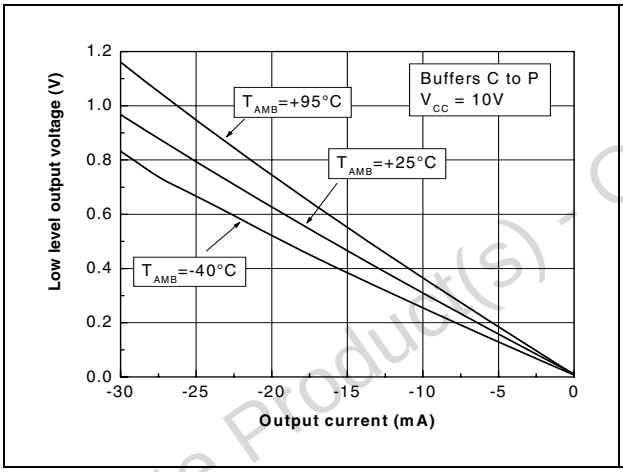


Figure 17. Voltage output low (V_{OL}) vs. output current - buffers C to P

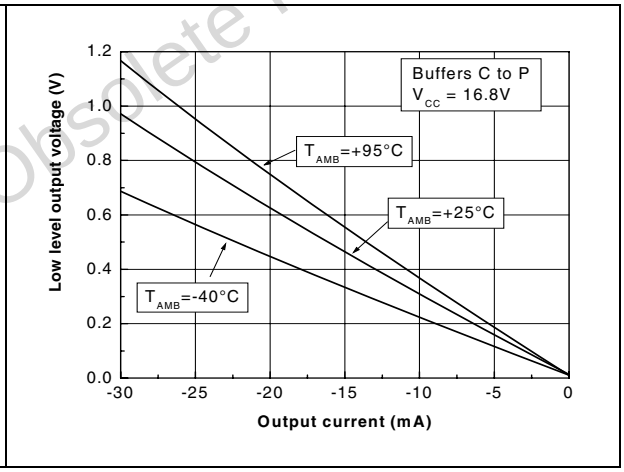


Figure 18. Voltage output low (V_{OL}) vs. output current - buffer Q, R & COM

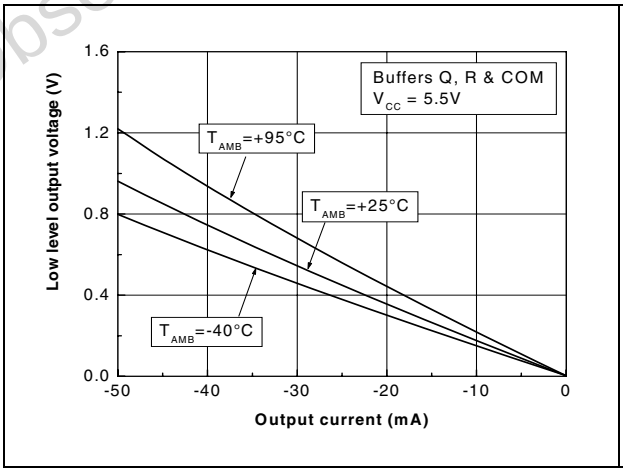


Figure 19. Voltage output low (V_{OL}) vs. output current - buffer Q, R & COM

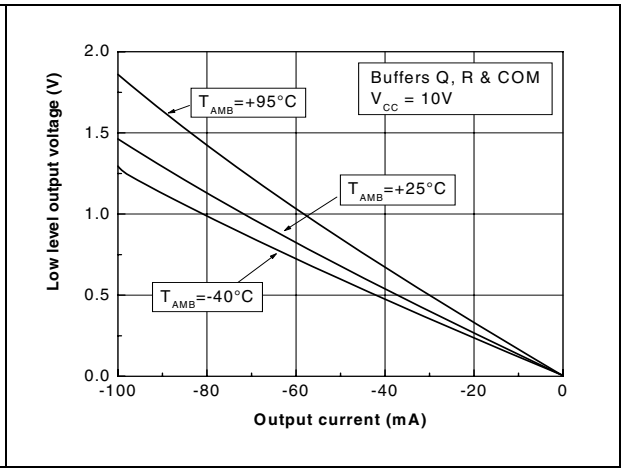


Figure 20. Voltage output low (V_{OL}) vs. output current - buffer Q, R & COM

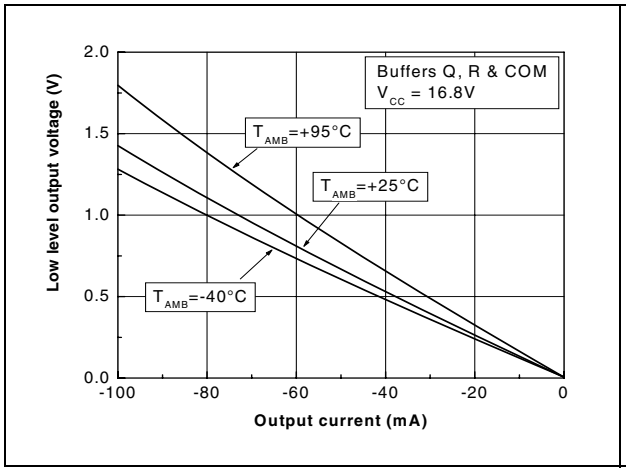


Figure 21. Positive slew rate vs. temperature

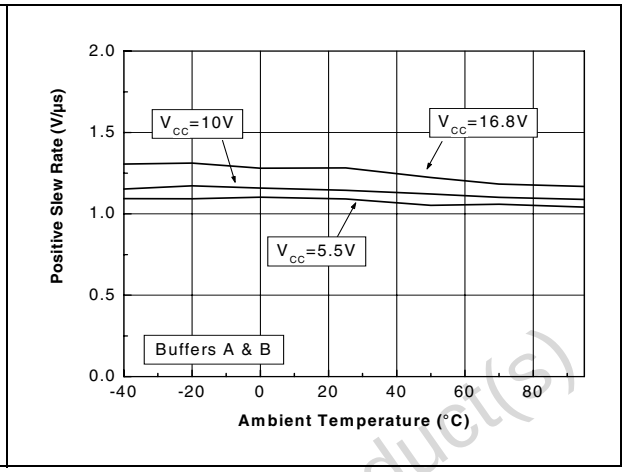


Figure 22. Positive slew rate vs. temperature

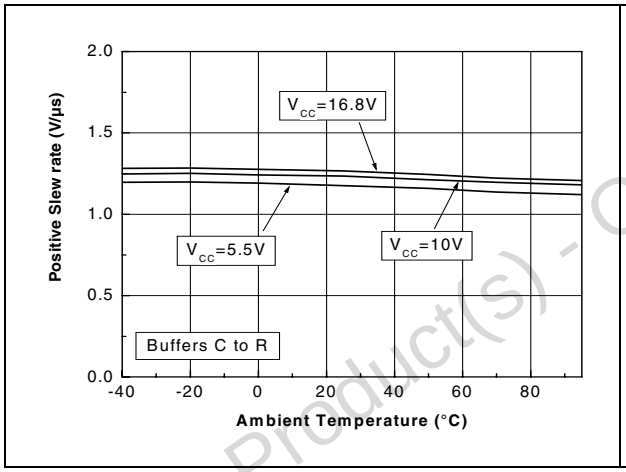


Figure 23. Positive slew rate vs. temperature

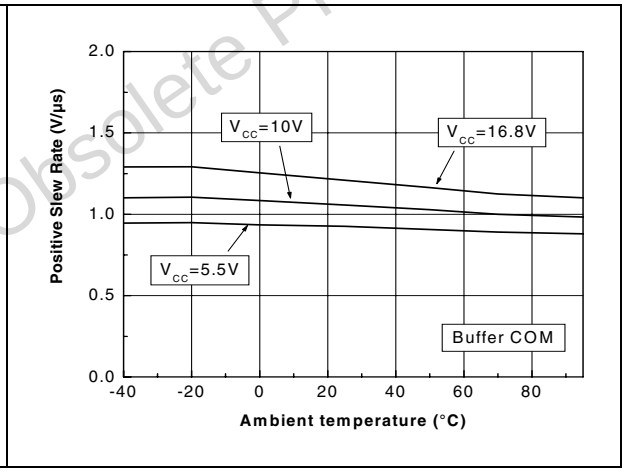


Figure 24. Negative slew rate vs. temperature

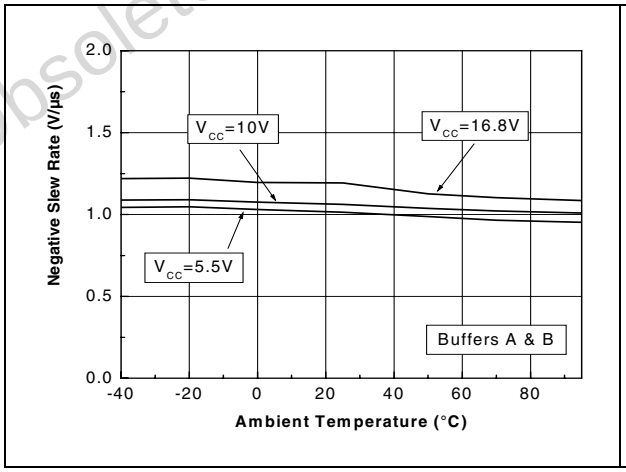


Figure 25. Negative slew rate vs. temperature

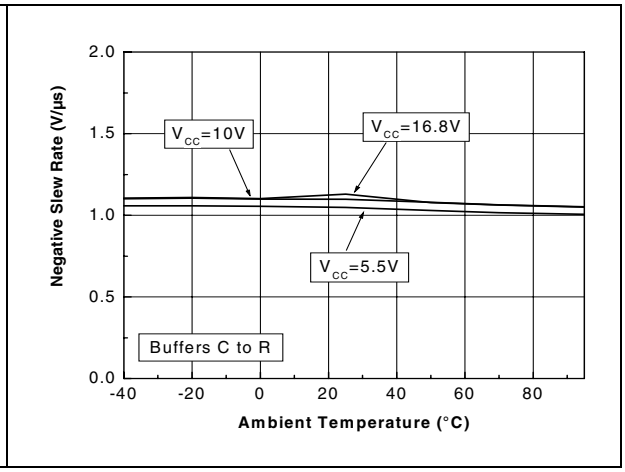


Figure 26. Negative slew rate vs. temperature

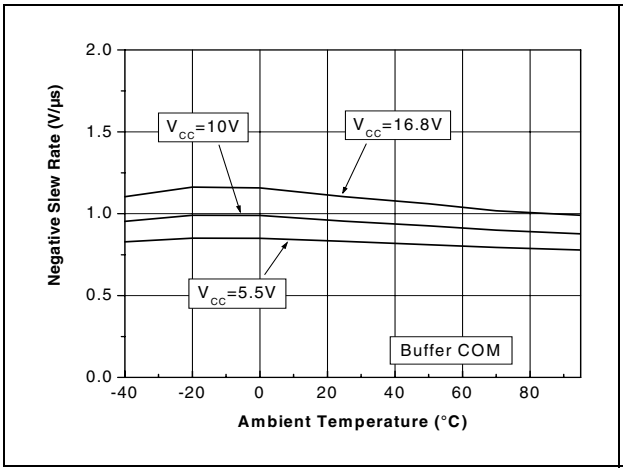


Figure 27. Large signal response - buffers A & B

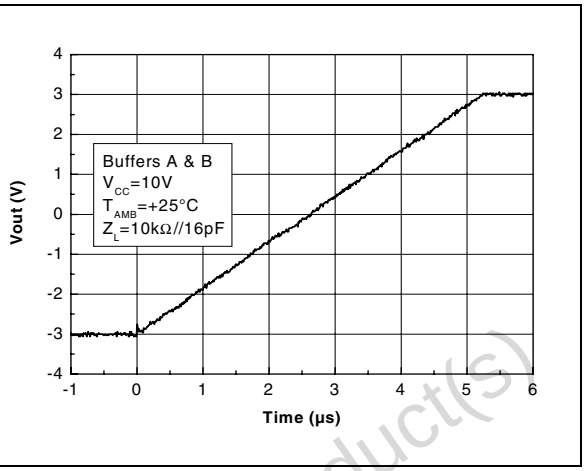


Figure 28. Large signal response - buffers A & B

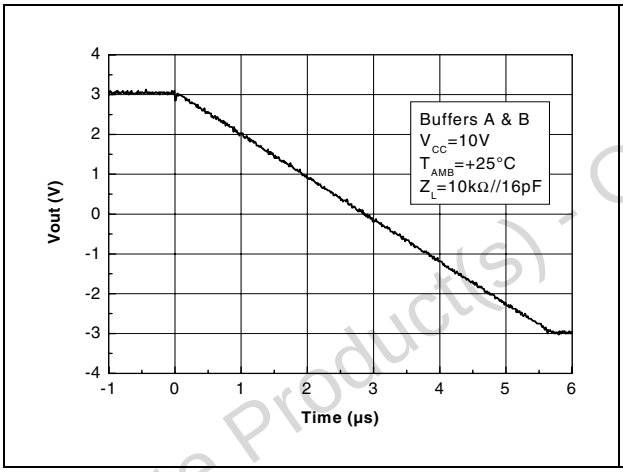


Figure 29. Large signal response - buffers C to R

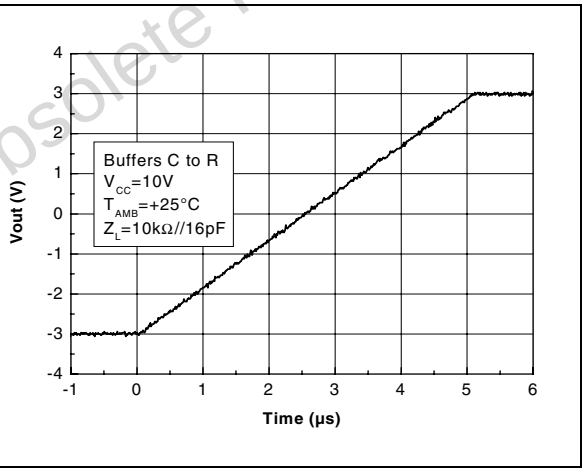


Figure 30. Large signal response - buffers C to R

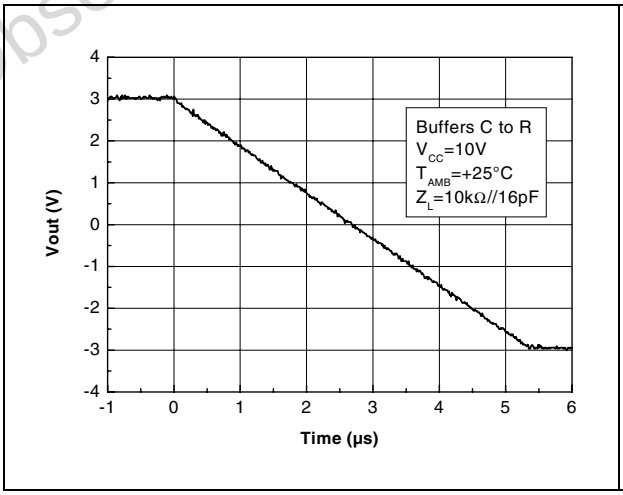


Figure 31. Large signal response - buffer COM

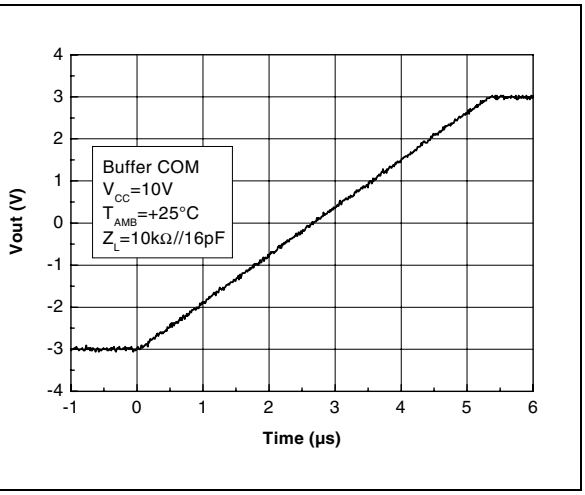


Figure 32. Large signal response - buffer COM

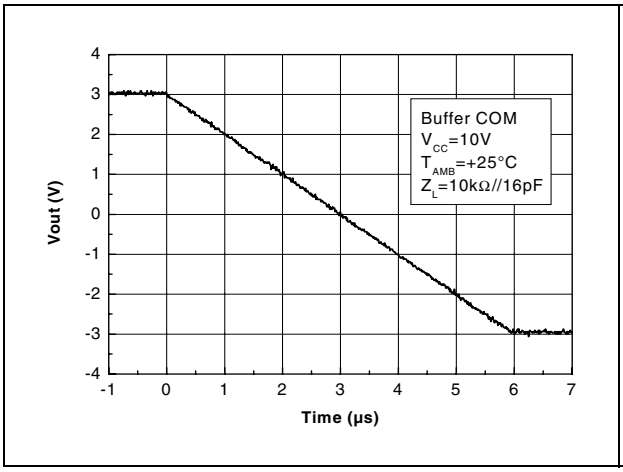


Figure 33. Small signal response - buffers A & B

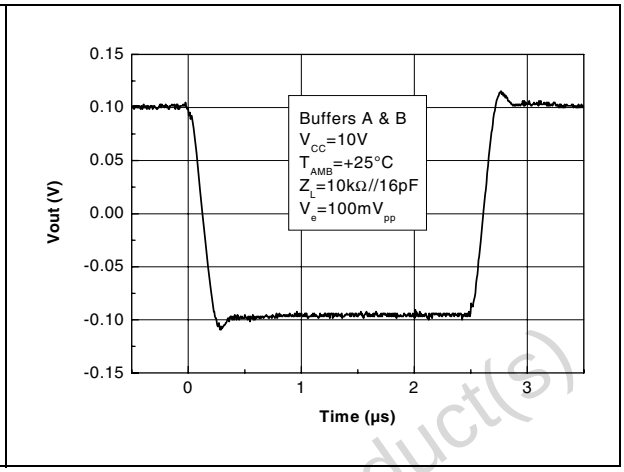


Figure 34. Small signal response - buffers C to R

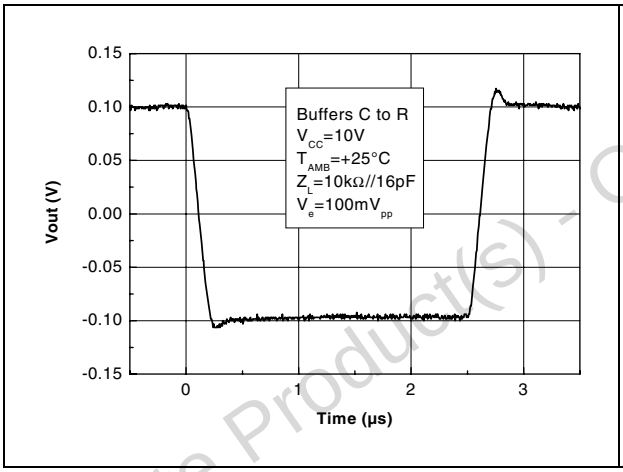


Figure 35. Small signal response - buffer COM

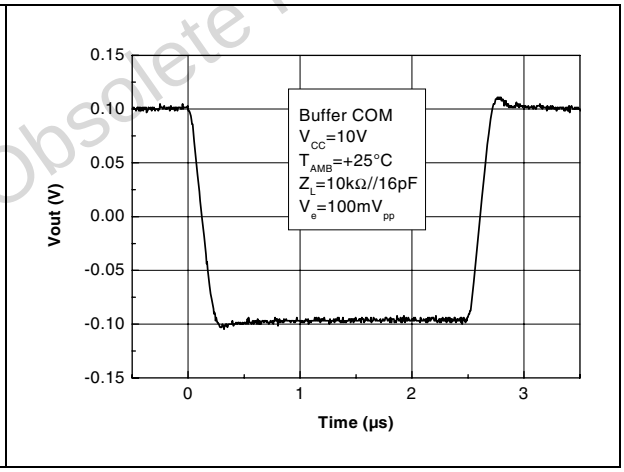


Figure 36. Output voltage response to current transient - buffers A & B

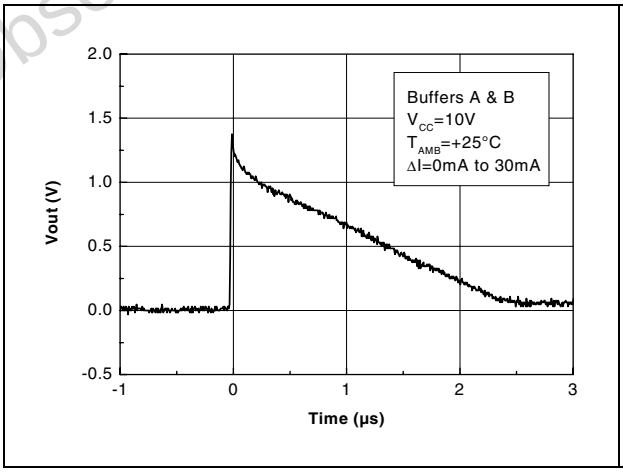


Figure 37. Output voltage response to current transient - buffers A & B

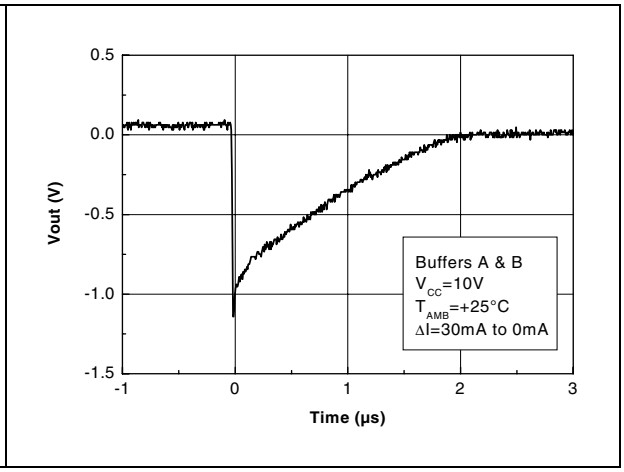


Figure 38. Output voltage response to current transient - buffers C to R

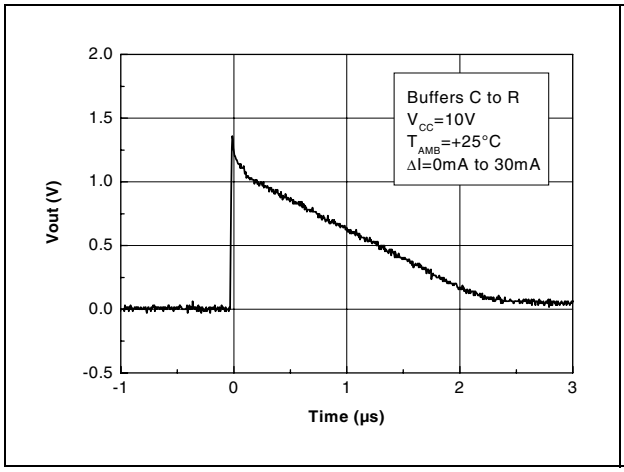


Figure 39. Output voltage response to current transient - buffers C to R

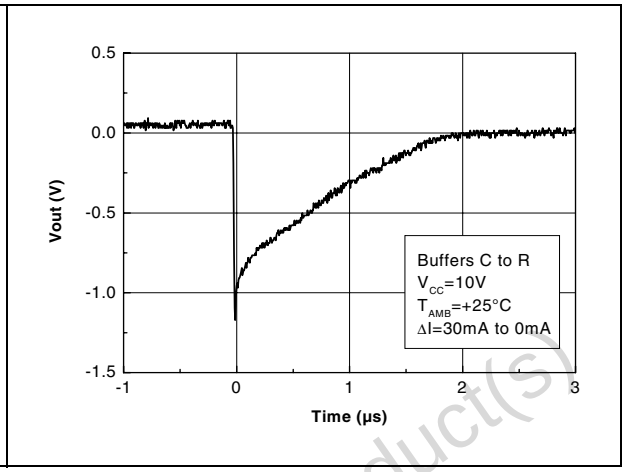


Figure 40. Output voltage response to current transient - buffer COM

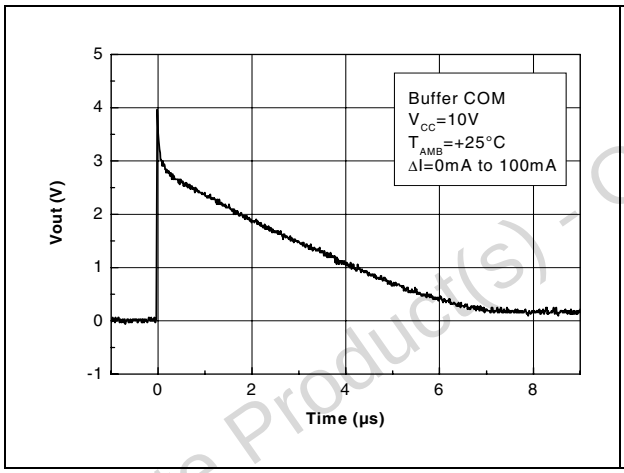


Figure 41. Output voltage response to current transient - buffer COM

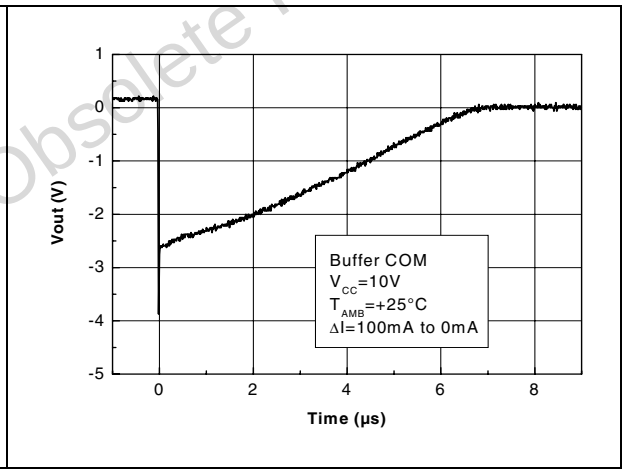


Figure 42. Output voltage response to current transient - buffer COM

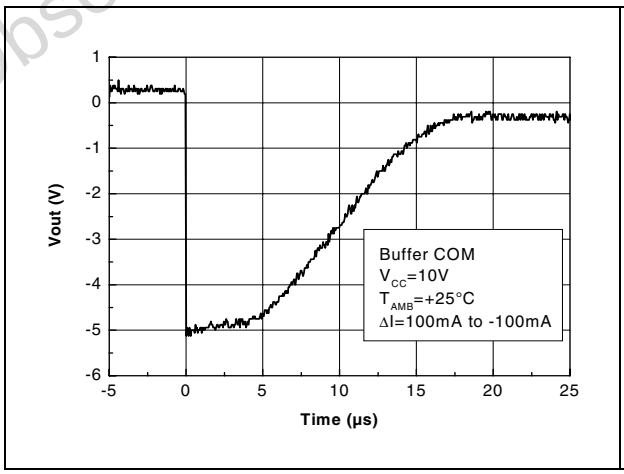
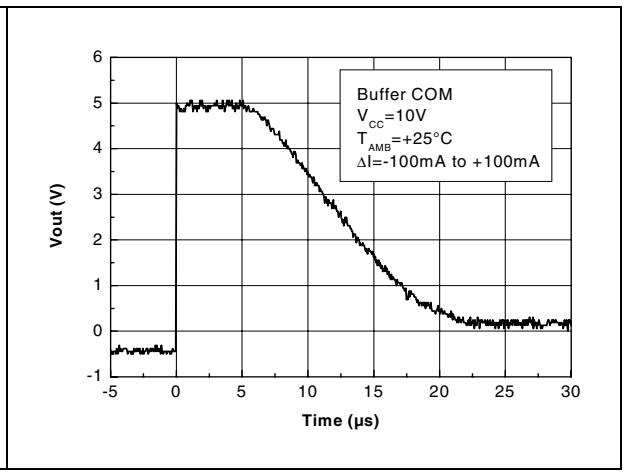


Figure 43. Output voltage response to current transient - buffer COM



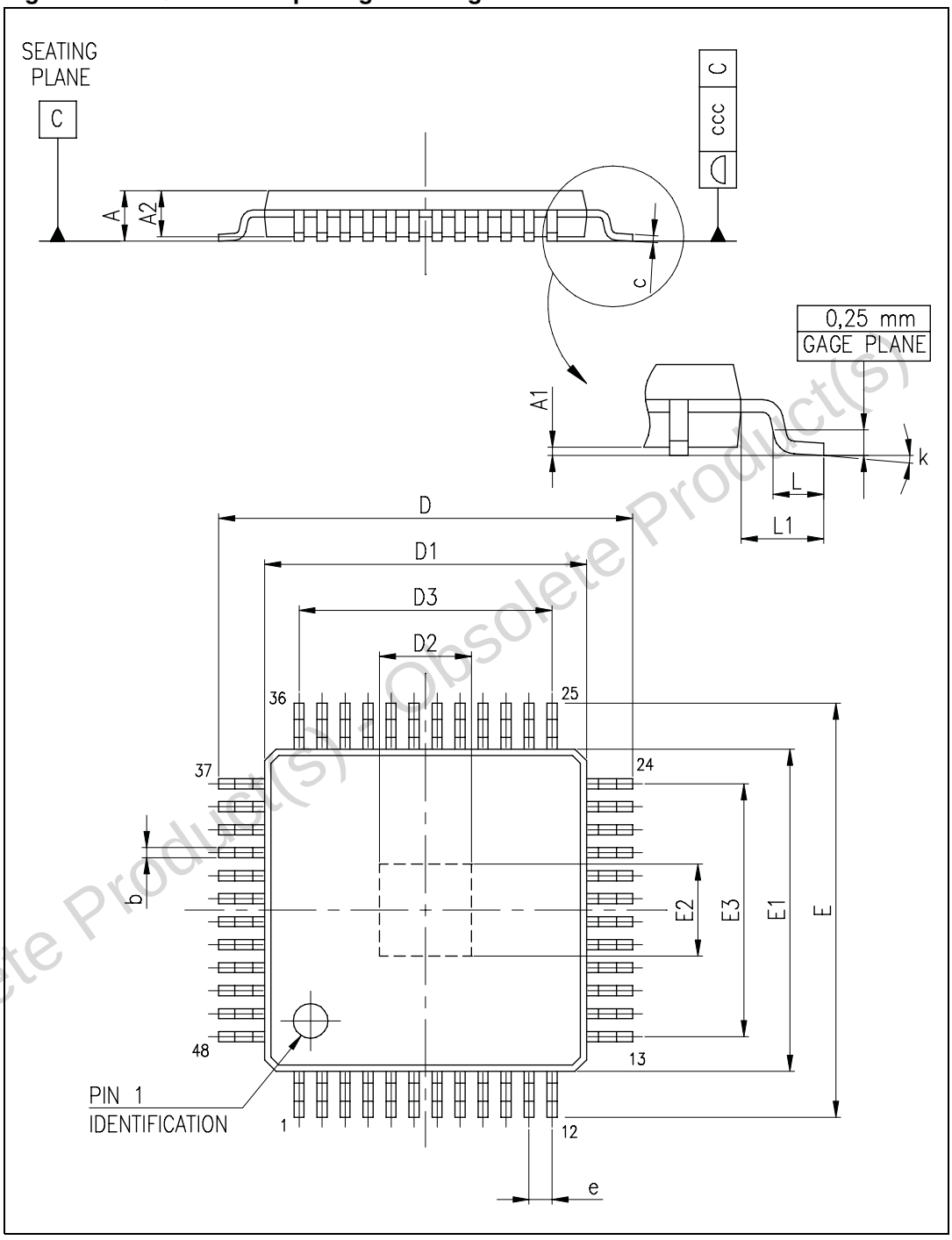
4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Table 4. TQFP48 ePad package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.80	7.00	7.20	0.268	0.276	0.283
D2	2.00			0.079		
D3		5.50			0.217	
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.80	7.00	7.20	0.268	0.276	0.283
E2	2.00			0.079		
E3		5.50			0.217	
e		0.50			0.020	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.08			0.003

Figure 44. TQFP48 ePad package drawing



5 Ordering information

Table 5. Order codes

Part number	Temperature range	Package	Packing	Marking
TSL1018IF	-40°C to +95°C	TQFP48 ePad	Tray	SL1018I
TSL1018IFT			Tape & reel	

6 Revision history

Date	Revision	Changes
22-Mar-2007	1	Initial release.
15-Jul-2008	2	Modified I_{CC} typical and maximum values in *Table 3*. Updated all curves (*Figure 2* to *Figure 43*). Added ESD charged device model value in *Table 1*.

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