200 MHz Laser Diode Driver with Light Power Control

AD9660

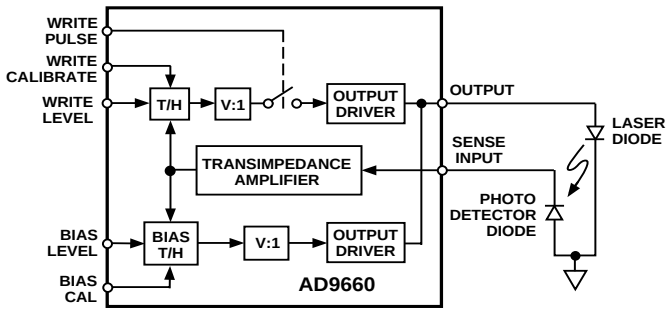
FEATURES

1.5 ns Rise/2.0 ns Fall Times
Output Current: 180 mA @ 3 V, 200 mA @ 2.5 V
Bias Current: 90 mA @ 3 V
Modulation Current: 60 mA @ 3 V
Offset Current: 30 mA @ 3 V
Single +5 V Power Supply
Switching Rate: 200 MHz
Onboard Light Power Control Loops

APPLICATIONS

Laser Printers and Copiers
Optical Disk Drives
FO Datacomm

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9660 is a highly integrated driver for laser diode applications such as optical disk drives, printers, and copiers. The AD9660 gets feedback from an external photo detector and includes two analog feedback loops to allow users to set "bias" and "write" (for optical disk drives) power levels of the laser, and switch between the two power levels at up to 200 MHz. Output rise and fall times are typically 1.5 ns and 2.0 ns to complement printer applications that use image enhancing techniques such as pulse width modulation to achieve gray scale, and allow disk drive applications to improve density and take advantage of pulsed write formats. Control signals are TTL/CMOS compatible.

The driver output provides up to 180 mA of current @ 3 V, 90 mA of BIAS current, 60 mA of modulation current, and 30 mA of offset current. The onboard disable circuit turns off the output drivers and returns the light power control loops to a safe state.

The AD9660 can also be used in closed loop applications in which the output power level follows an analog WRITE LEVEL voltage input. By optimizing the external hold capacitor, and the photo detector, the write loop can achieve bandwidths as high as 25 MHz.

The AD9660 is offered in a 28-pin plastic SOIC for operation over the commercial temperature range (0°C to +70°C).

REV. 0

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AD9660—SPECIFICATIONS ($+V_S$ = +5 V, Temperature = +25°C unless otherwise noted. Sourced currents defined as positive.)

Parameter	Test Level	Temp	AD9660KR Min	Typ	Max	Units	Conditions
ANALOG INPUTS (WRITE LEVEL, BIAS LEVEL)							
Input Voltage Range	IV	Full	V_{REF}		V_{REF} + 1.6	V	
Input Bias Current	I	+25°C	–50		+50	µA	
Analog Bandwidth	V	Full		25		MHz	External Hold Cap = 20 pF
OUTPUTS							
Maximum Output Current, I_{OUT}	I	+25°C	200			mA	V_{OUT} = 2.5 V
I_{OUT}	I	+25°C	180			mA	V_{OUT} = 3.0 V
Bias Current, I_{BIAS}	I	+25°C	90			mA	V_{OUT} = 3.0 V
Modulation Current, $I_{MODULATION}$	I	+25°C	60			mA	V_{OUT} = 3.0 V
Offset Current, I_{OFFSET}	I	+25°C	30			mA	V_{OUT} = 3.0 V
Output Compliance Range	I	+25°C	0		3.0	V	
Idle Current	I	+25°C	3		13	mA	WRITE PULSE = LOW, DISABLE = HIGH
SWITCHING PERFORMANCE							
Maximum Pulse Rate	IV	+25°C	200	250		MHz	3 dB Reduction in I_{OUT}
Output Propagation Delay (t_{PD}), Rising[1]	IV	Full	1.6		3.0	ns	
Output Propagation Delay (t_{PD}), Falling[1]	IV	Full	1.6		2.5	ns	
Output Current Rise Time[2]	IV	Full	1.1	1.5	1.7	ns	
Output Current Fall Time[3]	IV	Full	1.4	2.0	2.8	ns	
WRITE CAL Aperture Delay[4]	V	+25°C		13		ns	
Disable Time[5]	V	+25°C		5		ns	
HOLD NODES (WRITE HOLD, BIAS HOLD)							
Input Bias Current	I	+25°C	–200		200	nA	V_{HOLD} = 2.5 V
Input Voltage Range	IV	Full	V_{REF}		V_{REF} + 1.6	V	Open Loop Application Only
Minimum External Hold Cap	V	Full		20		pF	
TTL INPUTS[6]							
Logic "1" Voltage	I	+25°C	2.0			V	DISABLE = LOW
Logic "1" Voltage	IV	Full	2.0			V	While Other
Logic "0" Voltage	I	+25°C			0.8	V	TTL Inputs Are
Logic "0" Voltage	IV	Full			0.8	V	Tested
Logic "1" Current	I	+25°C	–10	20	10	µA	
Logic "0" Current	I	+25°C	–1.5			mA	
BANDGAP REFERENCE							
Output Voltage V_{REF}	I	+25°C	1.55	1.75	1.90	V	
Temperature Coefficient	V			–0.2		mV/°C	
Output Current	V	+25°C	–0.5		1.0	mA	
SENSE IN							
Current Gain	V	+25°C		1.85		mA/mA	
Voltage	I	+25°C	3.7	4.0	4.3	V	$I_{MONITOR}$ = 2 mA
Input Resistance	V	+25°C		<150		Ω	
POWER SUPPLY (DISABLE = HIGH)							
$+V_S$ Voltage	I	+25°C	4.75	5.00	5.25	V	DISABLE = HIGH
$+V_S$ Current	I	+25°C	75	110	150	mA	
Power Dissipation	I	+25°C		550		mW	
OFFSET CURRENT							
OFFSET SET Voltage	I	+25°C	1.1	1.4	1.7	V	$I_{MONITOR}$ = 4.0 mA

NOTES

[1]Propagation delay measured from the 50% of the rising/falling transition of WRITE PULSE to 50% point of the rising/falling edge of the output modulation current.

[2]Rise time measured between the 10% and 90% points of the rising transition of the modulation current.

[3]Fall time measured between the 10% and 90% points of the falling transition of the modulation current.

[4]Aperture Delay is measured from the 50% point of the rising edge of WRITE PULSE to the time when the output modulation begins to recalibrate, WRITE CAL is held during this test.

[5]Disable Time is measured from the 50% point of the rising edge of DISABLE to the 50% point of the falling transition of the output current. Fall time during disable is similar to fall time during normal operation.

[6]WRITE PULSE, WRITE CAL, BIAS CAL, OFFSET PULSE are TTL compatible inputs.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ ..... +6 V
V_{REF} Current ..... 2 mA
WRITE LEVEL, BIAS LEVEL ..... –0.5 V to $+V_S$
TTL INPUTS ..... –0.5 V to $+V_S$
Output Current ..... 300 mA
Operating Temperature
AD9660KR ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature[2] ..... +150°C
Lead Soldering Temp (10 sec) ..... +300°C

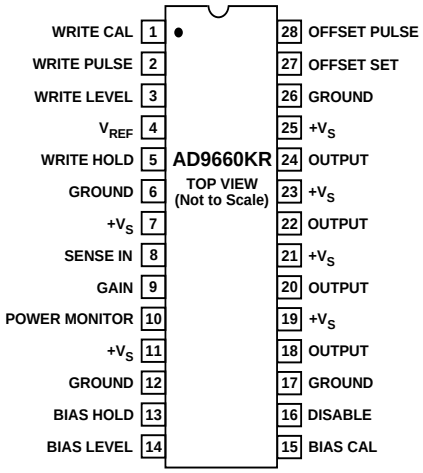
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]Typical thermal impedance is θ_{JA} = 45°C/W, θ_{JC} = 41°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9660KR	0°C to +70°C	R-28
AD9660KR-REEL	0°C to +70°C	R-28 (1000/reel)

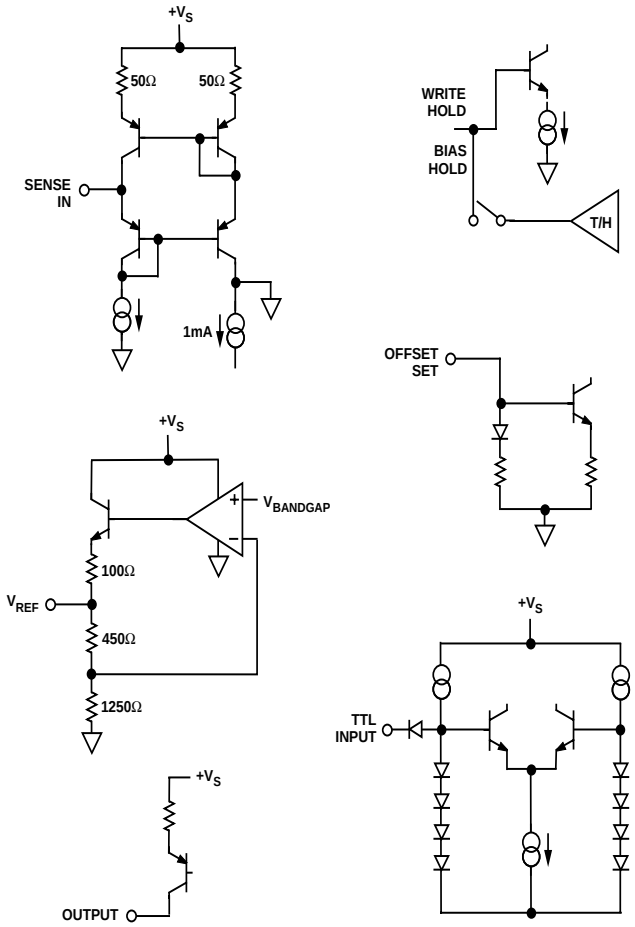
PIN ASSIGNMENTS



EXPLANATION OF TEST LEVELS

Test Level

I. 100% Production Tested.
II. 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III. Sample Tested Only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.
VI. All devices are 100% production tested at +25°C, sample tested at temperature extremes.



Equivalent Circuits

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9660 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTIONS

Pin	Function
OUTPUT	Analog laser diode current output. Connect to anode of laser diode, cathode connected to GROUND externally.
BIAS LEVEL	Analog voltage input, V_{REF} to V_{REF} + 1.6 V. Bias current is set proportional to the BIAS LEVEL during calibration as follows: $I_{MONITOR} = \frac{V_{BIAS\ LEVEL} - V_{REF}}{1.85 \times (R_{GAIN} + 50\ \Omega)}$
BIAS CAL	TTL/CMOS compatible, Bias loop T/H control signal. Logic HIGH enables calibration mode, and the bias loop T/H immediately goes into track mode. Logic LOW disables the bias loop T/H and immediately places it in hold mode. WRITE PULSE should be held logic LOW while calibrating. Floats logic HIGH.
BIAS HOLD	External hold capacitor for the bias loop T/H. Approximate droop in the bias current while BIAS CAL is logic LOW is: $\pm\Delta I_{BIAS} = \frac{18 \times 10^{-9}\ t_{BIAS\ HOLD}}{C_{BIAS\ HOLD}}$. Bandwidth of the loop is: $\mathrm{BW} = \frac{1}{2\pi\,(550\ \Omega)\,C_{\mathrm{BIAS\,HOLD}}}$
WRITE PULSE	TTL/CMOS compatible, current control signal. Logic HIGH supplies $I_{MODULATION}$ to the laser diode. Logic LOW turns $I_{MODULATION}$ off. Floats logic HIGH.
WRITE CAL	TTL/CMOS compatible, write loop T/H control signal. Logic HIGH enables calibration mode; before enabling calibration the bias loop should be calibrated and OFFSET PULSE driven to an appropriate state. In calibration mode, 13 ns after the WRITE PULSE goes logic HIGH, the write loop T/H goes into track mode (there is no delay if WRITE PULSE is HIGH before WRITE CAL transitions to a HIGH level). The write loop T/H immediately goes into hold mode when the WRITE PULSE goes Logic LOW. WRITE CAL LOW disables the write loop T/H and places it in hold mode. Floats logic HIGH.
WRITE LEVEL	Analog voltage input, V_{REF} to V_{REF} +1.6 V. Write current is set proportional to the input voltage during calibration as follows: $I_{MONITOR} = \frac{V_{WRITE\ LEVEL} - V_{REF}}{1.85 \times (R_{GAIN} + 50\ \Omega)}$
WRITE HOLD	External hold capacitor for the write loop T/H. Approximate droop in $I_{MODULATION}$ current while WRITE CAL is logic LOW is: $\pm\Delta I_{MODULATED} = \frac{18 \times 10^{-9} t_{WRITE\ HOLD}}{C_{WRITE\ HOLD}}$. Bandwidth of the loop is: $BW = \frac{1}{2\pi\,(550\ \Omega)\,C_{BIAS\ HOLD}}$
SENSE IN	Analog current input, $I_{MONITOR}$, from PIN photo detector diode. SENSE IN should be connected to the cathode of the PIN diode, with the PIN anode connected to GROUND or a negative voltage. Voltage at SENSE IN varies slightly with temperature and current, but is typically 4.0 V.
GAIN	External connection for the feedback network of the transimpedance amplifier. External feedback network, R_{GAIN} and C_{GAIN}, should be connected between GAIN and POWER MONITOR. See text for choosing values.
POWER MONITOR	Output voltage monitor of the internal feedback loop. Voltage is proportional to feedback current from photo diode.
OFFSET CURRENT SET	Set resistor connection for the offset current source. Resistor between OFFSET CURRENT SET and $+V_S$ determines offset current level. The input voltage at this node varies slightly with temperature and current, but is typically 1.4 V. See curves. Can also be driven with a current out DAC.
OFFSET PULSE	TTL/CMOS compatible, OFFSET current control signal. Logic HIGH adds I_{OFFSET} to I_{OUT}. Logic LOW turns off I_{OFFSET}. Floats logic HIGH.
DISABLE	TTL/CMOS compatible, current output disable circuit. Logic LOW for normal operation; logic HIGH disables the current outputs to the laser diode, and drives the voltage on the hold capacitors close to V_{REF} (minimizes the output current when the device is re-enabled). DISABLE floats logic HIGH.
V_{REF}	Analog Voltage Output, internal bandgap voltage reference, ~1.75 V, provided to user for power level offset.
$+V_S$	Positive Power Supply. Nominally +5 V, pin connections should be tied together externally.
GROUND	Ground Reference. All grounds should be tied together externally.

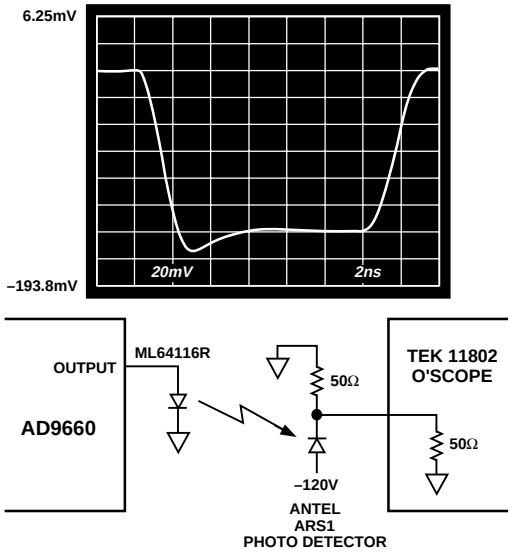


Figure 1. Driving ML64116R Laser @ 30 mW

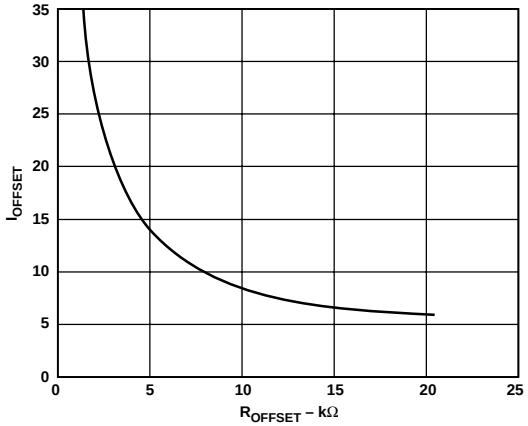


Figure 2. I_{OFFSET} vs. R_{OFFSET}

THEORY OF OPERATION

The AD9660 combines a very fast output current switch with onboard analog light power control loops to provide the user with a complete laser diode driver solution. The block diagram illustrates the key internal functions. The control loops of the AD9660, the bias loop and the write loop, adjust the output current level, I_{OUT}, so that the photo diode feedback current, $I_{MONITOR}$, out of SENSE IN is proportional to the analog input voltage at BIAS LEVEL or WRITE LEVEL. Since the monitor current is proportional to the laser diode light power, the loops effectively control laser power to a level proportional to the analog inputs. The control loops should be periodically calibrated independently (see Choosing $C_{BIAS\ HOLD}$ and $C_{WRITE\ HOLD}$).

The offset current generator produces an open loop output current, I_{OFFSET}. Its level is controlled by an external set resistor or a current out DAC (see Figure 2). While I_{OFFSET} is not calibrated as the currents from the bias and write loops are, it can be very versatile (see Offset Current below).

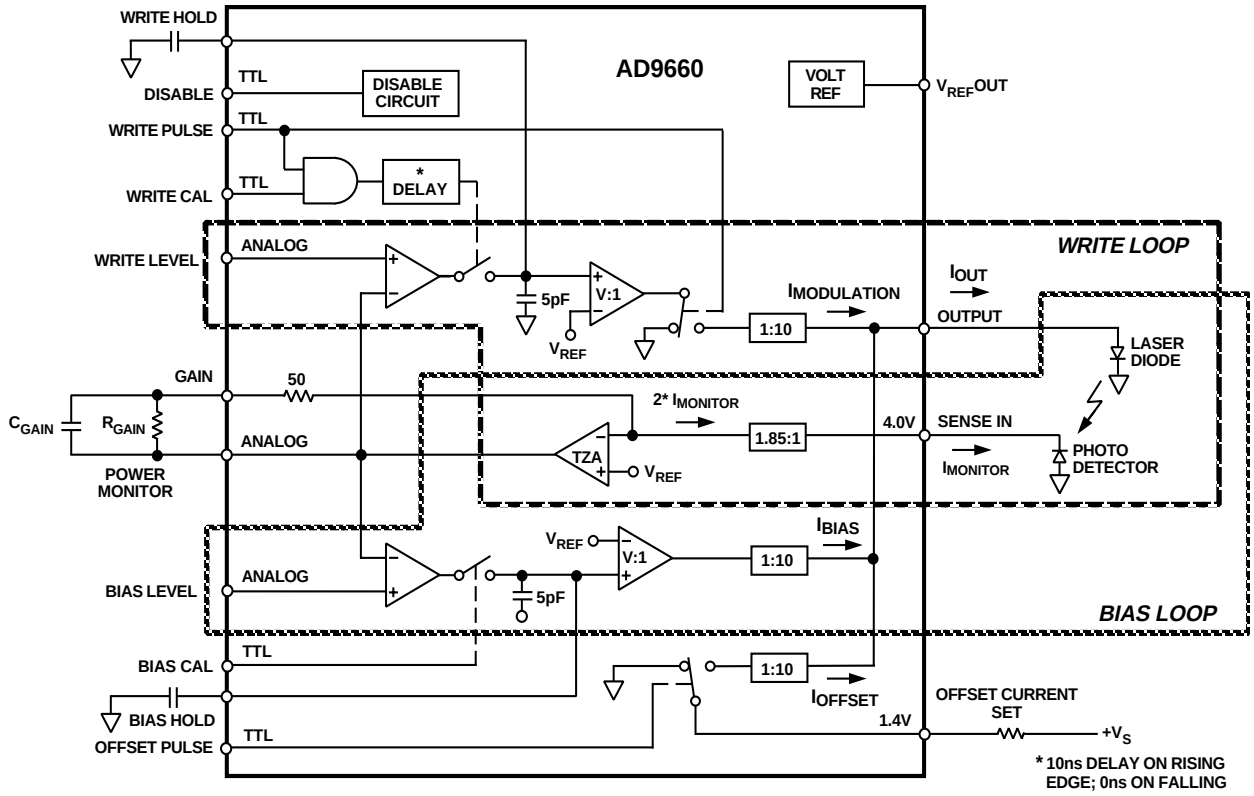


Figure 3. Functional Block Diagram

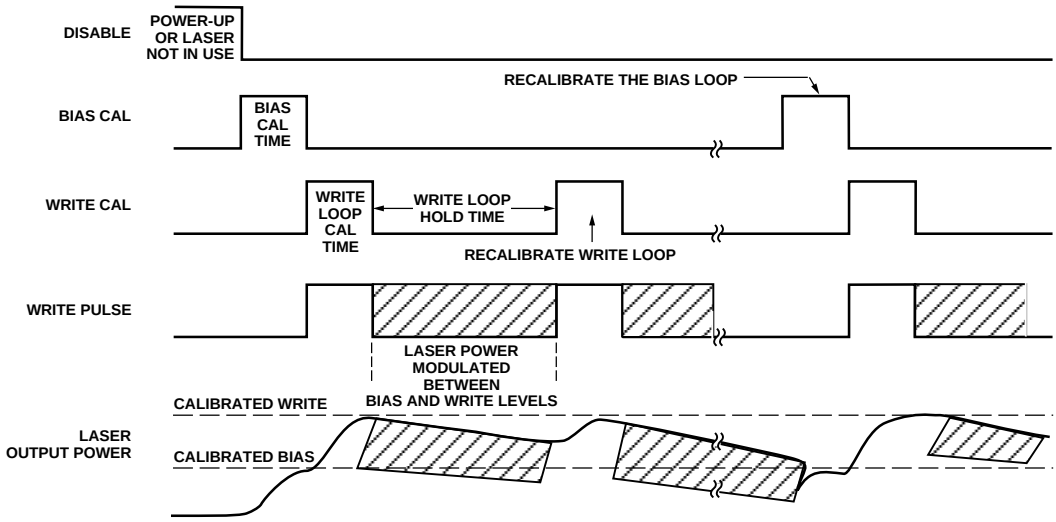


Figure 4. Normal Operating Mode

The disable circuit turns off I_{OUT} and returns the hold capacitor voltages to their minimum levels (minimum output current) when DISABLE = logic HIGH. It is used during initial power-up of the AD9660 or during time periods when the laser is inactive. When the AD9660 is re-enabled the control loops must be recalibrated.

Normal operation of the AD9660 involves (in order, see figure):

1. The AD9660 is enabled (DISABLE = logic LOW).
2. The input voltages (BIAS LEVEL and WRITE LEVEL) are driven to the appropriate levels to set the calibrated laser diode output power levels.
3. The bias loop is closed for calibration (BIAS CAL = logic HIGH), and then opened (BIAS CAL = logic LOW).
4. The write loop is closed for calibration (WRITE PULSE and WRITE CAL = logic HIGH) and then opened.
5. While both loops are open, the laser is pulsed between the two calibrated levels by WRITE PULSE.
6. The bias and write loops are periodically recalibrated as needed.
7. The AD9660 is disabled when the laser will not be pulsed for an indefinite period of time.

Control Loop Transfer Functions

The relationship between $I_{MONITOR}$ and $V_{BIAS\ LEVEL}$ is

$$I_{MONITOR} = \frac{V_{BIAS\ LEVEL} - V_{REF}}{1.85 \times (R_{GAIN} + 50\ \Omega)}$$

once the bias loop is calibrated. When the bias loop is open (BIAS CAL = logic LOW), its output current, I_{BIAS}, is proportional to the held voltage at BIAS HOLD; the external hold capacitor on this pin determines the droop error in the output bias current between calibrations.

The relationship between $I_{MONITOR}$ and $V_{WRITE\ LEVEL}$ is

$$I_{MONITOR} = \frac{V_{WRITE\ LEVEL} - V_{REF}}{1.85 \times (R_{GAIN} + 50\ \Omega)}$$

once the write loop is calibrated. The current supplied by the write loop output is referred to as the modulation current, $I_{MODULATION}$.

When the write loop is open (WRITE CAL logic LOW), $I_{MODULATION}$ is proportional to the held voltage at WRITE HOLD. The external hold capacitor (WRITE HOLD) determines the droop error between calibrations. $I_{MODULATION}$ may be switched on and off by WRITE PULSE when the write loop is open.

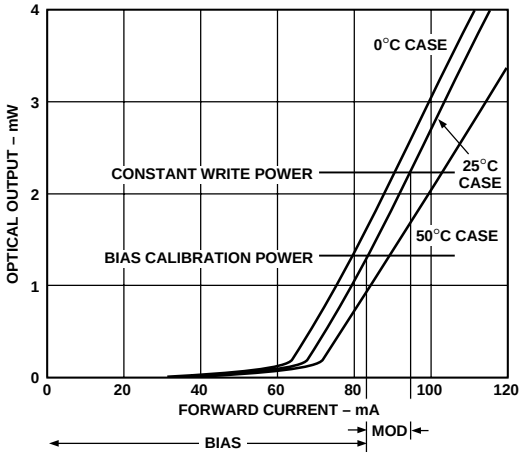


Figure 5. Typical Laser Diode Current-to-Optical Power Curve

The sections below discuss choosing the external components in the feedback loops for a particular application.

Choosing R_{GAIN}

The gain resistor, R_{GAIN}, allows the user to match the feedback loop's transfer function to the laser diode/photo diode combination.

The user should define the maximum laser diode output power for the intended application, $P_{LD\ MAX}$, and the corresponding photo diode monitor current, $I_{MONITOR\ MAX}$. A typical laser diode transfer function is illustrated in Figure 5. R_{GAIN} should be chosen as: $R_{GAIN} = \frac{1.6\ V}{1.85 \times I_{MONITOR\ MAX}} - 50\ \Omega$.

The laser diode's output power will then vary from 0 to $P_{LD\ MAX}$ for an input range of V_{REF} to V_{REF} +1.6 V @ the BIAS LEVEL and WRITE LEVEL inputs.

Minimum specifications for $I_{MONITOR\ MAX}$ should be used when choosing R_{GAIN}. Users are cautioned that laser diode/photo diode combinations that produce monitor currents that are less than $I_{MONITOR\ MAX}$ in the equation above will produce higher laser output power than predicted, which may damage the laser diode. Such a condition is possible if R_{GAIN} is calculated using typical instead of minimum monitor current specifications. In that case the input range to the AD9660 BIAS LEVEL and WRITE LEVEL inputs should be limited to avoid damaging laser diodes.

Although not recommended, another approach would be to use a potentiometer for R_{GAIN}. This allows users to optimize the value of R_{GAIN} for each laser diode/photo diode combination's monitor current. The drawback to this approach is that potentiometer's stray inductance and capacitance may cause the transimpedance amplifier to overshoot and degrade its settling, and the value of C_{GAIN} may not be optimized for the entire potentiometer's range.

C_{GAIN} optimizes the response of the transimpedance amplifier and should be chosen as from the table below. Choosing C_{GAIN} larger than the recommended value will slow the response of the amplifier. Lower values improve TZA bandwidth but may cause the amplifier to oscillate.

Table I.

R_{GAIN}	Recommended C_{GAIN}
≥2.5 kΩ	2 pF
1.5 kΩ	3 pF
1 kΩ	4 pF
500 Ω	8 pF

The circuit in Figure 6 allows an adjustable gain with low variance in bandwidth, but requires several external components.

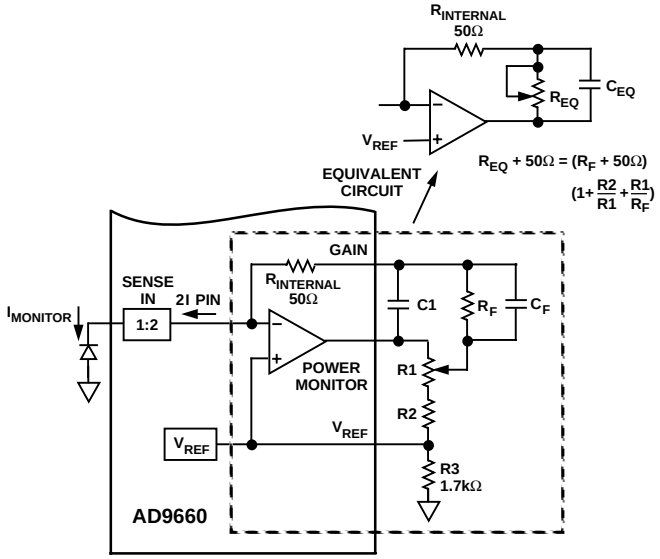


Figure 6. Adjustable Gain Configuration

Choosing $C_{BIAS\ HOLD}$ and $C_{WRITE\ HOLD}$

Choosing values for the hold capacitors, C_{WRITE} and C_{HOLD}, is a tradeoff between output current droop when the control loops are open, and the time it takes to calibrate and recalibrate the laser power when the loops are closed.

The amount of output current droop is determined by the value of the hold capacitor and the leakage current at that node. When either of the two control loops are open (WRITE CAL or BIAS CAL logic LOW), the pin connections for the hold capacitors (WRITE HOLD and BIAS HOLD) are high impedance inputs. Leakage currents will range from ±200 nA; this low current minimizes the droop in the output power level. Assuming the worst case current of ±200 nA, the output current will change as follows:

$$\pm\Delta I_{BIAS} = \frac{18\times10^{-9}\ t_{BIAS\ HOLD}}{C_{BIAS\ HOLD}}$$

$$\pm\Delta I_{MODULATED} = \frac{18\times10^{-9}\ t_{WRITE\ HOLD}}{C_{WRITE\ HOLD}}$$

To choose a value, the user will need to determine the amount of time the loop will be in hold mode, $t_{WRITE\ HOLD}$ or $t_{BIAS\ HOLD}$, the maximum change in laser output power the application can tolerate, and the laser efficiency (defined as the change in laser output power to the change in laser diode current). As an example, if an application requires 5 mW of laser power ±5%, and the laser diode efficiency is 0.25 mW/mA, then

$$\Delta I_{MAX} = 5\ mW\times(5\%)/\left(0.25\frac{mW}{mA}\right) = 1.0\ mA$$

If the same application had a hold time requirement of 250 µs, then the minimum value of the hold capacitor would be:

$$C_{HOLD} = \frac{18\times10^{-9}\times250\ \mu s}{1.0\ mA} = 4.5\ nF$$

When determining the calibration time, the T/H and the external hold capacitor can be modeled using the simple RC circuit illustrated in Figure 7.

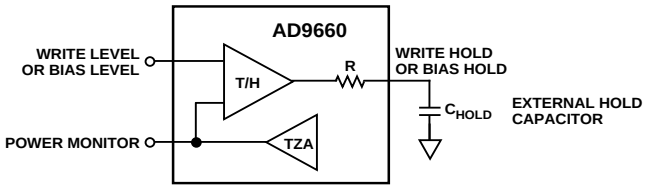


Figure 7. Circuit Model for Determining Calibration Times

Using this model, the voltage at the hold capacitor is

$$V_{C_{HOLD}} = V_{t=0} + (V_{t=\infty} - V_{t=0})\left(1 - e^{\frac{-t}{\tau}}\right)$$

where t_0 is when the calibration begins (WRITE CAL or BIAS CAL goes logic HIGH), $V_{t=0}$ is the voltage on the hold cap at $t = 0$, $V_{t=\infty}$ is the steady state voltage at the hold cap with the loop closed, and $\tau = R_{C_{HOLD}}$ is the time constant. With this model the error in $V_{C_{HOLD}}$ for a finite calibration time, as compared to $V_{t=\infty}$, can be estimated from the following table and chart:

Table II.

$t_{CALIBRATION}$	% Final Value	Error %
7τ	99.9	0.09
6τ	99.7	0.25
5τ	99.2	0.79
4τ	98.1	1.83
3τ	95.0	4.97
2τ	86.5	13.5
τ	63.2	36.8

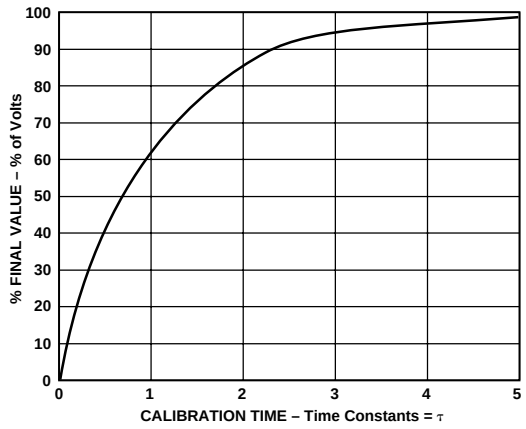


Figure 8. Calibration Time Curve

Initial calibration is required after power-up or any other time the laser has been disabled. Disabling the AD9660 drives the hold capacitors back down to V_{REF}. In this case, or in any case where the output current is more than 10% out of calibration, R will range from 300 Ω to 550 Ω for the model above; the higher value should be used for calculating the worst case calibration time. Following the example above, if C_{HOLD} were chosen as 4.5 nF, then $\tau = RC = 550\ \Omega \times 4.5$ nF would be 2.5 µs. For an initial calibration error <1%, the initial calibration time should be $>5\tau = 12.4$ µs.

Initial calibration time will actually be better than this calculation indicates, as a significant portion of the calibration time will be within 10% of the final value, and the output resistance in the AD9660's T/H decreases as the hold voltage approaches its final value.

Recalibration is functionally identical to initial calibration, but the loop need only correct for droop. Because droop is assumed to be a small percentage of the initial calibration (<10%), the resistance for the model above will be in the range of 75 Ω to 140 Ω. Again, the higher value should be used to estimate the worst case time needed for recalibration.

Continuing with the example above, since the error during hold time was chosen as 5%, we meet the criteria for recalibration and $\tau = RC = 140\ \Omega \times 4.5$ nF = 0.63 µs. To get a final error of 1% after recalibration, the 5% droop must be corrected to within a 20% error (20% × 5% = 1%). A 2τ recalibration time of 1.26 µs is sufficient.

Continuous Recalibration

In applications where the hold capacitor is small (<500 pF) and the WRITE PULSE signals always have a pulse width >25 ns, the user may continuously calibrate the write loop. In such an application, the WRITE CAL signal should be held logic HIGH, and the WRITE PULSE signal will control write loop calibration via the internal AND gate.

The bias loop may be continuously recalibrated whenever WRITE PULSE is logic LOW.

Example Calculations

The example below (in addition to the one included in the sections above) should guide users in choosing R_{GAIN}, C_{GAIN}, the hold capacitor values, and worst case calibration times.

System Requirements:

- Bias laser power: 4 mW Bias ± 5%
- Write laser power: 25 mW ± 0.5%
- Bias Hold Time: 1 ms
- Write Hold Time: 1 μs

Laser diode/photo diode characteristics:

- Laser efficiency 0.5 mA/mA
- Monitor current: 5 μA/mA
- From the laser power requirements and efficiency we can estimate:

$$\Delta I_{BIAS\ MAX} = 4\ mW \times (5\%) / \left(0.5 \frac{mW}{mA}\right) = 400.0\ \mu A$$

and

$$\Delta I_{WRITE\ MAX} = 25\ mW \times \left(0.5\%\right) / \left(0.5 \frac{mW}{mA}\right) = 250\ \mu A$$

- Choosing hold caps based on these:

$$C_{BIAS\ HOLD} = \frac{18 \times 10^{-9} \times 1\ ms}{400\ \mu A} = 0.045\ \mu F$$

and

$$C_{WRITE\ HOLD} = \frac{18 \times 10^{-9} \times 1\ \mu s}{250\ \mu A} = 72\ pF$$

- The bias loop initial calibration time for a <1% error:
  $5\tau = 5 \times RC = 5 \times 550\ \Omega \times 0.045\ \mu F = 123.75\ \mu s$
- Bias loop recalibration for a 1% error after 5% droop (need to correct within 20%):
  $2\tau = 2 \times RC = 2 \times 140\ \Omega \times 0.045\ \mu F = 12.6\ \mu s$
- The write loop initial calibration time for <0.1% error:
  $7\tau = 7 \times RC = 7 \times 550\ \Omega \times 72\ pF = 277.2\ ns$
- Write loop re-calibration for a 0.1% error after 0.5% droop (need to correct within 20%):
  $2\tau = RC = 2 \times 140\ \Omega \times 72\ pF = 20.2\ ns$
- From the monitor current specification and the max power specified:

$$I_{MONITOR\ MAX} = 25\ mW \frac{5\ \mu A}{mW} = 125\ \mu A$$

and

$$R_{GAIN} = \frac{1.6\ V}{1.85 \times I_{MONITOR\ MAX}} - 50\ \Omega = 6.9\ k\Omega$$

- C_{GAIN} would be chosen as 2 pF (see Table I).

Driving the Analog Inputs

The BIAS LEVEL and WRITE LEVEL inputs of the AD9660 drive the track and hold amplifiers and allow the user to adjust the amount of output current as described above. The input voltage range on both inputs is V_{REF} to V_{REF} + 1.6 V, requiring the user to create an offset of V_{REF} for a ground based signal. The circuit in Figure 9 will perform the level shift and scale the output of a DAC whose output is from ground to a positive voltage. This solution is attractive because both the DAC and the op amp can run off a single +5 V supply, and the op amp doesn't have to swing rail to rail.

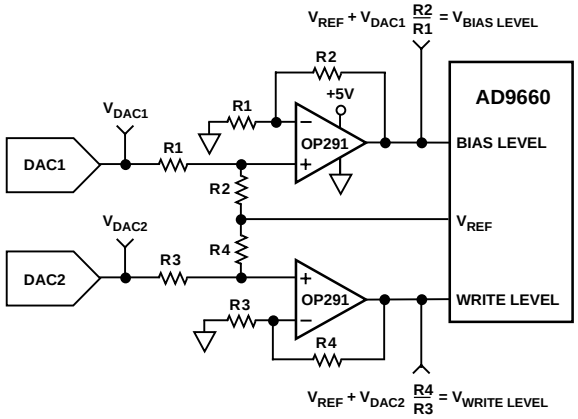


Figure 9. Driving the Analog Inputs

Offset Current Generator

The offset current source allows the user to inject a fixed, uncalibrated current into the laser diode. The offset current source is set by an external resistor connected between OFFSET CURRENT SET and $+V_S$, and is controlled by OFFSET PULSE. See Figure 2 for a transfer function of the offset current source.

The offset current may be used to increase the output current provided by the bias and/or write loops after calibration. Alternatively, the offset current may be added during the calibration of the bias loop and switched off after calibration to drop the bias current below the knee of the laser diode power curve. This is illustrated in Figure 10.

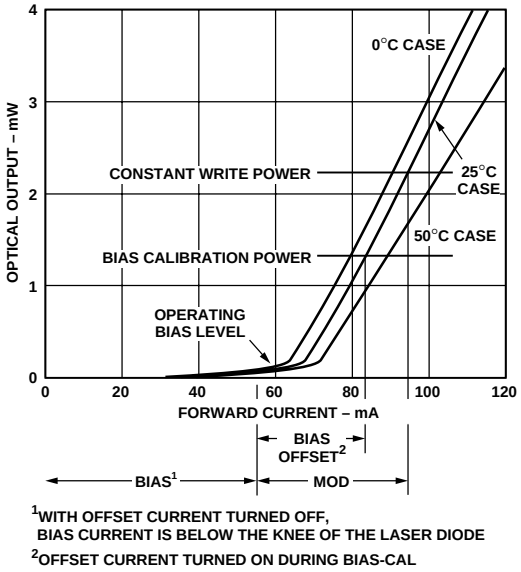


Figure 10. Laser Diode Current-to-Optical Power Curve Illustrating Bias Below Diode Knee

AD9660 Layout Considerations

As in all high speed applications, proper layout is critical; it is particularly important when both analog and digital signals are involved. Analog signal paths should be kept as short as possible, and isolated from digital signals to avoid coupling in noise. In particular, digital lines should be isolated from OUTPUT, PIN SENSE, WRITE LEVEL, and BIAS LEVEL traces. Digital signal paths should also be kept short, and run lengths matched to avoid propagation delay mismatch.

Layout of the ground and power supply circuits is also critical. A single, low impedance ground plane will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. 0.1 µF surface mount capacitors, placed as close as possible to the AD9660 $+V_S$ connections meet this requirement. Multilayer circuit boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance power planes to further reduce noise.

Minimizing the Impedance of the Output Current Path

Because of the very high current slew that the AD9660 is capable of producing (70+ mA in 1.5 ns), the inductance of the output current path to and from the laser diode is critical. A good layout of the output current path will yield high quality light pulses with rise times of about 1.5 ns and less than 5% overshoot. A poor layout can result in significant overshoot and ringing. The most important guideline for the layout is to minimize the impedance (mostly inductance) of the output current path to the laser. It is important to recognize that the laser current path is a closed loop. The figure illustrates the path that current travels: (1) from the output pins of the AD9660 to the anode of the laser, (2) through the laser to the cathode (ground), (3) through the return path, (4) through the 0.1 µF bypass capacitors back to the $+V_S$ pins of the AD9660 where (5) the current travels through the output driver circuitry of the AD9660, and back to the output pins. The inductance of this loop can be minimized by placing the laser as close to the AD9660 as possible to keep the loop short, and by placing the send and return paths on adjacent layers of the PC board to take advantage of mutual coupling of the path inductances. This mutual coupling effect is the most important factor in reducing inductance in the current path.

The trace from the output pins of the AD9660 to the anode of the laser (send trace) should be several millimeters wide and should be as direct as possible. The return current will choose the path of least resistance. If the return path is the ground plane, it should have an unbroken path, under the output trace, from the laser cathode back to the AD9660. If the return path is not the ground plane (such as on a two layer board, or on the $+V_S$ plane), it should still be on the board plane adjacent to the plane of the output trace. If the current cannot return along a path that follows the output trace, the inductance will be drastically increased and performance will be degraded.

Optimizing the Feedback Layout

In applications where the dynamic performance of the analog feedback loop is important, it is necessary to optimize the layout of the gain resistor, R_{GAIN}, as well as the monitor current path to SENSE IN. Such applications include MOD systems which recalibrate the write loop on pulses as short as 25 ns, and closed loop applications.

The best possible TZA settling will be achieved by using a single carbon surface mount resistor (usually 5% tolerance) for R_{GAIN} and small surface mount capacitor for C_{GAIN}. Because the GAIN pin (Pin 9) is essentially connected to the inverting input of the TZA, it is very sensitive to stray capacitance. R_{GAIN} should be placed between Pin 9 and Pin 10, as close as possible to Pin 9. Small traces should be used, and the ground and $+V_S$ planes adjacent to the trace should be removed to further minimize stray capacitance.

The trace from SENSE IN to the cathode of the PIN photodetector should be thin and routed away from the laser anode trace.

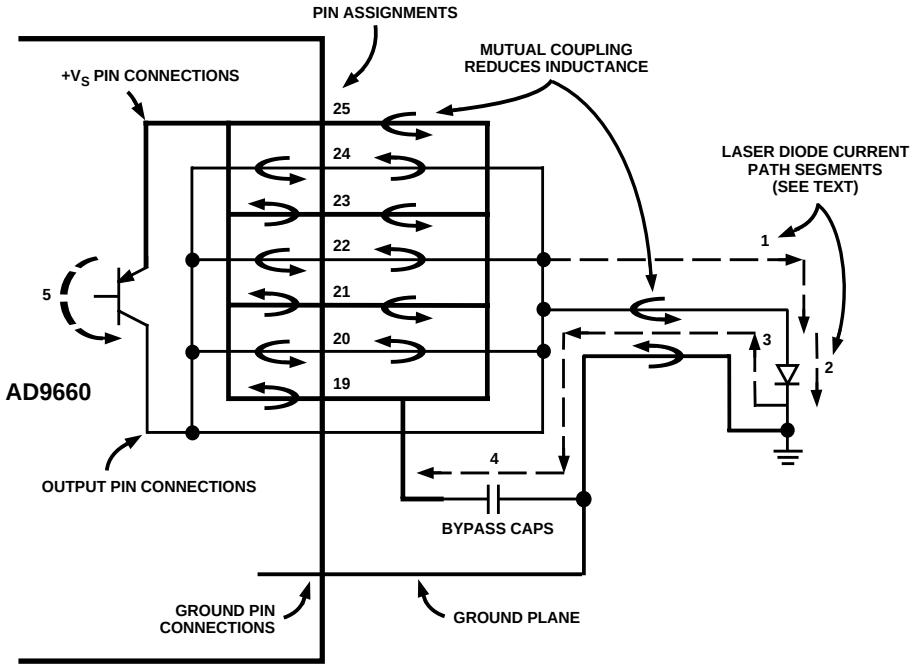
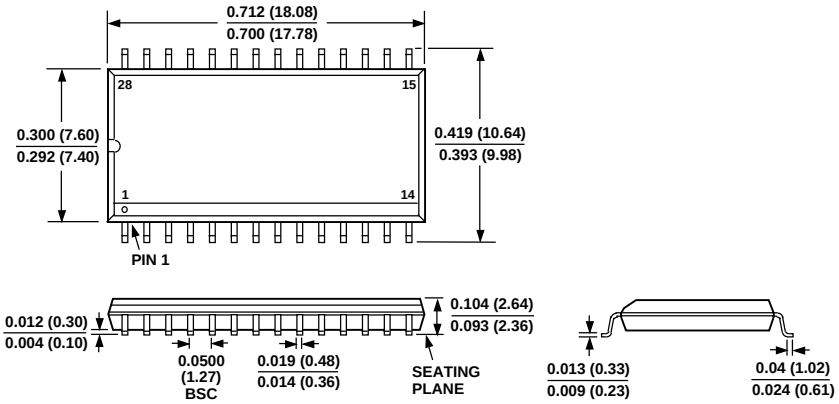


Figure 11. Laser Diode Current Loop

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Pin Plastic SOIC
(R-28)



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