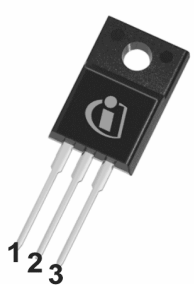
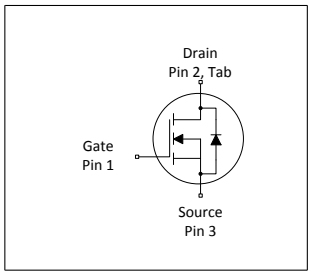
MOSFET

600V CoolMOS™ P7 Power Transistor

PG-TO 220 FP



The CoolMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of body diode against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.



Features

- Suitable for hard and soft switching (PFC and LLC) due to an outstanding commutation ruggedness
- Significant reduction of switching and conduction losses
- Excellent ESD robustness >2kV (HBM) for all products
- Better $R_{DS(on)}$/package products compared to competition enabled by a low $R_{DS(on)}$*A (below 1Ohm*mm²)
- Large portfolio with granular RDS(on) selection qualified for a variety of industrial and consumer grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to low switching and conduction losses
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due to >2 kV ESD protection
- Suitable for a wide variety of applications and power ranges

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	99	mΩ
$Q_{g.typ}$	45	nC
$I_{D,pulse}$	100	A
E_{oss}@400V	5.0	µJ
Body diode di/dt	900	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPA60R099P7	PG-TO 220 FullPAK	60R099P7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	31 20	A	T_C=25°C T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	100	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	105	mJ	I_D=5.1A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.53	mJ	I_D=5.1A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	5.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	80	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	29	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	31	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	100	A	T_C=25°C
Reverse diode dv/dt[3)]	dv/dt	-	-	50	V/ns	V_{DS}=0...400V, I_{SD}<=31A, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	900	A/µs	V_{DS}=0...400V, I_{SD}<=31A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

[1)] Limited by $T_{j\,max}$. Maximum Duty Cycle D = 0.50; TO-220 equivalent
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical Rg

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.31	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	-
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.53mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.077 0.18	0.099 -	Ω	V_{GS}=10V, I_D=10.5A, T_j=25°C V_{GS}=10V, I_D=10.5A, T_j=150°C
Gate resistance	R_G	-	5.9	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1952	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	33	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	62	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	649	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=10.5A, R_G=5.3Ω; see table 9
Rise time	t_r	-	15	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=10.5A, R_G=5.3Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	89	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=10.5A, R_G=5.3Ω; see table 9
Fall time	t_f	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=10.5A, R_G=5.3Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	11	-	nC	V_{DD}=400V, I_D=10.5A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	14	-	nC	V_{DD}=400V, I_D=10.5A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	45	-	nC	V_{DD}=400V, I_D=10.5A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	V_{DD}=400V, I_D=10.5A, V_{GS}=0 to 10V

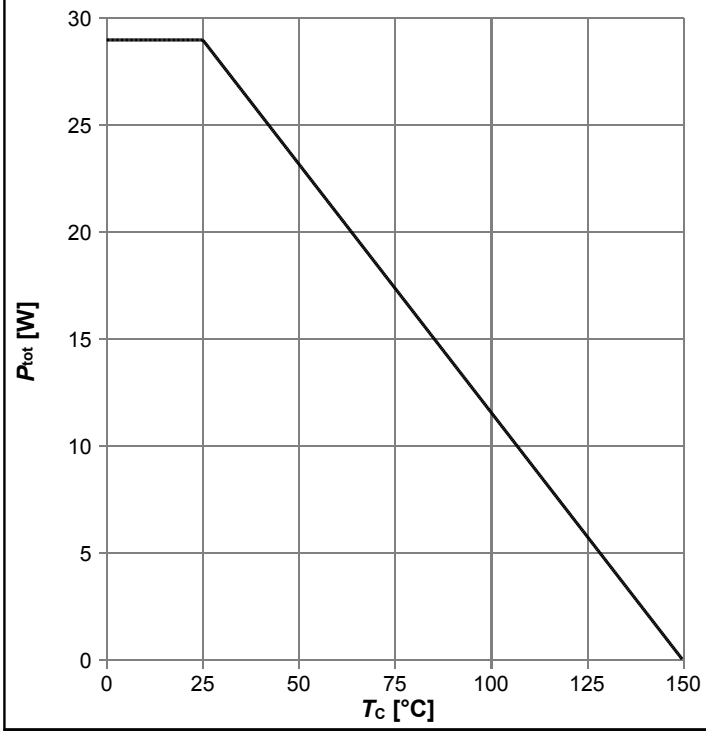
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=10.5A, T_j=25°C
Reverse recovery time	t_{rr}	-	211	-	ns	V_R=400V, I_F=4A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	2.1	-	µC	V_R=400V, I_F=4A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	20.1	-	A	V_R=400V, I_F=4A, di_F/dt=100A/µs; see table 8

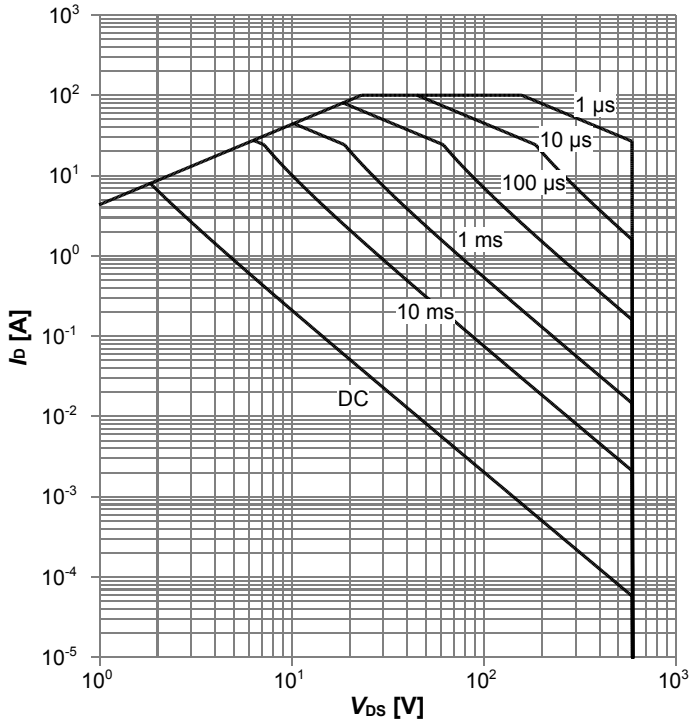
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



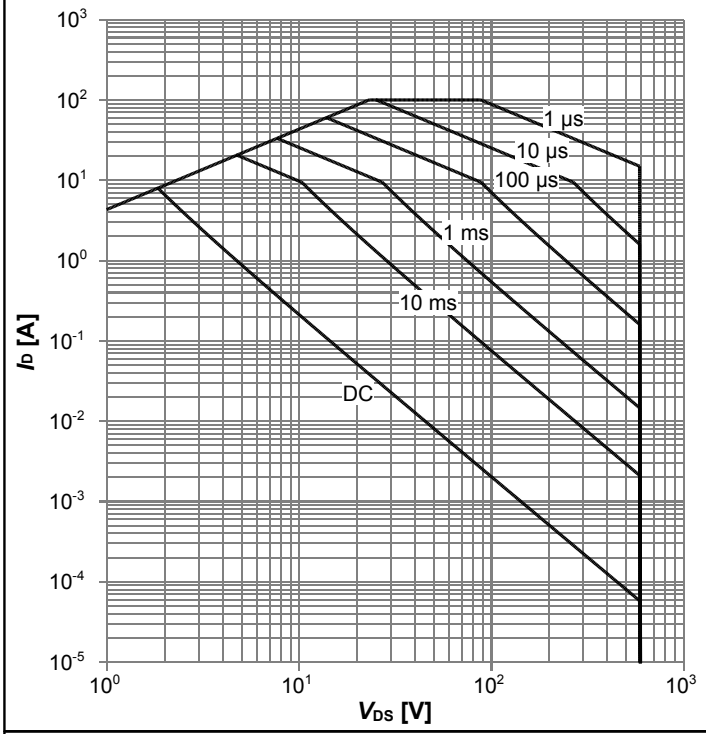
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



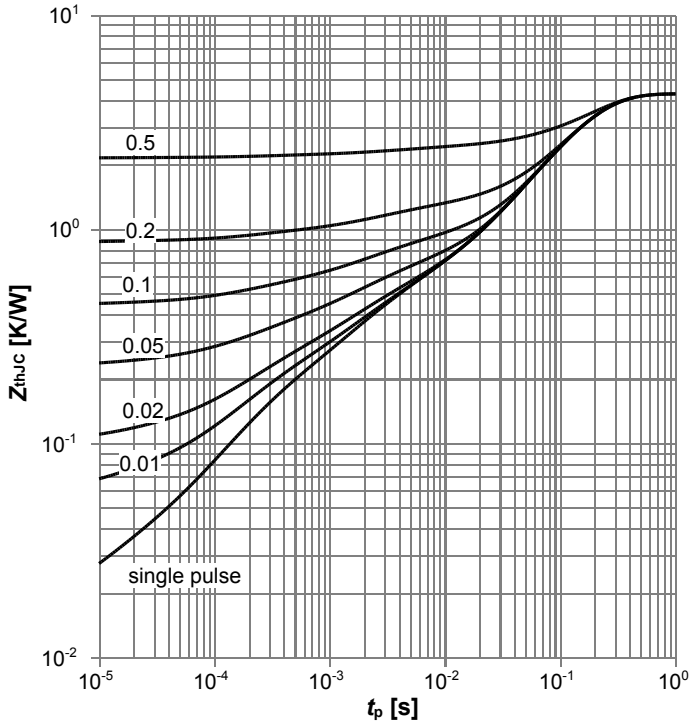
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



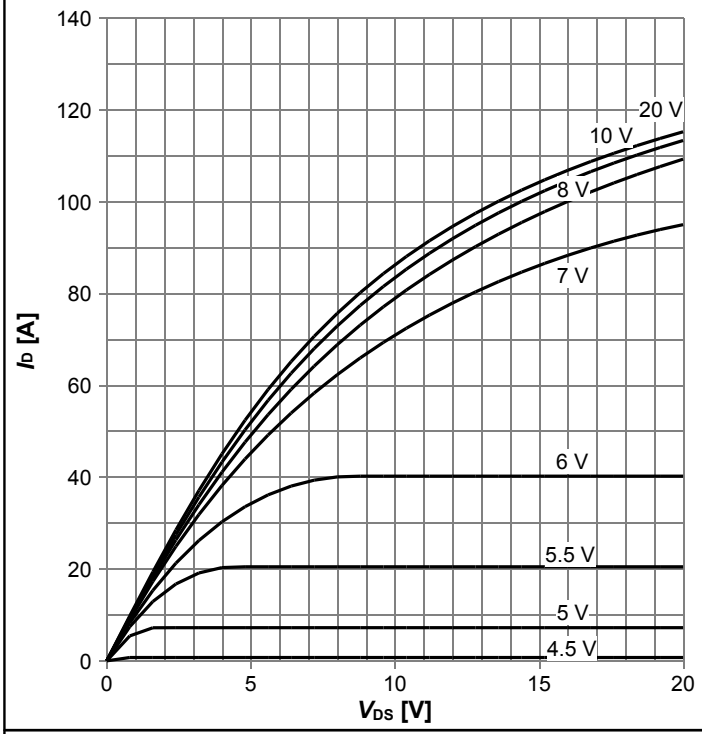
$I_D=f(V_{DS})$; T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



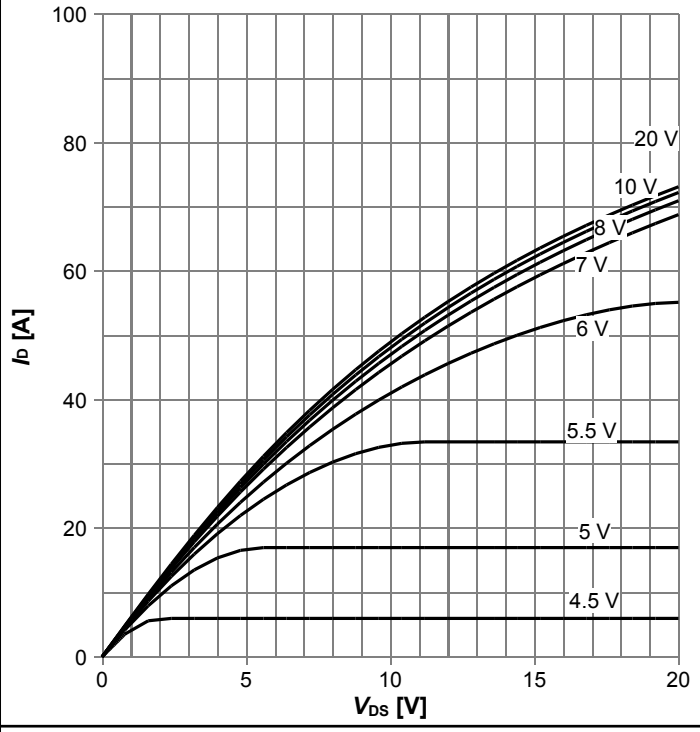
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



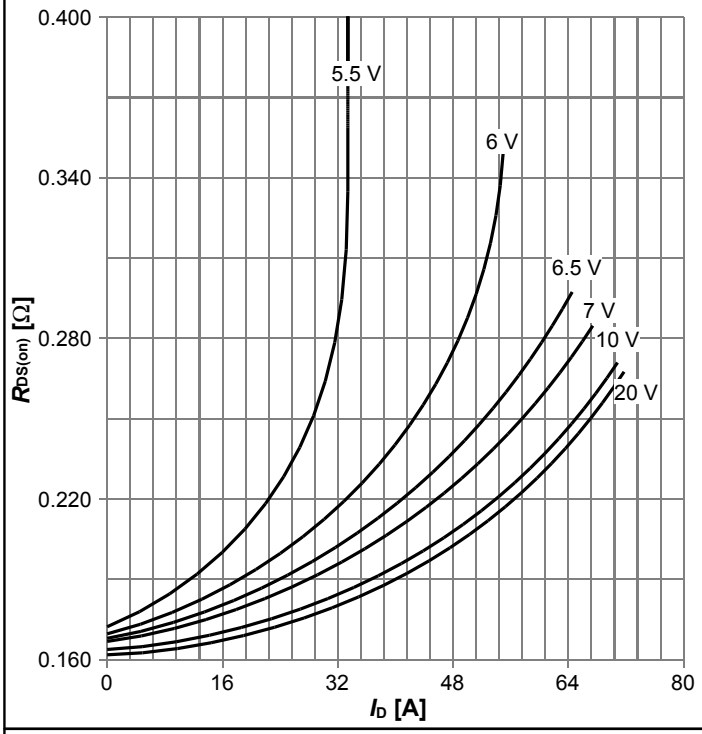
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



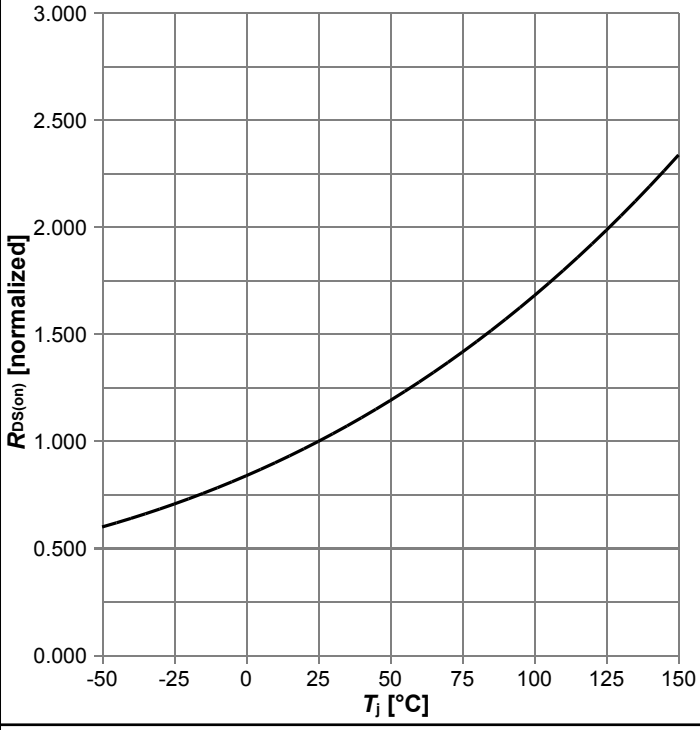
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



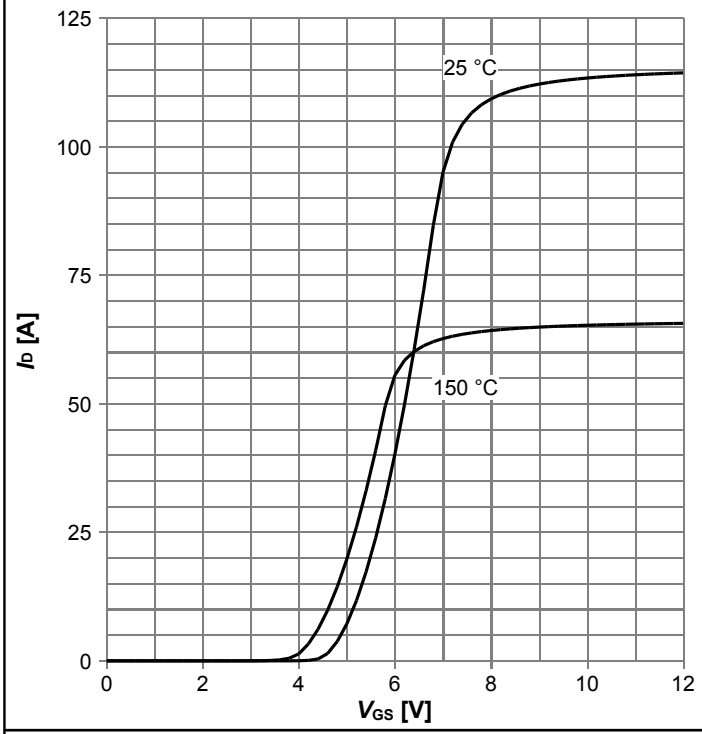
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



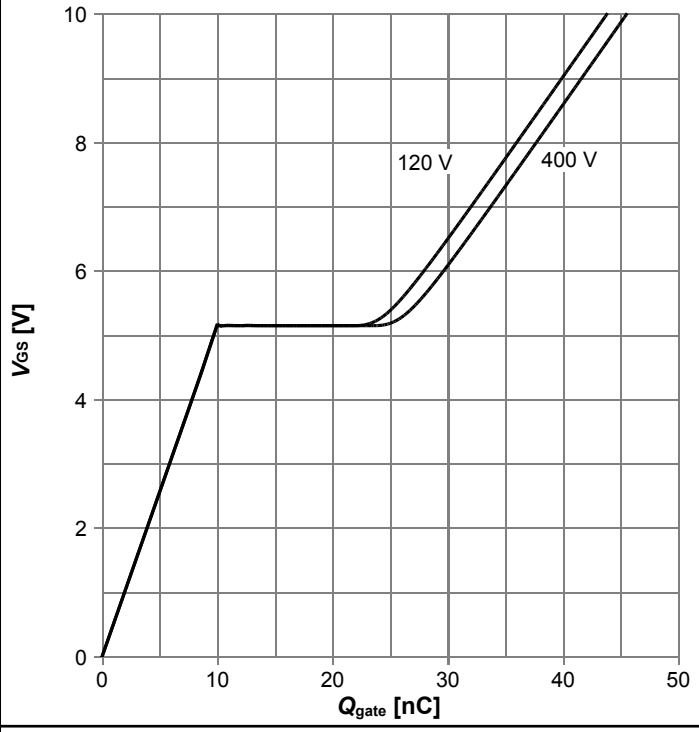
$R_{DS(on)}=f(T_j)$; $I_D=10.5$ A; $V_{GS}=10$ V

Diagram 9: Typ. transfer characteristics



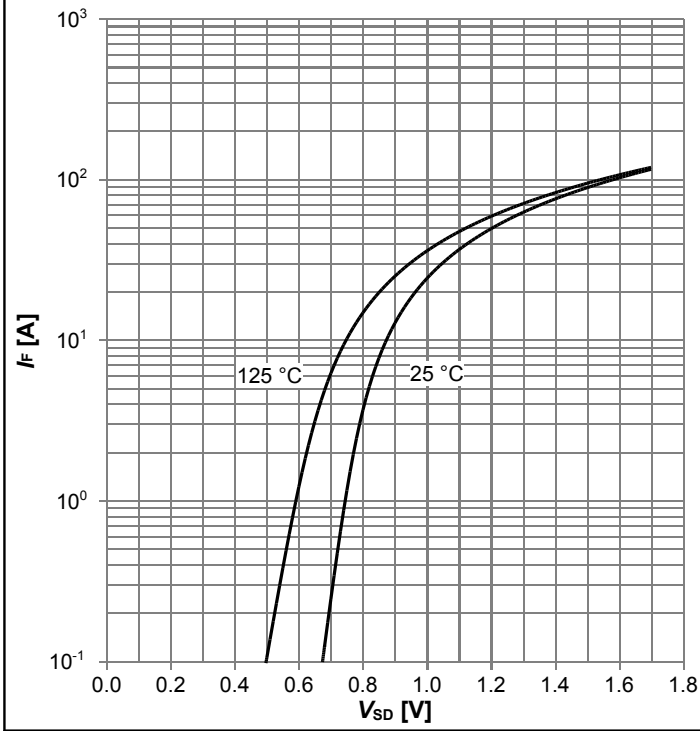
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



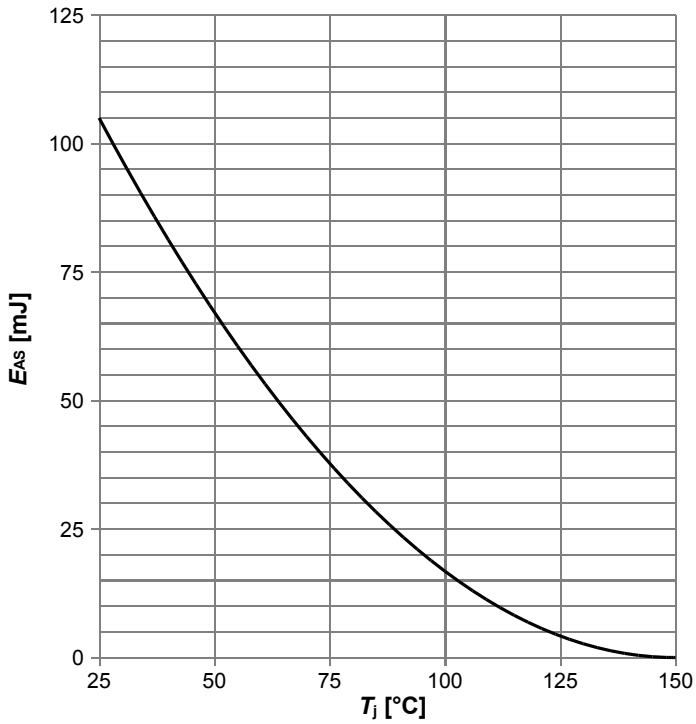
$V_{GS}=f(Q_{gate})$; I_D=10.5 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



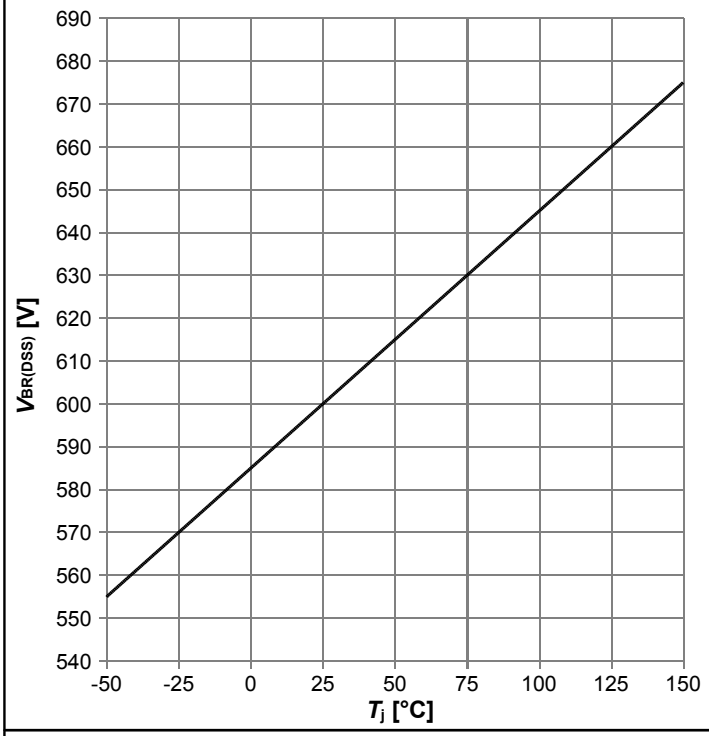
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



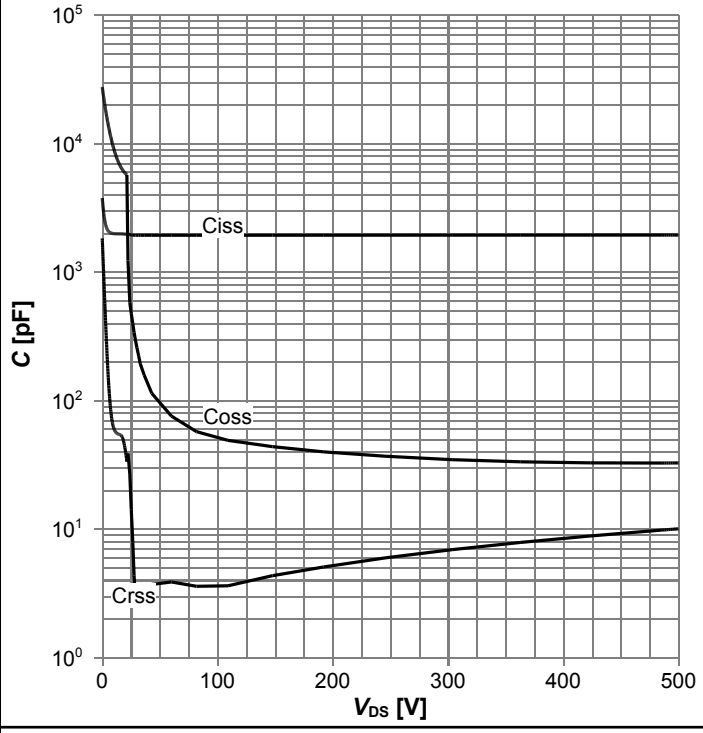
$E_{AS}=f(T_j)$; I_D=5.1 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



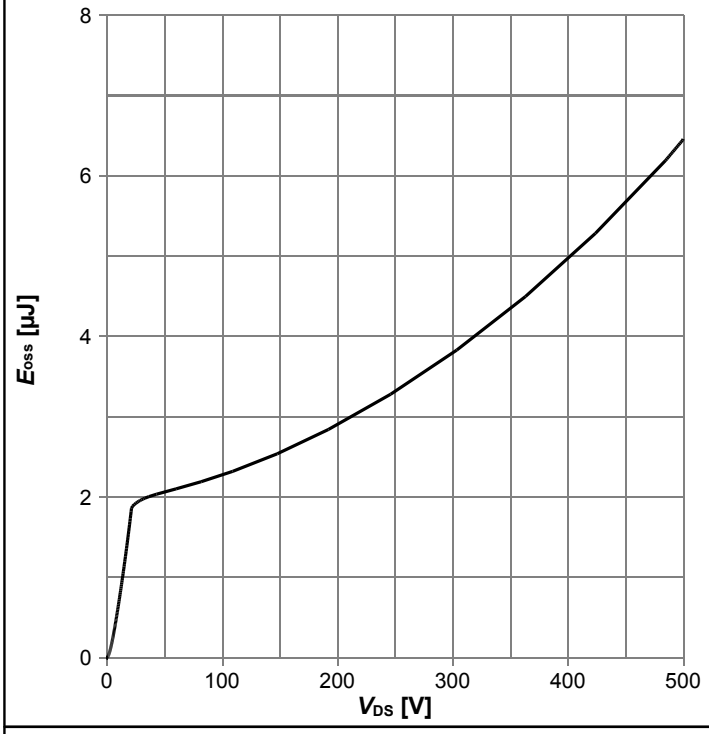
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

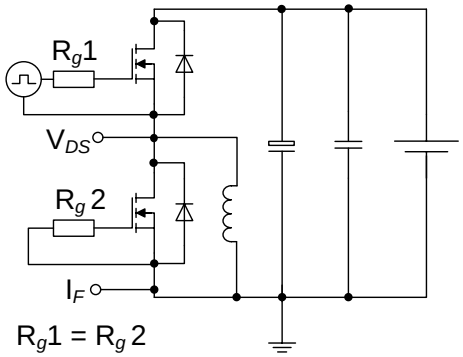
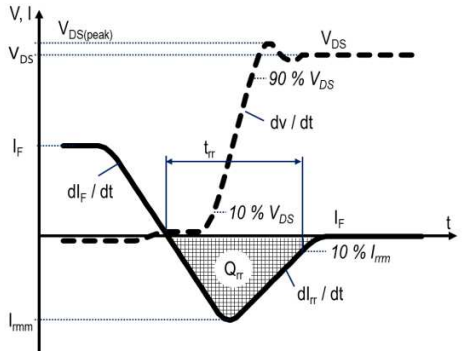
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

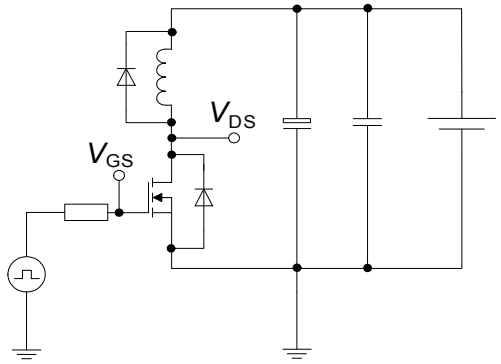
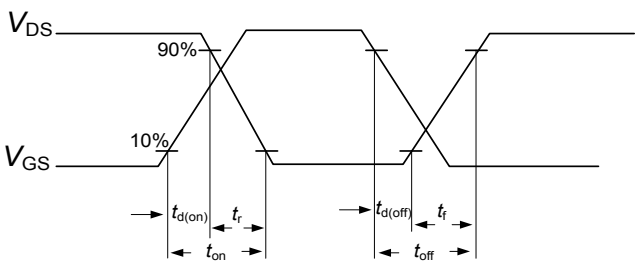
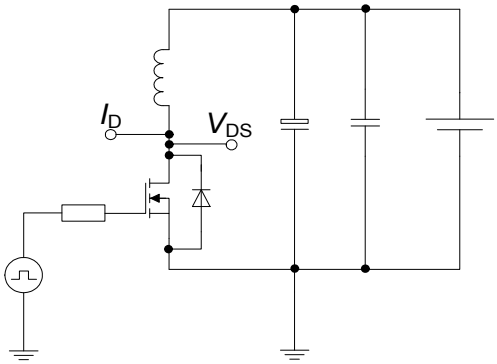
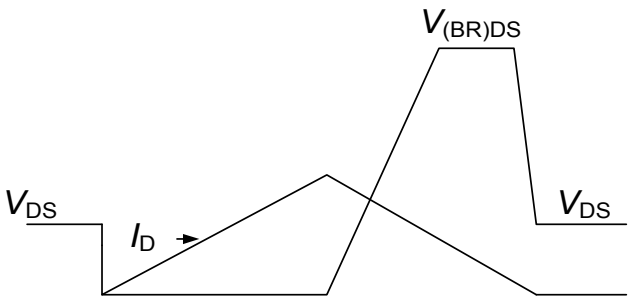
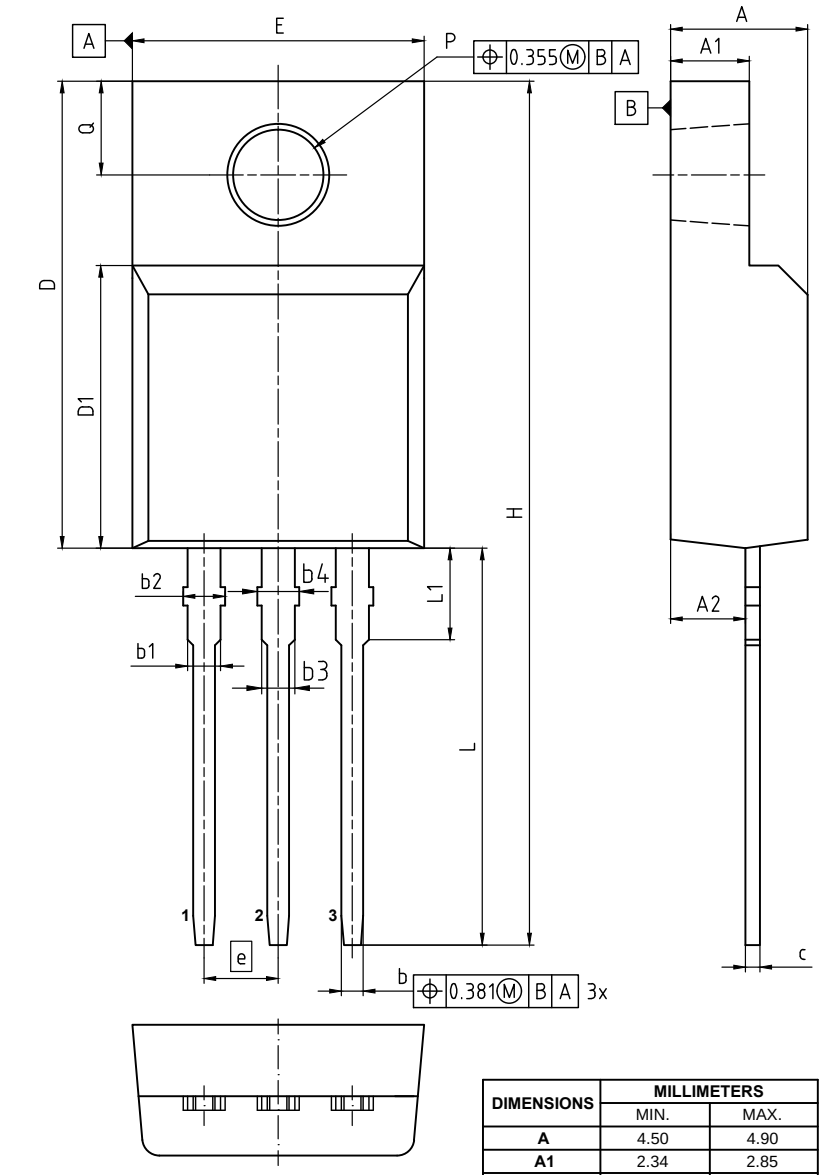
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281 AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

DOCUMENT NO.
Z8B00003319

REVISION
07

SCALE 5:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION

ISSUE DATE
27.01.2017

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS P7 Webpage:** www.infineon.com
- **IFX CoolMOS P7 application note:** www.infineon.com
- **IFX CoolMOS P7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA60R099P7

Revision: 2017-05-18, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2017-05-18	Release of final version

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