Hot-Swapping Delta39K™ and Quantum38K™ CPLDs

Introduction

This application note details the native ability of Delta39K™ and Quantum38K™ CPLDs to support hot-swapping, also known as hot-socketing. Hot-swappability protects against destructive events resulting from swapping system components while a host system remains active. The general levels of hot-swap protection are discussed herein, concluded by a description of the specific Delta39K hot-swap capabilities and an example CompactPCI Hot-Swap compliance declaration. This document refers to Delta39K, but the discussion is also applicable to Quantum38K.

The Delta39K family of Complex Programmable Logic Devices (CPLDs) combines dense logic, embedded memory, a Phase Locked Loop (PLL), and configurable I/O standards. This combination helps to make Delta39K devices the PLD of choice for reliable, high-performance designs in such areas as telecommunications, networking, and data processing. The Quantum38K family offers high-density CPLDs specifically designed for high-volume, low-cost applications.

The Delta39K's inherent hot-swap capability complements this application space. Component hot-insertion and extraction is no longer reserved for critical high-end systems; it is increasingly expanding to mainstream designs. This movement is spurred by hot-swap specification adoption from such bus standards as CompactPCI used in backplanes, to Universal Serial Bus (USB) and PCMCIA used for PC peripheral communication. Now a way of life, systems supporting hot-swapping promote high-reliability, datapath redundancy, ease-of-use, and system maintenance with zero downtime.

The robustness of the Delta39K I/O structures permits active signals to be applied to the device pins even with device power disabled. The internal circuitry is protected against undesired current flow induced by external voltage stimuli. This improves durability and long-term reliability at the device and board levels.

The Hot-Swap Environment

Hot-swap capabilities permit swapping of system components (modules in a host system) without cycling system power. In this way, system operation can continue uninterrupted with an updated hardware configuration.

For a host-module hot-swap-enabled system, two scenarios are of concern:

- A module containing a Delta39K is plugged into a powered system
- A module containing a Delta39K is powered down while connected to a live system

In the first situation, active system signals are asserted to the device I/Os before the board V_{CC} ramps. If no protection circuitry exists, current can flow from an input pin to device V_{CC} (initially at GND state) through diode clamps if sufficient voltage is applied to the I/Os. This low-impedance path can cause significant thermal damage or latch-up (latch-up being the phenomenon by which input current triggers activation of parasitic transistors within the device substrate in positive feedback yielding damaging uncontrolled currents).

In the second situation, the main concern is ensuring that there is no signal disturbance on the active system bus during the module power-down event. Driver contention or glitches resulting from the power-down can lead to data corruption on the system side.

At a minimum, a hot-swap compatible device should be able to withstand, without damage to itself, active signals on its pins while powered down. In constant-operation systems, one must also ensure that the power-up and power-down of the device does not disturb attached system bus signals.

When designing boards to withstand hot-swap conditions, it is important to understand the causes, effects, and protective measures associated with these principles.

Levels of Hot-Swap Protection

The ability to support hot-swapping at the device level is typically a feature of the device family. There are distinct degrees to which a device can support hot-swapping; each higher level provides additional protection above the lower to guard against system data corruption.

The generally accepted levels of hot-swap protection are discussed below. Level 1 isolation protects the hot-swap device itself from damage when live signals are applied while the V_{CC} level lies well below nominal voltage. Level 2 and above extend protection to the system-level to protect against data disruption on the active bus. Further information can be found in the references found at the end of this application note.

Level 0 Isolation: No Protection

This level represents those devices that lack hot-swap protection which thereby lead to catastrophic device failures under hot-swap conditions.

For example, consider a standard CMOS implementation as illustrated in *Figure 1*. Under- and over-voltage protection clamp diodes are often chained to the I/O pins to protect against MOS gate oxide breakdown. While this protects internal I/O structures from destructive voltage overshoot and undershoot, at the same time it forms a direct current path between a signal pin and V_{CC}. This path can also take the form of parasitic diodes with the same destructive effect.

In a hot-insertion event or when a board is powered-down, commonly live system signals arrive at device pins before board power has a chance to ramp to nominal levels. The effect is potentially a forward-biased clamp diode if a high voltage is applied to the I/O prior to V_{CC} reaching nominal levels. In this way, destructive high currents from signal pins into V_{CC} are possible which can cause latch-up and irreparable thermal damage within a device. Even if the device sur-

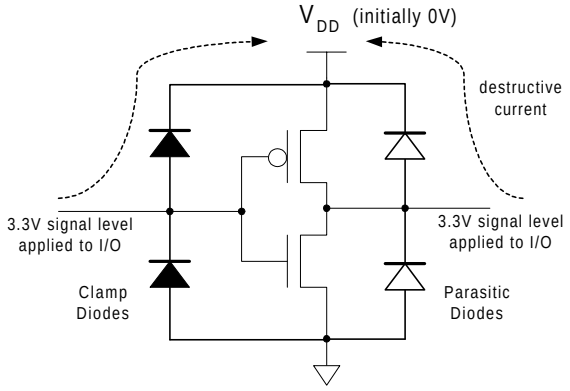

Figure 1. Standard CMOS Buffer Without Isolation

vives, the likely outcome is corrupted system data or out-of-spec loading conditions.

Level 1 Isolation: I/Os Three-Stated when Powered Down

The first level of hot-swap protection isolates the basic clamp diodes (eliminating the high-current path from signal I/O to V_{CC}) and prevents bus-loading on an active system while the device is powered-down.

The condition for device I/Os to remain in a high-impedance state while the device is powered off is added to achieve this minimum isolation.

This isolation level protects a powered-down device from being damaged by active bus signals, and at the same time protects the system bus from inadvertent loading or contention while powered-down components are connected.

Level 2 Isolation: I/Os Three-Stated During Power Ramp

The second level of isolation builds from Level 1 by requiring that the device I/Os must remain three-stated during the power-up and power-down ramp of V_{CC}. This eliminates the possibility of system bus contention during board power transitions.

In this way, device outputs are enabled only after V_{CC} rises above a set threshold (on power-up) or until V_{CC} falls below the threshold (on power-down). Built-in logic management circuitry (manipulating pin output enables) performs this function, thereby providing system-level protection during module power transitions.

Level 3 Isolation: Transient Protection at Hot-Insertion

The third level of isolation contains all lower-level protection measures, and additionally includes pre-bias circuitry to ease transients on the system bus at hot-insertion events. It provides the highest system-level protection.

Consider a Level 2 isolated hot-swap board being plugged into an active system bus. During this occurrence, the system bus instantaneously sees extra stray capacitance from disabled I/Os on the daughter board, causing a signal glitch of a duration that depends on the board electrical characteristics. A significant glitch crossing a system receiver's threshold will lead to data corruption.

Level 3 isolation works to eradicate possible glitches by minimizing the impact of stray capacitance transiently loading the system. This is achieved by adding pre-bias circuitry to precharge the stray capacitance on I/O pins before they contact the system bus. This precharge circuitry is disengaged once power ramps above a set threshold and the hot-swapping event completes.

Since bus activity is not suspended during hot-swap of system boards, the highest level of isolation is required to maintain system reliability. As a system consideration, in order to support Level 3 protection V_{CC} and GND must mate (to perform precharge) before signal voltages reach device I/O pins. This is typically accomplished by staggering pins on the board connector such that the pin contact sequence is assured during mechanical insertion and extraction. *Figure 2* illustrates this system-level solution.

This precharge voltage can be established internal to the Level 3 capable device using early power, or can exist as external board circuitry.

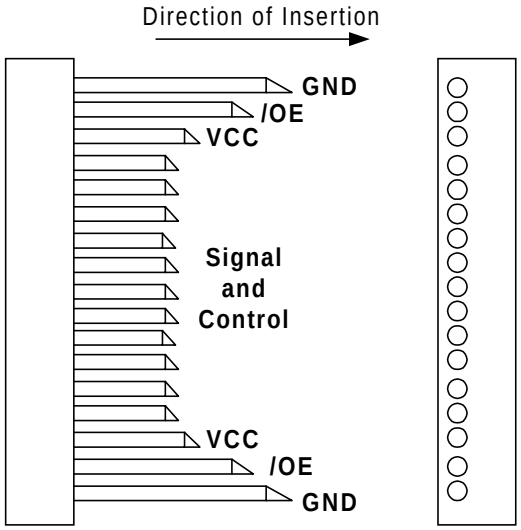

Figure 2. Level 3 Isolation Implemented at System-Level Staggers Pin Lengths to Control Power-Up Sequence

Delta39K Hot-Swap Capability

The Delta39K family of CPLDs natively supports hot-swap capabilities up to Level 2 isolation discussed above; that is, I/Os are guaranteed to be three-stated when device power is disabled or ramping. Extension to Level 3 isolation can be accomplished at the board level, and depends on the specific bus specification. An example is described in the CompactPCI Hot-Swap Ready Delta39K solution discussed below.

Beyond power-up, Delta39K I/Os are guaranteed to remain in three-state during configuration cycles (outputs are enabled only after configuration completes). The Delta39K I/O structures are tolerant to live signals with or without device power applied.

These characteristics allow Delta39K CPLDs to be used in a wide variety of applications without fear of device or system

damage. In many cases, additional hot-swap management logic is not required.

CompactPCI Hot-Swap Compliance

An Application of Delta39K Hot-Swap Capabilities

The hot-swap capability of Delta39K CPLDs can be translated to specific hot-swap specification compliance such as CompactPCI Hot-Swap Specification R2.0. The Delta39K compliance to CompactPCI Hot-Swap silicon requirements is overviewed below.

There are three grades of CompactPCI Hot-Swap: Capable, Friendly, and Ready. Ready is the easiest to use, and requires the most capability on the part of the silicon. Each grade offers the capabilities of the lower grades, plus additional functionality. Delta39K meets all requirements excluding the exception noted below:

CompactPCI Hot-Swap Capable

- Full compliance for 3.3V PCI signal environment

CompactPCI Hot-Swap Friendly

- Full compliance for 3.3V PCI signal environment

CompactPCI Hot-Swap Ready

- Delta39K does not natively offer bias voltage support (precharge bias must be supplied externally)

The exception for CompactPCI Hot-Swap Ready silicon can be solved at the board level. As described in the CompactPCI Hot-Swap specification, the CompactPCI Signal Electrical Model allows a precharge voltage to be established (optimally 1V ± 20%) from the presence of a pull-up precharge resistor to the precharge voltage supply. The upper leakage current limits from the active bus upon hot-insertion, as well as from the on-board hot-swap device is specified.

Cypress recommends any precharge voltage level within this range of 0.8V to 1.2V, at the discretion of the system designer. This precharge voltage can be maintained for any arbitrary duration.

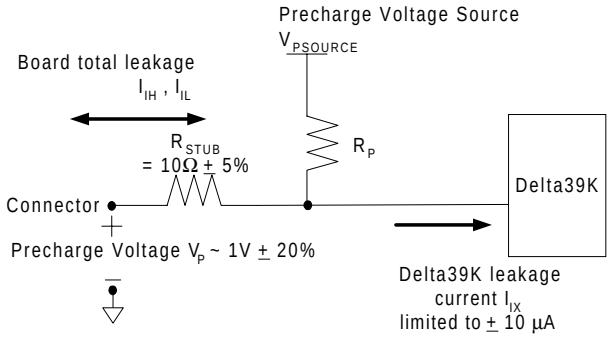

Figure 3. CompactPCI Board External Precharge

As the CompactPCI Hot-Swap spec recommends, an external resistor selected as a pullup to the precharge voltage source creates the beneficial voltage bias prior to pin contact with the CompactPCI backplane. *Figure 3* illustrates a simplified signal electrical model of a conventional hot-swap board implementation (see CompactPCI spec section 3.1). Listed in *Table 1* is a brief description of model parameters.

Table 1. Electrical Model Parameters

R_{STUB}	10Ω board stub resistor which provides load isolation and some series damping
R_P	Precharge voltage source resistance
$V_{PSOURCE}$	Precharge voltage source
V_P	Resultant precharge bias voltage on the board connector prior to contact with the CompactPCI bus, specified to 1V ± 20%
I_{IX}	(or $I_{PCILeakage}$) Leakage of the PCI silicon
I_{IH}, I_{IL}	Resultant board leakage current resulting from contact between the board and Compact-PCI backplane

The hot-swap board designer must select compatible R_P and $V_{PSOURCE}$ to remain within the CompactPCI specifications of V_P (before board insertion) and I_{IH}/I_{IL} (after insertion contact).

In such a configuration, the board leakage currents can be solved by Equation 1 and 2 shown below.

$$I_{IH} = \frac{V_{IN} + I_{IX} \bullet R_P - V_{PSOURCE}}{R_P + R_{STUB}} \quad \text{Eq. 1}$$

$$I_{IL} = \frac{V_{PSOURCE} - V_{IN} + I_{IX} \bullet R_P}{R_P + R_{STUB}} \quad \text{Eq. 2}$$

where V_{IN} is an external voltage applied to the node V_P.

Example 1

In this example, the precharge resistor R_P must be disconnected prior to the CompactPCI BDSEL# signal connection (last stage of insertion sequence). This removes the significant DC loading on bus signals.

For $V_{PSOURCE}$ = 1.0V, R_P = 10 kΩ, R_{STUB} = 10Ω, and Delta39K I/O leakage bound between ± 10 µA (per Delta39K family spec), the precharge circuit theoretical leakage results are:

I_{IH} max (@ V_{IN} = 2.7V): 160 µA (spec limit 200 µA)

I_{IL} max (@ V_{IN} = 0.5V): –40 µA (spec limit –70 µA)

The typical leakage current from Delta39K I/Os is more closely limited to ± 2 µA, however. Given this, the CompactPCI Hot Swap Specification R2.0 permits a configuration whereby an external resistor (> 50 kΩ) selected as a pullup to the precharge voltage source is allowed to be permanently connected even during normal board operations. In this 3.3V environment, the leakage currents are more tightly specified.

Example 2

The precharge resistor R_P (50 kΩ) remains connected during normal board operations. In this configuration, it is critical to ensure that the precharge voltage V_P remain in the specified range of 1V ±20%. Before insertion, the leakage through the

hot-swap silicon device (Delta39K) will cause variation of V_P. This variation is amplified with a larger selected R_P.

For $V_{PSOURCE}$ = 1.0V, R_P = 50 kΩ, R_{STUB} = 10Ω, and typical Delta39K I/O leakage between ±2 µA, the precharge voltage becomes 1V ± 0.1V. This allows for ± 10% uncertainty in the selected $V_{PSOURCE}$. The maximum board leakage is found from the above equations when V_{IN} = 3.3V for I_{IH} and 0V for I_{IL}:

I_{IH} max: 48 µA (spec limit 55 µA)

I_{IL} max: –22 µA (spec limit –35 µA)

Both examples show that Delta39K meets CompactPCI Hot-Swap specification limits for external hot-swap Level 3 isolation solutions.

In short, Delta39K CPLDs are fully CompactPCI Hot-Swap Ready except for a lack of internal pre-bias circuitry. This is easily overcome at the board-level as shown above, giving sufficient guardband for voltage source and component variation. Note that Delta39K supports only 3.3V PCI.

Summary

Clearly, the intrinsic hot-swap capabilities of Delta39K and Quantum38K CPLDs allow for use in a wide array of applications demanding system tolerance to varying power and signal sequence combinations. In promoting hot-swapping, these devices are guaranteed resilient to active signals and prevent system bus loading while powered-down.

When used in conjunction with hot-swap power management ICs (which limit inrush current to protect board connector and bypass capacitors upon board V_{CC} ramp), the Delta39K and Quantum38K families of CPLDs provide an effective solution for hot-swap applications. No intermediate bus isolation devices are required.

With the high impedance initial state, robust ESD structures, and programmable-per-pin signaling standards, the Delta39K and Quantum38K provide flexible and predictable I/Os. The hot-swap capability of these CPLD families complements the enhanced feature set of high CPLD logic density with embedded features like single-port, dual-port, and FIFO memory and PLLs.

References

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