

EB13C5F2H-33.333M

[Click part number to visit Part Number Details page](#)

REGULATORY COMPLIANCE (Data Sheet downloaded on Jul 18, 2018)


[Click badges to download compliance docs](#)

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ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVCMOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 33.333MHz ± 20 ppm over 0°C to +70°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	33.333MHz
Frequency Tolerance/Stability	± 20 ppm over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Supply Voltage	3.3Vdc $\pm 10\%$
Input Current	5mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	4nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 $\pm 5\%$ (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Logic Control / Additional Output	Tri-State
Tri-State Input Voltage (Vih and Vil)	90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)
Standby Current	10 μ A Maximum (Disabled Output: High Impedance)
RMS Phase Jitter	1pSec Maximum (Fj = 12kHz to 20MHz)
Period Jitter (Deterministic)	0.2pSec Typical, 3pSec Maximum
Period Jitter (Random)	2pSec Typical, 5pSec Maximum
Period Jitter (RMS)	3pSec Typical, 7pSec Maximum
Period Jitter (pk-pk)	40pSec Typical, 100pSec Maximum
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

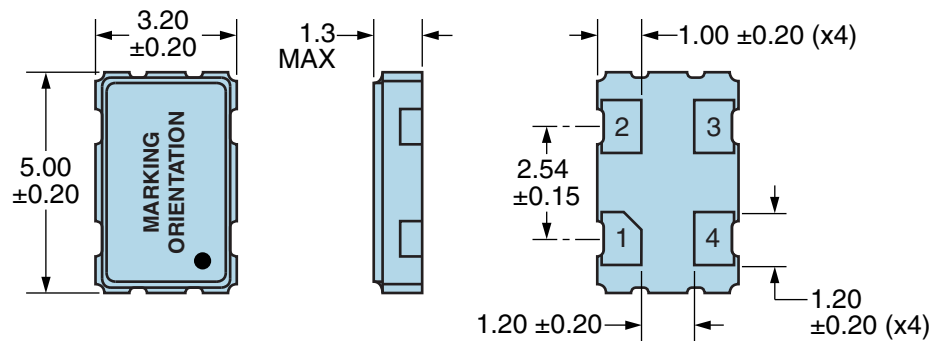
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)

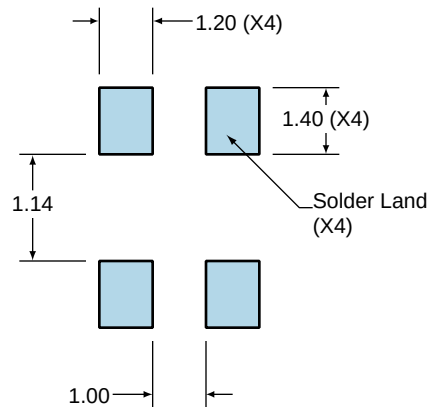


PIN	CONNECTION
1	Tri-State
2	Case/Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E33.333 E=Ecliptek Designator
2	XXXXX XXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters

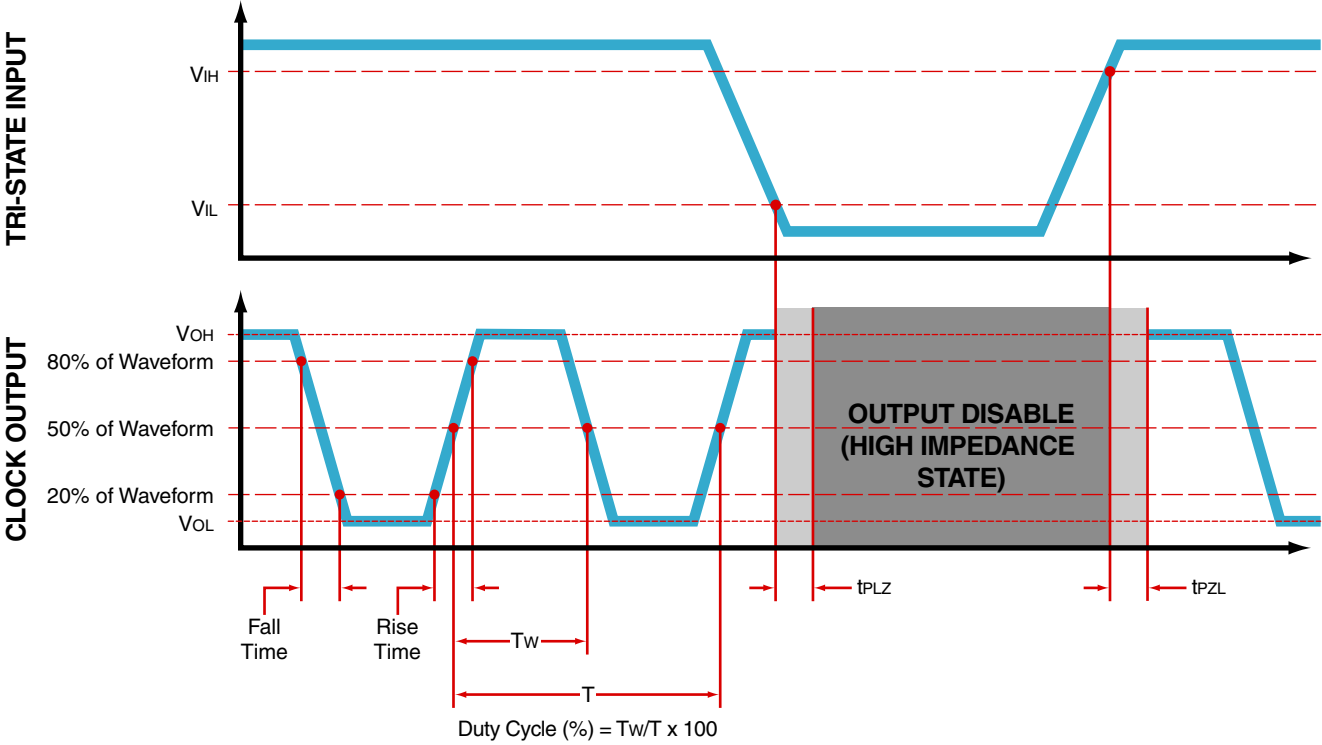


All Tolerances are ±0.1

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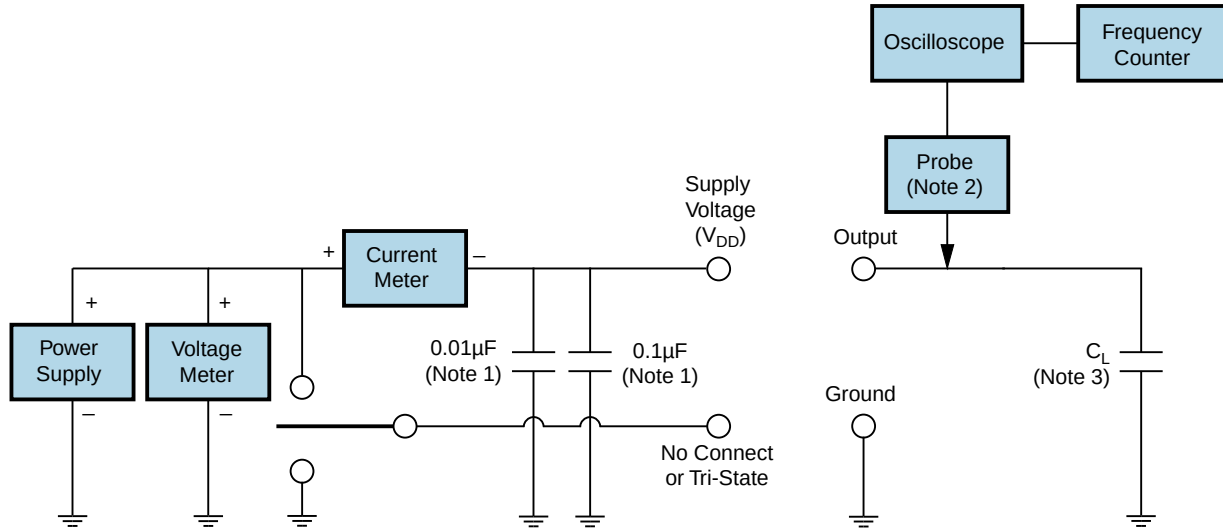
OUTPUT WAVEFORM & TIMING DIAGRAM



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Test Circuit for CMOS Output



Note 1: An external $0.1\mu\text{F}$ low frequency tantalum bypass capacitor in parallel with a $0.01\mu\text{F}$ high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>300\text{MHz}$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.