

# DTMF receiver for telephones

## BU8871F

The BU8871F is a DTMF receiver ICs developed for use in telephone answering machines, and converts 16 different types of DTMF signals into 4-bit binary serial data. It features a wide dynamic range, eliminating the need for an external input amplifier. Expertise from a number of companies has been incorporated into these products to enable guard time control through a host microcomputer.

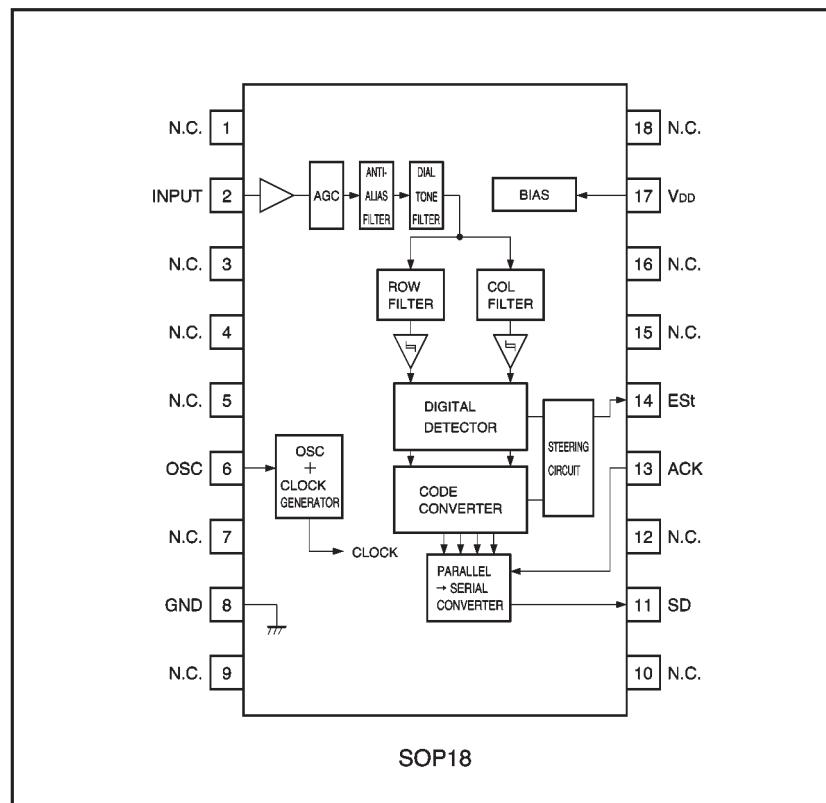
### ● Applications

Telephone answering machines

### ● Features

- 1) Dynamic range of 45dB. (internal AGC)
- 2) 4-bit binary serial data output.
- 3) Guard time can be controlled through host microcontroller.
- 4) Input pins equipped with hysteresis. (ACK pin)
- 5) 4.19MHz crystal resonator can be used.

### ● Block diagram



## ●Absolute maximum ratings (Ta=25°C)

| Parameter             | Symbol           | Limits                       | Unit |
|-----------------------|------------------|------------------------------|------|
| Power supply voltage  | V <sub>DD</sub>  | 7                            | V    |
| Input voltage         | V <sub>IN</sub>  | GND-0.3~V <sub>DD</sub> +0.3 | V    |
| Output voltage        | V <sub>OUT</sub> | GND-0.3~V <sub>DD</sub> +0.3 | V    |
| Power dissipation     | P <sub>d</sub>   | 550*1                        | mW   |
| Operating temperature | T <sub>opr</sub> | -10~+70                      | °C   |
| Storage temperature   | T <sub>stg</sub> | -55~+125                     | °C   |

\*1 Reduced by 5.5 mW for each increase in Ta of 1°C over 25°C.

## ●Recommended operating conditions (Ta=25°C)

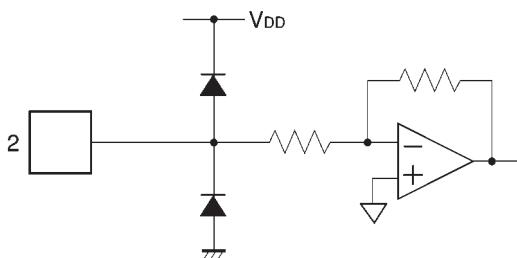
| Parameter                       | Symbol            | Limits    | Unit |
|---------------------------------|-------------------|-----------|------|
| Power supply voltage            | V <sub>DD</sub>   | 4.75~5.25 | V    |
| Oscillation frequency           | f <sub>osc</sub>  | 4.194304  | MHz  |
| Oscillation frequency deviation | Δf <sub>osc</sub> | -0.1~+0.1 | %    |

## ●Pin descriptions

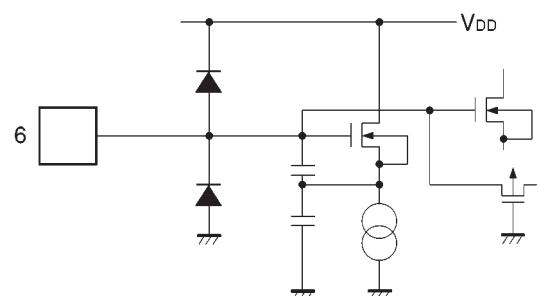
| Pin No.                                  | Pin name        | Function  |
|--|-----------------|---|
| 2  | INPUT           | This is the audio signal input pin, and should be AC coupled.   |
| 6  | OSC             | This is the input pin for the internal oscillator. Connect a 4.194304 MHz crystal resonator between this pin and GND, or use input from an external oscillator.   |
| 8  | GND             | This is the ground pin.   |
| 11                                       | SD              | This is the serial data output pin. If a series of pulses is input to the ACK pin while the ESt pin is HIGH, the SD output pin outputs a 4-bit binary code corresponding to the DTMF signal shown in Table 1.   |
| 13                                       | ACK             | This is the acknowledgement pulse input pin. It is equipped with hysteresis. After the ESt pin goes HIGH, the four consecutive pulses input to the ACK pin cause the 4-bit data corresponding to the DTMF signal of the SD pin output to be output. The rising edge of the first pulse is latched before the data is shifted. |
| 14                                       | ESt             | This is the steering signal output pin. When there is a valid DTMF signal, this pin goes HIGH.  |
| 17                                       | V <sub>DD</sub> | This is the power supply pin.   |
| 1, 3, 4, 5, 7<br>9, 10, 12<br>15, 16, 18 | N.C.            | This is the N.C. pin. It is not connected inside the IC.  |

## ● Input / output circuits

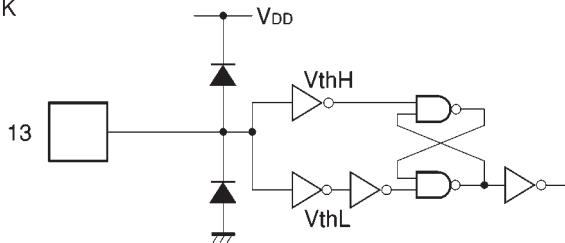
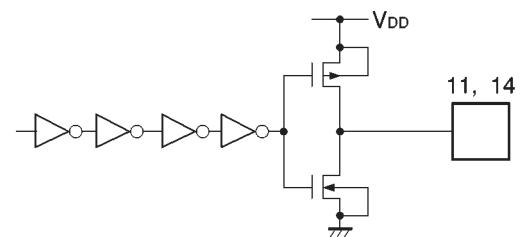
## INPUT



## OSC



## ACK

SD  
EST

## ●Electrical characteristics

DC characteristics (unless otherwise noted,  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=5.0\text{V}$ )

| Parameter                            | Symbol   | Min.         | Typ. | Max.     | Unit             | Conditions                                  | Measurement circuit |
|--------------------------------------|----------|--------------|------|----------|------------------|---|---------------------|
| Supply current                       | $I_{DD}$ | 1.0          | 2.2  | 3.4      | mA               |   | Fig.1               |
| Input high level voltage             | $V_{IH}$ | $V_{DD}-0.8$ | —    | $V_{DD}$ | V                | ACK pin                                     | Fig.1               |
| Input low level voltage              | $V_{IL}$ | GND          | —    | GND+0.8  | V                | ACK pin                                     | Fig.1               |
| Input high level current             | $I_{IH}$ | —            | 0.1  | 1.0      | $\mu\text{A}$    | ACK pin                                     | Fig.1               |
| Input low level current              | $I_{IL}$ | —            | 0.1  | 1.0      | $\mu\text{A}$    | ACK pin                                     | Fig.1               |
| Pin 1 input impedance                | $Z_{IN}$ | 10           | 30   | 50       | $\text{k}\Omega$ | $v_{in}=0\text{dBm}$ , $f_{in}=1\text{kHz}$ | Fig.1               |
| Output saturation high level voltage | $V_{OH}$ | 4.6          | —    | —        | V                | $I_{OH}=0.4\text{mA}^*2$                    | Fig.1               |
| Output saturation low level voltage  | $V_{OL}$ | —            | —    | 0.4      | V                | $I_{OL}=1\text{mA}^*2$                      | Fig.1               |

AC characteristics (unless otherwise noted,  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=5.0\text{V}$ )

| Parameter                      | Symbol          | Min.                       | Typ. | Max.    | Unit | Conditions       | $v_{in}$ (dBm) | Measurement circuit |
|--------------------------------|-----------------|----------------------------|------|---------|------|------------------|----------------|---------------------|
| Valid input level range        | $V_{IV}$        | -42                        | —    | 3       | dBm  | *3, 4, 5         | —              | Fig. 2              |
| Dual tone level difference     | Positive $VTWP$ | —                          | —    | 6       | dB   | *4               | -15            | Fig. 2              |
|                                | Negative $VTWN$ | —                          | —    | 6       | dB   | *4               | -15            | Fig. 2              |
| Frequency detection range      | $BWA$           | $\pm 1.5\% \pm 2\text{Hz}$ | —    | —       | —    | *5               | -27            | Fig. 2              |
| Frequency rejection range      | $BWR$           | —                          | —    | $\pm 4$ | %    | *5               | -27            | Fig. 2              |
| 3rd tone tolerance             | $TTT$           | —                          | —    | -16     | dB   | *5, 6            | -27            | Fig. 2              |
| Noise tolerance                | $TN$            | —                          | -12  | —       | dB   |                  | -27            | Fig. 2              |
| Dial tone tolerance            | $TDT$           | —                          | 14   | 7       | dB   | *7               | -27            | Fig. 2              |
| Signal presence detection time | $tDP$           | 5                          | 12   | 20      | ms   |                  | -27            | Fig. 2              |
| Signal absence detection time  | $tDA$           | 0.5                        | 5    | 15      | ms   |                  | -27            | Fig. 2              |
| Data shift rate                | $fDS$           | —                          | —    | 1       | MHz  | ACK Duty 40%~60% | —              | Fig. 2              |
| Output delay time              | $tPAD$          | —                          | 70   | 150     | ns   | ACK→SD           | —              | Fig. 2              |
| Setup time                     | $tDL$           | 0                          | —    | —       | ns   |                  | —              | Fig. 2              |
| Hold time                      | $tDH$           | 30                         | 60   | —       | ns   |                  | —              | Fig. 2              |

\*2 Applies to EST pin and SD pin.

\*3 A DTMF signal is input, and the voltage level of the single tone component is set as  $V_{IV}$ .\*4 Specified for a DTMF signal with a frequency deviation at the maximum standard frequency  $\pm 0.73\%$ .

\*5 No difference in level between the two tones.

\*6 Composite signal consisting of DTMF signals and the third harmonics of each input.

\*7 Specified for signals of 350 Hz and 440 Hz ( $\pm 2\%$ ).

© Not designed for radiation resistance.

## ● Measurement circuits

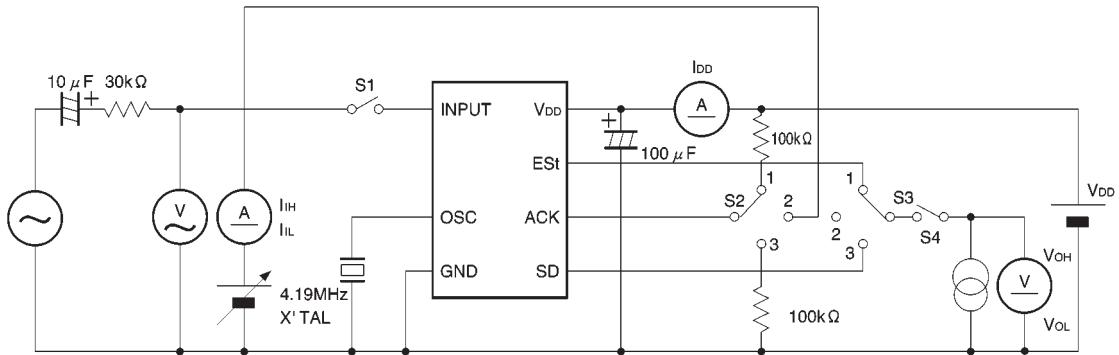


Fig. 1 DC characteristics measurement circuit

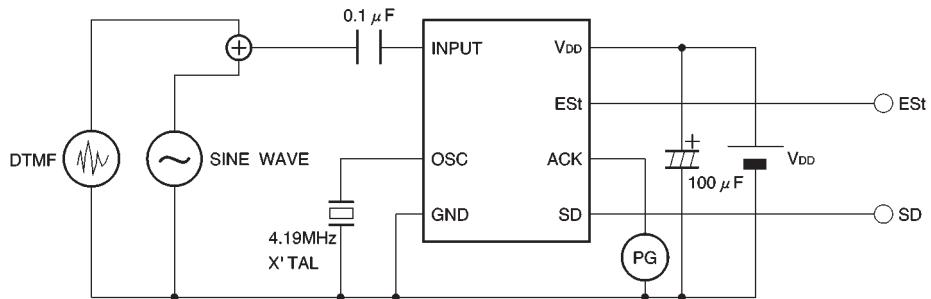


Fig. 2 AC characteristics measurement circuit

### ●Circuit operation

#### (1) An overview of operation

A DTMF signal is supplied to the INPUT pin and applied to a pair of 6th-order bandpass filters, which separate the DTMF signal into its high (COL) and low (ROW) frequencies. The separated tones are converted into square waves and fed to a digital detector. (See the block diagram.)

The digital detector checks the two tones to see if they are within the valid DTMF frequency bands. If they are, it sends a DETECT signal to the steering circuit, and sends the appropriate column and row address signals to a code converter.

The code converter encodes the received and detected DTMF signal, and outputs an ENABLE signal to the steering circuit.

Based on the DETECT and ENABLE signals, the steering circuit outputs an Early Steering (ESt) signal, which sets the ESt pin to HIGH, indicating that a valid DTMF signal has been detected.

If a series of pulses is input at the ACK pin while ESt is HIGH, a decoded DTMF signal is output to the SD pin as a binary code. (See Figure 3 for the overall timing.)

If a pulse sequence is input at the ACK pin, the data is latched at the rising edge of the first pulse by a parallel-serial converter, and at the same time, the LSB is output from the SD pin. Following this, three bits of data are output from the SD pin for each bit of each pulse in the pulse sequence input from the ACK pin. As a result, a total of four bits of data are output for the four pulses. (See Figure 4 for the ACK and SD timing.)

If the pulse sequence input to the ACK pin consists of three or fewer pulses, the next DTMF input cannot be decoded properly. Any ACK pulses in excess of four are ignored until ESt goes HIGH again.

Table 1 shows the format of serial data output from the SD pin.

#### (2) Overall timing chart

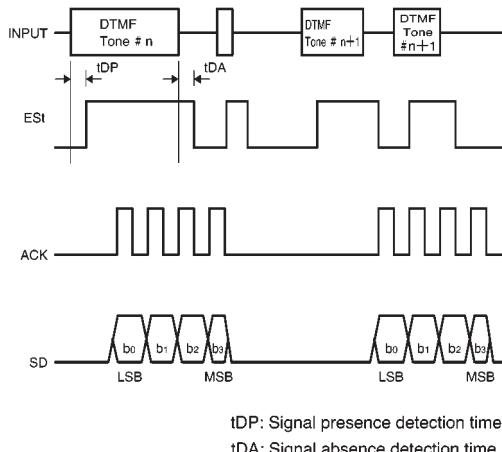


Fig. 3

#### (3) ACK and SD timing

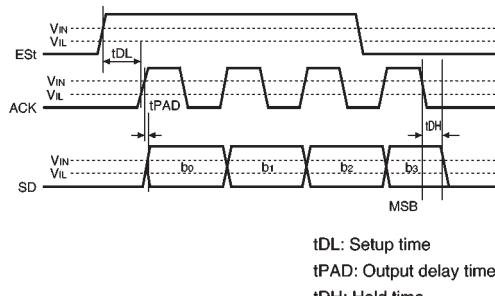


Fig. 4

## ●Circuit operation

## (4) Serial data correspondence table

Table 1. Serial data correspondence table

| ROW<br>[Hz] | COL<br>[Hz] | No. | b <sub>3</sub><br>(MSB) | b <sub>2</sub> | b <sub>1</sub> | b <sub>0</sub><br>(LSB) |
|-------------|-------------|-----|-------------------------|----------------|----------------|-------------------------|
| 697         | 1209        | 1   | 0                       | 0              | 0              | 1                       |
| 697         | 1336        | 2   | 0                       | 0              | 1              | 0                       |
| 697         | 1477        | 3   | 0                       | 0              | 1              | 1                       |
| 770         | 1209        | 4   | 0                       | 1              | 0              | 0                       |
| 770         | 1336        | 5   | 0                       | 1              | 0              | 1                       |
| 770         | 1477        | 6   | 0                       | 1              | 1              | 0                       |
| 852         | 1209        | 7   | 0                       | 1              | 1              | 1                       |
| 852         | 1336        | 8   | 1                       | 0              | 0              | 0                       |
| 852         | 1477        | 9   | 1                       | 0              | 0              | 1                       |
| 941         | 1336        | 0   | 1                       | 0              | 1              | 0                       |
| 941         | 1209        | *   | 1                       | 0              | 1              | 1                       |
| 941         | 1477        | #   | 1                       | 1              | 0              | 0                       |
| 697         | 1633        | A   | 1                       | 1              | 0              | 1                       |
| 770         | 1633        | B   | 1                       | 1              | 1              | 0                       |
| 852         | 1633        | C   | 1                       | 1              | 1              | 1                       |
| 941         | 1633        | D   | 0                       | 0              | 0              | 0                       |

0= "L" level, 1= "H" level

## ●Application example

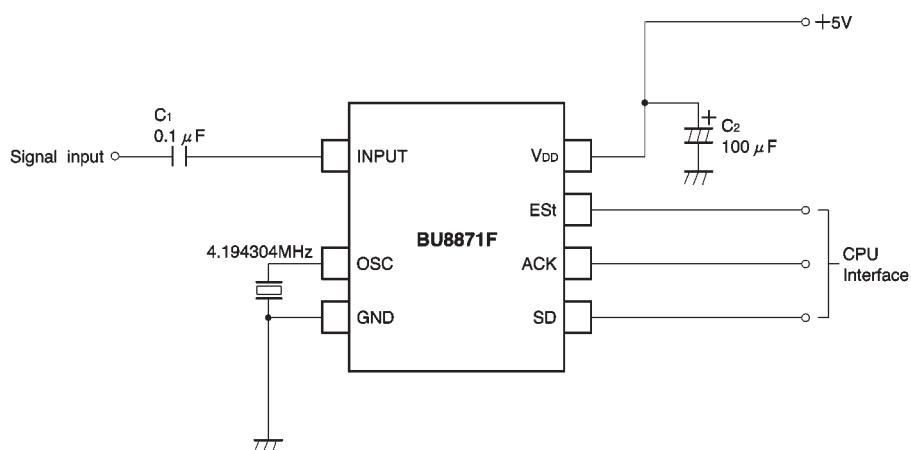


Fig. 5

- Selecting attached components
- (1) Power supply components

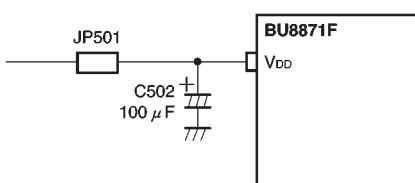


Fig. 6 Power supply circuit

- (2) Oscillation components

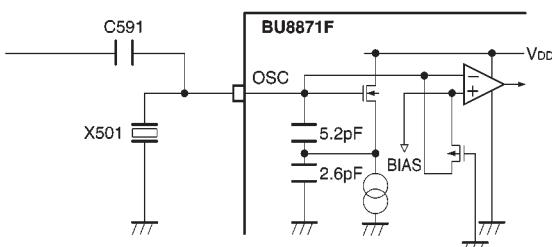


Fig. 7 Oscillation circuit

- (3) DTMF input

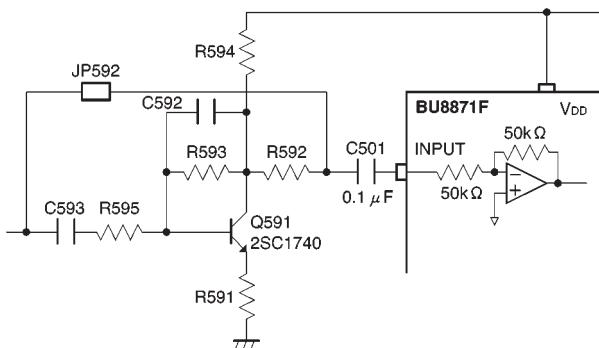


Fig. 8 DTMF input circuit

C501 : This is the DC blocking capacitor. Select a capacitor that will pass DTMF signals (greater than 697Hz) without significantly attenuating the signals.

C502 : This is the V<sub>DD</sub> bypass capacitor, and is normally 100μF. The maximum recommended operating power supply voltage is 5.25V, so a voltage withstand value of 6.3V is sufficient.

JP501 : This is normally shorted. To test the current consumption of the IC, insert a DC ammeter in place of JP501.

X501 : Use a crystal or ceramic resonator with an oscillation frequency of 4.194304MHz. If using a ceramic resonator, there may be problems with the precision of the oscillation frequency, so please consult the manufacturer of the resonator to make sure problems will not occur.

C591 : If you are using the X501 dedicated resonator designed for DTMF receivers, capacitor C591 should be left open. If you are injecting an external clock, X501 should be omitted and DC blocking capacitor C591 used in its place. Typically, this capacitor should be 47nF.

JP592 : If DTMF signals are being input directly, both ends should be shorted.

Q591  
R591 ~ R595  
C592, C593

Use these to increase the sensitivity of the DTMF receiver.

## (4) ESt output

The ESt guard time is determined by the CPU of the host computer, but to reduce the load on the host computer, the guard time can be set using an external circuit, as shown below.

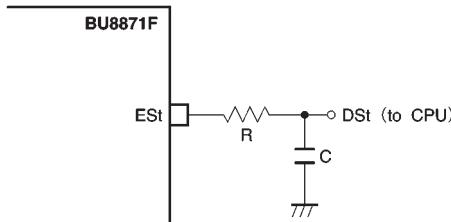


Fig. 9 Guard time setting circuit

The relation between a momentary falter in the ESt guard time ( $t_{GL}$ ), a momentary HIGH level in the ESt guard time ( $t_{GH}$ ), and the time constant is shown below. Figure 10 shows a timing diagram for guard times.

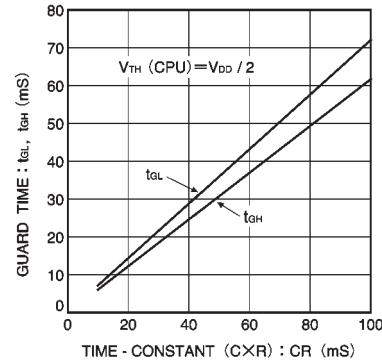
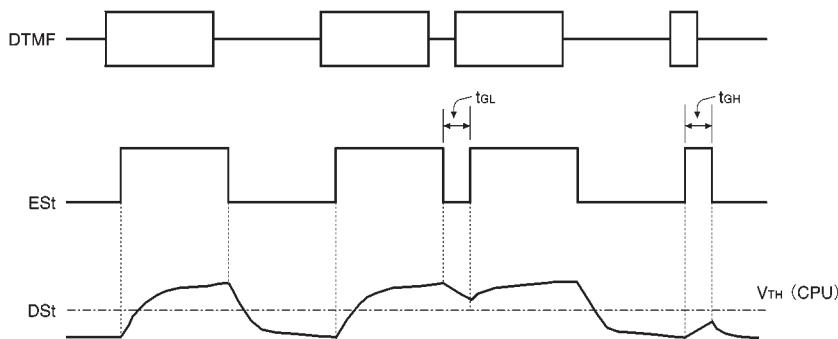
Fig. 10 Guard time vs. time constant ( $C \times R$ )

Fig. 11 Timing indicating guard times

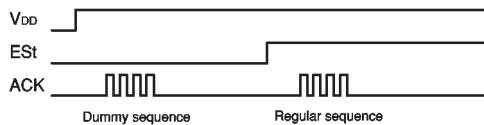
## ● Operation notes

## • Oscillation

Oscillation frequency precision can be a problem with ceramic resonators. Before including a ceramic resonator in your design, please consult the resonator manufacturer to make sure this will not be a problem.

Also, if an external clock is being injected, a DC blocking capacitor must be inserted. Select a capacitor that will neither attenuate the frequency components or put an excessive load on the drive side.

This LSI is not equipped with the power-on reset function. Also, since the internal circuit (flip-flop circuit) becomes unstable at the rising edge of the power supply, the internal circuit is initialized as shown below by the first DTMF sequence received after the rising edge of the power supply. Therefore, input four dummy ACK pulses before the DTMF reception.



### ● Electrical characteristic curves

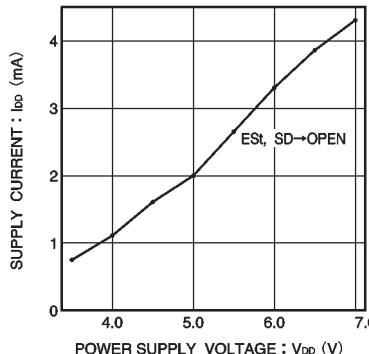


Fig. 12 Supply current vs. power supply voltage

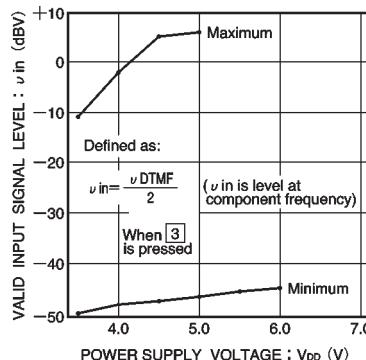


Fig. 13 Valid input level range vs. power supply voltage

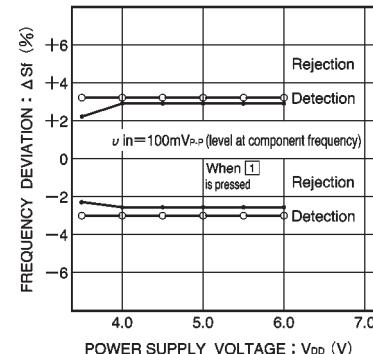


Fig. 14 Frequency detection/rejection ranges vs. power supply voltage

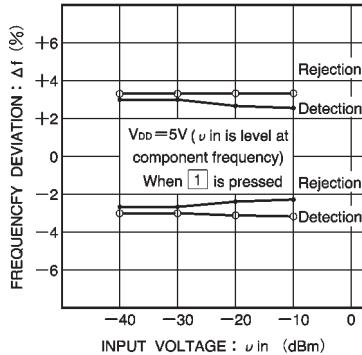


Fig. 15 Frequency detection/rejection ranges vs. input voltage

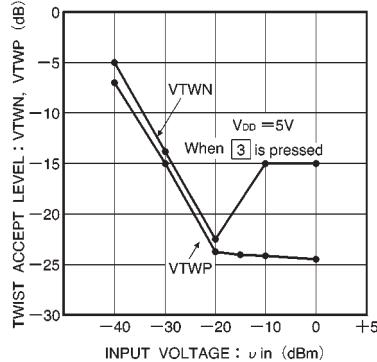


Fig. 16 2-frequency level vs. input voltage

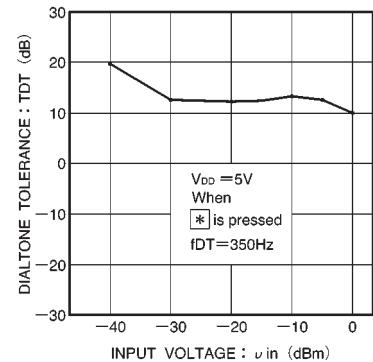


Fig. 17 Dial tone tolerance range vs. input voltage

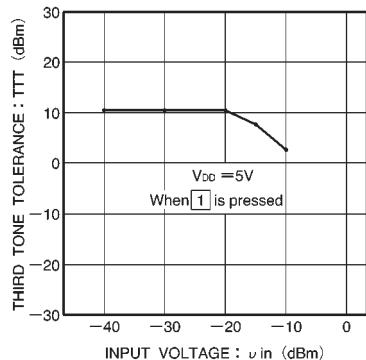


Fig. 18 Third tone tolerance range vs. input voltage

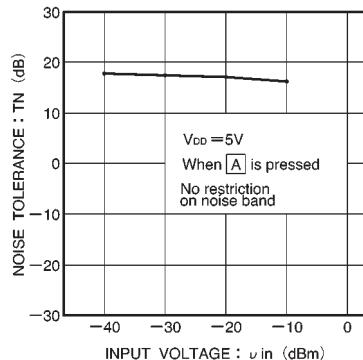
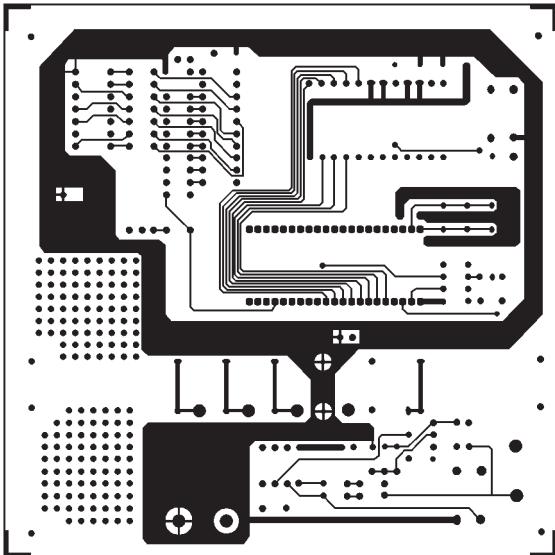


Fig. 19 Noise tolerance range vs. input voltage

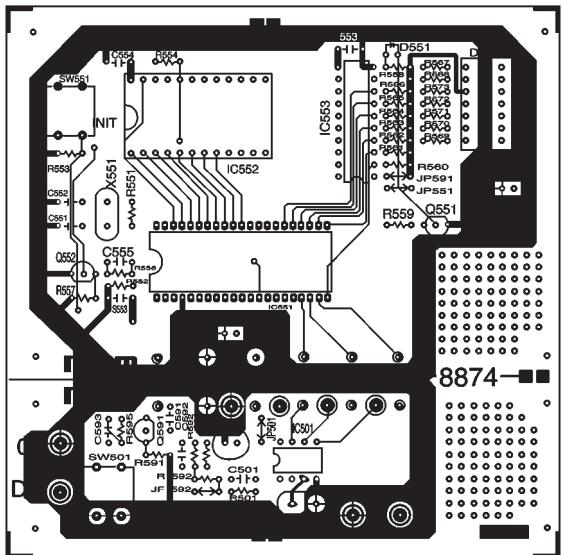
## ● Application board patterns

(1) Pattern (soldering surface)



The BU8874 application board (AB-8874) can be used.

## (2) Pattern (silk screening)



The BU8874 application board (AB-8874) can be used.

## ● External dimensions (Units: mm)

