

### Features

- Synchronous or Asynchronous Preset
- Cascadable in Synchronous or Ripple Mode
- Fanout (Over Temperature Range)
  - Standard Outputs ..... 10 LSTTL Loads
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_L \leq 1\mu A$  at  $V_{OL}, V_{OH}$

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC40103F3A	-55 to 125	16 Ld CERDIP
CD74HC40103E	-55 to 125	16 Ld PDIP
CD74HC40103M	-55 to 125	16 Ld SOIC
CD74HC40103MT	-55 to 125	16 Ld SOIC
CD74HC40103M96	-55 to 125	16 Ld SOIC
CD74HCT40103E	-55 to 125	16 Ld PDIP
CD74HCT40103M	-55 to 125	16 Ld SOIC
CD74HCT40103MT	-55 to 125	16 Ld SOIC
CD74HCT40103M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Description

The 'HC40103 and CD74HCT40103 are manufactured with high speed silicon gate technology and consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The 40103 contains a single 8-bit binary counter. Each has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the  $\overline{TC}$  output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK (CP). Counting is inhibited when the  $\overline{TE}$  input is high. The  $\overline{TC}$  output goes low when the count reaches zero if the  $\overline{TE}$  input is low, and remains low for one full clock period.

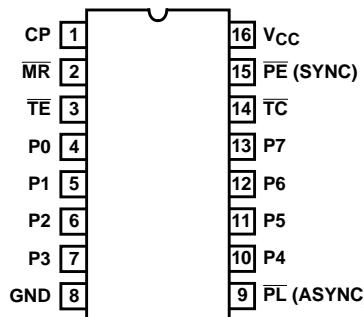
When the  $\overline{PE}$  input is low, data at the P0-P7 inputs are clocked into the counter on the next positive clock transition regardless of the state of the  $\overline{TE}$  input. When the  $\overline{PL}$  input is low, data at the P0-P7 inputs are asynchronously forced into the counter regardless of the state of the  $\overline{PE}$ ,  $\overline{TE}$ , or CLOCK inputs. Input P0-P7 represent a single 8-bit binary word for the 40103. When the MR input is low, the counter is asynchronously cleared to its maximum count of 255<sub>10</sub>, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except  $\overline{TE}$  are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100<sub>16</sub> or 256<sub>10</sub> clock pulses long.

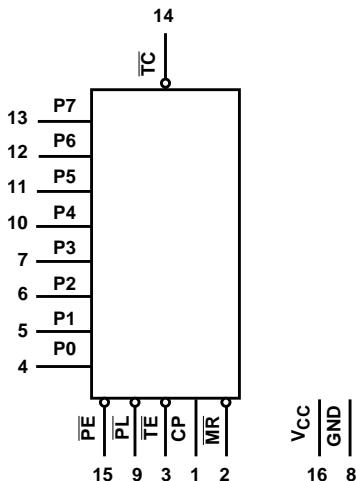
The 40103 may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output, in either a synchronous or ripple mode. These circuits possess the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits and can drive up to 10 LSTTL loads.

**Pinout**

**CD54HC40103  
(CERDIP)  
CD74HC40103, CD74HCT40103  
(PDIP, SOIC)  
TOP VIEW**



**Functional Diagram**



**TRUTH TABLE**

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset On Next Positive Clock Transition
1	0	X	X	Asynchronously	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

1 = High Level.

0 = Low Level.

X = Don't Care.

Clock connected to clock input.

Synchronous Operation: changes occur on negative-to-positive clock transitions.

Load Inputs: MSB = P7, LSB = P0.

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$	.....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$ For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	.....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$ For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	.....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$ For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	.....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$	.....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

### Operating Conditions

Temperature Range, $T_A$	.....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$		
HC Types	.....	2V to 6V
HCT Types	.....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$	.....	0V to $V_{CC}$
Input Rise and Fall Time		
2V	.....	1000ns (Max)
4.5V	.....	500ns (Max)
6V	.....	400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

1. The package thermal impedance is calculated in accordance with JESD 51-7.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS		
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
<b>HC TYPES</b>														
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V		
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V		
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V		
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V		
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V		
			4	4.5	-	-	0.26	-	0.33	-	0.4	V		
			5.2	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$		
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$		

# CD54HC40103, CD74HC40103, CD74HCT40103

## DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

INPUT	UNIT LOADS (NOTE)
P0-P7	0.20
TE, MR	0.40
CP	0.60
PE	0.80
PL	1.35

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

## Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
CP Pulse Width	t <sub>W</sub>	2	165	-	-	205	-	250	-	ns
		4.5	33	-	-	41	-	50	-	ns
		6	28	-	-	35	-	43	-	ns
PL Pulse Width	t <sub>W</sub>	2	125	-	-	155	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns

# CD54HC40103, CD74HC40103, CD74HCT40103

## Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR Pulse Width	t <sub>W</sub>	2	125	-	-	135	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns
CP Max. Frequency (Note 3)	f <sub>CP(MAX)</sub>	2	3	-	-	2	-	2	-	MHz
		4.5	15	-	-	12	-	10	-	MHz
		6	18	-	-	14	-	12	-	MHz
P to CP Set-up Time	t <sub>SU</sub>	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
P̄E to CP Set-up Time	t <sub>SU</sub>	2	75	-	-	95	-	110	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	13	-	-	16	-	19	-	ns
T̄E to CP Set-up Time	t <sub>SU</sub>	2	150	-	-	190	-	225	-	ns
		4.5	30	-	-	38	-	45	-	ns
		6	26	-	-	33	-	38	-	ns
P to CP Hold Time	t <sub>H</sub>	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
T̄E to CP̄ Hold Time	t <sub>H</sub>	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
MR to CP Removal Time	t <sub>REM</sub>	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
P̄E to CP̄ Hold Time	t <sub>H</sub>	2	2	-	-	2	-	2	-	ns
		4.5	2	-	-	2	-	2	-	ns
		6	2	-	-	2	-	2	-	ns
<b>HCT TYPES</b>										
CP Pulse Width	t <sub>W</sub>	4.5	35	-	-	44	-	53	-	ns
PL Pulse Width	t <sub>W</sub>	4.5	43	-	-	54	-	65	-	ns
MR Pulse Width	t <sub>W</sub>	4.5	35	-	-	44	-	53	-	ns
CP Max. Frequency (Note 3)	f <sub>CP(MAX)</sub>	4.5	14	-	-	11	-	9	-	MHz
P to CP Set-up Time	t <sub>SU</sub>	4.5	24	-	-	30	-	36	-	ns
P̄E to CP Set-up Time	t <sub>SU</sub>	4.5	20	-	-	25	-	30	-	ns
T̄E to CP Set-up Time	t <sub>SU</sub>	4.5	40	-	-	50	-	60	-	ns
P to CP Hold Time	t <sub>H</sub>	4.5	5	-	-	5	-	5	-	ns
T̄E to CP Hold Time	t <sub>H</sub>	4.5	0	-	-	0	-	0	-	ns
MR to CP̄ Removal Time	t <sub>REM</sub>	4.5	10	-	-	13	-	15	-	ns
P̄E to CP Hold Time	t <sub>H</sub>	4.5	2	-	-	2	-	2	-	ns

# CD54HC40103, CD74HC40103, CD74HCT40103

## Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay CP to any $\overline{\text{TC}}$ (Async Preset)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	300	-	375	-	450	ns
		C <sub>L</sub> = 50pF	4.5	-	-	60	-	75	-	90	ns
		C <sub>L</sub> = 15pF	5	-	25	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	51	-	64	-	77	ns
CP to $\overline{\text{TC}}$ (Sync Preset)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	300	-	375	-	450	ns
		C <sub>L</sub> = 50pF	4.5	-	-	60	-	75	-	90	ns
		C <sub>L</sub> = 15pF	5	-	25	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	51	-	64	-	77	ns
$\overline{\text{TE}}$ to $\overline{\text{TC}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	200	-	250	-	300	ns
		C <sub>L</sub> = 50pF	4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	5	-	17	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	34	-	43	-	51	ns
PL to $\overline{\text{TC}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	275	-	345	-	415	ns
		C <sub>L</sub> = 50pF	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	47	-	59	-	71	ns
MR to $\overline{\text{TC}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	275	-	345	-	415	ns
		C <sub>L</sub> = 50pF	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	47	-	59	-	71	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
		C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
		C <sub>L</sub> = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>I</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 15pF	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C <sub>PD</sub>	-	5	-	25	-	-	-	-	-	pF
<b>HCT TYPES</b>											
Propagation Delay CP to $\overline{\text{TC}}$ (Async Preset)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	60	-	75	-	90	ns
		C <sub>L</sub> = 15pF	5	-	25	-	-	-	-	-	ns
$\overline{\text{CE}}$ to $\overline{\text{TC}}$ (Sync Preset)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	63	-	79	-	95	ns
		C <sub>L</sub> = 15pF	5	-	26	-	-	-	-	-	ns
$\overline{\text{TE}}$ to $\overline{\text{TC}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	5	-	21	-	-	-	-	-	ns
PL to $\overline{\text{TC}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	68	-	85	-	102	ns
		C <sub>L</sub> = 15pF	5	-	28	-	-	-	-	-	ns

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR to $\overline{\text{TC}}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 15pF	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C <sub>PD</sub>	-	5	-	27	-	-	-	-	-	pF

NOTES:

3. Noncascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enables ( $\overline{\text{PE}}$  or  $\overline{\text{TE}}$ )-to-clock SET UP TIMES, and count enables ( $\overline{\text{PE}}$  or  $\overline{\text{TE}}$ )-to-clock HOLD TIMES determine maximum clock frequency. For example, with these HC devices:

$$C_P f_{MAX} = \frac{1}{\text{CP-to-}\overline{\text{TC}} \text{ prop delay} + \overline{\text{TE}}\text{-to-CP Setup Time} + \overline{\text{TE}}\text{-to-CP Hold Time}} = \frac{1}{60 + 30 + 0} \approx 11\text{MHz}$$

4. C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

5. P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub> where f<sub>i</sub> = Input Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage, f<sub>o</sub> = Output Frequency.

**Timing Diagrams**

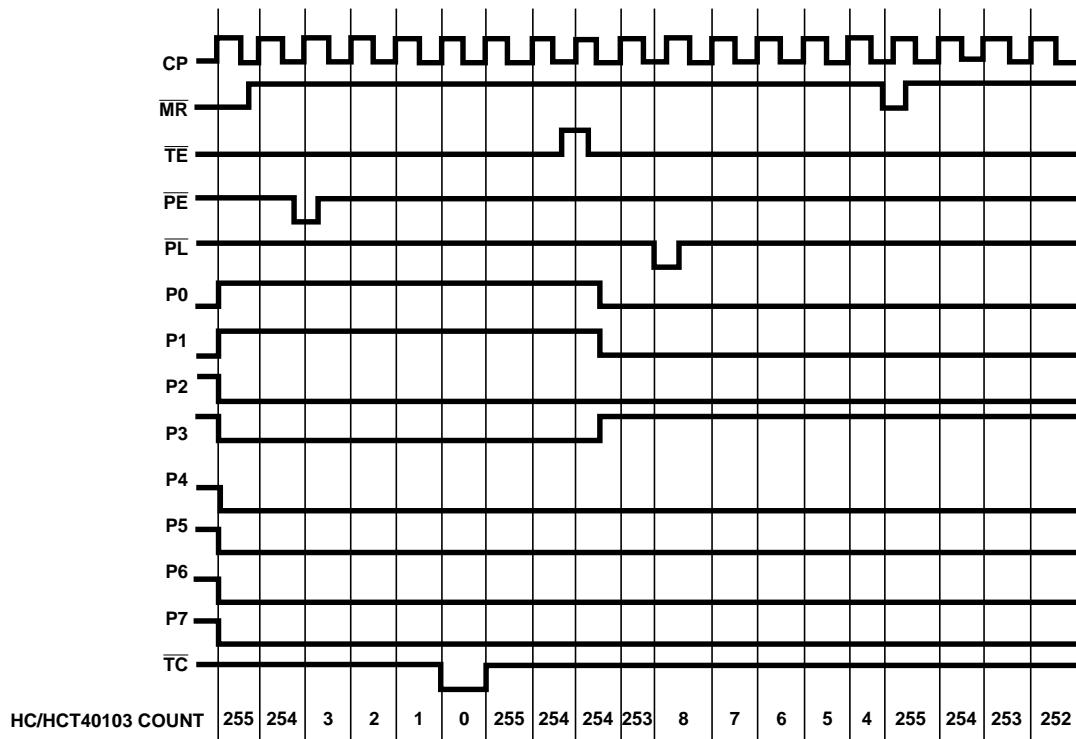


FIGURE 1.

### Test Circuits and Waveforms

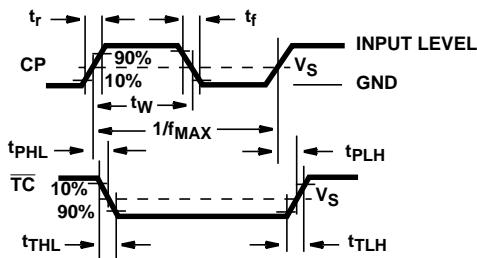


FIGURE 2.

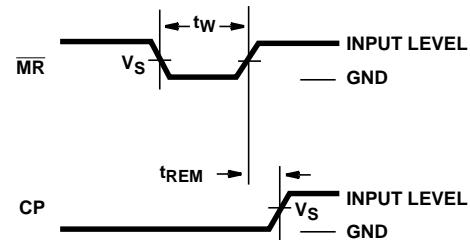


FIGURE 3.

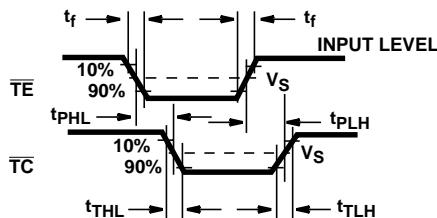


FIGURE 4.

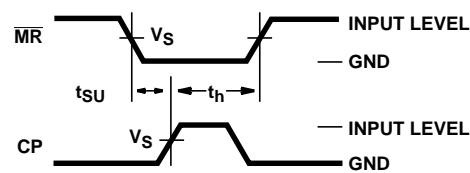


FIGURE 5.

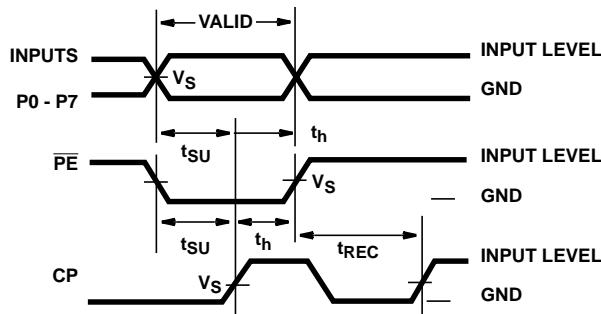


FIGURE 6.

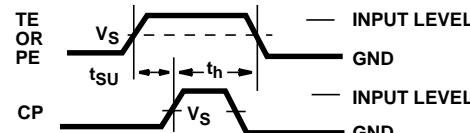
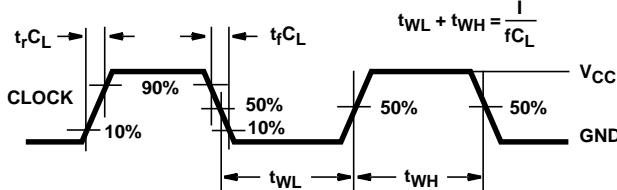
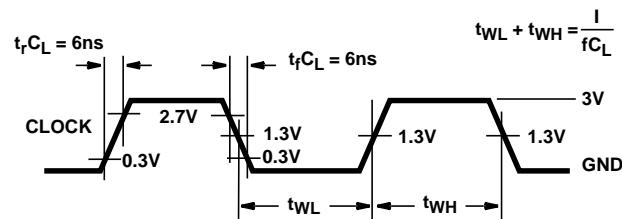


FIGURE 7.



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 8. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 9. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9055301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A	Samples
5HC40103F3AS228	OBsolete	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
CD54HC40103F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC40103F	Samples
CD54HC40103F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A	Samples
CD74HC40103E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC40103E	Samples
CD74HC40103EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC40103E	Samples
CD74HC40103M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HC40103MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M	Samples
CD74HCT40103E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT40103E	Samples
CD74HCT40103EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT40103E	Samples
CD74HCT40103M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	Samples
CD74HCT40103M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT40103M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	<a href="#">Samples</a>
CD74HCT40103MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	<a href="#">Samples</a>
CD74HCT40103MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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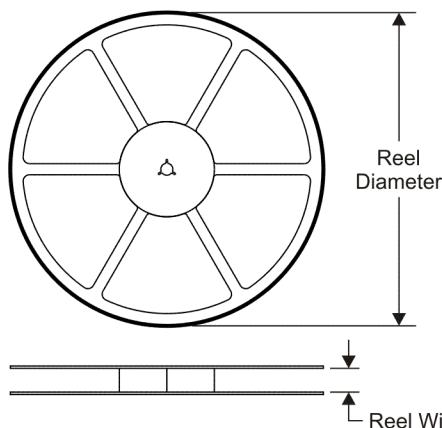
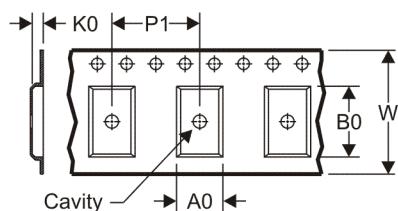
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC40103, CD74HC40103 :**

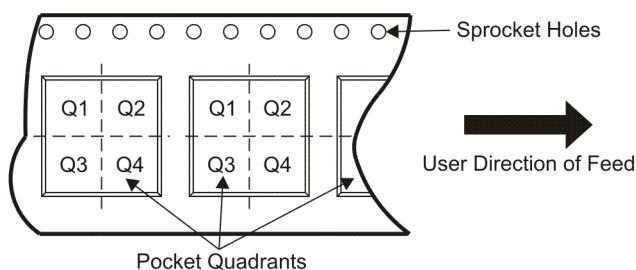
- Catalog: [CD74HC40103](#)
- Automotive: [CD74HC40103-Q1](#), [CD74HC40103-Q1](#)
- Enhanced Product: [CD74HC40103-EP](#), [CD74HC40103-EP](#)
- Military: [CD54HC40103](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


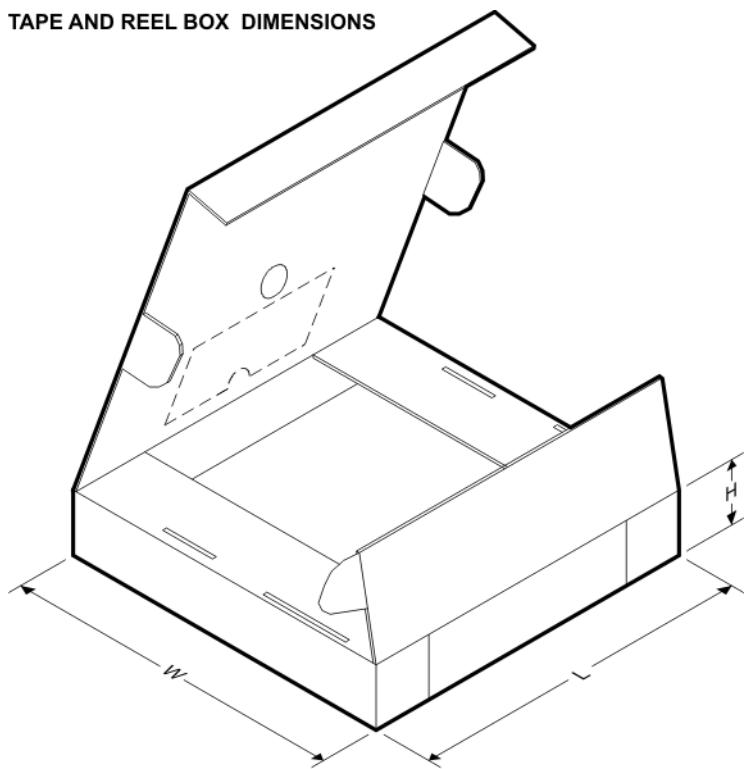
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40103M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT40103M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



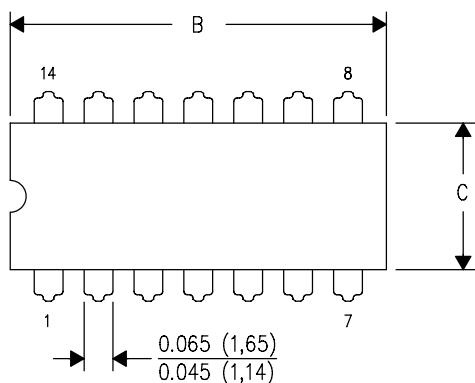
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC40103M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT40103M96	SOIC	D	16	2500	333.2	345.9	28.6

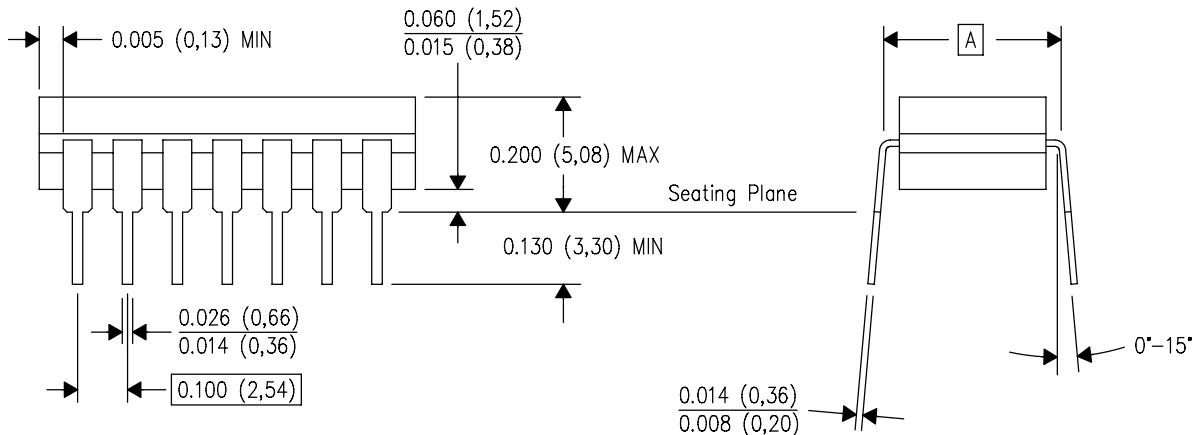
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



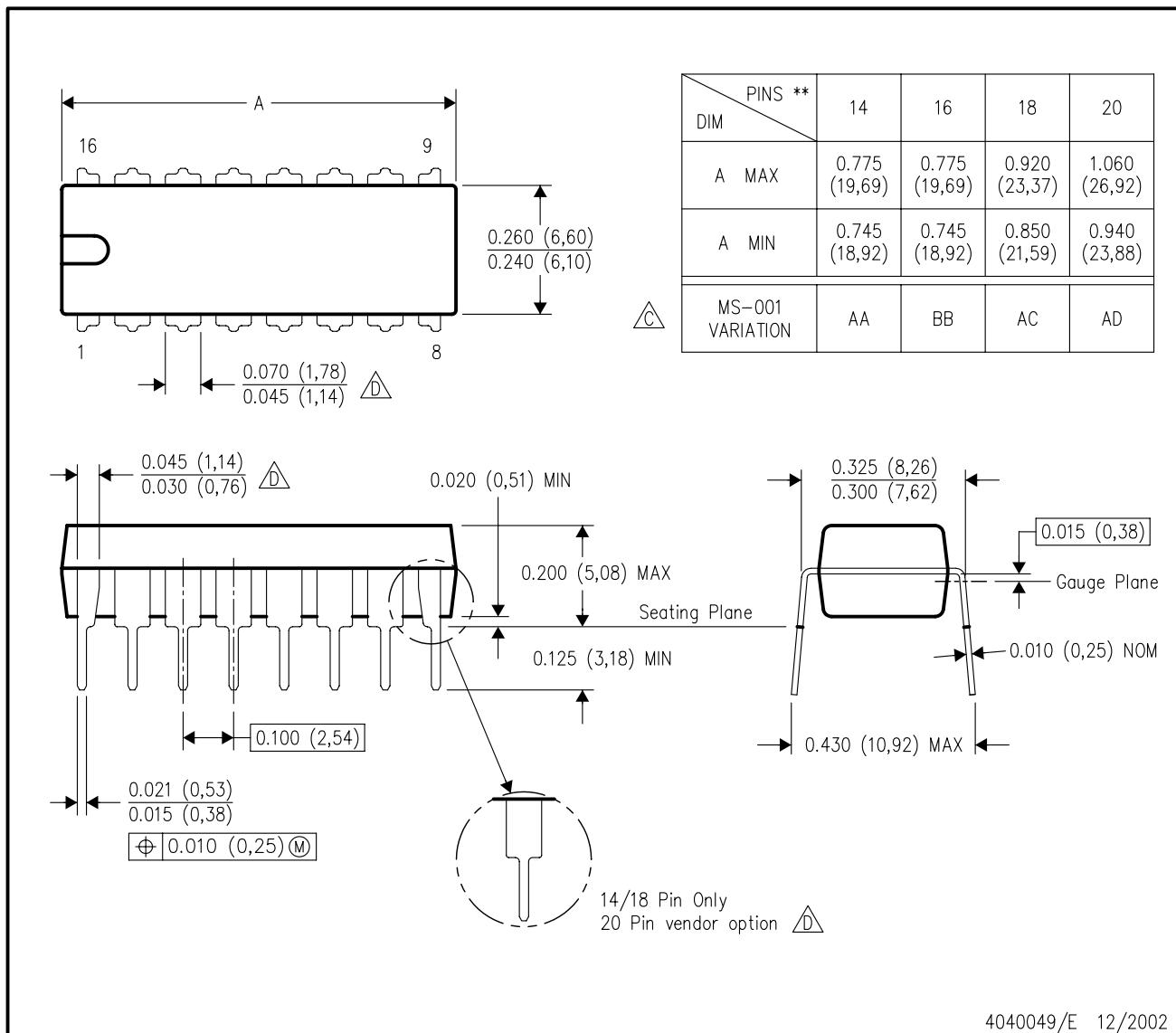
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

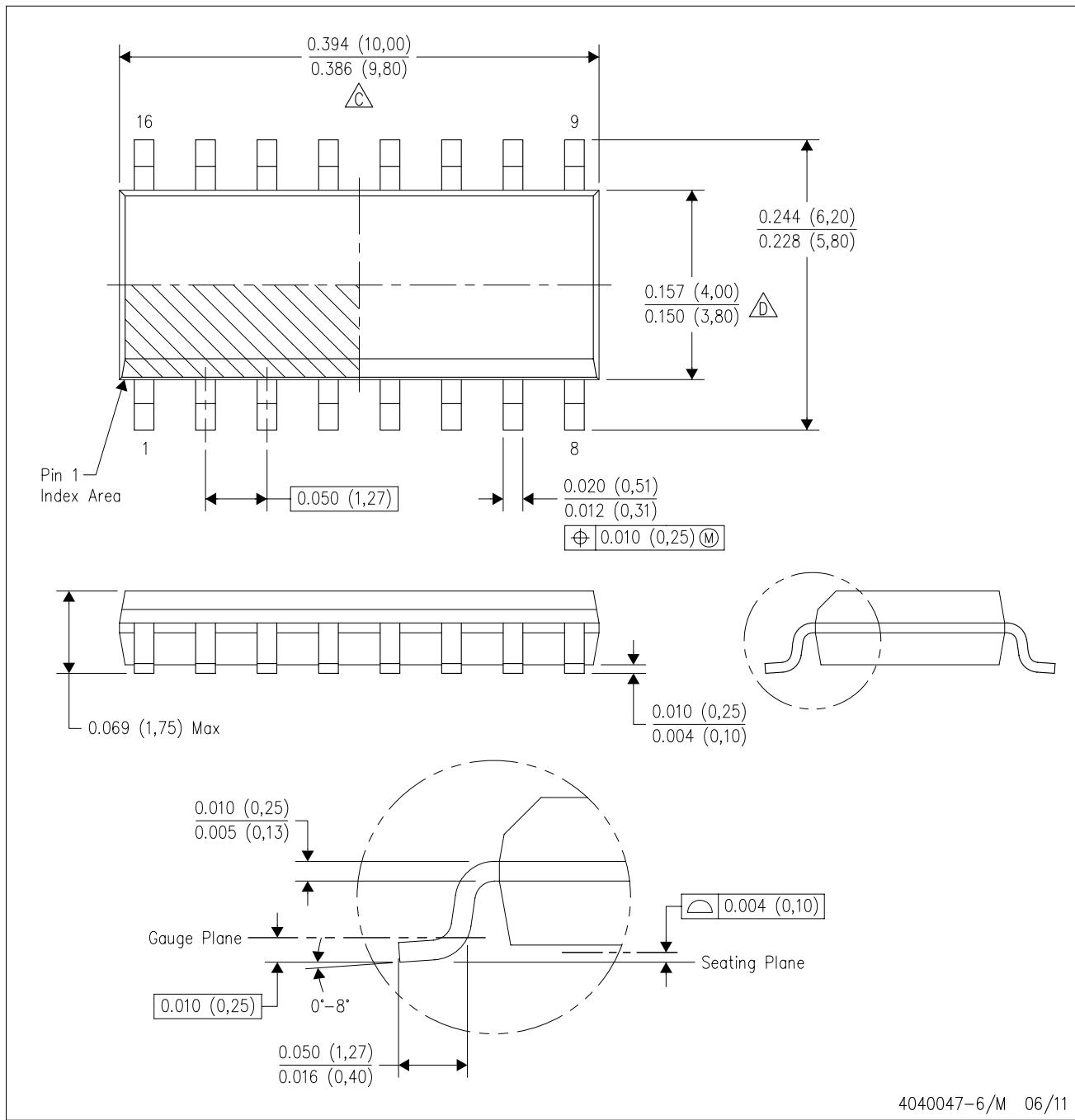
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

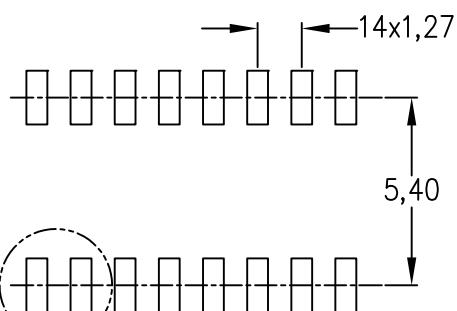
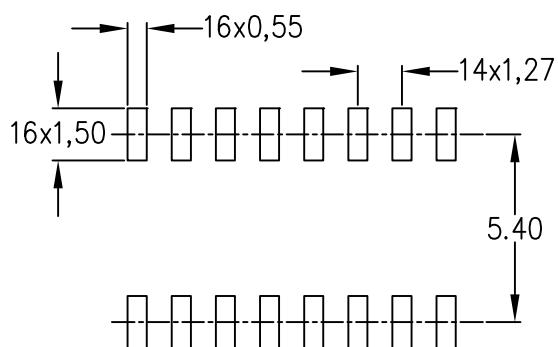
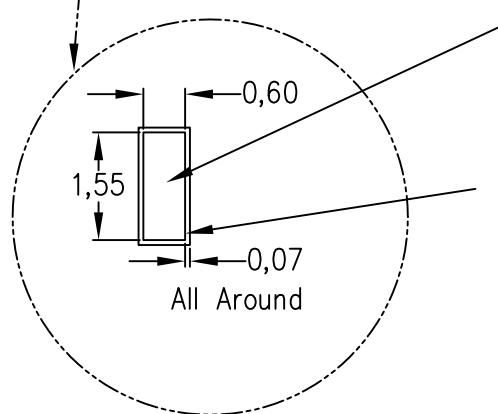
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>