# Single-phase full-wave motor driver for fan motor

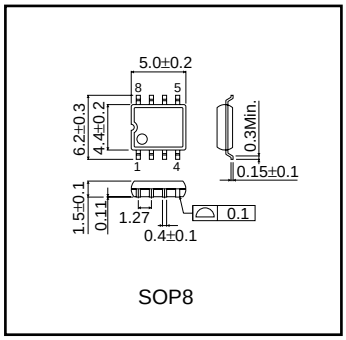
## BA6423AF

The BA6423AF is a single-phase full-wave motor driver for fan motor. Fan motor of single-phase full-wave motor driver can be composed of fewer components as compared with that composed of general-purpose components such as power operational amplifier. Lock detection, automatic reset function and lock alarm output necessary for fan motor are integrated.

### ●Features

1) Single-Phase Full-Wave drive system
2) Built-in power transistor
3) Lock detection, automatic restart circuit
4) Thermal shut-down circuit
5) Alarm signal output

### ●External dimensions (Unit : mm)




SOP8

### ●Applications

Single phase full-wave motor driver for fan motor

### ●Absolute maximum ratings (Ta=25°C)

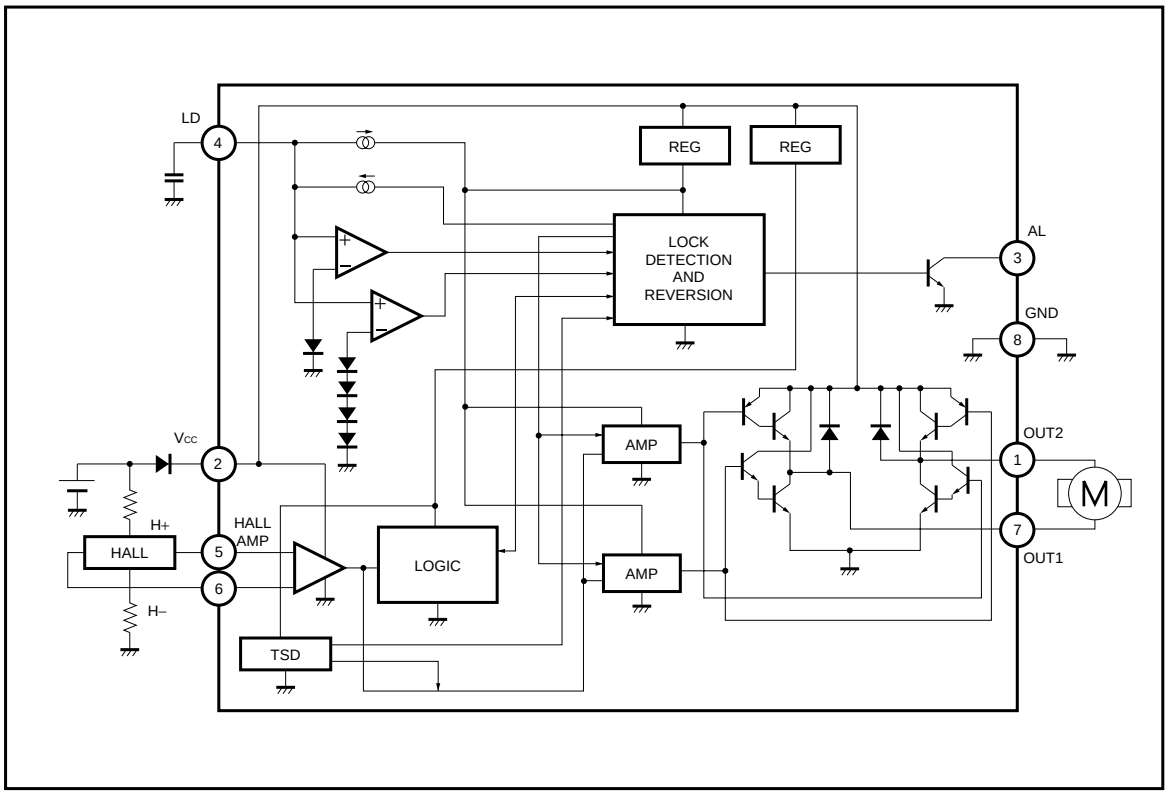
| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 30 | V |
| Power dissipation | Pd | 687 *1 | mW |
| Operating temperature | Topr | −25 to +75 | ˚C |
| Storage temperature | Tstg | −55 to +150 | ˚C |
| Output current | $I_{OUT}$ | 1.0 *2 | A |
| Output voltage | $V_{OUT}$ | 30 | V |
| Alarm signal output voltage | $V_{AL}$ | 30 | V |
| Junction temperature | Tjmax | 150 | ˚C |

*1 Reduce 5.5mW/˚C to use at temperature above Ta=25˚C.
(On 70.0mm × 70.0mm × 1.6mm glass epoxy board)
*2 This value is not to be over Pd and ASO.

### ●Recommended operating conditions (Ta=25°C)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 6 to 28 | V |

●**Block diagram**



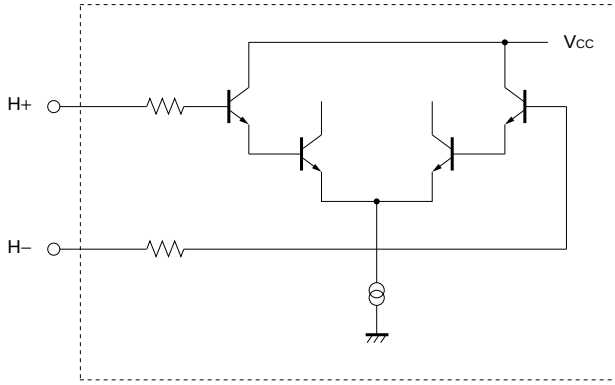

●**Terminal function table**

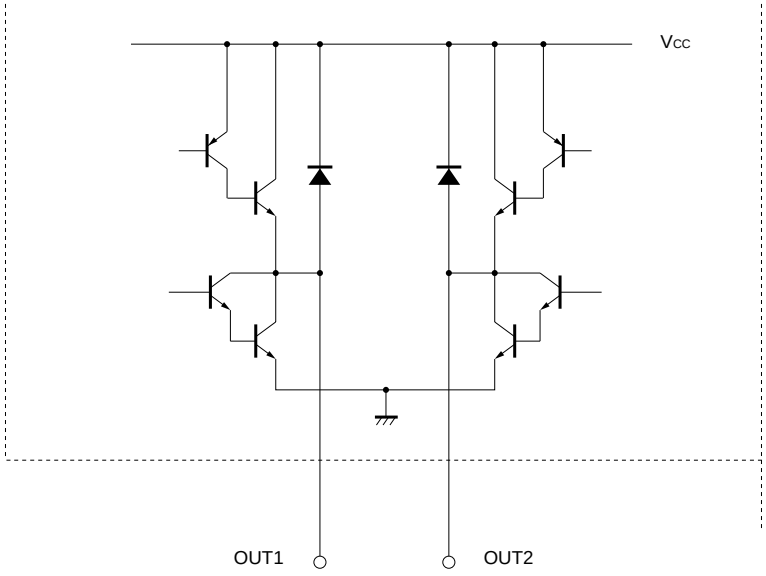
| Pin No. | Terminal name | Function |
|---|---|---|
| 1 | OUT2 | Output terminal 2 |
| 2 | $V_{CC}$ | Power supply terminal |
| 3 | AL | Alarm signal output terminal |
| 4 | LD | Connection terminal of capacitor for Lock detention, Auto restart |
| 5 | H+ | Hall signal input terminal + |
| 6 | H– | Hall signal input terminal – |
| 7 | OUT1 | Output terminal 1 |
| 8 | GND | Ground terminal |

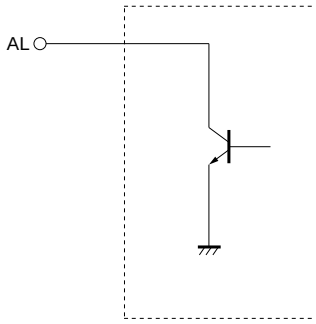
●**Hall signal input-output truth value table**

| H+ | H– | OUT1 | OUT2 |
|---|---|---|---|
| H | L | H | L |
| L | H | L | H |

●**Input-output circuit**



●**Electrical characteristics** (Unless otherwise specified, Ta=25°C, $V_{CC}$= 12V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | Test circuit |
|---|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$ | 2.7 | 5.4 | 8.1 | mA | At output : OFF | Fig.1 |
| Charge current of capacitor for lock detection | $I_{LDC}$ | 1.55 | 3.10 | 4.65 | μA | $V_{LD}$=1.8V | Fig.2 |
| Discharge current of capacitor for lock detection | $I_{LDD}$ | 0.33 | 0.66 | 0.99 | μA | $V_{LD}$=1.8V | Fig.2 |
| Charge-discharge current ratio of capacitor for lock detection | $r_{CD}$ | 3.0 | 4.7 | 6.4 | – | $r_{CD}=I_{LDC} / I_{LDD}$ | Fig.2 |
| Clamp voltage of capacitor for lock detection | $V_{LDCL}$ | 2.0 | 2.48 | 3.0 | V | | Fig.2 |
| Comparison voltage of capacitor for lock detection | $V_{LDCP}$ | 0.7 | 0.99 | 1.3 | V | | Fig.2 |
| Output voltage L | $V_{OL}$ | – | 0.8 | 1.2 | V | $I_O$=200mA | Fig.3 |
| Output voltage H | $V_{OH}$ | 10.6 | 11.1 | – | V | $I_O$=200mA | Fig.3 |
| "AL" terminal voltage L | $V_{ALL}$ | – | 0.1 | 0.3 | V | $I_{AL}$=10mA | Fig.4 |
| "AL" terminal leak current | $I_{ALL}$ | – | 0 | 10 | μA | $V_{AL}$=30V | Fig.4 |

◎ This product is not designed for protection against radioactive rays.

●**Test circuit**

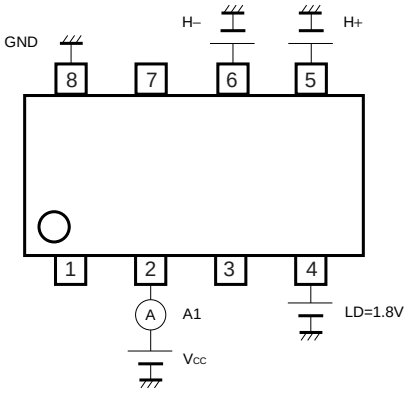



Fig.1

·$I_{CC}$ : Measure the value of A1 input condition
H+ : H (1 / 2$V_{CC}$ + 0.2V)
H– : L (1 / 2$V_{CC}$)

First, please input 3V at LD terminal and then 1.8V.

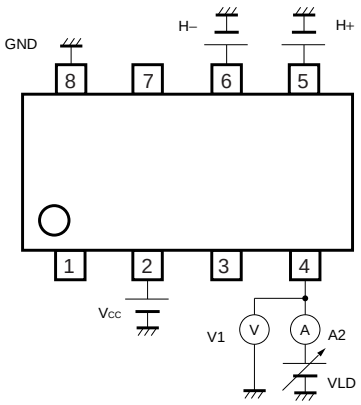
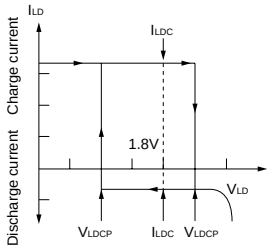



Fig.2

· $I_{LDC}$, $I_{LDD}$ : Measure the value of A2 ($V_{LD}$=1.8V)
· $V_{LDCL}$, $V_{LDCP}$ : Measure the value of V1
· $r_{CD}$ : $I_{LDC}$ / $I_{LDD}$

Input condition
H+ : H (1 / 2$V_{CC}$ + 0.2V)
H– : L (1 / 2$V_{CC}$)

Please input voltage at LD terminal according to the following diagram



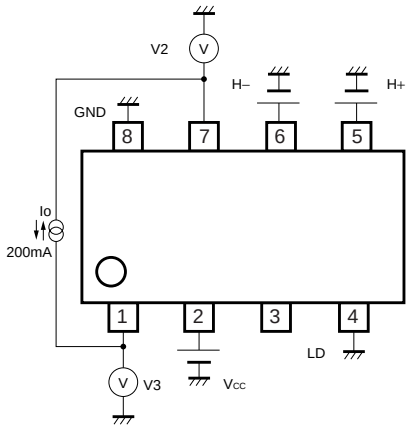




Fig.3

· $V_{OL}$, $V_{OH}$ : Measure the value of V2, V3

Io flows to output terminal that is "L" from output terminal that is "H".
Please be referred to Hall signal input-output truth value table about output mode.
Input "H" : 1 / 2$V_{CC}$ + 0.2V
Input "L" : 1 / 2$V_{CC}$

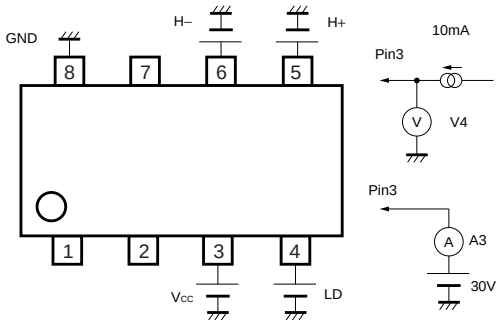



Fig.4

· VALL : Measure the value of V4
· IALL : Measure the value of A3

Please be referred to the following table about input condition.
Input "H" : 1 / 2$V_{CC}$ + 0.2V
Input "L" : 1 / 2$V_{CC}$

| Parameter | H+ | H– | LD |
|---|---|---|---|
| VALL | H | L | 0V |
| IALL | H | L | 3V |

**●Lock detect circuit and Automatic restart circuit**

Charge and discharge time at motor lock condition varies with the value of external capacitor at LD terminal and is given by the following equation.

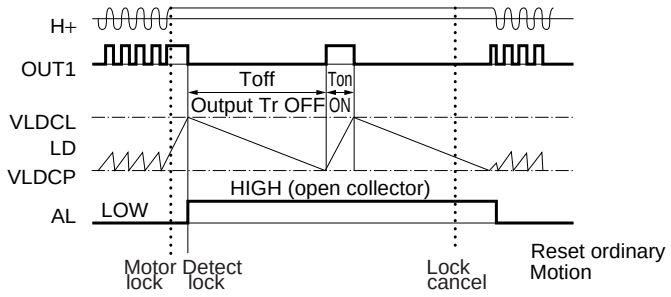
$$\text{Ton (Charge time)} = \frac{C \cdot (VLDCL - VLDCP)}{ILDC}$$

$$\text{Toff (Discharge time)} = \frac{C \cdot (VLDCL - VLDCP)}{ILDD}$$

C : Value of capacitor at LD terminal
$V_{LDCL}$ : Clamp voltage of capacitor lock detection (2.48V Typ.)
$V_{LDCP}$ : Comparison voltage of capacitor lock detection (0.99V Typ.)
$I_{LDC}$ : Charge current of capacitor lock detection (3.10μA Typ.)
$I_{LDD}$ : Discharge current of capacitor lock detection (0.66μA Typ.)

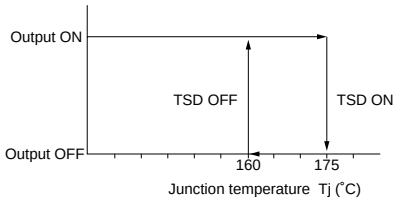
The following value shows charge time and discharge time at C=0.47μF for reference.
Charge time = 0.26SEC (Output : ON)
Discharge time = 1.06SEC (Output : OFF)

The following figure shows timing chart of LD terminal.



●**Cautions**

1) Thermal shut down(TSD)
This IC is built-in TSD.
TSD has the temperature hysteresis.




TSD ON (TYP. : 175˚C)
All output transistor OFF.
TSD OFF (TYP. : 160˚C)
Reset ordinary motion.
(It has the temperature hysteresis of 15˚C<TYP>)

Fig.5

2) Power dissipation
IC power dissipation widely varies with supply voltage, output current and application of IC. Please be careful for the thermal design not to exceed the allowable power dissipation.

3) Hall signal input terminals (H+, H–)

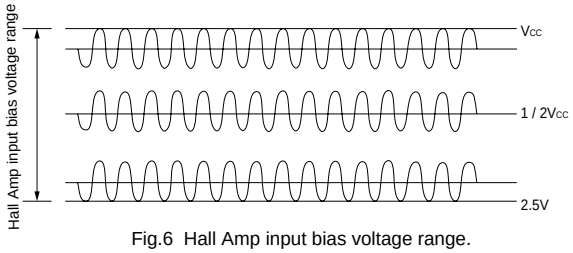



Fig.6 Hall Amp input bias voltage range.

A. Please adjust hall input bias voltage by value of resistor for hall element, so that hall signal contains amplitude input within rang from 2.5V to Vcc.
At this time, to set hall amp input bias voltage for Vcc/2 is recommended.
B. Please be careful of input signal, because hall amp of this I C doesn't have input hysteresis.

4) ASO
Please consider output transistors not to exceed absolute maximum ratings and ASO.

5) GND
Please keep up the voltage of GND less than the voltage of another terminal surely.

6) This product is produced with strict quality control, but destroyed in using beyond absolute maximum ratings. Once IC destroyed, a failure mode cannot be defined(like short-mode or open-mode). Therefore, physical security counter measure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

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