

## 100 MHz Differential Buffer for PCI Express and SATA

### Features

- Two differential 0.7V clock output pairs
- OE# input for enabling SRC outputs
- Individual OE controls
- Low CTC jitter (< 50 ps)
- Spread Aware
- 3.3V operation
- Industrial Temperature Grade -40°C to +85°C
- 16-pin TSSOP package

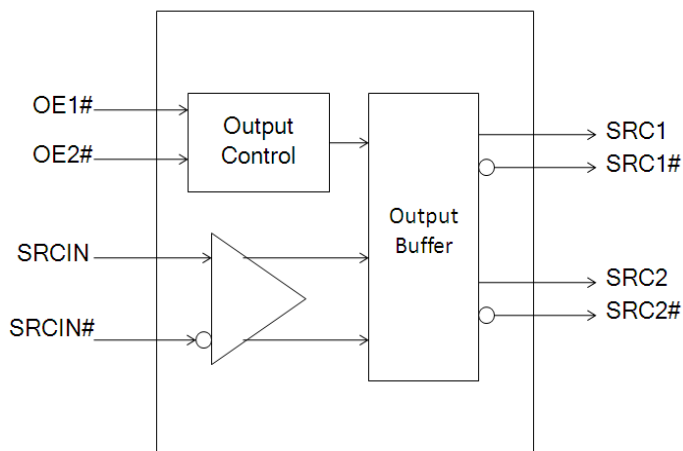
### Functional Description

The SL28DB200 is a differential buffer capable of distributing the Serial Reference Clock (SRC) for PCI Express Gen2 and SATA implementations. The buffer enables the application system to control the distribution of the SRC.

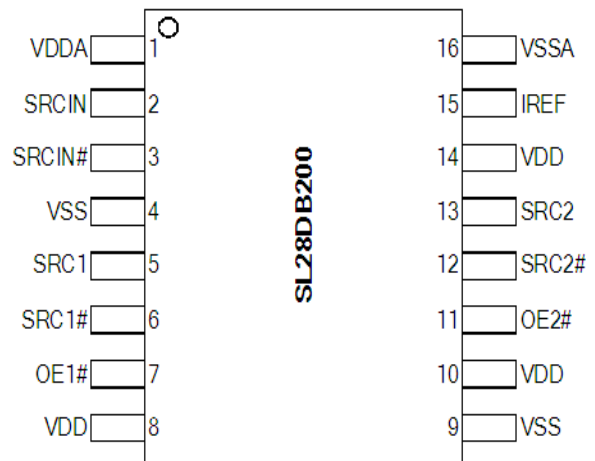
### Applications

- Network/Media Attached Storage
- Routers/IP Gateways
- Multi-function Printers

### Block Diagram



### Pin Configuration



16 TSSOP

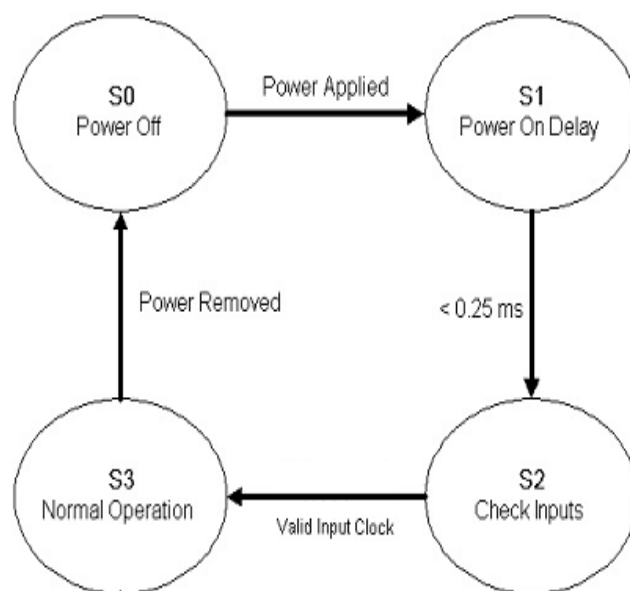
## Pin Description

| Pin       | Name                | Type  | Description                                                                                 |
|-----------|---------------------|-------|---------------------------------------------------------------------------------------------|
| 2,3       | SRCIN, SRCIN#       | I,DIF | 0.7V Differential inputs                                                                    |
| 5,6,13,12 | SRC[1:2], SRC[1:2]# | O,DIF | 0.7V Differential Clock Outputs                                                             |
| 7,11      | OE[1:2]#            | I,SE  | 3.3V LVTTTL input for enabling differential outputs                                         |
| 15        | IREF                | I     | A precision resistor 475 ohm is attached to this pin to set the differential output current |
| 1         | VDDA                | PWR   | 3.3V Power Supply                                                                           |
| 16        | VSSA                | GND   | Ground                                                                                      |
| 8,10,14   | VDD                 | PWR   | 3.3V power supply for outputs                                                               |
| 4,9       | VSS                 | GND   | Ground for outputs                                                                          |

Notes: I=Input, O=Output, DIF=Differential signal, SE=Single Ended, PWR=Power input, GND=Ground

**Table 1. Buffer Power-up State Machine**

| State | Description                                                                                                            |
|-------|------------------------------------------------------------------------------------------------------------------------|
| S0    | 3.3V Buffer power off                                                                                                  |
| S1    | After 3.3V supply is detected to rise above 1.8V - 2.0V, the buffer enters state 1 and initiates a 0.2-ms–0.3-ms delay |
| S2    | Buffer waits for a valid clock on the SRCIN input                                                                      |
| S3    | Once a valid input is detected, the buffer enters state 3 and enables outputs for normal operation                     |



**Figure 1. Buffer Power-up State Diagram**

## Output Enable Clarification

OE# functionality allows for enabling and disabling individual outputs. OE1# and OE2# are Active LOW inputs. Disabling the outputs may be implemented by deasserting the OE# input pin. If the OE# pin is deasserted, the output of interest will be tri-stated. (The assertion and deassertion of this signal is absolutely asynchronous.)

## OE Deassertion

The impact of deasserting OE# is that each corresponding output will transition from normal operation to tri-state in a glitch-free manner. The maximum latency from the deassertion to tri-stated outputs is between 2–6 DIF clock periods.

## OE Assertion

All differential outputs that were tri-stated will resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2–6 SRC clock periods. In addition, SRC clocks will be driven high within 15 ns of OE# assertion to a voltage greater than 200 mV

**Table 2. OE Functionality**

| OE# | SRC,SRC#  |
|-----|-----------|
| 0   | Enable    |
| 1   | Tri-State |

## Absolute Maximum Conditions

| Parameter          | Description                                       | Condition                   | Min. | Max.                  | Unit |
|--------------------|---------------------------------------------------|-----------------------------|------|-----------------------|------|
| VDD                | Core Supply Voltage                               |                             | –0.5 | 4.6                   | V    |
| VDDA               | Analog Supply Voltage                             |                             | –0.5 | 4.6                   | V    |
| V <sub>IN</sub>    | Input Voltage                                     | Relative to V <sub>SS</sub> | –0.5 | V <sub>DD</sub> + 0.5 | VDC  |
| T <sub>S</sub>     | Temperature, Storage                              | Non-functional              | –65  | +150                  | °C   |
| T <sub>A</sub>     | Temperature, Operating Ambient (Commercial Grade) | Functional                  | 0    | 85                    | °C   |
| T <sub>A</sub>     | Temperature, Operating Ambient (Industrial Grade) | Functional                  | –40  | 85                    | °C   |
| T <sub>J</sub>     | Temperature, Junction                             | Functional                  |      | 150                   | °C   |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model)                 | JEDEC (JESD 22 - A114)      | 2000 | –                     | V    |
| UL-94              | Flammability Rating                               | UL (Class)                  | V–0  |                       |      |

## DC Electrical Specifications

| Parameter           | Description                | Condition                                                                  | Min.                  | Max.                  | Unit |
|---------------------|----------------------------|----------------------------------------------------------------------------|-----------------------|-----------------------|------|
| VDDA, VDD           | 3.3V Operating Voltage     | 3.3 ± 5%                                                                   | 3.135                 | 3.465                 | V    |
| V <sub>IL</sub>     | 3.3V Input Low Voltage     |                                                                            | V <sub>SS</sub> – 0.5 | 0.8                   | V    |
| V <sub>IH</sub>     | 3.3V Input High Voltage    |                                                                            | 2.0                   | V <sub>DD</sub> + 0.5 | V    |
| I <sub>IL</sub>     | Input Low Leakage Current  | except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>   | –5                    |                       | μA   |
| I <sub>IH</sub>     | Input High Leakage Current | except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub> |                       | 5                     | μA   |
| C <sub>IN</sub>     | Input Pin Capacitance      |                                                                            | 1.5                   | 5                     | pF   |
| C <sub>OUT</sub>    | Output Pin Capacitance     |                                                                            | –                     | 6                     | pF   |
| L <sub>IN</sub>     | Pin Inductance             |                                                                            | –                     | 7                     | nH   |
| I <sub>DD3.3V</sub> | Dynamic Supply Current     | At max. load, Full Active, at 100MHz                                       | –                     | 60                    | mA   |

**AC Electrical Specifications**

All measurements at VDD (typical) = 3.3V, T<sub>A</sub> = 25°C unless otherwise stated

| Parameter                        | Description                                | Condition                                                                                             | Min.   | Max.                    | Unit |
|----------------------------------|--------------------------------------------|-------------------------------------------------------------------------------------------------------|--------|-------------------------|------|
| <b>SRCIN at 0.7V</b>             |                                            |                                                                                                       |        |                         |      |
| T <sub>PERIOD</sub>              | Average Period                             | Measured at crossing point V <sub>OX</sub>                                                            | 9.9970 | 10.0533                 | ns   |
| T <sub>ABSMIN-IN</sub>           | Absolute minimum clock periods             | Measured at crossing point V <sub>OX</sub>                                                            | 9.8720 |                         | ns   |
| T <sub>R</sub> / T <sub>F</sub>  | SRC and SRC# Rise and Fall Times           | Single ended measurement: V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V (Averaged)              | 0.6    | 4                       | V/ns |
| V <sub>IH</sub>                  | Differential Input High Voltage            |                                                                                                       | 150    |                         | mV   |
| V <sub>IL</sub>                  | Differential Input Low Voltage             |                                                                                                       |        | -150                    | mV   |
| V <sub>OX</sub>                  | Crossing Point Voltage at 0.7V Swing       | Single-ended measurement                                                                              | 250    | 550                     | mV   |
| ΔV <sub>OX</sub>                 | Vcross Variation over all edges            | Single-ended measurement                                                                              |        | 140                     | mV   |
| V <sub>RB</sub>                  | Differential Ringback Voltage              |                                                                                                       | -100   | 100                     | mV   |
| T <sub>STABLE</sub>              | Time before ringback allowed               |                                                                                                       | 500    |                         | ps   |
| V <sub>MAX</sub>                 | Absolute maximum input voltage             |                                                                                                       |        | 1.15                    | V    |
| V <sub>MIN</sub>                 | Absolute minimum input voltage             |                                                                                                       | -0.3   |                         | V    |
| T <sub>DC</sub>                  | SRC and SRC# Duty Cycle                    | Measured at crossing point V <sub>OX</sub>                                                            | 45     | 55                      | %    |
| T <sub>RFM</sub>                 | Rise/Fall Matching                         | Determined as a fraction of 2*(T <sub>R</sub> - T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> )   | -      | 20                      | %    |
| <b>SRC at 0.7V</b>               |                                            |                                                                                                       |        |                         |      |
| F <sub>IN</sub>                  | Input Frequency                            |                                                                                                       | 90     | 210                     | MHz  |
| F <sub>ERROR</sub>               | Input/Output Frequency Error               |                                                                                                       | -      | 0                       | ppm  |
| T <sub>DC</sub>                  | SRC and SRC# Duty Cycle                    | Measured at crossing point V <sub>OX</sub>                                                            | 45     | 55                      | %    |
| T <sub>PERIOD</sub>              | Average Period                             | Measured at crossing point V <sub>OX</sub> at 100 MHz                                                 | 9.9970 | 10.0533                 | ns   |
| T <sub>R</sub> / T <sub>F</sub>  | SRC[1:2] and SRC[1:2]# Rise and Fall Times | Single-ended measurement: V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V (Averaged)              | 175    | 700                     | ps   |
| T <sub>RFM</sub>                 | Rise/Fall Matching                         | Determined as a fraction of 2 * (T <sub>R</sub> - T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> ) | -      | 20                      | %    |
| ΔT <sub>R</sub> /ΔT <sub>F</sub> | Rise and Fall Time Variation Variation     | Single-ended measurement: V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V (Real Time)             | -      | 125                     | ps   |
| V <sub>HIGH</sub>                | Voltage High                               | Single-ended measurement                                                                              | 660    | 850                     | mv   |
| V <sub>LOW</sub>                 | Voltage Low                                | Single-ended measurement                                                                              | -150   | -                       | mv   |
| V <sub>OX</sub>                  | Crossing Point Voltage at 0.7V Swing       | Single-ended measurement                                                                              | 250    | 550                     | mv   |
| ΔV <sub>OX</sub>                 | Vcross Variation over all edges            | Single-ended measurement                                                                              | -      | 140                     | mV   |
| V <sub>OVS</sub>                 | Maximum Overshoot Voltage                  | Single-ended measurement                                                                              | -      | V <sub>HIGH</sub> + 0.3 | V    |
| V <sub>UDS</sub>                 | Minimum Undershoot Voltage                 | Single-ended measurement                                                                              | -      | -0.3                    | V    |
| V <sub>RB</sub>                  | Ring Back Voltage                          | Single-ended measurement                                                                              | 0.2    | N/A                     | V    |
| T <sub>CCJ</sub>                 | Cycle to Cycle Jitter                      | Jitter is additive                                                                                    | -      | 50                      | ps   |
| T <sub>SKEW</sub>                | Any SRC/SRC# to SRC/SRC# Clock Skew        | Measured at crossing point V <sub>OX</sub>                                                            | -      | 50                      | ps   |
| T <sub>PD</sub>                  | Input to output skew                       | Measured at crossing point V <sub>OX</sub>                                                            | 2.5    | 4.5                     | ns   |

## Test and Measurement Setup

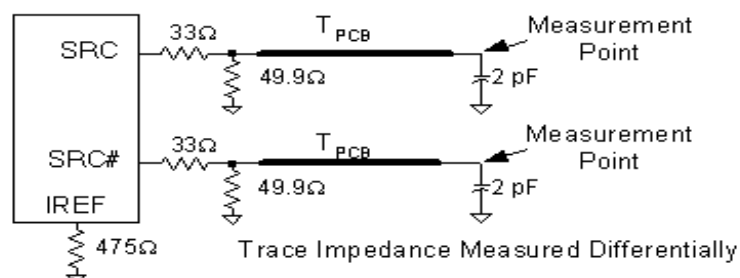


Figure 1. Differential Clock Termination

## Switching Waveforms

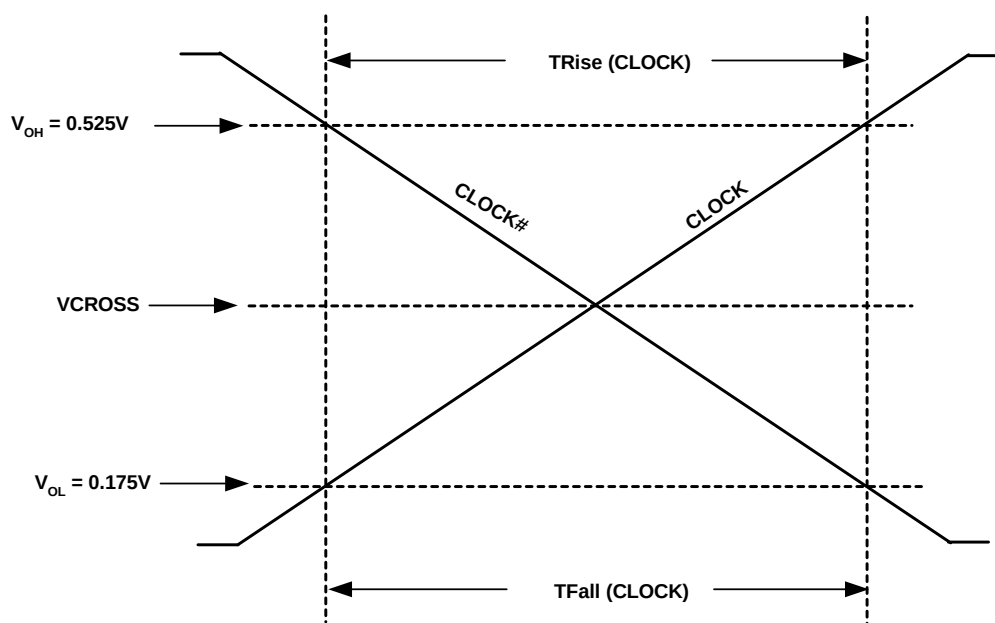


Figure 2. Single-Ended Measurement Points for TRise and TFall

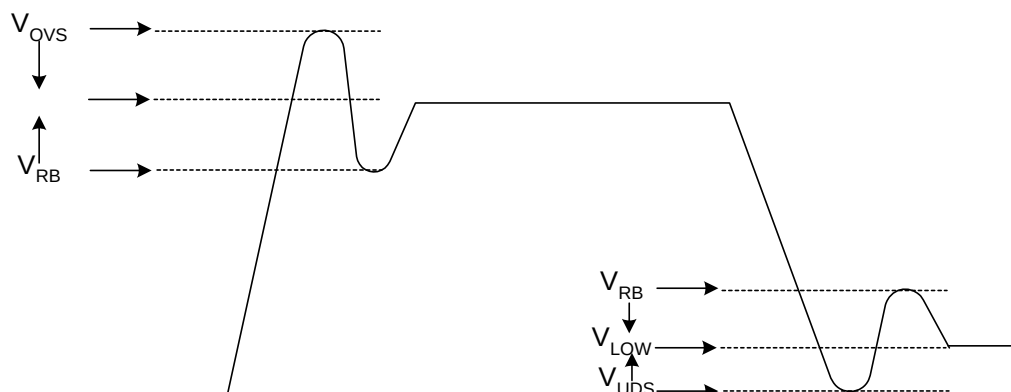


Figure 3. Single-ended Measurement Points for  $V_{OVS}$ ,  $V_{UBS}$  and  $V_{RB}$

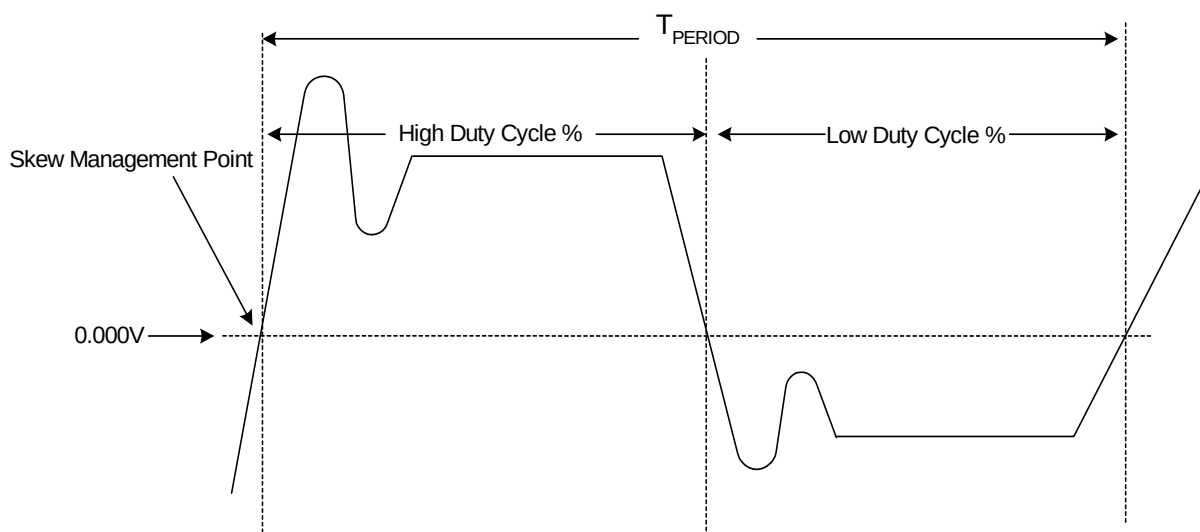


Figure 4. Differential (Clock-Clock#) Measurement Points (Tperiod, Duty Cycle and Jitter)

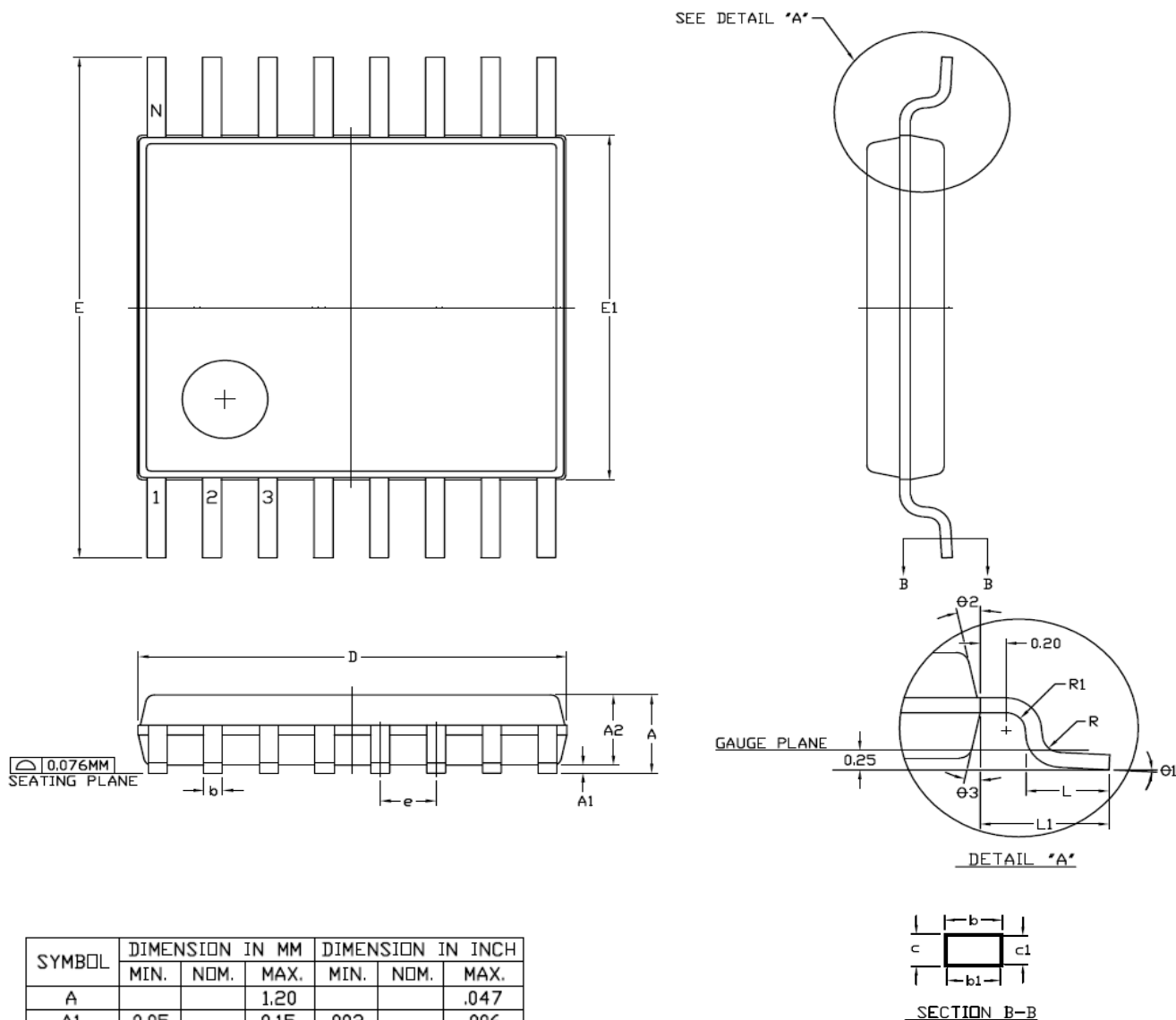
## Ordering Information

| Ordering Code    | Package Type                 | Operating Range           |
|------------------|------------------------------|---------------------------|
| <b>Lead-free</b> |                              |                           |
| SL28DB200AZC     | 16-pin TSSOP                 | Commercial, 0°C to 85°C   |
| SL28DB200AZCT    | 16-pin TSSOP—(Tape and Reel) | Commercial, 0°C to 85°C   |
| SL28DB200AZI     | 16-pin TSSOP                 | Industrial, -40°C to 85°C |
| SL28DB200AZIT    | 16-pin TSSOP—(Tape and Reel) | Industrial, -40°C to 85°C |

Note: All orderables are Lead-free and RoHS compliant

**Package Drawing and Dimensions**

**16-Lead Thin Shrunken Small Outline Package**



**NOTES:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. REFERENCE DRAWING JEDEC MO-153, VARIATION AB.

**Document History Page**

| <b>Document Title: SL28DB200 PCI Express Gen2 and SATA Differential Buffer</b> |             |                   |                        |                                |
|--------------------------------------------------------------------------------|-------------|-------------------|------------------------|--------------------------------|
| <b>Document #: 38-07722 Rev 0.4</b>                                            |             |                   |                        |                                |
| <b>REV.</b>                                                                    | <b>ECR#</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b>   |
| 1.0                                                                            |             | 06/17/10          | TRP                    | Initial Release                |
| AA                                                                             |             | 09/27/10          | TRP                    | Updated Dynamic Supply Current |

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