

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT6323A Programmable ripple counter with oscillator; 3-state

Product specification
Supersedes data of December 1990
File under Integrated Circuits, IC06

September 1993

Programmable ripple counter with oscillator; 3-state

74HC/HCT6323A

FEATURES

- 8-pin space saving package
- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 50 MHz ($V_{CC} = 5\text{ V} \pm 10\%$)
- 3-state output buffer
- Two internal capacitors
- Recommended operating range for use with third overtone crystals 3 to 6 V
- Oscillator stop function ($\overline{MR}$)
- Output capability: bus driver $\rightarrow$ (15 LSTTL)
- I_{CC} category: MSI.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation.

GENERAL DESCRIPTION

The HC/HCT6323A are high-speed Si-gate CMOS devices.

They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT6323A are oscillators designed for quartz crystal combined with a programmable 3-state counter, a 3-state output buffer and an overriding asynchronous master reset ($\overline{MR}$). With the two select inputs S1 and S2 the counter can be switched in the divide-by-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components applied. On-chip

capacitors minimize external component count for third overtone crystal applications.

The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on $\overline{MR}$ resets the counter, stops the oscillator

and sets the output buffer in the 3-state condition. $\overline{MR}$ can be left floating since an internal pull-up resistor will make the $\overline{MR}$ inactive. In the HCT version, the $\overline{MR}$ input and the two mode select pins S1 and S2 are TTL compatible, but the X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC} .

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay X1 to OUT (S1 = S2 = LOW)	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	17	17	ns
f_{max}	maximum clock frequency		90	90	MHz
C_i	input capacitance except X1 and X2		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	+1; notes 1 and 2	54	54	pF
		+2; notes 1 and 2	42	42	pF
		+4; notes 1 and 2	36	36	pF
		+8; notes 1 and 2	33	33	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull-up} \times V_{CC})$$

where:

f_i = input frequency in MHz; f_o = output frequency in MHz.

V_{CC} = supply voltage in V; C_L = output load capacitance in pF.

$I_{pull-up}$ = pull-up currents in μA .

2. For HC and HCT an external clock is applied to X1 with:

$t_r = t_f \leq 6\text{ ns}$, V_i is GND to V_{CC} , $\overline{MR} = \text{HIGH}$

$I_{pull-up}$ is the summation of $-I_i$ (μA) of S1 and S2 inputs at the LOW state.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT6323AD	8	SO	plastic	SOT96

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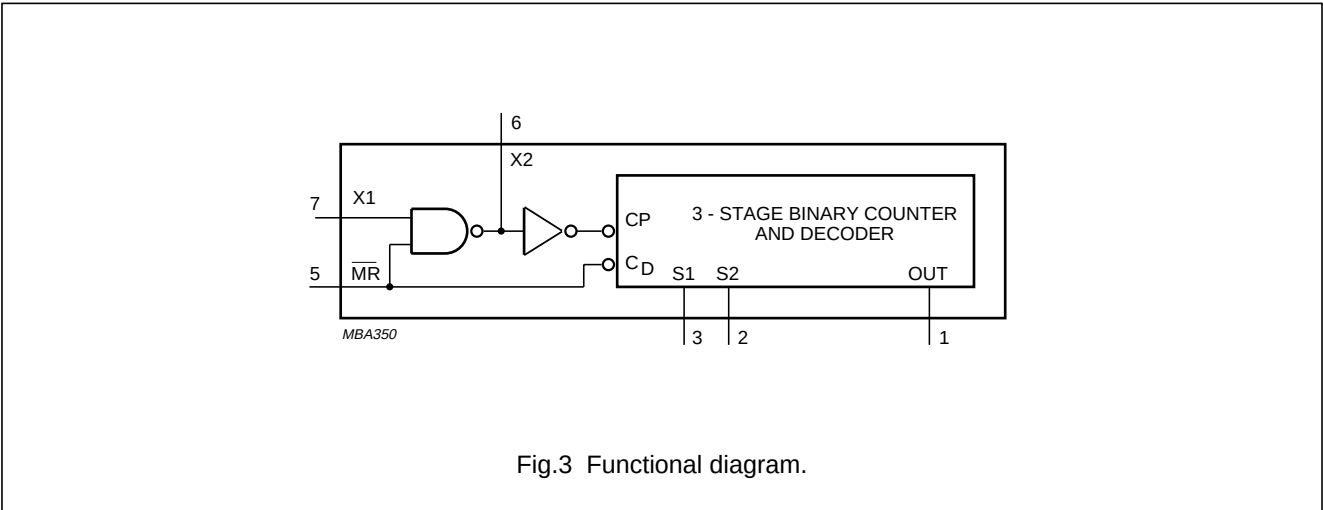
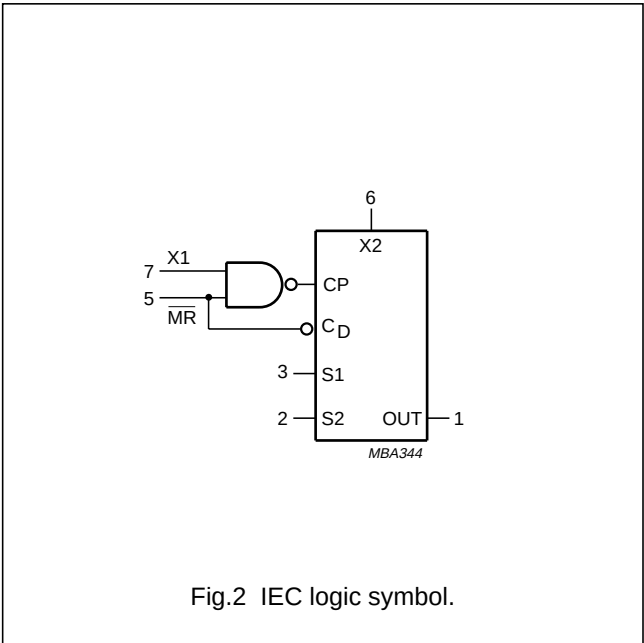
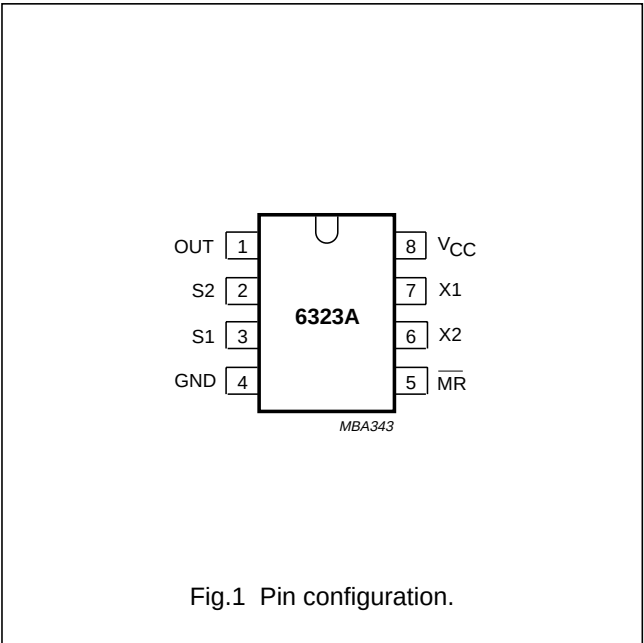
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PINNING

SYMBOL	PIN	DESCRIPTION
OUT	1	counter output
S1 - S2	3, 2	mode select inputs for divide by 1, 2, 4 or 8
GND	4	ground (0 V)
$\overline{\text{MR}}$	5	master reset (active LOW)
X2	6	oscillator pin
X1	7	clock input/oscillator pin
V _{CC}	8	positive supply

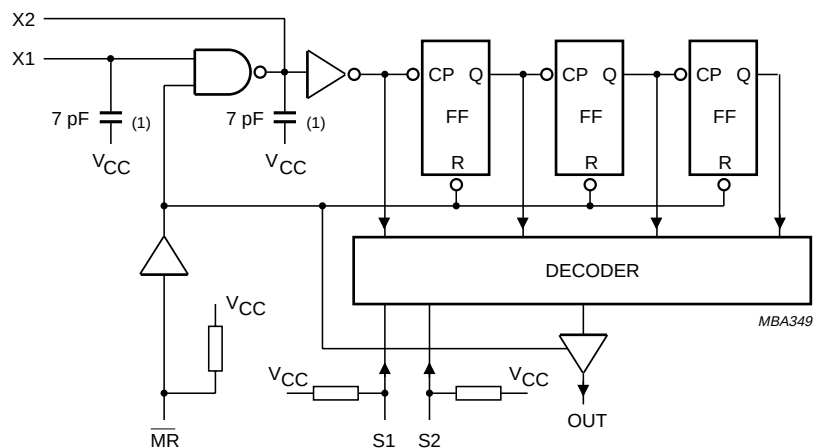
FUNCTION TABLE

INPUTS		OUTPUTS
S1	S2	OUT
0	0	f_i
0	1	$f_i/2$
1	0	$f_i/4$
1	1	$f_i/8$



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Internal capacitors typical 7 pF each. Including stray capacitors on pin X1 and X2, total capacitance will be typical 12 pF per pin.

Fig.4 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: non-standard; bus driver (except for X2)

I_{CC} category: MSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION		
		25			–40 to 85		–40 to 125			V _{CC} (V)	V _I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V _{IH}	HIGH level input voltage MR, X1 input	1.5	1.2	–	1.5	–	1.50	–	V	2.0		
		3.15	2.4	–	3.15	–	3.15	–	V	4.5		
		4.2	3.2	–	4.2	–	4.20	–	V	6.0		
V _{IL}	LOW level input voltage MR, X1 input	–	0.8	0.5	–	0.5	–	0.5	V	2.0		
		–	2.1	1.35	–	1.35	–	1.35	V	4.5		
		–	2.8	1.80	–	1.8	–	1.8	V	6.0		
V _{OH}	HIGH level output voltage X2 output	3.98	–	–	3.84	–	3.7	–	V	4.5	X1 = GND and MR = V _{CC}	I _O = –2.6 mA I _O = –3.3 mA
		5.48	–	–	5.34	–	5.2	–	V	6.0		
		3.98	–	–	3.84	–	3.7	–	V	4.5	X1 = V _{CC} and MR = GND	I _O = –2.6 mA I _O = –3.3 mA
		5.48	–	–	5.34	–	5.2	–	V	6.0		
		1.9	2.0	–	1.9	–	1.9	–	V	2.0	X1 = GND and MR = V _{CC}	–I _O = 20 μA I _O = –20 μA I _O = –20 μA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5		
		5.9	6.0	–	5.9	–	5.9	–	V	6.0		
		1.9	2.0	–	1.9	–	1.9	–	V	2.0	X1 = V _{CC} and MR = GND	I _O = –20 μA I _O = –20 μA I _O = –20 μA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5		
		5.9	6.0	–	5.9	–	5.9	–	V	6.0		
V _{OH}	HIGH level output voltage OUT	1.9	2.0	–	1.9	–	1.9	–	V	2.0	V _{IH} or V _{IL}	I _O = –20 μA I _O = –20 μA I _O = –20 μA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5		
		5.9	6.0	–	5.9	–	5.9	–	V	6.0		
V _{OH}	HIGH level output voltage OUT	3.98	–	–	3.84	–	3.7	–	V	4.5	V _{IH} or V _{IL}	I _O = –6 mA I _O = –7.8 mA
		5.48	–	–	5.34	–	5.2	–	V	6.0		
V _{OL}	LOW level output voltage X2 output	–	–	0.26	–	0.33	–	0.4	V	4.5	X1 = V _{CC} and MR = V _{CC}	I _O = 2.6 mA I _O = 3.3 mA
		–	–	0.26	–	0.33	–	0.4	V	6.0		
		–	0	0.1	–	0.1	–	0.1	V	2.0	X1 = V _{CC} and MR = V _{CC}	I _O = 20 μA I _O = 20 μA I _O = 20 μA
		–	0	0.1	–	0.1	–	0.1	V	4.5		
		–	0	0.1	–	0.1	–	0.1	V	6.0		
V _{OL}	LOW level output voltage OUT	–	0	0.1	–	0.1	–	0.1	V	2.0	V _{IH} or V _{IL}	I _O = 20 μA I _O = 20 μA I _O = 20 μA
		–	0	0.1	–	0.1	–	0.1	V	4.5		
		–	0	0.1	–	0.1	–	0.1	V	6.0		

Programmable ripple counter with oscillator; 3-state

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SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V _{CC} (V)	V _I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V _{OL}	LOW level output voltage OUT	− −	− −	0.26 0.26	− −	0.33 0.33	− −	0.4 0.4	V V	4.5 6.0	V _{IH} or V _{IL}	I _O = 6 mA I _O = 7.8 mA
±I _{LI}	input leakage current X1	−	−	0.1	−	1	−	1	μA	6.0	$\overline{MR} = V_{CC}$ S1 = V _{CC} S2 = V _{CC}	
−I _I	input pull-up current S1, S2 and $\overline{MR}$	5	30	100	−	−	−	−	μA	6.0	GND	see Fig.11 and Fig.12
I _{CC}	quiescent supply current	−	−	8	−	80	−	160	μA	6.0	V _{CC} or GND	I _O = 0

Programmable ripple counter with oscillator; 3-state

74HC/HCT6323A

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V _{CC} (V)	V _I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 1	−	61	185	−	230	−	275	ns	2.0	Fig.7	S1 = GND S2 = GND
		−	22	37	−	46	−	55	ns	4.5		
		−	19	31	−	39	−	47	ns	6.0		
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 2	−	74	235	−	290	−	350	ns	2.0	Fig.7	S1 = GND S2 = V _{CC}
		−	27	47	−	58	−	70	ns	4.5		
		−	23	40	−	49	−	60	ns	6.0		
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 4	−	91	285	−	355	−	425	ns	2.0	Fig.7	S1 = V _{CC} S2 = GND
		−	33	57	−	71	−	85	ns	4.5		
		−	28	48	−	60	−	72	ns	6.0		
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide by 8	−	105	335	−	415	−	500	ns	2.0	Fig.7	S1 = V _{CC} S2 = V _{CC}
		−	38	67	−	83	−	100	ns	4.5		
		−	32	57	−	71	−	85	ns	6.0		
t _{PLZ} /t _{PHZ}	3-state output disable time MR to OUT	−	75	150	−	185	−	225	ns	2.0	Fig.8	
		−	15	30	−	37	−	45	ns	4.5		
		−	13	26	−	31	−	38	ns	6.0		
t _{PZL}	3-state output enable time MR to OUT	−	36	150	−	185	−	225	ns	2.0	Fig.8	
		−	13	30	−	37	−	45	ns	4.5		
		−	11	26	−	31	−	38	ns	6.0		
t _{PZH}	3-state output enable time MR to OUT	−	61	200	−	250	−	300	ns	2.0	Fig.8	note 1
		−	22	40	−	50	−	60	ns	4.5		
		−	19	34	−	43	−	51	ns	6.0		
t _{THL} /t _{TLH}	output transition time	−	14	60	−	75	−	90	ns	2.0	Fig.7	
		−	5	12	−	15	−	19	ns	4.5		
		−	4	10	−	13	−	15	ns	6.0		
t _w	clock pulse width X1, HIGH or LOW	50	17	−	60	−	75	−	ns	2.0	Fig.7	
		10	6.0	−	12	−	15	−	ns	4.5		
		9	5	−	10	−	13	−	ns	6.0		
t _w	master reset pulse width MR; LOW	80	22	−	100	−	120	−	ns	2.0	Fig.9	
		16	8	−	20	−	24	−	ns	4.5		
		14	7	−	17	−	20	−	ns	6.0		
t _{rem}	removal time MR to X1	100	19	−	125	−	150	−	ns	2.0	Fig.9	
		20	7	−	25	−	30	−	ns	4.5		
		17	6.0	−	21	−	26	−	ns	6.0		
f _{max}	maximum clock pulse frequency	10	17	−	8	−	6.6	−	MHz	2.0	Fig.7	
		50	85	−	40	−	33	−	MHz	4.5		
		59	100	−	47	−	39	−	MHz	6.0		

Note to the 74HC AC Characteristics

1. t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (except for X2).

I_{CC} category: MSI.

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V _{CC} (V)	V _I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V _{IH}	HIGH level input voltage MR, S1 and S2 inputs	2.0	—	—	2.0	—	2.0	—	V	4.5 to 5.5		
V _{IL}	LOW level input voltage MR, S1 and S2 inputs	—	—	0.8	—	0.8	—	0.8	V	4.5 to 5.5		
V _{IH}	HIGH level input voltage X1 input	3.15 3.85	— —	— —	3.15 3.85	— —	3.15 3.85	— —	V V	4.5 5.5		
V _{IL}	LOW level input voltage X1 input	— —	— —	1.35 1.65	— —	1.35 1.65	— —	1.35 1.65	V V	4.5 5.5		
V _{OH}	HIGH level output voltage X2 output	3.98	—	—	3.84	—	3.7	—	V	4.5	X1 = GND and MR = V _{CC}	I _O = −2.6 mA
		3.98	—	—	3.84	—	3.7	—	V	4.5	X1 = V _{CC} and MR = GND	I _O = −2.6 mA
		4.4	4.5	—	4.4	—	4.4	—	V	4.5	X1 = GND and MR = V _{CC}	I _O = −20 μA
		4.4	4.5	—	4.4	—	4.4	—	V	4.5	X1 = V _{CC} and MR = GND	I _O = −20 mA
V _{OH}	HIGH level output voltage OUT	4.4	4.5	—	4.4	—	4.4	—	V	4.5	V _{IH} or V _{IL}	I _O = −20 μA
V _{OH}	HIGH level output voltage OUT	3.98	—	—	3.84	—	3.7	—	V	4.5	V _{IH} or V _{IL}	I _O = −6 mA

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SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V _{CC} (V)	V _I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V _{OL}	LOW level output voltage X2 output	−	−	0.26	−	0.33	−	0.4	V	4.5	X1 = V _{CC} and $\overline{MR}$ = V _{CC}	I _O = 2.6 mA
		−	0	0.1	−	0.1	−	0.1	V	4.5	X1 = V _{CC} and $\overline{MR}$ = V _{CC}	I _O = 20 μA
V _{OL}	LOW level output voltage OUT	−	0	0.1	−	0.1	−	0.1	V	4.5	V _{IH} or V _{IL}	I _O = 20 μA
V _{OL}	LOW level output voltage OUT	−	−	0.26	−	0.33	−	0.4	V	4.5	V _{IH} or V _{IL}	I _O = 6 mA
±I _{LI}	input leakage current	−	−	0.1	−	1.0	−	1.0	μA	5.5	$\overline{MR}$ = V _{CC} ; S1 = V _{CC} ; S2 = V _{CC}	
−I _I	input pull-up current S1, S2 and $\overline{MR}$	5	25	100	−	−	−	−	μA	5.5	GND	see Fig.11 and Fig.12
I _{CC}	quiescent supply current	−	−	8	−	80	−	160	μA	5.5	V _{CC} or GND	I _O = 0
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1	−	100	360	−	450	−	490	μA	5.5	V _{CC} or GND	other inputs at V _{CC} or GND; I _O = 0; (note 1)

Note to the HCT DC Characteristics

- The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$, S1, S2	0.40

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITION		
		25			−40 to 85		−40 to 125			V _{CC} (V)	V _I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide-by-1	−	24	40	−	50	−	60	ns	4.5	Fig.7	S1 = GND S2 = GND
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide-by-2	−	29	50	−	62	−	75	ns	4.5	Fig.7	S1 = GND S2 = V _{CC}
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide-by-4	−	35	60	−	75	−	90	ns	4.5	Fig.7	S1 = V _{CC} S2 = GND
t _{PHL} /t _{PLH}	propagation delay X1 to OUT divide-by-8	−	40	70	−	87	−	105	ns	4.5	Fig.7	S1 = V _{CC} S2 = V _{CC}
t _{PLZ} /t _{PHZ}	3-state output disable time MR to OUT	−	21	35	−	43	−	52	ns	4.5	Fig.8	
t _{PZ}	3-state output enable time MR to OUT	−	16	30	−	37	−	45	ns	4.5	Fig.8	
t _{PZH}	3-state output enable time MR to OUT	−	22	38	−	47	−	57	ns	4.5	Fig.8	see note 1
t _{THL} /t _{TLH}	output transition time	−	5	12	−	15	−	19	ns	4.5	Fig.7	
t _W	clock pulse width X1, HIGH or LOW	10	6	−	12	−	15	−	ns	4.5	Fig.7	
t _W	master reset pulse width MR; LOW	16	8	−	20	−	24	−	ns	4.5	Fig.9	
t _{rem}	removal time MR to X1	24	12	−	30	−	36	−	ns	4.5	Fig.9	
f _{max}	maximum clock pulse frequency	50	85	−	40	−	33	−	MHz	4.5	Fig.7	

Note to the 74HCT AC Characteristics

1. t_{PZH} only applicable in the divide-by-1 mode and X1 must be HIGH.

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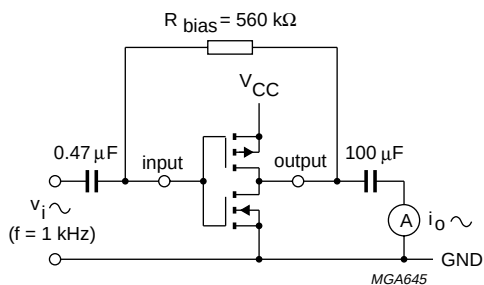


Fig.5 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also Fig.6); MR = HIGH.

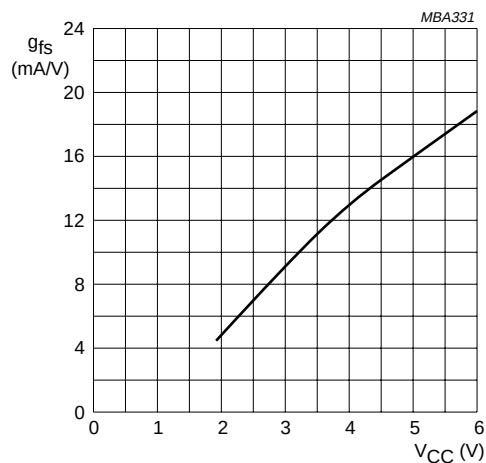
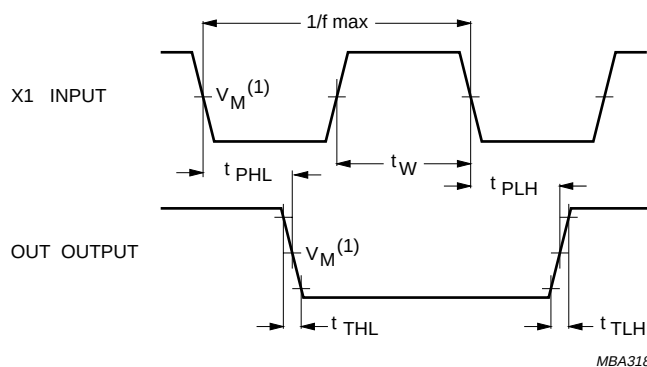


Fig.6 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at $T_{amb} = 25^\circ\text{C}$.

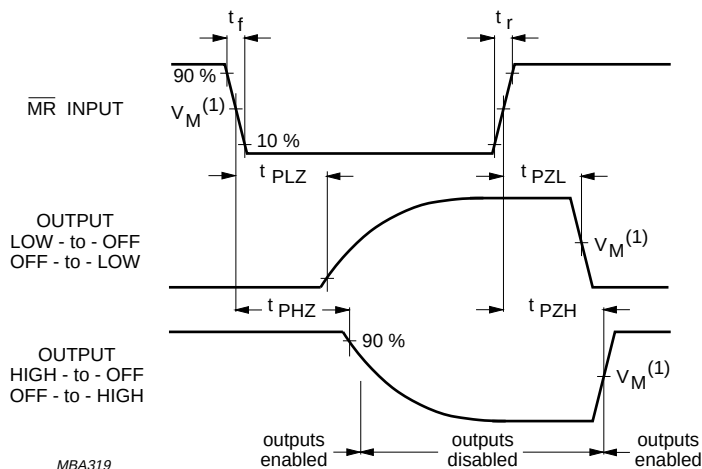


(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3\text{ V}$; $V_I = \text{GND to } 3\text{ V}$.

Fig.7 Waveforms showing the clock (X1) to output (OUT) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

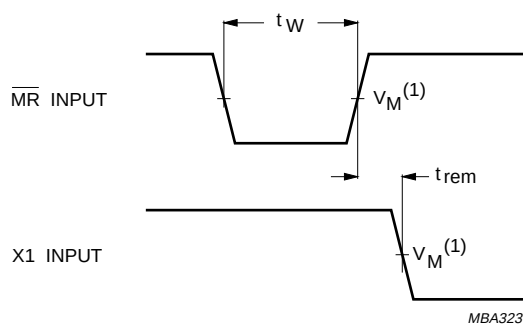
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- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.8 Waveforms showing the input $\overline{\text{MR}}$ to output OUT, 3-state enable and disable times.



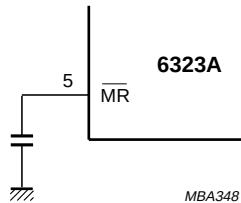
- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.9 Waveforms showing the $\overline{\text{MR}}$ minimum pulse width and $\overline{\text{MR}}$ to X1 removal time.

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APPLICATION INFORMATION



The input pull-up current is used to create a power-on delay time at MR.

Fig.10 Power-on reset.

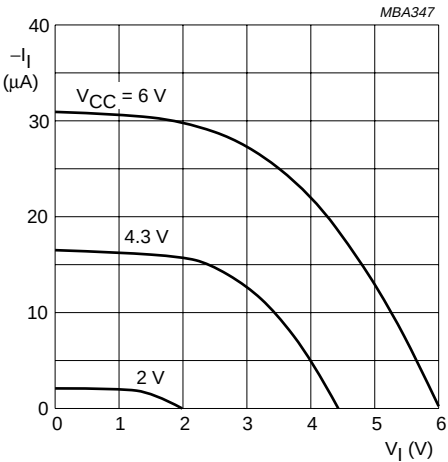


Fig.11 Typical input pull-up current as a function of the input voltage (V_I).

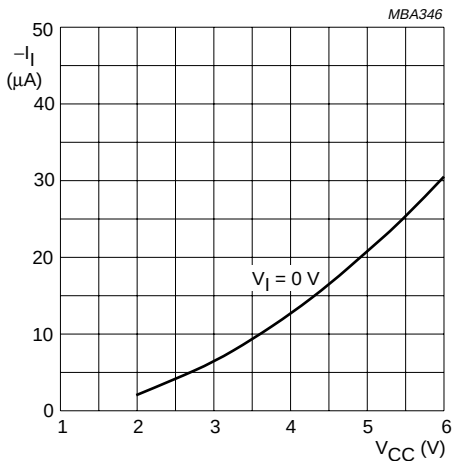


Fig.12 Typical input pull-up current as a function of the supply voltage (V_{CC}).

Table 1 Typical application values

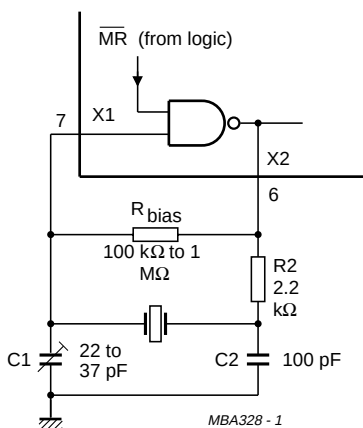
f (MHz)	R2 (k Ω)	C1 (pF)	C2 (pF)
1	4.7	47 to 68	
10	2.2	47 to 68	
25	1	33	33

Table 2 Typical Application Values

f (MHz)	R _{bias} (k Ω)	C1 (pF)
50	3.0	4.7

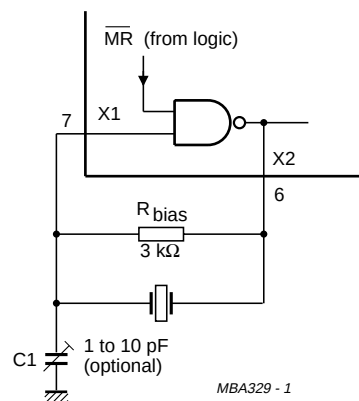
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Above 5 MHz replace R2 by a capacitor of half the value of C2.
 C_L at which a crystal is specified (or adjusted) equals for this application $C1 \cdot C2 / (C1 + C2)$.

Fig.13 Typical setup for a crystal oscillator operating in the fundamental mode (1 MHz to 25 MHz).



Applicable for third overtone crystals (lower damping resistance at the third harmonic frequency) at typical 50 MHz. For lower frequencies extra load capacitors must be supplied, or increase bias resistor.

Fig.14 Typical set-up for a crystal oscillator operating in the third overtone mode without the use of an inductor.

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Typical Crystal Oscillator

In Fig.13, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 k Ω .

The oscillator has been designed to operate over a wide frequency spectrum, for quartz crystals operating in the fundamental mode and in the overtone mode. The circuit is a Pierce type oscillator and requires a minimum of external components. There are two on-chip capacitors, X1 and X2, of approximately 7 pF. Together with the stray and input capacitance the value becomes 12 pF for 8-pin SO packages. These values are convenient and make it possible to run the oscillator in the third overtone without external capacitors applied. If a certain frequency is chosen, the IC parameters, as forward transconductance, and the crystal parameters such as the motional resistances R1 (fundamental), R3 (third overtone) and R5 (fifth overtone), are of paramount importance. Also the values of the external components as R_s (series resistance) and the crystal load capacitances play an important role. Especially in overtone mode oscillations, R_b (bias resistance) and the load capacitance values are very important.

Considerations for Fundamental Oscillator:

In the fundamental oscillator mode, the R_b has only the function of biasing the inverter stage, so that it operates as an amplifier with a phase shift of approximately 180°. The value must be high, i.e. 100 k Ω up to 10 M Ω . The load capacitors C1 and C2, must have a value that is suitable for the crystal being used. The crystal is designed for a certain frequency having a specific load capacitance. C1 can be used to trim the oscillation frequency. The series resistance reduces the total loop gain. One function of it is therefore to reduce the power dissipation in the crystal. R_s also suppresses overtone oscillations and introduces a phase shift over a broad frequency range. This is of less concern provided R_s is not too high a value.

Note

A combination of a small load capacitor value and a small series resistance, may cause a third overtone oscillation.

Considerations for Third-overtone Oscillator:

In the overtone configuration, series resistance is no longer applied. This is essential otherwise the gain for third overtone can be too small for oscillation. A simple solution to suppress the fundamental oscillation, is to spoil the crystal fundamental activity. By dramatically reducing the value of the bias resistor of the inverting stage, and applying small load capacitors, it is possible to have an insufficient phase in the total loop for fundamental oscillation. However the phase for third overtone is good. It can be explained by the R_b $\times$ C_l time constant. During oscillation the crystal with the load capacitors cause a phase shift of 180°. Because R_b is parallel with the crystal (no R_s), R_b spoils the phase for fundamental. R_b $\times$ C_l must be of a value, that it is not spoiling the phase for third overtone too much. Because third overtone is a 3 times higher frequency than the fundamental, the R_b $\times$ C_l cannot 'maintain' the higher third overtone frequency, which results in a less spoiled overtone phase.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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