LOW POWER DISSIPATION ADSL LINE DRIVER

FEATURES

- **Low Power Dissipation Increases ADSL Line Card Density**
- **Low THD of –88 dBc (100-Ω, 1 MHz)**
- **Low MTPR Driving +20 dBm on the Line**
  - **–76 dBc With High Bias Setting**
  - **–74 dBc With Low Bias Setting**
- **Wide Output Swing of 44V_{PP} Differential Into a 200 Ω Differential Load (V_{CC} = ±12 V)**
- **High Output Current of 600 mA (Typ)**
- **Wide Supply Voltage Range of ±5 V to ±15 V**
- **Pin Compatible with EL1503C and EL1508C**
  - **Multiple Package Options**
- **Multiple Power Control Modes**
  - **11 mA/ch Full Bias Mode**
  - **7.5 mA/ch Mid Bias Mode**
  - **4 mA/ch Low Bias Mode**
  - **0.25 mA/ch Shutdown Mode**
  - **I_{ADJ} Pin for User Controlled Bias Current**
  - **Stable Operation Down to 3 mA/ch**
- **Low Noise for Increased Receiver Sensitivity**
  - **3.2 nV/√Hz Voltage Noise**
  - **1.5 pA/√Hz Noninverting Current Noise**
  - **10 pA/√Hz Inverting Current Noise**

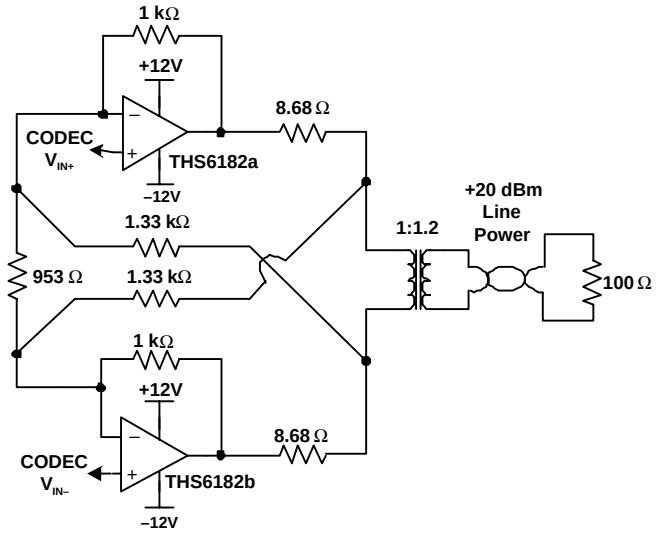
APPLICATIONS

- **Ideal for Full Rate ADSL Applications**

DESCRIPTION

The THS6182 is a current feedback differential line driver ideal for full rate ADSL systems. Its extremely low power dissipation is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique architecture of the THS6182 allows the quiescent current to be much lower than existing line drivers while still achieving very high linearity without the need for excess open loop gain. Fixed multiple bias settings of the amplifiers allow for enhanced power savings for line lengths where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, an I_{ADJ} pin is available to further lower the bias currents while maintaining stable operation with as little as 3 mA per channel. The wide output swing of 44 Vpp differentially with ±12V power supplies allows for more dynamic headroom, keeping distortion at a minimum. With a low 3.2 nV/√Hz voltage noise coupled with a low 10 pA/√Hz inverting current noise, the THS6182 increases the sensitivity of the receive signals, allowing for better margins and reach.

Typical ADSL CO Line Driver Circuit Utilizing Active Impedance



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	T_A	ORDER NUMBER	TRANSPORT MEDIA
THS6182PwP	TSSOP-20 PowerPAD™	PWP–20	THS6182	–40°C to 85°C	THS6182PWP	Tube
					THS6182PWPR	Tape and reel
THS6182RGU	Leadless 24-pin 5,mm x 4, mm PowerPAD™	RGU–24	6182		THS6182RGUR	Tape and reel
THS6182D	SOIC–16	D–16	THS6182		THS6182D	Tube
					THS6832DR	Tape and reel
THS6182DW	SOIC–20	DW–20	THS6182		THS6182DW	Tube
					THS6182DWR	Tape and reel

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	Θ_{JC}	$T_A \le 25°C$ POWER RATING(1)	$T_A = 70°C$ POWER RATING(1)	$T_A = 85°C$ POWER RATING(1)
RGU-24	32°C/W	1.7°C/W	3.28 W	1.87 W	1.41 W
PWP-20	32.6°C/W	1.4°C/W	3.22 W	1.84 W	1.38 W
D-16	62.9°C/W	25.7°C/W	1.67 W	0.95 W	0.72 W
DW-20	45.4°C/W	16.4°C/W	2.31 W	1.32 W	0.99 W

(1) Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		THS6132
Supply voltage, V_{CC}(2)		±16.5 V
Input voltage, V_I		$\pm V_{CC}$
Output current, I_O (2)		1000 mA
Differential input voltage, V_{IO}		±2 V
Maximum junction temperature, T_J (see Dissipation Rating Table for more information)		150°C
Operating free–air temperature, T_A		–40°C to 85°C
Storage temperature, T_{Sgt}		65°C to 150°C
Lead temperature, 1,6 mm (1/16–inch) from case for 10 seconds		300°C
ESD ratings	HBM	1000 V
	CDM	500 V
	MM	200 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The THS6182 may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

PowerPAD is a trademark of Texas Instruments.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}	Dual supply	±5	±12	±15	V
	Single supply	10	24	30	
Operating free-air temperature, T_A		–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 kΩ, Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

NOISE/DISTORTION PERFORMANCE								
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
MTPR	Multitone power ratio		Gain =+9.5, 163 kHz to 1.1 MHz DMT, +20 dBm Line Power, See Figure 1 for circuit			–76		dBc
	Receive band spill-over		Gain =+5, 25 kHz to 138 kHz with MTPR signal applied, See Figure 1 for circuit			–95		dBc
HD	Harmonic distortion, $V_{O(PP)}$ = 2 V		2^{nd} harmonic	Differential load = 200 Ω		–88		dBc
				Differential load = 50 Ω		–70		
			3^{rd} harmonic	Differential load = 200 Ω		–107		dBc
				Differential load = 50 Ω		–84		
V_n	Input voltage noise		V_{CC} = ±5 V, ±12 V, ±15 V, f = 100 kHz			3.2		nV/√Hz
I_n	Input current noise	+Input	V_{CC} = ±5 V, ±12 V, ±15 V, f = 100 kHz			1.5		pA/√Hz
		–Input				10		
	Crosstalk		f = 1 MHz, $V_{O(PP)}$ = 2 V, V_{CC} = ±5 V, ±12 V, ±15 V	R_L = 100 Ω		–65		dBc
				R_L = 25 Ω		–60		dBc
OUTPUT CHARACTERISTICS								
V_O	Single–ended output voltage swing		V_{CC} = ±5 V	R_L = 100 Ω	±3.9	±4.1		V
				R_L = 25 Ω	±3.7	±3.9		
			V_{CC} = ±12 V	R_L = 100 Ω	±10.8	±11.0		V
				R_L = 25 Ω	±10.2	±10.6		
			V_{CC} = ±15 V	R_L = 100 Ω	±13.6	±13.9		V
				R_L = 25 Ω	±12.9	±13.4		
I_O	Output current (1)		R_L = 5 Ω	V_{CC} = ±5 V	±350	±400		mA
			R_L = 10 Ω	V_{CC} = ±12 V	±450	±600		
				V_{CC} = ±15 V	±450	±600		
$I_{(SC)}$	Short-circuit current (1)		R_L = 1 Ω	V_{CC} = ±12 V		1000		mA
	Output resistance		Open-loop			6		Ω
	Output resistance—terminate mode		f = 1 MHz,	Gain = +10		0.05		Ω
	Output resistance—shutdown mode		f = 1 MHz,	Open-loop		8.5		kΩ

(1) A heatsink is rsequired to keep the junction temperature below absoulte maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 kΩ, Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

POWER SUPPLY

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	Dual supply		±4.5	±12	±16.5	V
		Single supply		9.0	24	33	
I_{CC}	Quiescent current (each driver)(1) Full-bias mode (Bias–1 = 0, Bias–2 = 0)	V_{CC} = ± 5 V	T_A = 25°C		8	9	mA
			T_A = full range			10	
		V_{CC} = ± 12 V	T_A = 25°C		11	12	mA
			T_A = full range			12.5	
		V_{CC} = ± 15 V	T_A = 25°C		11.5	12.5	mA
			T_A = full range			13	
	Quiescent current (each driver) Variable bias modes, V_{CC} = ± 12 V	Mid; Bias–1 = 1, Bias–2 = 0			7.5	8.5	mA
		Low; Bias–1 = 0, Bias–2 = 1			4	5	
		Shutdown; Bias–1 = 1, Bias–2 = 1			0.25	0.9	
PSRR	Power supply rejection ratio ($\Delta V_{CC(x)}$ = ± 1 V)	V_{CC} = ± 5 V, ΔV_{CC} = ± 0.5 V	T_A = 25°C	–63	–69		V
			T_A = full range	–60			
		V_{CC} = ±12 V, ±15 V, ΔV_{CC} = ± 1 V	T_A = 25°C	–64	–70		
			T_A = full range	–61			

(1) 0.5 mA flows from V_{CC+} to GND for internal logic control bias.

DYNAMIC PERFORMANCE

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Single-ended small-signal bandwidth (–3 dB), V_O = 0.1 Vrms	R_L = 100 Ω	Gain = +1, RF = 1.2 kΩ		100		MHz
			Gain = +2, RF = 1 kΩ		80		
			Gain = +5, RF = 1 kΩ		35		
			Gain = +10, RF = 1 kΩ		20		
		R_L = 25 Ω	Gain = +1, RF = 1.5k Ω		65		MHz
			Gain = +2, RF = 1 kΩ		60		
			Gain = +5, RF = 1 kΩ		40		
			Gain = +10, RF = 1 kΩ		22		
SR	Single-ended slew-rate(1)	V_O = 10 V_{PP},	Gain =+5		450		V/µs

(2) Slew-rate is defined from the 25% to the 75% output levels

DC PERFORMANCE

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_{CC} = ± 5 V, ±12 V, ±15 V	T_A = 25°C		1	20	mV
			T_A = full range			25	
	Differential offset voltage		T_A = 25°C		0.5	10	
			T_A = full range			15	
	Offset drift		T_A = full range		50		µV/°C
I_{IB}	–Input bias current	V_{CC} = ± 5 V, ±12 V, ±15 V	T_A = 25°C		8	15	µA
			T_A = full range			20	
	+ Input bias current		T_A = 25°C		8	15	
			T_A = full range			20	
Z_{OL}	Open loop transimpedance	R_L = 1 kΩ, V_{CC} = ± 12 V, ±15 V,		450	900		kΩ

ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 kΩ, Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

INPUT CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common–mode voltage range(1)	V_{CC} = ±5 V	T_A = 25°C	±2.7	±3.0		V
			T_A = full range	±2.6			
		V_{CC} = ±12 V	T_A = 25°C	±9.5	±9.8		V
			T_A = full range	±9.3			
		V_{CC} = ±15 V	T_A = 25°C	±12.4	±12.7		V
			T_A = full range	±12.1			
CMRR	Common-mode rejection ratio	$V_{CC(L)}$ = ±5 V, ±6 V	T_A = 25°C	62	72		dB
			T_A = full range	58			
R_I	Input resistance	+ Input			800		kΩ
		– Input			30		Ω
C_I	Input capacitance				1.7		pF

LOCAL CONTROL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Bias pin voltage for logic 1	Relative to GND pin voltage	2.0			V
V_{IL}	Bias pin voltage for logic 0	Relative to GND pin voltage			0.8	V
I_{IH}	Bias pin current for logic 1	V_{IH} = 3.3 V, GND = 0 V		4	30	µA
I_{IL}	Bias pin current for logic 0	V_{IL} = 0.5 V, GND = 0 V		1	10	µA
	Transition time—logic 0 to logic 1(1)			1		µs
	Transition time—logic 1 to logic 0(1)			1		µs

(1) Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final value.

LOGIC TABLE

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers ON with lowest distortion possible (default state)
1	0	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
0	1	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance
1	1	Shutdown mode	Amplifiers OFF and output has high impedance

NOTE: The default state for all logic pins is a logic zero (0).

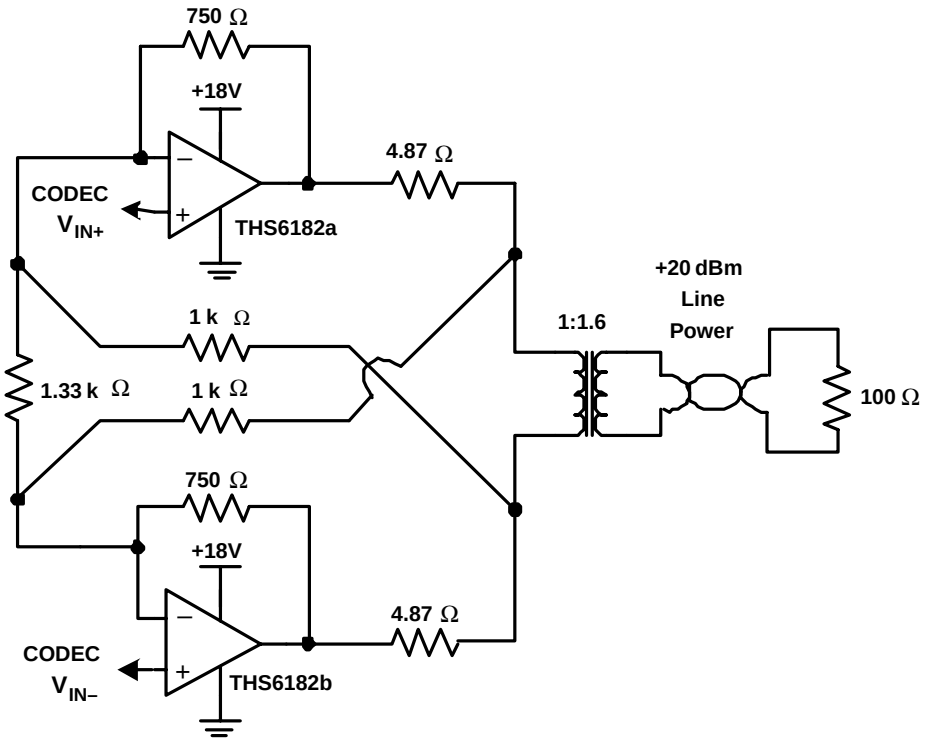
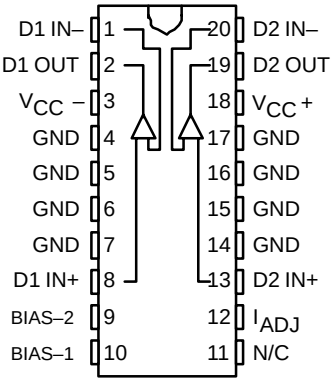


Figure 1. Single-Supply ADSL CO Line Driver Circuit Utilizing Active Impedance (SF = 4)

PIN ASSIGNMENTS

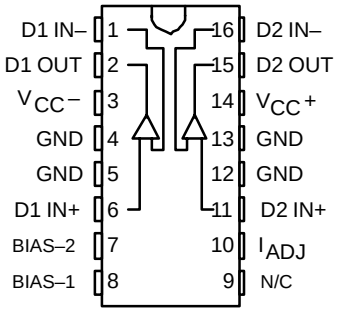
THS6182

TSSOP PowerPAD™ (PWP) and SOIC–20 (DW) PACKAGE(1) (TOP VIEW)

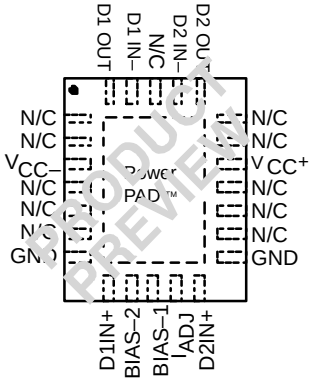


(1) Product preview

THS6182
SOIC–16 (D) PACKAGE (TOP VIEW)



THS6182
Leadless 24–pin PowerPAD™ 5mm X 4mm (RGU) PACKAGE (TOP VIEW)



TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage headroom	vs Output current	2
Common-mode rejection ratio	vs Frequency	3
Crosstalk	vs Frequency	4
Total quiescent current		5
Large signal output amplitude	vs Frequency	6 – 8
Voltage and current noise	vs Frequency	9
Overdrive recovery		10
Power supply rejection ratio	vs Frequency	11
Output amplitude	vs Frequency	12 – 37
Slew rate	vs Output voltage	38
Closed-loop output impedance	vs Frequency	39
Quiescent current	vs Supply voltage	40
Quiescent current	vs Temperature	41
Common-mode rejection ratio	vs Common-mode voltage	42
Input bias current	vs Temperature	43
Input offset voltage	vs Temperature	44
2nd Harmonic distribution	vs Frequency	45 – 52
3rd Harmonic distribution	vs Frequency	53 – 60
2nd Harmonic distribution	vs Output voltage	61 – 64
3rd Harmonic distribution	vs Output voltage	65 – 68

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HEADROOM vs OUTPUT CURRENT

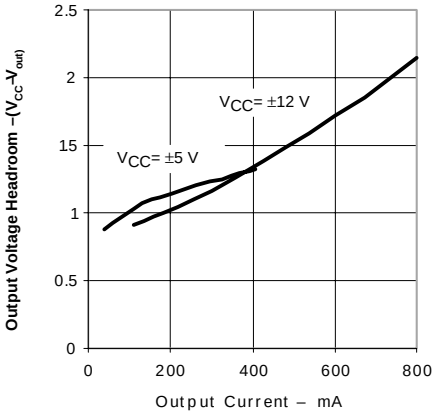


Figure 2

COMMON-MODE REJECTION RATIO vs FREQUENCY

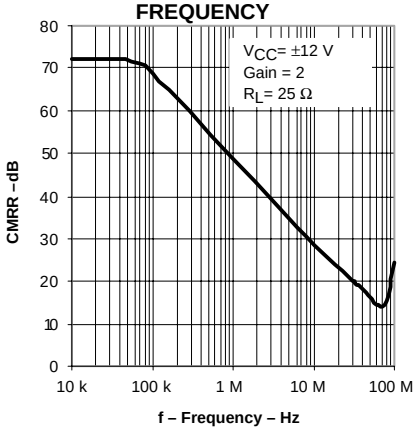


Figure 3

CROSSTALK vs FREQUENCY

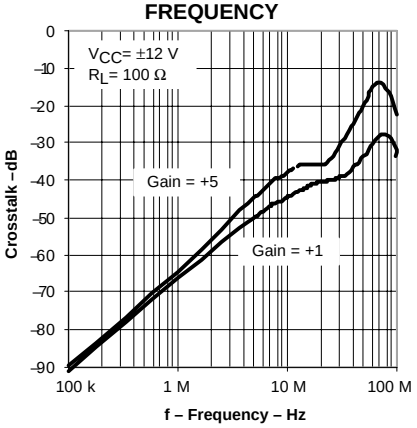


Figure 4

TOTAL QIESCENT CURRENT

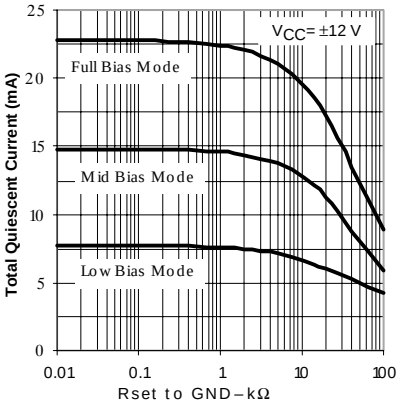


Figure 5

LARGE SIGNAL OUTPUT AMPLITUDE vs FREQUENCY

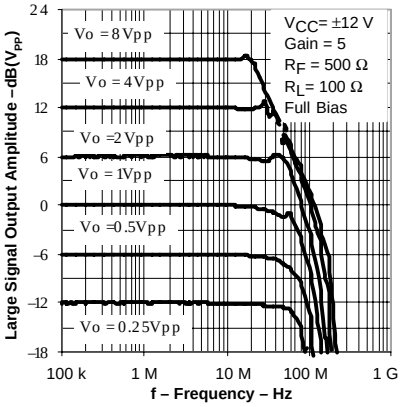


Figure 6

LARGE SIGNAL OUTPUT AMPLITUDE vs FREQUENCY

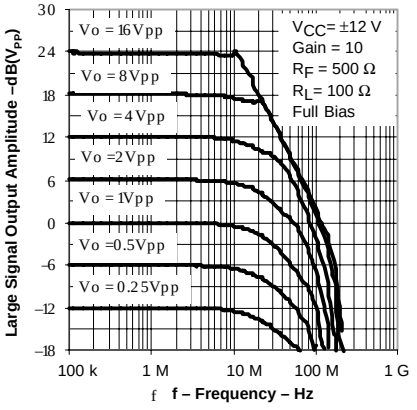


Figure 7

LARGE SIGNAL OUTPUT AMPLITUDE vs FREQUENCY

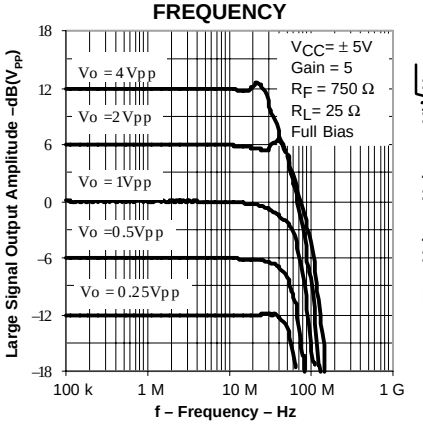


Figure 8

VOLTAGE AND CURRENT NOISE vs FREQUENCY

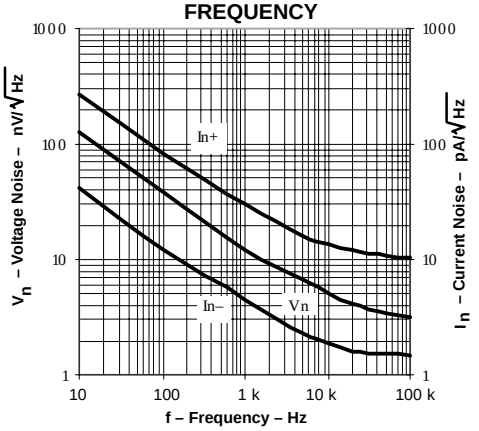


Figure 9

OVERDRIVE RECOVERY

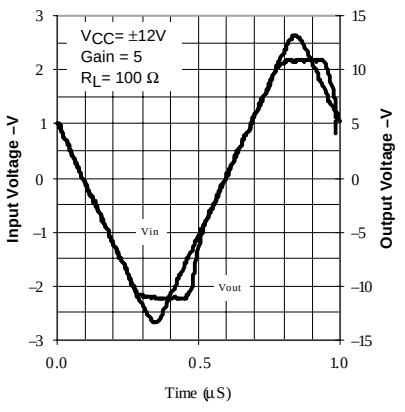


Figure 10

POWER SUPPLY REJECTION RATIO vs FREQUENCY

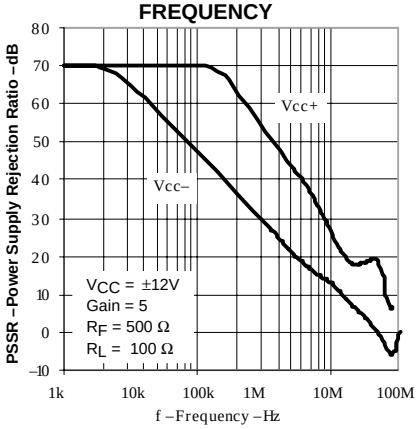


Figure 11

OUTPUT AMPLITUDE vs FREQUENCY

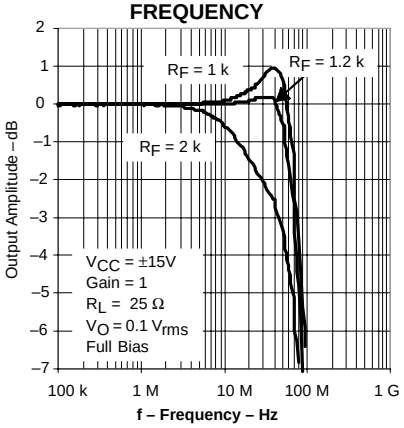


Figure 12

OUTPUT AMPLITUDE vs FREQUENCY

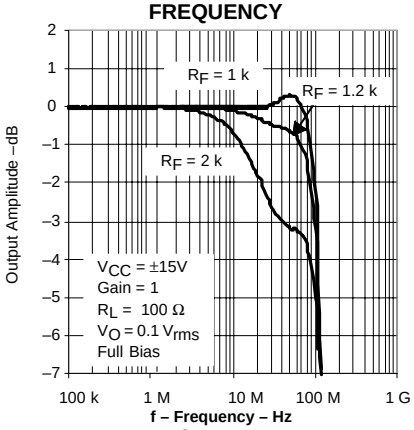


Figure 13

OUTPUT AMPLITUDE vs FREQUENCY

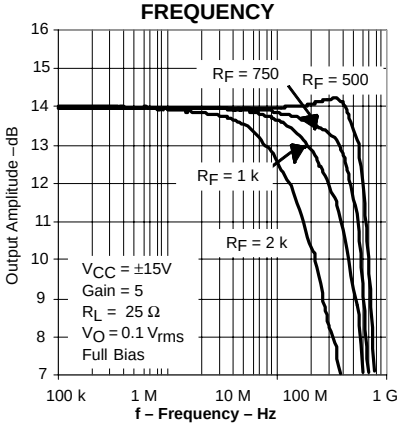


Figure 14

OUTPUT AMPLITUDE vs FREQUENCY

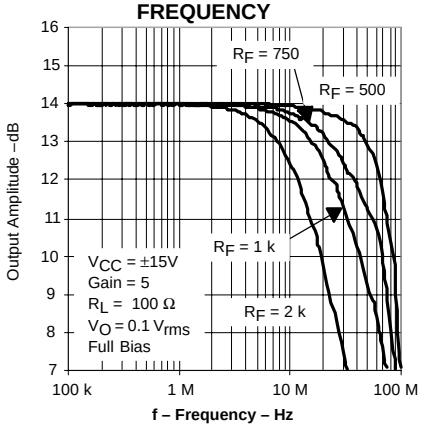


Figure 15

OUTPUT AMPLITUDE vs FREQUENCY

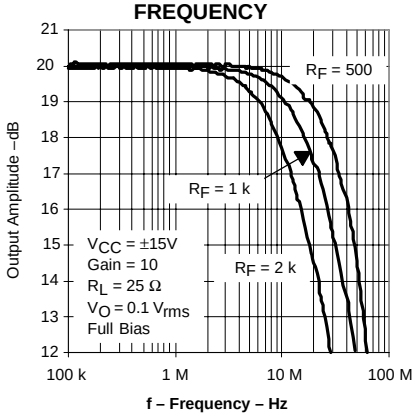


Figure 16

OUTPUT AMPLITUDE vs FREQUENCY

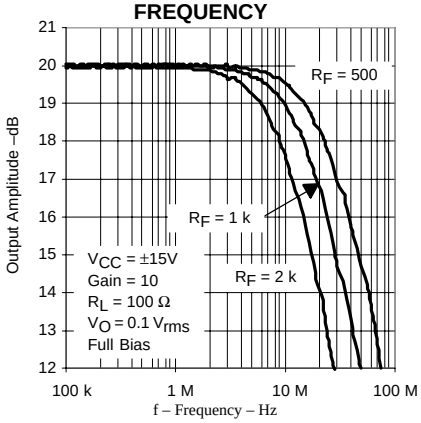


Figure 17

OUTPUT AMPLITUDE vs FREQUENCY

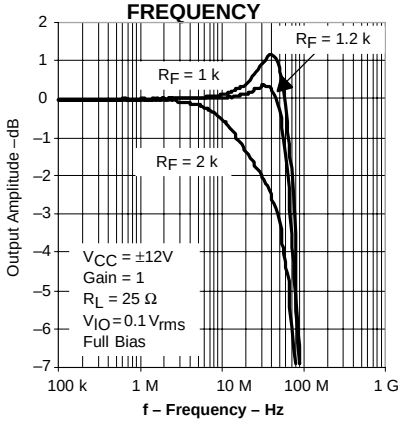


Figure 18

OUTPUT AMPLITUDE vs FREQUENCY

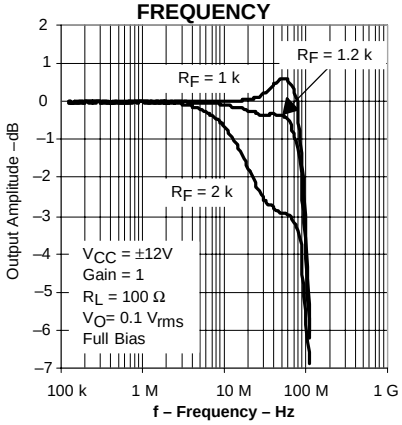


Figure 19

OUTPUT AMPLITUDE vs FREQUENCY

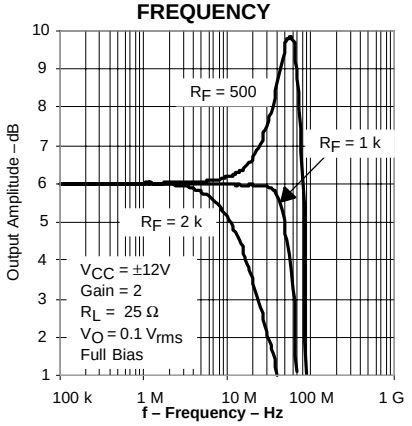


Figure 20

OUTPUT AMPLITUDE vs FREQUENCY

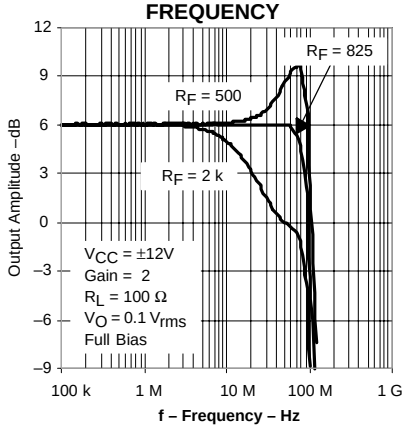


Figure 21

OUTPUT AMPLITUDE vs FREQUENCY

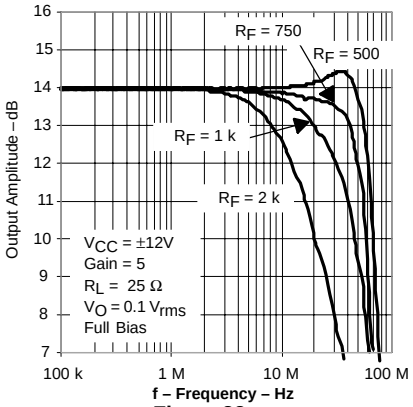


Figure 22

OUTPUT AMPLITUDE vs FREQUENCY

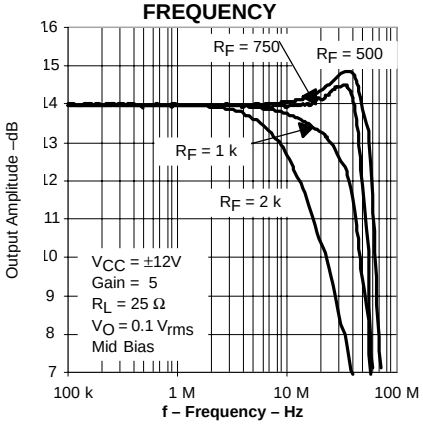


Figure 23

OUTPUT AMPLITUDE vs FREQUENCY

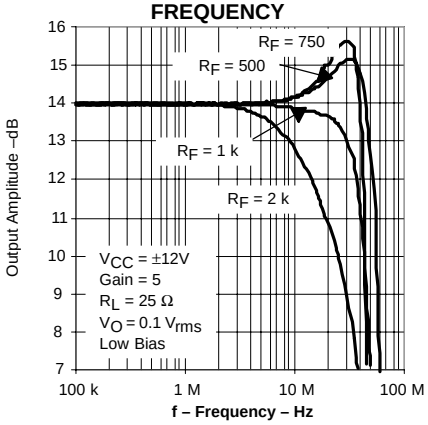


Figure 24

OUTPUT AMPLITUDE vs FREQUENCY

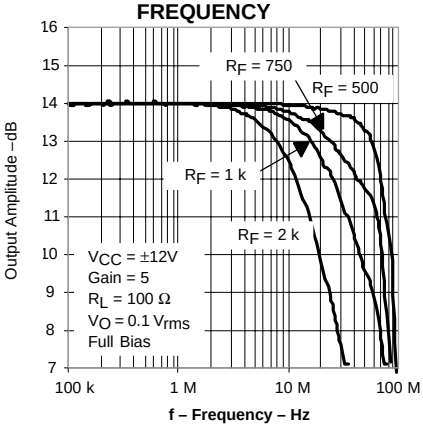


Figure 25

OUTPUT AMPLITUDE vs FREQUENCY

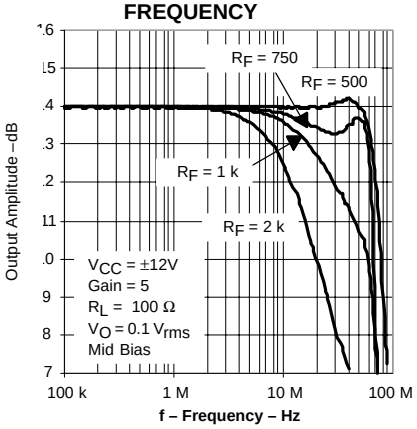


Figure 26

OUTPUT AMPLITUDE vs FREQUENCY

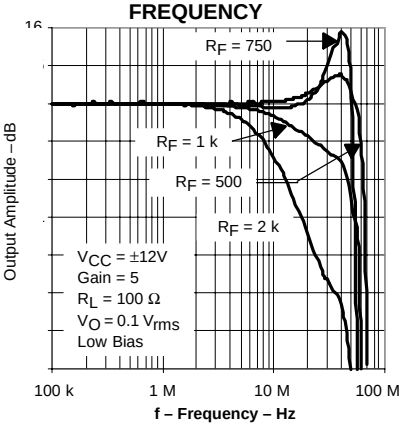


Figure 27

OUTPUT AMPLITUDE vs FREQUENCY

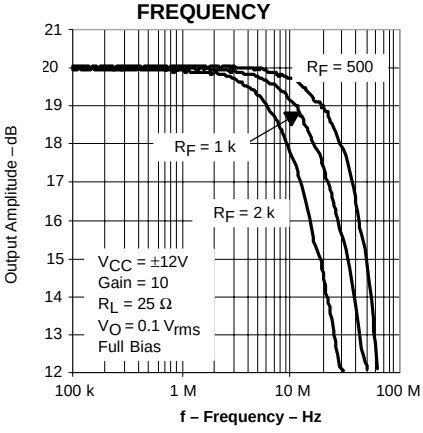


Figure 28

OUTPUT AMPLITUDE vs FREQUENCY

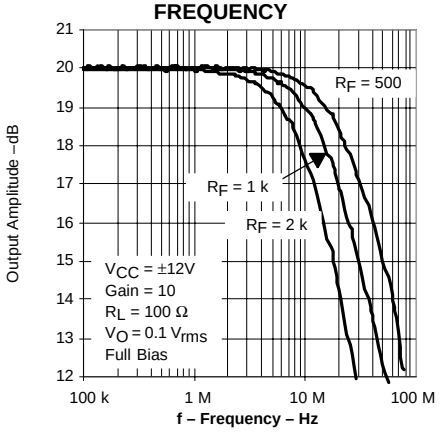


Figure 29

OUTPUT AMPLITUDE vs FREQUENCY

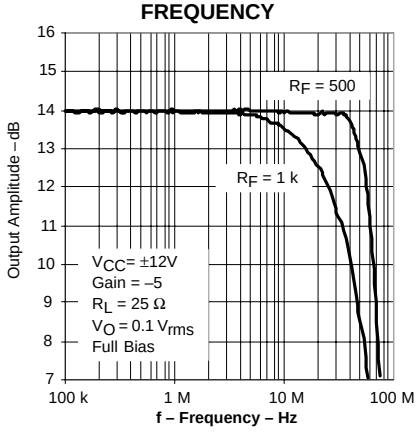


Figure 30

OUTPUT AMPLITUDE vs FREQUENCY

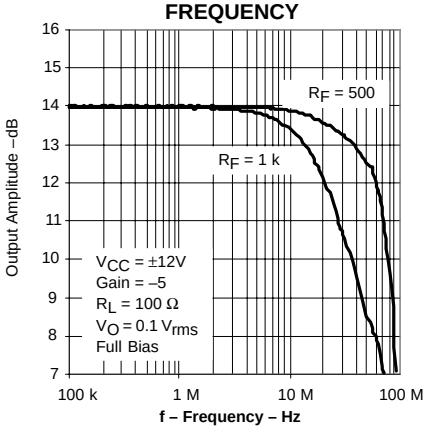


Figure 31

OUTPUT AMPLITUDE vs FREQUENCY

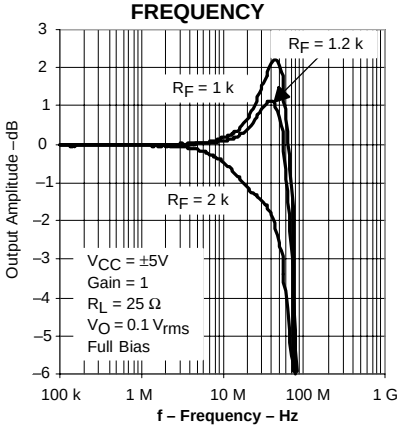


Figure 32

OUTPUT AMPLITUDE vs FREQUENCY

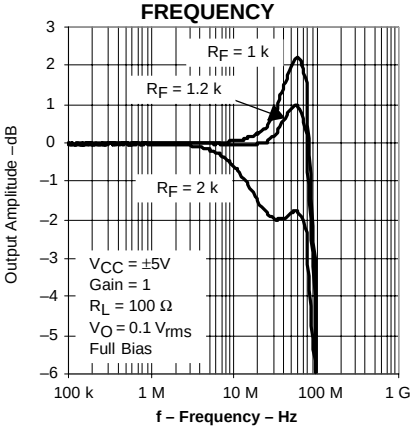


Figure 33

OUTPUT AMPLITUDE vs FREQUENCY

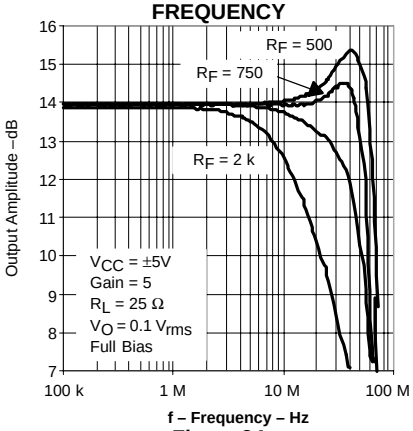


Figure 34

OUTPUT AMPLITUDE vs FREQUENCY

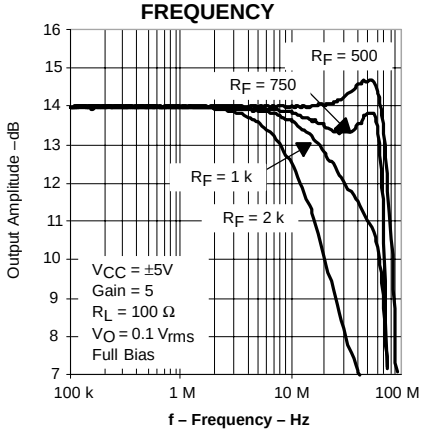


Figure 35

OUTPUT AMPLITUDE vs FREQUENCY

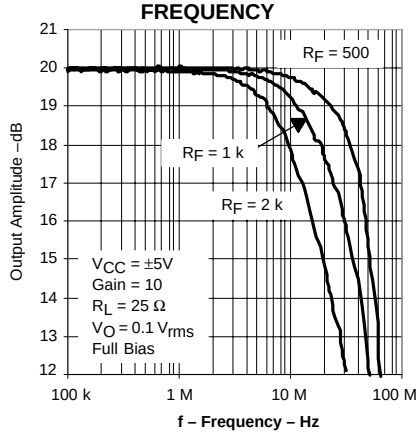


Figure 36

OUTPUT AMPLITUDE vs FREQUENCY

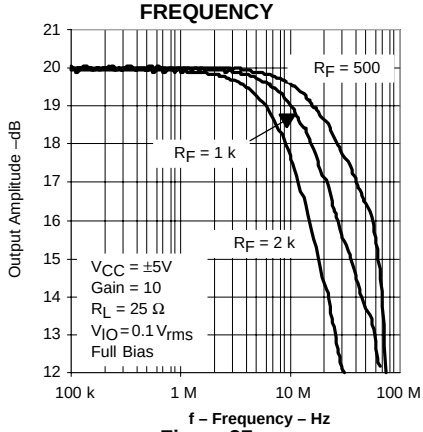


Figure 37

SLEW RATE vs OUTPUT VOLTAGE

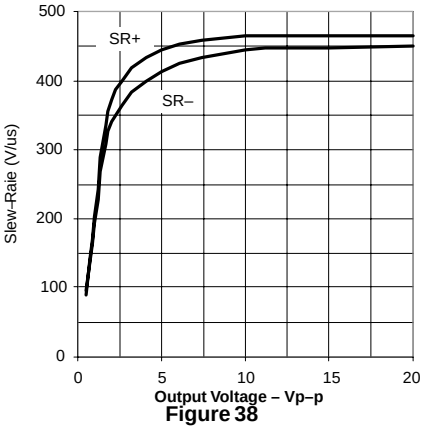


Figure 38

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

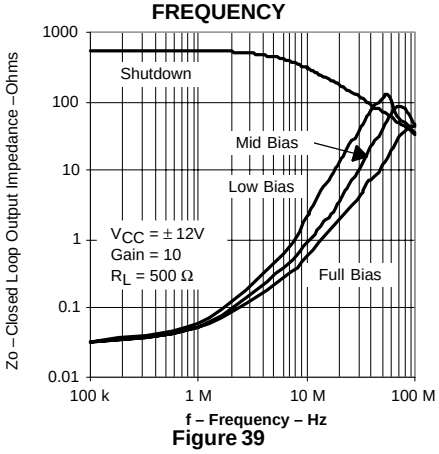


Figure 39

QUIESCENT CURRENT vs SUPPLY VOLTAGE

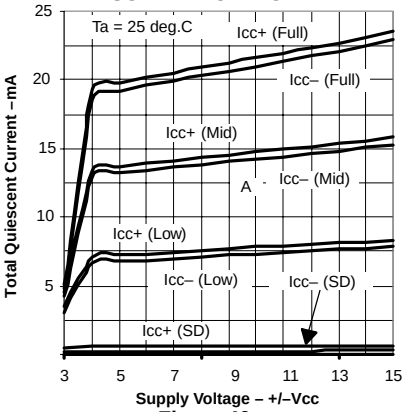


Figure 40

QUIESCENT CURRENT vs TEMPERATURE

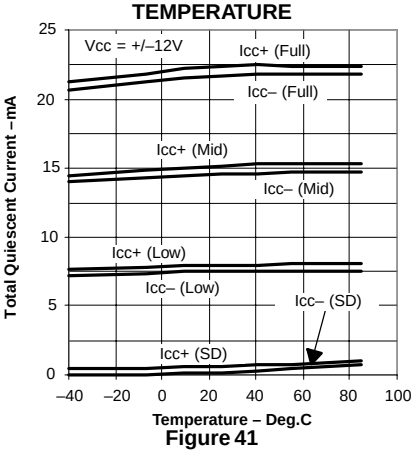


Figure 41

COMMON-MODE REJECTION RATIO vs COMMON-MODE VOLTAGE

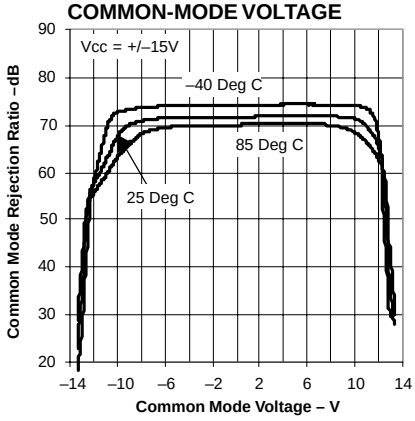


Figure 42

INPUT BIAS CURRENT vs TEMPERATURE

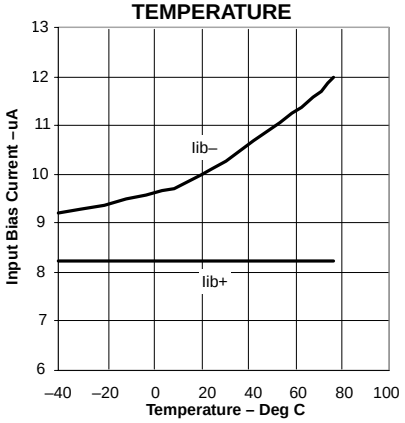


Figure 43

INPUT OFFSET VOLTAGE vs TEMPERATURE

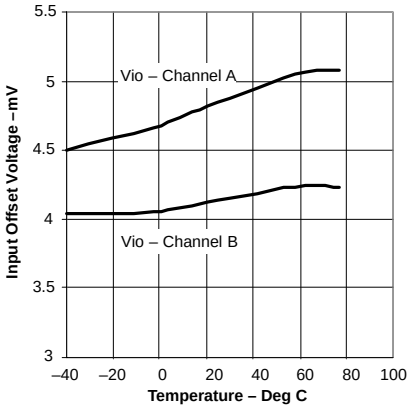


Figure 44

2ND HARMONIC DISTORTION vs FREQUENCY

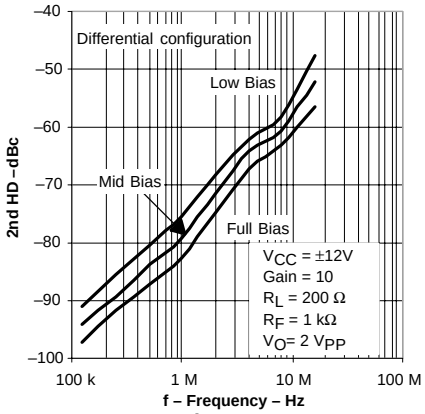


Figure 45

2ND HARMONIC DISTORTION vs FREQUENCY

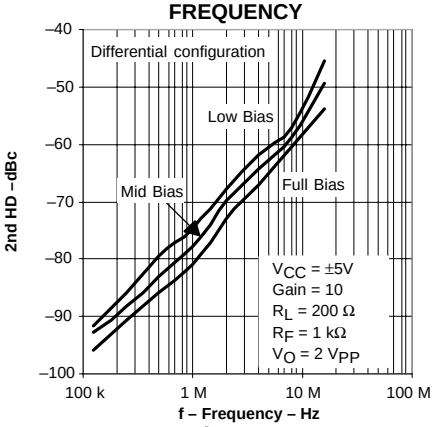


Figure 46

2ND HARMONIC DISTORTION vs FREQUENCY

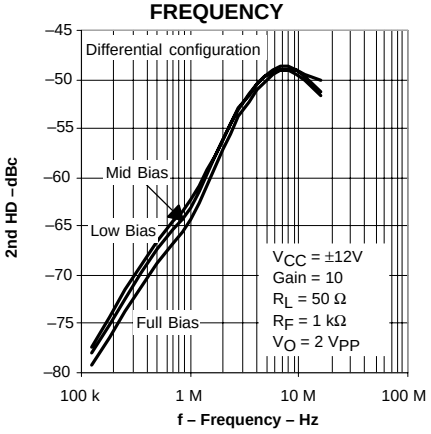


Figure 47

2ND HARMONIC DISTORTION vs FREQUENCY

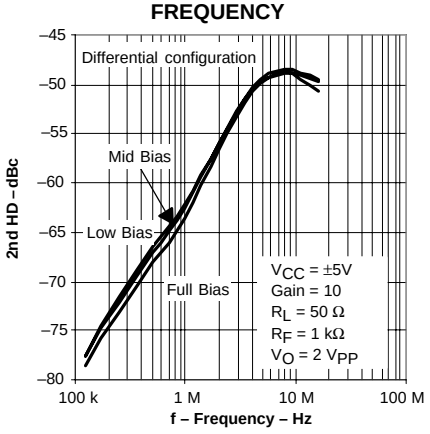


Figure 48

2ND HARMONIC DISTORTION vs FREQUENCY

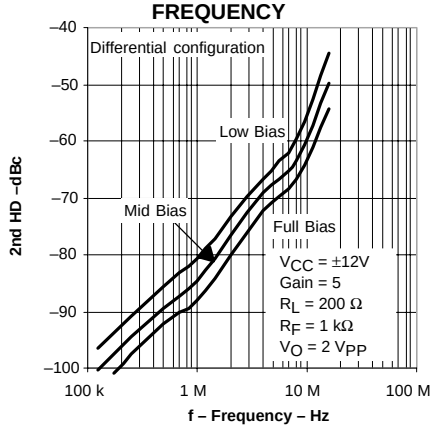


Figure 49

2ND HARMONIC DISTORTION vs FREQUENCY

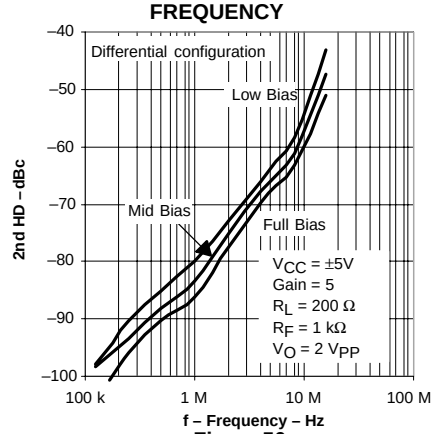


Figure 50

2ND HARMONIC DISTORTION vs FREQUENCY

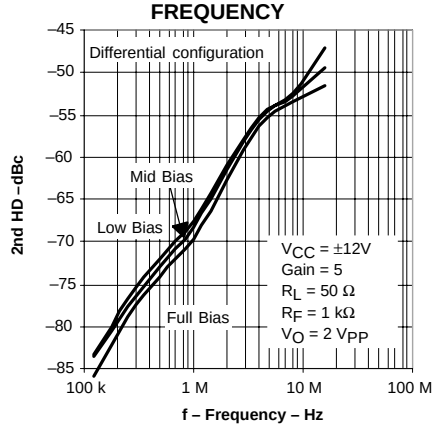


Figure 51

2ND HARMONIC DISTORTION vs FREQUENCY

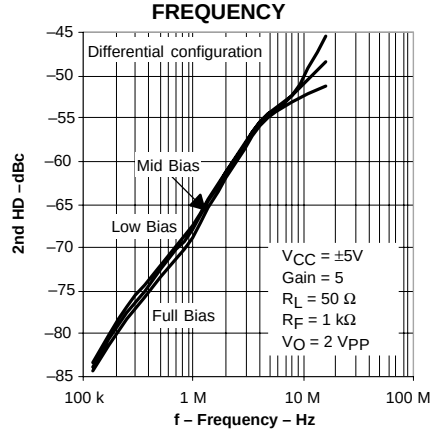


Figure 52

3RD HARMONIC DISTORTION vs FREQUENCY

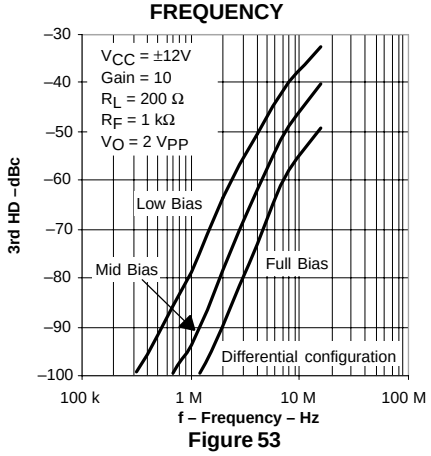


Figure 53

3RD HARMONIC DISTORTION vs FREQUENCY

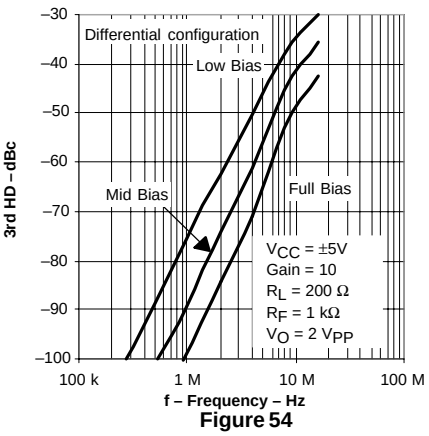


Figure 54

3RD HARMONIC DISTORTION vs FREQUENCY

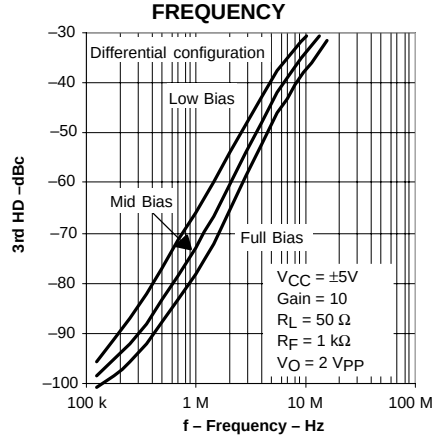


Figure 55

3RD HARMONIC DISTORTION vs FREQUENCY

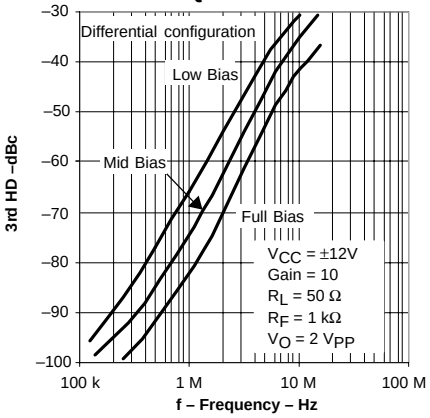


Figure 56

3RD HARMONIC DISTORTION vs FREQUENCY

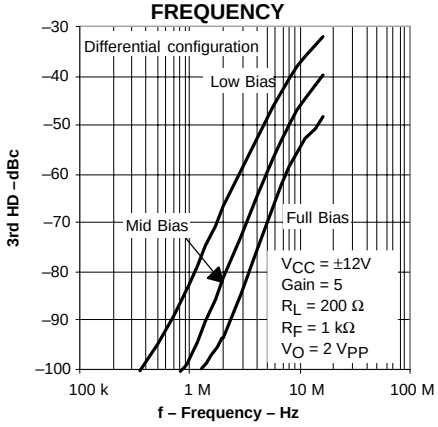


Figure 57

3RD HARMONIC DISTORTION vs FREQUENCY

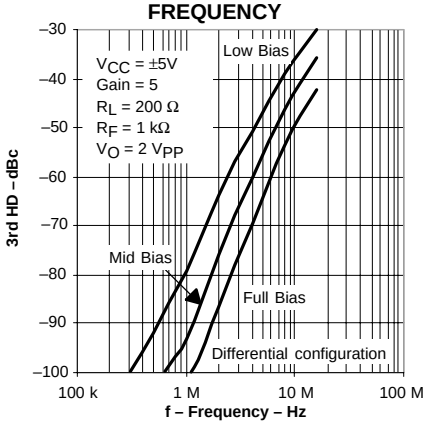


Figure 58

3RD HARMONIC DISTORTION vs FREQUENCY

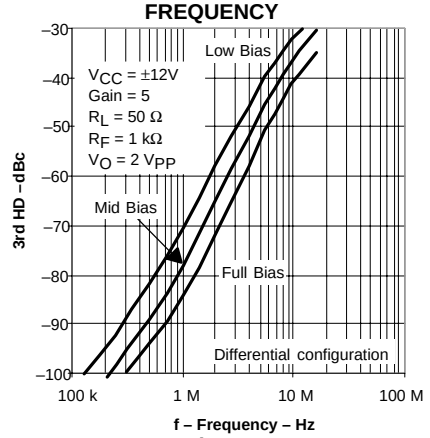


Figure 59

3RD HARMONIC DISTORTION vs FREQUENCY

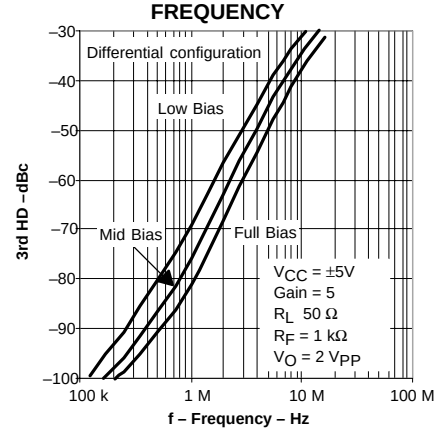


Figure 60

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

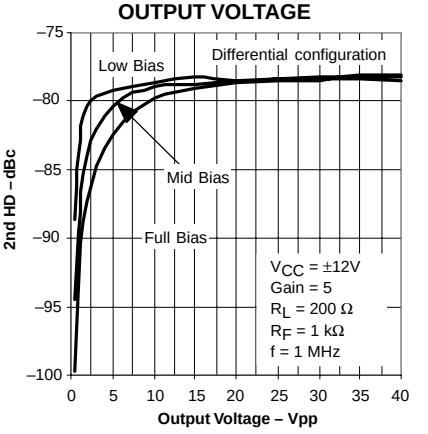


Figure 61

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

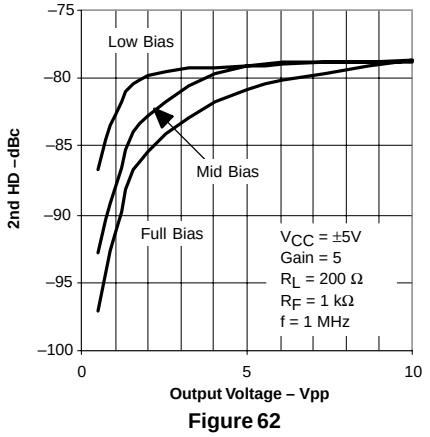


Figure 62

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

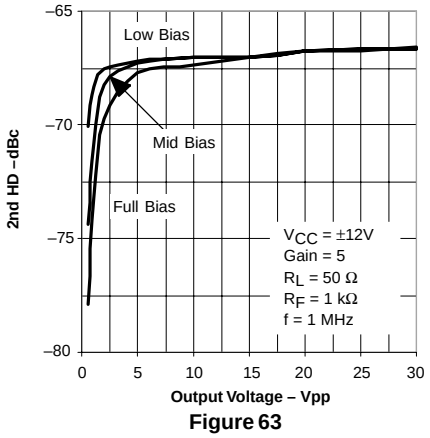


Figure 63

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

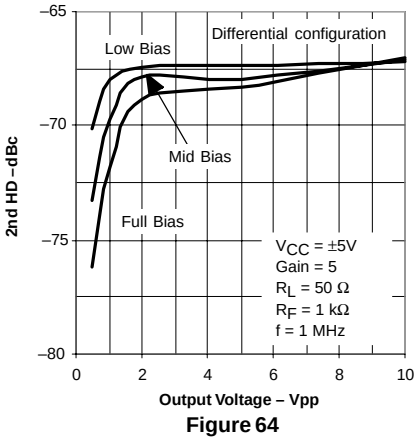


Figure 64

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

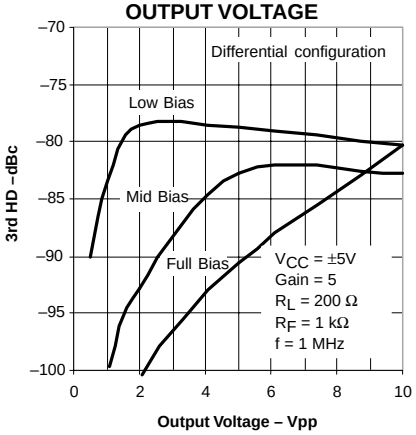


Figure 65

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

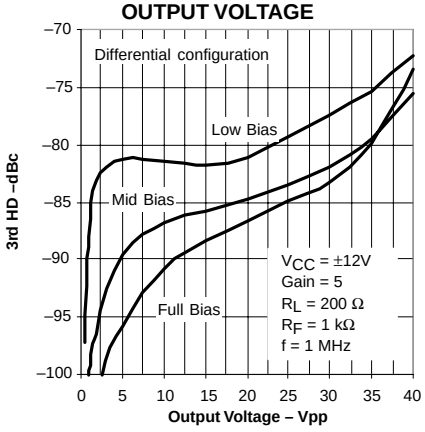


Figure 66

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

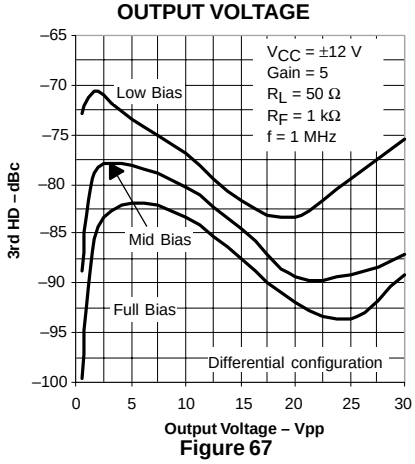


Figure 67

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

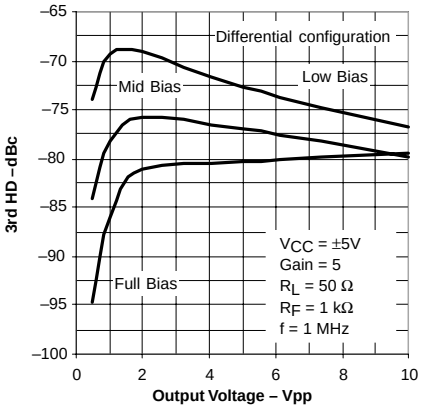
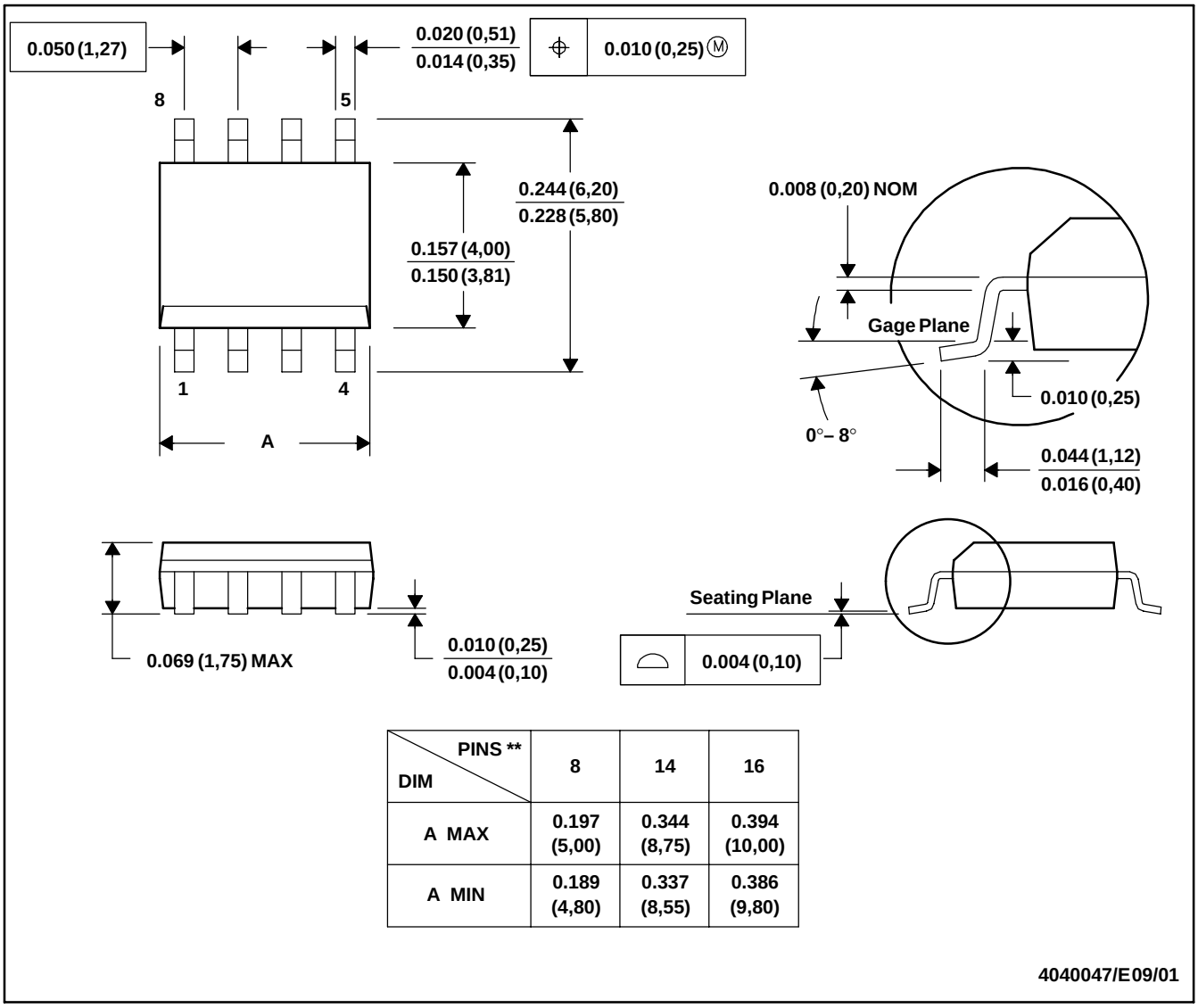


Figure 68

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

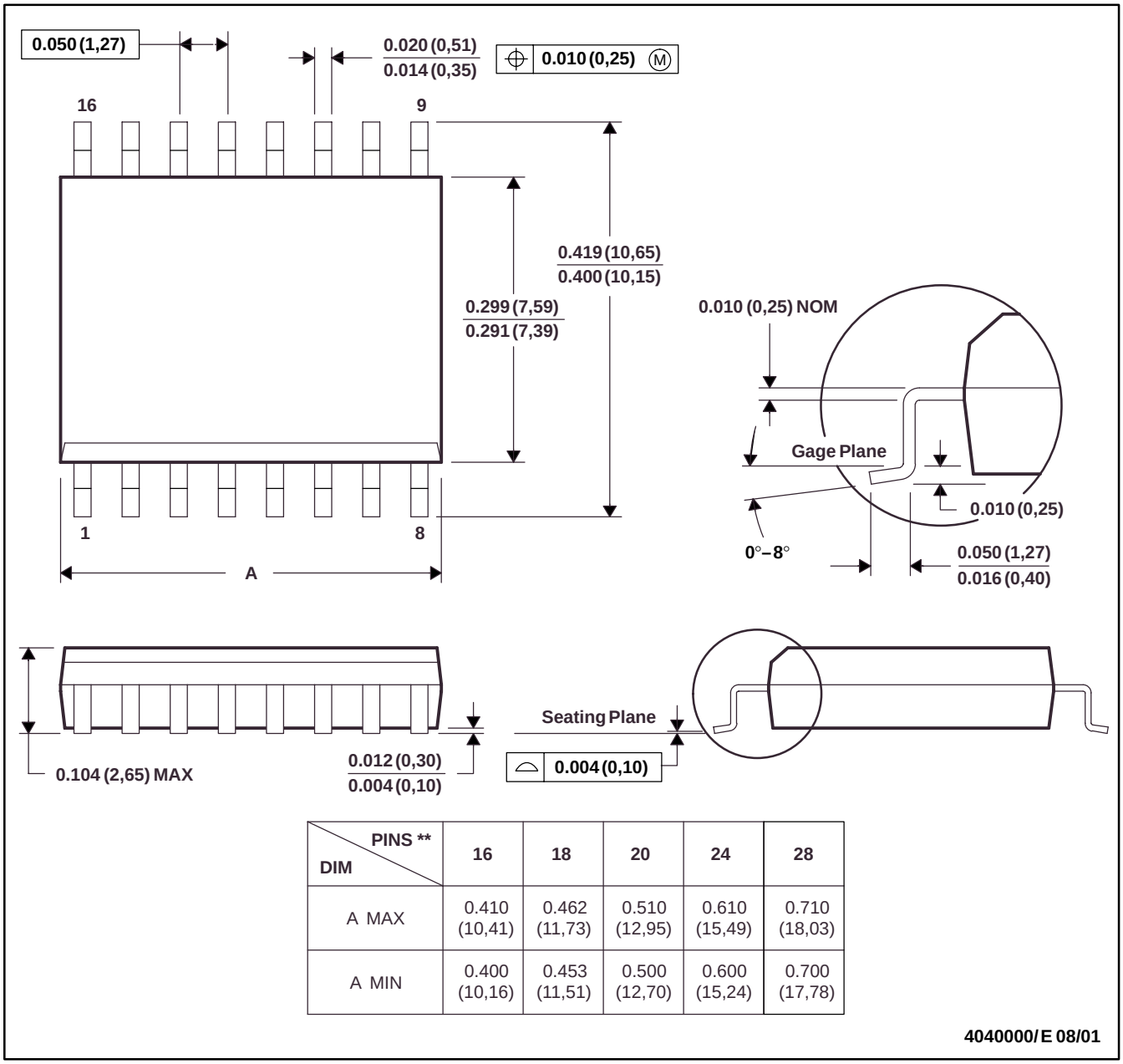
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

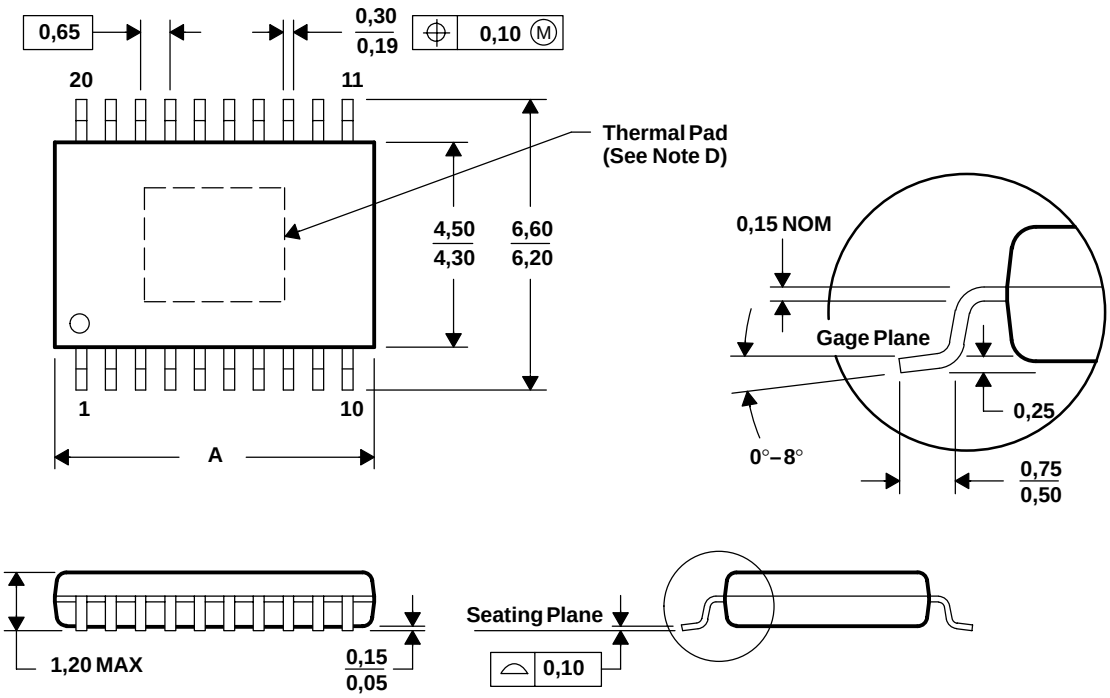
4040000/ E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

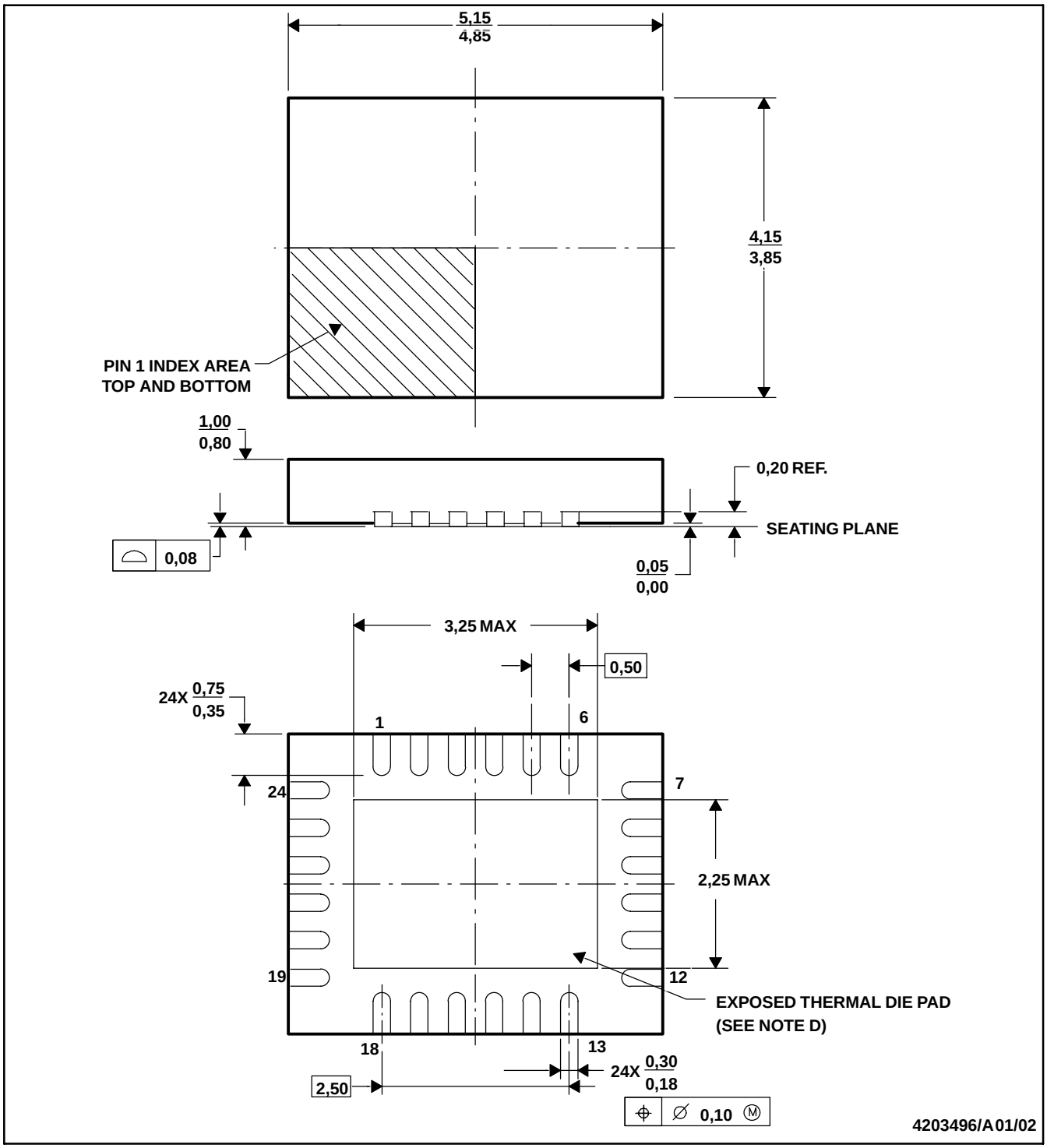
4073225/F10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.

MECHANICAL DATA

RGU (R–PQFP–N24) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Falls within JEDEC MO–220.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265